

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS, LLC,
Petitioner

v.

BESANG INC.,
Patent Owner.

Case No. IPR2023-00900
U.S. Patent No. 7,378,702

**PETITIONER'S REPLY TO
PATENT OWNER'S RESPONSE**

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I. INTRODUCTION

PO boasts that its alleged invention is “paradigm-shifting.” Paper 18 at 1. Yet, BeSang’s founder and the ’702 Patent’s inventor acknowledged that stacked-surrounding gate transistors (S-SGT) were not invented by BeSang, Ex-1042, and were “known for many decades,” Ex-1043, Ex-1046, before the ’702 Patent. *See, e.g.*, Ex-1001, 6:53-55 (“[T]he add-on pillar type SGT structures...may be combined with conventionally processed wafers.”). PO also alleges, “Micron acknowledged this feat of engineering.” Paper 18 at 1. But Micron actually viewed BeSang’s designs as “flawed at a Jr engineering level,” Ex-1044, and “fundamentally flawed.” Ex-1045.

The ’702 Patent is approaching expiration and PO has not provided, nor is BeSang’s expert or Petitioner aware of, any evidence that its allegedly “paradigm-shifting invention” was ever practiced commercially or that any company licensed it. Ex-1051, 118:3-17. Even BeSang’s expert has “no recollection of having heard of BeSang” or the ’702 Patent’s inventor before being retained for this matter, Ex-1051, 117:18-118:2, undercutting BeSang’s grandiose claims of fame.

The alleged weaknesses PO identifies for the prior art are also present in the ’702 Patent. Despite PO’s assertion that “[t]he ’702 Patent told the world how to build its architecture with low-temperature processing and how to align the layers,” Paper 18 at 1, the specification provides little detail on how to fabricate a stacked

device. For example, “[b]oth Dr. Lee and BeSang’s expert Dr. Przybylski agree that transistors are subject to a thermal budget,” *id.*, 2, but the ’702 Patent fails to acknowledge that thermal budget is defined as the product of process temperature *and* process time, and is silent on the duration of its “low temperature processing.” *See generally* Ex-1001; Ex-1041 ¶¶36-40.

Further, the ’702 Patent’s alleged teaching regarding wafer alignment merely identifies several known methods, such as using “a wafer alignment mark,...bump-type alignment structure,” or “simple notch alignment,” without any teaching specific to the alleged invention. Ex-1001, 6:13-23. PO contends that not describing how to precisely align Watanabe’s wafers is “a fundamental flaw,” Paper 18 at 21, while inconsistently arguing that the world would know how to build the alleged invention with nothing more than a mention of known techniques. Ex-1051, 111:19-116:16. Indeed, the ’702 Patent’s disclosure does more to emphasize the difference between the stacking and sequential deposition methods than it does to explain how to properly align the ’702 Patent’s wafers. The ’702 Patent’s disclosure contrasts alignment required for conventional “photolithographic processes” using sequential deposition with those for “combining the SOI layer with a semiconductor substrate” through the stacking method. Ex-1001, 6:13-23.

The ’702 Patent also assumes that a POSITA would know how to apply its teachings to multiple types of memory devices—the same proposition PO rejects for

Watanabe. The '702 Patent applies its teachings to multiple types of memory devices (*i.e.*, DRAM, SRAM, and nonvolatile memory, claimed separately), without disclosing different circuit design techniques, by relying on what was known in the art. *See, e.g.*, Ex-1001, Abstract, 2:4-9, 9:24-35 (“[A] vertical memory cell...could work as a DRAM and/or a nonvolatile memory device....”), 10:29-32. PO's criticisms of the prior art ignore the level of skill in the art by 2004, including well-known teachings on which the '702 Patent relies.

BeSang's expert Dr. Przybylski has done nothing to support the '702 Patent or PO's arguments. He repeatedly refused to testify on anything beyond the written words of his declaration to the point that his declaration and testimony lack credibility. *See, e.g.*, Ex-1051, 50:13-15 (“I've not opined upon that in my report....I can't answer your question specifically.”); *id.* 40:17-25 (“I don't recall having used [that term] and therefore it's not relevant to my opinions in this matter.”); *see id.* 54:6-8, 55:25-56:3, 71:3-5, 80:6-11, 81:21-82:9, 102:22-23, 106:25-107:4, 112:12-13, 114:23-115:2, 115:5-8 (refusing to opine on topics despite appearing in his declaration). Dr. Przybylski's testimony indicates that he had not carefully read the '702 Patent, his declaration, the Board's institution decision, the Petition, or the prior art references because he was unable to answer questions that required more than what was previously written in his declaration. Dr. Przybylski struggled with the concept of a POSITA and even raised a reasonable doubt as to whether he would

constitute a POSITA by the priority date of the '702 Patent. Ex-1051, 25:14-28:4, 108:2-109:24, 113:19-114:7. Just as ALJ Essex previously described Dr. Przybylski in ITC Investigation No. 337-TA-753, here he “was evasive, forgetful, contradictory and offered set statements with no explanation.” Ex-1040, 146; Ex-1051, 118:18-123:13. “He often merely disputed the words on the paper, rather than offering an explanation or argument for the court to consider.” Ex-1040, 144. Where an alleged expert no longer can explain inconsistencies or contradictions, “the witness ceases to act as an expert.” *Id.*; Ex-1051, 123:2-8. That is true of Dr. Przybylski here.

II. CLAIM CONSTRUCTION

A. “stackable add-on layer”

Petitioner agrees in substance with the Board's preliminary construction of “stackable add-on layer,” but Dr. Lee and Petitioner propose a slightly modified construction of “stackable add-on layer” to mean “a layer structure ~~that is~~ formed separately from the substrate ~~and then~~ suitable to be bonded ~~as whole~~ to the dielectric layer positioned above the substrate.” *See* Paper 9 at 9 (differences marked); Ex-2028, 12:18-16:8, 56:12-59:11, 88:8-92:4, 115:1-118:6, 119:18-133:11; Ex-1041 ¶12. Dr. Lee and Petitioner further agree that “stackable add-on layer” should not be read “to include memory cells that are formed by sequential deposition on or above a substrate without being added to a separately formed substrate.” Ex-1002, 13 n.2; Paper 1 at 6 n.2.

The intrinsic record supports the Board's and Petitioner's construction. The plain language of Claim 13 requires "a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells." Ex-1001, 12:29-30. The '702 specification states, "non-volatile memory cells, and similar structures may be formed in a stackable add-on layer for use in *conjunction* with the *separately fabricated* substrate." *Id.* 2:4-9 (emphasis added). "The plurality of vertically oriented semiconductor memory cells can be added to the *separately fabricated* substrate as a thin layer including several doped semiconductor regions," or "[a]lternatively, the plurality of vertically oriented semiconductor memory cells may be completely fabricated prior to attachment." *Id.*, Abstract (emphasis added), 1:47-50. The '702 Patent consistently states that "a stackable add-on layer" is formed separately from the substrate.

Further, as the Board noted, the '702 Patent's definition of "SOI" refers to "a relatively thin, single crystal portion of a semiconductor wafer that can be cleaved and bonded to another *previously fabricated* wafer, or similar type of substrate, such that a three dimensional stack is formed from the SOI layer and the previously fabricated wafer or similar type of substrate." *Id.* 4:47-53 (emphasis added). "[T]he SOI layer may be thought of as an attachment layer, or stackable add-on structure which is *suitable for bonding* to a semiconductor substrate already containing devices and/or interconnections." *Id.* 4:53-57 (emphasis added); *id.* 5:11-17

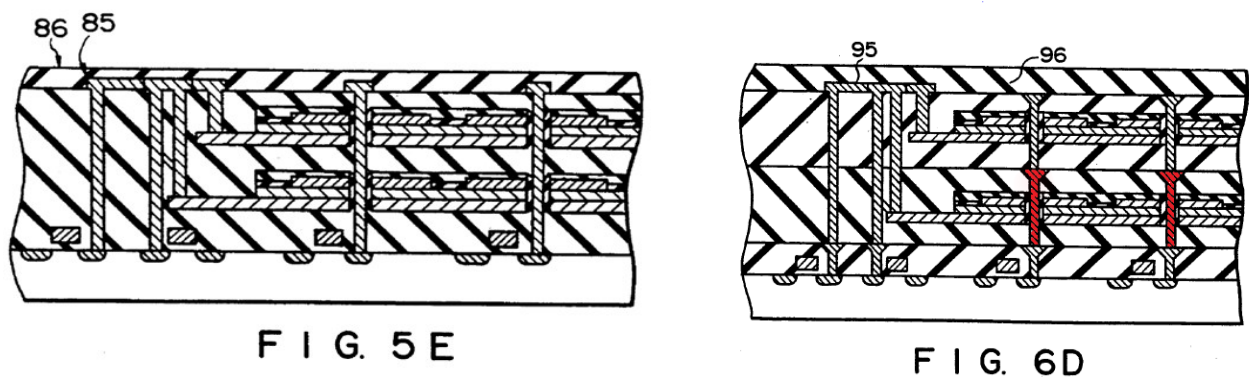
(defining “3D-IC” to include a semiconductor substrate and a stackable add-on layer “stacked and bonded to each other”). Thus, the ’702 Patent states that “a stackable add-on layer” is formed separately from the substrate and then stacked on and bonded to the substrate. Because Dr. Lee and Petitioner’s construction follows the ’702 specification closely, that construction is strongly supported. *See, e.g.*, Ex-1001, Abstract, 1:47-50, 2:4-9, 4:45-5:7, 5:11-17, 12:29-30.

The Board also asked the parties “to explain how a ‘stackable add-on layer’ is structurally distinguishable from a layer that is sequentially deposited.” Paper 9, 9 n.5. Petitioner identifies three structural distinctions between a “stackable add-on layer” and a sequentially-deposited structure.

First, a memory array formed through the stacking method can include “single-crystal silicon in the upper layer[s].” Ex-2028, 141:20-22. Because each layer in the stacking method is processed separately, one can start with monocrystalline silicon for each layer, in which “the speed of the transistor and, therefore, the speed of the circuit might be higher.” *Id.* 141:22-142:2; Ex-1041 ¶¶16-17; *see* Ex-1016, Ex-1028, Ex-1029. By contrast, the sequential deposition method typically deposits polycrystalline silicon by CVD in upper transistors. *See* Ex-1034, 715, Fig. 5. Although polycrystalline silicon can be converted to monocrystalline silicon by heating to high temperatures, processing the upper transistors at high temperatures will cause “dopant diffusion and interfacial oxide growth, which is

detrimental to the characteristics of the transistors.” Ex-2028, 122:19-128:14. Thus, stacking enables one to use single-crystal silicon in the upper layers of the memory array, whereas sequential deposition typically involves forming the upper layers using polycrystalline or amorphous silicon. *Id.*

Second, “the stacking method requires larger contact area” between the interconnects of the stacked layers (compared with sequential deposition), *id.* 142:3-7, because there is a risk of misalignment using the stacking method. Ex-1041 ¶¶18-19; Ex-1034, 714. Misalignment of the cells would lead to larger interconnect resistance and possibly render the device inoperable, so a POSITA designing a memory array using the stacking method would use larger contact areas, such as landing pads. Ex-1041 ¶18; Ex-2029 ¶80. This structural difference is illustrated by comparing Watanabe’s Figs. 5E (sequential deposition) and 6D (stacking) below:



Ex-1005, Figs. 5E, 6D (showing enlarged contact areas as funnel-shaped landing pads annotated in red). BeSang’s expert admitted “[t]he landing pads of the stacking method...have no comparable structures in the figures associated with the

lamination [*i.e.*, sequential deposition] method of Watanabe.” Ex-1051, 87:20-88:24, 85:10-86:19. Larger contact areas mean that “the chip size might be larger and, therefore, the cost per memory cell might be higher and the...overall yield might be degraded.” Ex-2028, 142:3-7, 119:18-121:15; *see* Ex-1033, 0003, Table I.

Third, “there is an interfacial quality concern with the stacking method and not with sequential deposition method.” Ex-2028, 142:8-11. When forming a three-dimensional integrated circuit through the stacking method, the interfaces between stacked layers are more prone to defects. *See id.* 132:3-12. Voids caused by air bubbles in the interface can cause surface roughness that leads to adhesion issues, resulting in weak bonding. *Id.* And “[i]f bonding strength is not good,” “over time, or even after fabrications, the layer might...start peeling off and that affects your yield and that affects your reliability.” *Id.* 131:7-12; *see* Ex-1033, Figs. 1, 9; Ex-1035, 268-71; Ex-1041 ¶¶20-21. Thus, the physical differences in the layer interfaces present another structural distinction between the two approaches.

While PO “disagrees with the Board’s preliminary construction,” PO fails to offer an alternative. Paper 18 at 13. PO also fails to address Dr. Lee’s construction stated during his deposition, Ex-2028, 12:18-16:8, which is consistent with Petitioner’s and the Board’s constructions. Dr. Przybylski also did not offer any opinion on this term. *See generally* Ex-2029; Ex-1051, 30:10-14, 83:3-84:18. Thus, the Board’s and Petitioner’s constructions are un rebutted.

PO's Response seeks to have it both ways on the "stackable add-on layer" term. On one hand, PO argues that its purported invention encompasses sequential deposition because it relates to "*monolithic* 3D memory," Paper 18 at 1 (emphasis added), where PO later relies on Lee's definition of "monolithic" as a structure formed by sequential deposition. Paper 18 at 33-34. On the other hand, PO relies on the Board's construction of "stackable add-on layer" to distinguish Lee (Grounds 3-4) because Lee teaches sequential deposition, not stacking. PO even reaches the legally incorrect conclusion that these grounds did not "survive[] the first stage of this trial." Paper 18 at 49; *cf. SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348 (2018). PO does not dispute that Lee and Watanabe each disclose all elements of at least Claim 13 if the Board were to construe "stackable add-on layer" to encompass sequential deposition. Because PO concedes the term is in controversy, *see* Paper 18 at 13, and advances arguments based on inconsistent interpretations, construction of this term is needed. *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019).

B. "SOI pillar"

The '702 Patent defines "SOI layer" "to refer to a relatively thin, *single crystal portion of a semiconductor wafer* that can be cleaved and bonded to another *previously fabricated wafer, or similar type of substrate.*" Ex-1001, 4:47-53 (emphasis added). "The *transferred*, unpatterned, SOI layer has only a vertically

oriented stack of layers.” *Id.* 6:13-25 (emphasis added). “[A] FLD can be directly contacted by metal electrodes at top, bottom, and intermediate regions of the individual *doped stack structures* (*i.e.*, pillar structures).” *Id.* 6:26-29 (emphasis added). Thus, using the language from the ’702 specification, a “pillar” is a “doped stack structure” and “SOI pillar” means “a doped stack structure formed from a single-crystal portion of a semiconductor wafer transferred from one wafer to another previously fabricated wafer or similar type of substrate.”

Petitioner’s expert Dr. Lee supports this construction in both his supplemental declaration and deposition testimony. Ex-1041 ¶25; Ex-2028, 79:20-80:17, 137:15-140:17. Dr. Lee explained “that nowhere in the ’702 patent when they describe what a pillar is, mention[s] the dimension, whether it’s vertical dimension, horizontal dimension, whether vertical dimension is wider—larger than the horizontal dimensions or vice versa.” Ex-2028, 137:22-138:6. “So, therefore, if a device...is of broad horizontal structure, as long as it is a doped stack structure formed from a single-crystal portion of a semiconductor wafer transferred from one wafer to another previously fabricated wafer, or similar type of substrate, whether it’s broad or narrow...it will still be an SOI pillar.” *Id.* 138:7-15. This is because, by 2004, the horizontal dimension of a memory cell was harder to control during processing than the vertical dimension, which was smaller and easier to control. *See id.* 139:2-140:17.

Dr. Przybylski also conceded, “In general, the vertically oriented collections of doped silicon...Ns, Ps, or N+, P+, constitute SOI pillars.” Ex-1051, 64:3-7. PO’s argument that a “pillar” must be “taller than it is wide,” is not supported by, and conflicts with, record evidence. PO argues that “the aspect ratio of SOI pillar 124” is “‘relatively small’ given its larger height relative to its width.” Paper 18 at 15. Not only is “relatively small” indefinite, but PO’s statement implies that aspect ratio means width/height—it instead means height/width. Ex-1041 ¶26. Under the correct meaning, PO’s construction of “pillar” requires an aspect ratio greater than one, but the ’702 specification expresses a preference for “relatively small” height-to-width ratios. *Id.*; Ex-1001, 9:19-23.

PO’s attempt to rely on proportions shown in the patent figures also fails. “[I]t is well established that patent drawings do not define the precise proportions of the elements....” *See, e.g., Hockerson-Halberstadt v. Avia*, 222 F.3d 951, 956 (Fed. Cir. 2000). The Federal Circuit “has repeatedly cautioned against overreliance on drawings that are neither expressly to scale nor linked to quantitative values in the specification.” *See, e.g., Krippelz v. Ford*, 667 F.3d 1261, 1268 (Fed. Cir. 2012). In addition, both experts agreed that the figures in the ’702 Patent, Lee, and Watanabe should not be presumed to be drawn to scale. Ex-2028, 139:22-140:3; Ex-1051, 54:9-56:3; Ex-2029 ¶80. Although the figures “might [be] draw[n] in such a way that it looks like [the] vertical dimension is larger than [the] horizontal

dimension...the actual reality is that it's reversed. The vertical dimension is smaller than [the] horizontal dimension." Ex-2028, 140:3-9. "Perhaps one reason why they do this is so that they can write n⁺, p, n⁺ within the space that is allowed." *Id.* 140:10-12.

PO's construction is further called into question because Dr. Przybylski refused to provide any meaningful bounds for a "pillar" during his deposition—even when asked whether a *single* doped silicon region (*e.g.*, n⁺ or p) of a memory cell could constitute an SOI pillar (it plainly cannot). Ex-1051, 64:3-67:7, 70:24-71:8, 71:25-72:7, 93:17-96:11. The '702 specification does not provide quantitative guidance to require an "SOI pillar" to be taller than it is wide.

PO cannot identify any intrinsic support for its construction, instead relying on common dictionary definitions outside the field of the relevant technology. As Dr. Lee explained, a POSITA around 2004—when the state-of-art process technology was at the 90-nanometer node—would have understood that the processing limitations in the horizontal direction had dimensions far greater than that in the vertical direction. Ex-1041 ¶29; Ex-2028, 139:2-140:17; *see* Ex-1047, Table 74a; Ex-2022, Table B. In addition to the processing limitations, a POSITA would have understood that a pillar's height is related to the "channel length" of the MOSFET—the most critical dimension of the memory device's function—and that *increasing* the channel length would disadvantage the memory cell. Ex-1041 ¶¶30-

31. Conversely, *reducing* the channel length would offer several advantages. *Id.* ¶32. Thus, a POSITA would not have understood “pillar” to require an aspect ratio greater than one, as such a dimensional requirement would result in inferior devices and conflict with common process technology parameters. *Id.* ¶33.

III. GROUNDS 5-6: CLAIMS 13-17 ARE OBVIOUS OVER LEE IN VIEW OF WATANABE AND FURTHER IN VIEW OF ENDOH

PO does not dispute that Lee, Watanabe, and Endoh disclose all limitations of Claims 13-17 but attacks only the motivations to combine the references and reads the references in ways that would render them inoperable.

A. A POSITA would have been motivated to combine the teachings of Lee and Watanabe and would have had a reasonable expectation of success

PO's argument that one would not apply Watanabe's stacking method to Lee's structure is baseless. Watanabe contemplates both stacking and sequential deposition methods and explains that both approaches may be used to arrange memory cells “three-dimensionally, thereby providing a high integration density.” Ex-1005, 1:49-52. PO tries to distance Watanabe from Lee by arguing that Lee expresses a preference for “monolithic” structures by comparing *three*-dimensional monolithic and *two*-dimensional non-monolithic structures. Ex-1007, 11:24-31. However, as Dr. Lee explained, “A [POSITA] would understand that [a] three-dimensional array, whether you do it monolithically or non-monolithically, in other words, whether you use stacking method or sequential deposition method, would improve the device

density.” Ex-2028, 62:20-63:4. A POSITA would have understood that Lee’s benefits derived from 3-D integration would be obtained if Lee’s memory structures are formed using Watanabe’s alternative stacking method. Ex-1041 ¶34.

Further, PO alleges two obstacles for which there were well-known solutions in the art within the skill of a POSITA by 2004. Ex-1041 ¶35. First, PO argues that Watanabe’s high-temperature bonding would damage Lee’s memory transistors. Paper 18 at 24-27. As both Drs. Lee and Przybylski acknowledge, thermal budget is a measure of both temperature *and time*. Ex-2028, 125:6-14; Ex-2029 ¶71; *see* Ex-1052, 247. A POSITA would have known about bonding techniques consistent with Watanabe’s bonding temperature (*i.e.*, 900-1000°C) that do not exceed the thermal budget and avoid damage to the lower memory cells. Ex-1041 ¶¶35-44; *see* Ex-1053, 15, 17-18, Table 1.

For example, a POSITA would have recognized that electromagnetic induction heating (EMIH) offers “a method of bonding a stack of silicon wafers...in a shorter time period than prior methods” to bond wafers at a high temperature without exceeding the thermal budget and while “limit[ing] both ‘kick-out’ and traditional diffusion processes.” Ex-1048, 1:26-29, 1:40-43, 1:64-67; Ex-1059, 9-10; *see* Ex-1049 (“[H]igher temperature (900°C), but low-thermal budget, rapid thermal annealing...minimize[s] both interfacial and bulk dielectric defects, thereby improving device performance.”); *see also* Ex-1050, 515-16, 519. Because a

POSITA would have understood that EMIH bonds stacked wafers at 900-1000°C while limiting heating time, a POSITA would have known how to perform Watanabe's stacking method without exceeding thermal budget. Ex-1041 ¶¶41-42.

PO's argument also reads Watanabe in such a way as to render it unworkable. PO argues that "repeated baking" is required but that is not so. Paper 18 at 25. A POSITA would have understood that stacked layers in Watanabe can be bonded during a single step. Watanabe's Figure 6C shows two previously fabricated planar members stacked and bonded together with the substrate and peripheral circuit, and describes bonding all three structures during a single bonding step, not separate bonding steps per layer. *See* Ex-1005, 6:6-7.

In addition, a POSITA would have known about several methods of bonding, including EMIH, that allow all levels of the memory array to be bonded at once, avoiding PO's parade of horrors. Ex-1041 ¶44. Using EMIH, "four pairs of stacked wafers were bonded *simultaneously* in 5 min, demonstrating the potential for multiwafer bonds and high-throughput batch processing." Ex-1060, 285 (emphasis added); *see* Ex-1059, 29. Thus, a POSITA would have known how to bond the layers of Watanabe's stacking method without cumulatively exceeding the thermal budget.

Second, a POSITA would have known how to align Watanabe's stackable add-on layers in its stacking method despite PO's exaggeration of this obstacle. PO again disregards the skill and knowledge of a POSITA. The Federal Circuit

“explained that there is no absolute requirement for a relied-upon reference to be self-enabling in the § 103 context, so long as the overall evidence of what was known at the time of invention establishes that a skilled artisan could have made and used the claimed invention.” *Raytheon v. General Electric*, 993 F.3d 1374 (Fed. Cir. 2021).

Here, a POSITA would have known how to precisely align the planar members of Watanabe's stacking method because techniques for wafer alignment were well-known and discussed extensively in prior art. Ex-1041 ¶46. Two common wafer-to-wafer alignment techniques for fabricating a three-dimensional semiconductor memory structure using stackable add-on layers are mechanical alignment and optical alignment. In mechanical alignment, physical structures—such as the silicon wafers' main flats (or grooves)—are used to align the wafers to each other. Ex-1054, 315-16, Fig. 1; *see* Ex-1055, 276-77. Optical alignment uses well-defined patterns called alignment marks, located on the frontside or backside of the wafers to be stacked. Ex-1055, 274, Fig. 1.

Throughout its Response, PO demands more from the prior art than the teachings of its '702 Patent. For example, the '702 Patent never mentions how to bond its stackable add-on layers. *See generally* Ex-1001. Similarly, the '702 Patent merely lists several different methods of wafer alignment without providing any detail on application. Ex-1001, 6:13-25. Dr. Przybylski had not even “considered

whether [the '702 Patent's] description is sufficient for a POSITA to perform the necessary alignment.” Ex-1051, 111:24-114:7. Because by 2004 a POSITA would have known how to resolve PO's alleged obstacles using well-known techniques, PO has not identified any reason the teachings of Lee and Watanabe cannot be combined.

B. A POSITA would have been motivated to combine the teachings of Lee, Watanabe, and Endoh and would have had a reasonable expectation of success

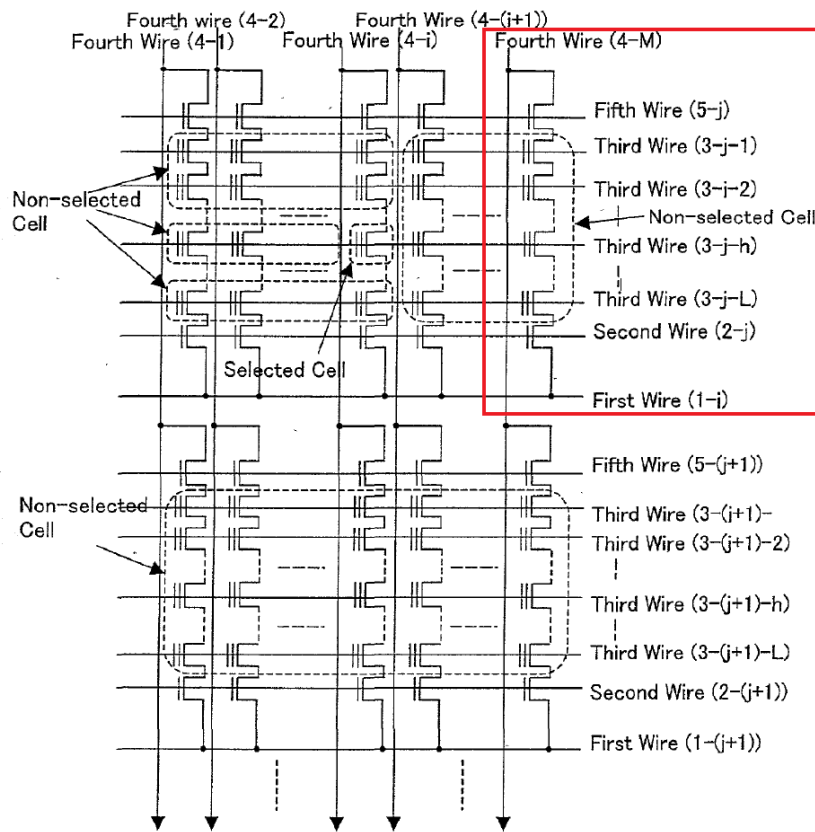
A POSITA would have known how to construct Lee's and Watanabe's memory array using Endoh's NAND architecture. Flash memory products have existed since at least the late 1980s, Ex-1025, 2; Ex-1057, 490, and the two most common types of flash memory architectures are NOR and NAND. Ex-1002, VIII-H. As Dr. Lee explained, a POSITA would have known how to implement the memory cells of Lee and Watanabe within NAND architecture because the differences between NOR and NAND architectures reside in the circuitry that couples the memory cells. *Id.*; Ex-1041 ¶¶51-53.

A POSITA would have understood that memory cells could generally be used in either NOR or NAND architecture. *Id.* ¶54. Neither the '702 Patent nor the prior art the Petition cites are directed to a particular circuit design—they apply their teachings to multiple types of memory devices and architectures. The '702 Patent relies on the knowledge of a POSITA in its attempt to claim stackable add-on layers

of DRAM, SRAM, and nonvolatile memory cells without specifying how a POSITA would modify the architecture. Ex-1001, 2:4-9. The '702 Patent states generally, "Since the body of SOI pillar is usually floating, the nonvolatile could work as a DRAM device." *Id.* 10:31-32; *see id.* 3:11-29, 9:24-50 (applying the same teachings to DRAM and nonvolatile memory devices). Thus, a POSITA would have understood that the memory cells of the '702 Patent were interchangeable. Ex-1041 ¶54.

Similarly, a POSITA would have known how to implement Lee and Watanabe's memory cells in a NAND architecture by using well-known circuit design teachings. Ex-1041 ¶55. As Dr. Przybylski conceded, Endoh discloses "memory cell transistors in a NAND flash memory array...connected serially." Ex-2029 ¶138. For example, Endoh's Figure 65 illustrates a NAND array with four floating gate transistors (within annotated red box) connected in series forming a chain between the bit line (Fourth Wire) and ground (First Wire) through two select gate transistors (above and below the four floating gate transistors).

Fig. 65



Ex-1006, Fig. 65; *see* Ex-1058, 0020-21, Fig. 40. Each of the four floating gate transistors is controlled by a control gate (within each of the floating gate transistors); *see* Ex-1007, Fig. 2, 15:41-54. Because NAND architecture was well-known in the art and a POSITA would have understood that the memory cells were interchangeable, there would not be a “cascading set of modifications” to overcome. Ex-1041 ¶55. Rather, a POSITA would have begun with the teachings of NAND architecture, such as Endoh’s, and would have implemented the nonvolatile memory cells of Watanabe’s or Lee’s array in series within that architecture. *Id.* ¶56.

C. Applicable legal precedent compels a finding of motivation to combine

BeSang argues for a high bar regarding motivation to combine that is inconsistent with current caselaw. For example, the Federal Circuit recently held that (1) a known technique can provide motivation to combine and (2) a known technique does not need to improve upon the primary reference—it just must be a “suitable option.” *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380-81 (Fed. Cir. 2023). Further, USPTO’s Section 103 Guidance calls for a “flexible approach.” Ex-1056. “[A] proper understanding of the prior art extends to all that the art reasonably suggests, and is not limited to its articulated teachings regarding how to solve the particular technological problem with which the art was primarily concerned.” *Id.* 14,450. Using the correct standard, a POSITA would have been motivated to combine the teachings of Lee, Watanabe, and Endoh because of the benefits offered by the known stacking method (improved integration density and transistor performance) and NAND architecture (fewer contacts per memory cell improving integration density) and would have had a reasonable expectation of success in combining these teachings.

IV. GROUNDS 3-4: CLAIMS 13-17 ARE OBVIOUS OVER LEE IN VIEW OF ENDOH

Although PO argues that no construction of “stackable add-on layer” is necessary, PO’s arguments against Grounds 3-4 depend on a claim construction

consistent with the Board's preliminary construction. PO implicitly adopts the Board's preliminary construction throughout its Response in trying to distinguish Lee. And PO does not dispute that Lee alone or in view of Endoh discloses all elements of at least Claim 13 if the Board were to construe "stackable add-on layer" to encompass sequential deposition.

Instead, PO's arguments amount to misinterpretation of Petitioner's mapping for Grounds 3-4, a failure to appreciate the level of skill in the art regarding NAND architecture, and an inconsistent construction of "SOI pillar." First, as stated in the Petition and clarified in Petitioner's Preliminary Reply, Petitioner does not combine disparate embodiments to arrive at the claimed subject matter. The Board correctly recognized this. Paper 9 at 25. Second, as discussed above, a POSITA would have known how to implement Lee's memory cell array within NAND architecture. Ex-1041 ¶¶54-56.

Third, Dr. Lee's identification of the memory cells in Figure 12B as separate pillars is not dispositive because those memory cells can form a single pillar consistent with both PO's and Petitioner's construction of "SOI pillar." Ex-1041 ¶62. The '702 specification allows for multiple memory cells within a single pillar. *See, e.g.*, Ex-1001, Figures 4, 20, 27 (showing multiple memory cells on singular "SOI pillar 124"), 8:7-10, 9:14-17, 9:51-55. PO's construction does not define whether a single or multiple memory cells constitute a "pillar." And given that Dr.

Przybylski refused to provide bounds for a “pillar” during his deposition—testifying that “‘taller than it is wide’...is the only indication of what constitutes a pillar,” Ex-1051, 66:25-67:1—the two memory cells of Lee’s Figure 12B may form a single pillar consistent with PO’s construction in the same way that multiple memory cells of the ’702 Patent’s Figures 4, 20, and 27 form a single pillar. Ex-1041 ¶62.

The memory cells of Lee’s Figure 12B may also form a single pillar consistent with Petitioner’s construction of “SOI pillar” because the ’702 Patent defines a pillar as a “doped stack structure.” Ex-1001, 6:28-29. Dr. Lee agreed that “the pillars in Figure 12B are just the n+, p-, n+ dope stack structures,” Ex-2028, 79:15-19, and a POSITA would have understood that two memory cells could together form a single pillar. Ex-1041 ¶63.

V. GROUNDS 1-2: CLAIMS 13-17 ARE OBVIOUS OVER WATANABE IN VIEW OF ENDOH

A. Watanabe discloses a nonvolatile memory cell

Ground 1 does not combine Watanabe’s DRAM and EPROM embodiments. Watanabe discloses two “method[s] used to manufacture a semiconductor memory device,” having “memory cells arrayed three-dimensionally.” Ex-1005, 5:8-6:19, 1:49-52. Watanabe explains that “the present invention provides a 3-dimensional memory cell array in which memory cells are respectively located at the cross points of a plurality of planar members (21, 22) arranged in parallel.... By virtue of such a 3-dimensional memory cell array, the integration density of the semiconductor

memory device can be greatly increased.” Ex-1005, 1:65-2:5. Watanabe further states, “FIG. 1 is a rough schematic illustration of a semiconductor memory device...made up of two conductive planes, or planar members, 21 and 22.” *Id.* 2:44-48. Thus, Watanabe’s Figure 1 is a high-level schematic that generally illustrates how the memory cells of the invention are constructed, *i.e.*, using multiple device layers. “In this instance [Figure 1], there are 8 cross points. The *memory cell* of the present *invention* is applicable to any type of memory device *i.e.*, a SRAM, a PROM, or a DRAM....” *Id.* 2:50-55 (emphasis added); *see, e.g.*, Paper 1 at 9, 25. Thus, Watanabe explicitly states that the *memory cells* depicted at the cross points of Figure 1 (*i.e.*, 27-34) can be “any type of memory device,” including the EPROM nonvolatile memory cell depicted in Figure 7.

Although the memory cells in Figures 5 and 6 illustrating the manufacturing methods are “depicted as incorporated in a DRAM,” Ex-1005, 2:53-55, a POSITA would have understood that Watanabe’s teachings regarding the manufacturing methods apply equally to any type of memory cell disclosed in the invention. Petitioner does not attempt to combine or alter embodiments of different memory types shown in Figures 2A and 5-7. Rather, Petitioner is using these figures to illustrate how Watanabe’s “stacking” and “laminating” (*i.e.*, sequential deposition) methods apply to the EPROM memory cell structure shown in Figure 7. Watanabe makes clear that one could replace the contents of Figure 2A’s cell 50 (shown as a

dashed-line box) with the nonvolatile memory cell shown in Figure 7 because the photolithography steps necessary to make an EPROM memory cell were well known and within the skill of a POSITA. Ex-1041 ¶65.

The '702 Patent takes a similar approach in its description of volatile and nonvolatile memory devices. For example, "FIG. 23 shows a vertical memory cell with a vertical MOSFET in a stackable add-on layer [that]...could work as a DRAM and/or a nonvolatile memory device." Ex-1001, 9:24-28. Thus, a POSITA would have understood that Watanabe's "stacking" and "laminating" (*i.e.*, sequential deposition) methods apply equally to the EPROM nonvolatile memory device depicted in Figure 7 and how to manufacture the resulting device. Ex-1041 ¶66.

B. Watanabe in view of Endoh discloses an "SOI pillar"

"SOI pillar" should be construed as "a doped stack structure formed from a single-crystal portion of a semiconductor wafer transferred from one wafer to another previously fabricated wafer or similar type of substrate." Because Watanabe discloses a vertical structure with "[a]t least two stack structures (two layers) [*i.e.*, two planar members] each consisting of layers 41 to 46"—*i.e.*, a doped stack structure—formed over an insulator, a POSITA would have understood that Watanabe discloses a SOI pillar or renders it obvious. *See* Ex-1005, 3:12-13, Figs. 1, 2A (showing doped stack structures forming vertical pillars above insulator 49); Ex-1041 ¶67. Further, Watanabe discloses that the "n+ type Si layer 45 is layered on

an insulating film 49” and that “[w]hen a vapor phase epitaxial method”—commonly used to form a SOI structure—“is used for forming these layers, these may be successively formed by appropriately changing doping gases.” Ex-1005, 3:33-37, Figs. 2A-2B; Ex-1041 ¶67. Endoh also discloses “a semiconductor memory device” in which “a bulk substrate but also a SOI substrate, a multi-layered SOI substrate and the like may be used,” and where “island-like semiconductor layers are formed in the form of *pillars* by selective epitaxial silicon growth.” Ex-1006 ¶¶329, 1206 (emphasis added). Thus, Watanabe in view of Endoh discloses or renders obvious “SOI pillar” as properly construed. Ex-1041 ¶67.

Conversely, PO’s construction of “SOI pillar” is inconsistent with the state of the art at the time. As discussed above, the figures of Watanabe, Lee, and the ’702 Patent were not drawn to scale. Ex-1041 ¶68; Ex-2028, 139:22-140:3; Ex-1051, 54:9-56:3; Ex-2029 ¶80.

Watanabe discloses a “SOI pillar” under PO’s erroneous construction, which does not limit “SOI pillar” to a single doped silicon region or even a single memory cell. Ex-1041 ¶69. Even under PO’s construction, Watanabe discloses a “pillar” because it describes stacking multiple layers as shown in Figure 6C, which would result in a structure taller than it is wide. Ex-1005, 3:12-15, 6:3-5, Fig. 6C.

C. Watanabe’s stacking method is enabled

Despite Watanabe’s bonding process at 900-1000°C, a POSITA would have

understood how to perform Watanabe's stacking method without exceeding thermal budget. Ex-1041 ¶70. For example, a POSITA would have understood that EMIH offers "a method of bonding a stack of silicon wafers...in a shorter time period than prior methods" to manage the thermal budget while bonding the wafers at a high temperature. Ex-1048, 1:26-29, 1:40-43, 1:64-67; *see* Ex-1049; Ex-1050.

VI. CONCLUSION

For the reasons given in the Petition and this Reply, Petitioner requests cancellation of Claims 13-17 of the '702 Patent.

Dated: May 3, 2024

Respectfully submitted,

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CERTIFICATE OF WORD COUNT

Under 37 C.F.R. §42.24(d), Petitioner certifies that Petitioner's Reply to Patent Owner's Response includes 5,599 words, as measured by Microsoft Word, exclusive of the table of contents, mandatory notices under §42.8, certificates of service, word count, and exhibits.

CERTIFICATE OF SERVICE

The undersigned certifies pursuant to 37 C.F.R. § 42.6(e) that on May 3, 2024, a true and correct copy of **PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE**, together with all exhibits filed therewith was served in its entirety by filing these documents through the PTAB E2E System, as well as by email, on the counsel of record for the Patent Owner.

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