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Advances Toward Reliable High Density Cu–Cu Interconnects by Cu-SiO₂ Direct Hybrid Bonding

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Abstract—Cu-SiO₂ direct hybrid bonding is considered as one of the most promising approaches for matching the needs of three dimensional integrated circuits (3D-IC). In this paper we present the results of a complete morphological, electrical and reliability study conducted on four-layer copper structures realized by Cu-SiO₂ direct hybrid bonding. Ultra-fine 7 μm pitch, 3 μm $\times$ 3 μm pads daisy chains with up to 30 160 connections are bonded with submicron accuracy, matching the interconnection needs in upcoming 3D circuits. A focus is paid on the influence of the temperature of annealing on the bonding quality and electrical performances. Thanks to SEM, FIB/SEM tomography, AFM, TEM and TEM-EDX analysis, the morphology of the bonded structures is described. Electrical parametric tests exhibit very low resistance structures, with high functional yields and low variability. State-of-the-art contact resistivity is obtained for 200 and 400 °C treatments. Unbiased HAST, temperature cycling and temperature storage tests demonstrate excellent reliability performances. Finally, an electromigration resistance comparative study is conducted on bonded copper lines with TaN/Ta and TiN diffusion barriers.

I. INTRODUCTION

Direct bonding technology consists in joining together two flat and clean surfaces without any intermediate adhesive layer. At room temperature, the adhesion at the interface is the result of attractive surface forces such as van der Waals force and hydrogen bonds. A thermal treatment, usually performed at 200 or 400 °C, is necessary to irreversibly seal the interface thanks to the formation of covalent bonds between the surfaces in contact. The direct bonding of homogenous surfaces such as Si/Si and SiO₂/SiO₂ has been extensively reported in the literature [1]. Recently, the electrical performances and reliability of Cu-SiO₂ direct hybrid bonding have been investigated by means of test structures with two copper layers on 200 mm wafers in both wafer-to-wafer (WtW) and chip-to-wafer (CtW) integrations [2, 3]. Outstanding reported results are compatible with industry standards, including low contact resistivity and extrapolated life time over 10 years. Moreover, interconnection pitches below 3 μm , soon required for future high performance devices, are only achievable with direct hybrid bonding. This is why this technology is considered as the most promising approach for matching the needs of upcoming 3D integrated circuits (3D-IC) [4]. However, a lot of questions have to be answered regarding the compatibility of

the direct bonding process and integration with a full industrial process/manufacturing flow. The bonding quality being very dependent of the surface topology, this aspect has to be investigated in the case of devices with more than two layers of interconnections, as well as the overall mechanical robustness of such stacks. Electrical performances, environmental and electrical reliability are also major concerns in the presence of multiple connection layers, implying different materials and thus thermo-mechanical stresses at the bonding interface. In that regard, electrical and reliability studies conducted on four-layer daisy chains with 6 μm and 10 μm pitch using respectively thermocompression and direct bonding methods have already been reported [5, 6]. However, the bonding quality and electrical reliability of direct bonded four-layer daisy chains with a pitch below 10 μm have yet to be demonstrated.

The present paper gives an overview of the latest achievements in regard to Cu-SiO₂ direct hybrid bonding with four interconnect layers. Descriptions of the experimental setup and test structures, including 7 μm pitch 3 μm $\times$ 3 μm pads daisy chains with up to 30 160 connections, are first presented. Morphological characterizations of the bonding interfaces after annealing at 200 and 400 °C, using SEM, FIB/SEM tomography, AFM, TEM and TEM-EDX analysis are then discussed. Additionally, electrical and reliability investigation results are shown for the three types of daisy chain structures employed. To conclude, an electromigration resistance comparison between fully bonded NIST-like test structures with TaN/Ta and TiN diffusion barriers is carried out and compared to the behavior of traditional Cu damascene lines.

II. EXPERIMENTAL SETUP

A. Wafer-to-wafer integration

The fabrication of the four-layer copper interconnects was based on a typical single-damascene process on 200 mm wafers, including 500 nm high SiO₂ layer deposition and line opening, diffusion barrier and Cu seed deposition by Chemical Vapor Deposition (CVD), Cu filling by Electrochemical Deposition (ECD) and Chemical-Mechanical Polishing (CMP). The latter was optimized to obtain a low total thickness variation, a minimal surface roughness and a well-controlled dishing effect on Cu surfaces in agreement with the

requirement of the Cu direct bonding technique. Special attention was given to preserve minimal surface topology at all metal levels of this BEoL-like integration, featuring SiN barrier in between dielectric layers and symmetrical bonding pads dedicated to reduce the amount of Cu/SiO₂ interfaces compared to previous direct bonding studies [2, 3]. While the bonding step is carried out at room temperature and ambient pressure, thermal treatments aimed at strengthen the bonding interface thanks to the creation of Cu–Cu and Si–O–Si covalent bonds were performed at 200 and 400 °C in two different batches. The bonding interface was strong enough to sustain thinning down to 40 µm and a complete removal of the backside silicon of the top wafer by wet etching. Finally, a redistribution layer (RDL) in Ti/TiN/AlSi was realized after SiON hard mask deposition. This simple backside process permits to directly observe bonded structures through the transparent SiON and SiO₂ layers. Moreover, the aluminum being resistant to corrosion up to 400 °C, there is no need for further passivation steps. Fig. 1 shows a schematic representation of the whole WtW integration.

B. Experimental structures

For the needs of this study, test structures had to allow the characterization of the electrical resistance, the contact resistivity, the environmental and electromigration resistances of the bonding interface as well as the feasibility and reproducibility of ultra-fine pitch connections. NIST-like test structures and daisy chain (DC) structures were designed to reach these goals. A schematic description of the four NIST structures employed can be found in the Fig. 2. The stand-alone NIST A0 structures were used to extract the copper resistivity which allowed to calculate the theoretical resistance of the bonded structures A1, A2 and A3. The contact area is 640 µm × 3 µm and 340 µm × 3 µm respectively for the NIST A1 / A3, and A2 test structures. The fact that probe pads of the NIST A1 and A2 structures are located on two different layers forces the current to pass through the bonding interface during the electrical characterization. On the contrary, the contact pads of the bonded NIST A3 structures are on the same metal layer. Therefore, if the contact resistance is too high, in the case of a poor bonding quality for instance, the current would flow only in the upper line without crossing the bonding interface.

The DC structures consist in long chains of interconnections between the top wafer and the bottom one, composed of buried lines connected by square bonding pads. In the scope of our study, the purpose of this structure is to validate the compatibility of the direct bonding process with high interconnection density stacks and to obtain a good estimation of the mean contact resistivity of the Cu/Cu interface, thanks to high number of bonding pads. Three types of DC were designed, called DCP1, DCP2 and DCP3, with different connection numbers and pitches. Contrary to the other DC, the bonding pads of DCP1 located on the top wafer are larger than the ones on the bottom wafer. This design allows maintaining a constant contact area despite the bonding misalignment, which helps to better estimate the contact resistivity. Top view pictures and detailed characteristics of all DC are available in Fig. 3 and Table I respectively.

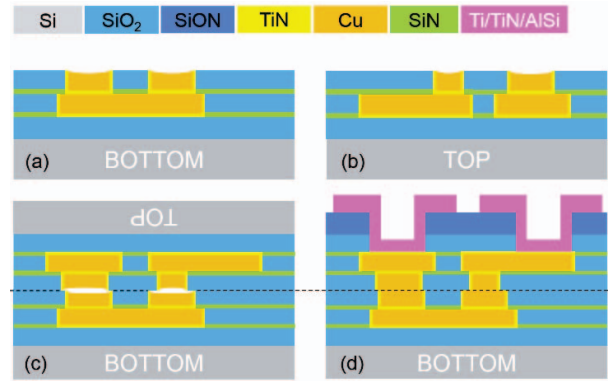


Figure 1. Test vehicle fabrication process: (a, b) successive damascene processes optimized for multilayer Cu–SiO₂ direct hybrid bonding, (c) bonding at room temperature, atmospheric pressure and ambient air, (d) annealing, Si removal and redistribution layer (RDL) realization.

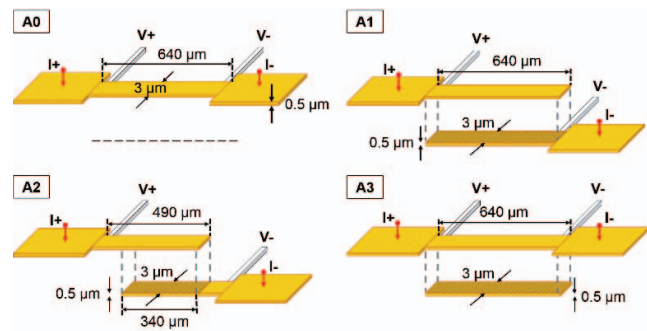


Figure 2. Schematic view of the stand-alone NIST A0 structure used for determining the copper resistivity, and fully and partially bonded NIST A1, A2 and A3 structures.

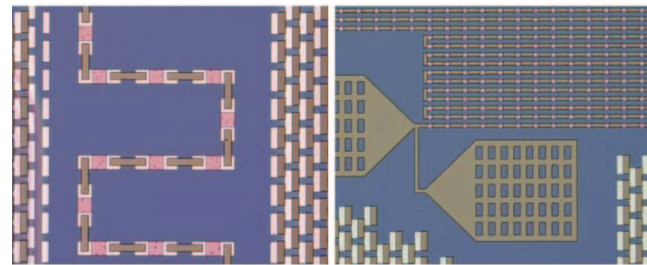


Figure 3. Optical observations of daisy chain structures after complete removal of the backside silicon of the top wafer.

Table I. Detailed characteristics of the three daisy chain structures.

Daisy chain	Interco. number	Pad width top / bottom (µm)	Pitch x / y (µm)	Top view and cross section
DCP1	7068	5 / 3	15 / 15	
DCP2	11 056	3 / 3	12 / 12	
DCP3	30 160	3 / 3	7 / 7	

III. FOUR-LAYER INTEGRATION CHARACTERIZATIONS

In this section we first present the results of an extensive morphological characterization study of the bonding interface. Electrical resistances and contact resistivity of NIST and DC structures are then discussed, along with environmental reliability test results. The influence of the annealing temperature is investigating through comparisons between results obtained after annealing at 200 and 400 °C.

A. Morphological investigations

Bonding misalignment and Cu/Cu interface. Before any advanced structural investigations, a quantitative alignment study is conducted after annealing. Fig. 4 depicts a vector field typically obtained in our studies, using the x and y components of the misalignment, measured thanks to dedicated vernier structures implemented in each 1 cm wide die. A slight angular misalignment is noticeable, with a maximum amplitude of 0.8 μm . State-of-the-art minimum and mean bonding accuracies of about 0.1 and 0.25 μm respectively are detailed in the table next to the map, which are compatible with roadmaps for high interconnect density 3DICs.

Morphological characterizations focuses mainly on the copper interface of 7 μm pitch, 3 $\mu\text{m} \times 3 \mu\text{m}$ pads of daisy chains DCP3. Post-bonding annealing stages carried out at 200 and 400 °C allow us to compare the influence of the annealing conditions on the bonding quality. SEM observations depicted in Fig. 5 are first conducted after thermal treatment at 200 and 400 °C for 2 h on two different samples. In both cases, bonded pads exhibit a well closed Cu/Cu interface on the entire width of the structure with a mostly linear shape. Additionally, while some typical interfacial voids with a width of a few hundred nanometers are present after an annealing at 200 °C, no significant defect is noticeable. Further FIB imaging of other bonding pads thermally treated at 400 °C shown in Fig. 6 even demonstrate copper diffusion and grain growth at triple points though the bonding interface. This phenomenon is responsible for the disappearance of the previously observed linear interface in favor of a bulk-like copper interface.

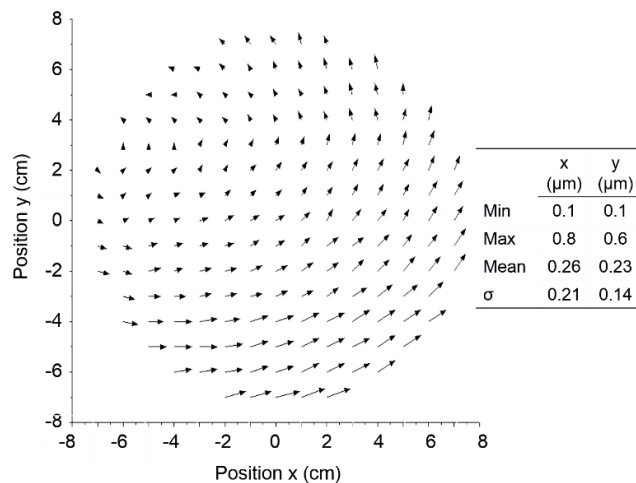


Figure 4. (left) Bonding misalignment map after annealing at 400 °C for 2 h. The table summarizes the results of this study, with an alignment accuracy comprised between 0.1 and 0.8 μm ($\pm 0.1 \mu\text{m}$).

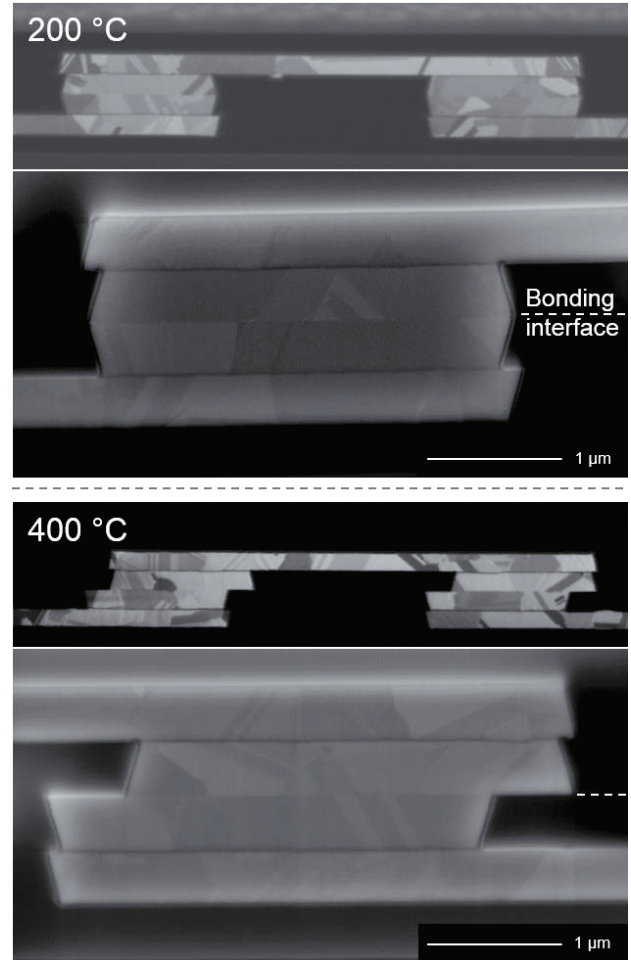


Figure 5. SEM cross section of a 3 $\mu\text{m} \times 3 \mu\text{m}$ daisy chain connection annealed at 200 and 400 °C for 2 h. Overall bonding quality and alignment accuracy are remarkable.

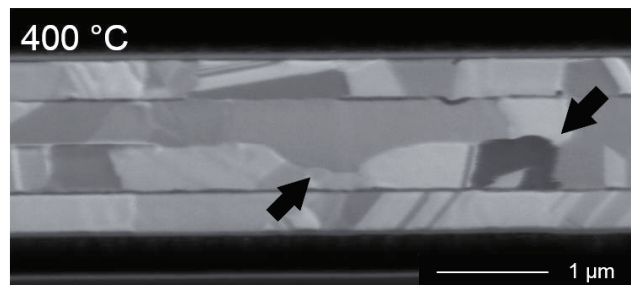


Figure 6. Ionic cross section of bonded pads annealed at 400 °C for 2 h. Grain growth through the bonding interface is noticeable (black arrows).

Interfacial voids observation. The observation of the void distribution at the bonding interface after annealing at 400 °C has been made possible thanks to FIB/SEM tomography surface reconstruction (FIB/SEM slice and view). On the result shown in Fig. 7 we can notice the presence of two kinds of voids. A-type voids with a width of around 100 nm are located at the edges of the copper pads and do not seem to be related to the direct bonding process, as they can be found at both Cu/Cu and Cu/SiO₂ interfaces. B-type voids are located at the Cu/Cu interface, unequally distributed at the center of the bonded area, with various shapes and sizes ranging from a few nanometers to around 150 nm.

A series of AFM, TEM and TEM-EDX characterizations, presented in Fig. 8 to Fig. 10, helps to pinpoint the main mechanisms responsible for the formation of A-type and B-type voids. AFM scans of the 3 μm wide bonding pad, carried out prior to bonding, indicate important defects at the edge of the structure under the form of missing copper at the Cu/TiN interface. Furthermore, while the surface roughness is about 0.65 nm RMS, Fig. 8a and Fig. 8b close up views indicate a slightly higher surface roughness at the center of the pad, with the presence of small trenches due to missing copper crystallites. Both phenomena are attributed to the over-polishing action of the CMP step, which results in a lack of copper at weak interfaces and higher roughness at the center of the pad. Those surface imperfections are identified as the main reason for the formation of A-type voids at the edge of the bonding structures, and B-type voids located mostly at the center of the bonding interface.

TEM observations of the Cu/Cu interface shown in Fig. 9 indicate the occurrence of copper grain growths at triple points similarly to ionic characterization presented in Fig. 6, which is a sign of strong diffusion of copper along grain boundaries and through the bonding interface. We can also observe the existence of slit voids (blue arrows) and circular ones (red arrows). While both void types can be originated from surface imperfections, such as surface roughness and small trenches visible on the AFM images, some of the circular ones are known to be the result of copper oxide diffusion. Previous studies have indeed shown that the inevitable native copper oxide layer on the surface of the bonding pad, with a height of a few nanometers, becomes instable under thermal treatment [7] and can therefore diffuse along the bonding interface and create oxide droplets. While this mechanism allows Cu diffusion through the interface and thus Cu–Cu covalent bonds to form, this also creates interfacial voids partially filled with copper oxide and oxygen [8]. TEM-EDX pictures of the Cu/Cu interface depicted in Fig. 10 confirm this phenomenon, with oxygen atoms mostly located in the circular voids, which validate the copper oxide diffusion as a void formation mechanism in the scope of our study.

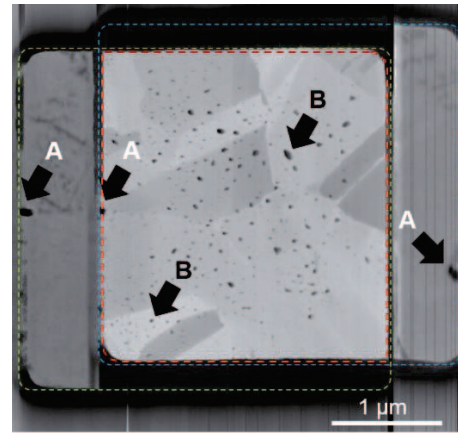


Figure 7. FIB/SEM tomographic surface reconstruction, showing a top view of the bottom pad (green dashed line), the top pad (blue dashed line) and the void distribution at the Cu/Cu bonding interface of a 3 μm $\times$ 3 μm daisy chain connection (red dashed line), after annealing at 400 $^{\circ}\text{C}$ for 2 h. A-type and B-type voids are indicated.

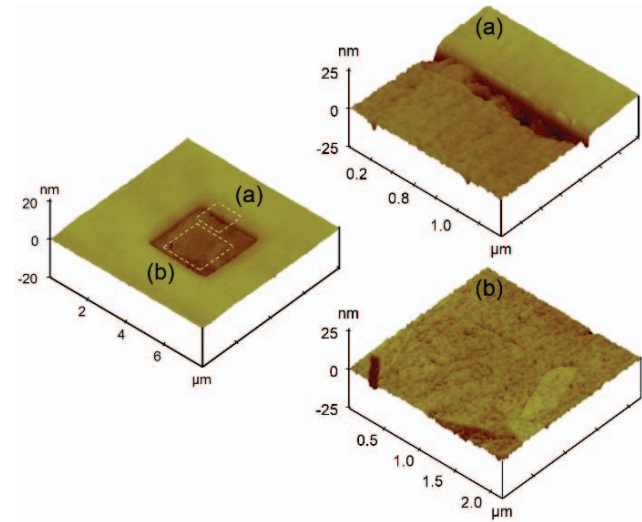


Figure 8. (Left) AFM scans of a 3 μm $\times$ 3 μm daisy chain bonding pad after CMP; (a) Close up view of the edge of the structure, indicating a lack of copper at the Cu/TiN interface; (b) Close up view of the center of the structure, showing irregularities in the copper surface roughness.

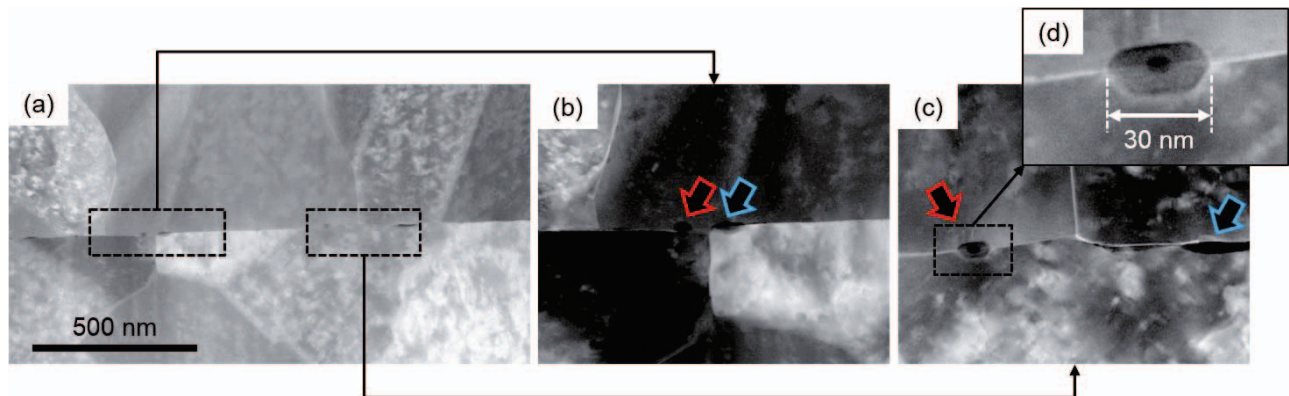


Figure 9. TEM characterization of the bonding interface of a DCP3 connection annealed at 400 $^{\circ}\text{C}$ for 2 h; (b)(c) Close up views of circular voids mostly due to surface roughness and oxide diffusion (red arrows) and slit ones due to surface imperfections (blue arrows). Copper grain growths at triple points are also visible; (d) Typical interfacial void.

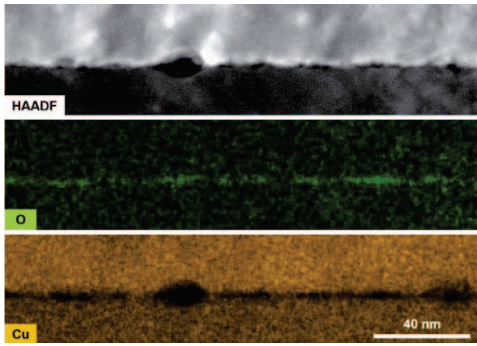


Figure 10. TEM-EDX characterizations of the Cu/Cu bonding interface in the presence of B-type voids. The presence of oxygen in the vicinity of the interface and inside the voids is observable.

Copper diffusion investigations. One common concern for Cu-SiO₂ direct bonding technology and integration is related to the potential Cu diffusion into the surrounding SiO₂ due to the ever existing misalignment between bonded substrates. In order to investigate the occurrence of this phenomenon in the scope of our test vehicle, the surroundings of the Cu/SiO₂ interface located at the edge of misaligned bonded pads are characterized with TEM-EDX spectroscopy. Copper diffusion being a thermally activated process [9], this study is conducted on samples annealed at 400 °C for 2 h and after temperature storage at 300 °C for 336 h. Fig. 11 shows a TEM image of the structure, presenting no structural degradation, with the path of the EDX analysis spot (red arrow). In addition, the concentration profile also illustrated, related to the samples stored for 336 h, is identical for both annealing conditions and indicates no Cu diffusion in the SiO₂ part. This result tends to prove that such phenomenon, susceptible to alter electrical performances and reliability, does not occur at the bonding interface.

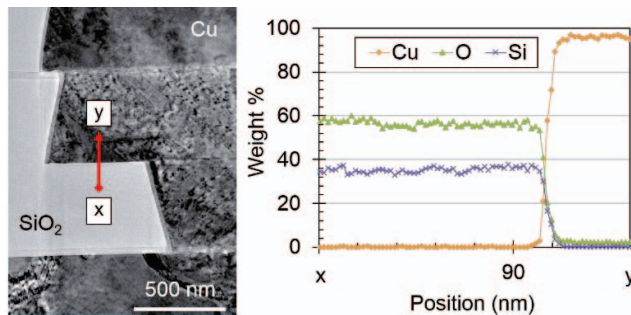


Figure 11. TEM-EDX profile of Cu, O and Si elements, after temperature storage at 300 °C for 336 h, along the red arrow shown on the TEM picture. Presence of Cu inside the SiO₂ layer is not noticeable.

B. Electrical characterizations

Annealing temperature influence and contact resistivity. We have seen that morphological characterizations of a 3 µm wide bonding pad revealed well sealed Cu/Cu and Cu/SiO₂ interfaces, after 200 and 400 °C annealing. While FIB/SEM tomography surface reconstruction helped to have a better understanding on the nature and distribution of interfacial voids, electrical characterizations of NIST and daisy chain structures can give statistical information regarding their

impact on electrical resistance at wafer level. It is first important to determine if whether or not the four-layer integration has an influence on the bonding quality and thus electrical performances. To do so, the electrical resistance of the NIST A1, A2 and A3 test structures are measured and compared to theoretical resistance values and also previous measurements done on two-layer integration [3]. In order to calculate the theoretical resistances, it is necessary to extract the copper resistivity. Measurements of the A0 structures give $\rho_{200^\circ\text{C}} = 2.08 \times 10^{-2}$ and $\rho_{400^\circ\text{C}} = 2.06 \times 10^{-2} \Omega \cdot \mu\text{m}$ after annealing at 200 and 400 °C respectively. Table II summarizes the electrical resistances obtained for the 3 NIST structures in the four-layer integration, in good agreement with both theoretical calculations and previous results obtained on test vehicles with two copper layers. Additionally, NIST A1 and A3 structures have similar resistances in both integrations, which demonstrate that electrons indeed travel through both copper lines in the case of the A3 structure, even if they are not forced to. This shows that the contact resistance of the bonding interface is low in any case. These results therefore prove that the four-layer integration, dedicated to mimic BEoL interconnects, does not affect negatively the electrical performance and confirm the good bonding quality observed in the previous section after annealing at 200 and 400 °C.

Electrical characterization results of the daisy chains DCP1, DCP2 and DCP3 annealed at 200 and 400 °C, labeled α and β respectively, are summarized in Table III. In both cases, functional yields are above 96 % and standard deviations are below the commonly accepted standard of 3 % regarding BEoL interconnections.

Table II. Electrical resistance comparison between NIST structures present on test vehicles with two and four copper layers, annealed at 400 °C for 2 h.

NIST	Integration type	Resistance (Ω)	
		Experimental	Theoretical
A1	Two Cu layers	4.39	4.27
	Four Cu layers	4.26	4.23
A2	Two Cu layers	6.34	6.26
	Four Cu layers	6.24	6.22
A3	Two Cu layers	4.31	4.27
	Four Cu layers	4.29	4.27

Table III. Electrical characterization results conducted on daisy chains DCP1, DCP2 and DCP3 after annealing at 200 and 400 °C for 2 h.

		DCP1	DCP2	DCP3
200 °C - α	Functional yield (%)	99	96	96
	Mean R_{exp} (Ω)	888.02	1873.86	3264.80
	Std. deviation (%)	1.33	1.97	2.67
	Contact resistivity	154 m $\Omega \cdot \mu\text{m}^2$		
400 °C - β	Functional yield (%)	99	99	98
	Mean R_{exp} (Ω)	873.48	1857.50	3227.54
	Std. deviation (%)	0.99	0.84	1.37
	Contact resistivity	123 m $\Omega \cdot \mu\text{m}^2$		

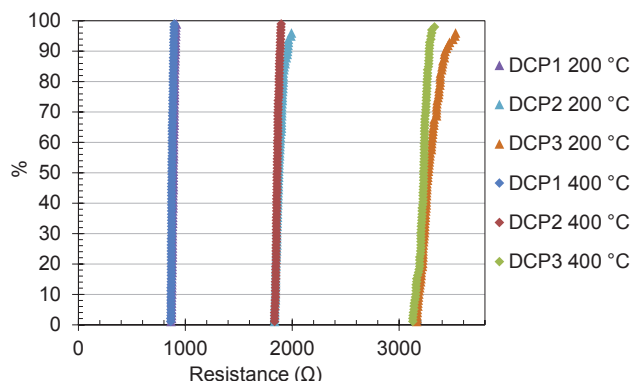


Figure 12. Cumulative percentage of the resistance of the daisy chains DCP1, DCP2, and DCP3 annealed at 200 and 400 °C for 2 h.

We can however observe that an annealing at 400 °C offers better electrical performances than an annealing at 200 °C, with functional yields up to 99 % and standard deviations as low as 0.8 %. The DCP1 structures having a constant contact area of $9 \mu\text{m}^2$ thanks to asymmetrical bonding pads, their electrical resistance is not affected by bonding misalignment. For this reason these structures are used to estimate the maximum contact resistivity ρ_c for both annealing conditions. Extracted values range from 123 to $154 \text{ m}\Omega \cdot \mu\text{m}^2$ for β -type and α -type structures respectively, which are around 3 times lower than the latest reported values related to four-layer daisy chains [6]. A comparison of the cumulative percentage of the resistance of α -type and β -type DC illustrated in Fig. 12 indicates that the longest DC is the most beneficiary of the lower contact resistivity, with less deviation of the resistance. This can be explained by the cumulative effect of the contact resistivity of a connection on the global resistance, which is negated in the case of a higher temperature annealing. Those results show that $7 \mu\text{m}$ pitch interconnections with electrical performances compatible with industry standards are achievable with Cu-SiO₂ direct hybrid bonding, with an annealing temperature as low as 200 °C. As observed during morphological investigations, a thermal treatment at 400 °C results in a bulk-like copper interface, offering better electrical performances especially in the case of a high number of successive interconnections.

Environmental reliability studies. In order to investigate the environmental reliability of direct bonded high density interconnections with four levels, unbiased HAST (uHAST, JESD22-A118A), temperature cycling (TC, JESD22-A104D) and temperature storage (TS, JESD22-A103C) tests were

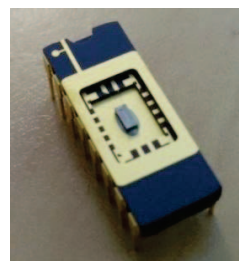


Figure 13. Picture of a packaged bonded structure used for monitored reliability tests.

Table IV. Description of the reliability test conditions.

Reliability test	Conditions	Samples
Unbiased HAST	85 °C / 85 % RH	20 DCP1
	168 h	20 DCP2
	(package level)	20 DCP3
Temperature cycling	-50 °C / +150 °C	20 DCP1
	500 cycles	20 DCP2
	(package level)	20 DCP3
Temperature storage	300 °C	99 DCP1
	336 h	99 DCP2
	(wafer level)	98 DCP3

conducted on a total of 416 β -type daisy chains. While the first test aims at validating the resistance to corrosion of the bonded interconnects, the two others are destined to study the mechanical robustness of the whole 3D stack. After standard dicing of bonded wafers, copper test structures were packaged as illustrated in Fig. 13. This configuration allowed to monitor and record the electrical resistance during the uHAST and TC tests and therefore to detect any resistance variations. The TS test was carried out at wafer level, with comparative electrical characterizations performed before and after the test. For all cases, the post-bonding annealing was done at 400 °C for 2 h and an arbitrary failure criterion was set to a resistance increase of 10 %. The specifications of the reliability tests and the related sample sizes are summarized in Table IV.

No electrical resistance increase or dramatic failure was observed during the uHAST test. This satisfying result demonstrates the hermetic nature of the integration as no penetration of humidity was electrically detected at this location. Therefore, the bonding interface should not be responsible for any critical absorption of humidity in a fully integrated device.

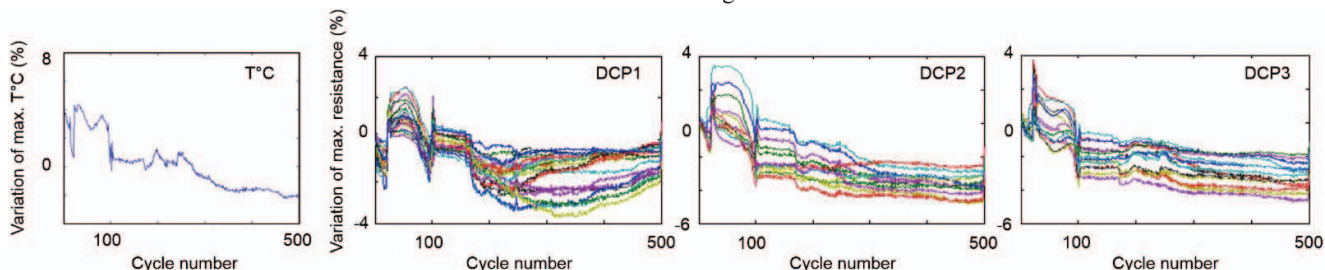


Figure 14. Variations in percentage of the temperature and the resistance during the high temperature dwell time recorded during the temperature cycling test. The failure criterion is set to 10 %. Outside of a minor resistance increase of about 2 % in the case of DCP1, no significant resistance increase or failure is noticeable.

Fig. 14 presents the results of the TC reliability test. The variations of the temperature and the resistance during the high temperature dwell time are shown for all three DC structures, as a function of the cycle number. All the samples passed the test successfully except one DCP1. Additionally, most of the resistance variations can be attributed to the temperature variations during the test, due to non-perfect temperature cycles. The only observable resistance increase is related to the daisy chain DCP1, with a magnitude of about 2 % starting from the 200th cycle. An increase of resistance during a TC test is generally attributed to delamination occurring most likely at weakest interfaces, such as Cu/TiN and Cu/SiO₂ interfaces in our case. One can notice that resistance plots related to the daisy chains DCP2 and DCP3 do not present any sign of electrical performance deterioration, which suggests that major delamination phenomena do not occur in the whole chains. For this reason, we suspect that the resistance increase happening in the case of DCP1 could be due to its asymmetrical bonding pads. Among the three types of daisy chains, only DCP1 structures present this configuration (see Table I), which could indeed induce delamination in the vicinity of the bonding interface. Further failure analyses should be conducted to verify this hypothesis. Nevertheless, this resistance increase of 2 % is well under the failure criterion of 10 % and thus does not constitute a sign of major structural degradation.

Table V summarizes the results of the TS test conducted at wafer level. This reliability test induces a slight decrease of the overall performances of all structures, with a decrease of 3 to 4 % of the functional yield and a resistance increase comprised between 0.39 and 0.60 %. As an example, the cumulative resistance of the DCP3 structure before and after the TS test is depicted in Fig. 15. Optical observations of the bonded test structures reveal no significant defect. However, some current leads located under the aluminum vias of the RDL are heavily oxidized, as shown in Fig. 16. This is due to a small delamination of the SiO₂ above the Cu, resulting from integration-related defects. This prevents the dielectric layer to act as a good passivation layer at this location, and can therefore explain some of the slight performance degradations.

Table V. Temperature storage results.

	DCP1	DCP2	DCP3
Results	96/99 pass	96/99 pass	94/98 pass
Resistance increase (%)	0.39	0.60	0.49

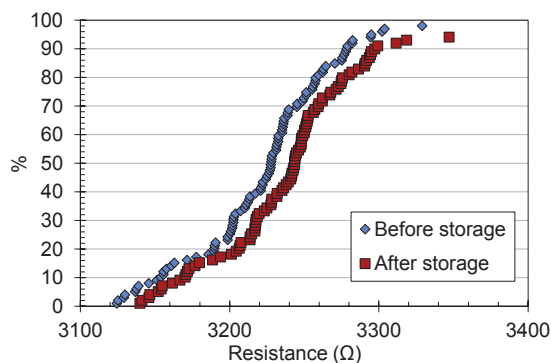


Figure 15. Cumulative percentage resistance of the daisy chain DCP3 before and after temperature storage at 300 °C for 336 h.

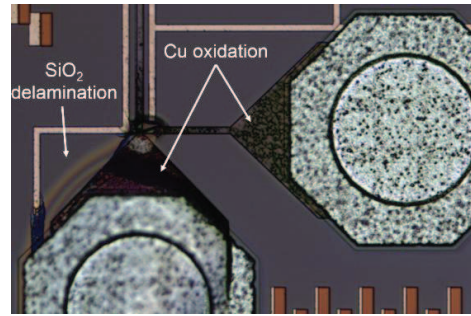


Figure 16. Optical observation of the oxidized copper under the aluminum redistribution layer after the temperature storage test. The delamination of the SiO₂ above the copper is recognizable thanks to the interference fringes.

IV. ELECTROMIGRATION RESISTANCE COMPARISON BETWEEN TiN AND TAN/TA DIFFUSION BARRIER

The various results that we present in this study, along with those reported in the literature, confirm that copper direct bonding technology allows realizing reliable high density interconnections with a low contact resistivity. In the scope of an industrial use of this bonding technique to connect the BEoL part of different dies, interrogations remain regarding the behavior of bonded copper lines compared to standard damascene ones.

While both TiN and TaN/Ta are traditionally used as diffusion barriers for copper structures, it is common knowledge that TaN/Ta barriers offer a stronger adhesion with the Cu compared to TiN ones. As a result, Cu/Ta/TaN damascene lines have a higher electromigration (EM) resistance, quantified by higher activation energy E_a . Depending on the fabrication process and the integration, values of E_a related to today's Cu damascene interconnects generally fall in the range 0.8–1.0 eV [10]. These values correspond to interface material diffusion paths, typically along Cu/TiN or Cu/Ta/TaN interfaces. With copper direct bonding, the Cu/Cu bonding interface is a potential preferential diffusion path in the case of a poor bonding quality. As we were able to realize bonded NIST structures in a two-layer integration with both diffusion barrier types, an EM resistance comparison between Cu/TiN and Cu/Ta/TaN is proposed in order to observe if whether or not direct bonded lines behave like Cu damascene ones in terms of activation energy values and thus diffusion paths.

Black's parameters activation energy E_a and current exponent n values have been reported recently in the case of 3 μ m NIST A1 structures (see Fig. 2) with 25 nm high TaN/Ta barrier annealed at 400 °C [11]. Those results are now compared to the latest EM resistance test results obtained on 3 μ m wide NIST A1 structures with 20 nm TiN barrier, also annealed at 400 °C. Typical defects, voids and Cu extrusion at the bonding interface can be observed in Fig. 17, consistent with previous EM studies conducted on NIST structures annealed at 200 °C [2]. Black's parameters are extracted through time to failure data presented in Fig. 18, along with the EM stress conditions including temperature, current and corresponding sample sizes. As we can notice in Table VI comparing the parameters extracted for both barriers, higher activation energy is found for lines with TaN/Ta. This indicates that the Cu/Ta/TaN interface is stronger and then

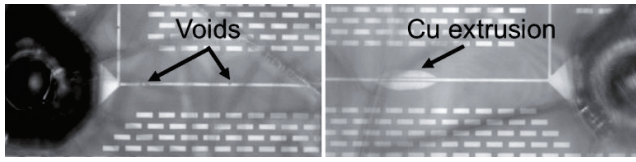


Figure 17. Typical voids and copper extrusion observed after electromigration tests conducted on NIST structures with 20 nm high TiN barrier.

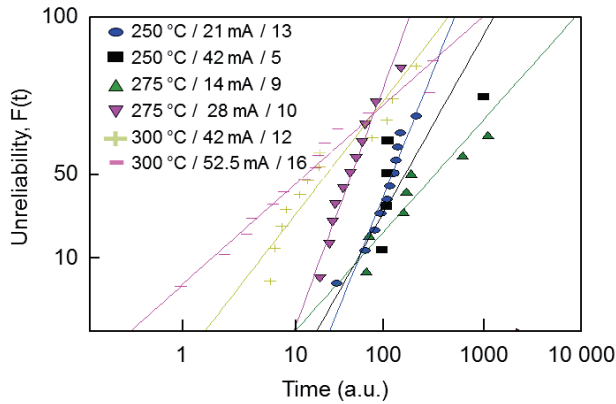


Figure 18. Lognormal probability plot for NIST A1 test structures with 20 nm high TiN barrier. Stress conditions are given, including temperature, current and sample sizes.

Table VI. Activation energy E_a and current exponent n of the Black's equation for NIST A1 structures with TaN/Ta and TiN diffusion barriers.

	E_a (eV)		n (n.a.)	
	TaN/Ta	TiN	TaN/Ta	TiN
NIST A1	1 ± 0.15	0.75 ± 0.7	0.87 ± 0.2	1.86 ± 1

more reliable than the Cu/TiN one. Furthermore, E_a values are comparable with the ones found for interface diffusion in Cu damascene interconnections. Despite the quite high uncertainty regarding parameter values for TiN samples, partly due to small sample sizes and some corrosion problems during EM tests, those encouraging results confirm that direct bonded copper lines act as standard BEoL interconnects thanks to an excellent bonding quality. Additional EM studies should however be conducting using a four-layer integration in order to investigate its influence on the Black's parameters.

V. CONCLUSION

We have successfully demonstrated that reliable 7 μm pitch daisy chain structures with four copper levels can be achieved with Cu-SiO₂ direct hybrid bonding. Extensive morphological characterizations of 3 μm $\times$ 3 μm bonding pads have been conducted after annealing at 200 and 400 °C for 2 h. Well closed Cu/Cu interfaces have been observed in both cases, aligned with submicron accuracy. Three possible origins for the non-critical voids present at this interface have been proposed, including surface roughness, lack of Cu at the Cu/TiN interface and diffusion of copper oxide along the bonding interface during the annealing. No copper diffusion was detected in the vicinity of the Cu/SiO₂ interface in the case of misaligned connections stored at 300 °C for 336 h. Along

with these results, electrical characterizations have proven that an annealing at 200 °C is sufficient to obtain outstanding electrical performance and functional yields. A thermal treatment at 400 °C offers the best results though, including a state-of-the-art contact resistivity of 123 m Ω . μm^2 . Additionally, most of the daisy chain structures successfully passed the environmental reliability tests, demonstrating the excellent resistance to corrosion and mechanical robustness of the four-layer high density daisy chains. Finally, electromigration studies have shown that fully bonded copper lines with two layers behave like bulk interconnects with TiN and TaN/Ta barriers, as the Cu/Cu bonding interface does not introduce any new failure mechanism. This proves the excellent electromigration resistance of the Cu/Cu interface after annealing at 400 °C.

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