

TECHNOLOGY AND APPLICATIONS OF THREE-DIMENSIONAL INTEGRATION

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ABSTRACT

Three-dimensional (3-D) integration holds tremendous potential to reduce global interconnect latency and power dissipation, and to improve integrated circuits (ICs) form factor. Moreover, it allows heterogeneous integration of different functional blocks (e.g., logic, memory, RF, etc) and materials (e.g., Silicon, SiGe, III-IV, etc). This paper explores the opportunities and challenges of a 3-D integration approach based on a silicon layer transfer process. It combines low temperature direct wafer bonding (Cu-to-Cu and SiO₂-to-SiO₂), high rate and selectivity silicon etching, and wafer de-bonding. A thorough description of process integration will be given and key technological challenges will be highlighted. In addition, CAD tools for 3-D ICs design and layout are being developed. Potential 3-D applications for system-on-a-chip (SoC) and related issues will be discussed.

INTRODUCTION

While dimensional scaling has consistently improved device gate switching delay, it has a reverse effect on global interconnects [1]. The global interconnects RC delay has increasingly become the circuit performance limiting factor especially in the deep sub-micron regime. Even though Cu/low-K material systems have been introduced to improve the interconnects RC delay, they are not a long-term solution. This is because the diffusion barrier material used in Cu metallization is of a finite thickness and has higher resistivity than Cu resulting in a higher effective resistivity than bulk Cu. The surface electron scattering effect and high operating temperature make the situation worse [2]. When chip size continues to increase to accommodate more functionality, the total interconnects length increases at the same time. This causes tremendous amount of power being dissipated unnecessarily in the interconnects. On chip signals also require more clock cycles to travel across the entire chip as a result of increasing chip size and operating frequency. To seek a long-term solution, the ITRS has outlined 3-D interconnects as one of the promising options that allows shorter global interconnects and hence improved RC delay [3]. Shorter global interconnects can also lower power

dissipation.

System-on-a-chip (SoC) is a potential solution to the mounting demand for functionality on a single chip. There are a few challenges associated with planar implementation of system-on-a-chip (SoC) on a single substrate. Each functional block has to be built in sequence and it is challenging to optimize each functional blocks on the same substrate. Substrate coupling might cause signals corruption between functional blocks [4]. 3-D integration is an attractive choice for SoC implementation as it allows integration of various functional blocks in a vertical fashion. In this way, each block can be optimized independently and stacked to form a 3-D system. Since there is no common substrate in this type of implementation, noise between blocks is expected to improve compared to a planar implementation. Improved form factor is another advantage 3-D integration can offer.

This paper discusses the opportunities for 3-D integration using a silicon layer transfer approach based on low temperature Cu-to-Cu and oxide-to-oxide wafer bonding. In addition, we will discuss computer-aided-design (CAD) tools development works intended for 3-D integration. We will also highlight potential 3-D applications, specifically system-on-a-chip application and benefits offered by 3-D integration in terms of noise and crosstalk reduction.

OVERVIEW OF 3-D RESEARCH

There are research efforts on a few possible technology options to realize a 3-D structure, either using recrystallization [5-6] or wafer bonding [7-9]. Subramanian *et al.* [5] reported 100-nm TFT devices having on-off current ratio $> 10^6$ and subthreshold slope of 107 mV/dec hence attesting the suitability of Germanium-seeding for fabrication of high performance TFT, suitable for use in vertically integrated three-dimensional (3-D) circuits. Chan *et al.* [6] used recrystallization of amorphous silicon by metal(Nickel)-induced-lateral-crystallization (MILC) to demonstrate a 3-D ring oscillator with lower propagation delay than that of a 2-D circuit.

While the recrystallization technique finds specific applications in memory devices, it is not suitable for other applications. Thermal budget imposed by the first layer and imperfect crystallization of the second layer make this technique less attractive. Another approach that is under intense research is the wafer bonding approach. The wafer bonding technique can be achieved by using a dielectric or a conductive layer at the bonding interface. Lu *et al.* [8] have demonstrated the potential of wafer bonding using dielectric glue (Flare) as a baseline process for 3-D interconnects. Using Low Temperature Oxide (LTO) bonding, Warner *et al.* [9] have fabricated operational 3-D ring oscillators and via chains.

Our 3-D approach is based on a silicon layer transfer method enabled by earlier works on low temperature direct Cu-to-Cu and oxide-to-oxide wafer bonding [7, 10].

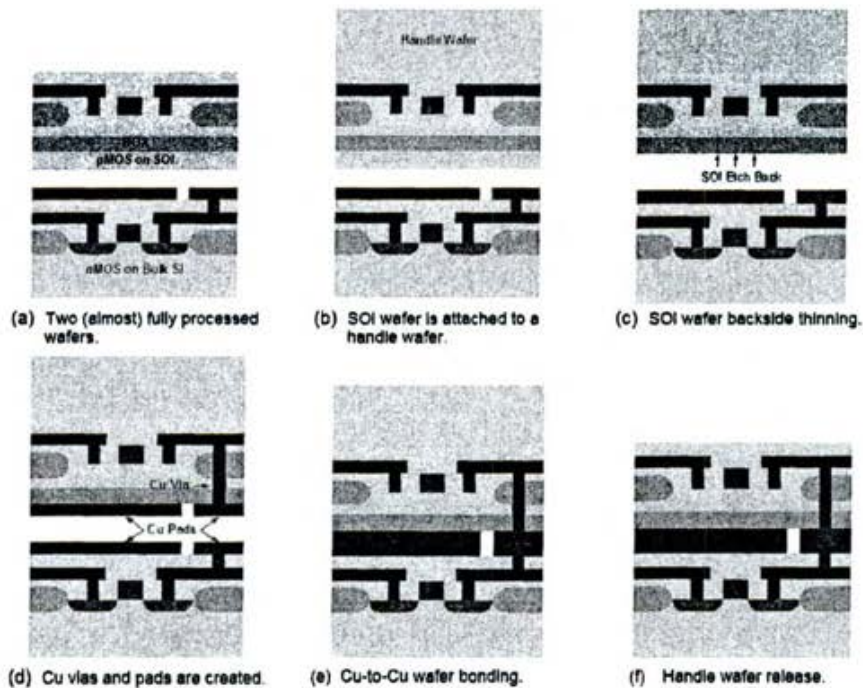


Figure 1: Process flow for 3-D integration scheme using Cu wafer bonding [11].

3-D PROCESS FLOW

Three-dimensional integrated circuit (3-D IC) is a vertical stack consisting of multiple device and interconnect layers that are connected by interlayer vertical vias. In our 3-D integration scheme, two front-end-of-line (FEOL) active device wafers are stacked in a back-to-face fashion and bonded by means of low temperature Cu-to-Cu thermo compression. Interlayer vertical vias electrically interconnect the device layers. Low temperature wafer bonding is necessary since the pre-bonding device layers already have Al metal interconnect lines. This is an attractive scheme because it allows lower aspect ratio interlayer vertical via and thinner bonding layer. We will briefly discuss the process sequence in this proposed 3-D integration scheme as illustrated in Fig. 1(a)-(f) and technological challenges will be highlighted.

Handle Wafer Attachment

Figure 1(a)-(f) depicts the process sequence to fabricate a 3-D CMOS inverter. The bottom device layer is an nMOS device fabricated on bulk Si while the top device layer is a pMOS device fabricated on SOI wafer independently prior to stacking. To start with, the front side of the top layer is attached to a handle wafer as shown in Fig. 1(b) to provide mechanical support for ease of wafer handling. Therefore, the bonding has to be strong enough to hold the SOI wafer during subsequent processes. Note that this bonding is a sacrificial one, as the handle wafer will be released from the final 3-D stack. This

dictates the ease of handle wafer release at the end. There are a few bonding options currently under investigation, either using an oxide-to-oxide [10] or metallic [12] bonding interface.

SOI Thin Back

In Fig. 1(c), the SOI substrate is thinned back after bonding to a handle wafer. A combination of mechanical grinding, plasma dry etch and chemical wet etch can be used for this thinning step. In order to achieve good etch stop behavior, it is typical to etch the final 50 to 100 μm of Si using wet chemical etch. The buried oxide (BOX) serves as the etch stop layer as there is an excellent selectivity between Si and oxide in wet etchants like KOH or TMAH [13]. The handle wafer has to be protected against chemical attack by SiN or SiO₂ coating.

Backside Vias and Bonding Pads Formation

Backside interlayer vertical vias and Cu pads are created on the thinned SOI wafer. Note that in this 3-D integration scheme, the requirement for via aspect ratio is relaxed as vias are formed on both wafers and connected. There are two sets of Cu pads. The first set is the via pads to form electrical connection between both device layers and the second set is the dummy pads to increase the bonding area hence increase the bonding strength. This is schematically shown in Fig. 1(d).

Low Temperature Cu Wafer Bonding

Figure 1(e) shows that the top device layer is aligned to the bottom device layer, presumably with Cu pads already created on it, and bonded at low temperature with a constant down force in an inert ambient. A final post-bonding annealing step allows inter-diffusion at the Cu-Cu interface and promotes grain growth. A more elaborate discussion on Cu wafer bonding will be given in the next section.

Handle Wafer Release

The handle wafer must be attached with a special adhesive that is: (a) strong enough to withstand vigorous shearing force from grinding, (b) chemically inert to hot aqueous hydroxide solutions, and (c) easily removed with another solution.

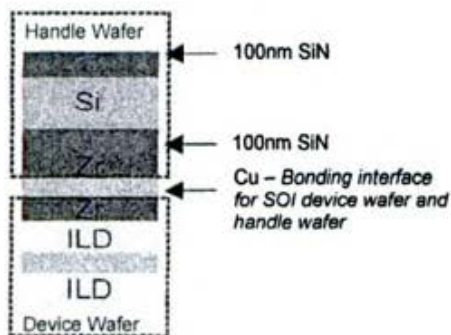


Figure 2: The use of Zr/Cu-to-Cu/Zr stack to bond SOI wafer to handle wafer.

Because hot basic solutions will usually delaminate organic polymers from their substrates, it is very difficult for CMOS-compatible polymer adhesives to satisfy all three criteria. However, these requirements can be met with a careful choice of metallic bonding layers; hence, one can use a copper-copper bond as the adhesion layer itself, while flanking layers of zirconium can be used as the “wafer release” medium. This is due to the fact that zirconium dissolves extremely rapidly in dilute HF (much faster than silicon dioxide). This handle wafer attachment scheme is shown below in Fig. 2.

In this scheme, the substrate is bonded to a handle wafer coated with 100 nm LPCVD nitride. On both the SOI substrate and the handle wafer, 150 nm zirconium and 300 nm copper are deposited in sequence. With no need for wafer-wafer alignment, the SOI and the nitride handler are simply bonded at 300-400 °C in vacuum with a persistent contact pressure of 4000 mbar for 30 min. The wafer pair may then undergo a further anneal in nitrogen, in which the Cu-Cu interface forms a strong bond that passes both the razor test [7, 14] and subsequent mechanical substrate grinding.

Alternatively, an oxide-oxide bond can be used to attach the handle wafer. This method has the advantage that the bond is materially distinct from the permanent Cu-Cu bond used for mechanical and electrical connectivity. In this layer transfer method, the finished SOI wafer is coated with 1-2 μm of Plasma-Enhanced Chemical Vapor Deposition oxide (PECVD oxide). Since the PECVD oxide is porous, a low temperature densification is performed at 350 °C for 12 hours in inert nitrogen ambient. This step allows degassing from the porous silicon dioxide, which is detrimental to the bonding, to take place prior to bonding. Surface smoothness is very critical to successful wafer bonding, and it is well known that the PECVD oxide has a very rough surface. Therefore, it is necessary to smoothen the oxide surface by means of chemical mechanical polishing (CMP). It is also essential to ensure that a particle-free post-CMP oxide surface. Since the SOI wafer-thinning step (silicon etching) comes partly in the form of a KOH chemical etch, the silicon handle wafer needs to be protected against KOH attack. So 500 nm of oxide is grown on the handle wafer. High-dose, high-energy H^+ ions are implanted into the handle wafer with the expected range of about 0.5 μm . Hydrogen plays a role in wafer exfoliation during handle wafer release. Prior to bonding, the SOI and the handle wafers are chemically cleaned, rinsed in deionized water, and dried. The two wafers are bonded face-to-face, i.e. thermal oxide (on the handle wafer) with PECVD oxide (on the

SOI wafer) bonding, with no requirement for precision alignment at room temperature. In order to enhance the bonding strength, the bonded pair will be annealed at 300 °C. We have successfully demonstrated the ability to bond thermal oxide to PECVD oxide with careful surface preparation [10]. We will present results on oxide wafer bonding work in the next section. The SOI wafer is ready for thinning now. Upon formation of vertical electrical vias and copper pads on the BOX, the SOI wafer is aligned to the bottom wafer (a finished wafer with copper bonding pads) and bonded. This can be done at 350 °C and 4000 mbar for 30 min. After bonding, the stack is annealed in nitrogen ambient for 30 min at 400 °C to allow copper grain growth that will enhance the bond. This step might potentially lead to handle wafer release as well. Under this condition, the hydrogen will cluster together and cause lateral cracking, thus releasing the handle wafer from the actual 3-D device stack. The remaining thin silicon (about 0.5 μm) can be stripped away easily by a five-second dip in KOH solution.

Using metal as bonding interface is an attractive choice because metal is a good heat conductor and this will help circumvent the heat dissipation problem encountered in 3-D IC. At the same time, a metal interface allows additional wiring and routing. Cu is a metal of choice because it is a mainstream CMOS material, and it has good electrical ($\rho_{\text{Cu}} = 1.7 \text{ m}\Omega\cdot\text{cm}$ vs $\rho_{\text{Al}} = 2.65 \text{ m}\Omega\cdot\text{cm}$) and thermal ($K_{\text{Cu}} = 400 \text{ W m}^{-1} \text{ K}^{-1}$ vs $K_{\text{Al}} = 235 \text{ W m}^{-1} \text{ K}^{-1}$) conductivities and longer electro-migration lifetime. Another advantage offered by metal bonding interface is that the metal layer can act as a ground shield if properly grounded hence better noise isolation between device layers on the stack.

COPPER WAFER BONDING

Since our 3-D integration is enabled by low temperature Cu-to-Cu wafer bonding, this section will be devoted to discussion on several aspects of it, including bonding mechanism and interfacial morphologies of bonded Cu-Cu layer.

In order to achieve a reliable Cu-Cu bonding for 3-D ICs application, both the electrical and structural properties of the bonded layer need to be taken into account. The bond strength, quality and interfacial morphologies under different bonding parameters must be studied carefully. The electrical performances such as the contact resistance of the bonded interconnect of different sizes and densities need to be investigated as well since they directly affect 3-D circuit performance. For best conditions of Cu wafer bonding in 3-D integration, blank Cu wafer bonding and bonded Cu interconnects were studied. In order to acquire the best bonding quality and bonding parameters, microstructures at the interfaces were examined by TEM and oxide distribution in the bonded layer was investigated with EDS [14]. The relationship between defects and the formation of the homogeneous bonded layer were discussed. In a "good" bonded wafer, the bonded layer became a homogeneous layer, and the oxide concentration is low and uniformly distributed. The interfacial morphologies of bonded layers and proposed mechanisms for copper wafer bonding were investigated [15]. The different interfacial morphologies and grain orientation during bonding were also analyzed. Figure 3(a)-(c) show TEM images of the Cu-Cu bonded layer and the major diffraction pattern of single

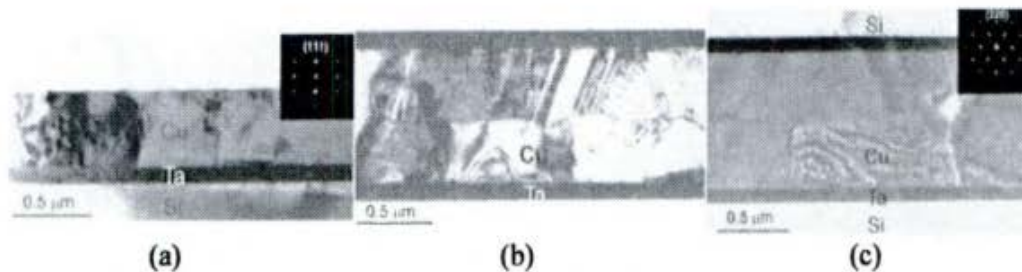


Figure 3 (a)-(c): XTEM images of the Cu-Cu bonded layer and the major diffraction pattern of single grains for selective area: (a) before bonding (b) after 30 min bonding (c) after 30 min bonding and annealing [16].

grains for selective area: (a) before bonding (b) after 30 min bonding (c) after 30 min bonding and annealing. It is surprising that there is an abnormal grain growth during bonding and annealing [16]. Since the resistance to electromigration is sensitive to the texture of Cu films, understanding and controlling Cu texture of the bonded layer is also essential. The effects of yielding and energy minimization is presented to explain the evolution of the preferred grain orientation.

TEM morphologies and the fraction of die failure during diesaw test are used to build a bond strength map under different bonding/annealing temperature and duration [17-19]. Figure 4 shows morphology and strength map for copper wafer bonding under different bonding temperatures and conditions.

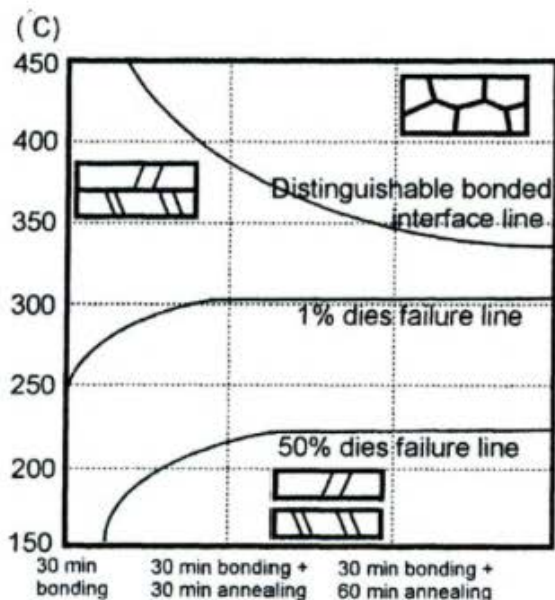


Figure 4: Morphology and strength map for copper wafer bonding under different bonding temperatures and conditions [19].

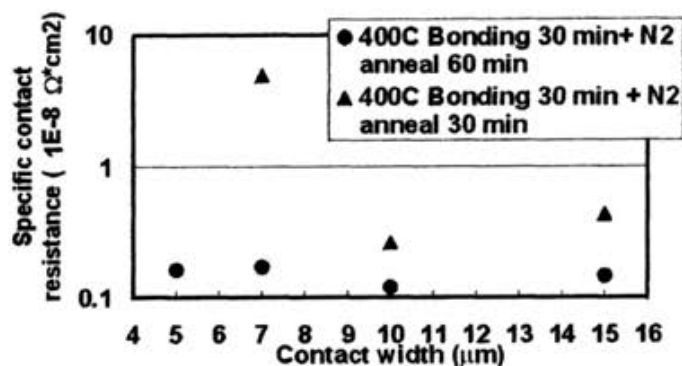


Figure 5: Average Cu-Cu bonded specific contact resistances as a function of interconnects size for different bonding conditions [20].

For bonded Cu interconnects, a novel and simple method to measure the contact resistance of the bonded interconnect is proposed. This new approach simplifies the fabrication process of the test structure and eliminates errors due to possible misalignments. The experimental results show reasonable specific contact resistances after bonding. Average Cu-Cu bonded specific contact resistances as a function of interconnect size for different bonding conditions is shown in Fig. 5. The specific contact resistance can be effectively reduced with a longer anneal time. At this bonding condition, it is observed that specific contact resistances of smaller size interconnects do not show higher value than larger size interconnects [20]. Contact resistance as a function of contact area and the location of the bonded interface on the wafer were also presented [8]. The specific contact resistance does not change when the stress current is increased or decreased as the bonded structure has reached a stable state. This shows excellent stability and reversibility of the bonded interconnects [21].

OXIDE WAFER BONDING

In this section, we describe low-temperature direct thermal oxide to Plasma-Enhanced Chemical Vapor Deposition (PECVD) oxide wafer bonding as a sacrificial bond for 3-D integration. PECVD oxide is an attractive choice as interlayer dielectric (ILD) because of its high deposition rate and its low temperature process. Wafer preparations and bonding steps are described in the above section on 3-D process flow.

To achieve high quality bonding, the root-mean-square (RMS) roughness of the wafers must be below 1.0 nm [22]. We have performed AFM surface scans on various wafers in the tapping mode on a D3000 unit from Digital Instruments. Table I summarizes the mean and RMS roughness of various wafers with different surface preparations estimated from AFM surface scans. The handle wafers with a layer of 5000 Å of thermal oxide exhibit an RMS roughness of 0.273 nm, and this value is acceptable for bonding. Hence the handle wafers do not require additional surface polishing.

Table I: Mean and RMS roughness of wafers with different surface preparations estimated from AFM [10].

Wafer Description	Mean Roughness (nm)	RMS Roughness (nm)
Bare Si wafer	0.097	0.143
5000Å SiO ₂ /Si	0.202	0.273
4μm PECVD SiO ₂ /SOI (As prepared)	7.929	9.757
4μm PECVD SiO ₂ /SOI (Annealed at 350°C for 16 hrs)	6.877	8.501
4μm PECVD SiO ₂ /SOI (Annealed at 350°C for 16 hrs + 3min CMP)	0.312	0.394

On the other hand, the RMS roughness of the as-deposited PECVD oxide on SOI dummy wafers is 9.757 nm. This value is too high for wafer bonding and the wafers need extra polishing to smoothen their surfaces. CMP has improved the surface roughness tremendously to a value of 0.394 nm after 3 min of polishing.

Figure 6 compares the 3μm x 3μm surface profiles of the as-deposited PECVD oxide and PECVD oxide that has undergone 16 hours of N₂ anneal at 350°C and 3 min of CMP. Note the obvious difference between the two wafers in terms of surface profile. The uneven surface profile of the as-deposited oxide film will limit the amount of surface area that can be in intimate contact with its pairing wafer, which in turn will degrade the quality of the bonding. The densified and polished wafer, on the other hand, is much more even and will promote better wafer bonding.

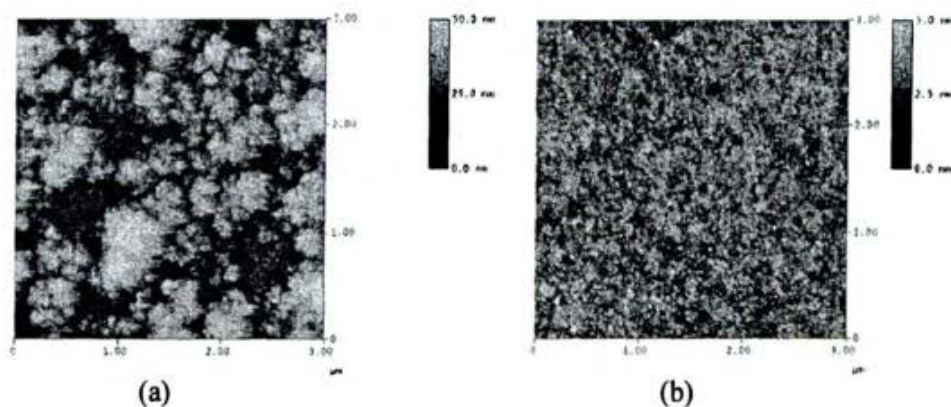


Figure 6: AFM scans for (a) as-deposited PECVD oxide, and (b) densified and polished PECVD oxide [10].

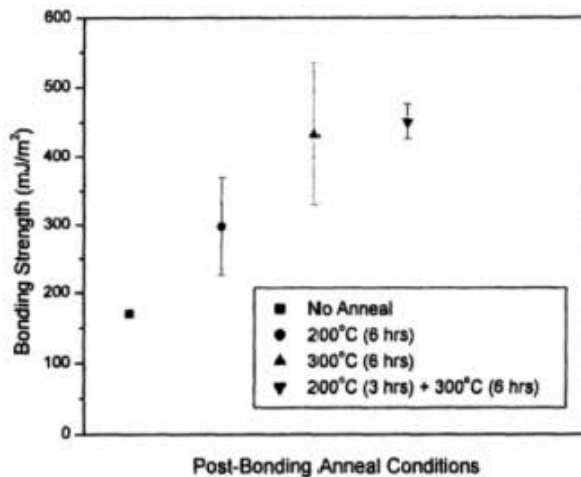


Figure 7: Bonding strength of the bonded wafer pairs with different post-bonding heat treatments [10].

When the oxide wafers are bonded at room temperature, the main force between them are from hydrogen bonds. Since hydrogen bonds between the bonded wafer pair are relatively weak, a heat treatment can be used to strengthen the bond. In this section, we will study the effect of post-bonding anneal on the bonding strength. We have used the Maszara's crack opening method to quantify the bond strength [23]. Figure 7 shows how bond strength evolves as a function of post-bonding anneal temperature. The bonding strength is only 170 mJ/m² after room temperature bonding and increases to 298 mJ/m² after a 6 hours anneal at 200°C. At 200°C, the OH groups on the oxide surfaces (from chemical clean prior to bonding) gain more surface mobility and more hydrogen bonds develop across the gap [12]. The reaction of surface silanol (Si-OH) groups also takes place during post bonding annealing:



The bonding strength is 432 mJ/m² after a 6 hours anneal at 300°C. This is because at higher temperature, reaction (1) is promoted and the water molecules gain more surface mobility and diffuse out of the bonding interface. As a result, the strong siloxane (Si-O-Si) bonds are formed. This shows that post-bonding anneal is useful in enhancing the bonding strength.

During wafer bonding, trapped air bubbles can cause undesired interface voids and this will affect the interface quality of the bonded wafer pair. Figure 8 shows IR images from the bonded wafer pairs before and after post-bonding anneal. Figures 5(a) and 8(b) are the IR images for wafer pair without pre-bonding densification of the PECVD oxide. It is evident that voids form in this wafer pair. The voids form possibly due to out-gassing from the undensified PECVD oxide during post-bonding anneal. However, the wafer pair with densified PECVD oxide bonds very well and no observable void is found from the IR images. The IR images for this wafer pair before and after post-bonding densification

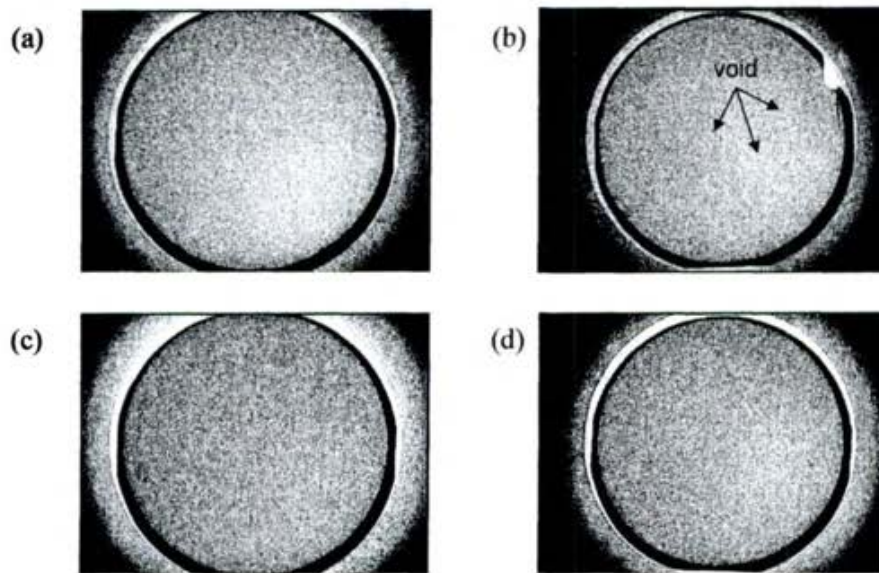


Figure 8: The effect of post-bonding annealing on bonding interface for: (a)-(b) wafer pair without densification on PECVD oxide, and (c)-(d) wafer pair with densification on PECVD oxide. (a) and (c) are IR images before annealing, and (b) and (d) are IR images after annealing [10].

are shown in Figs. 8(c) and 8(d) respectively. This suggests the importance of densification for successful bonding.

We concluded that low temperature bonding of PECVD oxide to thermal oxide is achievable with proper surface preparations. To ensure successful bonding, the PECVD oxide needs to be densified to prevent out-gassing and polished to smoothen its surface. The bonding strength of the wafer pair bonded at room temperature can be further improved by post-bonding anneal.

3-D CAD TOOLS DEVELOPMENT

Another aspect of our research concerns the digital design flow for 3-D integrated circuits. With a view towards full-system synthesis using 3-D technology, we are developing a set of design tools for 3-D integration. This effort comprises placement, routing, layout, and verification tools for 3-D digital integrated circuits. With the use of such tools, we will be able to verify and expand upon the predictions made by stochastic interconnect models for 3-D, in addition to being able to design and fabricate digital circuits for 3-D integration.

In order to adapt the conventional design flow for a 3-D integration technology, we have developed a standard-cell placement tool, global routing tool, and a layout editor for 3-D ICs [24,25]. Our standard-cell place-and-route tool, PR3D, operates on circuit netlists in GSRC [26] or Cadence LEF/DEF [27] formats, either of which may be generated from Verilog or VHDL descriptions of the circuits. The user specifies the number of device layers to be targeted, as well as the wire-length cost of inter-layer vias relative to the cost of 2-D wire (for example, if least interconnect power is the target, the cost of inter-layer vias may be given as the capacitance of such vias relative to the capacitance of a unit length of 2-D wire). The user also must choose whether to minimize the total wire length or to minimize the number of inter-layer vias (for technologies where the inter-layer wire pitch dominates over other factors such as capacitance). Placement is performed using a min-cut partitioning algorithm [28] that we have adapted for 3-D placement [24]. Once placement is complete, global routing is performed in order to localize the routes taken by nets in the circuit. In our 3-D global router, we must allocate area for inter-layer vias: in the face-to-back configuration, such vias present obstacles not only for device placement, but also for routing in first-level metal. We perform the allocation of routes, including inter-layer vias, using a hierarchical algorithm based on [29]. When the locations of inter-layer vias have been set, the individual layers of the placement may be passed to existing tools for detailed routing.

We have also extended the Berkeley layout editor Magic [30] to manage multiple-layer designs. Our tool, called 3-D Magic, automates the methodology introduced in [31] for 3-D IC design. 3-D Magic allows hand-design of 3-D integrated circuits, as well as manipulation of designs generated by our place-and-route tool. The display of inter-layer vias between the two relevant layers of the circuit is automated, and electrical-connectivity information for circuit nodes is maintained across all layers. 3-D Magic can also extract an entire 3-D circuit at once, using a user-configurable lumped-parameter model for the inter-layer interconnect. With this extraction, existing tools can be used to simulate circuit performance and close the design loop. In Figure 9, we show 3-D Magic layout of a Fast-Fourier-Transform (FFT) datapath that has been placed and routed in two device layers using our tools.

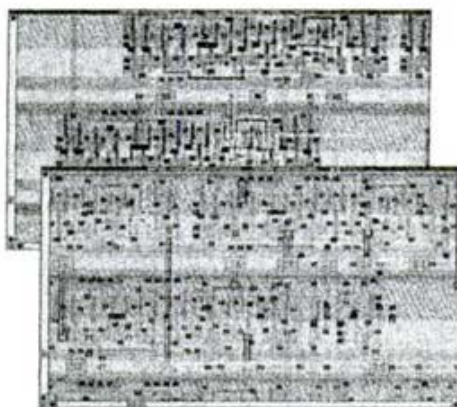


Figure 9: Two-wafer layout of a standard-cell circuit, as viewed in 3-D Magic.

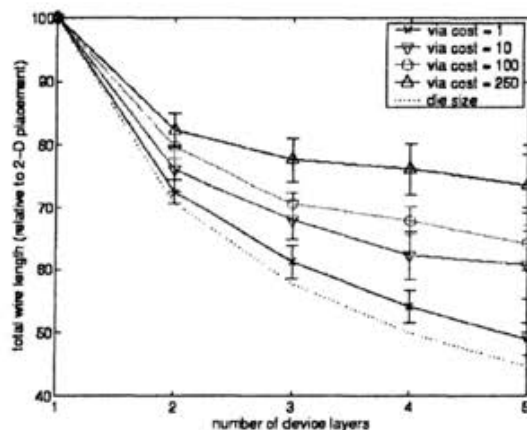


Figure 10: Total wire length (as a function of number of device layers) for various inter-layer via capacitances, obtained from placement. Total wire length is minimized by the placement tool. Via cost is the via capacitance expressed relative to the capacitance of one micron of metal wire.

Using our tools on the ISPD '98 set of 18 digital benchmark circuits [32], we have performed several analyses of the potential of 3-D integration [25]. For example, in Figure 10 we show the total wire length of the average of these circuits as a function of number of device layers, determined from placement. We observe that relative to a 2-D (conventional single-die) placement, 28% to 51% reduction in total wire length is possible; we expect that capacitance (and therefore energy consumption) follows the wire length. Furthermore, with our tool we can set the capacitance of an inter-layer via relative to the capacitance of an equal length of wiring from, say, metal 1. The four curves in the figure show quantitatively how as the inter-layer via capacitance increases, the benefit of 3-D integration decreases. We conclude that optimizing inter-layer interconnect is of key importance for 3-D integration technologies.

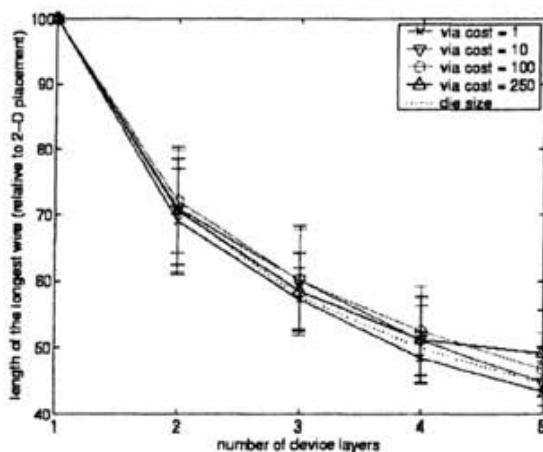


Figure 11: Length of the longest wire (as a function of number of device layers) for various inter-layer via capacitances. Total wire length is minimized by the placement tool. Via cost is the via capacitance expressed relative to the capacitance of one micron of metal wire.

Figure 11 shows length of the longest wire from the same analysis, where we observe up to 31% to 56% reduction in this length. We see that the longest wire is not affected strongly by the inter-layer via capacitance. We can also see that this length tracks the side length of the die fairly well.

3-D INTEGRATION FOR SYSTEM-ON-A-CHIP APPLICATIONS

3-D integration permits the realization of systems-on-a-chip (SoC) and can result in substantial performance improvements. For example, 3-D integration using bonding allows monolithic integration of disparate technologies. A device layer that is optimized for analog circuits could be combined with another device layer that is optimized for logic, yielding optimal system performance. Also, a significant challenge to mixed-signal design is substrate noise coupling generated by high-speed digital circuits. Analog circuits lack the large noise margins of digital circuit and thus are easily corrupted by substrate noise. 3-D integration mitigates this coupling by breaking the resistive connection that exists because of a shared substrate. Nearly perfect isolation can be achieved by fabricating the analog and digital systems on separate substrates while communicating through high-density vias. Furthermore, crosstalk within a digital block as a result of capacitive coupling of switching signals can also be reduced in a 3-D design. The additional capacitance due to the presence of another device layer diverts field lines from the wire-wire interaction, thus reducing the wire-wire coupling as depicted in Figure 12. In Figure 12, V_p is the voltage induced in a wire as a result of a switching voltage, V_{in} , in an adjacent wire.

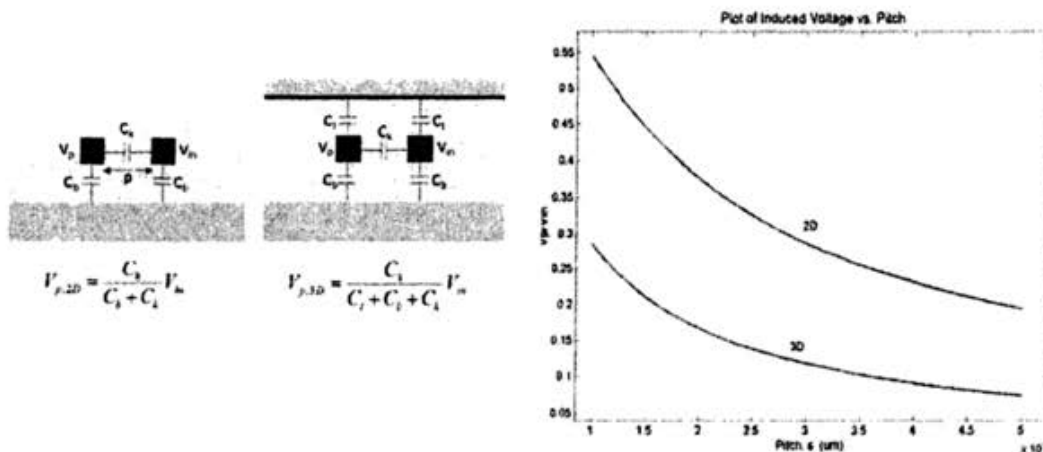


Figure 12: Crosstalk comparison in 2-D and 3-D structure [11].

CONCLUSIONS

We discussed the process flow for 3-D interconnects based on low temperature Cu-to-Cu wafer bonding. The impressive bonding properties of wafer using Cu thermo compression hold tremendous promise for 3-D IC integration. In particular, 3-D integration is an attractive technology for mixed-signal system-on-a-chip applications.

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