

USITC Inv. No. 337-TA-753 (U.S.Intern.Trade Com'n), 2012 WL 927056

United States International Trade Commission (U.S.I.T.C.)

*1 Administrative Law Judge Order

IN THE MATTER OF CERTAIN SEMICONDUCTOR CHIPS AND PRODUCTS CONTAINING SAME
INITIAL DETERMINATION ON VIOLATION OF SECTION 337 AND
RECOMMENDED DETERMINATION ON REMEDY AND BOND

USITC Inv. No. 337-TA-753

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March 2, 2012

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Pursuant to the Notice of Investigation, 76 Fed. Reg. 384 (2010), this is the Initial Determination of the in the matter of *Certain Semiconductor Chips And Products Containing Same*, United States International Trade Commission Investigation No. 337-TA-753. See 19 C.F.R. § 210.42(a).

It is held that no violation of section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337, has occurred in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain semiconductor chips and products containing same by reason of infringement of one or more of claims 11-13, 15, and 18 of U.S. Patent No. 6,470,405, claims 11-13 of U.S. Patent No. 6,591,353, claims 1-6, 11-13, 20-22, and 24 of U.S. Patent No. 7,287,109, claims 1, 2, 4-6, 9-13, 24-28, 31-36, 39-44, 47 and 49-53 of U.S. Patent No. 7,602,857 and claims 1-3, 6, 8, 25, 26, 30, 39, 40 and 42 of U.S. Patent No. 7,715,494.

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The following abbreviations may be used in this Initial Determination:

CDX	Complainants' demonstrative exhibit
CFF	Complainants' proposed findings of fact
CIB	Complainants' initial post-hearing brief
CORFF	Complainants' objections to Respondents' proposed findings of fact
COSFF	Complainants' objections to Staff's proposed findings of fact
CPX	Complainants' physical exhibit
CRB	Complainants' reply post-hearing brief
CX	Complainants' exhibit
Dep.	Deposition

JSUF	Joint Statement of Undisputed Facts
JX	Joint Exhibit
RDX	Respondents' demonstrative exhibit
RFF	Respondents' proposed findings of fact
RIB	Respondents' initial post-hearing brief
ROCFF	Respondents' objections to Complainants' proposed findings of fact
ROSFF	Respondents' objections to Staff's proposed findings of fact
RPX	Respondents' physical exhibit
RRB	Respondents' reply post-hearing brief
RRX	Respondents' rebuttal exhibit
RX	Respondents' exhibit
SFF	Staff's proposed findings of fact
SIB	Staff's initial post-hearing brief
SOCFF	Staff's objections to Complainants' proposed findings of fact
SORFF	Staff's objections to Respondents' proposed findings of fact
SRB	Staff's reply post-hearing brief
Tr.	Transcript

I. BACKGROUND

A. Institution and Procedural History of This Investigation

*4 By publication of a notice in the *Federal Register* on January 4, 2010, pursuant to subsection (b) of section 337 of the Tariff Act of 1930, as amended, the Commission instituted Investigation No. 337-TA-753 with respect to U.S. Patent Nos. 6,470,405; 6,591,353; 7,287,109; 7,602,857; 7,602,858; and 7,715,494¹ to determine:

[W]hether there is a violation of subsection (a)(1)(B) of section 337 in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain semiconductor chips and products containing same that infringe one or more of claims 11-13, 15, and 18 of the '405 patent; claims 11-13 of the '353 patent; claims 1, 2, 4, 5, 12, 13, 20, 21, and 24 of the '109 patent; claims 1, 2, 4-6, 9-13, 24-28, 31-36, 39-44, 47, and 49-53 of the '857 patent; claims 1, 2, 4, 7, and 20 of the '858 patent; and claims 1-3, 6, 8, 25, 26, 30, 39, 40, and 42 of the '494 patent, and whether an industry in the United States exists as required by subsection (a)(2) of section 337.

76 Fed. Reg. 384 (2010).

Rambus, Inc. ("Rambus") of Los Altos, California is the complainant. (*Id.*) The respondents named in the Notice of Investigation were: Freescale Semiconductor, Inc. of Austin, Texas ("Freescale"); Broadcom Corporation of Irvine, California; LSI Corporation of Milpitas, California; MediaTek, Inc. of Hsin-Chu, Taiwan; nVidia Corporation of Santa Clara, California; STMicroelectronics NV of Geneva, Switzerland; STMicroelectronics Inc. of Carrollton, Texas (all collectively "Supplier Respondents"); Asustek Computer, Inc. of Taipei City, Taiwan; Asus Computer International Inc. of Fremont, California; Audio Partnership PLC, of London, United Kingdom; Biostar Microtech (USA) Corp. of City of Industry, California; Biostar Microtech International Corp of Hsin Tien, Taiwan; Cisco Systems, Inc. of San Jose, California; Elitegroup Computer Systems of Taipei, Taiwan; EVGA Corporation of Brea, California; Galaxy Microsystems, Ltd. of Kowloon Bay, Hong Kong; Garmin International of Olathe, Kansas; GBT Inc. of City of Industry, California; Giga-Byte Technology Co., Ltd. of Taipei, Taiwan; Gracom Technologies LLC of City of Industry, California; Hewlett-Packard Company of Palo Alto, California; Hitachi Global Storage Technologies of San Jose, California; Jatón Corporation of Fremont, California; Jatón Technology TPE of His-Chih, Taiwan; Micro-Star International Co, Ltd. of Taipei Hsien, Taiwan; MSI Computer Corporation of City of Industry, California; Motorola, Inc. of Schaumburg, Illinois; Oppo Digital, Inc. of Mountain View, California; Palit Microsystems Ltd. of Taipei, Taiwan; Pine Technology Holdings, Ltd. of North Point, Hong Kong; Seagate Technology of Scotts Valley, California; Sparkle Computer Co., Ltd. of Taipei County, Taiwan; Zotac International (MCO) Ltd. of Shatin, N.T. Hong Kong; and Zotac USA Inc. of City of Industry, California (all collectively "Customer Respondents"). (*Id.*) The Commission Investigative Staff ("Staff") of the Commission's Office of Unfair Import Investigations is also a party in this investigation. (*Id.*)

*5 On June 20, 2011, the ALJ issued an order terminating Freescale from the investigation on the basis of settlement agreement. *See* Order No. 26 (June 20, 2011). The Commission determined not to review the order. *See* Notice of Commission Determination not to Review an Initial Determination Terminating the Investigation as to Respondent Freescale Semiconductor, Inc. Based on Settlement Agreement (July 13, 2011).

On August 10, 2011, the ALJ issued an order terminating the '858 Patent from the investigation. *See* Order No. 42 (August 10, 2011). The Commission determined not to review the order. *See* Notice of Commission Determination not to Review Initial Determination Terminating the Investigation as to Certain Asserted Patent Claims (September 9, 2011).

The evidentiary hearing on the question of violation of section 337 commenced on October 11, 2011, and concluded on October 20, 2011. Rambus, Supplier and Customer Respondents, and Staff were represented at the hearing. (Tr., 10:17-14:1.)

On January 17, 2012, the ALJ issued an order terminating respondent Broadcom Corporation from the investigation on the basis of a settlement agreement.² *See* Order No. 60 (January 17, 2012.) The Commission determined not to review the order. *See* Notice Of Commission Decision Not To Review An Initial Determination Terminating A Respondent On The Basis Of A Settlement Agreement (February 7, 2012).

On February 22, 2012, the ALJ issued two orders: (1) an order terminating respondent NVIDIA Corporation from the investigation on the basis of a settlement agreement and (2) an order terminating NVIDIA customer respondents from the investigation on the basis of the aforementioned settlement agreement.³ *See* Order Nos. 62 (February 22, 2012.) Those decisions are still pending before the Commission.

B. The Parties

Rambus

Rambus is a Delaware corporation with a principal place of business in Los Altos, California. (Complaint, ¶18.)

LSI

Respondent LSI Corporation (“LSI”) is a Delaware Corporation with a principal place of business in Milpitas, California. (LSI Corporation's Second Amended Response to Complaint Under Section 337 of the Tariff Act of 1930, as Amended, and to the Notice of Investigation, at ¶162(Oct. 28, 2011).)

MediaTek

Respondent MediaTek Inc. (“MediaTek”) is a Taiwanese corporation with a principal place of business in Hsin-Chu, Taiwan. (Amended Response of MediaTek Inc. to Complaint Under Section 337 of the Tariff Act of 1930, as Amended, and Notice of Investigation, at ¶208 (Oct. 20, 2011).)

STM

Respondent STMicroelectronics N.V. is a Netherlands corporation with a principal place of business in Geneva, Switzerland and respondent STMicroelectronics Inc. is a Delaware corporation (and an indirect wholly-owned subsidiary of STMicroelectronics N.V.) having a principal place of business in Carrollton, Texas (collectively “STM.”). (Second Amended Response of STMicroelectronics Inc. and STMicroelectronics N.V. to Complaint Under Section 337 of the Tariff Act of 1930, as Amended, and Notice of Investigation, EDIS Doc. ID 462260 at ¶252 (Oct. 24, 2011).)

ASUS

*6 Respondent ASUSTek Computer Inc. is a Taiwanese corporation with a principal place of business in Taipei, Taiwan and respondent ASUS Computer International Inc. is a California corporation (and a wholly-owned subsidiary of ASUSTek Computer Inc.) with a principal place of business in Fremont, California (collectively “ASUS”). (The ASUS Respondents' Response to Rambus Inc.'s Complaint and the Commission's Notice of Investigation, at ¶298 (Feb. 1, 2011).)

Audio Partnership

Respondent Audio Partnership PLC is a British corporation with a principal place of business in London, United Kingdom. (Amended Response of Audio Partnership PLC to Complaint Under Section 337 of the Tariff Act of 1930, as Amended, and Notice of Investigation, at ¶333 (Oct. 20, 2011).)

Cisco

Respondent Cisco Systems Inc. is a California corporation with a principal place of business in San Jose, California. (Amended Response of Cisco Systems Inc. to Complaint Under Section 337 of the Tariff Act of 1930, as Amended, and Notice of Investigation, at ¶374 (Oct. 20, 2011).)

Garmin

Respondent Garmin International, Inc. is a Kansas corporation with a principal place of business in Olathe, Kansas. (Amended Response to Complaint and Notice of Investigation by Respondent Garmin International Inc., at ¶482 (Oct. 21, 2011).)

HP

Respondent Hewlett Packard Company is a Delaware corporation with a principal place of business in Palo Alto, California. (Respondent Hewlett-Packard Company's Response to Rambus Inc.'s Complaint and the Commission's Notice of Investigation, at ¶523 (Feb. 1, 2011).)

Hitachi

Respondent Hitachi Global Storage Technologies Inc. is a Delaware corporation with a principal place of business in San Jose, California. (Amended Response of Respondent Hitachi Global Storage Technologies, Inc. to the Complaint and Notice of Investigation, at ¶562 (Oct. 26, 2011).)

Motorola

Respondent Motorola Mobility, Inc. is a Delaware corporation with a principal place of business in Libertyville, Illinois. (Amended Response of Motorola Mobility, Inc. to Complaint Under Section 337 of the Tariff Act of 1930, as Amended, and Notice of Investigation, at ¶642 (Oct. 20, 2011).)

Oppo Digital

Respondent Oppo Digital, Inc. is a California corporation with a principal place of business in Mountain View, California. (Amended Response of Oppo Digital, Inc. to Complaint Under Section 337 of the Tariff Act of 1930, as Amended, and Notice of Investigation, at ¶675 (Oct. 20, 2011).)

Seagate

Respondent Seagate Technology LLC is a Delaware corporation with a principal place of business in Scotts Valley, California. (Seagate Technology's Second Amended Response to Complaint Under Section 337 of the Tariff Act of 1930, as Amended, and to the Notice of Investigation, at ¶739 (Oct. 28, 2011).)

C. The Patents at Issue and Overview of the Technology

*7 The Barth Patents are generally directed at memory devices and their associated memory controllers as used, for example, in personal computers (PCs), gaming consoles, mobile devices, and the like. (Complaint, ¶¶23-25; CX-9543C, Przybylski Direct at Q&A 66.) This investigation is particularly focused on the memory controllers of consumer electronics that interface with memory devices compliant with industry standards promulgated by the Joint Electron Device Engineering Council ("JEDEC"). (CX-9543C, Przybylski Direct Q&A 40-42, 273, 280-296.) Implicated standards include JEDEC's Double Data Rate ("DDR") memory technology standards, such as JEDEC's DDR, DDR2, DDR3, Graphics DDR3 ("GDDR3"), Low Power DDR ("LPDDR") and LPDDR2 standards (collectively, the "Accused JEDEC Standards"). (CX-9543C, Przybylski Direct Q&A 38, 74.) The Accused JEDEC Standards specify the signaling associated with certain memory device operations, as well as certain physical characteristics of the interfaces for connecting a memory device to an associated memory controller. (CX-9543C, Przybylski Direct Q&A 39-42.)

The Dally patents are generally directed at the use of equalization techniques within transmitter circuits of PCs, gaming consoles, mobile devices and the like. (Complaint, ¶¶26-27; CX-9542C, Singer Direct at Q&A 40-53; Singer, Tr. 571:02-08.) This investigation are particularly focused on the transmitter circuitry of consumer electronics that are compliant with industry standards promulgated by various entities. (CX-9542C, Singer Direct at Q&A 54.) Implicated standards include PCI Express, DisplayPort, Serial Advanced Technology Attachment (SATA), and Serial Attached Small Computer System Interface (SAS) (collectively, the "Accused Transmitter Standards"). (CX-9542C, Singer Direct at Q&A 54-74.) The Accused Transmitter Standards specify certain signaling parameters associated with various interfaces. (CX-9542C, Singer Direct Q&A 54-74.)

The Barth Patents

a) The '405 Patent

U.S. Patent No. 6,470,405 (“the ‘405 Patent”), entitled “Protocol for Communication With Dynamic Memory,” was filed on May 29, 2001, and issued on October 22, 2002. (JX-3 (the ‘405 Patent)). Richard M. Barth, Fredrick A. Ware, John B. Dillon, Donald C. Stark, Craig E. Hampel, and Matthew M. Griffin are the named inventors of the ‘405 Patent, and complainant Rambus is the named assignee. (*Id.*)

The asserted claims of the ‘405 Patent are claims 11-13, 15, and 18. These claims read as follows:

11. A method of controlling a semiconductor memory device, wherein the memory device includes an array of memory cells, the method comprises: providing a plurality of control codes to the memory device wherein the plurality of control codes include a first code which specifies that a write operation be initiated in the memory device and a second code which specifies that a precharge operation be initiated automatically after initiation of the write operation; delaying for an amount of time after providing the plurality of control codes; and issuing an external strobe signal to the memory device after delaying for the amount of time, to signal the memory device to sample data, wherein the data is to be written to the array during the write operation.

*8 12. The method of claim 11 further comprising issuing a first portion of the data and a second portion of the data to the memory device, wherein the first portion of the data is sampled during an odd phase of an external clock signal, and the second portion of the data is sampled during an even phase of the external clock signal.

13. The method of claim 12 wherein the first and second portions of the data are both issued during a first clock cycle of the external clock signal.

15. The method of claim 11 further comprising providing address information to the memory device.

18. The method of claim 11 wherein the plurality of control codes includes a third code which specifies that a row of sense amplifiers be activated.

The ‘405 patent generally discloses and claims a system and method for performing data transfers within a computer system. (*Id.*)

b) The ‘353 Patent

U.S. Patent No. 6,591,353 (“the ‘353 Patent”), entitled “Protocol for Communication With Dynamic Memory,” was filed on May 1, 2000, and issued on July 8, 2003. (JX-4 (the ‘353 Patent)). Richard M. Barth, Fredrick A. Ware, John B. Dillon, Donald C. Stark, Craig E. Hampel, and Matthew M. Griffin are the named inventors of the ‘353 Patent, and complainant Rambus is the named assignee. (*Id.*)

The asserted claims of the ‘353 Patent are claims 11-13. These claims read as follows:

11. A method of controlling a memory device that includes a plurality of memory cells, the method comprising: issuing a first write command to the memory device, the memory device being configured to defer sampling data that corresponds to the first write command until a strobe signal is detected; delaying for a first time period after issuing the write command; and after delaying for the first time period, issuing the strobe signal to the memory device to initiate sampling of a first portion of the data by the memory device.

12. The method of claim 11, further comprising issuing the first portion of the data and a second portion of the data to the memory device, wherein the first portion of the data is sampled during an odd phase of an external clock signal, and the second portion of the data is sampled during an even phase of the external clock signal.

13. The method of claim 12, wherein the first and second portions of the data are both issued during a common clock cycle of the external clock signal.

The '353 Patent generally discloses and claims a method and apparatus for controlling data transfers to and from a dynamic random access memory. (*Id.*)

c) The '109 Patent

U.S. Patent No. 7,287,109 ("the '109 Patent"), entitled "Method Of Controlling A Memory Device Having A Memory Core," was filed on October 15, 2004, and issued on October 23, 2004. (JX-5 (the '109 Patent)). Richard M. Barth, Fredrick A. Ware, John B. Dillon, Donald C. Stark, Craig E. Hampel, and Matthew M. Griffin are the named inventors of the '109 Patent, and complainant Rambus is the named assignee. (*Id.*)

***9** The asserted claims of the '109 Patent are claims 1, 2, 4, 5, 12, 13, 20, 21 and 24. These claims read as follows:

1. A method of controlling a memory device having a memory core, wherein the method comprises: providing control information to the memory device, wherein the control information includes a first code which specifies that a write operation be initiated in the memory device; providing a signal to the memory device, wherein the signal indicates when the memory device is to begin sampling write data, wherein the write data is stored in the memory core during the write operation; providing a first bit of the write data to the memory device during an even phase of a clock signal; and providing a second bit of the write data to the memory device during an odd phase of the clock signal.

2. The method of claim 1, wherein the control information further includes: address information that specifies a location in the memory core for the write operation; a second code that specifies whether to perform a sense operation; and a third code that specifies whether to perform a precharge operation.

4. The method of claim 1, wherein the memory core includes a plurality of banks, wherein each bank of the plurality of banks includes a memory cell array, wherein the method further includes: transmitting bank selection information to the memory device, wherein the bank selection information identifies a bank of the plurality of banks, wherein the write operation is initiated in a subset of the memory cell array included in the bank identified by the bank selection information; and transmitting address information to the memory device, wherein the address information identifies the subset of the memory cell array.

5. The method of claim 4, wherein the control information further includes a second code which specifies that a precharge operation be initiated in the bank identified by the bank selection information after the write data is written to the subset of the memory cell array.

12. A method of controlling a memory device, wherein the memory device includes a plurality of banks, wherein each bank of the plurality of banks includes a memory cell array, wherein the method comprises: providing a plurality of operation codes to the memory device, wherein the plurality of operation codes includes a first code which specifies that a write operation be initiated in the memory device; providing bank selection information to the memory device, wherein the bank selection information identifies a bank of the plurality of banks, wherein the write operation is initiated in the memory cell array included in the bank identified by the bank selection information; providing address information to the memory device, wherein the address information identifies where to initiate the write operation in the memory cell array included in the bank identified by the bank selection information; providing a signal to the memory device, wherein the signal indicates when the memory device is to begin receiving write data to be written during the write operation; providing a first bit of the write data to the memory device during an even phase of a clock signal; and providing a second bit of the write data to the memory device during an odd phase of the clock signal.

***10** 13. The method of claim 12, wherein the plurality of operation codes further includes a second code which specifies that a precharge operation be initiated in the bank identified by the bank selection information after the write data is written during the write operation.

20. A method of controlling a memory device having a memory core, wherein the method comprises: providing control information to the memory device, wherein the control information includes a first code which specifies that a transfer operation be initiated with the memory device; providing a signal to the memory device, wherein the signal indicates when the memory device is to begin the transfer operation; and during the transfer operation, transferring a first bit of data during an even phase of a clock signal, and transferring a second bit of data during an odd phase of the clock signal.

21. The method of claim 20, wherein the control information further includes: address information that specifies a memory location of the data; and a second code that specifies whether to perform a sense operation, wherein the data is transferred from a row of the memory core to a plurality of sense amplifiers when a sense operation is performed.

24. The method of claim 20, wherein the transfer operation is a write operation.

The '109 Patent generally discloses and claims a method and apparatus for controlling data transfers to and from a dynamic random access memory. (*Id.*)

The Dally Patents

d) The '857 Patent

U.S. Patent No. 7,602,857 ("the '857 Patent"), entitled "Digital transmitter," was filed on August 31, 2006, and issued on October 13, 2009. (JX-122 (the '857 Patent)). William J. Dally is the named inventor of the '857 Patent. (*Id.*)

The asserted claims of the '857 Patent are claims 1, 2, 4-6, 9-13, 24-28, 31-36, 39-44, 47 and 49-53. These claims read as follows:

1. A component comprising: a semiconductor chip; a processor within the chip; and a transmitter circuit within the chip, the transmitter circuit being coupled to the processor to accept a digital input signal including a plurality of digital values from the processor, the transmitter circuit being operable to send an output signal including a series of signal levels representing the digital values and to emphasize high frequency components of the output signal relative to low frequency components of the output signal so that: (i) an output bit signal of the output signal representing a particular bit value has one signal level when the bit value is the same as a bit value represented by a predetermined preceding output bit signal; and (ii) the output bit signal representing the particular bit value has another signal level when the bit value is different from the bit value represented by the predetermined preceding output bit signal.

2. The component as claimed in claim 1 wherein the transmitter circuit is operable to send the output signal with an output frequency of at least 1 GHz and a bandwidth greater than 100 MHz.

*11 4. The component as claimed in claim 1 wherein the transmitter circuit is operable to emphasize signal levels representing values following transitions between values relative to signal levels representing repeated values.

5. The component as claimed in claim 1 wherein the chip has I/O connections and the transmitter circuit is coupled to one or more of the I/O connections to send the output signal through the one or more I/O connections.

6. The component as claimed in claim 5 wherein the transmitter circuit is operable to send the output signal in nonmodulated form.

9. The component as claimed in claim 1 wherein each digital value is represented by one of the signal levels in the output signal.

10. The component as claimed in claim 1 wherein the digital input signal includes a plurality of bits and each bit of the digital input signal is represented by one of the signal levels in the output signal.

11. The component as claimed in claim 1 further comprising at least one additional transmitter circuit within the chip, each additional transmitter circuit being coupled to the processor and operable to accept an additional digital input signal from the processor and send an additional output signal representing such additional input signal.

12. The component as claimed in claim 11 wherein the chip has I/O connections and the transmitter circuits are coupled to a plurality of the I/O connections and operable to send the output signals through the I/O connections.

13. The component as claimed in claim 11 wherein the transmitter circuits are operable to provide output signals representing a parallel stream of data from the processor.

24. A component comprising: a semiconductor chip; a component circuit within the chip; and a transmitter circuit within the chip, the transmitter circuit being coupled to the component circuit to accept a digital input signal including a plurality of digital values from the component circuit, the transmitter circuit being operable to send an output signal including a series of signal levels representing the digital values and to emphasize high frequency components of the output signal relative to low frequency components of the output signal; wherein each digital value in the digital input signal is represented by one of the signal levels in the output signal and the transmitter circuit is operable to select each signal level as a function of the digital value represented by that signal level and of the digital values represented by one or more preceding signal levels.

25. The component as claimed in claim 24 wherein the component circuit is a processor.

26. The component as claimed in claim 24 wherein the transmitter circuit is operable to emphasize signal levels representing values following transitions between values relative to signal levels representing repeated values.

27. The component as claimed in claim 24 wherein the chip has I/O connections and the transmitter circuit is coupled to one or more of the I/O connections to send the output signal through the one or more I/O connections.

*12 28. The component as claimed in claim 27 wherein the transmitter circuit is operable to send the output signal in nonmodulated form.

31. The component as claimed in claim 24 wherein the transmitter circuit is operable to send the output signal with an output frequency of at least 1 GHz and a bandwidth greater than 100 MHz.

32. The component as claimed in claim 24 further comprising at least one additional transmitter circuit within the chip, each additional transmitter circuit being coupled to the component circuit and operable to accept an additional digital input signal from the component circuit and send an additional output signal representing such additional input signal.

33. The component as claimed in claim 32 wherein the chip has I/O connections and the transmitter circuits are coupled to a plurality of the I/O connections and operable to send the output signals through the I/O connections.

34. The component as claimed in claim 33 wherein the transmitter circuits are operable to provide output signals representing a parallel stream of data from the component circuit.

35. A component comprising: a semiconductor chip; a component circuit within the chip; and a transmitter circuit within the chip, the transmitter circuit being coupled to the component circuit to accept a digital input signal including a plurality of digital values from the component circuit, the transmitter circuit being operable to send an output signal including a series of signal levels representing the digital values and to emphasize high frequency components of the output signal relative to low frequency components of the output signal; wherein each digital value in the digital input signal is represented by one of the signal levels in the output signal and the transmitter circuit is operable to select each signal level as a function of the digital value represented by that signal level and the digital value represented by the immediately preceding signal level.

36. The component as claimed in claim 35 wherein the component circuit is a processor.

39. A component comprising: a semiconductor chip; a component circuit within the chip; and a transmitter circuit within the chip, the transmitter circuit coupled to the component circuit and operable to accept a digital input signal including a plurality of bit values from the component circuit and send an output signal representing the digital input signal, the output signal including a series of output bit signals having signal levels so that: (i) an output bit signal of the output signal representing a particular bit value has one signal level when the bit value is the same as a bit value represented by a predetermined preceding output bit signal; and (ii) the output bit signal representing the particular bit value has another signal level when the bit value is different from the bit value represented by the predetermined preceding output bit signal.

40. The component as claimed in claim 39 wherein the component circuit is a processor.

*13 41. The component as claimed in claim 39 wherein the transmitter circuit is operable to select each signal level as a function of the bit value represented by that signal level and of the bit values represented by one or more preceding signal levels.

42. The component as claimed in claim 39 wherein the transmitter circuit is operable to select each signal level as a function of the bit value represented by that signal level and the bit value represented by the immediately preceding signal level.

43. The component as claimed in claim 39 wherein the chip has I/O connections and the transmitter circuit is coupled to one or more of the I/O connections to send the output signal through the one or more I/O connections.

44. The component as claimed in claim 43 wherein the transmitter circuit is operable to send the output signal in nonmodulated form.

47. The component as claimed in claim 39 wherein each bit value in the digital input signal is represented by one of the signal levels in the output signal.

49. The component as claimed in claim 39 wherein the transmitter circuit is operable to send the output signal with an output frequency of at least 1 GHz and a bandwidth greater than 100 MHz.

50. The component as claimed in claim 39 further comprising at least one additional transmitter circuit within the chip, each additional transmitter circuit being coupled to the component circuit and operable to accept an additional digital input signal from the component circuit and send an additional output signal representing such additional input signal.

51. The component as claimed in claim 50 wherein the chip has I/O connections and the transmitter circuits are coupled to a plurality of the I/O connections and operable to send the output signals through the I/O connections.

52. The component as claimed in claim 51 wherein the transmitter circuits are operable to provide output signals representing a parallel stream of data from the component circuit.

53. The component as claimed in claim 39 wherein the transmitter circuit is operable to select each signal level as a function of only the bit value represented by that signal level and the bit value represented by the immediately preceding signal level.

The '857 Patent is generally directed to an equalizer in a digital transmitter that compensates for attenuation in a signal channel to a digital receiver. (*Id.*)

e) The '494 Patent

U.S. Patent No. 7,715,494 ("the '494 Patent"), entitled "Digital transmitter," was filed on August 31, 2006, and issued on May 11, 2010. (JX-121 (the '494 Patent)). William J. Dally is the named inventor of the '494 Patent. (*Id.*)

The asserted claims of the '494 Patent are claims 1-3, 6, 8, 25, 26, 30, 39, 40 and 42. These claims read as follows:

1. A circuit comprising: a semiconductor chip; a transmitter circuit within the chip, the transmitter circuit being operable to accept a digital input signal including a plurality of bits and send an output signal including a series of output bit signals, each bit of the digital input signal being represented by a single output bit signal, the transmitter circuit generating a sign which depends upon the value of the bit represented by such output bit signal and generating a magnitude which is a function of the value of the bit represented by such output bit signal and the values of the bits represented by one or more preceding output bit signals, each output bit signal having sign and magnitude determined by the generated sign and generated magnitude.

*14 2. The circuit as claimed in claim 1 wherein the function is such that an output bit signal representing a bit having a value different from the value of the bits represented in the one or more preceding output bit signals has a greater magnitude than an output bit signal representing a bit having the same value as the bits represented by the one or more preceding output bit signals.

3. The circuit as claimed in claim 1 wherein the transmitter is operable to provide the output signal with an output frequency of at least 1 GHz and a bandwidth greater than 100 MHz.

6. The circuit as claimed in claim 1 wherein the transmitter circuit is operable to select the magnitude of each output bit signal based only on the value of the bit represented by that output bit signal and the value of the bit represented by the immediately preceding output bit signal.

8. The circuit as claimed in claim 1 wherein the function is reprogrammable.

25. A circuit comprising: a semiconductor chip; and a transmitter circuit within the chip, the transmitter circuit being operable to accept a digital input signal including a plurality of bits and send a differential output signal including a series of output bit signals, each bit of the digital input signal being represented by a single output bit signal; where the transmitter circuit drives the series of output bit signals to have sign represented by logic level of a first bit that is to be transmitted, and magnitude represented by whether the first bit represents a common logic level relative to an immediately previous bit, the magnitude being driven to be relatively smaller when the first bit has a common logic level with the immediately previous bit, and to be relatively larger when the first bit does not have the common logic level.

26. The circuit of claim 25, where the chip includes plural of said transmitter circuits, each transmitter circuit to output a respective series of output bit signals on lines of a parallel bus.

30. The circuit of claim 25, where the series of output signals is transmitted by the transmitter onto a signal path at a rate of at least 400 megahertz.

39. A method of operation in an integrated circuit having a transmitter, the method comprising: accepting a digital input signal including a plurality of bits and sending a differential output signal including a series of output bit signals, each bit of the digital input signal being represented by a single output bit signal; using the transmitter to drive the series of output bit signals to have sign represented by logic level of a first bit that is to be transmitted, and magnitude represented by whether the first bit represents a common logic level relative to an immediately previous bit, the magnitude being relatively smaller when the first bit has a common logic level with the immediately previous bit, and being relatively larger when the first bit does not have the common logic level.

40. The method of claim 39, where the integrated circuit includes plural of said transmitters, the method further comprising using each transmitter circuit to output a respective series of output bit signals on a respective line of a parallel bus.

*15 42. The method of claim 39, further comprising driving the series of output signals using the transmitter onto a signal path at a rate of at least 400 megahertz.

The '494 Patent is generally directed to an equalizer in a digital transmitter that compensates for attenuation in a signal channel to a digital receiver. (*Id.*)

D. The Products At Issue

The accused products are memory controllers that are designed to interface with DDR, DDR2, DDR3, GDDR3, LPDDR or LPDDR2 compliant memory devices and products incorporating such a controller that infringe the Barth Patents ("the Accused Barth Products"). (Complaint, ¶¶122, 125, 129, 134, 139 (Broadcom accused products); *id.* at ¶¶166, 169, 172, 177, 182 (LSI accused products); *id.* at ¶¶212, 214, 217, 222 (MediaTek accused products); *id.* at ¶¶256, 259, 263, 268, 273 (STM accused products); CX-9543C, Przybylski Direct Q&A 75-90 (Broadcom accused products); *id.* at Q&A 91-113 (LSI accused products); *id.* at Q&A 114-132 (MediaTek accused products); *id.* at Q&A 133-162 (STM accused products); *id.* at Q&A 163256 (accused downstream products); Stipulation Regarding Representative Broadcom Accused Products, at 2 (June 17, 2011) ("Broadcom Slip"); Smith, Tr. 896:10-897:01 (LSI accused products); *id.* at 898:15-899:02 (Seagate accused products); RX-5505C, Salem Rebuttal Q&A 12-16 (Broadcom accused products).)

The accused products also include interface chips that are designed according to PCI Express, DisplayPort, SATA, and SAS interface standards and products incorporating such an interface chip that infringe the Dally Patents ("the Accused Dally Products"). (Complaint at ¶¶123, 125, 146, 152, 158 (Broadcom accused products); *id.* at ¶¶167, 169, 189, 190, 196, 197, 203, 204 (LSI accused products); *id.* at ¶¶231, 233, 239, 244, 249 (nVidia accused products); *id.* at ¶¶257, 259, 280, 286, 292 (STM accused products); CX-9542C, Singer Direct Q&A 75-86 (Broadcom accused products); *id.* at Q&A 87-96 (LSI accused products); *id.* at Q&A 97-100 (nVidia accused products); *id.* at Q&A 101-104 (STM accused products); *id.* at Q&A 105-110 (downstream accused products); Singer, Tr. 753:25-755:12, 765:10-766:11 (LSI accused products); Ozguc, Tr. 1186:24-1187:05 (nVidia accused products); RX-6271C, Ozguc Rebuttal Q&A 19 (nVidia accused products); Singer, Tr. 674:19-25 (Cisco accused products).)

II. IMPORTATION OR SALE

The ALJ finds that the importation or sale requirement of section 337 has been satisfied. Rambus has entered into a series of stipulations with certain respondents. (CX-9027C, Garmin Stip at 1-3; Stipulation Between Rambus and Cisco Systems, Inc., EDIS Doc. ID 460973 at ¶3 (Oct. 5, 2011) ("Cisco Stip"); Stipulations Regarding ASUS, EDIS Doc. ID 460646 at 1 (Sept. 1, 2011) ("ASUS Stip"); Stipulations Regarding Micro-Star, EDIS Doc. ID 460655 at 1 (Sept. 12, 2011) ("MSI Stip"); Stipulations Regarding ECS, EDIS Doc. ID 460649 at 1 (Sept. 2, 2011) ("ECS Stip"); Stipulations Regarding Biostar, EDIS Doc. ID 460647 at 1 (Sept. 9, 2011) ("Biostar Stip"); Stipulations Regarding Galaxy, EDIS Doc. ID 460651 at 1 (Sept. 9, 2011) ("Galaxy Stip"); Stipulations Regarding Pine, EDIS Doc. ID 460658 at 1 (Sept. 22, 2011) ("Pine Stip"); Stipulations Regarding Sparkle, EDIS Doc. ID 460659 at 1 (July 13, 2011) ("Sparkle Stip"); Stipulations Regarding EVGA, EDIS Doc. ID 460650 at 1 (Sept. 16, 2011) ("EVGA Stip"); Stipulations Regarding Gigabyte, EDIS Doc. ID 460652 at 1 (Sept. 12, 2011); Stipulations Regarding HP, EDIS Doc. ID 460653 at 1 (Sept. 27, 2011) ("HP Stip"); Stipulations Regarding Jatón, EDIS Doc. ID 460654 at 1 (Oct. 4, 2011) ("Jatón Stip"); Stipulations Regarding Palit, EDIS Doc. ID 460657 at 1 (Sept. 16, 2011) ("Palit Stip"); Stipulations Regarding Zotac, EDIS Doc. ID 460660 at 1 (Sept. 13, 2011) ("Zotac Stip"); Stipulation Between Rambus and Motorola Mobility Inc., EDIS Doc. ID 459583 at ¶3 (Sept. 7, 2011) ("Motorola Stip"); Stipulations Regarding Respondent Hitachi Global Storage Technologies Inc., EDIS Doc. ID 454292 at 1 (July 12, 2011) ("Hitachi Stip").)

*16 Respondents LSI, Seagate, and Oppo do not dispute that they import the accused products into the United States. (RIB at 16-19.) The evidence shows that the importation requirement for these respondents has been satisfied. (CX-7473C.0177-78 (LSI); CX7274C.0074 (Oppo); JX-115C.00329-30 at 108-11 (Seagate).)

On December 2, 2011, the Commission issued its opinion in *Certain Electronic Devices with Image Processing Systems, Components Thereof, and Associated Software*, Inv. No. 337TA-724 ("Electronic Devices with Image Processing Systems"), which was after completion of the post-hearing briefs in this investigation. In *Electronic Devices with Image Processing Systems*, the Commission stated that "the ALJ's importation analysis must include an evaluation of whether the type of infringement alleged will support a finding that there has been an importation of an article that infringes in violation of section 337." *Certain Electronic Devices with Image Processing Systems, Components Thereof, and Associated Software*, Inv. No. 337TA-724, Comm'n Op. at 13, note 8 (December 2, 2011). The Commission held that [S]ection 337(a)(1)(B)(i) covers imported articles that directly or indirectly infringe when it refers to "articles that -- infringe." We also interpret the phrase "articles that -- infringe" to reference the status of the articles at the time of importation. Thus, infringement, direct or indirect, must be based on the articles as imported to satisfy the requirements of section 337.

Id. at 13-14. The Commission further held that "[w]e analyze a violation of section 337(a)(1)(B)(i) based on method claim[s] [] under the statutory rubrics of indirect infringement." *Id.* at 18. In that investigation, the Commission held that the complainant failed to show importation, sale for importation, or sale after importation of articles that infringe a method claim directly or indirectly. *Id.* at 18-19.

Here, as set forth *supra* in Section I.D, the accused products are memory controllers designed to interface with DDR, DDR2, DDR3, GDDR3, LPDDR or LPDDR2 compliant memory devices and products incorporating such devices and interface chips that are designed according to PCI Express, DisplayPort, SATA and SAS interface standards and products incorporating such chips. Rambus has alleged that these accused products directly and indirectly infringe the asserted claims, which include apparatus and method claims, of the Barth and the Dally Patents. As set forth *infra* in Section IV, to the extent that the ALJ finds that Respondents' accused products directly or indirectly infringe the asserted claims of the Barth and the Dally Patents, the importation requirement has been satisfied.

III. JURISDICTION

A. Personal and Subject Matter Jurisdiction

In order to have the power to decide a case, a court or agency must have both subject matter jurisdiction and jurisdiction over either the parties or the property involved. *See Certain Steel Rod Treating Apparatus and Components Thereof*, Inv. No. 337-TA-97, Commission Memorandum Opinion, 215 U.S.P.Q. 229, 231 (1981). For the reasons discussed below, the ALJ finds the Commission has jurisdiction over this investigation.

*17 Section 337 declares unlawful the importation, the sale for importation, or the sale after importation into the United States of articles that infringe a valid and enforceable United States patent by the owner, importer, or consignee of the articles, if an industry relating to the articles protected by the patent exists or is in the process of being established in the United States. *See* 19 U.S.C. §§ 1337(a)(1)(B)(1) and (a)(2). Pursuant to Section 337, the Commission shall investigate alleged violations of the Section and hear and decide actions involving those alleged violations.

Respondents argue that the Commission lacks jurisdiction because (1) Rambus cannot satisfy the domestic industry requirement; (2) Rambus lacks standing to assert the Dally Patents; and (3) certain respondents do not import, sell for importation or sell after importation any accused products. (RIB at 7.) As set forth *supra* in Section II, the ALJ found that the importation requirement has been satisfied. The ALJ notes that Respondents do not dispute that the Commission has *in personam* or subject

matter jurisdiction. (RIB at 7.) Respondents have fully participated in the investigation, including participating in discovery, participating in the hearing, and filing pre-hearing and post-hearing briefs. Accordingly, the ALJ finds that Respondents have submitted to the jurisdiction of the Commission. *See Certain Miniature Hacksaws*, Inv. No. 337-TA-237, Pub. No. 1948, Initial Determination at 4, 1986 WL 379287 (U.S.I.T.C., October 15, 1986) (unreviewed by Commission in relevant part). Furthermore, as the Federal Circuit held in *Amgen, Inc. v. Int'l Trade Comm'n*

As is very common in situations where a tribunal's subject matter jurisdiction is based on the same statute which gives rise to the federal right, the jurisdictional requirements of section 1337 mesh with the factual requirements necessary to prevail on the merits. In such a situation, the Supreme Court has held that the tribunal should assume jurisdiction and treat (and dismiss on, if necessary) the merits of the case.

Amgen, Inc. v. United States Int'l Trade Comm'n, 902 F.2d 1532, 1536 (Fed. Cir. 1990). Thus, as for Respondents' remaining arguments, e.g., lack of domestic industry and lack of standing relating to the Dally Patents, the ALJ will address those *infra* in the appropriate sections.

IV. CLAIM CONSTRUCTION

A. Barth Patents

On June 22, 2009, the ALJ issued *Order No. 12: Construing the Terms of the Asserted Claims of the Patent at Issue* in Investigation No. 337-TA-661.⁴ The parties in the instant investigation have agreed that the claim terms construed in that order should govern in this investigation, but that any terms not previously construed should be given their plain and ordinary meaning. (CIB at 11; RIB at 20-21; SIB at 18.) To the extent that the parties disagree about the plain and ordinary meaning of any claim terms, such disputes were addressed in the context of infringement and/or invalidity. As such, the ALJ will follow a similar practice and address those disputes in the relevant sections below.

B. Dally Patents

“Processor”

Rambus

“Circuitry for processing data”

Staff/Respondents

“Circuitry for processing data”

*18 The parties agree on the construction of “Processor” but disagree on what that definition means. Rambus contends that the parties dispute the application of this construction in the context of certain prior art references. Specifically, Rambus argues that the definition does not include certain prior art references that use Manchester encoders. Respondents and Staff argue that “circuitry for processing data” is broad enough to include Manchester encoders and biphase encoders because these circuits process data. Rambus does not argue that a claim construction compels this result and instead offers factual testimony about whether these prior art references come within the scope of the claims. The ALJ discerns no reason to further construe the claims because the dispute between the parties is a factual dispute. Accordingly, the ALJ will deal with this factual dispute below in the context of the specific prior art references.

“Output Frequency”

Rambus

“One-half of the value of the output data rate”

Staff/Respondents

“output data rate”

Rambus argues that “output frequency” as used in the claims and in the context of the technology requires that “output frequency” be one half the output data rate. Staff and Respondents argue that in light of the disclosure of the patent, the term should be construed as output data rate. The ALJ agrees with Staff and Respondents that the term should be construed as “output data rate.”

Beginning with the language of the claims, Rambus argues that the plain meaning of “frequency” compels its construction. Rambus notes that frequency is often expressed in units of Hertz, where one Hertz is one cycle per second. (CIB at 181 (citing Tr. 684:9-13.)) Rambus further argues that in the context of electrical signaling, one cycle corresponds to one high signal level and one low signal level. (CIB at 181 (citing Tr. 684:17-685:5).) Rambus argues that the asserted claims of the Dally patents are directed to non-return-to-zero signaling and that in this type of signaling, each high signal level represents one bit of data (*i.e.*, a one) and each low signal level also represents one bit of data (*i.e.*, a zero). (CIB at 181 (citing Tr. 1472:221473:5).) Rambus contends that because under this conceptualization, two bits of data are represented in a single Hertz then the plain and ordinary meaning of “output frequency” is onehalf of the output data rate. (CIB at 181.)

*19 Staff and Respondents disagree with Rambus's plain meaning of the term “output frequency.” Contrary to Rambus's assertion regarding the plain meaning, Staff explains that in a digital system such disclosed in the Dally patents, cycles-per-second is often referred to in terms of the system's “symbol rate” (also known as baud (Bd)), with each symbol representing one or more bits depending on the particular implementation. (SIB at 135 (citing Tr. 1555:21-24; RX5506C at Q/A 59-61).) Staff notes that Dr. Singer, Rambus's expert, agreed with this assessment at his deposition, but attempted to rescind that prior testimony at trial. (SIB at 136 n.87 (citing Tr. 710:09-714:06).) Respondents agree with Staff's assessment and point out that Rambus's model depends on a series of mistaken assumptions. Respondents argue that Rambus's first mistaken assumption is that one cycle corresponds to one high signal level and one low signal level. (RRB at 55.) Respondents assert that this is based testimony from Dr. Singer concerning sine waves oscillating at fixed frequencies and is inconsistent with the type of signaling disclosed in the Dally patents. (RRB at 55.) The second error Respondents point to is Rambus's allegation that the asserted claim relate to non-return to zero signaling. (RRB at 56.) The third error Respondents contend that Rambus makes in its “plain meaning” analysis is that the Dally patents only use the rising edge of the clock to sample each bit of data. (RRB at 56.) Staff agrees with these criticisms (SRB at 69-71) and argues that these assumptions may not be true. Thus, Staff contends that contrary to Rambus's assertion, there is or no plain meaning that necessarily requires that output frequency be one-half the output data rate. (CRB at 71.)

The ALJ agrees with Staff and Respondents that at the very least Rambus's assertion that its definition is necessarily the “plain meaning” of the claim term “output frequency” is simply not correct. The ALJ agrees with Respondents and Staff that Rambus's “proof requires a number of assumptions that may or may not be true and certainly are not mandated without review of the other intrinsic evidence. As Staff and Respondents cogently illustrated, underlying Rambus's construction is the assumption that the signal is a simple sinusoidal wave (illustrated below):

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But as Staff explained, a one hertz clock signal could also be generated using 4 bits, 8 bits, etc...:

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Moreover, Respondents correctly note that the error of Rambus's assumption that one cycle necessarily includes one high signal and one low signal is further illustrated by Figure 2 of the Dally, which does not follow that assumption:

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Thus, it is apparent that Rambus's assumption that “[i]n the context of electrical signaling, one cycle corresponds to one high signal level and one low signal level [”] is not necessarily correct and cannot establish that Rambus's definition is the “plain meaning” of the term output frequency.

***20** As for Rambus's assumption that the Dally Patents require Non-Return to Zero signaling, the ALJ finds nothing in the plain language that would support such an assumption. While that assumption might be valid in light of the other intrinsic evidence, Rambus has failed to provide sufficient evidence to establish that based on the claim language alone that such an assumption is warranted. As the Staff further demonstrated, the evidence presented at the hearing established that other coding schemes exist within the art, such as Manchester or bi-phase coding. As Staff demonstrated in the following figure, in Manchester or bi-phase encoding, a clock signal can be represented by alternating high and low values with a clock rate in hertz that is equal to the bit rate required to represent that clock signal:

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The ALJ finds that while this information regarding the plain meaning presented by Staff and Respondents does not establish that Staffs and Respondents' construction is necessarily correct, it fundamentally undermines Rambus's principal argument that its construction is necessarily the plain meaning of the term "output frequency."

Respondents also argue that Rambus's construction would render other limitations in the same claims superfluous. (RIB at 120-121 (citing *Stumbo v. Eastman Outdoors, Inc.*, 508 F.3d 1358, 1362 (Fed. Cir. 2007)).) Respondents point to Claim 2, which includes two separate limitations, one related to output frequency and another related to bandwidth. Respondents assert that Dr. Singer acknowledges that under his construction, for a non-modulated system, "just saying the output frequency was at least a gigahertz would make the 100 megahertz irrelevant." (RIB at 121 (quoting Tr. at 725:12-16).) Respondents note that, in contrast, Dr. Hassoun does not specify a relationship between "output frequency" and bandwidth, nor does his construction rely on one; therefore, "[Dr.] Hassoun's construction does not render the bandwidth limitation superfluous." (RIB at 123 (citing RX-5431C at Q/A 68).) Respondents contend that in a modulated system, the "output frequency" is the center or carrier frequency, and not half the data rate. (RIB at 123 (citing Singer Depo Tr. at 350:25-351:24).) Thus, Respondents argue that Rambus's construction only applies to a subset of systems covered by claim 2 (*i.e.* excludes modulated systems) and for nonmodulated systems, its construction renders the bandwidth limitation superfluous.

Rambus argues that Respondents' argument rests on the assumption that the claims are only directed to nonmodulated systems, but dependent claim 6 recites a nonmodulated limitation demonstrating that the claims are directed to both modulated and non-modulated systems. (CRB at 100.) Rambus asserts that in a modulated system that it is possible to have an output frequency of greater than 1GHz while the bandwidth is less than 100 MHz because the output frequency and bandwidth are independent. (CRB at 100.)

***21** The ALJ agrees with Respondents that this flaw does cast further doubt on Rambus's argument, but it is not dispositive. It simply reinforces the need to look closely at the specification for additional guidance on what a person of ordinary skill in the art would understand this term to mean.

Rambus contends that the specification supports its construction as well. Specifically, Rambus relies on two passages that it contends confirm its construction. In the first passage, the specification relates "a 4 Gb/s signal (FIG. 2A)" and the attenuation of "[t]he highest frequency of interest (2 GHz)." (CIB at 181 (citing JX-120 at 3:59-63).) The second passage states "our operating frequency of 2GHz corresponding to a bit rate of 4 Gb/s." (CIB at 181 (citing JX-120 at 4:16-19).) Rambus argues that these two passages confirm that a Non-Return to Zero signal with an output frequency of 2 GHz has a data rate of 4 Gb/s. (CIB at 181-182.) Rambus asserts that none of the passages cited by the Respondents and Staff can support the one-bit-per Hertz construction that Respondents and Staff advocate. (CIB at 182.) Rambus argues that the passages relied on by Respondents and Staff do not support Respondents' and Staff's construction because they are silent as to the relationship between Hertz and bit rate. (CIB at 182-183.) Rambus argues that the references to 4 GHz pertains to the clock rate used to operate on the data. (CIB at 183.) Rambus asserts that "[w]hen only the rising edge of a clock is used, the clock needs to operate at twice the frequency of the data." (CIB at 183.)

Respondents and Staff argue that the specification specifically ties data rates to output frequency. Respondents and Staff note that in the Background of Invention section the applicant distinguishes prior art by tying frequency with data rates:

Most digital systems today use full-swing unterminated signaling methods that are unsuited for data rates over 100 MHz on one meter wires. Even good currentmode signaling methods with matched terminations and carefully controlled line and connector impedance are limited to about 1 GHz by the frequency-dependent attenuation of copper lines.:

(JX-120 at 1:32-37.) Respondents urge that this shows that specification uses Hertz in connection with data rates contrary to Rambus's suggestion. (RIB at 119.) Respondents further argue that the specification "closely ties "4 GHz" and "4 Gbps" together in the context of frequency and data rate, demonstrating a 1-to-1 correlation between output frequency and output data rate." (RIB at 119.) Specifically, Respondents note that Figure 12, for example, depicts a transmitter that "accepts 10 bits of data, D₀₋₉, at 400 MHz." (RIB at 119 (quoting JX-120 at 7:56).) Respondents assert that the specification shows that these 10 bits of 400 MHz parallel data are ultimately converted and output at 4 Gbps serially. (RIB at 119.) Respondents also point to the discussion of Figure 1 of the Dally patents, which discusses converting 10-bit parallel data at 400 MHz to serial data operating at an output data rate of 4 Gbps. (RIB at 119 (citing JX-120 at 3:16-19).) Finally, Respondents argue that the specification also states that a "4 Gbps serial channel replaces 40 100 MHz pins," which corresponds to one serial channel at 4 GHz. (RIB at 119 (quoting JX-120 at 8:13-16).) However, Rambus argues that this also supports their construction because it improperly assumes that the reference is to single-ended signaling, whereas it is in fact differential signaling where two pins are used for a single channel. (CIB at 183-184.)

***22** The ALJ agrees with Respondents and Staff that the specification supports their construction of output frequency. The ALJ notes that outside of the claims, the term "output frequency" is not used in the specification. The preferred embodiments, however, would suggest to a person of ordinary skill in the art what was meant by the term output frequency. One such preferred embodiment is shown in Figure 1, which "shows one channel of a high-speed signaling system embodying the invention." (JX-120 at 3:15-17; *see also* Tr. 1556:20-1560:06.) This Figure appears as follows:

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The ALJ agrees with Staff that in the embodiment of Figure 1, the "transmitter module 22 accepts 8-bit parallel data at 400 MHz." (JX-120 at 3:16-17; *see also* Tr. 1558:12-1559:06.) Staff is correct that the bit rate for data input to the transmitter is thus 8-bits parallel x 400 MHz, *i.e.*, the equivalent of 1-bit serial x 3.2 GHz (*i.e.*, 8 x 400 MHz = 1 x 3.2 GHz). (Tr. 1558:04-11.) Staff is further correct that within the transmitter module 22, the 8-bit parallel data "is coded into 10 bits for band-limiting and forward error correction and transmitted . . . across a single differential transmission line." (JX-120 at 3:17-19; *see also* Tr. 1558:12-1559:15.) Thus, the transmitter module 22 is processing the equivalent of 10-bits parallel x 400 MHz. (Tr. 1558:12-1559:15.) However, Figure 1 specifies the rate for the serial channel on which the transmitter module 22 transmits those bits in terms of bits-per-second (*i.e.*, 4 Gbps) rather than in terms of Hertz (*i.e.*, 10 x 400 MHz = 4 GHz). The 4 Gbps label thus suggests that the embodiment of Figure 1 has a 1:1 ratio between bits-per-second and Hertz, which is consistent with the previous discussion of the prior art embodiment in column 1. (Tr. 1559:18-1560:06.)

The ALJ agrees with Staff and Respondents that the embodiment shown in Figure 12 is also consistent with the construction proposed by the Staff and Dr. Hassoun:

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In this embodiment, "[t]he transmitter accepts 10 bits of data, D₀₋₉, at 400 MHz." (JX-120 at 7:5-6; *see also* Tr. 1560:07-1561:21; Tr. 804:16-805:16, 809:18-22 (Dr. Singer).) The 10 bits of data at 400 MHz (parallel) are ultimately converted and output at 4 GHz serially (over the differential "++--" output) = *i.e.*, 10 x 400 MHz = 4 GHz. (Tr. 1560:07-1561:21; Tr. 805:19-806:06 (Dr. Singer).) However, Figure 12 does not label its output in terms of GHz. Rather, Figure 12 specifies a "4 Gbps" output, again equating 4 Gbps with the 4 GHz of data known to be leaving the transmitter per the prior calculation. (Tr. 1560:24-1561:21.) Thus, the ALJ agrees with Respondents and Staff that more than just mentioning 4 Gb/s and 4 GHz close to each other, as

Rambus suggests (CIB at 183), the embodiment of Figure 12 *and* the embodiment of Figure 1 both appear to use a 1:1 ratio between bits-per-second and Hertz.

***23** The ALJ finds that yet another example supporting a 1:1 ratio appears in column 8, which reads in part:

A 4 Gbs serial channel can also be used as a replacement technology at both the component and system level. At the component level, a single serial channel (two pins) replaces 40 100 MHz pins.

(JX-120 at 8:13-16.) Forty parallel channels at 100 MHz equates to one serial channel at 4 GHz, *i.e.*, 40 x 100 MHz (parallel) = 4 GHz (serial). The ALJ agrees with Staff that Rambus misreads this passage. Staff is correct that the 4 Gbps single channel described in this embodiment is a “two pin” implementation that uses differential signaling (requiring two pins for a given channel) described elsewhere in the patent. (JX-120 at 3:17-19 (describing differential signaling).) However, Staff is correct that because this passage describes only the single serial channel as a “two pin” differential configuration, the “40 100 MHz pins” also disclosed in this same passage is not “two pin” differential configuration. The ALJ agrees that the “40 100 MHz” configuration instead refers to single-ended signaling, requiring one pin for a given channel. In any event, the ALJ finds that even if Rambus is correct, the fact that one embodiment is inconsistent is not fatal to Respondents' and Staff's construction. *See August Tech. Corp. v. Camtek, Ltd.*, 655 F.3d 1278, 1285 (Fed. Cir. 2011) (quoting *TIP Sys., LLC v. Phillips & Brooks Gladwin, Inc.*, 529 F.3d 1364, 1373 (Fed. Cir. 2008)) (“The mere fact that there is an alternative embodiment disclosed in the asserted patent that is not encompassed by our claim construction does not outweigh the language of the claim, especially when the court's construction is supported by the intrinsic evidence.” (alternations and quotation marks omitted)). Thus, here again the Dally patents speak in terms of Gbps with a 1:1 ratio between bits-per-second and Hertz.

The ALJ further agrees that Rambus is simply incorrect that these examples are merely referring to “clock rate.” Moreover, the ALJ agrees with Respondents that the passages cited by Rambus are not particularly persuasive because they are discussing the relationship between data rate and operating frequency, not output frequency, which do not appear to be the same thing, or at the very least, Rambus has not presented evidence that they are the same thing. (*See* CIB at 181 (JX-120 at 3:59-69, 4:16-19 (“our operating frequency correspond[s] to a bit rate of 4 Gb/s”).)

Staff also cite various extrinsic evidence. (SIB at 138; SRB at 72.) However, the ALJ finds that based on the intrinsic evidence, the meaning of the term “output frequency” is clear. The ALJ does not find it necessary to consult this evidence.

Accordingly, the ALJ finds that the intrinsic evidence supports Respondents' and Staff's construction of the term “output frequency” as “output data rate.”

***24 “Transmitter Circuit”/ “Transmitter”⁵**

Rambus/Staff/LSI Seagate

Plain and ordinary meaning

Respondents (other than LSI/Seagate)

“digital transmitter that comprises an equalizer that generates signal levels as a logical function of bit history to emphasize transition signal levels as distinguished from a conventional FIR filter in which the input is delayed and the individual delayed signals are weighted and

summed, but not applied to additional digital circuitry”

Rambus and Staff argue that these terms should be given their plain and ordinary meaning. One of Respondents' experts, who testified on behalf of LSI and Seagate, Dr. Hajimiri agrees. The remaining Respondents (who will be referred to as “Respondents” for the remainder of this section) and their expert, Dr. Hassoun contend that “transmitter circuit” and “transmitter” should be construed as set forth above. The critical dispute between the parties is whether the claims include so-called conventional FIR filters or not or as Respondents put it: a transmitter circuit that “comprises an equalizer that generates signal levels as a logical function of bit history to emphasize transition signal levels as distinguished from a conventional FIR filter in which the input is delayed and the individual delayed signals are weighted and summed, but not applied to additional digital circuitry.” Rambus and Staff (and Dr. Hajimiri) argue that Respondents are improperly attempting to read limitations into the claims.

Beginning with the language of the claims, the parties appear to agree that there is nothing in the language of the claims that would support Respondents' construction. Indeed, the parties agree that the plain meaning of the terms “transmitter circuit” or “transmitter” does not exclude conventional FIR filters. (See SIB at 141 (citing Tr. 1439:19-1440:12, 1578:25-1579:07, 1579:8-15, 597:13-598:1, 815:9-817:4).)

*25 Rambus also argues that the claims of an unasserted patent related to the asserted Dally patents expressly recite the limitation -- “a logical function of bit history” -- that Respondents seek to include in the asserted claims. (RIB at 186 (citing CX-9687 at claims 2, 4-6).) Thus, Rambus contends that the applicant could not have meant to define “transmitter circuit” as Respondents do.

The ALJ agrees that the claim language does not support Respondents' construction. There is no dispute that the terms “transmitter” and “transmitter circuit” have a clear and established meaning in the relevant art. As for Rambus's reliance on what can loosely be described as claim differentiation between the claims in the asserted patents and certain claims in other patents in the Dally patent family, the ALJ does not find it particularly convincing. While the ALJ agrees with Rambus that this language does suggest that the applicant could explicitly include the limitations that Respondents now seek to include in “transmitter” and “transmitter circuit,” Respondents are also correct that the claims Rambus seeks to rely do not include the disputed limitations of “transmitter” or “transmitter circuit.” Thus, the ALJ finds that this evidence is not particularly persuasive. See *Curtiss-Wright Flow Control Corp. v. Içla, Inc.*, 438 F.3d 1374, 1380 (Fed. Cir. 2006) (“[C]laim drafters can also use different terms to define the exact same subject matter...”).

Looking next at the specification, Rambus responds that the specification refutes Respondents' construction. (CIB at 185.) Specifically, Rambus points to a statement in the specification that “[p]referred implementations of the invention include finite input [*sic.* Impulse] response filters....” (CIB at 185 (citing JX-120 at 5:50-52).) Rambus argues that this statement “provides no limitation on the type of FIR filters that may be used to implement the claimed inventions.” (CIB at 185.) Finally, Rambus relies on a statement at the end of the specification that “[w]hile this invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.” (RIB at 185-186 (citing JX-120 at 8:37-42).)

Rambus also argues that the portions of the specification that Respondents rely on do not support Respondents' arguments. For instance, Rambus contends that the statement in the specification distinguishing “conventional FIR filters” is limited to the embodiment in Figure 8 and does not apply to the embodiments shown in Figures 9 and 10. (CIB at 186.) Rambus argues that none of this evidences the clear disavowal required to narrow the claims. (CRB at 102.)

*26 Staff agrees with Rambus that the specification does disclose the non-conventional FIR filter embodiment that Respondents' rely on, but Staff notes that the Dally patents also disclose embodiments that use more rudimentary conventional FIR filter techniques to perform equalization:

Preferred implementations of the invention include finite input response (FIR) filters, and FIG. 8 illustrates one such implementation. In this case, a 5 tap filter has been selected as a balance between higher fractional bandwidth and circuit complexity. With a greater number of taps, equalization can be obtained at lower frequencies.

(JX-120 at 5:50-55.)

Staff argues that while there are some references in the specification referring to the non-conventional FIR filters as the “present invention” these other embodiments show the invention is broader than that and therefore the use of the “present invention” should not be limiting. (SIB at 143.)

Respondents, on the other hand, contend that the specification “unequivocally limits the patent to a transmitter that generates signal levels as a logical function of bit history and excludes conventional FIR filters that weight and sum individual delayed input bits.” (RIB at 115.) Respondents point to a statement in the specification where the inventors distinguished the filter used in one of the embodiments from a “conventional” FIR filter. *See* JX-120 at 5:59-63 (“As in a conventional FIR filter, the input D_i is delayed in successive delay elements 28. However, rather than weighting the individual delayed signals and summing the weighted signals to obtain the desired output, the delayed signals are applied to a 5-to-32 decoder.”).

Respondents also argue that none of the preferred embodiments show weighting of individual delayed bits and instead, they argue that each depicts executing a logical function of bit history using ‘logic elements (*e.g.*, 5-to-32 decoders, random access memory, and look-up tables).’ (RIB at 113.) Respondents further point to statements in the Abstract that describe the transmitter as including an equalizer and that “[t]he equalizer generates signal levels as a logical function of bit history to emphasize transition signal levels relative to repeated signal levels.” (RIB at 115 (quoting JX-120 at Abstract).) Respondents further point to the Summary of the Invention, which states that:

In accordance with the present invention, a digital transmitter comprises an equalizer which emphasizes transition levels relative to repeated signal levels. In particular, a novel equalizer generates signal levels as a logical function of bit history to emphasize transition signal levels. Preferred implementations define the logical function of bit history in a look up table. (JX-120 at 1:61-67.)

*27 Respondents say they do not dispute that the specification includes embodiments using a FIR filter. Rather, Respondents argue that they dispute whether the specification includes embodiments that use *conventional* FIR filters. (RRB at 59.) Respondents contend that Rambus is incorrect that the statements distinguishing conventional FIR filters are limited to the embodiment shown in Figure 8 and do not involve Figure 9 and 10. (RRB at 60.) Respondents assert that as shown in Figure 8, the individual delayed input signals are applied directly to the decoder without any weighting. (RRB at 60.) Respondents argue that “[t]he Specification explains that the embodiments of Figures 9 and 10 ‘simplify’ the circuit in Figure 8 by replacing the decoder (*i.e.*, the circuitry that performs a logical function of bit history) with a “find-first-one unit’ and ‘exclusive-OR gate,’ respectively.” (RRB at 60.) Respondents contend that “[t]he embodiments [of Figures 9 and 10] ‘approximate’ the functionality of Figure 8 by simplifying the circuitry that generates the signals as a logical function of bit history.” (RRB at 60 (citing JX-120 at 6:8-24).) Respondents assert that “[t]he embodiments of Figures 9 and 10, contrary to Rambus’s suggestion, do not weight and sum the individual delayed signals, but rather use the same technique Dally said was his invention.” (RRB at 61.) Respondents also contest Staff’s assertions arguing that contrary to Staff’s suggestion that Figure 8 represents a conventional FIR filter, the specification explains that Figure 8 in fact is different than a conventional FIR filter. (RRB at 63.)

The ALJ agrees with Rambus and Staff that the specification does not provide the support for Respondents' construction. While the specification does distinguish conventional FIR filters, the ALJ agrees with Rambus that this distinction is being drawn between the FIR filter used in the embodiment shown in Figure 8, not the invention generally, and conventional FIR filters. Moreover, the entire discussion is with respect to "[p]referred implementations" of the invention not the invention generally. As for Respondents' reliance on the statements in the Summary of the Invention that provides that "[i]n accordance with the present invention, a digital transmitter comprises an equalizer which emphasizes transition signal levels relative to repeated signal levels[]" and "[i]n particular, a novel equalizer generates signal levels as a logical function of bit history to emphasize transition signal levels." (JX-120 at 1:61-65.) The ALJ agrees with Rambus and Staff that the quoted passage is consistent with the view that the invention is broad enough to encompass multiple types of transmitter circuits including those that emphasize based on a logical function of bit history as well as those that do not. Indeed, the specification states that "[p]referred implementations of the invention include finite input [impulse] response (FIR) filters, and FIG. 8 illustrates one such implementation." (JX-120 at 5:50-53.) Thus, the specification does not limit itself to a particular subset of FIR filters as Respondents suggest.

*28 While Respondents are correct that the specification does emphasize certain preferred embodiments of the invention, Staff is correct that this does not justify reading those embodiments into the claims. See *Absolute Software, Inc. v. Stealth Signal, Inc.*, 659 F.3d 1121, 1136 (Fed. Cir. 2011) ("[U]se of the phrase 'present invention' or 'this invention' is not always so limiting, such as where the reference to a certain limitation as being the 'invention' are not uniform, or where other portions of the intrinsic evidence do not support applying the limitation to the entire patent."). As for Respondents' contentions that all of the embodiments are limited in a way similar to Figure 8 in that none of them weight and sum the bits and that all of the equalizers disclosed operate as a logical function of bit history, this is more a question of enablement (which they do not raise) than claim construction. See *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898 (Fed. Cir. 2004). Accordingly, the ALJ agrees with Rambus and Staff that the specification supports a broad interpretation of "transmitter" and "transmitter circuit" that encompasses both conventional FIR filter techniques and the more elaborate techniques of the preferred embodiments.

Respondents have a few more arrows in their quiver. They also point to the prosecution history in support of their construction. Specifically, Respondents rely on statements made by the applicant during the prosecution of a related patent, U.S. Patent No. 7,602,858, which was previously asserted in this investigation and has since been dropped. Respondents argue that "Dally expressly disclaims weighting and summing in the prosecution history." (RIB at 115.)

During the prosecution of the '858 Patent, the applicant stated that "Burlage [a prior art reference cited by the examiner] weighs prior input bits and sums those weighted values ... By contrast, with the present invention, the strength of each output bit signal can be simply determined by the number of output bit signals since the last preceding transition." (RX-2240 at 103-104.) Respondents assert that even though the claims in the '858 Patent are different, the applicant was referring to the entire invention and not just the particular claims of that application. (RRB at 63.)

Rambus argues that these statements should not be limiting because they were made about a set of claims that are "fundamentally different than the Asserted claims because they recited emphasis signals based on the output of a transmitter instead of emphasizing based on its input." (CIB at 187.) Staff agrees with Rambus that "[w]hile similar in some respects, the claims of the [application that became the '858 Patent] are different in several other, material respects from the issued claims of the '858 and '494 patents." (SIB at 143.) Staff argues that "[t]he evidence thus shows that the applicant was at most distinguishing the particular embodiments covered by the pending ['858 Patent] claims from prior art being asserted by the Examiner -- *not* that there has been a clear disavowal of conventional FIR filter techniques for the Dally invention as a whole." (SIB at 143 (emphasis in the original).)

*29 The ALJ does not find these statements made in a related co-pending application to be particularly helpful to Respondents for at least two reasons. First, the ALJ agrees with Rambus and Staff that while the claims are similar in some respects, the claims of the '858 Patent are different in several other, material aspects. As Rambus correctly explains, the claims that were actually distinguished by the applicant recited emphasizing based on input. (RX-2240 at 96; CX10764C at 15.) The ALJ agrees

with the Staff that the evidence shows that the applicant was at most distinguishing the particular embodiments covered by the pending '858 Patent claims from the prior art being cited by the examiner and does not amount to a clear disavowal of conventional FIR filter techniques for the Dally patent family as a whole. (See CX-9542C at Q/A 130-131; Tr. 661:10-667:17; JX-32C at 372:22-373:09.) Given this difference, the ALJ finds that the statement applicant made in the prosecution of the '858 Patent does not meet the requirement that “the alleged disavowing statements to be both so clear as to show reasonable clarity and deliberateness, and so unmistakable as to be unambiguous evidence of disclaimer.” *Omega Eng'g v. Raytek Corp.*, 334 F.3d 1314, 1323 (Fed. Cir. 2003). *Second*, this finding is further supported by the fact that not only is language different, but these statements were made during the prosecution of a related application that is not a parent or earlier application of the patents-in-suit. See, e.g., *Ventana Med. Sys., Inc. v. Biogenex Labs., Inc.*, 473 F.3d 1173, 1182 (Fed. Cir. 2006) (“[T]he doctrine of prosecution disclaimer generally does not apply when the claim term in the decedent patent uses different language.”); *Invitrogen Corp. v. Clontech Labs., Inc.*, 429 F.3d 1052, 1078 (Fed. Cir. 2005) (“[T]he prosecution of one claim term in a parent application will generally not limit different claim language in a continuation application.”). Accordingly, the ALJ finds that the prosecution history does not limit the plain meaning of the asserted claims here.

Finally, Respondents also rely on statements made by Dr. Dally, the named inventor, and Dr. Poulton, a scientist who worked with Dr. Dally (but who is not a named inventor) to the effect that Dr. Dally did not invent convention FIR filters, but rather something different. (RIB at 116-117.) Rambus responds that this is irrelevant because the claims are not directed to the filter used but something broader and most inventions are combinations of old elements. (CRB at 102.) Staff responds with the definition from an electrical engineering dictionary that defines “transmitter” as “an equipment for producing and sending signals.” (SIB at 56 (quoting SX-5 at 597).) The ALJ finds the extrinsic evidence cited by the Respondents to not be persuasive here. Not only is Rambus correct that the claimed invention here is broader than just the filter, this type of post hoc testimony cannot overcome the clear intrinsic evidence in this case. See *N. Am. Vaccine, Inc. v. Am. Cyanamid Co.*, 7 F.3d 1571 (Fed. Cir. 1993) (holding “after-the-fact testimony is of little weight compared to the clear import of the patent disclosure itself”).

*30 Accordingly, the ALJ agrees with Rambus and Staff that the terms “transmitter” and “transmitter circuit” should have their plain and ordinary meaning. The ALJ agrees with Staff that the claim language itself is not inherently ambiguous and that there is a well-established meaning for the disputed terms and that there has been no clear effort to limit the scope of the claims in the intrinsic evidence. (See SRB at 56 (citing SX-5 at 597).) The ALJ notes that Respondents have presented a compelling argument, but the ALJ believes that the intrinsic evidence demonstrates that the inventor did not limit his invention in the way that Respondents contend.

V. INFRINGEMENT DETERMINATION

A. Applicable Law

In a Section 337 investigation, the complainant bears the burden of proving infringement of the asserted patent claims by a preponderance of the evidence. *Certain Flooring Products*, Inv. No. 337-TA-443, Commission Notice of Final Determination of No Violation of Section 337, 2002 WL 448690 at 59, (March 22, 2002); *Enercon GmbH v. Int'l Trade Comm'n*, 151 F.3d 1376 (Fed. Cir. 1998).

Each patent claim element or limitation is considered material and essential. *London v. Carson Pirie Scott & Co.*, 946 F.2d 1534, 1538 (Fed. Cir. 1991). Literal infringement of a claim occurs when every limitation recited in the claim appears in the accused device, i.e., when the properly construed claim reads on the accused device exactly. *Amhil Enters., Ltd. v. Wava, Inc.*, 81 F.3d 1554, 1562 (Fed. Cir. 1996); *Southwall Tech. v. Cardinal IG Co.*, 54 F.3d 1570, 1575 (Fed. Cir. 1995).

If the accused product does not literally infringe the patent claim, infringement might be found under the doctrine of equivalents. The Supreme Court has described the essential inquiry of the doctrine of equivalents analysis in terms of whether the accused product or process contains elements identical or equivalent to each claimed element of the patented invention. *Warner-Jenkinson Co., Inc. v. Hilton Davis Chemical Co.*, 520 U.S. 17, 40 (1997).

Under the doctrine of equivalents, infringement may be found if the accused product or process performs substantially the same function in substantially the same way to obtain substantially the same result. *Valmont Indus., Inc. v. Reinke Mfg. Co.*, 983 F.2d 1039, 1043 (Fed. Cir. 1993). The doctrine of equivalents does not allow claim limitations to be ignored. Evidence must be presented on a limitation-by-limitation basis, and not for the invention as a whole. *Warner-Jenkinson*, 520 U.S. at 29; *Hughes Aircraft Co. v. U.S.*, 86 F.3d 1566 (Fed. Cir. 1996). Thus, if an element is missing or not satisfied, infringement cannot be found under the doctrine of equivalents as a matter of law. See, e.g., *Wright Medical*, 122 F.3d 1440, 1444 (Fed. Cir. 1997); *Dolly, Inc. v. Spalding & Evenflo Cos., Inc.*, 16 F.3d 394, 398 (Fed. Cir. 1994); *London v. Carson Pirie Scott & Co.*, 946 F.2d 1534, 1538-39 (Fed. Cir. 1991); *Becton Dickinson and Co. v. C.R. Bard, Inc.*, 922 F.2d 792, 798 (Fed. Cir. 1990).

***31** The concept of equivalency cannot embrace a structure that is specifically excluded from the scope of the claims. *Athletic Alternatives v. Prince Mfg., Inc.*, 73 F.3d 1573, 1581 (Fed. Cir. 1996). In applying the doctrine of equivalents, the Commission must be informed by the fundamental principle that a patent's claims define the limits of its protection. See *Charles Greiner & Co. v. Mari-Med. Mfg., Inc.*, 92 F.2d 1031, 1036 (Fed. Cir. 1992). As the Supreme Court has affirmed:

Each element contained in a patent claim is deemed material to defining the scope of the patented invention, and thus the doctrine of equivalents must be applied to individual elements of the claim, not to the invention as a whole. It is important to ensure that the application of the doctrine, even as to an individual element, is not allowed such broad play as to effectively eliminate that element in its entirety.

Warner-Jenkinson, 520 U.S. at 29.

Prosecution history estoppel may bar the patentee from asserting equivalents if the scope of the claims has been narrowed by amendment during prosecution. A narrowing amendment may occur when either a preexisting claim limitation is narrowed by amendment, or a new claim limitation is added by amendment. These decisions make no distinction between the narrowing of a preexisting limitation and the addition of a new limitation. Either amendment will give rise to a presumptive estoppel if made for a reason related to patentability. *Honeywell Int'l Inc. v. Hamilton Sundstrand Corp.*, 370 F.3d 1131, 1139-41 (Fed. Cir. 2004), cert. denied, 545 U.S. 1127 (2005) (citing *Warner-Jenkinson*, 520 U.S. at 22, 33-34; and *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 535 U.S. 722, 733-34, 741 (2002)). The presumption of estoppel may be rebutted if the patentee can demonstrate that: (1) the alleged equivalent would have been unforeseeable at the time the narrowing amendment was made; (2) the rationale underlying the narrowing amendment bore no more than a tangential relation to the equivalent at issue; or (3) there was some other reason suggesting that the patentee could not reasonably have been expected to have described the alleged equivalent. *Honeywell*, 370 F.3d at 1140 (citing, *inter alia*, *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 344 F.3d 1359 (Fed. Cir. 2003) (*en banc*)). “Generalized testimony as to the overall similarity between the claims and the accused infringer’s product or process will not suffice [to prove infringement under the doctrine of equivalents].” *Tex. Instruments, Inc. v. Cypress Semiconductor Corp.*, 90 F.3d 1558, 1567 (Fed. Cir. 1996).

Section 271(b) of the Patent Act prohibits inducement: “[w]hoever actively induces infringement of a patent shall be liable as an infringer.” 35 U.S.C. § 271(b) (2008). As the Federal Circuit stated:

***32** To establish liability under section 271(b), a patent holder must prove that once the defendants knew of the patent, they “actively and knowingly aid[ed] and abett[ed] another’s direct infringement.” However, “knowledge of the acts alleged to constitute infringement” is not enough. The “mere knowledge of possible infringement by others does not amount to inducement; specific intent and action to induce infringement must be proven.”

DSU Med. Corp. v. JMS Co., 471 F.3d 1293, 1305 (Fed. Cir. 2006) (*en banc*) (citations omitted); See also *Cross Medical Products, Inc. v. Medtronic Sofamor Danek, Inc.*, 424 F.3d 1293, 1312 (Fed. Cir. 2005) (“In order to succeed on a claim

inducement, the patentee must show, first that there has been direct infringement, and second, that the alleged infringer knowingly induced infringement and possessed specific intent to encourage another's infringement.”). Mere knowledge of possible infringement by others does not amount to inducement. Specific intent and action to induce infringement must be proven. *Warner-Lambert Co. v. Apotex Corp.*, 316 F.3d 1348, 1363 (Fed. Cir. 2003). In *DSU*, the Federal Circuit clarified the intent requirement necessary to prove inducement. As the court recently explained:

In *DSU Med. Corp. v. JMS Co.*, this court clarified en banc that the specific intent necessary to induce infringement “requires more than just intent to cause the acts that produce direct infringement. Beyond that threshold knowledge, the inducer must have an affirmative intent to cause direct infringement.”

Kyocera Wireless Corp. v. Int'l Trade Comm'n, 545 F.3d 1340, 1354, (Fed. Cir. 2008) (citation omitted). “Proof of inducing infringement requires the establishment of a high level of specific intent.” *Lucent Techs. Inc. v. Gateway, Inc.*, 2007 WL 925510, at *2-3 (S.D. Cal. 2007)

Under 35 U.S.C. § 271(c), “[w]hoever offers to sell or sells within the United States or imports into the United States a component of a patented machine, manufacture, combination, or composition, or a material or apparatus for use in practicing a patented process, constituting a material part of the invention, knowing the same to be specifically made to or specially adapted for use in the infringement of the patent, and not a staple article or commodity suitable for substantial non-infringing use, shall be liable as a contributory infringer.”

A seller of a component of an infringing product can also be held liable for contributory infringement if: (1) there is an act of direct infringement by another person; (2) the accused contributory infringer knows its component is included in a combination that is both patented and infringing; and (3) there are no substantial non-infringing uses for the accused component, *i.e.*, the component is not a staple article of commerce. *Carborundum Co. v. Molten Equip. Innovations, Inc.*, 72 F.3d 872, 876 (Fed. Cir. 1995).

*33 To prove direct infringement, Rambus must prove by a preponderance of the evidence that the accused products either literally infringe or infringe under the doctrine of equivalents the method of asserted claims of the '353, '405, '109, '494 and '857 Patents. *Advanced Cardiovascular Sys., Inc. v. Scimed Life Sys., Inc.*, 261 F.3d 1329, 1336 (Fed. Cir. 2001). Notably, method claims are only infringed when the claimed process is performed. *Ormco Corp. v. Align Technology, Inc.*, 463 F.3d 1299, 1311 (Fed. Cir. 2006). Furthermore, in order to establish a violation of Section 337 of a method claim, it is insufficient for Rambus to show that the accused products directly infringe. Rather, Rambus must show that the accused products indirectly infringe those method claims. *Electronic Devices with Image Processing Systems*, Inv. No. 337-TA-724, Comm'n Op. at 18-19.

B. The Barth Patents

Rambus asserts that the Accused Barth Products infringe claims 11-13 of the '353 Patent and claims 1, 2, 4, 12, 20, 21 and 24 of the '109 Patent. (CIB at 25.) Rambus asserts that Accused Barth Products that issue the write command with autoprecharge commands (“the Accused Autoprecharge Products”) infringe the claims 11-13, 15 and 18 of the '405 Patent and claims 5 and 13 of the '109 Patent. (CIB at 25.) Staff agrees. (SIB at 18-35.)

The '353 Patent

a) Claim 11

Claim 11 is a method claim and the only asserted independent claim from the '353 Patent. Rambus and Staff argue that the Accused Barth Products meet each and every limitation of claim 11 of the '353 Patent. Respondents argue that the Accused Barth Products do not practice the “strobe signal” elements of claim 11. The ALJ finds that Rambus has shown by a preponderance of the evidence that the Accused Barth Products directly infringe claim 11.

(1) A Method of Controlling a Memory Device that Includes a Plurality of Cells

The evidence shows that the Accused Barth Products include a memory controller that performs a method of controlling a memory device that includes a plurality of cells. (CX-9543C, Przybylski Direct Q&A 136-43, 216-25, 250-51, 265-68, 310-325, 775-77, 789-808, 860-62, 879-82, 1599-1601, 1617-29, 1668-69, 1688, 2124-25, 2210-12; JX-100C at 14:22-24; JX-110C at 110:18-20; CX-6363C.0001-2; CX-8551C.001-2; JX-107C at 82:13-16; JX-053C at 134:24135:10; CX-8806.0087; JX-135C at 59:16-18; JX-055C at 24:11-25:10; CX-8065C.0006.) Respondents do not dispute that the Accused Barth Products meet this limitation except to the extent that the claim term “memory devices” includes stacked memory. (RIB at 37-38.) As set for *infra* in Section VI.B.1.c, the ALJ has declined to adopt Rambus's construction and, as such, Respondents' argument is moot.

Therefore, the ALJ finds that Rambus has shown by a preponderance of the evidence that the preamble of claim 11 is met during normal operation of the Accused Barth Products.

(2) Issuing a First Write Command to the Memory Device

*34 The evidence also shows that, when operated with a JEDEC-compliant memory device, the memory controllers in the Accused Barth I Products issue a first write command to the memory device. Specifically, the memory controllers issue one or more bits that specify that the memory device receive and store data. (CX-9543C, Przybylski Direct Q&A 143-167, 225-36, 251-57, 268-82, 326-31, 777-83, 808-36, 862-69, 882-95, 1601-09, 1629-51, 1669-77, 1688-92, 2125-34, 2212-26; JX-144C at 310:13-18; JX-075C at 67:19-68:2; CX-8566C.0017; CX-6572.0004; CX-8602C.0081; JX-103C at 119:10-18; CX-8807.0087; JX-055C at 53:17-25; Smith, Tr. 901:19-22.) Respondents do not dispute that the Accused Barth Products meet this limitation. (RIB at 29-41.) Therefore, the ALJ finds that the Accused Barth Products meet this limitation.

(3) Delaying for a First Time Period after Issuing the Write Command

The evidence shows that after issuing a write command, the memory controllers in the Accused Barth Products delay for a period of time (“tDQSS,” “WL,” or some combination of the two) before asserting a strobe signal and that time must elapse before the controller issues the strobe signal. (CX-9543C at Q&A 167-69, 237-41, 257-59, 282-91, 356-359, 783-85, 836-42, 869-73, 895-902, 1609-12, 1651-56, 1678-81, 1692-93, 2134-37, 2226-32; JX-100C at 40:10-19; CX-6879C.0142; JX-053C at 141:5-10; JX-103C at 119:10-18; JX-055C at 208:12-209:1.) Respondents do not dispute that their Accused Barth Products meet this limitation. (RIB at 29-41.) Thus, the evidence shows that this limitation is met during normal operation of the Accused Barth Products.

(4) The Memory Device Being Configured to Defer Sampling Data That Corresponds to the First Write Command until a Strobe Signal Is Detected/ After Delaying for the First Time Period, Issuing the Strobe Signal to the Memory Device to Initiate Sampling of a First Portion of the Data by the Memory Device

Rambus and Staff argue that the Accused Barth Products issue a strobe signal -- the data strobe, DQS or WDQS -- that initiates sampling in the memory device. (CIB at 27-31; SIB at 27-30.) Respondents argue that the “strobe signal” in the Barth Patents does not cause the actual sampling of data and that DQS signal in the Accused Barth Products does not initiate sampling as required by the claims, but actually causes sampling to happen. (RIB at 29-32.)

The ALJ finds that the Accused Barth Products meet these claim limitations. The ALJ finds that the “strobe signal” in the Accused Barth Products is the DQS or WDQS strobe signal, depending on the particular JEDEC standard. There does not appear to be a material difference between the two types of signals as they relate to infringement of claim 11. (See RIB at 30-32.) Taking the DDR standard as an example, the evidence shows that the DQS strobe signal and its relationship to data propagated on a DQ data bus are mandatory features of the standard:

Symbol	Type	DESCRIPTION
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DQ	I/O	Data Bus: Input/Output
DQS	I/O	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data. For the X16, LDQS corresponds to the data on DQ0-DQ7; UDQS corresponds to the data on DQ8-DQ15.
(LDQS)		
UDQS		

*35 CX-4347.0012 (the “DDR Standard”). Indeed, there appears to be no dispute that, when performing a write operation with a JEDEC-compliant memory device, the Accused Barth Products issue a DQS strobe signal to the memory device in accordance with the applicable JEDEC standard.

The evidence further shows that data precedes the DQS signal for some period of time and follows the DQS strobe signal for some period of time. The time period during which data appears in advance of the DQS signal is generally referred to as “setup” time (t_{DS}). (CX-9543C, Przybylski Direct Q&A 336; CX-4347.0070 (Figure 43); Przybylski, Tr. 2721:06-14.) The setup time t_{DS} ensures that the memory device's sampling circuitry is given sufficient time to stabilize before the edge of the DQS signal initiates sampling of the data. (*Id.*) The time period during which data is held constant after the DQS strobe signal is generally referred to as “hold” time (t_{DH}). (*Id.*) The hold time t_{DH} ensures that the memory device's sampling circuitry has sufficient time to sample the data after the edge of the DQS signal initiates sampling. As shown in Figure 21 of the JEDEC standard, the DQS signal tells the memory device that valid data is on the data lines and the data is sampled on the “rising edge” and the “falling edge” of the DQS signal:

TABULAR OR GRAPHIC MATERIAL SET FORTH AT THIS POINT IS NOT DISPLAYABLE

(CX-4347.0039; *see also* CX-9543C, Przybylski Direct Q&A 335-336.) The memory controller's issuance of the DQS strobe signal is carefully coordinated with data transmitted to the memory device. (Przybylski, Tr. 847:06-851:06.) Thus, the DQS signal initiates sampling of data by the memory devices.

The evidence further shows that Respondents' witnesses and documentation confirm that this mandatory strobe to data timing relationship exists with respect to operation of the Accused Barth Products with JEDEC-compliant memory devices. (*See* Jacobs, Tr. 1040:12-1041:21; Smith, Tr. 909:13-910:08, 911:03-913:07, 916:13-19; CX-9543C, Przybylski Direct Q/A 307393, 489-520, 626-668, 799-831, 902-911, 930-940.) ***

Respondents argue that the Accused Barth Products do not infringe the Barth Patents because (1) the “strobe signal,” as construed by Respondents, merely indicates when data transfer can happen, but does not act as a timing signal for actually sampling data and (2) the DQS signal in the Accused Barth Products actually causes sampling of data and does not merely initiate it. Rather, it is the write command that initiates sampling. (RIB at 29-32.) The ALJ finds their arguments unpersuasive.

As for the latter argument, the evidence shows that the write command initiates the write operation, whereas the DQS signal initiates the sampling of data associated with that operation. As set forth *supra*, the evidence shows that the DQS/WDQS signal in the Accused Barth Products initiates sampling of data. Indeed, Respondents' own experts acknowledged that it is the DQS signal -- not the write command -- that initiates sampling in JEDEC-complaint memory devices. (*See* JX-147C, Walker at 85:07-11; CX-9543C, Przybylski Q&A 350 (quoting deposition testimony of Martin Walker); Jacobs, Tr. 1043:23-1044:17 (discussing same); Smith, Tr. 915-16, 938.) Respondents' expert, Dr. Smith, acknowledges that JEDEC-complaint memory devices delay between the receipt of a write command and the sampling of data associated with that write command, which

supports the view that the DQS signal initiates the sampling of data whereas the write command initiates the write operation. (See Smith, Tr. 904:25-905:04.) The evidence further shows that the write command initiates the write operation: ***

*36 ***

As for Respondents' first argument that the "strobe signal" cannot act as a timing signal for actually sampling data, the ALJ finds that, as Staff correct noted, this is merely a re-hashing of Respondents' written description defense. The ALJ finds that the "strobe signal" that can encompass a signal that is capable of indicating when sampling may begin ("indirect control") and a signal that actually initiates data sampling ("direct control").

The Barth Patents disclose methods of performing both "read" and "write" data transfer operations with synchronous devices, which inherently requires that a data receiving device "sample" and retain data associated with such an operation.⁶ ('353 Patent, 1:11-14; 7:41-43; CX-10765, Przybylski Rebuttal Q&A 175.) There is nothing in the specification or the asserted claims require that sampling (once initiated) be accomplished in a specific manner or by a specific structure. (CX-9543C, Przybylski Direct Q&A 349; Przybylski, Tr. 839:17-840:02.) Correspondingly, it does not matter whether the strobe is directly or indirectly connected to the sampling mechanism. As Staff correctly noted, one can directly turn a light switch on/off by herself operating the light switch or alternatively indirectly turn the light switch on/off by ordering someone else to do so at a specified time -- in both instances the individual has initiated the process by which the light switch is turned on/off.

The ALJ finds Respondents' narrow construction is unsupported by the claims, the specification and the prosecution history. The specification discloses the broad concept of data "sampling" as well as data "sampling" mechanisms that can be employed in a given system. In one such example, the specification explicitly describes a "latch" and the "latching" of data. ('353 patent, 2:13-16 (describing a "latch in the memory controller"); *id.* at 2:25-26 (describing a data input of a memory device that is "latched on the rising edge of the clock"); *id.* at 6:1-2 (describing a memory bank with "a latching sense amplifier cache 604 and 608"); *id.* at 24:19-22, 29:42-44, 37:23-26; Przybylski, Tr. 2734:11-2736:06 (describing "bus samples"). Furthermore, the asserted claims of the Barth Patents are method claims that are broadly directed at the use of a strobe signal that initiates sampling regardless of the specific sampling mechanism for a given system. (CX-9543C, Przybylski Direct Q&A 349; Przybylski, Tr. 839:03-22.) Thus, detailed examples need not be provided for the *claimed* invention to be adequately supported for written description purposes.

The ALJ finds that Respondents' reliance on the testimony of Dr. Przybylski is also misplaced as their arguments mischaracterize his testimony. Dr. Przybylski did not testify that he agrees with the Respondents' experts that sampling in the Accused Barth I Products is initiated by a write command rather than a DQS strobe signal. (RIB at 31-32.) Rather, Dr. Przybylski explained that sampling in a JEDEC-compliant memory device is initiated upon detection of the DQS strobe signal, *not* the write command, which is timed so as to coincide with the middle of a data packet to be sampled. (Przybylski, Tr. 873:11-17; 878:02-879:13; CX-9543C, Przybylski Direct Q&A 333-336.)

*37 Therefore the ALJ finds that the Accused Barth Products meet the limitations of claim 11.

b) Claim 12

The ALJ finds that the Accused Barth Products meet the limitations of claim 12. Claim 12 depends from claim 11 and states "issuing the first portion of the data and a second portion of the data to the memory device, wherein the first portion of the data is sampled during an odd phase of an external clock signal, and the second portion of the data is sampled during an even phase of the external clock signal." (JX-4 at 41:41-47.) The evidence shows that the Accused Barth Products, when interfaced with a DDR based memory device (*i.e.*, a memory device compliant with any one of the Accused JEDEC Standards, which are all DDR based), issues data in this way. (CX-9543C, Przybylski Direct Q&A 363-390; Jacobs, Tr. 1048:10-1050:07, 1136:06-09; Smith, Tr. 922:11-932:24.) Specifically, two portions of data are provided for sampling during one cycle of an external clock provided to the memory device. The external clock cycle or period may be divided into two portions, one termed an odd phase

and the other termed an even phase. Data is presented in each phase and for proper operation the memory device samples the data during those phases. This operation is confirmed by Respondents' testimony and documents and JEDEC standards. (CX-9543C at 171-83, 303-19, 912-31, 1697-1710, 2141-44, 2242-45; CX-7670C.0048; JX-100C at 51:6-52:7; JX-075C at 59:22-60:14; JX-073C at 81:9-11; CX-8178.0005; JX-042C at 59:4-5; CX-8078.0044; JX-055C at 44:5-10.) Indeed, the word "double" in the larger phrase "double data rate" (DDR) refers to the issuance of data during both of the two phases of a clock signal.

Respondents argue the terms "even phase" and "odd phase" in claim 12 fails to encompass any portion of the transitions between the two phases and that since the Accused Barth Products sample data during these transition phases, they do not infringe. (RIB at 33-34.) The ALJ finds such an argument unpersuasive. The evidence shows that a person of ordinary skill in the relevant art would appreciate that an "even" and an "odd" phase of a given clock period together encompass the entire clock period, *including* transitions. (CX-9543C, Przybylski Direct Q&A 177-78; 376-390.) Respondents' own expert agreed that, "[w]hether you say low is odd or low is even is really not significant . . . it is interchangeable. You could just as well refer to odd as high." (Smith, Tr. at 927.) He also agreed that JEDEC defines the transitions as being part of the high and low portions of a clock cycle. (Smith, Tr. at 931.)

Therefore, the ALJ finds that the Accused Barth Products meet every limitation of claim 12.

c) Claim 13

Claim 13 is dependent from claim 12, and further states that "the first and second portions of the data [to be] both issued during a common clock cycle of the external clock signal." (JX-4 at 41:48-50.) In other words, the data is issued during a "common" clock cycle, *i.e.*, the "even" and "odd" phases of claim 12 are back-to-back. The evidence shows that the Accused Barth Products contain double data rate controllers, which issue both portions of the data during a common clock cycle. CX-9543C at 183, 320-36, 391-393; 931-49, 1711-22, 2145-47, 2246-50; CX-6879C.0142; JX-100C at 51:6-52:7; JX-075C at 64:17-23; CX-8178.0005; JX-042C at 59:4-5; CX-8078.0044; JX-055C at 44:5-10.) Respondents' arguments disputing that the Accused Barth Products meet this limitation are the same as those for claim 12. (See RIB at 34.) To the extent that they failed with respect to claim 12, they similarly fail with respect to claim 13.

***38** Therefore, the ALJ finds that the Accused Barth Products meet every limitation of claim 13.

'405 Patent

Rambus asserts that Accused Autoprecharge Products infringe the claims 11-13, 15 and 18 of the '405 Patent. (CIB at 25.) Staff agrees. (SIB at 33-34.)

d) Claim 11

Claim 11 of the '405 Patent is similar claim 11 of the '353 Patent and the same type of evidence demonstrating infringement of the '353 Patent similarly can demonstrate infringement of the asserted '405 Patent claims. Claim 11 of the '405 patent is directed to a write with autoprecharge operation and states "a second code which specifies that a precharge operation be initiated automatically after initiation of the write operation." (JX-03.0046.) This is the only additional feature that was not already set forth *supra* in Section V.B.1.a. The ALJ finds that the Accused Autoprecharge Products meet each and every limitation of claim 11.

The evidence shows that the Accused Autoprecharge Products issue write with autoprecharge commands. (CX-9543C, Przybylski Direct Q&A at 24-25, 32-39, 61-63, 188-97, 342-43, 355-58, 407-412, 954-56, 978-80, 999-1000, 1726-27; JX-066C 90:3-7, 122:21-24; JX-110C 112:6-12.) Before a read or write operation can occur on a different row of data than the one present in the sense amplifiers, a precharge operation must occur, which can be initiated via a separate precharge command, or it can be specified to occur automatically after a column operation is completed, such as at the conclusion of a write operation. The

latter is known as automatically precharging (or autoprecharging). The mechanism for accomplishing an autoprecharge in the Accused Autoprecharge Products is for the controller to provide a second code to the memory device when a read or write command is issued. That code is generally provided by signaling HIGH on address line A10. The evidence shows that the Accused WAP Products practice the asserted '405 patent claims for the reasons discussed above in the context of the asserted '353 patent claims. (CX-9543C, Przybylski Direct Q&A 184-197, 338-378, 950-1012, 1723-1733, 400-406, 413-424.)

Respondents' only dispute is that certain of the Accused Barth Products do not use the "write with autoprecharge" and that Rambus has failed to prove that these products infringe on this basis. (RIB at 36-37.) The ALJ finds Respondents' argument irrelevant as Rambus has not asserted that these non-accused products infringe the '405 Patent. (CIB at 25 (separating "products that issue write with autoprecharge commands" from all of the Accused Barth Products.) Thus, Respondents have failed to provide any valid argument as to why the Accused Autoprecharge Products do not meet each and every limitation of claim 11.

Therefore, the ALJ finds that the Accused Autoprecharge Products meet each and every limitation of claim 11.

e) Claims 12 and 13

*39 Claims 12 and 13 of the '405 Patent are similar to claims 12 and 13 of the '353 Patent. The evidence shows that the Accused Autoprecharge Products are infringed for the same reasons. (CX-9543C at Q&A 198-199, 378-392, 1013-1031, 1733-1737.) Therefore, the ALJ finds that the Accused Autoprecharge Products meet each and every limitation of claims 12 and 13.

f) Claims 15 and 18

Dependent claim 15 recites providing "address information to the memory device." (CX-9543C at 393.) The evidence shows that Accused Autoprecharge Products provide address information to memory devices in the form of bank, row, and column addresses. (CX-9543C at 199-200, 393-396, 1032-1040, 1738-1739; CX-6880C.0083; CX-6879C.0142; JX-144C at 284:2-5; JX-039C at 123:25-124:4; CX-6572.0004; JX-042C at 66:9-15.)

Dependent claim 18 recites "the plurality of control codes includes a third code which specifies that a row of sense amplifiers be activated." (CX-9543C at 200.) The evidence shows that the Accused Autoprecharge Products provide activate commands to the attached memory device, which includes address information to identify a particular row in a particular bank. That row is then transferred to a set of sense amplifiers. (CX-9543C at 200-201, 397-400, 1040-1046, 1739-1740; CX-6880C.0083, 0021-22; JX-100C 35:18-36:3, 36:16-21, 38:1-3, 38:4-11, 70:2-18; JX-039C 121:16-24; CX-6572C.0004; JX-103C 108:12-20.)

Therefore, the ALJ finds that the Accused Autoprecharge Products meet each and every limitation of claims 15 and 18.

'109 Patent

Rambus asserts that the Accused Barth Products infringe claims 1, 2, 4, 12, 20, 21 and 24 of the '109 Patent. (CIB at 25.) Rambus asserts that the Accused Autoprecharge Products infringe claims 5 and 13 of the '109 Patent. (CIB at 25.) Staff agrees. (SIB at 18-35.) Respondents do not dispute that the Accused Barth Products meet the limitations of the asserted claims of the '109 Patent, except to the extent that they do not meet the '353 and the '405 Patents. (RIB at 29-41.)

The evidence shows the Accused Barth Products infringe claims 1, 2, 4, 12, 20, 21, and 24 of the '109 Patent, and that the Accused Autocharge Products infringe claims 5 and 13 of the '109 patent. (CX-9543C at 202-214, 402-774, 1048-1598, 1741-2122, 2148-2210, 2251-2357.) The analysis as to the '109 Patent is substantially the same as the analysis above with respect to the '353 and '405 Patents. (CX-9543C, Przybylski Direct Q&A 439-481, 554-625, 714-798, 845-884, 912-929, 941-959; Smith, Tr. 920:10-921:23.) The evidence further shows that the Accused Barth Products provide a code that specifies whether to perform a precharge operation (claim 2) and transmitting bank selection information (e.g., claim 4). Specifically, the control information provided by the controllers in each of the Accused Barth Products includes "a third code that specifies whether to perform a

precharge operation,” as recited in ‘109 Patent claim 2. (CX-9543C at 206-08, 488-90, 493, 504-8, 1164-66, 1177-81, 1185, 1193-96, 1829-30, 1839-42, 1845-48, 2165, 2283-85; CX-8558C.0009; CX-8566C.0017; JX-066C.044; CX-8593C.0004; CX-7029C.0043.) This feature is found in the Accused Barth Products because they provide automatic precharge commands, standalone precharge commands, or both, which were discussed in connection with the ‘405 claims. For example, the JEDEC DDR SDRAM Specification provides for a standalone precharge code in its command truth table, which is a table that identifies the signals that must be present on the various signal lines to form the listed commands. (CX-4020.0018.) The precharge command “is used to deactivate the open bank in a particular row or the open row in all banks.” *Id.* at 26.

*40 As for “transmitting bank selection information, wherein the bank selection information identifies a bank of the plurality of banks,” the evidence shows that that this occurs on lines BA0 and BA1 when an active command is sent in the Accused Barth Products.⁷ (CX-9543C at 508-551, 1196-1263, 1848-92, 2166-172, 2286-95; CX-4020.0025; CX-6880C.0122-25; CX-6879C.0142; CX-8566C.0017; CX-7051C.0070; CX-6387C.0005; CX-6385C.0107-12; CX-7029C.0043.)

Therefore, the ALJ finds that the Accused Autoprecharge Products meet each and every limitation of the asserted claims of the ‘109 Patent.

Sufficient Evidence to Prove Direct Infringement

The ALJ finds Respondents' arguments unpersuasive. First, the Accused Barth Products include memory controllers and products containing the same, which include products with memory controllers and memory devices, such as a Tivo, storage adapter, Blu-ray disc player, and phone. (CX 9543C.0026-0112.) The evidence shows that these products were purchased in the United States and include both a memory controller and memory devices. (*Id.*) The evidence shows that the Accused Barth Products contain memory controllers that are designed for use and are used with DDR-type memory. (*Id.*)

In addition, the evidence shows that Respondents have extensively sold the Accused Products in the United States. *See* CX-9543C.2370-75; CIB 40-41. Such extensive sales support a finding of direct infringement. *See Lucent Techs., Inc. v. Gateway, Inc.*, 580 F.3d 1301, 1318-19 (Fed. Cir. 2009); *Moleculon Research Corp. v. CBS, Inc.*, 793 F.2d 1261, 1272 (Fed. Cir. 1986); 661 ID at 43. The ALJ finds it implausible, nor is there any evidence, that such customers would purchase the products in the United States and never use them here. (CX-9543C.2373-74.)

The ALJ further finds that LSI's argument that Rambus cannot show infringement by the LSI 3 Ware products because it “has not presented a limitation-by-limitation infringement analysis for any of these products” to be unpersuasive. The evidence shows that the Accused Barth Products are used in conjunction with JEDEC-complaint memory devices and, as standardized products, operate in substantially the same way for infringement purposes. (Jacobs, Tr. 1045:08-17; Smith, Tr. 897:02-20, 900:04-901:02.) Thus, Rambus need not provide a detailed product-by-product infringement analysis to show infringement of certain asserted claims to the extent that they practice the JEDEC industry standard. *See Fujitsu Ltd. v. Netgear, Inc.*, 620 F.3d 1321, 1327 (Fed. Cir. 2010) (“We hold that a district court may rely on an industry standard in analyzing infringement. If a district court construes the claims and finds that the reach of the claims includes any device that practices a standard, then this can be sufficient for a finding of infringement.”).

*41 ***

Contributory and Induced Infringement

Rambus argues that Respondents induce or contribute to the direct infringement of others within the United States. (CIB at 42-44.) Staff agrees. (SIB at 28-35.) Respondents argue that they do not contributorily infringe because there is no evidence that Respondents “knew that the combination for which its components were especially made were both patented and infringed” and Rambus has failed to show that there are no substantial non-infringing uses. (RIB at 39-40.) Respondent further argue that they do not induce infringement because there is no evidence that any Respondent possesses the requisite intent for inducement or that the Supplier Respondents solicit or encourage their customers to infringe. (RIB at 40-41.)

As set forth *supra*, all of the Accused Barth Products infringe the asserted claims of the '353, '405 and the '109 Patent. The ALJ further finds that the Respondents induce or contribute to the direct infringement of others, such as end users of their products, within the United States.

The evidence shows that Respondents have induced infringement. Respondents' knowledge of the Asserted Patents cannot be disputed since they have had notice since at least December of 2010, when the Complaint in this Investigation was filed. (See, CX-10856C.0001; CX-8173C.0003; Garmin Stip at 4; ASUS Stip at 2; MSI Stip at 2; Biostar Stip at 2; ECS Stip at 1; Galaxy Stip at 2; Pine Stip at 2; Sparkle Stip at 2; EVGA Stip at 2; Gigabyte Stip at 2; HP Stip at 1; Jatón Stip at 2; Palit Stip at 1; Zotac Stip at 2; Motorola Stip at ¶7; Hitachi Stip at 3.) See *Certain Inkjet Ink Cartridges With Printheads And Components Thereof*, Inv. No. 337-TA-723, Initial Determination, 2011 ITC LEXIS 1503 at *145 (June 10, 2011) (unreviewed in relevant part) (finding knowledge requirement for contributory infringement satisfied based on service of the complaint). In addition to the Complaint, the evidence shows that certain of the Barth I Respondents were made aware of the Asserted Patents during licensing negotiations. (See *infra* Section XIV.) Furthermore, the issuance of the Final Initial Determination on Violation in *Certain Semiconductor Chips Having Synchronous Dynamic Random Access Memory Controllers and Products Containing Same*, Inv. No. 337-TA-661 also put the Respondents on notice of infringement by Respondent nVidia and its named customers. (See Public Version of 661 ID, EDIS Doc. ID 423948 at 20-31, 41-44.)

Despite having notice of the Asserted Patents and their infringement, none of the Respondents has stopped selling the Accused Products or made any design changes to avoid infringement. (CX-9543C at 2383, 2386-88, 76; CX-8173C.0003. See *Ricoh*, 550 F.3d at 1343 (“a failure to remove or diminish infringing features of a distributed product is relevant to a party's intent that those features be used for direct infringement”).) The Barth I Respondents have nonetheless taken active steps demonstrating a specific intent to induce infringement, such as advertising the infringing use and providing technical support, instructions, tutorials, software device drivers and other materials directing end users to operate the Accused Products in an infringing manner. (CX-9543C, Przybylski Direct Q&A 982-992, 994-998, 1000, 2374-88; CX-9543C at 2374-88; JX-044C at 32:8-33:6; JX-072C at 62:8-20; JX-016C at 131:7-138:8; JX-080C at 95:17-22; JX-042C at 214:23-215:23; CX-10856C.0002; CX-8173C.0003; Garmin Stip at 4; ASUS Stip at 2; MSI Stip at 2; Biostar Stip at 2; ECS Stip at 2; Galaxy Stip at 2; Pine Stip at 2; Sparkle Stip at 2; HP Stip at 2; Jatón Stip at 2; Palit Stip at 2; Zotac Stip at 2; Hitachi Stip at 4.) Therefore, the ALJ finds that these actions induce infringement and demonstrate Respondents' intent to encourage infringement by end-users.

*42 Respondents also contribute to infringement by end-users. The evidence shows that the Respondents had specific knowledge of the asserted Barth Patents and Complainant's infringement allegations at least as of the filing of the Complaint on December 1, 2010. The evidence further shows that there are no substantial non-infringing uses. The only way to use the Accused Barth Products is in a manner that infringes the asserted claims since all of the Accused Barth Products use a data strobe in the manner claimed in the Barth Patents and will not operate without the remaining claimed features.⁸ (CX-9543C at 1002-1013, 2388-93; JX-135C at 136:14-19; JX-016C at 98:25-99:4.) Furthermore, the manuals provided by Respondents list only a single, infringing method of use.⁹ (*Id.*)

Respondents have known of their infringement since at least December 2010. Yet they have taken no actions to change how their products work and have not stopped distribution or sale of the Accused Products, which have no substantial noninfringing uses. (CX-9543C at 2383, 2386-93, 76; CX-8173C.0003.) Respondents thus contribute to direct infringement by end-users.

As for Respondents' argument that the Accused Products are capable of substantial non-infringing uses because they perform both read and write operations, the evidence shows that the Accused Products must issue write commands or there will be no data to read. (CX-9543C at Q&A 1010, 2391.) In fact, Respondents have not alleged that their controllers do not issue write commands and the Accused Products cannot operate without writing to a memory device. (*Id.*)

Therefore, the ALJ finds that the Accused Barth Products directly and indirectly infringe the asserted claims of Barth Patents.

C. The Dally Patents

The Asserted Claims can be divided into three groups, as discussed below, the ALJ finds that the evidence demonstrates that each Accused Dally Product infringes one or more groups of claims. (CX-9542C.0063-473).

Asserted Claims	Infringing Products
'857 patent claims 1, 4-6, 9, 10, 24-28, 35, 36, 39-44, 47, and 53	All Accused Dally Products
'494 patent claims 1, 2, 6, 8, 25, 30, 39, and 42	
'857 patent claims 11-13, 32-34, and 50-52	Accused Dally Products with multiple transmitters
'494 patent claims 26 and 40	
'857 patent claims 2, 31, and 49	Accused Dally Products able to output data at 2 Gb/s or greater
'494 patent claim 3	

*43 ***

The Accused Products Infringe the Independent Claims of the Dally Patents

The ALJ finds that the Accused Products have all of the features recited in the asserted independent claims.

a) "A Component Comprising a Semiconductor Chip"

Independent claims 1, 24, 35, and 39 of the '857 Patent each recite "[a] component comprising: a semiconductor chip." Independent claims 1, 25, and 39 of the '494 patent also recite a semiconductor chip or an integrated circuit. Rambus and Staff contend that all of the accused products meet this limitation. Respondents do not dispute that their products meet this limitation. Indeed, Respondents' experts concede that the Accused Products include these features. (Tr. 1471:14-17, 1584:23-25.) The evidence shows that all of Respondents' accused Products are semiconductor chips. (CX-9542C at Q/A 204-206, 234-237; JX-68C; CX-4055.0005 (LSI); CX-4087.0004 (ST Micro)).

(a) "A Processor Within the Chip" and "A Component Circuit Within the Chip"

Independent claim 1 of the '857 Patent recites "a processor within a chip." Independent claims 24, 35, and 39 similarly recite "a component circuit within the chip." The ALJ finds that the evidence shows that Respondents' Accused Dally Products include a processor or component circuit within the chip. (CX-9542C at Q/A 57, 63, 69, 72, 149-155, 207-209, 238-242.) Moreover,

the relevant PCI Express, DisplayPort, SATA, and SAS standards all require the use of an 8b/10b encoder. (CX-4027.0152.) For example, the Accused Dally Products all include an 8b/10b encoder or analogous circuitry. (Tr. 1470:17-23; RX-5506C; JX-68C at 82:2-83:05; JX-95C at 118:05-21.) Because an 8b/10b encoder includes circuitry for processing data, *i.e.*, to perform the encoding function thereof, it literally meets the proposed constructions of this term. (See CX-9542C at Q/A 154-155; Tr. 1470:20-1471:21.) Respondents do not challenge that their Accused Dally Products include these elements. (See Tr. 1470:20-1471:21, 1587:3-15.)

b) “A Transmitter Circuit Within the Chip”

Independent claims 1, 24, 35, and 39 of the '857 Patent and claims 1 and 25 of the '494 Patent each recite “a transmitter circuit within the chip.” Independent claim 39 of the '494 Patent similarly recites “an integrated circuit having a transmitter.” The ALJ finds that the evidence shows that each of the Accused Dally Products includes a transmitter circuit or transmitter within the chip within the plain and ordinary meaning as construed by the ALJ. (CX-9542C at Q/A 210-222; 248-254; Tr. 1461:22-1464:06; 1588:14-20.) Respondents contested this element, but only based on the rejected construction proposed by Dr. Hassoun. Accordingly, this element is present in the Accused Dally Products.

c) Transmitter Circuit Coupled to a Processor or Component Circuit

*44 Independent claim 1 of the '857 Patent recites “the transmitter circuit being coupled to the processor to accept a digital input signal including a plurality of digital values from the processor.” Claims 24, 35, and 39 recite similar features but in relation to coupling the transmitter circuit to the claimed “component circuit.” The ALJ finds that the evidence shows that Respondents' Accused Dally Products include these features. (CX-9542C at Q/A 210-222; 248-254; Tr. 1461:22-1464:06; 1588:14-20.) Moreover, the ALJ finds that the relevant standards require that the Accused Dally Products include a transmitter circuit within the chip. (CX-4027.0202; CX-4029.0242; CX-9368.0024; CX-4033.0166; CX-4036.0082.)

As discussed above, the Accused Dally Products use 8b/10b encoding. The ALJ finds that the transmitter circuits in the Accused Dally Products receive a parallel digital input signal with a plurality of digital values or bit values from the 8b/10b or similar encoder. (See *e.g.*, JX-144C.0022 at 61:4-8; CX-7398C.0010-11.) The ALJ finds that the transmitter serializes the values before transmitting them, and, as a result, the processor or component circuit must be coupled to the transmitter circuit to provide the input signal for transmission. (CX-4027.0152. See *e.g.*, JX-144C.0022-23 at 61:12-62:13; JX-81C.0020 at 59:4-60:3; JX-68C.0026 at 98:8-99:18; CX-6610C.0044; CX-7398C.0010-11.)

d) Transmitter Circuit Operable to Send an Output Signal

Independent claims 1, 24, and 35 of the '857 Patent each recite “the transmitter circuit being operable to send an output signal including a series of signal levels representing the digital values and to emphasize high frequency components of the output signal relative to low frequency components of the output signal.” Independent claim 39 of the '857 Patent and independent claims 1, 25, and 39 of the '494 Patent also recite similar limitations directed to sending an output signal. The ALJ finds that the evidence shows that in Respondents' Accused Dally Products, the transmitter circuit is operable to send an output signal as claimed. (CX-9542C at Q/A 162-172, 221-224, 255-257.) Respondents do not appear to dispute that this limitation is met.¹⁰ (Ozguc, Tr. 1187:09-11, 1187:16-23, 1188:05-1190:23, 1192:13-23 (Ozguc); Tr. 1465:08-1467:10, 1469:22-1470:06 (Hassoun); JX-068C at 80:11-81:18 (Kobayashi).)

The ALJ also finds that the relevant standards require that the transmitter circuits in the Accused Dally Products send output signals that include a series of signal levels representing the digital values as claimed. As an example, the PCI Express standards require devices to send an output signal including a series of signal levels. The signal levels represent the digital values provided to the transmitter. (See *e.g.*, CX-4029.0169 (illustrating that the transmitter outputs data serially).) The PCI Express standards also show that the transmitters emphasize high-frequency components of the output signal relative to low-frequency components of the output signal. (*Id.* at 255.) All PCI Express 2.0 transmitters support this type of signal de-emphasis. (See *e.g.*,

CX-4029.0169, 255.) The ALJ finds that the evidence also shows that for the Accused Dally Products that operate in accordance with other relevant standards, the transmitter circuit is operable to send an output signal including a series of signal levels representing the digital values and to emphasize high-frequency components of the output signal relative to low-frequency components of the output signal. (CX-9542C at Q/A 171.)

***45** As Rambus correctly notes, independent claim 1, 25, and 39 of the '494 Patent also requires the transmitter circuit to generate a sign and a magnitude, with its output bit signal having a sign and magnitude. The ALJ finds that evidence shows that the transmitter circuits in each of the Accused Dally Products generate a differential output signal that has both a sign and a magnitude. (CX-9542C at Q/A 430-438; CX-6841C; JX-144C.0026 at 74:21-75:4; JX-144C.0031 at 95:12-96:8; JX-95C.0018 at 62:20-63:4; JX-117C.0024 at 83:9-84:21; CX-6610C.0044; JX-68C.0017 at 63:12-21; JX-68C.0021 at 80:11-24; JX-102C.0024 at 77:8-24; CX-6815C.0090.)

Cisco raises the argument that certain of its accused products do not infringe because the accused interface is not connected to anything within the accused product. (RIB at 133.) Cisco argues that there can be no infringement because “[w]ith these downstream products, the products cannot practice the accused standard because the interface is not used in the accused end product.” (RIB at 133.) However, the ALJ agrees with Staff and Rambus that merely stating that they are “not connected” without further detail, is not evidence that the interface is permanently disabled. (CRB at 106; SIB at 153.) Moreover, as Rambus notes, Cisco has ***

e) Sending Output Signals with Emphasis

Claims 1 and 39 of the '857 Patent recite a transmitter circuit sending an output signal so that “(i) an output bit signal of the output signal representing a particular bit value has one signal level when the bit value is the same as a bit value represented by a predetermined preceding output bit signal; and (ii) the output bit signal representing the particular bit value has another signal level when the bit value is different from the bit value represented by the predetermined preceding output bit signal.” Independent claims 24 and 35 of the '857 Patent and independent claims 1, 25, and 39 of the '494 Patent also recite similar limitations. The ALJ finds that the evidence shows that the Accused Dally Products include these “Output Signals with Emphasis” features these claims. (CX-9542C at Q/A 0099-104, 124-37, 181-87, 237-58.)

f) ST Microelectronics

g) LSI

The ALJ finds that the evidence shows that LSI's Accused Products include the claimed Output Signals with Emphasis, as required by the independent claims of the '857 and '494 Patents. (See CX-9542C at Q/A 258-261.) ***

*** The ALJ finds that the record fails to support LSI's arguments in this regard.

The ALJ agrees with Staff and Rambus that neither of these arguments has any support. First, as Staff points out, documentation from LSI contradicts its position that ***

(***

*** The ALJ finds that this evidence confirms the position of Rambus and the Staff that LSI's *** products operate as an infringing *** product when ***

*46 As for LSI's second argument, the ALJ notes that LSI fails to recognize that the asserted claims of the Dally patents are apparatus claims, not method claims. The law is clear that Rambus need not show actual use of *** to demonstrate infringement of the asserted apparatus claims. Rather, Rambus need only show that the *** are designed for operation in an infringing *** and that users of those products can enable the *** mode without having to modify the product in question. *See Silicon Graphics, Inc. v. ATI Techs., Inc.*, 607 F.3d 784, 794 (Fed. Cir. 2010) (quoting *Fantasy Sports Props., Inc. v. Sportsline.com, Inc.*, 287 F.3d 1108, 1118 (Fed. Cir. 2002) (holding infringement of an apparatus claim occurs “so long as the product is designed “in such a way as to enable a user of that [product] to utilize the function . . . without having to modify [the product].”)). LSI admits that such a showing has indeed been made. ***

In its reply brief, LSI attempts to argue for *** implementations that *** takes LSI's *** outside the asserted Dally claims.” (RRB at 65.) *** Thus, the ALJ finds that this *** has no impact on the output signal level. (See Tr. 1421:9-1422:1; 1437:7-1438:18; CX-9542C at Q/A 53.) *** (CX-9542C at Q/A 47-53; Tr. 1437:7-1438:18; 1421:9-1422:1) Accordingly, the ALJ finds that this is within the scope of the asserted claims of the Dally patents.

The Accused Products Infringe the Dependent Claims of the '857 and '494 Patents

The ALJ finds that the evidence further shows that the Accused Dally Products infringe dependent claims 2, 4, 5, 6, 9, 10-13, 25-28, 31-34, 36, 40-44, 47, 49-53 of the '857 Patent. The Accused Dally Products also infringe dependent claims 2, 3, 6, 8, 26, 30, 40 and 42 of the '494 Patent.

Dependent claims 2, 31, and 49 of the '857 Patent all require that “the transmitter circuit is operable to send the output signal with an output frequency of at least 1 GHz and a bandwidth greater than 100 MHz.” Claim 3 of the '494 Patent recites similar features. The ALJ finds that the Accused Dally Products that output data at a rate of at least 2 Gb/s satisfy these claims. CX-9542C at Q/A 92-96, 103-104.) Indeed, the ALJ notes that the relevant PCI express standards all require a data rate of at least 2 Gb/s for each output. (See CX-9542C at Q/A 263.) The ALJ also finds that Respondents' witnesses and documents also confirm that many of the Accused Dally Products operate at these speeds. (JX-094C.0023 at 81:13-17; JX-137C.0043 at 147:5-148:4; JX-137C.0047 at 163:3-16; JX-56C.0021 at 71:4-6; CX-9104C.0001-2; CX-9105C.0001.) Respondents have not disputed that their Accused Dally Products that output data at a rate of at least 2 Gb/s include the features recited in these claims.

Dependent claims 4, 9, 10, 26, 41, 42, 47, and 53 of the '857 Patent and claims 2 and 6 of the '494 Patent each recite features related to the previously discussed output-signals-with-emphasis features of the claims. The ALJ finds that the same evidence showing that the Accused Dally Products have those features, discussed above also demonstrates that the Accused Dally Products include the features of these claims. (See CX-9542C at Q/A 273-275.)

*47 Dependent claim 11 of the '857 Patent recites that the component circuit includes “at least one additional transmitter circuit within the chip, each additional transmitter circuit being coupled to the processor and operable to accept an additional digital input signal from the processor and send an additional output signal representing such additional input signal.” Dependent claims 32 and 50 of the '857 Patent recite similar limitations. The ALJ finds that the evidence shows that many of the Accused Dally Products include additional transmitter circuits such that they contain these claimed features. (See CX-9542C at Q/A 294-295, 298-306.) In addition, the ALJ finds that Respondents' documents and witnesses confirm that many of the Accused Dally Products contain multiple transmitter circuits. (See JX-144C.0038 at 124:4-13; JX-144C.0046 at 156:3-10; CX-6847C.0005; CX-6848C.0004; CX-6849C.0003; JX-95C.0028 at 115:10-21; JX-117C.0018 at 58:8-9; CX-6349C.0021; CX-9208C.0008.)

Dependent claims 5, 27, and 43 of the '857 Patent recite that “the chip has I/O connections and the transmitter circuit is coupled to one or more of the I/O connections to send the output signal through one or more I/O connections.” The ALJ finds that the evidence shows that the Accused Dally Products include a number of different types of I/O connections, such as PCI Express, SATA, or SAS, as well as memory controller and other I/O connections. (See CX-9542C at Q/A 276-277.) In addition, by virtue

of having one or more of these I/O connections, the transmitter circuits in each of the Accused Dally Products is coupled to one or more of those I/O connections. (*Id.*)

Dependent claims 12, 33, and 51 of the '857 Patent, which depend on claims that require multiple transmitters, recite that “the chip has I/O connections and the transmitter circuits are coupled to a plurality of the I/O connections and operable to send the output signals through the I/O connections.” The ALJ finds that the same evidence discussed above with respect to claims 5, 27, and 43 of the '857 Patent shows that the Accused Dally Products with multiple transmitters include the features of dependent claims 12, 33, and 51 of the '857 Patent. (*See* CX9542C at Q/A 307-309.)

Dependent claims 6, 28, and 44 of the '857 Patent recite that “the transmitter circuit is operable to send the output signals in a nonmodulated form.” The ALJ finds that the evidence shows that the relevant PCI Express, DisplayPort, SATA, and SAS standards all require signals to be sent in nonmodulated form. (*See* CX-9542C at 279-280.) The ALJ also finds that Respondents' documents and witnesses confirm that the transmitter circuits in the Accused Dally Products are operable to send the output signal in a nonmodulated form. (*See* CX-9542C at Q/A 283-286; JX-144C.0032 at 100:6-12; CX-6841C; CX-6844C, CX-6847C - CX-6864C; CX-7398C0013; JX-137C.00130-31 at 535:20-538:2; JX-094C.0024 at 82:15-83:3; CX-6401C.0011; CX-6946C.0011; CX-6610C.0046; CX-9229C.0017; CX-6408C.0018.)

***48** Claim 13 of the '857 Patent recites that “the transmitter circuits are operable to provide output signals representing a parallel stream of data from the processor.” Claims 34 and 52 of the '857 Patent similarly recite that “the transmitter circuits are operable to provide output signals representing a parallel stream of data from the component circuit.” The ALJ finds that the evidence shows that many of the Accused Dally Products include the features of dependent claims 13, 34, and 52 of the '857 Patent. (*See* CX-9542C at Q/A 310-320.) The ALJ finds that the same evidence showing that “[t]he transmitter circuit being coupled to the processor to accept a digital input signal including a plurality of digital values from the processor” of '857 Patent claim 1 also shows that many of the Accused Dally Products include the features of claims 13, 34, and 52 of the '857 Patent. In addition, the ALJ finds that Respondents' documents and witnesses confirm that many of the Accused Dally Products include these features. (*See* CX-9542C at Q/A 310-320; JX-144C.0022-23 at 61:12-62:13; CX-6844C; JX-95C.0030 at 123:15-125:19; JX-117C.0026 at 91:9-92:7; CX-6610C.0044; CX-6406C.0008-09; CX-6408C.0009-10; JX-68C.0026 at 98:11-99:18.)

Dependent claims 25, 36, and 40 of the '857 Patent each recite that the “component circuit is a processor.” The ALJ finds that the same evidence showing that the Accused Dally Products include “a processor within the chip” as recited in '857 Patent claim 1 shows that the Accused Dally Products have this claimed feature. *See* CX-9542C at Q/A 356-358.)

Dependent claims 26 and 40 of the '494 Patent recite that the chip “includes plural of said transmitter circuits [or transmitters]” and that each transmitter circuit or transmitter outputs “a respective series of output bit signals on [respective] lines of a parallel bus.” The ALJ notes that these claims are similar to claims 11 and 13 of the '857 Patent. The same evidence showing that the Accused Dally Products include the features of those claims also demonstrates that the Accused Products include the features of claims 26 and 40 of the '494 Patent. (*See* CX-9542C at Q/A 464.)

Dependent claims 30 and 42 of the '494 Patent both recite that “the series of output signals” be transmitted by the “transmitter onto a signal path at a rate of at least 400 megahertz.” The ALJ notes under the ALJ's construction that a rate of 400 megahertz corresponds to a rate of 400 Mb/s. All Accused Dally Products with PCI Express, DisplayPort, SATA, and SAS interfaces meet this claim requirement, and the same evidence discussed with respect to claim 2 of the '857 Patent showing that the Accused Dally Products operate at speeds of at least 2 Gb/s also demonstrates that the Accused Dally Products include the features of these claims. (*See* CX-9542C at Q/A 465.)

Respondents Directly and Indirectly Infringe the Dally Patents

*49 *** stores, and/or testing them to ensure proper operation. (CX-8173C; CX-10763C; CX-10863C; CX-9027C.0007-9; JX-26C.0017 at 57:16-24; JX-24C.0028 at 94:20-95:6; JX-28C.0022 at 93:7-14; JX-50C.0033 at 127:21-128:4; JX-62C.0025 at 90:5-17; JX-133C.0029 at 98:11-17; IX-139C.0024 at 86:7-24.)

End-users of the Accused Dally Products also always directly infringe the asserted apparatus claims. (CX-9542C.0498.) The high volume of products that Respondents import into the United States (CX-9542G.0498-500), indicates that end-users do in fact use the products in the United States and thus directly infringe the Asserted Claims. *Lucent Techs. v. Gateway, Inc.*, 580 F.3d 1301, 1318-19 (Fed. Cir. 2009); *Moleculon*, 793 F.2d at 1272.

*** December 2010, yet there is no evidence that any of them have changed their practices since that time. (*Id. Broadcom*, 543 F.3d at 699-700.

Respondents LSI and Seagate also assert that “Rambus has failed to prove infringement with respect to LSI and Seagate products because its expert, [Dr.] Singer failed to evaluate the issue of infringement in relation to each and every limitation of the Asserted Claims of the Dally Patents.” (RIB at 139.) LSI and Seagate raise several specific complaints. The ALJ finds these arguments to be frivolous. First, they complain that Dr. Singer only performed his analysis on the LSI SerDes core -- a functional circuit block that is incorporated into an integrated circuit. (RIB at 139.) LSI and Seagate argue that “[e]ach of the asserted claims of the Dally Patents requires a ‘semiconductor chip’ and various components are required to be on the chip.” Based on this, LSI and Seagate conclude that “an appropriate infringement analysis requires evaluation of a SerDes core in the context of the semiconductor chip.” (RIB at 139.) It is beyond any doubt that the SerDes cores are intended to be incorporated into a semiconductor chip. The SerDes cores include the essential circuitry relevant to the issues at hand. Unless LSI and Seagate identified specific elements of the claims where Rambus’s analysis is lacking, the ALJ is not going to consider their broadside assault on Rambus’s analysis.

Second, LSI and Seagate complain that Dr. Singer did not analyze every one of the hundreds of products at issue in this investigation. However, Dr. Singer testified he relied on testimony by LSI witnesses that the products operated in the same fashion and proceeded accordingly. There is nothing wrong with this approach. *See Tivo, Inc. v. Echostar Comm’ns Corp.*, 516 F.3d 1290, 1308 (Fed. Cir. 2008) (“there is nothing improper about an expert testifying in detail about a particular device and then stating that the same analysis applies to other allegedly infringing devices that operate similarly”). LSI complains that these witnesses were not corporate representatives. But there is no requirement that the deposition testimony be disregarded for infringement purposes because she is not a corporate witness and LSI points to no reason why the ALJ should disregard her testimony. *See Martek Biosciences Corp. v. Nutrinova, Inc.*, 579 F.3d 1363, 1372 (Fed. Cir. 2009) (“A patentee may prove infringement by any method of analysis that is probative to the fact of infringement”) (internal quotation marks omitted). Accordingly, LSI’s and Seagate’s arguments are rejected.

VI. VALIDITY

A. Background

*50 One cannot be held liable for practicing an invalid patent claim. *See Pandrol USA, LP v. AirBoss Railway Prods., Inc.*, 320 F.3d 1354, 1365 (Fed. Cir. 2003). However, the claims of a patent are presumed to be valid. 35 U.S.C. § 282; *DAM Inc. v. Deere & Co.*, 802 F.2d 421 (Fed. Cir. 1986). Although a complainant has the burden of proving a violation of section 337, it can rely on this presumption of validity.

Respondents have the burden of overcoming the presumption that the asserted patents are valid and must prove invalidity by clear and convincing evidence in order to do so. *Technology Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1327 (Fed. Cir. 2008) (stating, “When an alleged infringer attacks the validity of an issued patent, [the] well-established law places the burden of persuasion on the attacker to prove invalidity by clear and convincing evidence.” (emphasis added)); see also *Checkpoint Systems, Inc. v. United States Int’l Trade Comm’n*, 54 F.3d 756, 761 (Fed. Cir. 1995). Respondents’ burden of persuasion never shifts to Rambus; the risk of “decisional uncertainty” remains on the respondent. *Id.*; see also *PowerOasis, Inc. v. T-Mobile*

USA, Inc., 522 F.3d 1299, 1303, 1305 (Fed. Cir. 2008); *Pfizer, Inc. v. Apotex, Inc.*, 480 F.3d 1348, 1360 (Fed. Cir. 2007). Thus, it is Respondents' burden to prove by clear and convincing evidence that any of the alleged prior art references anticipate or render obvious the asserted claims of the patents in suit. Failure to do so means that Respondents loses on this point. *Id.* (stating, "[I]f the fact trier of the issue is left uncertain, the party with the burden [of persuasion] loses.").

Respondents also bears the burden of going forward with evidence, *i.e.*, the burden of production. *Id.* This is "a shifting burden the allocation of which depends on where in the process of a trial the issue arises." *Id.* However, this burden does not shift until a respondent presents "evidence that might lead to a conclusion of invalidity." *Pfizer*, 480 F.3d at 1360. Once a respondent "has presented a prima facie case of invalidity, the patentee has the burden of going forward with rebuttal evidence." *Id.*

B. Anticipation

A patent may be found invalid as anticipated under 35 U.S.C. § 102(a) if "the invention was known or used by others in this country, or patented or described in a printed publication in this country, or patented or described in a printed publication in a foreign country, before the invention thereof by the applicant for patent." 35 U.S.C. § 102(a). A patent may be found invalid as anticipated under 35 U.S.C. § 102(b) if "the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States." 35 U.S.C. § 102(b). Under 35 U.S.C. § 102(e), a patent is invalid as anticipated if "the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent." 35 U.S.C. § 102(e). Anticipation is a question of fact. *Texas Instruments, Inc. v. U.S. Int'l Trade Comm'n*, 988 F.2d 1165, 1177 (Fed. Cir. 1993) ("*Texas Instruments II*"). Anticipation is a two-step inquiry: first, the claims of the asserted patent must be properly construed, and then the construed claims must be compared to the alleged prior art reference. *See, e.g., Medichem, S.A. v. Rolabo, S.L.*, 353 F.3d 928, 933 (Fed. Cir. 2003). It is axiomatic that claims are construed the same way for both invalidity and infringement. *W.L. Gore v. Garlock, Inc.*, 842 F.2d 1275, 1279 (Fed. Cir. 2008.)

*51 "Claimed subject matter is 'anticipated' when it is not new; that is, when it was previously known. Invalidation on this ground requires that *every element and limitation* of the claim was *previously described in a single prior art reference*, either *expressly or inherently*, so as to place a person of ordinary skill in possession of the invention." *Sanofi-Synthelabo v. Apotex, Inc.*, 550 F.3d 1075, 1082 (Fed. Cir. 2008) (*emphasis added*) (citing *Schering Corp. v. Geneva Pharms., Inc.*, 339 F.3d 1373, 1379 (Fed. Cir. 2003) and *Continental Can Co. USA v. Monsanto Co.*, 948 F.2d 1264, 1267-69 (Fed. Cir. 1991)).

To anticipate, a single prior art reference must be enabling and it must describe the claimed invention, *i.e.*, a person of ordinary skill in the field of the invention must be able to practice the subject matter of the patent based on the prior art reference without undue experimentation. *Sanofi*, 550 F.3d at 1082. The presence in said reference of *both* a specific description and enablement of the subject matter at issue are required. *Id.* at 1083.

To anticipate, a prior art reference also must disclose all elements of the claim within the four corners of said reference. *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008) ("*NMI*"); *see also Abbott Labs. v. Sandoz, Inc.*, 544 F.3d 1341, 1345 (Fed. Cir. 2007) (stating, "Anticipation is established by documentary evidence, and requires that every claim element and limitation is set forth in a single prior art reference, in the same form and order as in the claim."). Further, "[b]ecause the hallmark of anticipation is prior invention, the prior art reference--in order to anticipate under 35 U.S.C. § 102--must not only disclose all elements of the claim within the four corners of the document, but must also disclose those elements 'arranged as in the claim.'" *Id.* (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)). The Federal Circuit explained this requirement as follows:

The meaning of the expression 'arranged as in the claim' is readily understood in relation to claims drawn to things such as ingredients mixed in some claimed order. In such instances, a reference that discloses all of the claimed ingredients, but not in the order claimed, would not anticipate, because the reference would be missing any disclosure of the limitations of the claimed invention 'arranged as in the claim.' But the 'arranged as in the claim' requirement is not limited to such a narrow set of 'order of limitations' claims. Rather, *our precedent informs that the %7F 'arranged as in the claim' requirement applies to all*

claims and refers to the need for an anticipatory reference to show all of the limitations of the claims arranged or combined in the same way as recited in the claims, not merely in a particular order. The test is thus more accurately understood to mean 'arranged or combined in the same way as in the claim.'%7D

*52 *Id.* at 1370 (emphasis added). Therefore, it is not enough for anticipation that a prior art reference simply contains all of the separate elements of the claimed invention. *Id.* at 1370-71 (stating that "it is not enough [for anticipation] that the prior art reference discloses part of the claimed invention, which an ordinary artisan might supplement to make the whole, or that it includes multiple, distinct teachings that the artisan might somehow combine to achieve the claimed invention." (emphasis added)). Those elements must be arranged or combined in said reference in the same way as they are in the patent claim.

If a prior art reference does not expressly set forth a particular claim element, it still may anticipate the claim if the missing element is inherently disclosed by said reference. *Trintec Indus., Inc. v. Top-U.S.A. Corp.*, 295 F.3d 1292, 1295 (Fed. Cir. 2002); *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). Inherent anticipation occurs when "the missing descriptive material is 'necessarily present,' not merely probably or possibly present, in the prior art." (*Id.*); see also *Rhino Assocs. v. Berg Mfg. & Sales Corp.*, 482 F. Supp.2d 537, 551 (M.D. Pa. 2007). In other words, inherency may not be established by probabilities or possibilities. See *Continental Can*, 948 F.2d at 1268. Thus, "[t]he mere fact that a certain thing may result from a given set of circumstances is not sufficient." *Id.*

The critical question for inherent anticipation here is whether, as a matter of fact, practicing an alleged prior art reference necessarily features or results in each and every limitation of the asserted claim at issue. See, e.g., *Toro Co. v. Deere & Co.*, 355 F.3d 1313, 1320 (Fed. Cir. 2004). Such is the case even if one of ordinary skill in the art would not have recognized said inherent anticipation at the time of the invention of the '829 Patent. *Id.* at 1320-21.

If there are "slight differences" between separate elements disclosed in a prior art reference and the claimed invention, those differences "invoke the question of obviousness, not anticipation." *NMI*, 545 F.3d at 1071; see also *Trintec*, 295 F.3d at 1296 (finding no anticipation and stating that "the difference between a printer and a photocopier may be minimal and obvious to those of skill in this art. Nevertheless, obviousness is not inherent anticipation."). Statements such as "one of ordinary skill may, in reliance on the prior art, complete the work required for the invention," and that "it is sufficient for an anticipation if the general aspects are the same and the differences in minor matters is only such as would suggest itself to one of ordinary skill in the art," actually relate to obviousness, not anticipation. *Connell*, 722 F.2d at 1548; see *infra*.

The Barth I Patents

*53 Respondents argue that certain of the asserted claims of the '353 and the '109 Patents are anticipated by the following references: (1) Japanese Patent Publication No. 3-276344 ("Yano"); (2) European Patent Application No. 94304672.2 ("Dan"); (3) the NextBus Specification ("NextBus"); (4) U.S. Patent No. 5,313,624 ("Harriman"); (5) U.S. Patent No. 5,218,684 ("Hayes"); (6) U.S. Patent No. 6,584,037 ("Farmwald"); and (7) the SyncLink draft IEEE Standard ("SyncLink").¹¹ (RIB at 43.)

a) Yano

Respondents argue that Yano anticipates claim 11 of the '353 Patent. (RIB at 43.) Staff agrees. (SIB at 46-55.) Yano, entitled "Method for Writing Data to Memory," was filed by Sharp K.K. Company in Japan on March 26, 1990, and lists Eijiro Yano as the sole inventor. (RX-4261 at 1.) Yano discloses a system by which a processor can write data to memory through the use of a write command, a delay period, and a data strobe. (*Id.*) It was published on December 6, 1991 and, therefore, qualifies as prior art to the Barth Patents under 35 U.S.C. § 102(b). (*Id.*) Figure 1 of Yano illustrates the major pieces of the system disclosed in the application (with annotations):

TABULAR OR GRAPHIC MATERIAL SET FORTH AT THIS POINT IS NOT DISPLAYABLE

As shown, Yano discloses a microprocessor (yellow), that controls a memory device (blue). “As shown in the figure, 1 is an 8 bit microprocessor, 2 is a memory, $AB_0 \sim AB_{15}$ is an address bus with 16 lines, $DB_0 \sim DB_7$ is a databus with 8 lines, AS is a control bus for address strobe signal, DS is a control bus for data strobe signal, and R/W is a control bus for the read/write switching signal.” (RX-4261 at 3:30-33.)

Figure 2, annotated below, is a timing diagram for a write operation disclosed in Yano.

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The memory controller sends command, address, and data information to the memory device timed in accordance with the system clock (A). Specifically:

Figure 2 is a timing chart of the embodiment shown in Figure 1. As shown in the figure, (A) indicates the system clock, (B) indicates address buses ($AB_0 \sim AB_{15}$), (C) is the address strobe signal (AS). (D) is the read/write changeover signal (R/W), (E) is a bit enable signal (BEx) corresponding to a bit that is to be overwritten, (F) is a bit enable signal (BE) corresponding to other bits, (G) is a databus corresponding to a bit in which writing is to be conducted, (H) is a databus (DB) corresponding to other bits and (I) is the data strobe signal (DS).

(See *id.* at 3:40-46) As shown, each transition of the command, address, and data information is aligned with either a rising or falling edge of the system clock. (RX-5429C at Q232; RDX-3441; Tr. at 2608:23-2613:3.)

*54 Rambus' argues that Yano is an asynchronous memory interface that fails to disclose the strobe signal that “initiate[s] sampling of a first portion of the data” and write command of claim 11 that is “one or more bits which specify that the memory device receive and store data.” (CEB at 59-60; 65-66; CRB at 27-34.) Rather, the data strobe in Yano creates an “active state,” which is an indeterminate amount of time during which data flows into the memory. (CIB at 65.) The asynchronous memory does not receive a clock signal or any other signal used to capture data at a discrete point in time and, as such, does not issue the claimed strobe signal. (CIB at 65-66.) Yano discloses a R/W signal that must be held through the execution of the operation and fails to convey information indicative of a write operation. (CIB at 65-66.)

For the reasons set forth below, the ALJ finds that Respondents and Staff have shown by clear and convincing evidence that Yano discloses each and every element of claim 11 of the '353 Patent.

(1) A Method of Controlling a Memory Device That Includes a Plurality of Memory Cells, the Method Comprising:

The evidence shows that Yano discloses the preamble of claim 11. (RX-5429C, Jacobs Direct Q&A 241.) Figure 1 of Yano depicts a memory 2 that is controlled by a microprocessor 3:

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(RX-4261 at Figure 1; Jacobs, Tr. 1137:12-18; Przybylski, Tr. 2599:04-2600:25, 2605:07-12.) As Yano explains, the microprocessor 3 and memory 2 depicted in Figure 1 can be used to perform a method for writing data to memory 2:

Specifically, according to a method for writing data to microprocessor memory, at the same time when said microprocessor outputs an address signal, a control signal is output specifying any bit within multiple bits creating the structure of 1 word. In addition, data corresponding to said any bit is transmitted through a

databus so that this transmitted data is written to the memory corresponding to any of said bits specified by the address signal and by the control signal.

(RX-4261.0003; Przybylski, Tr. 2597:14-2598:17 (testifying as to same).) Rambus does not dispute that Yano discloses this element. (CIB at 27-34.) Therefore, the evidence shows that Yano discloses the preamble of claim 11.

(2) Issuing a First Write Command to the Memory Device

The evidence also shows that Yano discloses the first portion of the first step of claim 11. (Jacobs, Tr. 1142:14-21, 1144:09-1145:01; RX-5429C, Jacobs Direct Q&A 233, 234, 241, 247.) The R/W signal disclosed in Yano corresponds to the write command called for in claim 11. Figure 1 of Yano depicts a “R/W switching” line 8 running between the microprocessor 3 and memory 2. A timing diagram in Yano (reproduced below) depicts the R/W signal (as propagated on the R/W switching line of Figure 1) asserted low from clock phase S2 through clock phase S6 during which a write operation takes place:

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*55 (RX-4261 at Figure 2; *see also* Jacobs, Tr. 1144:09-1145:01; Przybylski, Tr. 2603:09-2604:02, 2632:24-2633:12, 2636:22-2637:01.)

As set forth *supra*, Rambus disputes whether the “write command” limitation of claim 11 is broad enough to encompass a signal or combination of signals asserted through the entire write operation, as was common in asynchronous memory systems available at that time. The ALJ finds that the claimed “write command” is broad enough to encompass a combination of signals asserted through the entire write operation. (RX-5429C, Jacobs Direct Q&A 247.) Various electronics dictionaries from the relevant timeframe define “write command” as simply an instruction to store data:

write store data in a MEMORY.

(SX-6, Harper Collins Electronics Dictionary (1991) at 360 (emphasis in original).)

write In computer practice, to transfer data from one form of storage to another form.

(SX-5, Illustrated Dictionary of Electronics (5th Ed. 1991) at 655 (emphasis in original).)

command ... 1. In computer practice, the group of selected pulses or other signals which cause the computer to execute a step in its program. **2.** Instruction.

Id. at 113 (emphasis in original). Respondents' expert Dr. Jacobs testified that the dictionary definitions set forth above are consistent with how a person of ordinary skill in the relevant art would have interpreted the “write command” of the Barth I patents in light of the intrinsic record. (RX-5429C, Jacobs Direct Q&A 234; Jacobs, Tr. 1142:22-1144:08.) Indeed, nothing in the intrinsic record supports limiting the claimed “write command” to a particular form (*e.g.*, represented by one or more bits) or to a particular duration as Rambus contends. This is confirmed by the testimony of one of the inventors of the Barth Patents.¹² (JX-47C.0043 at 166:21-167:8.) Thus, the plain and ordinary meaning of “write command,” as supported by the weight of the intrinsic and extrinsic evidence of record, is simply an instruction to store data (*i.e.*, irrespective of form and duration), such as the R/W signal of Yano.

Rambus argues that the write command must take the form of “one or more bits” because the specification of the Barth I patents supposedly use the terms command control information, operation code, command, and bits interchangeably. (CIB at 66; CX-10765C, Przybylski Rebuttal Q&A 163.) The evidence shows, however, that one of ordinary skill in the art would understand the specification at most confirms that different techniques *can* be used instruct the memory device to store data

associated with a write operation. In other words, the use of an operation code consisting of one or more bits is merely one preferred technique falling within the broader scope of write commands in general. (RX-5429C, Jacobs Direct Q&A 234.) One of ordinary skill in the art would view the R/W signal of Yano as satisfying this element of claim 11 of the '353 Patent.

*56 Thus, the ALJ finds that Respondents and Staff have shown by clear and convincing evidence shows that Yano discloses a R/W signal that satisfies the “write command” of claim 11 of the '353 Patent.

(3) The Memory Device Being Configured to Defer Sampling Data that Corresponds to the First Write Command Until a Strobe Signal is Detected

The evidence shows that Yano discloses the second portion of the first step of claim 11. (Jacobs, Tr. 1147:07-12; 1148:13-1150:20; RX-5429C, Jacobs Q&A 235, 236, 241, 248.) Specifically, Yano discloses “data strobe (DS)” signal that is issued from microprocessor 3 to memory 2:

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(RX-4261, Yano at Figure 1; 4:18-21; Przybylski, Tr. 2601:01-2602:07, 2604:03-12.) Yano further discloses a delay after issuing the write command (at time S2 on the system clock) until S5 on the system clock before issuing the “data strobe (DS)” signal from microprocessor 3 to memory 2. (RX-4261.0004 at 4:18-21; *see also* Figure 2.) Yano describes the use of its data strobe (DS) in the context of a write operation as follows:

[T]he memory cell corresponding to the bit in which writing is performed is discriminated with address signals ($AB_0 \sim AB_{15}$) and with the bit enable signal (BEx) on the side of memory 2, the data strobe signal (DS) creates the active state, the write data is transmitted by the databus (DBx) corresponding to this bit and the data is written to this bit.

(RX-4261.0004 at 4:18-21.) The evidence shows that one of ordinary skill in the art would understand that this disclosure in Yano, *i.e.*, the creation of an “active state” by the data strobe during which the data is written to the bit, corresponds to the sampling disclosed in the Barth specification. (RX-5429C at Q&A 236.)

Rambus argues that data strobe (DS) disclosed in Yano is distinguishable from the claimed strobe signal because the data in Yano “is simply passed into memory” rather than “sampled” at a discrete point in time. (CIB at 65-66.) However, the weight of the evidence does not support this purported distinction. (RX-5429C, Jacobs Direct Q&A 248.) Figure 2 shows that the data strobe signal (DS) is asserted low contemporaneous with the high phase of the system clock at S5 which causes data to be written to memory 2 at that point in time:

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(RX-4261, Yano at Figure 2; *see also* RX-5429C, Jacobs Direct Q&A 232, 235-236, 241, 248; Jacobs, Tr. 1139:23-1140:16; Przybylski, Tr. 2629:18-2631:21.) Therefore, the ALJ finds that Respondents and Staff have shown by clear and convincing evidence shows that Yano's memory devices defer sampling data that corresponds to the write command until the data strobe (DS) is detected as claimed.¹³

(4) Delaying for a First Time Period after Issuing the Write Command

The evidence shows that the microprocessor 3 in Yano delays for a first time period after first asserting low the R/W signal and before asserting low the data strobe (DS). (RX-5429C, Jacobs Direct Q&A 237, 241.) Indeed, as depicted in the timing diagram of Figure 2, one and a half clock cycles (corresponding to S2 to S4) lapse between the assertion of the R/W signal at the transition from S1 to S2 and the assertion of the data strobe (DS) at the transition from S4 to S5:

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*57 (RX-4261, Yano at Figure 2, 4:8-21; *see also* RX-5429C, Jacobs Direct Q&A 237, 241.) Rambus does not dispute that Yano disclosed this limitation. (CRB at 27-34.) Indeed, Dr. Przybyski stated:

Q. Do you see there is a delay between the R/W bar being asserted and the DS bar being asserted from here to here (indicating [in RDX-3293])?

A. Yes. There is a temporal difference the -- between the transition on the read/write line and the transition on the DS signal.

Q. There is a delay, right?

A. There is -- there is a delay. There is a temporal difference, right.

(Przybyski, Tr. 2604:22-2605:04.) Thus, the ALJ finds that Respondents and Staff have shown by clear and convincing evidence that Yano delays for a first period of time as claimed.

(5) After Delaying for the First Time Period, Issuing the "Strobe Signal" to the Memory Device to Initiate Sampling of a First Portion of the Data by the Memory Device

The final disputed limitation in claim 11 as to Yano involves the "strobe signal" recited in the last clause of the last step, and is closely related to the "strobe signal" limitation recited in the first step of this same claim. As set forth *supra* in Section Vi.B.1.a.3, the evidence shows that the data strobe (DS) in Yano is issued by microprocessor 3 to *initiate* sampling of data by memory 2 as claimed by the Barth Patents.

b) Dan

Respondents argue that Dan anticipates claim 11 of the '353 Patent. (RIB at 50.) Staff agrees. (SIB at 55-60.) Dan was filed by Tandem Computers, Inc. in the European Union on June 27, 1994, and lists Yei-Fong Dan as the sole inventor. (RX-4262 at cover page.) It was published on January 4, 1995 and, therefore, qualifies as prior art to the Barth Patents under 35 U.S.C. § 102(b). (*Id.*)

Rambus argues that Dan is an asynchronous memory interface that fails to disclose the strobe signal that "initiate[s] sampling of a first portion of the data" and write command of claim 11 that is "one or more bits which specify that the memory device receive and store data." (CIB at 59-60; 63-65; CRB at 27-34.) Rather, the data strobe in Dan does not initiate sampling of the data by the memory 110, but, rather, data flows into the memory over a period of time. (CIB at 63.) The clocking in the Dan reference refers to the system clock of the memory controller and does not disclose a signal that initiates the capture of data at a discrete point in time. (CIB at 63.) Dan discloses an external write strobe signal that initiates the write operation and not the sampling of data. (CIB at 63-64.)

For the reasons set forth below, the ALJ finds that Respondents and Staff have shown by clear and convincing evidence that Dan discloses each and every element of claim 11 of the '353 Patent.

(1) A Method of Controlling a Memory Device That Includes a Plurality of Memory Cells, the Method Comprising:

*58 The evidence shows that Dan discloses the preamble of claim 1. (RX-5429C, Jacobs Direct Q&A 262.) Figure 1 of Dan includes a memory interface unit 120 and a memory 110:

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(RX-4262, Dan at Figure 1; RX-5429C, Jacobs Direct Q/A 255 (describing same).) As Dan explains, the memory interface unit 120 shown in Figure 1 can be used to perform a method for writing data to memory 110:

The present invention relates generally to *an interface on a semiconductor integrated circuit (IC) to write and read data to an external memory*. More specifically, the present invention relates to a memory interface on a semiconductor IC that transfers data to a data bus and writes the data to an external memory upon the clocking of a write strobe signal. The memory interface enables and disables the semiconductor IC from transferring data to the data bus upon the assertion and deassertion of the write strobe signal.

(*Id.* at 1:01-10 (emphasis added).) Rambus does not dispute that Dan discloses this limitation. (CRB at 27-34.) Thus, the ALJ finds that Respondents and Staff have shown by clear and convincing evidence shows that Dan discloses the preamble of claim 11.

(2) Issuing a First Write Command to the Memory Device

The evidence also shows that Dan discloses this limitation of claim 11. (RX-5429C, Jacobs Direct Q&A 256-257, 262.) Specifically, Dan discloses a write command in the form of an “output enable signal 300” that is similar to the R/W signal of Yano. (RX-4262, Dan at 6:44-7:41 (“To begin the write cycle, memory interface unit 120 deasserts output enable signal 300, which is normally asserted low...to indicate external memory 110 that a write operation will take place.”), *see also* Figure 3 (timing diagram for a write operation); RX-5429C, Jacobs Direct Q&A 256-257, 262.) This output enable signal 300 of Dan is depicted in the context of a write operation in the timing diagram of Figure 3:

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(RX-4262, Dan at Figure 3; RX-5429C, Jacobs Direct Q&A 256 (describing same).)

Rambus's arguments that Dan fails to disclose this limitation are similar to those set forth *supra* for Yano, namely arguing for a narrow construction of the “write command.” As set forth *supra* in Section VI.B.1.a.2, Rambus's arguments fails for the same reason as they failed for Yano. (RX-5429C, Jacobs Direct Q&A 257, 262, 266.) Therefore, the ALJ finds that Respondents and Staff have shown by clear and convincing evidence that Dan discloses the “write command” limitation of the Barth Patents.

(3) The Memory Device Being Configured to Defer Sampling Data that Corresponds to the First Write Command Until a Strobe Signal is Detected

The evidence also shows that Dan discloses this limitation of claim 11. (RX-5429C, Jacobs Direct Q&A 258-260, 262.) Specifically, Dan discloses a “write strobe signal 309” that initiates the sampling of data by a memory device:

*59 The present invention relates generally to an interface on a semiconductor integrated circuit (IC) to write and read data to an external memory. More specifically, the present invention relates to a memory interface on a semiconductor IC that transfers data to a data bus and *writes the data to an external memory upon the clocking of a write strobe signal*. The memory interface enables and disables the semiconductor IC from transferring data to the data bus upon the assertion and deassertion of the write strobe signal.

(*Id.* at 1:01-10 (emphasis added).) As Dr. Jacobs testified at trial, this strobe signal 309 in Dan causes data to be sampled by the memory device in essentially the same manner as the claimed strobe signal of the Barth I patents. (RX-5429C, Jacobs Direct Q&A 258-260, 262.)

Rambus's arguments that Dan fails to disclose this limitation are similar to those set forth *supra* for Yano, namely arguing for a narrow construction of the "sampling." As set forth *supra* in Section VI.B.1.a.3, Rambus's arguments fails for the same reason as they failed for Yano. (RX-5429C, Jacobs Direct Q&A 258-259, 262, 267.) Therefore, the ALJ finds that Respondents and Staff have shown by clear and convincing evidence that Dan discloses this limitation of the Barth Patents.

(4) Delaying for a First Time Period after Issuing the Write Command

The evidence shows that the memory interface unit 120 delays for a first time period after first asserting the output enable signal 300 and before asserting write strobe signal 309. (RX-5429C, Jacobs Direct Q&A 260, 262.) Indeed, as depicted in the timing diagram of Figure 3, some period of time lapses between the assertion (low-to-high) of the output enable signal 300 and the assertion (high-to-low) of the external write strobe 309 as part of a write operation:

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(RX-4262 at 6:44-7:2, Figure 3; RX-5429C, Jacobs Direct Q&A 256 (describing same).) Therefore, the ALJ finds that Respondents and Staff have shown by clear and convincing evidence shows that Dan delays for a first period of time as claimed.

(5) After Delaying for the First Time Period, Issuing the "Strobe Signal" to the Memory Device to Initiate Sampling of a First Portion of the Data by the Memory Device

The final disputed limitation in claim 11 as to Dan involves the "strobe signal" recited in the last clause of the last step, and is closely related to the "strobe signal" limitation recited in the first step of this same claim. The evidence shows that the memory interface unit 120 issues the write strobe signal 309 to *initiate* sampling of data by memory 110 as claimed. (RX-4262 at 1:3-7 ("the present invention relates to a memory interface on a semiconductor IC that transfers data to a data bus and writes the data to an external memory upon the clocking of a write strobe signal.") For reasons discussed above with respect to the first step of claim 11, clear and convincing evidence shows that the write strobe signal 309 in Dan is issued by memory interface unit 120 to *initiate* sampling of data by memory 110. (RX-4262, Dan at Figure 3; RX-5429C, Jacobs Direct Q&A 256 (describing same).)

c) NextBus/Harriman

*60 Respondents argue that NextBus anticipates claims 11-13 of the '353 Patent and claims 1, 20, and 14 of the '109 Patent. (RIB at 53-62.) Staff agrees. (SIB at 62-72.)

U.S. Patent No. 5,313,624 ("Harriman") incorporates by reference the NextBus specification. Respondents argue that to the extent that NextBus fails to disclose each and every element, Harriman also anticipates claims 11-13 of the '353 Patent and claims 1, 20 and 24 of the '109 Patent. Staff agrees. (SIB at 62-72.) While Respondents performed an element by element analysis of Harriman in their initial post-hearing brief, that analysis is similar to the NextBus analysis set forth below. Indeed, many of Rambus's arguments against Harriman parallel those to NextBus, *e.g.*, Harriman does not disclose the claimed "memory device." (CRB at 37-40.) To the extent that the anticipation analysis for Harriman is strikingly similar to the analysis for NextBus, the ALJ incorporates by reference his analysis below for the Harriman reference. The ALJ finds that setting forth the analysis for Harriman would be a duplicative effort, especially in light of the fact that Harriman specifically incorporates by reference the entire NextBus specification.

Rambus argues that NextBus is not prior art and, further, that it fails to anticipate because the claimed memory device does not include a memory board containing a memory controller as disclosed by NextBus. (CRB at 37-40.) Rambus further argues that

NextBus fails to anticipate claims 12 and 13 of the '353 Patent and claims 1, 20 and 24 of the '109 Patent because it fails to disclose sampling during the odd and even phases. (CRB at 40.)

(1) *NextBus is prior art*

The NextBus Specification is a document by NeXT Inc. bearing a 1990 copyright date, and generally describes a synchronous bus architecture that could be used, for example, in a NeXT computer system. (RX-4265.0002.) If the NextBus Specification was indeed made publicly available sometime in 1990 as its copyright date suggests, it would constitute prior art under 35 U.S.C. § 102(b) based on the Barth I Patent's October 1995 priority date. However, Rambus disputes whether the the NextBus Specification was publicly available any time prior to October 1995. (CRB at 34-37.)

The Federal Circuit has articulated the standard for determining the public availability of a reference as follows:

In order to qualify as a printed publication within the meaning of § 102, a reference “must have been sufficiently accessible to the public interested in the art.” “Because there are many ways in which a reference may be disseminated to the interested public, ‘public accessibility’ has been called the touchstone in determining whether a reference constitutes a ‘ ‘ ‘ ‘ ‘printed publication’ bar under 35 U.S.C. § 102(b).” Whether a reference is publicly accessible is determined on a case-by-case basis based on the “facts and circumstances surrounding the reference's disclosure to members of the public.” A reference is considered publicly accessible if it was “disseminated or otherwise made available to the extent that persons interested and ordinarily skilled in the subject matter or art exercising reasonable diligence, can locate it.”

***61** *In re Lister*, 583 F.3d 1307, 1311 (Fed. Cir. 2009) (internal citations omitted).

The ALJ finds that the NextBus Specification is prior art under 35 U.S.C. § 102(b). The evidence shows that the NextBus Specification was publicly available sometime prior to the October 1995 priority date of the Barth I patents. In particular, the 1990 copyright date, a specified reorder number N6010 (that allowed customers to order the NextBus Specification), and technical support telephone number within the NextBus Specification collectively suggest that the document was indeed publicly available. (RX-4265.0002, RX-4265.0017; Jacobs, Tr. 1152:24-1154:07; Przybylski, Tr. 2647:14-22.) In addition, other publicly available documents in the 1991 timeframe, such as Harriman, specifically incorporate by reference a NextBus Specification, further suggesting that persons of ordinary skill in the relevant art exercising reasonable diligence could locate a copy of that reference. (RX-4277.0019 at 15:43-46; Jacobs, Tr. 1154:08-1155:07, 1165:10-1167:17.) See *Orion IP, LLC v. Hyundai Motor Am.*, 605 F.3d 967, 974-75 (Fed. Cir. 2010) (finding an Electronics Parts Catalogue with a 1987 copyright date to qualify as prior art *before* the 1988 critical date of the asserted patent “because it was accessible to those interested in the business of auto parts prior to November 10, 1988”). For at least these reasons, the ALJ finds that the evidence shows the NextBus specification is prior art at least under 35 U.S.C. § 102(b).

Rambus argues that the NextBus Specification is not prior art because there is no publication date or a retrieval date and that the reorder number and warranty information are insufficient to show public availability. (CRB at 34-35.) Rambus further argues that the cases relied upon by Staff and Respondents fail to support their arguments. (CRB at 34-37.) The ALJ finds Rambus' arguments unpersuasive in light of the evidence. Specifically, the facts and circumstances surrounding the public availability of the NextBus Specification, as set forth *supra*, support a finding that it was publicly available. Rambus's arguments simply state that such evidence is insufficient without providing a reason as to why they are insufficient.

(2) “A method of controlling a memory device that includes a plurality of memory cells” ('353 Patent claim 11)/ “A method of controlling a memory device having a memory core” ('109 Patent claims 1, 20, 24)

The NextBus Spec discloses a system that connects a processor, such as a CPU, to other devices, including memory devices with a plurality of cells. Figure 1-1 of the NextBus Spec illustrates the component parts of the NextBus system:

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(RX-4265.00014.) The NextBus connects the “master” (CPU) with the “slave” devices located in Slots 2, 4, and 6 that the CPU controls, including ““memories.” (See RX-4265.0040.) The evidence shows that “a person of ordinary skill in the art would know that one type of board you could put into [slot 2] is a memory board.” (Przybylski, Tr. at 2655:15-18.) The memory board may be used to perform burst write transactions wherein the data is written from a memory controller to a DRAM on the memory board:

62 Figure 4-11 shows timing for a NextBus burst write transaction in which the slave board uses the TMO signal to indicate that it will not accept more than one four-word data burst.

RX-4265.0048.

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(RX-4265.0049.)

Rambus argues, however, that the memory boards disclosed in the NextBus Spec are not “memory devices” as required in the asserted Barth claims. (CX-10765C at Q247; CRB at 37-38.) Rambus argues that the “memory device” in the Barth Patents is an “integrated circuit device--meaning a circuit constructed on a single monolithic substrate, commonly called a chip-in which information can be stored and retrieved electronically” and that the NextBus Spec only applies to ““memory boards,” which Rambus claims are not “memory devices.” (CX-10765C at Q244, 246; CRB at 37-38.)

The ALJ finds Rambus's arguments unpersuasive. First, Rambus fails to point to anything in the Barth Patents that supports their construction of “memory device.” Rather, the evidence shows that a memory device is simply “a device in which information can be stored and retrieved electronically.” (RX-5429C at Q310.) The IEEE dictionary, which defines the term “*device*” as a “circuit or logical group of circuits resident to *one or more boards* capable of interacting with other such devices through a bus.” (*Id.* (emphasis added).) Indeed, Rambus fails to offer any extrinsic evidence (not a single dictionary definition) to support their proposed construction that the term “memory device” has to be limited to a single monolithic substrate. (Tr. at 2657:19-2658:25.)

Second, Rambus's proposed construction of the “memory device” term was recently rejected by the Examiner during reexamination of the Barth Patents:

The Examiner agrees that a memory device can be considered a single chip, however, the Examiner notes that a memory device is not always limited to a single chip and that the patent specification also does not support that the broad term ‘memory device’ is a signal chip.

(SX-0008, February 26, 2010 Office Action at 2; RX-4246.0005; *see also* Przybylski, Tr. 2660:08-20 (disputing the construction adopted by the Examiner during reexamination of the '353 patent).) This is further supported by the evidence in this investigation. (RX-5429C, Jacobs Direct Q/A 306, 310; Jacobs, Tr. 1157:08-1158:06, 1158:25-1161:13.) For example, Dr. Jacobs testified: First, the Barth patents do not provide any special meaning to the term memory device. In fact, nothing in the Barth patents gives any indication that a memory device can only be a single monolithic chip. While I agree that a memory device can be a single monolithic chip, I do not believe a general term like memory device is that limited in scope.

*63 Second, in the reexamination of the '353 patent, the Examiner considered this issue and agreed with my opinion. Specifically, the Examiner found in the Right of Appeal Notice on page 7, which is found in R.X-4246, that a term memory

device is not limited to only a single monolithic chip, but rather “a device in which information can be stored and retrieved electronically.” The Examiner then cited to the IEEE dictionary definition to provide the plain and ordinary meaning of “device” as a “circuit or logical group of circuits resident to one or more boards capable of interacting with other such devices through a bus.” With respect to the plain meaning of the term memory device, I agree with the Examiner. It is my opinion that one of ordinary skill considering the term “memory device” as used in the asserted claims of the Barth patent would understand that a memory device can be more than simply a monolithic chip.

The NextBus Specification (RX-4265) discloses “memories” that can be connected to the NextBus in Slots 2, 4 and/or 6 as shown in Figure 1.1. A person of ordinary skill would certainly consider such “memories” as memory devices. Dr. Przybylski argues that NextBus Specification only discloses memory boards. Even [if] this is true, a person of ordinary skill would consider a memory board to be a memory device.

(RX-5429C, Jacobs Direct Q&A 310; *see also* Jacobs, Tr. 1119:15-1121:07, 1122:21-1123:17, 1156:02-1161:20.) The evidence shows that one of ordinary skill in the art would conclude that the “memories” of the NextBus Spec are “memory devices” within the meaning of the asserted claims.

Therefore, the ALJ finds that Respondents and Staff have shown by clear and convincing evidence that the NextBus Specification anticipates (or renders obvious) the “memory device” limitations and the preamble of the asserted Barth I patent claims.

(3) “issuing a first write command to the memory device” (‘353 Patent, claim 11)/ “providing control information to the memory device, wherein the control information includes a first code which specifies that a write/transfer operation be initiated in the memory device” (‘109 Patent claims 1, 20, 24)

The NextBus Spec discloses sending a write command to the memory device using a combination of signals. Specifically, as shown in Table 4-1 below, a write command for a burst write transaction is TM1* (L), TM0*(H), AD1*(L), and AD0* (H). (See RX-4265.0035; RX-5429C at Q295; CX-10765C at Q244-246.)

The evidence shows that NextBus discloses the first portion of the first step of claim 11 by sending a write command to the memory device using a combination of signals. (RX-4265.0035; RX-5429C at Q295, 306; CX-10765C at Q244-246.) More specifically, NextBus discloses a combination of signals TM1* (L), TMO*(H), AD1 *(L), and AD0*(H) that collectively represent a write command as shown in Table 4-1 below:

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*64 (RX-4265.0035; RX-5429C, Jacobs Direct Q&A 295, 306.) Rambus does not dispute that NextBus discloses this limitation. (CRB at 37-38.) As set forth *supra*, the ALJ declines to adopt Rambus's proposed narrow construction for “memory device” and, as such, the ALJ finds that Respondents and Staff have shown by clear and convincing evidence that NextBus discloses this limitation.

(4) “the memory device being configured to defer sampling data that corresponds to the first write command until a strobe signal is detected, delaying for a first time period after issuing a write command” (‘353, Cl. 11)

The evidence further shows that NextBus discloses this limitation. Specifically, the NextBus Spec discloses a system whereby two different strobe signals--DRQ* and DSTB* (discussed *supra*)--are used to write data to memory. Both signals are depicted in Figure 4-11:

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(RX-4265.0049; RX-5429C at Q&A 294, 297.) As shown above, after the combination of signals constituting the write command is issued at time D1, at time D2, the “master” sending data issues a “Data Request” strobe signal “DRQ*” “to indicate

that it is supplying two words of data in the current major cycle.” (See RX-4265.0026; see also RX-4265.0045 (“During a burst write operation, the master uses the DRQ* signal to indicate when the source is ready to transfer data.”).) This corresponds to the “strobe signal” disclosed in the Barth Patents. (RX-4540 at 8:61.) Given that DRQ* is issued to indicate that it is supplying two words of data in the current major cycle, DRQ* is data transfer start information, just like the strobe signal of the Barth Patents. (RX-5429C at Q296.)

NextBus also discloses a data strobe (DSTB*) that initiates the sampling of data by a memory device:

Data Strobe (DSTB*)

During burst transfers, the board sending data (the master during writes, and the slave during reads) generates the DSTB* signal by gating BUSCLK. The data sender asserts DSTB* at the same time that it places data on the bus. The receiver then captures data at the rising edge of DSTB*.

(RX-4265.0025 (emphasis in original); RX-5429C, Jacobs Direct Q&A 296, 306; see also Przybylski, Tr. 2648:21-2649:24, 2652:17-2653:16.) As shown in Figure 4-11, the master asserts the write command at time D1, but delays until after time D2 to assert the strobe signals DRQ* and DSTB*. Thus, DSTB* is used to sample the data (rather than a clock signal) in order to “minimiz[e] skew between the data and its clock.” (See RX-4256.0071.) Thus, as Jacob testified, DSTB* is the same type of signal and has the same purpose as DQS in the JEDEC DDR SDRAM specification Rambus alleges is covered by the asserted Barth claims. (RX-5429C at Q296.)

In addition, Rambus's own expert Dr. Przybylski admitted the relationship between the DSTB* signal and sampling in this regard:

*65 Q: Please tell His Honor yes or no, does this disclose using the strobe signal to sample data off the data bus? Yes or no, sir.

A: The receiver captures the data on the rising edge of DSTB. That's what it says.

Q: And that's sampling, isn't it?

A: That's sampling . . .

(Przybylski, Tr. 2651:17-23; 2653:13-16 (similar testimony).) Rambus does dispute that the DSTB* signal represents a data strobe signal that initiates the sampling of data. (CRB at 37-40; Przybylski, Tr. at 2651:17-21 (arguing that the DRQ* signal is not the claimed “strobe signal,” but not disputing that DSTB* reads on the “strobe signal” from the asserted Barth claims). As set forth *supra*, the ALJ declines to adopt Rambus's proposed narrow construction for “memory device” and, as such, the ALJ finds that Respondents and Staff have shown by clear and convincing evidence also shows that NextBus discloses this limitation.

(5) “issuing a strobe signal to the memory device to initiate sampling of a first portion of the data by the memory device” (“353 Patent Claim 11)/“““““providing a signal to the memory device, wherein the signal indicates when the memory device is to begin sampling write data/the transfer operation/the write operation, wherein the write data is stored in the memory core during the write operation” (“109 Patent claims 1, 20, 24)

The NextBus Spec discloses the use of two strobe signals that “initiate sampling of a first portion of the data by the memory device” and indicate “when the memory device is to begin sampling write data,” that satisfies the ““strobe signal”‘DDDD’/‘FFFF’‘FFFF’signal’DDDD’ elements of the ’353 and ’109 Patents, respectively. In the NextBus Spec, write operations take place between the CPU and the attached “slaves” (e.g., “memories”) controlled by the CPU. In the context of a burst write transaction (i.e., a write transaction involving multiple pieces of data), the NextBus Spec discloses a system whereby two different strobe signals—DRQ* and DSTB* (discussed *supra*)—are used to write data to memory. Both signals are depicted in Figure 4-11:

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(RX-4265.0049.) First, as shown in Figure 4-11, after the combination of signals constituting the write command is issued at time D1, at time D2, the “master” sending data issues a “Data Request” strobe signal “DRQ*” “to indicate that it is supplying two words of data in the current major cycle.” (See RX-4265.0026; see also RX-4265.0045 (“During a burst write operation, the master uses the DRQ* signal to indicate when the source is ready to transfer data.”).) This corresponds to the “strobe signal” disclosed in the Barth Patents. (RX-4540 at 8:61.) Given that DRQ* is issued to indicate that it is supplying two words of data in the current major cycle, DRQ* is data transfer start information, just like the strobe signal of the Barth Patents. (RX-5429C at Q296.)

66 The second separate “Data Strobe” signal “DSTB” whereby the “data sender asserts DSTB* at the same time it places data on the bus” was already discussed *supra*. Therefore, the ALJ finds that Respondents and Staff have shown by clear and convincing evidence that the strobe signal DSTB* in NextBus is issued by a memory controller to a memory device to initiate sampling as claimed.

(6) Providing / Transferring Two Portions of Data to the Memory Device and Sampling During Odd and Even Phases of a Common Clock Cycle (’353, Cl. 12-13; ’109, Cl. 1, 20, 24)

The evidence shows that NextBus discloses providing two portions of data and sampling that data during an odd and even phase of an external clock signal. (RX-5429C at Q298.) Specifically, a “synchronous (12.5 MHz), multiplexed, multimaster bus” where “a basic cycle rate of 12.5 MHz, and a mechanism that allows data burst transfers to occur at a rate of 25 MHz.” (See RX-4265.0013.) The NextBus Spec states that it “[t]ransfers two words per burst cycle.” (See RX-4265.0014.) Moreover, Figure 4-11 shows that DSTB* is used to sample the first portion of data in an odd phase of a clock cycle of MCLK* and a second portion of data in an even phase of the same cycle of MCLK*:

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(See RX-4265.0049.)

MCLK* is one of one of three clock signals disclosed in the NextBus Spec (i.e., BUSCLK, MCLKSEL*, and MCLK*), and is a 12.5 MHz internal clock with a 75% duty cycle. (RX-4265.0018-19.) MCLK* is generated from two external clocks—BUSCLK (Busclock) and MCLKSEL* (Major Clock Select). (*Id.*) The relationship between BUSCLK, MCLKSEL*, and MCLK* is shown in Figure 1-5 of the NextBus Spec. (RX-4265.0018.) As seen in Figure 1-5, BUSCLK and MCLKSEL* are used to create MCLK*. Specifically, MCLK* is the logical “OR” of BUSCLK and MCLKSEL* (i.e., MCLK is in a high position when either BUSCLK or MCLKSEL* is high):

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(RX-4265, Figure 1-5.) The reason why MCLK* has a long phase and a short phase is because it has a 75% duty cycle.

The evidence shows that a first portion of data is sampled during an even phase of the MCLKSEL* signal and a second portion of data is sampled during an odd phase of the MCLKSEL* signal, with the even and odd phases occurring during a common cycle of the MCLKSEL* signal:

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(RDX-0419; (overlaying the timing diagram of the clock signals (Figure 1-5) on the timing diagram of the other signals (Figure 4-11)); RX-5429C at 303-304.) As shown, during burst write transactions, the first piece of data is sampled by the rising edge of DSTB* during the odd phase of the external clock MCLKSEL* and the second piece of data is sampled by the rising edge of DSTB* during the even phase of external clock MCLKSEL*. (RX-5429C at 304.) As a result, both portions of data are issued during a common clock cycle of MCLKSEL*. (RX-5429C at Q298-304.) The evidence shows that one of ordinary skill in the relevant art would view this disclosure in NextBus as satisfying the double data rate limitations recited in the Barth Patent claims.

67 Rambus argues MCLKSEL does not constitute a “clock signal” as required in the asserted claims. (CRB at 40; CX-10765C at Q255.) The evidence shows, however, that MCLKSEL* is described as a clock, even containing the abbreviation “CLK” in its label. Moreover, MCLKSEL* is a free-running, periodic signal--characteristics that are indicative of a clock. As described above, MCLKSEL* is “OR” ed with another clock, BUSCLK, to form a third clock, MCLK*. (RX-5429C at Q299-301, RDX-0418.) The evidence further shows that even if MCLKSEL* were not a clock, it would make no sense to think you could “OR” a clock like BUSCLK with a non-clock signal (MCLKSEL*) and have the result still be a clock (MCLK*). (RX-5429C at Q311.) Therefore, the ALJ finds that Respondents and Staff have shown by clear and convincing evidence that NextBus discloses these limitations.

d) Hayes

Respondents argue that Hayes anticipates claim 11 of the '353 Patent. (RIB at 67-70.) Hayes is assigned to Digital Equipment Corporation was filed September 4, 1987, 1991 and issued June 8, 1993. (See RX-4268.001.) Hayes is prior art under 35 U.S.C. §102(b). (See *id.*) Staff agrees. (SIB at 62-72.)

Rambus argues that Hayes fails to disclose a “memory device” as claimed in the Barth Patents and fails to disclose a “strobo signal” that “initiates sampling” as required by the Barth Patents. (CRB at 42-43.)

(1) “A method of controlling a memory device that includes a plurality of memory cells”

The evidence shows that Hayes describes a “memory configuration system” wherein the “local bus 17 interfaces the processor chip 10 with local memory and on-board logic and supports direct memory access (DMA) transfers to and from local memory and the system bus.” (See RX-4268.0013 at 6:4-8.) Hayes also discloses a “single board computer module 9” connected to a number of “memory array boards” via a “memory array bus” as depicted in the portion of Figure 1 of the Hayes patent. (See RX-4268 at 3:45-58; 5:4-8.) Each memory array board includes a RAM Control Logic and 256Kbit Dynamic Ram Chips (DRAM), which is a “memory device” as that term is used in the asserted claims of the Barth Patents. (RX-5429C.0123.) This Examiner in the '353 Reexamination reached the same conclusion finding claim 11 of the '353 Patent invalid as anticipated by Hayes. (See RX-4246 at 7-8.) Furthermore, the evidence shows that the DRAM chips each have a plurality of memory cells as required by the asserted claims. (RX-5429C.0123.)

Rambus argues that Hayes fails to disclose the claimed “memory device.” Rambus again argues that a “memory device” cannot include memory boards that house multiple DRAM chips and an on-board controller. (CRB at 42; CX-10765C at Q358.) As the ALJ set forth *supra* in Section VI.B.1.c, the ALJ declined to adopt such a narrow reading of “memory device.” In addition, the Examiner in the '353 Reexam found that the RAM Control Logic and 256Kbit Dynamic Ram Chips (DRAM) (as shown in Fig. 7 of Hayes) to be a “memory device,” as was the entire memory array board. (See RX-4246 at 7-8.)

*68 Therefore, the ALJ finds that Respondents have shown by clear and convincing evidence that Hayes discloses the preamble of claim 11.

(2) “issuing a first write command to the memory device”

The evidence shows that Hayes discloses sending the claimed write command to a memory device. (RX-5429C.0123-25.) Figure 5 depicts the various signals used to write data from “module 9” (shown in Figure 1) to the memory array boards containing the memory devices (annotated):

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Hayes states:

Write line (WR) specifies the direction of a data transfer on DAL[31:0]. If the bus master asserts WR, then it will drive data onto DAL[31:0]. If the bus master does not assert WR, then the slave device will drive data onto DAL [31:0].

(RX-4268.0014 at 7:41-45; *see also* 19:57-59.) Rambus does not dispute that Hayes discloses this limitation. (CRB at 42-43.) Therefore, the ALJ finds that Respondent have shown by clear and convincing evidence that Hayes discloses this limitation.

(3) “the memory device being configured to defer sampling data that corresponds to the first write command until a strobe signal is detected, delaying for a first time period after issuing a write command”

The evidence shows that there is some delay period after the module 9 sends a write command to the memory device by asserting WR, “then [module 9] will drive data onto DAL [31:0].” (RX-4268 at 7:42-43; 9:58; *see also* 19:57-59 (“The byte mask, *write*, address strobe and data strobe signals perform the same functions on the memory array bus 21 as they did on the local bus 17.”) (emphasis added); RX-5429C.0125-26.) Rambus does not dispute that Hayes discloses this limitation. (CRB at 42-43.) Therefore, the ALJ finds that Respondents have shown by clear and convincing evidence that Hayes discloses this limitation.

(4) “after delaying for the first time period, issuing the strobe signal to the memory device to initiate sampling of a first portion of the data by the memory device”

The evidence shows that a Data Strobe (“DS”) is sent to the memory device to indicate that the data on the signals lines is valid and that the memory device can initiate sampling data. (RX-5429C at Q358.) Hayes teaches that a “Data Strobe line (DS) provides timing information for data transfers During a write cycle, the bus master [memory controller] asserts DS to indicate that [the data bus] contains valid write data.” (*Id.* at 7:56-65; 19:57-59 (“The byte mask, write, address strobe and *data strobe* signals perform the same functions on the memory array bus 21 as they did on the local bus 17.”) (emphasis added).). This was further corroborated during reexaminations of the '405 Patent and the '353 Patent reexamination, which found that the “DS signal let [s] the memory know when to start to read/write data” and initiate sampling. (RX-4246.0010-12; RX-5357.0014)

*69 Rambus argues that the data strobe (DS) disclosed in Hayes is not the claimed “strobe signal” because it merely identifies the type of information on the bus and does not initiate sampling of data by the memory device. (CRB at 42-43.) The evidence shows that Hayes discloses a bus master that “asserts DS, *indicating that the data is valid* on DAL [31:0].” (RX-4268.0014 at 7:61-64 (emphasis added).) Rambus relied on a similar disclosure for its infringement analysis, namely that the DQS signal “is the signal that is used to tell the receiver that *data is valid on the bus*, so not you can clock those data into . . . its registers.” (CX-9543C at 246-47 (emphasis added).) Rambus cannot construe “strobe signal” in two different ways to prove infringement and avoid invalidity. *See, e.g., Amazon.com, Inc. v. Barnesandnoble.com, Inc.*, 239 F.3d 1343, 1351 (Fed. Cir. 2001) (“A patent may not, like a “nose of wax,” be twisted one way to avoid anticipation and another to find infringement.”) (quoting *Sternner Lighting, Inc. v. Allied Elec. Supply, Inc.*, 431 F.2d 539, 544 (5th Cir. 1970) (citing *White v. Dunbar*, 119 U.S. 47 (1886))). Therefore, the ALJ finds that Respondents have shown by clear and convincing evidence that Hayes discloses this limitation.

e) Farmwald

Respondents argue that Farmwald anticipates claims 1, 2, 4, 5, 12, 13, 20, 21, and 24 of the '109 Patent. (See RX-4269; RX-5429C at Q366-384.) Farmwald '037 claims priority back to U.S. Application No. 07/510,898, which was filed on April 18, 1990. (See RX-4269.0001.) Therefore, Farmwald '037 is prior art under § 102(e). It is important to note that the only elements of claims 1, 2, 4, 5, 12, 13, 20, 21, and 24 of the '109 patent that Przybylski argues are not disclosed in Farmwald '037 are the elements concerning the signal (or code) that indicates when the memory is to begin sampling. (Tr. at 2717:10-2719:7; CX-10765C at Q379, 397-99.)

As Staff correctly noted, Respondents' arguments as to the Farmwald '037 are substantially the same as arguments made by nVidia in the prior 661 Investigation. The October 2011 hearing in this investigation did not introduce any significant, new evidence related to Farmwald '037 that would lead to a different outcome in this evidentiary hearing. (Jacobs, Tr. 1063:01-1066:09; CX-10765C, Przybylski Rebuttal Q&A 371-402.) Therefore, for the same reasons the ALJ found that the Farmwald reference in the 661 Investigation failed to anticipate the Barth Patents, he similarly finds that the Farmwald '037 fails to anticipate. Specifically, the evidence shows that AccessType [0] does not provide the "control information" or "operation codes" because it cannot be considered separate and apart from AccessType [1:3] bits. (CX-10765C.0084-85; *see also* 661 ID at 54-55.) Second, storing a delay value in an access register is not the claimed providing a signal that "indicates when the memory device is to begin sampling write data." (HTr. 1063:1-1065:6; CX-10765C.0085, 87, 89-90; *see also* 661 ID at 53-55.) The Barth Patent specification specifically distinguishes the claimed invention from prior art systems where the timing of data transfer is dictated by the timing of the request for the data transfer based on a value stored in a register. (JX-3 at 10:21-33.) The specification also identifies the use of a delay value as an alternative embodiment from the claimed signal embodiment, explaining that the alternative, unclaimed "value" embodiment does not use a strobe signal. (JX-5 at 10:52-56; CX-10765C.0087-88; *see also* 661 ID at 55-56.) Third, the evidence shows that claim 1 of the '109 Patent does require specific order. (JX-5 at 8:67-9:2; CX-10765C.0086-87.) Farmwald '037 transmits its value *before* what Respondents allege meets the providing a "code which specifies that a write operation be initiated." (CX-10765C.0086-87; RX-4269.0022 at 6:46-48.) Claim 1 recites the opposite order. (CX-10765C.0086-87.)

*70 Therefore, the ALJ finds that Respondents have failed to show by clear and convincing evidence that Farmwald '037 anticipates the '109 Patent.

f) SyncLink

Respondents argue that SyncLink anticipates claims 11-13 of the '353 Patent and claims 1, 20 and 24 of the '109 Patent. (RIB at 75-77.)

The ALJ finds that SyncLink fails to anticipate for the same reasons Farmwald '037 fails to anticipate. SyncLink discloses a packet-based communications system that is similar in many respects to that of the Farmwald '037 patent discussed above and the Farmwald '755 patent previously asserted in the 661 Investigation:

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(RX-4270C.0043; *see also* CX-10765C, Przybylski Q/A 412.) The ALJ finds that the the “flags” signal in SyncLink that Respondents contend fails to corresponds to the strobe signal/signal limitation of the asserted Barth patent claims. The evidence shows that the “flags” signal in SyncLink merely indicates “intermediary bytes,” such as address information, and thus fails to initiate sampling in the manner called for in the asserted claims. (CX-10765C, Przybylski Q&A 417) Therefore, the ALJ finds that Respondents have failed to show by clear and convincing evidence fails to show anticipation by the SynchLink. (*See id.* at Q&A 403-426; *see also* Jacobs, Tr. 1071-1081.)

The Dally Patents¹⁴

g) Effective Prior Art Date

The Respondents in their pre-hearing brief and post-hearing reply brief dispute the decision of the U.S. Patent & Trademark Office to grant Dr. Dally the benefit of a pre-filing conception/reduction to practice date. (*See* RPB at 222-224; RRB at 63-64.) However, the failure by Respondents to raise the issue in their initial post-hearing brief means that they have waived the issue. Moreover, the ALJ finds that even considering Respondents' half-hearted efforts to raise this issue in their reply brief simply do not show why it is even necessary to decide the issue. As the Staff points out, the Respondents failed to put forward any invalidity arguments where the priority date question plays any dispositive role. But even if it was relevant the ALJ agrees with Staff that the evidence fails to support the Respondents' position on priority. Accordingly, the ALJ declines Respondents' invitation to upset the U.S.P.T.O.'s decision to award the Dally patents their priority date.

h) Level of Skill in the Art

Rambus contends that a person having ordinary skill in the art during the relevant time frame of the Dally patents would have at least a bachelor's degree in Electrical Engineering or a related field and approximately three years post-baccalaureate experience working on high-speed signaling interfaces. (CX-10764C.0006.) Respondents assert that this person would have at least a Bachelor's degree in Electrical Engineering (EE) plus seven years of industry experience in the EE field, at least a Master's degree in EE plus three years of industry experience in the EE field, particularly in the field of integrated circuits, digital transmission, and communication systems. (RX-5431C at Q/A 13-14.) The ALJ does not detect a huge difference between the parties' proposed definitions of a person of ordinary skill. Indeed, this dispute does not appear to be definitive in the parties' invalidity analysis in any way.

***71** Rambus's proposed definition would have a person with fewer years of experience, but that experience would be much more focused than Respondents' propose. The ALJ believes that the level of skill in the art likely lies between the two proposals, but closer to Rambus's proposed definition. The ALJ agrees with Respondents that a person of ordinary skill would likely have a bit more experience than under Rambus's proposal, but the ALJ believes that Rambus is correct that the person's area of skill would be relatively focused. As such, the ALJ finds that the level of skill in the art would have at least a bachelor's degree in Electrical Engineering or a related field and approximately four years post-baccalaureate experience working on high-speed signaling interfaces.

i) Overview

The Respondents allege that the Dally patents are anticipated or obvious in view of eight primary references: Widmer Article (RX-4109); Odysseus (RX-4299C); LSI Logic SerialLink CWSL500 Technology; DP83840 (RX-2360C); Lau (RX-4106); Wurster (RX-4112); Widmer Patent (RX-2870), and Nakamura (RX-4114).

The Respondents further group these eight references into the following main groups: (1) The Widmer Art (Widmer Article, Widmer Patent, Odysseus, and Ewen Article); (2) LSI SerialLink CWSL500 Technology (SL 500 Art); (3) National Semiconductor Technology (DP83840 and Lau); and (4) Nakamura.

Respondents contend that DP83840, Lau, Wurster, Widmer Patent, and Nakamura anticipate and/or render obvious the asserted Dally claims. As an initial issue, Rambus and Staff argue that Respondents have waived a number of these references under Ground Rules 8(f) and 8(h) by treating the references in such a cursory manner. Rambus and Staff also argue that Respondents violated the instruction in Order No. 51 that "the parties [are to] set forth their contentions with sufficient detail so as to adequately inform the other parties of their positions on the issues for hearing" without trying to "circumvent the page limits by including contentions or arguments as exhibits to their pre-hearing statements." Rambus and Staff argue that in light of this waiver, the ALJ need not consider Respondents' arguments related to the DP83840 device, Lau, Wurster, the Widmer Patent, and Nakamura. The ALJ finds the clearest case of waiver to be the Wurster patent. It is raised only in the briefest passing in Respondents' Initial Post-Hearing Brief (RIB at 200) and in a footnote in Respondents' Reply Brief (RRB at 72 n.45). This is

completely inadequate. Accordingly, all arguments regarding Wurster are waived. As for the other references, the ALJ finds the case for a complete waiver to be less clear and will deal with those references in the individual discussion below.

j) The Widmer Art

The Respondents' first group of allegedly anticipatory art is referred to herein as the "Widmer Art," and includes the following four exhibits:

Reference	Abbreviated Name	RX Number
Single-Chip 4x500 Mbaud CMOS Transceiver (Feb. 9, 1996) (including the article and separate slides thereon)	Widmer Article	RX-4109
Odysseus Quad-SerDes Functional and Electrical Specification (Aug. 30, 1995)	Odysseus	RX-4299C
U.S. Patent No. 3,980,826	Widmer Patent	RX-2870
Single-Chip 1062Mbaud CMOS Transceiver for Serial Data Communication (Feb. 1995)	Ewen	RX-4125

(1) Background

*72 The "Widmer Art" generally relates to the work of Mr. Albert Widmer of IBM from the mid-1970s to the mid-1990s. Demonstrative RDX-0201 provides an overview of the relevant timeframe according to the Respondents:

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The first reference, chronologically, in this group, *i.e.*, U.S. Patent No. 3,980,826 (RX-2870) (the "Widmer Patent"), issued on September 14, 1976 and the ALJ finds that this qualifies as prior art to the Dally patents under 35 U.S.C. § 102(b).¹⁵ As Staff explained, this patent is an early example of an equalization mechanism that compensates for high frequency signal attenuation as similarly described and claimed in the Dally patents. (*See* RX-5431C at Q/A 279; CX-10764 at Q/A 223-224.)

Mr. Widmer called his technique predistortion, rather than pre-emphasis, though both were treated synonymously in the field. Predistortion, or pre-emphasis, had become so well known that by as early as 1992, the New IEEE Standard Dictionary of Electrical and Electronics Terms included definitions for these terms:

predistortion (pre-emphasis) (system) (transmitter performance). A process that is designed to emphasize or de-emphasize the magnitude of some frequency components with respect to the magnitude of others. *See: pre-emphasis.*

pre-emphasis (pre-equalization). (1) (General). A process in a system designed to emphasize the magnitude of some frequency components with respect to the magnitude of others, to reduce the adverse affects, such as noise, to subsequent parts of the system, de-emphasis may be applied to restore the original signal with a minimum loss of signal-to-noise ratio.

(IEEE Dictionary, RX-4429 at 999 (emphasis in original).)

As illustrated in RDX-0201 above, Mr. Widmer's work in this field continued after issuance of his patent in 1976 and resulted in an article, *i.e.*, the Widmer Article (RX-4109), that he presented at a conference in February 1996. Specifically, in the 1990s, Widmer and a team at IBM invented a chip, codenamed Odysseus that implemented the pre-distortion technique disclosed in the Widmer Patent in a semiconductor chip that was designed, built, and tested in the U.S. one year prior to the June 10, 1997 priority date. The IBM Odysseus Quad-SerDes Functional and Electrical Specification (August 30, 1995), describes the Odysseus chip. ("Odysseus Specification," RX-4299C at IBM000003.)

The same IBM employees listed on the Odysseus Specification authored a paper describing the Odysseus chip, titled *Single-Chip 4x500Mbaud CMOS Transceiver* (the "Widmer Article"). The Widmer Article was publically presented at the 1996 IEEE International Solid State Circuits Conference ("ISSCC") in San Francisco, demonstrating the operation of the Odysseus chip. (Compare RX-4299C at IBM000002 with the "Widmer Article," RX4109 at 126.) The conference took place from February 8-10, 1996.

***73** The ALJ finds that the Widmer Article was published in February 1996 at page 126 of Volume 39 of the IEEE's 1996 Digest of Technical papers. The Widmer Article was the seventh paper presented at the seventh session of the 1996 ISSCC, as indicated by the Paper FA7.7 at the top of the first page. (RX-4109 at 120; RX-5431C at Q/A 120.) The Widmer Article was distributed to attendees of the 1996 ISSCC at the conference on February 8-10, 1996 in a bound Digest of Technical Papers.

Based on the associated publication and public dissemination discussed above of the Widmer Article in February 1996, the ALJ finds that the article qualifies as prior art to the Dally patents under 35 U.S.C. § 102(b).

Respondents seek to further supplement the Widmer Article with slides that Respondents contend were presented as part of the article at the IEEE conference in whose proceedings the article was included. Respondents also rely on a set of slides describing this work that Respondents contend were presented at the conference, on February 9, 1996. Respondents argue that the slides used that day, February 9, 1996, which they contend Widmer was the primary drafter, were also published in February 1996 at pages 94-95 of the "Slide Supplement 1996" to the Digest of Technical Papers, Vol. 39 and are included in RX-4109. The ALJ finds that, while this is a close case, Respondents have presented clear and convincing evidence that the slides are a printed publication within the meaning of § 102 in part because Mr. Widmer, who was to verify that the slides were presented and publicly disseminated, failed to provide such testimony at the evidentiary hearing. *In re Klopfenstein*, 380 F.3d 1345, 1349 n.4 (Fed. Cir. 2004).

The ALJ finds that as described above the Widmer Article describes a chip with four transmitter circuits, each of which includes an equalization mechanism for high frequency signal attenuation. (See RX-5431C at Q/A 127.) In many respects, the Widmer Article is similar to the Widmer Patent in that both disclose equalization mechanisms, but the Widmer Article reflects various shifts in technology from the 1970s timeframe of the Widmer Patent to the 1990s timeframe of the Widmer Article, including a growing interest in implementing circuitry on integrated semiconductor chips rather than as discrete components. (See RX-5431C at Q/A 286; Tr. 2414:13-2416:09 (Dr. Singer).)

The ALJ finds that evidence shows that in order to submit and present the Widmer Article at the February 1996 conference, the article had to have been based on a working chip. (See RX-5431C at Q/A 205; Tr. 1551:01-07.) The ALJ finds that in the case of the Widmer Article, the working chip was "Odysseus," an IBM product described in "Odysseus Quad-SerDes Functional and Electrical Specification" (RX-4299C; Tr. 1551:08-1552:19; RX-5431C at Q/A 205-206, 208.)

(2) Enablement of Widmer Article

*74 As an initial matter, Rambus argues that the Widmer Article cannot anticipate because it is not enabled. The ALJ agrees with Respondents and Staff and finds that the Widmer Article is enabled. *See Am. Calcar, Inc. v. Am. Honda Motor Co.*, 651 F.3d 1318, 1341 (Fed. Cir. 2011) (“To be anticipatory, a reference must describe, either expressly or inherently, each and every claim limitation and enable one of skill in the art to practice an embodiment of the claimed invention without undue experimentation.”). The operative question is whether “one of ordinary skill in the art could practice the invention without undue experimentation.” *Novo Nordisk Pharms., Inc. v. Bio-Tech. Gen. Corp.*, 424 F.3d 1347, 1355 (Fed. Cir. 2005).

The Widmer Article includes as Figure 1 a block diagram of a “Quartet-transceiver”:

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(RX-4109.0002; *see also* Tr. 1534:04-14; RX-5431C at Q/A 127.) The “Quartet” part reflects the fact that there are four separate circuits therein, each circuit having a “Line Driver” and a “Line Receiver” connected to a serial output and a serial input respectively.

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Additional detail regarding the Line Driver and Line Receiver is provided in Figure 4:

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(RX-4109.0002, Figure 4; *see also* Tr. 1488:15-19, 1535:15-1538:12; RX-5431C at Q/A 127.) Notably, the label “Predistorting Driver” appears in Figure 4 in reference to the Line Driver shown to the left. (Tr. 1488:20-24, 1535:20-25.) This Predistorting Driver is described in the Widmer Article as follows:

The links have frequency-dependent attenuation (worst case 9dB at 500MHz) and discontinuities that cause significant signal distortion. The path can include 65cm of card trace and 3.5m of 25AWG, 50Ω. coax, along with 50mil-pitch microstrip card-to-card connectors, and dense 4-row 100mil-pitch shielded cable connectors. In the serial driver, a digital predistortion technique boosts high-frequency content, improving the eye opening of the received signal [2]. The low level and high level are each peaked by 50% for a 1-baud interval immediately following any transition. A circuit diagram of the predistorting driver is shown in Figure 4. Control inputs DHBASE and DLBASE set the base driver levels, and DHPEAK and DLPEAK turn on the extra drive required for peaking. The high and low levels are programmable to 1 of 4 levels. Dc-freecoding of serial data permits ac coupling to the receiver, reducing S/N degradation caused by ground shifts.

(RX-4109.0001; *see also* Tr. 1488:25-1489:14.) The “References” section of the Widmer Article explains that “[2]” in the paragraph above is a citation to the Widmer Patent previously discussed, *i.e.*, U.S. Patent No. 3,980,826. (*See* RX-4109.0002; *see also* Tr. 1543:06-25.)

The ALJ finds that the evidence shows that the Widmer Article expressly and explicitly-refers to the Widmer Patent (RX-2870) in the very paragraph discussing the “Predistorting Driver” of Figure 4. (*See* RX-4109.0002; Tr. 1543:06-25.) Thus, the Widmer Patent would have been an obvious addition to the disclosure of the Widmer Article. For at least this reason, the ALJ finds that the evidence shows that a person of ordinary skill in the relevant art would have found the Widmer Article to contain an enabling disclosure, with the Widmer Patent being exemplary of how equalization can be done using the circuits disclosed and described in the Widmer Article. (*See* RX-5431C at Q/A 134.)

*75 In a related argument, Rambus's expert, Dr. Singer, attempts to distinguish the Widmer Article as requiring the use of off-chip circuitry not disclosed in the reference. (*See* CX-10764C, at Q/A 82-83.) According to Dr. Signer, the required use of undisclosed, off-chip circuitry confirms his view that the Widmer Article is not enabled. (*See id.* at Q/A 84.) In addition, Dr. Signer contends that the off-chip circuitry required by the Widmer Article means it cannot be an anticipatory reference even assuming that it contains an enabling disclosure because the asserted claims all require that the transmitter circuitry be on-chip. (*See id.* at Q/A 85.) The ALJ finds that evidence fails to support this purported distinction.

Dr. Singer's argument relates to the DHPEAK and DLPEAK references in Figure 4, a portion of which is reproduced below:

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(RX-4109.0002.) Dr. Singer infers that DHPEAK and DLPEAK are necessarily provided from off-chip circuitry because the paragraph describing Figure 4 refers to these two signals as "control inputs." (See CX-10764C at Q/A 82-83.) However, the ALJ finds that the evidence shows that to the contrary, a person of ordinary skill in the relevant art would interpret the "input" language as referring to the signals being input *into the Predistorting Driver* portion of the chip as explicitly shown in Figure 4. (See RX-5431C at Q/A 133; Tr. 1489:15-1492:16, 1539:05-140:16.) The Widmer Article confirms this interpretation in stating that external (*i.e.*, off-chip) components are *not* required:

The 9.7x9mm² chip has 100k transistors and is fabricated in 0.5µm . . . CMOS with 4 global wiring levels (Figure 6). No external components are required.

(RX-4109.0001; *see also* Tr. 1539:18-1540:02.) As outlined during questioning of Dr. Hassoun, the Widmer Article as a whole thus provides sufficient disclosure to allow one of ordinary skill in the art to implement the Widmer chip without undue experimentation:

JUDGE ESSEX: Let me interrupt here since this is getting long. Doctor, are you familiar enough with patents to know what a person of ordinary skill in the art is?

THE WITNESS: Absolutely.

JUDGE ESSEX: If you looked at [the disclosure in Widmer] and I gave this to a person of ordinary skill in the art, could they come up with the circuit?

THE WITNESS: Your Honor, a sophomore, junior in electrical engineering would be able to look at that logic and build that simple logic circuit.

JUDGE ESSEX: Are they somewhere below the ordinary skill?

THE WITNESS: Way below the ordinary skill.

JUDGE ESSEX: Let's move on then.

MR. STACH: Thank you, Your Honor.

*76 (Tr. 1491:25-1492:16; RX-5431C at Q/A 134.) In addition, the evidence shows that it would at least have been obvious to implement the equalization mechanism described in the Widmer Article without the use of off-chip components. (Tr. 1540:17-1541:06.)

Moreover, the ALJ finds that the fact that the inputs to the DHPEAK and DLPEAK transistors are called "inputs" does not support Rambus' assertion that they must come from off-chip. First, the terms "input" and "output" are used throughout the

Widmer Article to describe on-chip signals, including those in the Serializer of Figures 1 and 2, which Rambus does not dispute are generated on-chip:

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(RX-4109 at 127.) Second, Figure 1 shows that signals received and transmitted *off-chip* are labeled “in” and “out,” not “input” and “output.” Rambus surmises that 181 pins are used “as inputs for other functions, such as providing clock signals or the ‘common logic’ signals shown in Figure 1.” (CIB at 219.) The Widmer Article discloses that these clock signals and common logic signals are made available “so output timing is controlled more precisely.” (RX-4109 at 126.) However, the ALJ finds that these signals are not related to DHPEAK and DLPEAK and are optional:

The reference input for the PLL can be selected among an external receiver clock, the transmitter reference clock, or the clock recovered from Link #0 . . . The PLL includes a dummy off-chip driver (OCD) and receiver (OCR) to compensate for I/O circuit delay variations so output timing is controlled more precisely.

(*Id.* (emphasis added)) Thus, consistent with the Widmer Article's disclosure that “[n]o external components are required,” a user can choose to use or not use these external clock and common logic signals.

Rambus suggests that the Staff improperly relies upon the Widmer Patent as supporting the disclosure of the Widmer Article. (See CIB at 217-218.) The ALJ finds this argument unpersuasive. As discussed herein, the Widmer Article is fully enabled and the Widmer Patent is merely an example of how equalization can be performed. Moreover, the record is replete with evidence justifying combining the Widmer Patent with the Widmer Article. (See Tr. 1543:06-1550:04.) Accordingly, any reference to and reliance upon the Widmer Patent is entirely proper and supported by the evidence of record.

For at least these reasons, the ALJ finds that the Widmer Article contains an enabling disclosure of an equalization mechanism as claimed in the Dally patents.

(3) *Odysseus Prior Art*

As part of the Widmer Art, Respondents rely on a document titled “IBM Odysseus Quad-SerDes Functional and Electrical Specifications” to describe an IBM project code-named “Odysseus.” (RX-4299C). Each page of this document is labeled “**IBM CONFIDENTIAL.**” (*Id.*) The cover page of the document further emphasizes that this is not a public document, stating:

*77 This document contains **IBM CONFIDENTIAL** information. All information contained herein shall be kept in confidence. The information should not be divulged to persons other than IBM employees authorized by the nature of their duties to receive such information or individuals and organizations authorized by the IBM Corporation in accordance with existing policy regarding release of company information.

(RX-4299C.0001.) Because it is not a public document, the ALJ finds that Respondents cannot rely on it as prior art.

To the extent Respondents rely on an alleged Odysseus *device* as prior art (as opposed to the Odysseus Functional and Electrical Specifications *document*), they must show, for example, that before the relevant date, the device was made in the United States, sold or offered for sale in the United States, and/or in public use in the United States. 35 U.S.C §§ 102(a), (b), and (g). As Rambus correctly points out, there is no record evidence that the device described in the Odysseus document was ever created in the United States, let alone sold or used in the United States. Instead, Dr. Hassoun speculates that because the Widmer Article

and the Odysseus document list the same authors, the Odysseus device “was the working chip that permitted the Widmer Article to be accepted and presented at ISSCC 1996.” (RX-5431C.0187.) However, besides Dr. Hassoun's speculation, Respondents provide no hard evidence to support this conclusion.

As Dr. Singer testified, there are differences in functionality between the chip described in the Widmer Article and the device described in the Odysseus document. (Tr. 2338:22-9.) For example, the Widmer Article and the Odysseus document describe differing levels of emphasis. (*Id.*) Thus, while the technology of the Widmer Article and Odysseus may have been similar in many ways, the evidence demonstrates that Odysseus was not necessarily the chip disclosed in the Widmer Article. Lacking any actual evidence that an Odysseus device was made in the United States, the ALJ finds that Respondents cannot carry their burden by clear and convincing evidence. As for prior invention, the ALJ finds the one document, standing alone, is insufficient to meet the clear and convincing standard of proof. *See Cooper v. Goldfarb*, 154 F.3d 1321, 1330 (Fed. Cir. 1998)

(4) Invalidity of U.S. Patent Nos. 7,602,857 and 7,715,494 Over the Widmer Article

The ALJ now turns to a comparison of the Widmer Article to the asserted '857 and '494 Patent claims. The ALJ finds that clear and convincing evidence shows that the Widmer Art (*e.g.*, the Widmer Article) anticipates claims 1, 4-6, 9-10, 24-28, 35-36, 39-44, 47, 53 of the '857 Patent and renders obvious claims 2, 11-13, 31-34, 49-52 of the '857 Patent, either alone or in combination with other art.

(a) Element-by-Element Analysis of Claim 1

*78 The ALJ also finds view, clear and convincing evidence shows that the Widmer Art (*e.g.*, the Widmer Article) anticipates claims 1, 2, 6, and 8 of the '494 Patent and renders obvious claims 3, 25, 26, 30, 39, 40, and 42. Indeed, the majority of the contested limitations in the '494 Patent are substantially identical in scope to corresponding limitations in the '857 Patent, and the private parties rely on the same analyses in their respective pre-trial briefs. Accordingly, the ALJ deals with the two asserted Dally patents together.

A Component Comprising A Semiconductor Chip

Clear and convincing evidence shows that the Widmer Article discloses a component comprising a semiconductor chip. (*See* RX-5431C at Q/A 131.) A micrograph of the chip disclosed in the Widmer Article appears as Figure 6:

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(RX-4109.0003, Figure 6; *see also* Tr. 1550:09-1552:19.)

A Processor Within The Chip

The evidence also shows that the Widmer Article discloses a processor within the chip. (*See* RX-5431C at Q/A 131; Tr. 1534:15-1534:11.) For example, Figure 2 depicts an “8b/10b Encoder Serializer” that processes data for a 500Mbaud Output:

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(RX-4109.0002, Figure 2; *see also* Tr. 1534:23-1535:11.) An 8b/10b encoder qualifies as the claimed processor for reasons previously discussed with respect to infringement. (Tr. 1535:09-11.) This is enlarged below:

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(RX-4109 at 126-27.)

A Transmitter Within The Chip And Coupled To The Processor To Accept A Digital Input Signal Including A Plurality Of Digital Values From The Processor

The evidence also shows that the Widmer Article discloses a transmitter within the chip and coupled to the processor. (See RX-5431C at Q/A 131.) For example, Figure 1 discloses a Line Driver within the chip and coupled to the Serializer (which includes the 8b/10b encoder):

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(RX-4109.0002, Figure 1; *see also* Tr. 1535:12-1538:12.) Further, the evidence shows that the “500Mbaud Output” accepted by the Line Driver from the Serializer (*e.g.*, as shown in Figure 2) is a digital input signal including a plurality of digital values. (See RX-5431C at Q/A 131.) This is blown up below:

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The Widmer Article discloses that the transmitter circuit (*i.e.* line driver) is coupled to the “processor” (*i.e.* the four 8B/10B encoders in the serializer). (RX-4109 at 127.) The line driver is configured to accept a 10B data from the processor (*i.e.* a digital input signal including a plurality of digital values from the processor.)

According to Rambus, the Widmer Article is distinguishable because its transmitter circuit requires off-chip components whereas the asserted Dally patent claims purportedly require that this circuitry wholly reside “within a semiconductor chip or an integrated circuit.” (CIB at 218.) Yet, as Staff clearly explains, Rambus’s expert Dr. Singer repeatedly waffled on this point during questioning by the Staff. At his deposition, Dr. Singer claimed that components of a transmitter circuit *could* reside off-chip and still fall within the scope of the asserted Dally patent claims:

*79 Q: Is it your opinion that components of a transmitter circuit could reside off chip and still satisfy the transmitter limitation of the asserted Dally patent claims?

A: It would depend on what you mean by components of. If by components of, we mean critical components to the functionality of? Then, no, I don’t believe they could be off chip and still satisfy the claims. On the other hand, if it were the power supply, or some decoupling capacitor or something that wasn’t part of the functionality, I guess in that context, I wouldn’t call that the transmitter.

(Tr. 2570:21-2571:10.) However, at trial Dr. Singer was resolute in saying that a transmitter circuit with off-chip components could *not* fall within the scope of the asserted Dally patent claims:

Q. With respect to your off-chip/on-chip distinction, are the asserted Dally patent claims broad enough to encompass a transmitter circuit with a portion that resides off-chip?

A. No.

(Tr. 2569:10-14.)

On a related point, at his deposition Dr. Singer testified that a person of ordinary skill in the relevant art could *not* tell what constitutes a “critical component” that must reside on-chip (and thus fall within the scope of the transmitter circuit limitation) without looking at an accused product or prior art reference:

Q: Could a person of ordinary skill in the art tell what a critical component is solely by looking at the asserted Dally patent claims?

A: Without looking at the transmitter in question?

Q: Yes.

A: No. I think one of ordinary skill would have to look at the specific transmitter to know.

(Tr. 2572:09-18.) However, at trial Dr. Singer flipped again in saying that such a person *could* make such a determination without looking at an accused product or prior art reference:

Q: Can a person of ordinary skill in the relevant art determine the scope of the transmitter circuit limitation in the Dally patent claims without looking at an accused product or prior art reference?

A: Yes.

(Tr. 2571:24-2572:04.)

The ALJ finds that Dr. Singer's inconsistency on this point carries over to his analysis of infringement versus validity. In instances where an Accused Dally Product or an embodiment of the Dally patents requires an associated off-chip component to transmit signals properly, Dr. Singer interprets that component as irrelevant to the analysis. (See Tr. 2544:02-2546:22, 2547:21-2552:01, 2553:06-2555:04; see also RX-5430C at Q/A 40-47.) The ALJ notes that in contrast, where a prior art product requires an analogous off-chip component, Dr. Singer interprets that component as critical to the analysis. (See, e.g. Tr. 2539:15-2544:01, 2546:24-2547:20; CX-10764C at Q/A 83-85.) In the ALJ's view, Dr. Singer's inability to maintain a consistent position on his purported off-chip/on-chip distinction and the corresponding scope of the "transmitter circuit" limitation reflects serious credibility problems that taint his entire analysis.

***80** Moreover, as for the Widmer Article in particular, Dr. Singer's position conflicts with how a person of ordinary skill in the relevant art would have interpreted the article. For example, Dr. Hassoun noted that article explicitly refers to its circuitry as being wholly on-chip:

Q. Doctor, do you see the DH peak and DL peak at the top and bottom [of RX-4109.0002, Figure 2] which I believe you testified about?

A. Yes, I do.

Q. Are those generated on chip or off chip?

A. On chip.

Q. Why do you say that?

A. Well, the title of the paper is a single chip, but also if you look at column 2 on the bottom, it says specifically, no external components are required. There is no doubt that it is on chip.

Q. Let's see if we can get that paragraph for you. Can I get the first page of the Widmer article [RX-4109.0001] and the last full paragraph. It starts with the "9.7." Is this the paragraph you are referring to?

A. That is.

Q. And what portion of this paragraph were you referring to?

A. If you look at the second sentence, it says, “no external components are required.”

Q. Despite this sentence here, do you have an opinion as to whether external components are nonetheless required to generate the DH peak and DL peak signals off chip?

A. It would be a ridiculous thing to do, because at that point, you have signals that are operating - the current bit and the previous bit are operating at 500 [meg]abit per second, which is a very, very high speed. So for you to take those off chip, build a circuit that has to handle that kind of high speed, and then bring those signals back on chip, that would be a very costly endeavor and it makes no sense whatsoever.

(Tr. 1539:05-1540:16.) In light of Dr. Hassoun's testimony and other evidence of record, the ALJ finds that a person of ordinary skill in the relevant art would have viewed the Widmer Article's circuitry as being *on-chip*.

The Transmitter Circuit Being Operable To Send An Output Signal (With Pre-Emphasis/Pre-Distortion)

Finally, the ALJ finds that the evidence shows that the Widmer Article anticipates or renders obvious a transmitter circuit with an equalization mechanism as claimed (*i.e.*, pre-emphasis/pre-distortion circuitry). (RX-5431C at Q/A 132, 135; Tr. 1535:12-1538:12, 1539:05-1541:06, 1543:06-1550:04.)

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The remaining limitations require a transmitter circuit that is operable to “emphasize high frequency components of the output signal relative to low frequency components of the output signal so that (i) an output bit signal of the output signal . . . has one signal level when the bit value is the same as a bit value represented by a predetermined preceding output bit signal; and (ii) the output bit signal . . . has another signal level when the bit value is different from the bit value represented by the predetermined preceding output bit signal.

*81 The Widmer Article discloses a transmitter circuit using a “predistortion technique [that] boosts high-frequency content, improving the eye opening of the received signal.” (*Id.* at 126.) “The low level and high level are each peaked by 50% for a 1-baud interval immediately following any transition.” (*Id.*) The Widmer Article also discloses the predistortion circuit that implements pre-emphasis, as shown here. The Widmer Article discloses that “no external components are required” (*i.e.*, the predistortion circuit, as well as all the circuitry required to perform pre-emphasis are found on-chip). (*Id.*) Thus, the ALJ finds that the Widmer Article discloses the remaining limitations of claim 1 by boosting higher components such that there is one signal level after repeated bits (non-peaked signal level) and another signal level after transition bits (50% peaked signal level). (Tr. at 1536:7 to 1540:16.)

Accordingly, the ALJ finds that Widmer anticipates claim 1 of the '857 Patent.

(b) The Remaining Independent Claims of the '857 Patent

The remaining independent claims of the '857 Patent generally capture the same functionality and therefore, are disclosed by the same prior art. For example, claims 24, 35 and 39 require a “component circuit” rather than a processor. A “component circuit” includes a “processor”; thus, the Widmer Article's four 8B/10B encoders of meet this limitation. Claims 24 and 35

require “the transmitter circuit is operable to select each signal level as a function of the digital value represented by that signal level and of the digital values represented by one or more preceding signal levels.” The Widmer Article discloses determining the output based on the present digital value and immediately preceding digital value. Moreover, Rambus does not raise any independent arguments against these particular claims. Accordingly, the ALJ finds that the Widmer Article anticipates the remaining independent claims of the '857 Patent.

(c) Independent Claims 1, 25, and 39 of the '494 Patent

The ALJ finds that the independent claims of the '494 Patent are either anticipated or rendered obvious by the same evidence considered above with regards to the other independent claims or rendered obvious by the Ewan article. The independent claims require a transmitter circuit (claims 1 and 25) or a transmitter (claim 39) within a semiconductor chip. (RX-5431C at Q/A 186.) Claim 1 of the '494 Patent requires “the transmitter circuit generating a sign which depends upon the value of the bit represented by such output bit signal and generating a magnitude which is a function of the value of the bit represented by such output bit signal and the values of the bits represented by one or more preceding output bit signals, each output bit signal having sign and magnitude determined by the generated sign and generated magnitude.” The Widmer Article discloses generating a sign (DHBASE and DLBASE) and a magnitude (DHPEAK and DHPEAK). (*Id.*) As shown in the pre-emphasized output signal to the left, each output bit has a sign and magnitude determined by DHBASE, DLBASE, DHPEAK, and DLPEAK. (RX-5431C at Q/A 186.)

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*82 Accordingly, the ALJ finds that this together with the analysis discussed above for Claim 1 of the '857 Patent, the Widmer Article anticipates claim 1 of the '494 Patent.

(d) Claims 25 and 39 of the '494 Patent

Independent claims 25 and 39 of the '494 Patent include a requirement not found in other asserted claims that the output signal be a *differential* output signal. Claim 25 is representative, and reads in pertinent part:

a transmitter circuit within the chip, the transmitter circuit being operable to accept a digital input signal including a plurality of bits and send a *differential output signal* including a series of output bit signals, each bit of the digital input signal being represented by a single output bit signal

(JX-121 at 10:42-47 (emphasis added).)

“a differential output signal”

As discussed above, Claims 25 and 39 of the '494 Patent require the additional feature of transmitter with a differential output signal. The Widmer Article cites to the Ewen Article, which explicitly discloses differential signaling.¹⁶ The Widmer Article points the reader to the Ewen Article, stating that the “serializer/deserializer (SerDes) design adopts techniques use previously” in the Ewen Article. (RX-4109 at 126, n.1.) The Ewen Article discloses a 1.062 Gbps high-speed transmitter including a serial driver with differential outputs. (RX-4125 at 32.)

Respondents contend that the Ewan Article is incorporated by reference into the Widmer Article and therefore, they should be considered together for anticipatory purposes. However, as the Federal Circuit has explained, “in order for one document to incorporate another document by reference, the incorporating document must identify the incorporated document with detailed particularity, clearly indicating the specific material for incorporation.” *Kyocera Wireless Corp. v. Int'l Trade Comm'n*, 545 F.3d

1340, 1352 (Fed. Cir. 2008). A mere cross-reference to another document, like the Widmer Article's reference to Ewen, is not sufficient. *Id.* (“[V]ague referencing practice is hardly sufficient to meet this court's legal requirements for incorporation”). Thus, the Widmer Article/Ewen Article combination cannot be used for purposes of anticipation.

However, while the combination cannot be used for anticipation, the ALJ finds that it would have obvious to one of ordinary skill to implement differential outputs. The ALJ finds that a person of ordinary skill would understand that an output signal can either be single-ended or differential. (RX-5431C at Q/A 194.) In differential signaling, the signal consists of two wires that carry complementary signals (*e.g.*, if one signal is “high,” the other is “low”). (Tr. 1486:20-22.) A single-ended signal consists of a single wire that carries one of the differential signals, but not the complement. (Tr. 1487:5-7.) To switch from a differential to single-ended output, one could simply ignore the complementary signal. Similarly, to switch to a differential signal, one merely needs to generate the complement of the single-ended signal.

*83 The ALJ finds that clear and convincing evidence also shows that it would have been obvious to modify the system disclosed in the Widmer Article to implement differential signaling as called for in claims 25 and 39. Specifically, while the Widmer Article discloses single-ended signaling, it explicitly references the Ewen article which used differential signaling instead. (Tr. 1486:01-1488:14.) The ALJ finds that the evidence shows that it would have been obvious to a person of ordinary skill in the relevant art to implement well known differential signaling techniques such as Ewen with the system of the Widmer Article where increased speed and noise tolerance were bigger concerns than reduced pincount. (*See* RX-5431C at Q/A 194; Tr. 1552:20-1553:23.)

Rambus alleges “the Widmer Article teaches away from differential signaling due to the increased wire count required to implement differential signaling.” (CIB at 227.) But “[a] known or obvious composition does not become patentable simply because it has been described as somewhat inferior to some other product for the same use.” *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994).

But the ALJ finds that the Widmer Article teaches that a single-ended output can be used to reduce wire count. One of ordinary skill would have been well aware of this and other benefits and drawbacks of single-ended versus differential signaling. (RX-5431C at Q/A 194.)

Moreover, the ALJ finds that a person of ordinary skill would understand the well benefits of using one type of signaling versus the other. (RX-5431C at Q/A 194.) For example, the Widmer Article discloses using single-ended outputs to reduce wire count. (RX-4109 at 126.) A person of ordinary skill in the art would understand the benefits of using differential signaling. For example, Dally discloses using differential signaling in part because it has better “noise immunity” than “any single-ended approach.” (RX-2239.0198.) The Dally Patents do not expressly teach single-ended signaling, but the independent Asserted Claims cover singled-ended, as well as, differential signaling. Similarly, the Widmer Article discloses using differential outputs signals to one of ordinary skill in the art.

This conclusion is further supported by Dr. Hassoun's testimony at trial where he explained at trial that engineers routinely switch between single-ended signaling versus differential signaling depending on the particular constraints they are facing when designing a given system:

Q. Would a person of ordinary skill in the art choose to implement single-ended signaling versus differential signaling in some contexts?

A. Yes, absolutely.

Q. Why?

A. Well, it depends on your constraints. For example -- or what problems are you going to solve? For example, if you look at the Widmer article, they made a choice to implement single-ended because they had wiring constraint. They were designing

the chip for a particular application that had that particular constraint. If you didn't have that constraint, you might choose to implement differential signaling in there, to make, for example, your receiver design a little bit easier. It doesn't have to work so hard at figuring out the high and the low. It can use differential signaling. So there is -- those are examples of considerations you would have, whether you would use differential or single-ended.

*84 (Tr. 1552:25-1553:23.) Thus, the ALJ finds that while the chip discussed in the Widmer Article may have been designed with single-ended signaling for a pin-count sensitive application, it would have been obvious to a person of ordinary skill in the relevant art to modify that chip to use differential signaling in other applications in which pin-count was *not* a significant concern. Stated another way, system constraints define whether single-ended or differential signaling is used rather than vice versa. Accordingly, the ALJ finds that independent claims 25 and 39 are invalid for obviousness.

(e) Claims 2, 31, and 49 of the '857 Patent, Claim 3 of the '494 Patent

Unlike claim 1 of the '857 Patent and claim 1 of the '494 Patent, the ALJ finds that clear and convincing evidence fails to show that the Widmer Article anticipates claims 2, 31, and 49 of the '857 Patent and claim 3 of the '494 Patent. However, clear and convincing evidence does show that claim 2 would have been obvious in view of the Widmer Article alone or in combination with other art.¹⁷ This claim reads:

2. The component as claimed in claim 1 wherein the transmitter circuit is operable to send the output signal with an output frequency of at least 1 GHz and a bandwidth greater than 100 MHz.

(JX-120 at 8:64-67.) With respect to claim 2, there appear to be different interpretations of the claim that materially impact the validity analysis. Rambus is of the view that claim 2 specifies a 1 Gbps output data rate “for a single channel NRZ waveform over one line” -- *i.e.*, a single, serial channel. (See Tr. 2326:04-08.) By contrast, the Respondents are of the view that claim 2 is broad enough to read on a system where a 1 Gbps output data rate is split over multiple channels, as allegedly recited in dependent claim 5. (RX-5431C at Q/A 155-157; Tr. 1564:15-1567:06.) The ALJ finds that the evidence supports Rambus's interpretation of the claims *in part*.

More specifically, the claims must be viewed collectively to fully understand the nature of the output data rate called for in claim 2. Starting with claim 1, this claim broadly recites a processor coupled to a transmitter circuit that sends an output signal -- *i.e.*, one processor, one transmitter circuit, and one output signal. (See JX-120 at 8:45-63.) Dependent claim 5 adds a requirement that the transmitter circuit of claim 1 be coupled to one or more I/O connections. (See JX-120 at 8:45-63.) In this system, the I/O connections are redundant such that the same “output signal” is duplicated on however many I/O connections are utilized, with the output data rate being merely that of a single transmitter circuit. (Tr. 2322:01-2323:13.) This fact is verified by contrasting claim 5 with claims 11 and 12. Namely, claim 11 requires the processor of claim 1 be coupled to at least one “additional” transmitter circuit which sends an “additional” output signal -- *i.e.*, one processor, multiple transmitters, and a corresponding number of output signals. (See JX-120 at 9:26-31.) Claim 12, which depends from claim 11, adds the requirement that the multiple transmitter circuits be coupled to a plurality of I/O connections. (See *id.* at 9:32-35.) Thus, claim 12 envisions a system different from claim 5 in which the I/O connections are *not* redundant. Namely, in claim 12 there are multiple transmitter circuits coupled to a common processor, each transmitter circuit providing an output signal on an I/O connection, the aggregate data rate of the multiple output signals collectively representing the total data rate for the overall system. (See Tr. 2326:20-2327:07.) It bears noting, however, that both claim 5 and claim 12 specify the “output signal” in terms of a given transmitter circuit. This supports Rambus's view that the “output signal” term recited in other claims, such as dependent claim 2, likewise refers to that of a given transmitter circuit rather than that of a combination of transmitter circuits as proposed by the Respondents.

*85 Applying this understanding to the Widmer Article, the individual transceivers disclosed therein have an output data rate of 500 Mbaud -- *i.e.*, one half the 1 Gbps output data rate required under a proper interpretation of this claim. (See RX-4109.0002, Figure 1.) Moreover, the ALJ finds that one cannot consider the data rates of all four of the transceivers as a collective (*i.e.*, $4 \times 500 \text{ Mbaud} = 2 \text{ Gbaud}$) because: (1) such a configuration no longer satisfies the requirement of claim 1 that *the* transmitter circuit (*e.g.*, the Line Driver in the Widmer Article) be coupled to *the* processor (*e.g.*, the 8b/10b Serializer in the Widmer Article); and (2) the data rate recited in claim 2 is specified in terms of "the output signal" of a given transmitter circuit rather than multiple output signals from multiple transmitter circuits. Thus, the ALJ finds that clear and convincing evidence fails to show anticipation of claim 2 by the Widmer Article.

However, the ALJ finds that clear and convincing evidence does show obviousness in view of the Widmer Article either alone or in combination with other art. For example, the Widmer Article refers to a secondary reference (Ewan, RX-4125) that its design "adopts techniques" from:

The serializer/deserializer (SerDes) design adopts techniques used previously but includes functions to support transparent operation and relax timing constraints at the system interface[1].

(RX-4109.0001; *see also* RX-4109.0002 ("[1] Ewen, J.F. et al. 'Single-Chip 1062MBaud CMOS Transceiver for Serial Data Communication,' ISSCC Digest of Technical Papers, pp. 32-33, Feb., 1995").) Ewen discloses a chip with a serial output at 1062 Mbaud:

This work implements the media independent functions specified in the emerging ANSI fibre channel standard at 1062.5Mbaud. Integrated onto a single CMOS chip are: two phase-locked loops (PLL) for clock generation and clock recovery, a selectable 1B or 2B parallel interface with corresponding multiplexer and demultiplexer for parallel-to-serial and serial-to-parallel conversion, word alignment logic for byte synchronization, 8B/10B coder and decoder, and high-speed differential CMOS PECL drivers and receivers for the serial I/O.

(RX-4125.0001; *see also* RX-5431C at Q/A 160; Tr. 1497:17-1498:05.) The evidence shows that it would have been obvious to modify the system disclosed in the Widmer Article to achieve an output data rate of 1.062 Gbps as disclosed in Ewen, particularly in light of the need for increasingly fast data transmission techniques in certain implementations. (Tr. 1498:06-13, 1501:08-15.)

The ALJ has already found the independent claims that claims 31 and 49 of the '857 Patent and claim 3 of the '494 Patent depend on invalid as anticipated by the Widmer Article. There is no material difference between these independent claims and claim 1 of the '857 Patent depends on. Rambus also raises no unique arguments for claims 31 and 49 of the '857 Patent and claim 3 of the '494 Patent. Accordingly, the ALJ finds that the analysis above for claim 2 of the '857 Patent applies with equal force to claims 31 and 49 of the '857 Patent and claim 3 of the '494 Patent.

*86 Accordingly, the ALJ finds that claims 2, 31, and 49 of the '857 Patent invalid as obvious in light of the combination of the Widmer Article and Ewan Article.

(f) Dependent Claims 30 and 42 of the '494 Patent

Dependent claims 30 and 42 of the '494 Patent recite a similar, but slightly different variation of this limitation. Exemplary claim 30 reads:

30. The circuit of claim 25, where the series of output signals is transmitted by the transmitter onto a signal path at a rate of at least 400 megahertz.

(JX-122 at 10:65-67.) While parties treat the “rate” aspect of '494 Patent claims 30 and 42 the same as the “output frequency” aspect of '494 Patent claim 3 and '857 Patent claims 2, 31, and 49, claims 30 and 42 of the '494 Patent requires a transmitter circuit that outputs at a rate of “400 megahertz,” which is *slower* than the “1 GHz” required to meet the latter set of claims. This distinction is relevant to the Widmer Article, which discloses a transmitter circuit that outputs at 500 MHz, which is less than 1 GHz but more than 400 MHz.

More specifically, the Widmer Article discloses a Quartet transceiver in which each transceiver has an output data rate of 500 MBaud. (See RX-4109.0002, Figure 1.) Because 500 MBaud is less than the “1 GHz” required to satisfy the output frequency limitation under both of the proposed constructions for that limitation, the ALJ has determined that the Widmer Article does not anticipate claim 3 of the '494 Patent and claims 2, 31, and 49 of the '857 Patent. Because 500 MBaud is *greater* than the “400 megahertz” required to satisfy the rate limitation of these claims as construed by the ALJ, the ALJ finds that the Widmer Article teaches this limitation. The ALJ has already determined that independent claims 25 and 39 are obvious in light of the combination of Widmer and Ewan. Rambus appears to agree as it only disputes anticipation of those claims under its flawed interpretation of “output frequency” and “rate.” (See CIB at 222.) Accordingly, the ALJ finds that claims 30 and 42 are also rendered obvious for the reasons stated above and for the reasons stated above with respect to independent claims 25 and 39.

(g) Claims 11, 32, and 50 of the '857 Patent

The ALJ finds that clear and convincing evidence fails to show that the Widmer Article anticipates claim 11, 32, and 50 of the '857 Patent. However, the ALJ finds that clear and convincing evidence does show that the additional limitations of these claims would have been obvious in view of the Widmer Article alone or in combination with other art.

More specifically, claim 11 (which is representative of claims 11, 32, and 50) requires “at least one additional transmitter circuit within the chip” that is also “coupled to the processor” of claim 1. (See JX-120 at 9:26-32.) According to the Respondents, the four individual transceivers correspond to the “additional transmitter circuit” of claim 11. (See RIB at 153-154.) However, as discussed in detail with respect to claim 2, the Respondents have not identified a common processor coupled to the four individual transceivers as claimed. (See RX-5431C at Q/A 174-175; Tr. 1492:20-1494:15.) Rather, the Respondents appear to be relying on the 8b/10b Encoder Serializer within a given transceiver as the claimed “processor” even though that particular component is not coupled to multiple transmitter circuits as claimed. (See RX-5431C at Q/A 174-175; Tr. 1492:20-1494:15.)

^{*87} Nonetheless, the ALJ finds that clear and convincing evidence shows that it would have been obvious to implement the system disclosed in the Widmer Article in a configuration with multiple transmitter circuits coupled to a common processor, particularly given the Widmer Article's disclosure of a Quartet-transceiver system that could be used with an upstream processor.¹⁸ (See Tr. 1542:05-1543:05.) Moreover, Rambus does not appear to raise any validity arguments specific to the additional limitations added in claim 11. (See CIB at 218-228.)

(h) Claim 8 of the '494 Patent

The ALJ finds that clear and convincing evidence shows that the Widmer Article discloses the “reprogrammable” limitation added by way of dependent claim 8 of the '494 Patent. For example, the Widmer Article explains that “[t]he high and low

levels are programmable to 1 of 4 levels.” (RX-4109.0001; *see also* RX-5431C at Q/A 192-193.) Rambus does not contest this limitation.

(i) Additional Dependent Claims of the '857 and '494 Patent

Clear and convincing evidence also shows that the Widmer Article discloses the limitations added by way of the remaining claims. (RX-5431C at Q/A 136-154, 169-173, 176, 177, 179, 180, 182-185, 187-191, 195, 196, 198-200.) In fact, Rambus does not appear to raise any validity arguments specific to these limitations added by way of these claims. (*See* CIB at 218-228.) Accordingly, the ALJ finds that clear and convincing evidence shows that the remaining dependent claims of the '857 Patent and the '494 Patent are rendered invalid by the Widmer Article.

The remaining claim limitations are discussed below:

(j) Pre-emphasis: claims 4, 9, 10, 26, 41, 42, 47 and 53 ('857 Patent) and 2 and 6 ('494 Patent)

This group of dependent claims includes limitations requiring specific forms of pre-emphasis. These claims are anticipated or rendered obvious based on the same evidence shown for claim 1 of the '857 Patent. Claims 4 and 26 of the '857 Patent and claim 2 of the '494 Patent recite emphasizing signal levels after transition bits related to repeated bits. Claims 9, 10 and 47 of the '857 Patent recite the each input bit is represented by one of the signal levels in the output signal. Claims 41, 42 and 53 of the '857 Patent and claim 6 of the '494 Patent recite selecting the signal level as a function of the present bit and one or more preceding or the immediately preceding bits. All of these limitations are disclosed by the Widmer Article, which teaches a transmitter circuit that emphasizes the output signal after transition bits relative to repeated bits by comparing the present bit value the immediately preceding bit value. (*See* RX-5431C at Q/A 137, 139, 140, 143, 149, 150, 152, 153, 154, 188-190.) Accordingly, for these reasons, and for the reasons stated above with respect to the independent claims on which these claims depend, the ALJ finds that the Widmer Article anticipates claims 4, 9, 10, 26, 41, 42, 47 and 53 ('857 Patent) and 2 and 6 ('494 Patent).

(k) I/O connections: claims 5, 12, 27, 33, 43 and 51 ('857 Patent)

*88 The “I/O connections” claims (claims 5, 12, 27, 33, 43 and 51) of the '857 Patent require that the chip have “I/O connections and the transmitter- circuit is coupled to one or more of the I/O connections to send the output signal through the one or more I/O connections.” As shown above in relation to claim 1 of the '857 Patent, the Widmer Article discloses that the chip has I/O connections and the transmitter circuit is coupled to a cable through an I/O connection. (RX4109 at 127; *see also id.* at 95 (“22 signal I/Os”).) Therefore, the Widmer Article discloses the I/O connections limitation. (*See, e.g.*, RX-5431C at Q/A 138, 144, 151.) Rambus does not appear to dispute that this limitation is present in the Widmer Article.

The ALJ has already determined that independent claims 1, 24, and 39 of the '857 Patent are anticipated by the Widmer Article. As discussed above, the I/O connection limitation is also disclosed in the Widmer Article. Claims 5, 27, and 43 depend on claims 1, 24 and 39 respectively and add only the I/O connection limitation. Accordingly, the ALJ finds that claims 5, 27, and 43 are anticipated as well.

As for claims 12, 33, and 51, they depend on claims 11, 32, and 50 respectively. The ALJ has found claims 11, 32, and 50 invalid as obvious in light of the Widmer Article. Claims 12, 33, and 50 only recite one additional limitation over the claims that have already been found invalid. That limitation is the I/O connection limitation discussed above. Because the I/O limitation is found in Widmer Article, claims 12, 33, and 51 are also obvious in light of Widmer for the reasons discussed with respect to claims 11, 32, and 50. Accordingly, the ALJ finds that claims 12, 33, and 51 are obvious.

(l) “nonmodulated”: claims 6, 28 and 44 ('857 Patent)

This group of claims require sending the output signal in nonmodulated form. As shown in relation to claim 1 of the '857 Patent, the Widmer Article discloses an output signal that is in nonmodulated form. (*See also* RX-4109 at Fig. 7.) Further, there is no description in the Widmer Article of a modulated output (*e.g.*, using the output signal of the transmitter to modulate a carrier signal). Therefore, the Widmer Article discloses the nonmodulated claims. (*See, e.g.*, RX-5431C at Q169.)

Claims 6, 28, and 44 are dependent claims. They depend on claims 5, 27, and 43 respectively. Claims 5, 27, and 43 have been found to be anticipated (*See* “I/O Connection Claims” discussion above). The only limitation that claims 6, 28, and 44 add is the non-modulated limitation, which is present in the Widmer Article. Accordingly, claims 6, 28, and 44 are also found anticipated by the Widmer Article.

(m) multiple transmitters/parallel stream of data/parallel bus: claims 13, 34, and 52 ('857 Patent) and 26 and 40 ('494 Patent)

*89 Claims 13, 34 and 52 of the '857 Patent recite output signals representing a parallel stream of data from the processor. Claims 26 and 40 of the '494 Patent recite sending output bit signals on lines of a parallel bus. All of these claims are disclosed by the four 500 Mbps transmitters of the Widmer Article, which can be configured to receive a parallel stream of data from the 8B/10B encoders and output bit signals on a parallel bus. (RX-4109 at 126-27.) Thus, the Widmer Article discloses the additional limitations of these claims. (*See, also*, RX-5431C at Q/A 175-76, 195, 198.) Rambus does not dispute the presence of these particular limitations.

Claims 13, 34, and 52 depend on claims 11, 32, and 50 respectively. The ALJ has found claims 11, 32, and 50 invalid as obvious in light of the Widmer Article. Claims 13, 34, and 52 only recite one additional limitation over the claims that have already been found invalid. That limitation is the parallel data stream from the processor limitation discussed above. Because the parallel data stream from the processor is found in Widmer Article, claims 13, 34, and 52 are also obvious in light of Widmer for the reasons discussed with respect to claims 11, 32, and 50. Accordingly, the ALJ finds that claims 13, 34, and 52 are obvious.

(n) processor: claims 25, 36 and 40 ('857 Patent)

The claims recite that the “component circuit” be a processor. As discussed above in relation to claim 1 of the '857 Patent, the Widmer Article discloses four 8B/10B encoders that make up the processor. Thus, the Widmer Article discloses the processor limitation. (*See, e.g.*, RX-5431C at Q/A 142.) Claims 25, 36, and 40 are dependent claims. They depend on claims 24, 35, and 39 respectively. The ALJ has found that claims 24, 35, and 39 are anticipated by the Widmer Article. The only additional limitation that claims 25, 36, and 40 have over claims 24, 35, and 39 is the processor limitation. Accordingly, because the Widmer Article discloses all of the limitations of claims 25, 36, and 40, they are anticipated by the Widmer Article.

k) The SL500 Art

In addition to the Widmer Art described above, the Respondents also rely on several invalidity theories stemming from a chip called the “SerialLink SL500” (which incorporates the “CWSL500 Technology” or “CWSL500 core”) that was allegedly “conceived, reduced to practice, used, and offered for sale well before the applicable bar dates associated with the Dally patents.” (RIB at 165-166.) The parties dispute whether the SL500 art even qualifies as prior art. The ALJ will turn to that issue first.

Respondents contend that the SL500 Art is prior art under §§ 102(b) and (g). However, Rambus contests whether the SL500 Art is available as prior art. (*See* CIB at 232-233; 240-241). The Staff agrees with Respondents that, at the very least, the SL500 Art qualifies as prior art under § 102(b).

(1) Availability of the SL500 Art as Prior Art

*90 The ALJ finds that the evidence shows that the SL500 Art indeed constitutes prior art to the Dally patents under 35 U.S.C. § 102(b) and/or § 102(g). More specifically, the ALJ finds that the SL500 Art to qualifies as prior art based on LSI having offered to sell the SL500 Art to customers Seagate and Cabletron in 1995 and based on LSI having conceived and reduced to practice the claimed invention (as implemented in the SL500 Art) prior to the June 1996 critical date of the asserted Dally patents. As discussed below, the ALJ finds that the evidence in this case shows that LSI manufactured the first SL500 chips in *** and provided prototype SL500 chips to Seagate no later than ***, both occurring prior to the June 1996 critical date of the asserted Dally patents. Thus, LSI was the first to reduce to practice the claimed invention. The evidence also shows that LSI conceived of the claimed invention (e.g., as to be implemented in a CWSL500 core) at least by ***, and was diligent in reducing to practice the invention as part of ultimately developing and producing the prototype chips provided to Seagate and Cabletron no later than ***. For at least these reasons, the SL500 Art also qualifies as a prior invention of the Dally patents by LSI under 35 U.S.C. § 102(g)(2). Moreover, the ALJ finds that the evidence shows that LSI also offered the device for sale to both Seagate and Cabletron more than one year before Dally filed for his patent. Thus, it also qualifies as prior art under § 102(b).

(a) Prior Invention Under 102(g)

As discussed below, the evidence in this case shows that LSI manufactured the first SL500 chips in *** and provided prototype SL500 chips to Seagate no later than ***, both occurring prior to the June 1996 critical date of the asserted Dally patents. Thus, LSI was the first to reduce to practice the claimed invention. The evidence also shows that LSI conceived of the claimed invention (e.g., as to be implemented in a CWSL500 core) at least by ***, and was diligent in reducing to practice the invention as part of ultimately developing and producing the prototype chips provided to Seagate and Cabletron no later than ***. For at least these reasons, the SL500 Art also qualifies as a prior invention of the Dally patents by LSI under 35 U.S.C. § 102(g)(2).

Legal Standard

A patent claim also is invalid if before the patentee's invention, "the invention was made in this country by another inventor who had not abandoned, suppressed, or concealed it. In determining priority of invention under [102(g)], there shall be considered not only the respective dates of conception and reduction to practice of the invention, but also the reasonable diligence of one who was the first to conceive and last to reduce to practice, from a time prior to conception by the other." 35 U.S.C. § 102(g)(2). "[A] challenger [to a patent's validity] such as [LSI] has two ways to prove that it was the prior inventor: (1) it reduced its invention to practice first . . . , or (2) it was the first party to conceive of the invention and then exercised reasonable diligence in reducing that invention to practice." *Mycogen Plant Sci., Inc. v. Monsanto Co.*, 243 F.3d 1316, 1332 (Fed. Cir. 2001). Claims of prior invention must be corroborated. *See Finnigan Corp. v. ITC*, 180 F.3d 1354 (Fed. Cir. 1999). Whether corroborating evidence is sufficient when considering all of the pertinent evidence is evaluated under the "rule of reason." *Loral Fairchild Corp. v. Matsushita Elec. Indus. Co.*, 266 F.3d 1358, 1363 (Fed. Cir. 2001). Under a "rule of reason" analysis, "it is not necessary to produce an actual over-the-shoulder observer. Rather, sufficient circumstantial evidence of an independent nature can satisfy the corroboration requirement." *Cooper v. Goldfarb*, 154 F.3d 1321, 1330 (Fed. Cir. 1998) (finding reduction to practice proven by the inventor's testimony corroborated by testimony of his co-workers that he had told them of his reduction to practice, and that they had seen him obtain materials of the type necessary to practice the invention.); *see also Lacotte v. Thomas*, 758 F.2d 611, 613 (Fed. Cir. 1985 (affirming finding of reduction to practice, stating "[t]he testimony of Thomas, the inventor, and the written evidence of his reduction to practice in his notebook, are corroborated by independent circumstantial evidence of his withdrawal of supplies to practice the invention, as well as independent corroborating testimony of his associate, Lee.")).

*91 The date of conception "defines the legally operative moment of invention." *Invitrogen Corp. v. Clontech Labs., Inc.*, 429 F.3d 1052, 1063 (Fed. Cir. 2005). Conception requires an actual recognition of that which constitutes the inventive subject matter. *See id.*

The earliest possible filing date of the parent application to which the Dally patents claim priority is June 20, 1997. Dally alleges a conception date of *** in his invention disclosure (RX-4147C; RX-4148C), this disclosure form does not demonstrate conception of all the claims of the Dally Patents although Rambus does not press the point in its briefs. Absent proof to the

contrary, Dally's conception date is the filing date of the parent application to which the Dally Patents claim priority, June 20, 1997. However, it is irrelevant because LSI has alleged a conception date well before Rambus's alleged conception date, so if LSI can establish conception and reduction to practice, the SL 500 art will be prior art regardless of Rambus's date of invention. See *Mahurkar v. C.R. Bard, Inc.*, 79 F.3d 1572, 1577 (Fed. Cir. 1996) ("Stated otherwise, priority of invention goes to the first party to reduce an invention to practice unless the other party can show that it was the first to conceive the invention and that it exercised reasonable diligence in later reducing that invention to practice." (quotation marks omitted)).

LSI's Conception of SL 500 Art

The ALJ finds that LSI Logic had conceived of the SL 500 Art as early as *** when it was informing its customers that the CWSL500 technology included the emphasis functionality. (RX-4173C.0030-31.) The ALJ finds that at this time, LSI Logic also had defined the basic characteristics of the CWSL500 technology and was offering the CWSL500 for sale to its customers as discussed in greater detail below. (RX-4150; RX-4128; and RX-4156C.0015.) The ALJ also finds that by ***, LSI Logic had developed documentation and product manuals detailing the functionality and characteristics of the CWSL500. (See e.g., RX-4116C.0002-0014; RX-4130.0007-60.) These documents illustrate that LSI Logic recognized the inventive subject matter *** and appreciated that which they had invented. By ***, LSI Logic engineers had completed SPICE configuration files and transistor level schematics. (RX-4116C.0044-191; RX-4143C and RX-4144C *** RX-4520C; see also, RX-5430C at Q/A 379-381, 486-490, 498-505.) LSI Logic also had performed simulations on the CWSL500 circuitry that depicted the emphasis functionality. (RX-4092C; (RDX-350); RX-4094C; see also RX-5430C at Q/A 379-391.) Accordingly, the ALJ finds LSI Logic conceived of the invention by *** at the latest. However, as previously described, LSI Logic's conception occurred much earlier, and in any case, earlier than Dally.

LSI's Reduction to Practice of the SL 500 Art

The ALJ finds LSI Logic reduced its invention of the CWSL500 technology to practice prior to Dally. Establishing an actual reduction to practice requires that (1) an inventor constructed an embodiment or performed a process that met all the limitations of the claims, (2) the inventor determined that the prior invention worked for its intended purposes, and (3) that the inventor engaged in sufficient testing to demonstrate reduction to practice in instances where testing is required to demonstrate that the invention worked for its intended purpose. See *4 Techs., Inc. v. Microsoft Corp.*, 507 F.3d 1340, 1352 (Fed. Cir. 2007) (citing *Cooper v. Goldfarb*, 154 F.3d 1321, 1327 (Fed. Cir. 1998)).

*92 Independent third-party evidence corroborates LSI Logic's reduction to practice of the SL500 chip. For example, the SL500 is alluded to in a *** email correspondence between ***. (RX-4176C.) *** Accordingly, the CWSL500 was reduced to practice in the SL500 chip as early as *** and no later than ***.

LSI Logic also published a paper in February 1997 related to the CWSL500 and its emphasis functionality. (RX-4107.) Because publication in the ISSCC requires that the author have manufactured a working chip, LSI Logic unquestionably had developed a functional SL500 chip that included emphasis. (Tr. 1675:16-1680:13.) In fact, for publication in February 1997, LSI Logic would have had to submit its paper in September 1996. (*Id.* at 1608:11-22.) Indeed, the design of the CWSL500 had been completed for almost a year and the first SL500 chips had been fabricated well before Dally presented his research. ***

(RX-2772C.0103.) Accordingly, as is further corroborated by Drs. Dally and Poulton, LSI Logic. (See also RX-5422C at Q/A 80-86.; RX-2772C.0077-78; RX-2772C.0102-103.)

The ALJ also finds that LSI Logic also reduced the CWSL500 technology to practice in the Shemp chip in ***. (RX-4142.0002, Schedule Table.) In particular, the ALJ finds that LSI Logic worked on layout and tape out of the Shemp chip from *** and sent the first prototype chips to Cabletron in ***. (*Id.*) As set forth above, the ALJ finds that the Shemp chips incorporated four CWSL500 cores and anticipated each and every claim of the Dally Patents. (RX-4128.0002.) Rambus argues that the Shemp

chip did not include the emphasis functionality. In support of this assertion, Rambus cites to a document that ***. (RX-4511C.) However, as testified by Dr. Hajimiri, however, the *** is not indicative of anything. Indeed, this document reflects ***. (Tr. at 1625:24-1626:24.)

LSI's Diligence in Reducing SL 500 to Practice

LSI was diligent in reducing the SL500 Technology to practice as demonstrated by the following evidence:

- LSI Logic began offering the CWSL500 technology for sale to its customers as early as *** and continued offering the CWSL500 technology to its customers throughout ***. (See RX-4156C.0015; RX-4128; RX-4142C.)
- LSI Logic regularly met with its customers to inform them of the CWSL500 technology and provided information regarding the CWSL500's functionality. (See, e.g., RX-4173C.0010, 23, 30-31, 48-49, and 65-67.) LSI Logic also provided its customers with product literature. (RX-4150; RX-4149.)
- From ***, LSI Logic engineers were diligently running simulations to verify the CWSL500 circuitry and design of the SL500 chip. (RX-4092C (RDX-350); RX-4094C; RX-4520C.)
- In ***, LSI Logic prepared CWSL500 product manuals and additional documentation. (RX-4116C.0002-14; RX-4130.0007-60.)
- From ***, LSI Logic engineers were diligently designing and developing the Shemp chip for Cabletron that incorporated the CWSL500. (See RX-4136; RX-4137C; RX-4138; RX-4519C.)

*93 • In January 1996, LSI Logic informed the general public that it had received SL500 chips back from fabrication as is evidenced by its ***. (RX-4176C.)

- In ***, LSI Logic worked on layout and tape out of the Shemp chip. (RX-4142C; RX-4138; RX-4519C.)
- In ***, LSI Logic delivered the first prototype Shemp chips to Cabletron. (RX-4142C.)
- July and September 1996, LSI Logic began publishing articles regarding the CWSL500 technology. (RX-4123; and RX-4107 (while this article was published in February 1997, testimony supports that it would have had to be submitted in September 1996 for inclusion in the publication (Tr. 1608:11-22.).)

Therefore, because LSI Logic (1) conceived of the invention disclosed in the Dally Patents (*i.e.*, the CWSL500 technology); (2) diligently reduced the invention to practice; and (3) did not abandon, suppress, or conceal its invention of the CWSL500 technology, each and every asserted claim of the Dally Patents is invalid under § 102(g).

Rambus's Arguments in Response

In response to this evidence, Rambus argues that this section of the Patent Act does not apply because “neither the SL500 nor the Shemp chip met all the limitations of the asserted Dally claims” and because the equalization circuitry “was not functional” in these chips. (See CIB at 241.) According to Rambus, these deficiencies preclude a finding that LSI (and/or its personnel) qualifies as having previously invented the subject matter of the asserted Dally patent claims under 35 U.S.C. § 102(g). Neither argument is persuasive.

The first argument is really whether the claims anticipate. The ALJ perceives the proper inquiry as whether the SL 500 prior art has the features LSI claims it does. If LSI can prove the SL 500 has the particular features it claims it does, then those features will be entitled to the priority date that LSI claims. The ALJ will then undertake the second step below of determining whether LSI's SL 500 Art anticipates or not.

Turning next to whether the equalization circuitry in the SL500 Art worked as intended, Rambus relies on the testimony of its expert Dr. Singer to establish *** (CIB at 234 (citing CX-10764C at Q/A 363-367; Tr. 2584:09-2586:12).) A similar argument is made Rambus as to *** (See CIB at 236 (citing Tr. 2587:04-2589:14).) *** (See CIB at 235 (citing RX-5430C.0018-19; RX-4171C.0006-7).) Rambus surmises that LSI never actually produced a version of the SL500 Art with working equalization circuitry, and certainly did not provide such a chip to Seagate or Cabletron. (See CIB at 236-237.) The ALJ finds that Rambus's arguments are contrary to the weight of the evidence.

First, the ALJ finds that clear and convincing evidence confirms that LSI conceived of using equalization circuitry within the SL500 Art in the ***. For example, ***:

***94** (RX-4116C.0007.) Similarly, a "SerialLink™ SL500 Document Set," also from the *** timeframe, describes this same set of inputs:

RX-4130.0047. ***. (See RX-4173C.0048; Tr. 2517:15-2518:13, 2520:10-19 (discussing RX-4173C.0048).) LSI further confirmed that this equalization circuitry would, in fact, perform pre-emphasis/de-emphasis as claimed in the Dally patents by performing simulations on the conceived design:

(RX-4094C; see also RX-5430C at Q/A 388-390 *** While the particular circuit diagrams/layouts of the equalization circuitry that LSI ultimately chose to implement within the SL500 Art may not be of record, such circuitry was well known in the prior art as exemplified by the Widmer Article, the Widmer Patent, and other art of record. Thus, the ALJ finds that clear and convincing evidence shows that LSI conceived of using equalization circuitry within the SL500 Art in the *** timeframe.

To the extent that Rambus disputes whether the simulations show *working* versions of equalization circuitry, Rambus's arguments are premised on the flawed reasoning of its expert Dr. Singer. As Respondent LSI's expert Dr. Hajimiri testified at trial, ***

(CX-5430C at Q/A 495-496.) Dr. Hajimiri's testimony is corroborated by an article from 1997, in which a version of the SL500 Art with equalization circuitry therein was described in considerable detail. (See RX-4017 (article entitled "A 1.0625 Gbps Transceiver with 2x-Oversampling and Transmit Signal Pre-Emphasis" and including reference to "The GigaBlaze(TM) SerialLink™ CWSL500 transceiver core.")) As Dr. Hajimiri explained, the IEEE conference at which this article was presented required that there be a working version of the chip, thus confirming his view that working equalization circuitry was indeed ultimately produced by LSI. (See Tr. 1675:10-1680:13.)

Lastly, Rambus correctly observes that some of the documents on which LSI relies *** (See RX-5430C.0018-19; RX-4171C.0006-0007).) However, the ALJ finds that this observation is not relevant. Much like the equalization circuitry in certain of the Accused Dally Products, the SL500 Art as conceived by LSI contained *** (See RX-5430C at Q/A 466.) This fact is verified *** Proof that the SL500 Art discloses working equalization circuitry that *could* be enabled invalidates even the asserted method claims because, unlike an infringement analysis under Section 271, an invalidity analysis under Section 102 does not require evidence of a prior art product actually being used in the claimed manner. See Manual of Patent Examining Procedure, § 2112.02 (Process Claims) (8th Ed. With July 2008 Revisions) (citing *In re King*, 801 F.2d 1324, 1326-1327 (Fed. Cir. 1986)).

Accordingly, Rambus's arguments against finding that the SL 500 Art is prior art under § 102(g) are rejected.

(b) Public Sale

Legal Standards

*95 With respect to the offers for sale alleged to be prior art, “the § 102(b) on-sale bar applies when two conditions are met before the critical date: (1) the product is the subject of a commercial offer for sale, and (2) the invention is ready for patenting.” *August Tech. Corp. v. Camtek, Ltd.*, 655 F.3d 1278, 1289 (Fed. Cir. 2011) (citing *Pfaff v. Wells Elecs., Inc.*, 525 U.S. 55, 67 (1998)). “An invention can be found to be ‘ready for patenting’ in at least the following ways: by proof that it was reduced to practice, or by proof that the inventor had prepared drawings or other descriptions of the invention that were sufficiently specific to enable a person skilled in the art to practice the invention.” *Cargill, Inc. v. Canbra Foods, Ltd.*, 476 F.3d 1359, 1368 (Fed. Cir. 2007). In addition, in certain circumstances an invention may qualify as prior art even if it is not ready for patenting at the time the offer is made. See *August Tech.*, 655 F.3d at 1289 (“The issue presented in this case is whether the invention must be ready for patenting at the time the alleged offer is made. We conclude that it does not.”). So long as an “offer for sale is extended and remains open, a subsequent conception will cause it to become an offer for sale of the invention as of the conception date.” *Id.* at 1289.

As discussed below, the ALJ finds that the evidence in this case shows that LSI offered to sell the SL500 Art to both Seagate and Cabletron ***, that the SL500 Art was ready for patenting prior to the June 20, 1996 critical date of the asserted Dally patents, and that the offers to sell remained open at that time. Thus, the SL500 Art qualifies as on-sale bar prior art to the Dally patents under 35 U.S.C. § 102(b).

Background Regarding SL 500 Sales

The ALJ finds the following background facts regarding the sales of the SL 500. The “CWSL500 core” refers to the “core ware” of the SL500 Art. (Tr. 1607:01-18.) A “core” constitutes a design that can subsequently be instantiated in an actual chip as discussed previously with respect to infringement. LSI personnel developed equalization circuitry within a CWSL500 core sometime in the ***, and reduced to practice a corresponding SL500 chip with a CWSL500 core instantiated therein sometime *** (RX-5430C at Q/A 519; Tr. 1607:19-25.) LSI also produced a BDSL500 evaluation board that contained an SL500 chip in this general timeframe. (Tr. 1608:01-04.) Thus, the three critical aspects of the SL500 Art consist of: (1) CWSL500 cores; (2) SL500 chips; and (3) BDSL500 evaluation boards. That a working SL500 chip (with associated cores and evaluation boards) was indeed ultimately produced by LSI is verified by a February 1997 article presented at the International Solid-State Circuits Conference on the SL500 chip, which required a working chip for presentation of an article. (See RX-4107.) The particular article here (RX-4107) refers to a SL500 chip with programmable pre-emphasis functionality, thus confirming that a working SL500 chip was produced in the *** timeframe. (RX-4107; Tr. 1675:10-1680:13.)

The Cabletron Prior Art Issues

*96 Turning to the Cabletron issues in particular, evidence of record as to the commercial offer for sale includes a ***, (RX-4128.0002; RX-5430C.0293 at Q/A 23-25; RX-4137C.0001; RX-4138.0004; Tr. 1685:18-1686:09, 1687:19-1688:09.) *** (RX-4142C.0001 (Business Table).) The chip was eventually shipped to Cabletron roughly one year later:

(Tr. 1683:04-09.)

The record includes considerable detail as to the development schedule for the chip sold to Cabletron. For example, the record includes a *** Thus, the evidence supports the Respondents' argument that LSI offered to sell an SL500 chip to Cabletron that was "ready for patenting" before the priority date of the asserted Dally patents. (RX-5430C.0294 at ¶ 30; Tr. 1611:25-1613:05; 1619:08-1620:09, 1620:25-1624:17, 1681:15-1682:03, 1683:04-09.)

The Cabletron Offer

Turning to the Cabletron offer, *** (See CIB at 234 (citing RX-4128.001; Tr. 1620:25-1622:09).) According to Rambus, *** that this offer to Cabletron cannot be a qualifying offer for sale under 35 U.S.C. § 102(b) because *** (CIB at 234.) Again, whether an offer was accepted is irrelevant as the Patent Act only requires that a qualifying offer be made -- *not* that it further be accepted. See 35 U.S.C. § 102(b). Here, the ALJ finds that clear and convincing evidence shows an offer for sale that qualifies under Section 102(b) based on conception (and ultimately reduction to practice) of the invention as embodied by the Shemp chip having occurred while the offer to Cabletron remained open. For example, the evidence includes ***

***. (RX-4142C.0002, Schedule Table.)

For at least these reasons, Rambus's arguments that LSI did not make a qualifying offer to sell Shemp to Cabletron should be rejected.

The Seagate Prior Art Issues

Turning to Seagate, evidence of record as to the commercial offer for sale to Seagate includes a ***

(RX-4156C.0011; see also RX-5430C.0290, at ¶¶ 1-4.) ***

(RX-4149.0011.) That an actual SL500 chip was indeed ultimately provided to Seagate is demonstrated by *** Thus, the ALJ finds that the evidence supports the Respondents' argument that an SL500 chip circuitry was offered for sale to Seagate and "ready for patenting" (*e.g.*, used by Seagate (during testing)) before the priority date of the asserted Dally patents. (RX-5430C.0292 to 0293, ¶¶ 21-22; Tr. 1611:25-1613:05; 1615:19-1616:01.)

Rambus argues that *** on which the Respondents rely include nothing more than *** and thus cannot constitute an offer for sale under 35 U.S.C. § 102(b). (CIB at 233.) However, the ALJ agrees with Staff that even assuming that Rambus's characterization of the *** is accurate, additional evidence of record is more specific to the SL500 Art in particular. ***

*97 (RX-4149.0004.) Indeed, the ALJ notes that *** Given the above, the ALJ finds that the evidence as a whole demonstrates that in *** LSI indeed offered to sell an SL500 chip to Seagate that included equalization circuitry.

Rambus's argument regarding the relevance of the offer for sale is based on a misleading cite to only a portion of the *August Tech.* opinion, wherein the Federal Circuit explained that "there is no offer for sale until such time as the invention is conceived." CIB at 233. (quoting *August Tech. Corp. v. CamTek, Ltd.*, 655 F.3d 1278, 1289 (Fed. Cir. 2011)). The larger paragraph from which this quote was taken explains that subsequent conception will cause a prior offer to qualify as an offer for sale under 35 U.S.C. § 102(b):

[W]e conclude that an invention cannot be offered for sale until its conception date. Hence, if an offer for sale is made and retracted prior to conception, there has been no offer for sale of the invention. In contrast, if an offer for sale is extended and remains open, a subsequent conception will cause it to become an offer

for sale of the invention as of the conception date. In such a case, the seller is offering to sell the invention once he has conceived of it. Before that time, he was merely offering to sell an idea for a product.

August Tech., 655 F.3d at 1289. Such a series of events occurred here. Namely, as discussed above clear and convincing evidence shows an offer for sale *** followed shortly thereafter by conception (and ultimately reduction to practice) of an SL500 chip that embodies the invention claimed in the Dally patents. That the conception occurred while the offer for sale remained open is demonstrated by *** who ultimately tested an SL500 chip provided by LSI, which would not have taken place had LSI retracted its prior offer. (See RX-4175C.0065 to 0074.)

Ready For Patenting

While LSI Logic was offering the CWSL500 technology to Seagate and Cabletron, the CWSL500 technology also was ready for patenting. First, ***

***RX-4094C; RX-4092C (RDX-350); see also RX-5430C at Q/A 379-391.)

LSI Logic engineers diligently ran hundreds of simulations *** while finalizing the CWSL500 circuitry and laying out the SL500 chip. (RX-4520C.) *** (RX-4520C.)

As discussed above, the CWSL500 technology was reduced to practice no later than *** in the SL500 chip. (RX-4176C.) The SL500 was a silicon implementation of the CWSL500. (RX-4130.0020.) As is standard practice in the industry, LSI Logic would have tested the SL500 chips to ensure they operated properly prior to distributing them to customers. (Tr. at 1644:5-1645:18.) *** Accordingly, the ALJ finds that the CWSL500 was ready for patenting in ***, and no later than *** based on the reduction to practice of the CWSL500 circuitry in the SL500 chip. As such, the ALJ finds that the CWSL500 was ready for patenting while LSI Logic was offering to sell the CWSL500 technology to Seagate and Cabletron.

Rambus's Arguments

*98 Rambus argues that Respondents cannot show that there was an offer to sell the CWSL500 technology to Seagate that would constitute an on-sale bar to the asserted Dally Patents. (CIB at 233.) The ALJ finds that despite Rambus's assertions to the contrary, the *** Additional documentation and the testimony of Dr. Hajimiri further confirm that these *** reflect an offer to sell the CWSL500. (See e.g., RX-5430C.0290-92; RX-4150; RX-4149.) Accordingly, LSI Logic began offering the CWSL500 technology to Seagate as early as ***

Rambus also argues that there is no evidence that an offer to Seagate remained open through the time the CWSL500 technology became ready for patenting. (CIB at 233.) However, *** Thus, the evidence shows that LSI Logic continued to offer to sell the CWSL500 technology to Seagate while the technology was ready for patenting.

Rambus also argues that Respondents cannot show that there was an offer to sell the CWSL500 technology to Cabletron that would constitute an on-sale bar to the Dally Patents. (CIB at 234.) The ALJ finds that this argument ignores evidence showing *** (RX-4142C.001-2; Tr. 1680:24-1683:9; see also RX-4136, RX-4138.) The ALJ finds that not only did the offer not expire, it resulted in a final contract and LSI shipping the Shemp chips that incorporated the CWSL500 cores. Accordingly, the ALJ finds that there can therefore be no dispute as to whether LSI Logic's offer to sell the CWSL500 technology to Cabletron satisfies the requirements of § 102(b).

(2) Invalidity Of U.S. Patent No. 7,602,857 and Over The SL500 Art

The ALJ finds that clear and convincing evidence shows that the SL500 Art discloses each and every limitation of asserted claims 1, 2, 3, 4-6, 9, 10, 24-28, 31, 35, 36, 39, 41-44, 47, 49 and 53 of the '857 patent, and also renders obvious asserted claims 11-13, 32-34, and 50-52. The invalidity analysis set forth in this section is based largely on the following documents, all of which describe the SL500 chip and/or the CWSL500 core instantiated within that chip, and collectively provide sufficient detail to show that the chip/core was “ready for patenting” prior to the critical date of the asserted Dally patents:

Exhibit Number	Document Description
RX-4520C	***
RX-4176C	***
RX-4175	*** RX-4175C.0065-73; RX4175C.0076-77 (excerpts included as RDX-4031 and RDX-4074) ***. RX-4173.0159-160 (excerpts included as RDX-4032).
RX-4130C	***
RX-4116C	***
RX-4094C	***. RDX-350 (excerpt provided in RDX-4076) ***
RX-4092C	***

⁹⁹ (See also RX-5430C at Q/A 376-392.) Additional supporting documentation is identified by Dr. Hajimiri in his direct witness statement. (See *id.* at Q/A 51.)

(a) Element-by-Element Analysis of Claim 1 of the '857 Patent

A Component Comprising A Semiconductor Chip

Clear and convincing evidence shows that the SL500 Art discloses a component comprising a semiconductor chip. (RX-5430C at Q/A 394.) More specifically, a CWSL500 core was instantiated within sample SL500 chips, and provided on BDSL500 evaluation boards to various customers. *Id.* at Q/A 374-375, 392-393. ***

(RX-4130.0021.)

Moreover, the CWSL500 itself was a high-speed serial interface core that consisted of fully defined, optimized and reusable circuits. (RX-4130.0015.) LSI Logic designed the CWSL500 core for integration and implementation on semiconductor chips. (RX-4130.0021, Fig. 1.3.) ***. (RX-4130.0020.) ***. (RX-4128 *** RX-4156C.0015 ***) in these customer-specific ASICs, *** (RX-4130.0015-16.) Thus, the ALJ finds that there can be no doubt that the CWSL500 technology, and LSI Logic's interactions involving the CWSL500, necessarily were directed towards implementing the CWSL500 on semiconductor chips and the SL 500 technology meets this limitation.

A Processor Within The Chip

Clear and convincing evidence also shows that the SL500 Art discloses (and/or renders obvious) a processor within the chip. (See RX-5430C at Q/A 395-396.) *** (See RX-4130C.0020 ***; see also RX-4130.0018 *** For example, the SL500 chip included *** (See e.g., RX-4130.0020 *** (RX-4128.0002, Table 1.)

A Transmitter Within The Chip And Coupled To The Processor To Accept A Digital Input Signal Including A Plurality Of Digital Values From The Processor

The ALJ finds that clear and convincing evidence also shows that the SL500 Art discloses (and/or renders obvious) a transmitter within the chip and coupled to the processor. (See RX-5430C at Q/A 397-398.) Moreover, this is discussed at least at RX-4130C.0017: *** In addition, a transmitter is shown in Figure 2.1 below:

(RX-4130C.0028.) The evidence further shows that the transmitter circuit in the SL500 Art accepts a digital input signal including a plurality of digital values from the processor. (See RX-5430C at Q/A 398.) For example,

In particular, Rambus is of the view that the SL500 Art required the use of "*****" (as illustrated below):

(RX-4116.0060.) The ALJ finds that the evidence fails to support this purported distinction. For example, the named inventor Dr. Dally took a contrary view during prosecution in relying on his reduction to practice of a chip that ***. (See RX-2014 at ¶¶ 6-7; RX-5430C at Q/A 40-43; see also Tr. 1761:16-1764:13 (Poulton); Tr. 1763:14-1764:6 (Dally); RPX-0002C.) In addition, Dr. Hajimiri testified at trial that *** (See Tr. 1627:14-1628:01.) Accordingly, the ALJ finds that Rambus is incorrect and the SL 500 prior art does disclose a transmitter.

The Transmitter Circuit Being Operable To Send An Output Signal (With Pre-Emphasis/Pre-Distortion)

*100 Finally, the ALJ finds that clear and convincing evidence shows that the SL500 Art anticipates a transmitter circuit with an equalization mechanism as claimed (i.e., pre-emphasis/pre-distortion circuitry). (RX-5430C at Q/A 399-401.) *** (CIB at 234-237.) *** (CIB at 234.) However the ALJ finds that the evidence instead shows that the equalization circuitry in the SL500 Art was indeed complete and operational with respect to the equalization circuitry therein. (See RX-5430C at Q/A 491-496.)

The CWSL500's transmitter circuit was operable *** (See RX-4130.0047 *** RX-4116C.0006(***; RX-4116C.0007 *** (See e.g., RX-4116C.0060, 62, 72, 80.) Further, the CWSL500 technology's emphasis functionality was operable such that "(i) an output bit signal of the output signal representing a particular bit value has one signal level when the bit value is the same as a bit value represented by a predetermined preceding output bit signal; and (ii) the output bit signal representing the particular bit value has another signal level when the bit value is different from the bit value represented by the predetermined preceding output bit signal." (See *id.*) ***

((RDX-348 (RX-4094C); see also RDX-3471 *** (RX-5430C at Q/A 388-90.) ***. (RX-5430C at Q/A 382-84.)

(RDX-4076 (excerpt from RDX-350), RX-4092C.)

Dr. Singer asserts that the emphasis *** (CX-10764C at Q/A 363-66.) However, the ALJ finds that the evidence shows that there is no *** (*Id.*) *** (*Id.*) *** (*Id.*) ***.

Rambus also argues that because the CWSL500's emphasis functionality was *** (RX-4130.0047; RIB at 167-72), either the CWSL500's transmitter did not have emphasis or that its emphasis functionality was inoperable. However, the evidence shows that *** (Tr. 1615:10-1616:1.)

In addition, the ALJ finds that as was discussed with respect to infringement, the fact that *** in the SL500FCT product does not constitute the absence of emphasis functionality. (*Compare* Tr. 790:22-791:5.) Under the same rationale as Rambus's infringement theory, ***

Accordingly, as set forth above, the CWSL500 technology anticipates each and every limitation of asserted claim 1 of the '857 Patent. (*See also*, RX-5430C at Q/A 394-401.)

(b) Independent Claims 24 and 35 of the '857 Patent:

Claims 24 and 35 of the '857 Patent are independent claims that are similar in scope to claim 1 of the '857 Patent except that claims 24 and 35 recite a “component circuit,” instead of a “processor,” and describe the emphasis functionality in a slightly different manner. Notwithstanding, the ALJ finds that claims 24 and 35 are disclosed by the CWSL500 technology for many of the same reasons cited above in relation to claim 1. (*See, e.g.*, RX-5430C at Q411-419, 428-436.) First, the ALJ finds that *** used in conjunction with the SL500 and Shemp chips were component circuits. (RX-4130.0017, Fig. 1.1, 20-21; RX-4128.0002.) Also, the ALJ finds that as set forth in relation to claim 1, the CWSL500 included the emphasis functionality. The CWSL500 simulations further show that each digital value was represented by one of the signal levels of the output signal.¹⁹ (RX-4092C (RDX-350); RDX-347; RX-4094C, hereinafter collectively referred to as “Simulation Waveforms”).

*101 With respect to claim 24, the ALJ finds that the simulations show that the output bit signal from the CWSL500's transmitter had one signal level when a digital bit value of the input signal was the same as a digital bit value represented by a predetermined preceding output bit signal, and one signal level when a digital bit value of the input signal was different from a digital bit value represented by a predetermined preceding output bit signal. (*Id.*; *see also* RX-5430C at Q419.)

With respect to claim 35, the ALJ finds that the simulations show that transmitter circuit was operable to select each signal level as a function of the digital value represented by that signal level and the digital value represented by the immediately preceding signal level. (Waveform Simulations; *See also* RX-5430C at 436.)

Accordingly, the ALJ finds that the SL 500 art anticipates independent claims 24 and 35.

(c) Independent Claim 39 of the '857 Patent:

Claim 39 of the '857 Patent is an independent claim that is similar in scope to claims 1 and 24 of the '857 Patent except claim 39 describes the transmitter circuit within the chip in a slightly different manner. Notwithstanding, the ALJ finds that claim 39 of the '857 Patent is disclosed by the CWSL500 technology for many of the same reasons cited above in relation to claims 1 and 24 of the '857 Patent. (*See, e.g.*, RX-5430C at Q438-443.) Additionally, the ALJ finds that the CWSL500's transmitter circuit was coupled to the component circuit ***, such that the transmitter accepted a digital input signal including a plurality of bit values from the component circuit. (RX-4130C.0018, 20.) The ALJ finds that the CWSL500's transmitter circuit also was operable to send an output signal including a series of signal levels representing the digital values. (RX-4130C.0018.)

Accordingly, as with all of the other asserted independent claims of the '857 Patent, the ALJ finds that the SL 500 art anticipates Claim 39.

(d) Dependent Claims 2, 31, and 49 of the '857 Patent

Turning to the dependent claims, the ALJ finds that clear and convincing evidence shows that the SL500 Art outputs data at a rate of 1.0625 Gbps and thus discloses the additional limitations (as construed by the ALJ) added by way of claims 2, 31, and 49. (*See* RX-5430C at Q/A 402; RX-5430C.0291, Hajimiri Direct at ¶ 11; Tr. 1628:09-13, 1683:18-1684:08; Tr. 2423:19-2427:13.) Indeed, Rambus only appears to contest this aspect of claim 2 under its proposed construction of “output frequency,” which has been rejected. (*See* CIB at 239-240.)

(e) Dependent Claims 11-13, 32-34, and 50-52 of the '857 Patent

The ALJ finds that clear and convincing evidence does not show that the SL500 Art anticipates claims 11, 32, and 50. But, the ALJ finds that clear and convincing evidence does show that the additional limitations of these claims would have been obvious in view of the SL500 Art alone or in combination with other art. Specifically, claim 11 requires “at least one additional transmitter circuit within the chip” that is also “coupled to the processor” of claim 1. (See JX-120 at 9:26-32.) According to the Respondents, *** The Respondents further argue that multiple cores were included within a version called “Shemp” that LSI purportedly offered to sell in *** However, even if true, the ALJ finds that the Respondents have to identify a *** Thus, the ALJ finds that the evidence fails to show anticipation for at least this reason.

*102 Nonetheless, the ALJ finds that clear and convincing evidence shows that it would have been obvious to implement the system disclosed in the SL500 Art in a configuration with multiple transmitter circuits coupled to a processor as claimed. Thus, the additional limitations of claim 11 (and claims 32 and 50) would have been obvious variations to one of ordinary skill in the relevant art.

For example, the evidence shows that the SL 500 art was explicitly designed to be scalable. (RX-4130C.0025 *** Accordingly, the SL500 could have been designed to implement multiple CWSL500 transmitters, and it would have been obvious to do so. (See RX-5430C at Q/A 408.) The analogous art strongly suggests that a person of ordinary skill would be motivated to include multiple transmitters. For example, as discussed above the Widmer article teaches a system including multiple transmitters that could be used with an upstream processor. (See Tr. 1542:05-1543:05.) Moreover, Rambus has not contested this limitation. The ALJ finds that the evidence clearly establishes that it would have been obvious to a person of ordinary skill given the SL 500 art to modify the art to have multiple transmitters couple to a single chip. *Perfect Web Tech., Inc. v. InfoUSA, Inc.*, 587 F.3d 1324, 1331 (Fed. Cir. 2008). As discussed below, the “secondary considerations” that Rambus raises are insufficient to overcome the strong case for modifying the SL 500 art. Accordingly, the ALJ finds that clear and convincing evidence shows that it would have been obvious to implement the system disclosed in the SL 500 art in a configuration with multiple transmitter circuits coupled to a common processor, particularly given the explicit disclosure of that the SL 500 art was designed to be scalable.²⁰

(f) Claims 12, 33, and 51 ('857 Patent)

Rambus does not dispute that the SL 500 art discloses the additional limitations of Claims 12, 33, and 51. The only limitation missing is the multiple transmitter limitation of the claims that claims 12, 33, and 51 depend on (namely, claims 11, 32, and 50). For the reasons discussed above with respect to claims 11, 32, and 50, the multiple transmitter limitation would have been obvious to a person of skill in the art. The remaining limitation as shown below:

Dependent Claim Analysis

Dependent Claim	Additional Claim Limitation	CWSL500 Technology Reference
'857 Claim 12, '857 Claim 33, '857 Claim 51	“the chip has I/O connections and the transmitter circuit is coupled to one or more of the I/O connections to send the output signal	The SL500 chip had I/O connections, and the CWSL500's transmitter circuit was coupled to one or more of these I/O connections to

through the one or more I/O connections” (certain claims require a plurality)

send the output signal through the one or more I/O connections. (RX-4130C.0021 (Fig 1.3), RX-4130C.0023 (Fig 1.5); RX-4116C.0006-08; RX-5430C at Q/A 404.) Similar to chips with a single transmitter, multiple transmitter chips were, and would have been, coupled to a plurality of I/O connections and operable to send the output signals through the I/O connections. (*Id.*; see also, e.g., RX-5430C at Q409.)

(g) Dependent Claims 13, 34, and 52 ('857 Patent)

*103 Rambus does not dispute that the SL 500 art discloses the additional limitations of Claims 13, 34, and 52. The only limitation missing is the multiple transmitter limitation of the claims that claims 13, 34, and 52 depend on (namely, claims 11, 32, and 50). For the reasons discussed above with respect to claims 11, 32, and 50, the multiple transmitter limitation would have been obvious to a person of skill in the art. The remaining limitation as shown below:

Dependent Claim Analysis

Dependent Claim	Additional Claim Limitation	CWSL500 Technology Anticipation Reference
'857 Claim 13, '857 Claim 34, '857 Claim 52	“operable to provide output signals representing a parallel stream of data from the processor”	Similar to implementation of a single transmitter, a chip with multiple CWSL500 transmitter circuits was operable to provide output signals representing a parallel stream of data from the processor. (RX-4130C.0020-21 ***; RX-5430C at Q/A 410.) As discussed in relation to claim 1 of the '857 Patent, the CWSL500's transmitter accepts this parallel data and sends a corresponding output

signal. (RX-4130C.0018
***)

(h) Additional Dependent Claims of The '857 Patent

*104 Finally, clear and convincing evidence shows that the LSI art discloses the limitations added by way of the remaining dependent claims. In fact, Rambus does not appear to raise any validity arguments specific to the limitations added by way of these claims. Accordingly, as detailed in the chart below, the ALJ finds those claims invalid as well.

Dependent Claim Anticipation Analysis

Dependent Claim	Additional Claim Limitation	CWSL500 Technology Anticipation Reference
'857 Claim. 4, '857 Claim 26	"operable to emphasize signal levels representing values following transitions between values relative to signal levels representing repeated values"	The CWSL500 simulations show that when two consecutive digital input bits are the same, the output signal from the CWSL500 transmitter has one level. (Simulation Waveforms.) When two consecutive digital input bits are different, the output signal from the CWSL500 transmitter has another level. (RX-5430C at Q/A 403,)
'857 Claim 5, '857 Claim 27, '857 Claim 43	"the chip has I/O connections and the transmitter circuit is coupled to one or more of the I/O connections to send the output signal through the one or more I/O connections" (certain claims require a plurality)	The SL500 chip had I/O connections, and the CWSL500's transmitter circuit was coupled to one or more of these I/O connections to send the output signal through the one or more I/O connections. (RX-4130C.0021 (Fig 1.3), RX-4130C.0023 (Fig 1.5); RX-4116C.0006-08; RX-5430C at Q/A 404.) Similar to chips with a single transmitter, multiple transmitter chips were,

and would have been, coupled to a plurality of I/O connections and operable to send the output signals through the I/O connections. (RX-5430C at Q/A 404; RX-5430C at Q409.)

'857 Claim 6, '857 Claim 28, '857 Claim 44

“operable to send the output signal in nonmodulated form”

If the CWSL500 were to send modulated signals, a modulator block would have been included in RX-4116C at Fig. 2 (RX-4116C.0006). The CWSL500's transmitter block diagram does not include a modulator block, nor does it receive a carrier wave, which would be necessary for modulation of the output signal. (RX-5430C at Q/A 405.) Therefore, the signal is sent in nonmodulated form. (RX-5430C at Q/A 405.)

'857 Claim 9, '857 Claim 47

“(each digital value/each bit value in the digital input signal) is represented by one of the signal levels in the output signal”

The CWSL500 simulation waveforms wherein each digital value is represented by one of the signal levels of the output signal. RX-4092C (RDX-350); RDX-347; RX-4094C (hereinafter collectively referred to as “Simulation Waveforms”); RX-5430C at Q/A 406.)

'857 Claim 10

“the digital input signal includes a plurality of bits and each bit of the digital input signal is represented by one of the signal levels in the output signal”

The CWSL500's transmitter accepted a digital input signal, which included a plurality of bits. (RX-4130C.0018, Fig. 1.2.) The CWSL500 simulation waveforms show that each bit of the digital input bit is represented by one of the signal levels in the

		output signal. (Simulation waveforms.; RX-5430C at Q/A 407.)
'857 Claim 25, '857 Claim 36, '857 Claim 40	"wherein the component circuit is a processor"	As discussed in relation to claim 1 of the '857 Patent, the CWSL500 technology discloses a component circuit, <i>i.e.</i> , an *** that was a processor. (<i>See also, e.g.</i> , RX-5430C at Q/A 420.)
'857 Claim 41	"operable to select each signal level as a function of the bit value represented by that signal level and of the bit values represented by one or more preceding signal levels"	The CWSL500 simulations show that when two consecutive digital input bits are the same, the output signal from the CWSL500 transmitter has one level, and when two consecutive digital input bits are different, the output signal from the CWSL500 transmitter has another level. (Simulation Waveforms; <i>see also, e.g.</i> , RX-5430C at Q/A 445.)
'857 Claim 42	"operable to select each signal level as a function of the bit value represented by that signal level and the bit value represented by the immediately preceding signal level"	The CWSL500 simulations show that when two consecutive digital input bits are the same, the output signal from the CWSL500 transmitter has one level, and when two consecutive digital input bits are different, the output signal from the CWSL500 transmitter has another level. (Simulation Waveforms; <i>see also, e.g.</i> , RX-5430C at Q/A 446.)
'857 Claim 53	"operable to select each signal level as a function of only the bit value represented by that signal level and the bit value represented by the	

immediately preceding
signal level”

(3) Invalidity Of U.S. Patent No. 7,715,494 Over The SL500 Art

***105** The ALJ finds that clear and convincing evidence shows that the SL500 art anticipates claims 1, 2, 3, 6, 8, 25, 30, 39, and 42 of the '494 patent and renders obvious claims 26 and 40 for similar reasons to those discussed above with respect to the '857 patent. Indeed, Rambus does not appear to raise any validity arguments specific to the '494 patent claims. (See CPB at 404-406.)

(a) Independent Claim 1 of the '494 Patent:

Claim 1 of the '494 Patent is an independent claim that is disclosed by the CWSL500 technology. (See RX-5430C at Q/A 455-462.) As discussed in relation to claim 1 of the '857 Patent, the CWSL500 technology discloses “a circuit comprising a semiconductor chip” and “a transmitter circuit within the chip.” The ALJ finds that the CWSL500 technology also discloses a “transmitter circuit being operable to accept a digital input signal including a plurality of bits.” In particular, the CWSL500's transmitter circuit is coupled to a component circuit ***, such transmitter accepts a digital input signal including a plurality of bits. (RX-4130C.0018, 20.)

The CWSL500 technology also discloses a transmitter circuit that is operable to “send an output signal including a series of output bit signals.” (See RX-4130C.0018.) The CWSL500 simulation waveforms further show “each bit of the digital input signal being represented by a single output bit signal.” (See Simulation Waveforms.) The simulation waveforms also show that the CWSL500's transmitter circuit generated a sign which depended upon the value of the bit represented by such output bit signal and generating a magnitude which is a function of the value of the bit represented by such output bit signal and the values of the bits represented by one or more preceding output bit signals, each output bit signal having sign and magnitude determined by the generated sign and generated magnitude. (Simulation Waveforms.)

(b) Independent Claims 25 and 39 of the '494 Patent:

Claim 25 of the '494 Patent is an independent claim that is similar in scope to claim 1 of the '494 Patent except that claim 25 requires the transmitter's output signal to be a differential signal and also describes the emphasis functionality in a slightly different manner. Notwithstanding, the ALJ finds that claim 25 of the '494 Patent is disclosed by the CWSL500 technology for many of the same reasons cited above in relation to claim 1 of the '494 Patent. (See RX-5430C at Q/A 467-474, 477-483.) Additionally, the CWSL500 technology discloses a transmitter circuit with a differential output signal. (RX-4130C.0018 *** The ALJ finds that CWSL500 simulation waveforms also show that the CWSL500's transmitter circuit drives the series of output bit signals to have sign an represented by logic level of a first bit that is to be transmitted, and magnitude represented by whether the first bit represents a common logic level relative to an immediately previous bit, the magnitude being driven to be relatively smaller when the first bit has a common logic level with the immediately previous bit, and to be relatively larger when the first bit does not have the common logic level. (Simulation Waveforms; RX-5430C at Q/A 474.)

***106** Claim 39 of the '494 Patent is a method claim that is otherwise equivalent to claim 25 of the '494 Patent. Accordingly, the CWSL500 technology discloses the limitations of claim 39 of the '494 Patent for at least the same reasons cited above in relation to claim 25 of the '494 Patent. (See RX-5430C at Q/A 477-483.)

As is shown above, the implementation of the CWSL500 technology in semiconductor chips anticipated each and every limitation of the Asserted Claims of the Dally Patents. (See also RX-5430C.0213-294.) Rambus has not provided any credible evidence to the contrary.

(c) Dependent Claims 26 and 40 of The '494 Patent

The ALJ finds that clear and convincing evidence does show that the SL500 Art anticipates claims 26 and 40. In addition, the ALJ finds that clear and convincing evidence also shows that the additional limitations of these claims would have been obvious in view of the SL500 Art alone or in combination with other art. Specifically, claims 26 and 40 requires that the chip “include [] plural of said transmitter circuits.” Unlike claims 11, 32, and 50, there is no requirement that the multiple transmitter circuits be also “coupled to the processor” (as discussed *supra* at 152-154). Thus, the ALJ finds that respondents are correct that the evidence shows that the core of the SL500 was designed to be scalable and thus “can include at least one additional transmitter circuit within the chip.” (See RX-5430C at Q/A 408.) The Respondents further argue that multiple cores were included within a version called “Shemp” that LSI purportedly offered to sell in *** Thus, the ALJ finds that the evidence show anticipation for at least this reason.

Moreover, the ALJ finds that even if this disclosure is lacking clear and convincing evidence shows that it would have been obvious to implement the system disclosed in the SL500 Art in a configuration with multiple transmitter circuits as claimed. Thus, the additional limitations of claim 26 and 40 would have been obvious variations to one of ordinary skill in the relevant art.

For example, the evidence shows that the SL 500 art was explicitly designed to be scalable. (RX-4130C.0025 *** Accordingly, the SL500 could have been designed to implement multiple CWSL500 transmitters, and it would have been obvious to do so. (See RX-5430C at Q/A 408.) The analogous art strongly suggests that a person of ordinary skill would be motivated to include multiple transmitters. For example, as discussed above the Widmer article teaches a system including multiple transmitters. (See Tr. 1542:05-1543:05.) Moreover, Rambus has not contested this limitation. The ALJ finds that the evidence clearly establishes that it would have been obvious to a person of ordinary skill given the SL 500 art to modify the art to have multiple transmitters couple to a single chip. *Perfect Web Tech., Inc. v. INfoUSA, Inc.*, 587 F.3d 1324, 1331 (Fed. Cir. 2008). As discussed below, the “secondary considerations” that Rambus raises are insufficient to overcome the strong case for modifying the SL 500 art. Accordingly, the ALJ finds that clear and convincing evidence shows that it would have been obvious to implement the system disclosed in the SL 500 art in a configuration with multiple transmitter circuits, particularly given the explicit disclosure of that the SL 500 art was designed to be scalable.

(d) Other Dependent Claims

*107 Rambus does not raise any other arguments with respect to the other dependent claims. Accordingly, the ALJ finds that Respondents have shown by clear and convincing evidence that they are anticipated. The evidence with respect to each of the remaining independent claims is listed in the chart below:

Dependent Claim Anticipation Analysis

Dependent Claim	Additional Claim Limitation	CWSL500 Technology Anticipation Reference
'494 Claim 3	“operable to (send/ provide) the output signal with an output frequency of at least 1 GHz and a bandwidth greater than 100 MHz”	Under Respondents' construction of the term “output frequency”, the CWSL500 technology satisfies this limitation. ²¹ (RX-4130.0021 ***; RX-4130.0024 ***; RX-5430C at Q/A 402.)

'494 Claim 30, '494 Claim 42

“the series of output signals is transmitted by the transmitter onto a signal path at a rate of at least 400 megahertz”

'494 Claim 2

“the function is such that an output bit signal is representing a bit having a value different from the value of the bits represented in the one or more preceding output bit signals has a greater magnitude than an output bit signal representing a bit having the same value as the bits represented by the one or more preceding output bit signals”

The CWSL500 simulations show that the CWSL500's transmitter performed the emphasis function such that an output bit signal representing a bit having a value different from the value of the bits represented in the one or more preceding output bit signals had a greater magnitude than an output bit signal representing a bit having the same value as the bits represented by the one or more preceding output bit signals. (Simulation Waveforms; RX-5430C at Q/A 463.)

'494 Claim 6

“operable to select the magnitude of each output bit signal based only on the value of the bit represented by that output bit signal and the value of the bit represented by the immediately preceding output bit signal”

The CWSL500 simulations show that the CWSL500's transmitter circuit was operable to select the magnitude of each output bit signal based only on the value of the bit represented by that output bit signal and the value of the bit represented by the immediately preceding output bit signal. (Simulation Waveforms; RX-5430C at Q/A 465.)

'494 Claim 8

“wherein the function is reprogrammable”

The CWSL500's transmitter was operable such that the relationship between the strength of the output bit signals and the number of bits since the last transition (0 or 1) is reprogrammable. (RX-4116C.0004 *** RX-4116C.0010 (Fig. 4);

RX-4116C.0060, 62, 72
and 80; RX-5430C at Q/A
66.)

C. Obviousness

***108** Included within the presumption of validity is a presumption of non-obviousness. *Structural Rubber Prods. Co. v. Park Rubber Co.*, 749 F.2d 707, 714 (Fed. Cir. 1984). Obviousness is grounded in 35 U.S.C. § 103, which provide, *inter alia*, that:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negative by the manner in which the invention was made.

35 U.S.C. § 103(a). Under 35 U.S.C. § 103(a), a patent is valid unless “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” 35 U.S.C. § 103(a). The ultimate question of obviousness is a question of law, but “it is well understood that there are factual issues underlying the ultimate obviousness decision.” *Richardson-Vicks Inc.*, 122 F.3d at 1479; *Wang Lab., Inc. v. Toshiba Corp.*, 993 F.2d 858, 863 (Fed. Cir. 1993).

Once claims have been properly construed, “[t]he second step in an obviousness inquiry is to determine whether the claimed invention would have been obvious as a legal matter, based on underlying factual inquiries including: (1) the scope and content of the prior art, (2) the level of ordinary skill in the art, (3) the differences between the claimed invention and the prior art; and (4) secondary considerations of non-obviousness” (also known as “objective evidence”). *Smiths Indus. Med. Sys., Inc. v. Vital Signs, Inc.*, 183 F.3d 1347, 1354 (Fed. Cir. 1999), citing *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). The ultimate determination of whether an invention would have been obvious is a legal conclusion based on underlying findings of fact. *In re Dembiczak*, 175 F.3d 994, 998 (Fed. Cir. 1999).

Obviousness may be based on any of the alleged prior art references or a combination of the same, and what a person of ordinary skill in the art would understand based on his knowledge and said references. If all of the elements of an invention are found, then:

a proper analysis under § 103 requires, *inter alia*, consideration of two factors: (1) whether the prior art would have suggested to those of ordinary skill in the art that they should make the claimed composition or device, or carry out the claimed process; and (2) whether the prior art would also have revealed that in so making or carrying out, those of ordinary skill would have a reasonable expectation of success. *Both the suggestion and the reasonable expectation of success must be founded in the prior art, not in the applicant's disclosure.*

***109** *Velander v. Garner*, 348 F.3d 1359, 1363 (Fed. Cir. 2003) (emphasis added) (internal citations omitted).

The critical inquiry in determining the differences between the claimed invention and the prior art is whether there is a reason to combine the prior art references. See *C.R. Bard v. M3 Sys.*, 157 F.3d 1340, 1352 (Fed. Cir. 1998). For example:

[A] patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art. Although common sense directs one to look with care at a patent application that claims as innovation the combination of two known devices according to their established functions, it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does. This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known.

KSR Int'l Co. v. Teleflex, Inc., 550 U.S. 398, 418-19 (2007) (emphasis added). The Federal Circuit case law previously required that, in order to prove obviousness, the patent challenger must demonstrate, by clear and convincing evidence, that there is a “teaching, suggestion, or motivation to combine. The Supreme Court has rejected this “rigid approach” employed by the Federal Circuit in *KSR Int'l Co. v. Teleflex Inc.*, 500 U.S. 398 (2007), 127 S.Ct. 1727, 1739. The Supreme Court stated:

When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. *Sakraida* and *Anderson's-Black Rock* are illustrative--a court must ask whether the improvement is more than the predictable use of prior art elements according to their established function.

Following these principles may be more difficult in other cases than it is here because the claimed subject matter may involve more than the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for the improvement. Often, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue. To facilitate review, this analysis should be made explicitly. See *In re Kahn*, 441 F.3d 977, 988 (CA Fed. 2006) (“[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusions of obviousness”). As our precedents make clear, however, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.

[...]

***110** The obviousness analysis cannot be confined by a formalistic conception of the words teaching, suggestion, and motivation, or by overemphasis on the importance of published articles and the explicit content of issued patents. The diversity of inventive pursuits and of modern technology counsels against limiting the analysis in this way. In many fields it may be that there is little discussion of obvious techniques or combinations, and it often may be the case that market demand, rather than scientific literature, will drive design trends. Granting patent protection to advance that would occur in the ordinary course without real innovation retards progress and may, in the case of patents combining previously known elements, deprive prior inventions of their value or utility.

KSR, 550 U.S. at 417-419; 127 S.Ct. at 1740-41. The Federal Circuit has harmonized the *KSR* opinion with many prior circuit court opinions by holding that when a patent challenger contends that a patent is invalid for obviousness based on a combination of prior art references, “the burden falls on the patent challenger to show by clear and convincing evidence that a person of ordinary skill in the art would have had reason to attempt to make the composition or device, or carry out the claimed process, and would have had a reasonable expectation of success in doing so. *PharmaStem Therapeutics, Inc. v. ViaCell, Inc.*, 491 F.3d 1342, 1360 (Fed. Cir. 2007)(citing *Medichem S.A. v. Rolabo S.L.*, 437 F.3d 1175, 1164 (Fed. Cir. 2006)); *Noelle v. Lederman*,