
From: kprall
Sent: Wednesday, November 28, 2007 10:43 AM
To: lctran; gsandhu
Subject: FW: BeSang - 1Gb Flash Design
Attachments: 7_Endoh_TohokuUniv.pdf

From: Sang-Yun Lee [mailto:sangyun.lee@besang.com]
Sent: Monday, November 26, 2007 6:01 AM
To: tjarnold; jpawlowski; jerryjohnson; ahill; pfeeley; spking; froohparvar; kprall; sdeboer; iblasch
Subject: RE: BeSang - 1Gb Flash Design

According to Prof. Endoh, who invented stacked SGT (S-SGT) flash memory, the S-SGT has NAND flash type. Please check the attached presentation slides for more information about S-SGT.

Best regards,
Sang-Yun Lee
CEO at BeSang Inc.

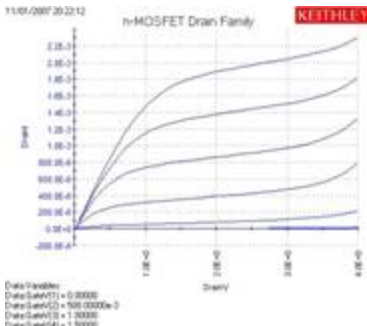
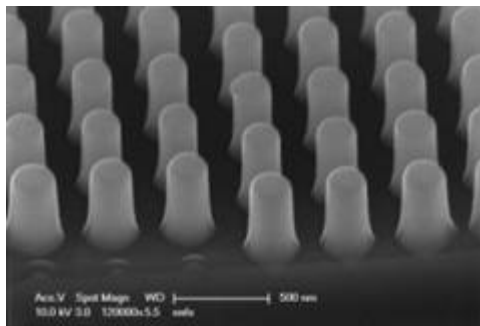
From: Sang-Yun Lee [mailto:sangyun.lee@besang.com]
Sent: Thursday, November 08, 2007 9:00 PM
To: 'tjarnold@micron.com'; 'jpawlowski@micron.com'; 'jerryjohnson@micron.com'; 'ahill@micron.com'; 'pfeeley@micron.com'; 'spking@micron.com'; 'froohparvar@micron.com'; 'kprall@micron.com'; 'sdeboer@micron.com'; 'iblasch@micron.com'
Subject: BeSang - 1Gb Flash Design

Dear Micron Technology

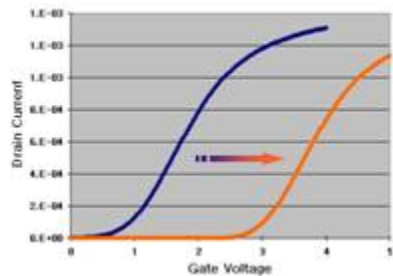
I would like to give you brief update of BeSang's progress.

BeSang successfully generated vertical flash devices at 0.18um design rule. Please find attached pictures for your information.

At this moment, BeSang engineering team is designing 1Gb flash with 0.18um design, which will have 25 mm square chip size. In case 90nm design rule is used, 16Gb flash with 99 mm square could be generated. 1Gb design will be specified at 3D Workshop in Stanford University on Nov. 20 (<http://nanodevice.stanford.edu/3dworkshop.html>). BeSang and Tokyo Electron co-sponsor this event.



Flash Program-Erase



I appreciate your interest in BeSang.

With My best regards,

Sang-Yun Lee
CEO at BeSang Inc.
Ph) 503-502-3366

ATTACHMENT A

Impact of 3D structured devices

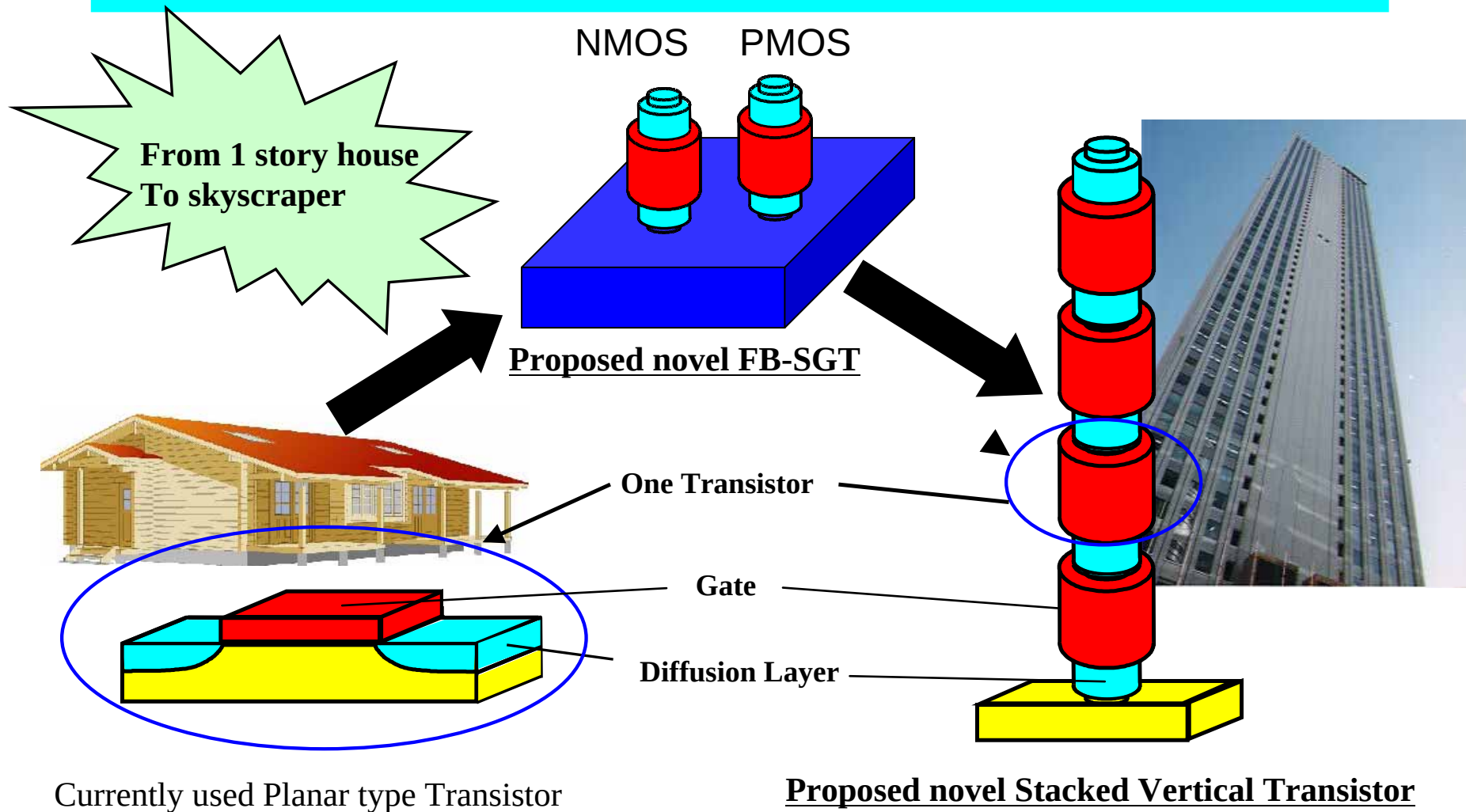
- High performance logic & high density memory -

Tetsuo Endoh

Research Institute of Electrical Communication

Tohoku University

Vertical MOSFET and Stacked Vertical MOSFET



Technology Trend of Bulk-MOSFETs from ITRS

Table 47a High-performance Logic Technology Requirements—Near-term

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node	lp90			lp65			
DRAM 1/2 Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) 1/2 Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC 1/2 Pitch (nm)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm)	65	59	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Physical gate length high-performance (HP) (nm) [1]	45	37	32	28	25	22	20
EOT: equivalent oxide thickness (physical) for high-performance (nm) [2]	1.3	1.2	1.1	1.0	0.9	0.8	0.8
Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.8	0.8	0.7	0.7	0.4	0.4	0.4
Equivalent electrical oxide thickness in inversion (nm) [4]	2.1	2.0	1.8	1.7	1.3	1.2	1.2
Nominal gate leakage current density limit (at 25°C) (A/cm^2) [5]	2.2E+02	4.5E+02	5.2E+02	6.0E+02	9.3E+02	1.1E+03	1.2E+03
Nominal power supply voltage (V_{DD}) (V) [6]	1.2	1.2	1.1	1.1	1.1	1.0	1.0
Saturation threshold voltage (V_T) [7]	0.21	0.20	0.20	0.21	0.18	0.17	0.16
Nominal high-performance NMOS sub-threshold leakage current, $I_{off,sub}$ (at 25°C) ($\mu A/\mu m$) [8]	0.03	0.05	0.05	0.05	0.07	0.07	0.07
Nominal high-performance NMOS saturation drive current, $I_{on,sat}$ (at V_{DD} at 25°C) (mA/mm) [9]	980	1110	1090	1170	1510	1530	1990
Required "mobility/transconductance improvement" factor [10]	1.0	1.3	1.3	1.4	2.0	2.0	2.0
Sub-threshold slope adjustment factor (full depletion/multiple-gate effects) ($\theta-1$) [11]	1.0	1.0	1.0	1.0	1.0	0.8	0.7
Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Parasitic source/drain series resistance (R_{sd}) (Ohm- μm) [13]	180	180	180	171	162	153	144
Ideal NMOS device gate capacitance ($F/\mu m$) [14]	7.40E-16	6.39E-16	6.14E-16	5.60E-16	6.64E-16	6.33E-16	5.76E-16
Parasitic fringe/overlap capacitance ($F/\mu m$) [15]	2.40E-16	2.40E-16	2.40E-16	2.30E-16	2.20E-16	2.00E-16	1.90E-16
High-performance NMOS intrinsic delay, $\tau = C_{gate} * V_{DD} / I_{on,sat}$ (ps) [16]	1.20	0.95	0.86	0.75	0.64	0.54	0.48
Relative NMOS intrinsic switching speed, 1/ τ , normalized to 2003 [17]	1.00	1.26	1.39	1.60	1.86	2.20	2.49
Nominal logic gate delay (NAND gate) (ps) [18]	30.26	23.94	21.72	18.92	16.23	13.72	12.13
NMOSFET power-delay product ($fJ/\mu m$) [19]	1.41E-15	1.27E-15	1.03E-15	9.66E-16	1.07E-15	8.33E-16	7.60E-16
NMOSFET static power dissipation due to drain and gate leakage ($W/\mu m$) [20]	3.96E-07	6.80E-07	6.05E-07	6.05E-07	8.47E-07	7.70E-07	7.70E-07

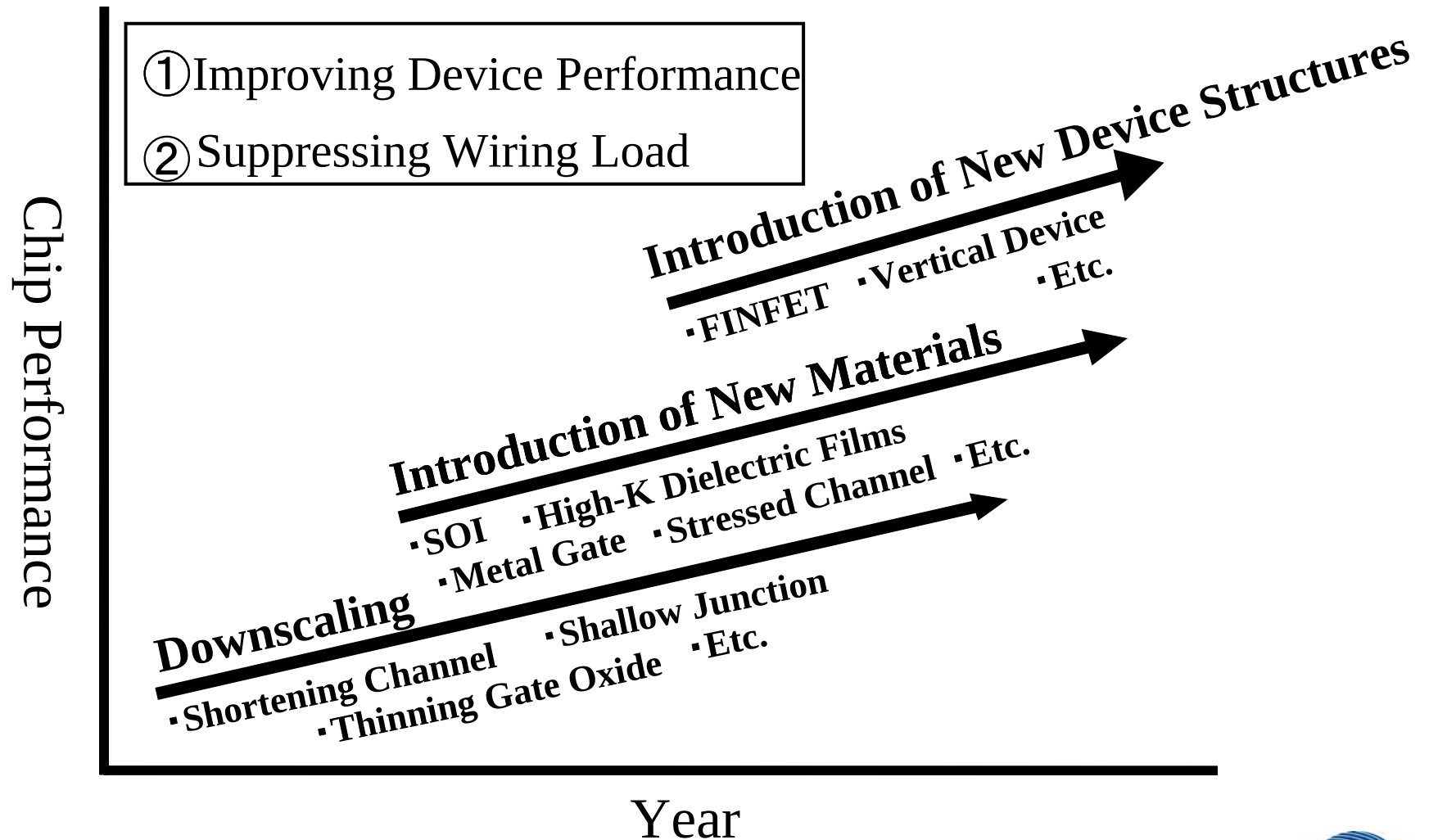
Table 48a Low Operating Power (LOP) Logic Technology Requirements—Near-term

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node	lp90			lp65			
DRAM 1/2 Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) 1/2 Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC 1/2 Pitch (nm)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm)	65	59	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Physical gate length low operating power (LOP) (nm) [1]	65	59	45	37	32	28	25
EOT: equivalent oxide thickness (physical) for LOP (nm) [2]	1.6	1.5	1.4	1.3	1.2	1.1	1.0
Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.8	0.8	0.7	0.7	0.7	0.4	0.4
Equivalent electrical oxide thickness in inversion (nm) [4]	2.4	2.3	2.1	2.0	1.9	1.6	1.4
Nominal gate leakage current density limit (at 25°C) (A/cm^2) [5]	0.61	1.89	2.22	2.70	5.31	6.96	6.67
Nominal LOP power supply voltage (V_{DD}) (V) [6]	1.0	0.9	0.9	0.9	0.8	0.8	0.8
Saturation threshold voltage (V_T) [7]	0.31	0.26	0.27	0.28	0.26	0.25	0.25
Nominal LOP NMOS sub-threshold leakage current, $I_{off,sub}$ (at 25°C) ($\mu A/\mu m$) [8]	1.0E-03	3.0E-03	3.0E-03	3.0E-03	5.0E-03	5.0E-03	5.0E-03
Nominal LOP NMOS saturation drive current, $I_{on,sat}$ (at V_{DD} at 25°C) ($\mu A/\mu m$) [9]	520	530	580	610	570	730	770
Required "mobility/transconductance improvement" factor [10]	1.0	1.0	1.0	1.0	1.0	1.3	1.3
Sub-threshold slope adjustment factor (full depletion/multiple-gate effects) ($\theta-1$) [11]	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Parasitic source/drain series resistance (R_{sd}) (Ohm- μm) [13]	180	180	180	180	180	180	180
Ideal NMOS device gate capacitance ($F/\mu m$) [14]	9.35E-16	7.96E-16	7.40E-16	6.39E-16	6.82E-16	6.48E-16	6.17E-16
Parasitic fringe/overlap capacitance ($F/\mu m$) [15]	2.40E-16	2.40E-16	2.40E-16	2.40E-16	2.40E-16	2.40E-16	2.40E-16
LOP NMOS intrinsic delay, $\tau = C_{gate} * V_{DD} / I_{on,sat}$ (ps) [16]	2.26	1.76	1.52	1.30	1.15	0.97	0.89
Relative NMOS intrinsic switching speed, 1/ τ , normalized to 2003 [17]	1.00	1.29	1.49	1.74	1.96	2.33	2.64
Nominal logic gate delay (NAND gate) (ps) [18]	57.0	44.3	38.3	32.7	29.1	24.4	22.4
NMOSFET power-delay product ($fJ/\mu m$) [19]	1.18E-15	8.39E-16	7.34E-16	7.12E-16	5.20E-16	5.68E-16	5.48E-16
NMOSFET static power dissipation due to drain and gate leakage ($W/\mu m$) [20]	2.8E-09	5.4E-09	5.4E-09	5.4E-09	8.0E-09	8.0E-09	8.0E-09

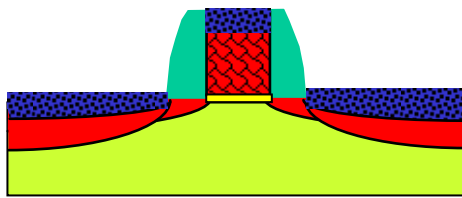
- ① Physical Gate length
 - ② Equivalent electrical oxide thickness in inversion
 - ③ Parasitic source/drain series resistance
 - ④ Normal saturation drive current
 - ⑤ delay (switching speed, logic gate delay)
- } Increase Device Performance
(Increase Drivability)

 } Suppress Wiring Load Capacitance

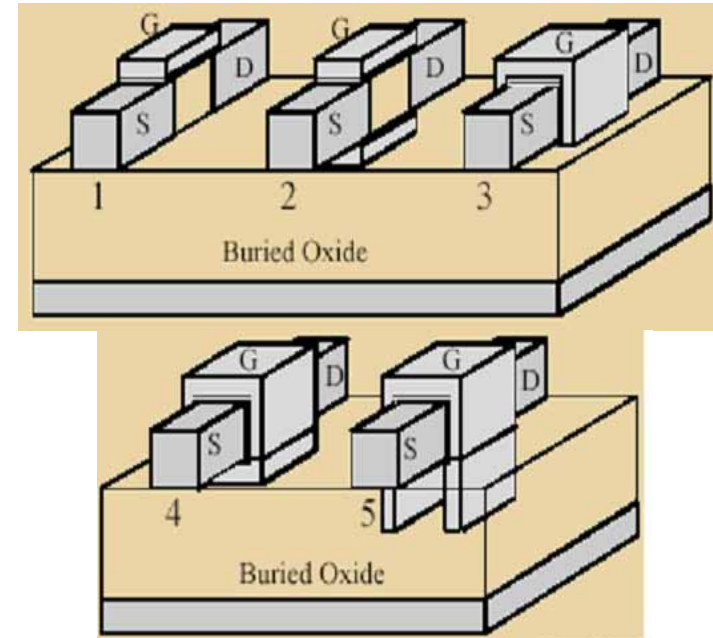
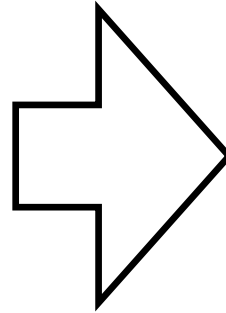
Technology Trend for Improving Chip Performance



Trend of Post-planar MOS Device Structures



Single Gate & Connected Body type Device



Multi-Gate & Floating Body type planar MOSFET

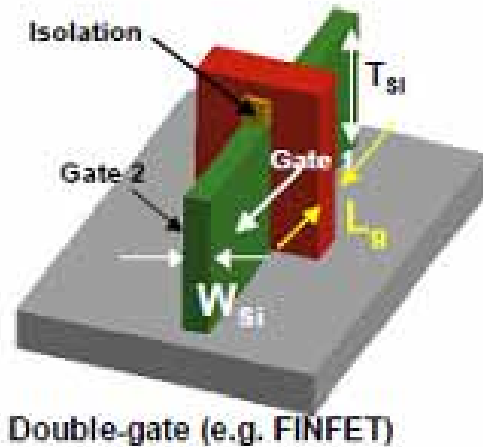
- ① Floating Body Structure.
- ② Multiple Gate Structure



Suppress Short Channel Effects & Increase Drivability
→ Improvement of Device Performance

Impact of Vertical MOSFET for High Performance Logic

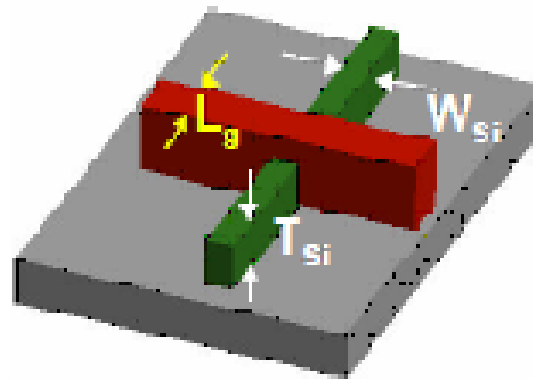
New Device Structure (Multi-gate & Floating Body Structure)



Double-gate (e.g. FINFET)

FINFET

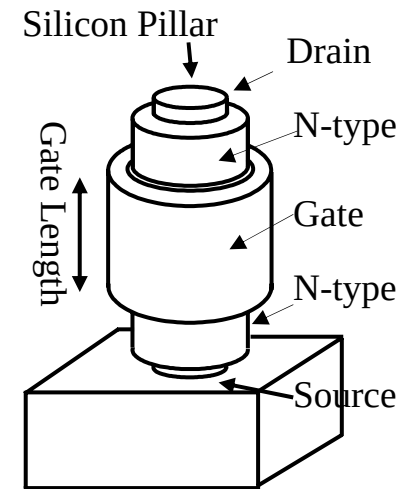
Gate Control from 2 Directions



Tri-gate D&T

Tri-Gate

Gate Control from 3 Directions



Floating Body SGT

Gate Control from 4 Directions

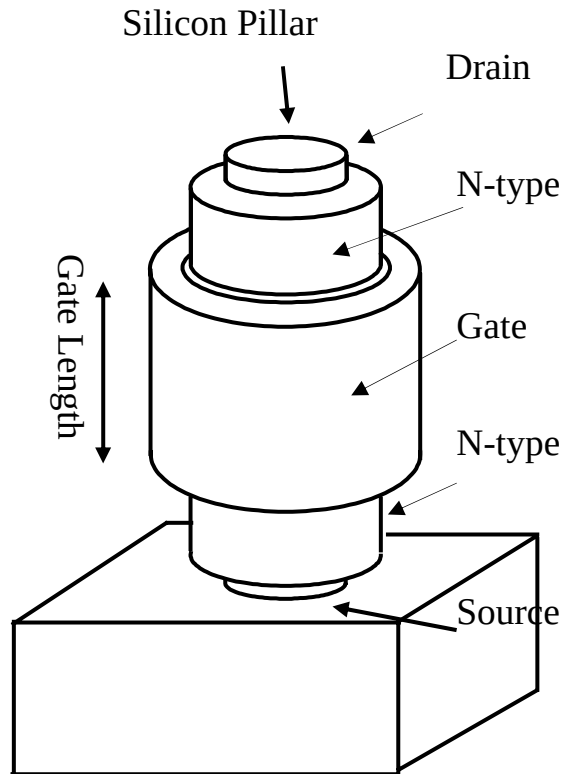
Multi-Gate & Floating Body type

Planar-type MOSFET

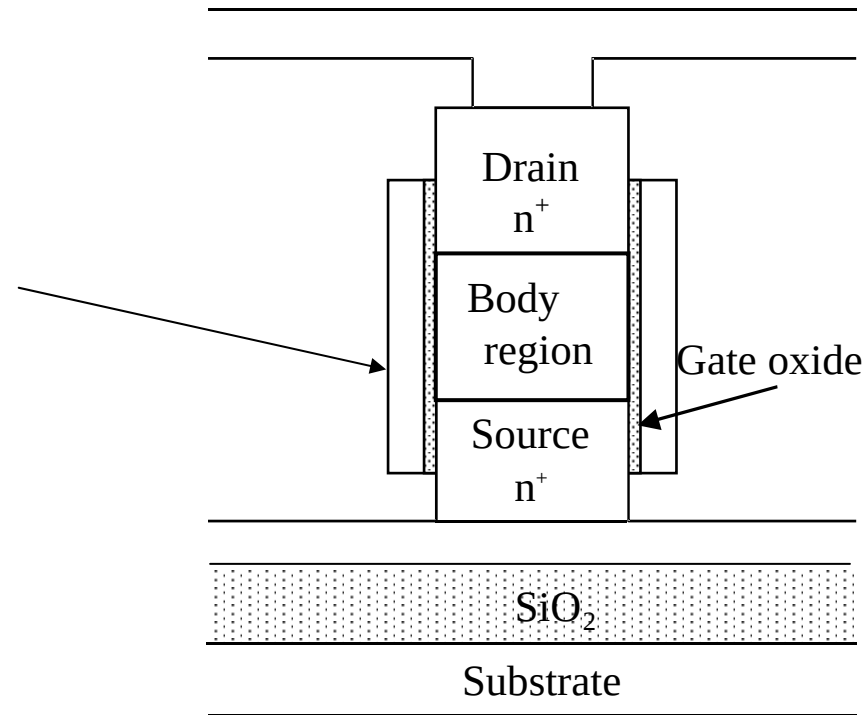
Multi-Gate & Floating Body type

Vertical MOSFET

Vertical MOSFET(Floating Body type SGT)Structure



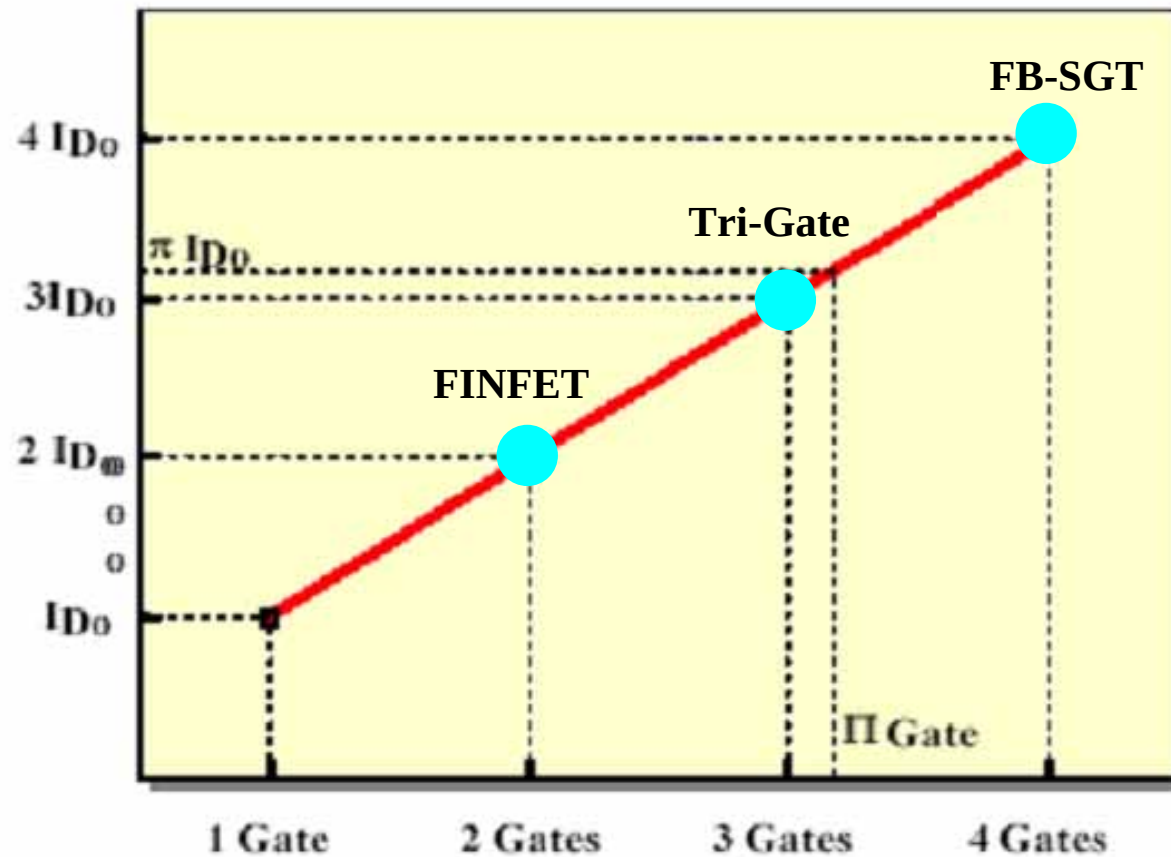
(a) Bird-Eye View



(b) Cross Sectional View

T. Endoh et.al. IEICE TRANSACTIONS ON ELECTRONICS, Vol. E80-C, No.7, pp. 911-917, July, 1997.

Simulation of Multiple-Gate SOI MOSFETs



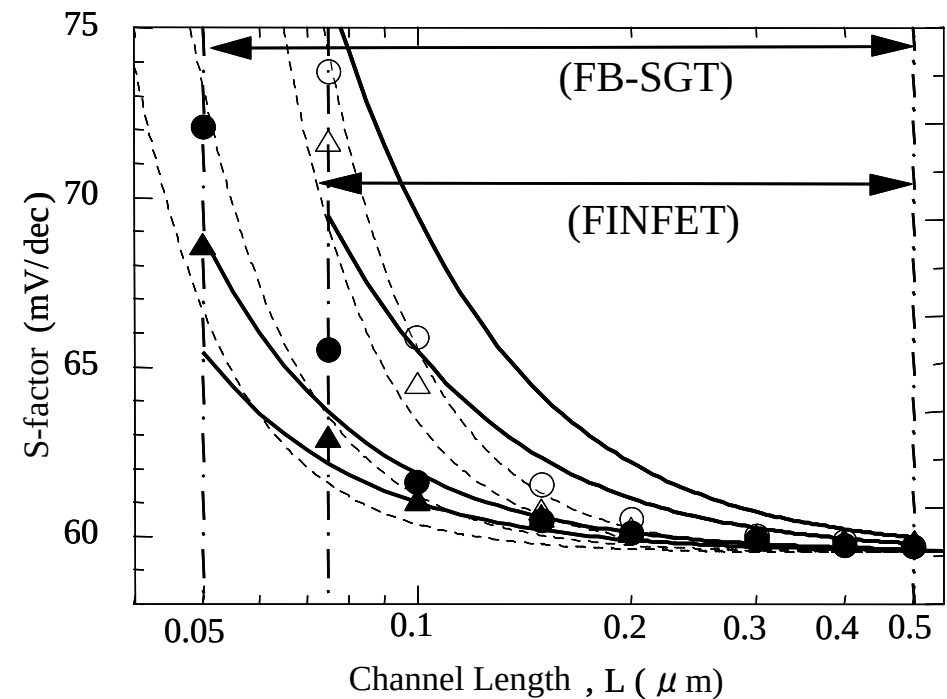
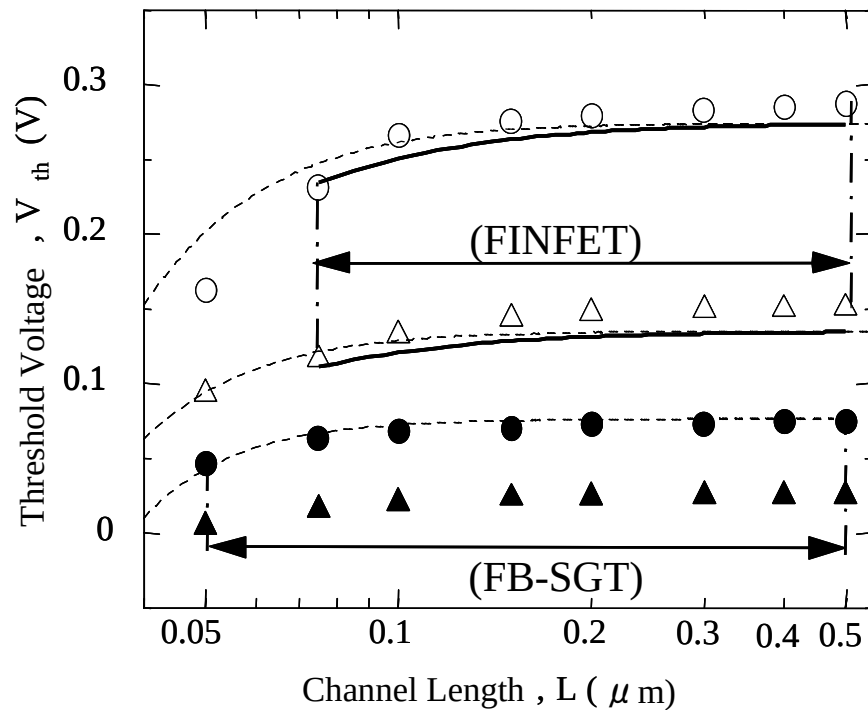
J-P Colinge, U.California., Davis

Mar 25, 2003

2003 International Conference on Characterization and Metrology for ULSI Technology

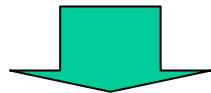
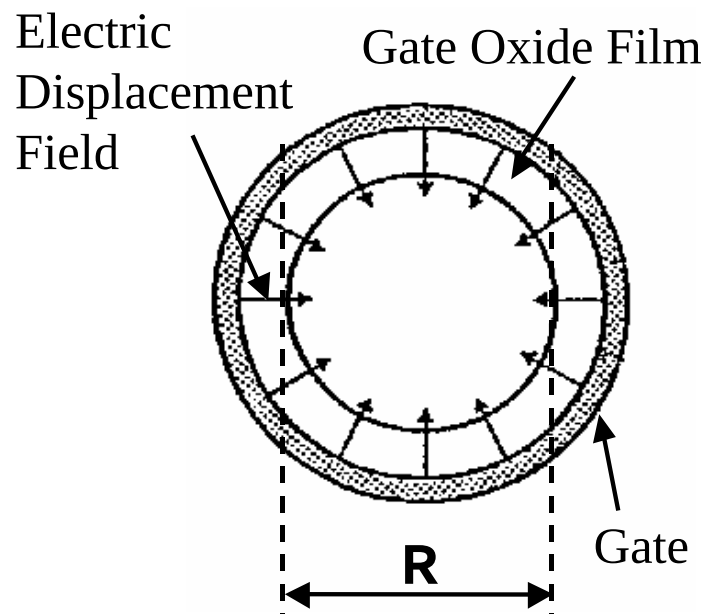
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48

Suppression of SCE due to Vertical MOSFET (FB-SGT vs FINFET)

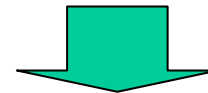
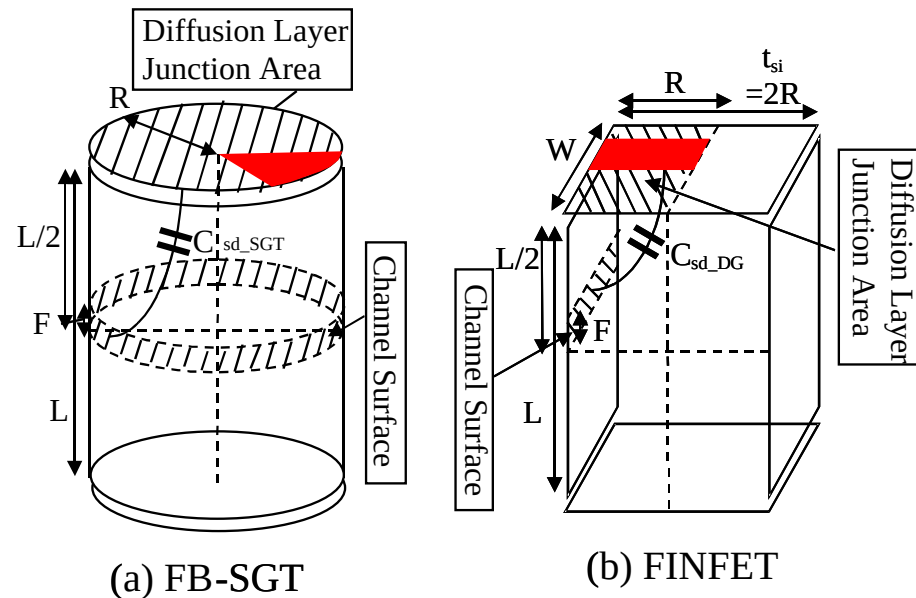


FB-SGT suppresses SCEs more than FINFET.

Principle of the Suppression of SCE in FB-SGT



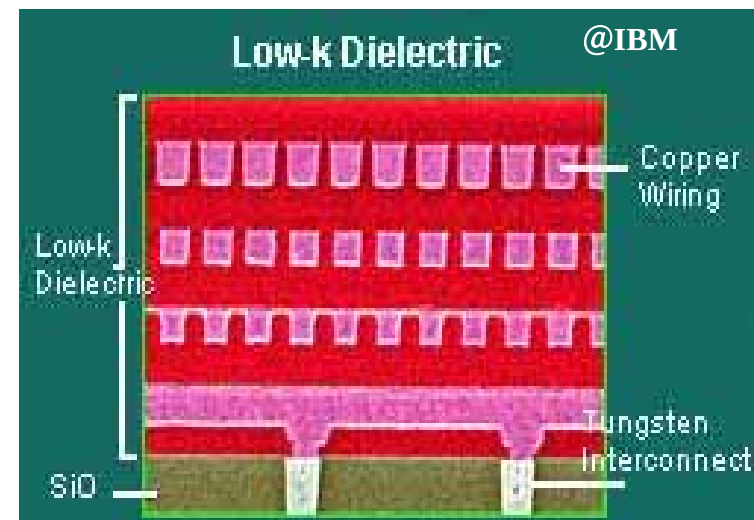
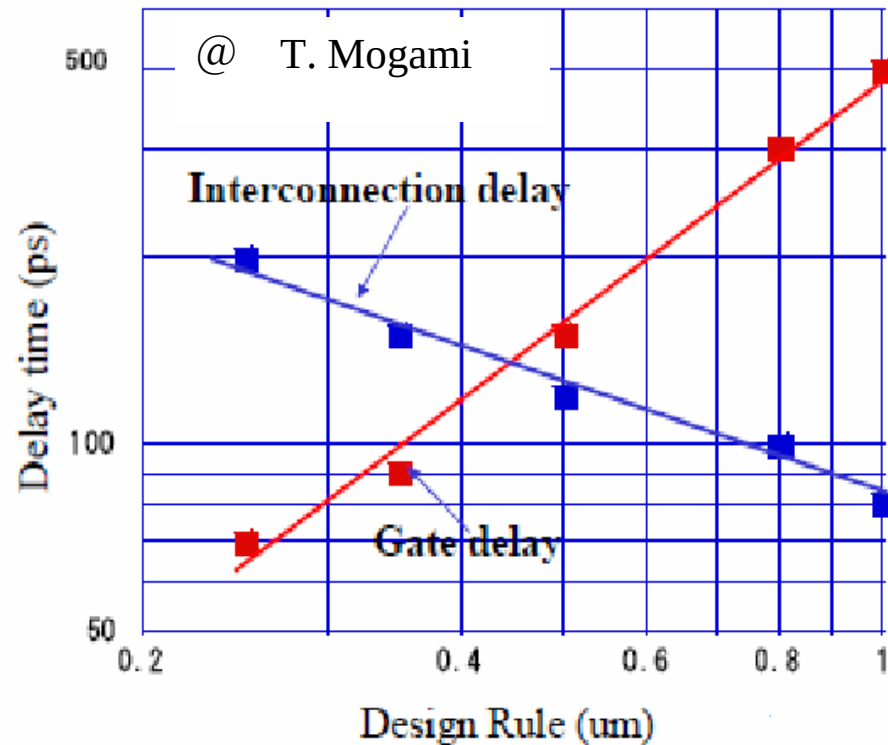
Increase of gate controllability due to Electric Field Enhancement Effect



Diffusion layer capacitance per unit channel length decreases due to the device structure.

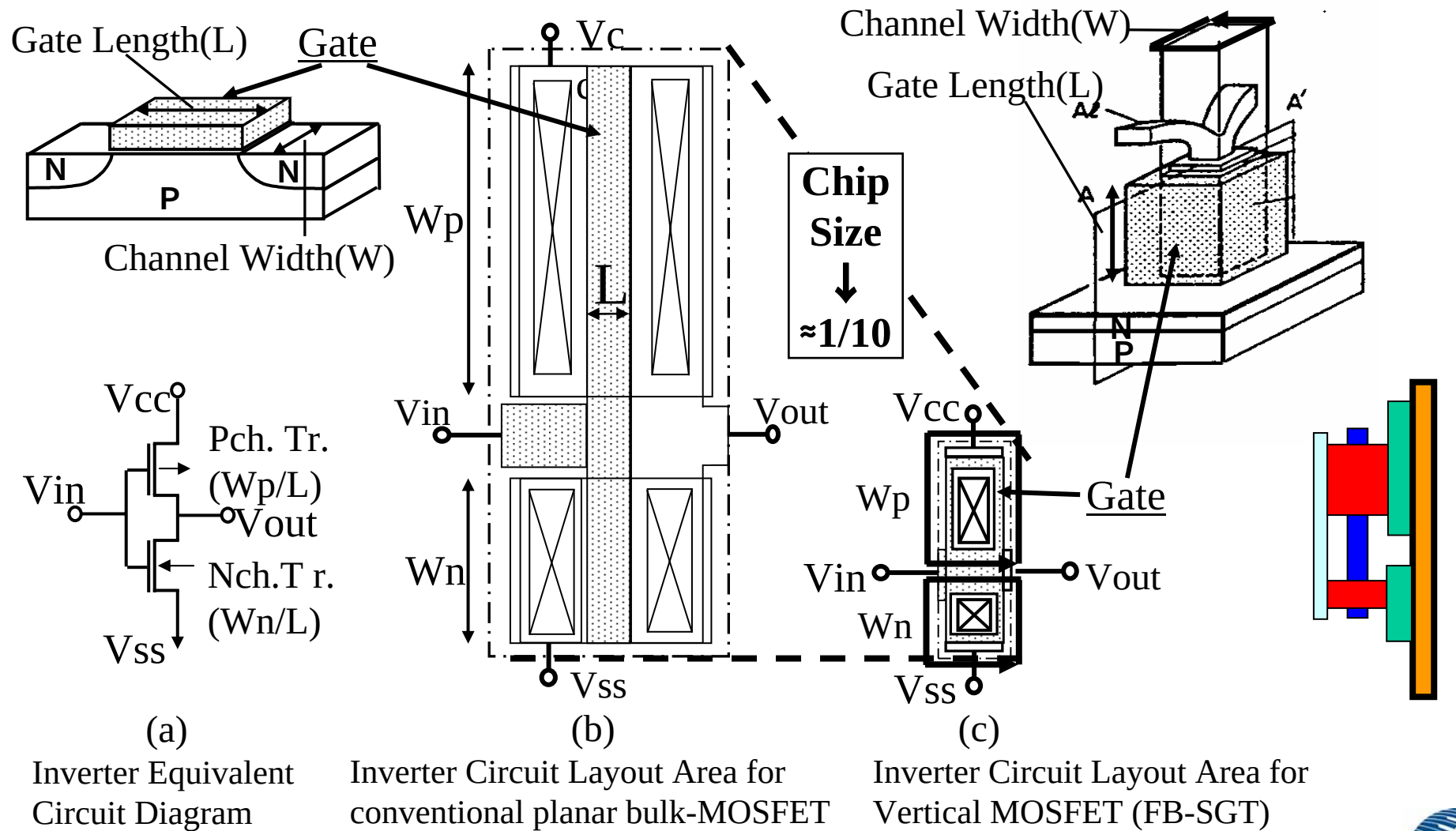
Backend Problems

(Low-K insulator-film & Low- ρ wiring material)



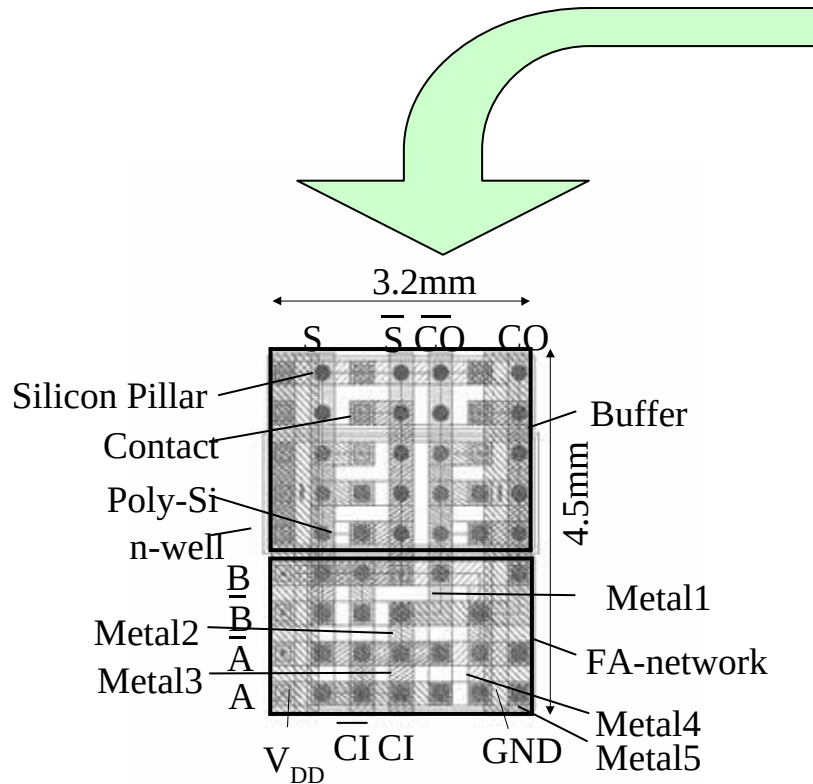
- * The delay time of LSI is determined by its wiring load.
- * The importance of Low-K Dielectric & Low- ρ wiring material is very high.

Principle of Downscaling of Chip Size with Vertical MOSFET (FB-SGT)

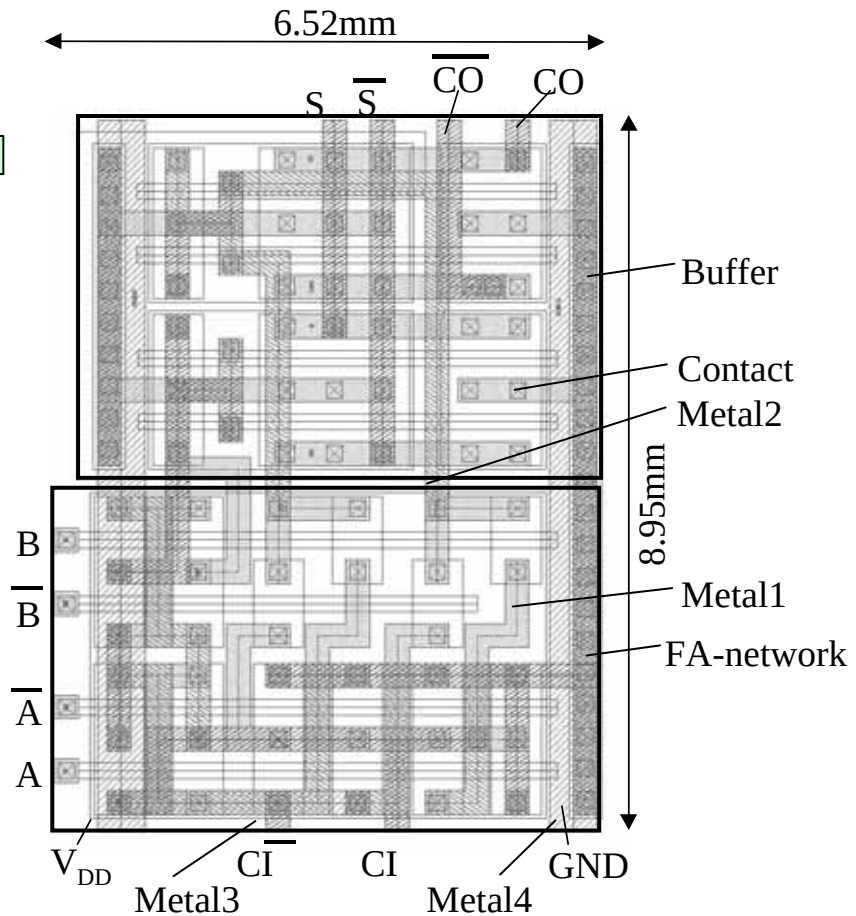


Downscaling of chip size by Vertical MOSFET (FB-SGT) (Full Adder)

Downscale by 24%

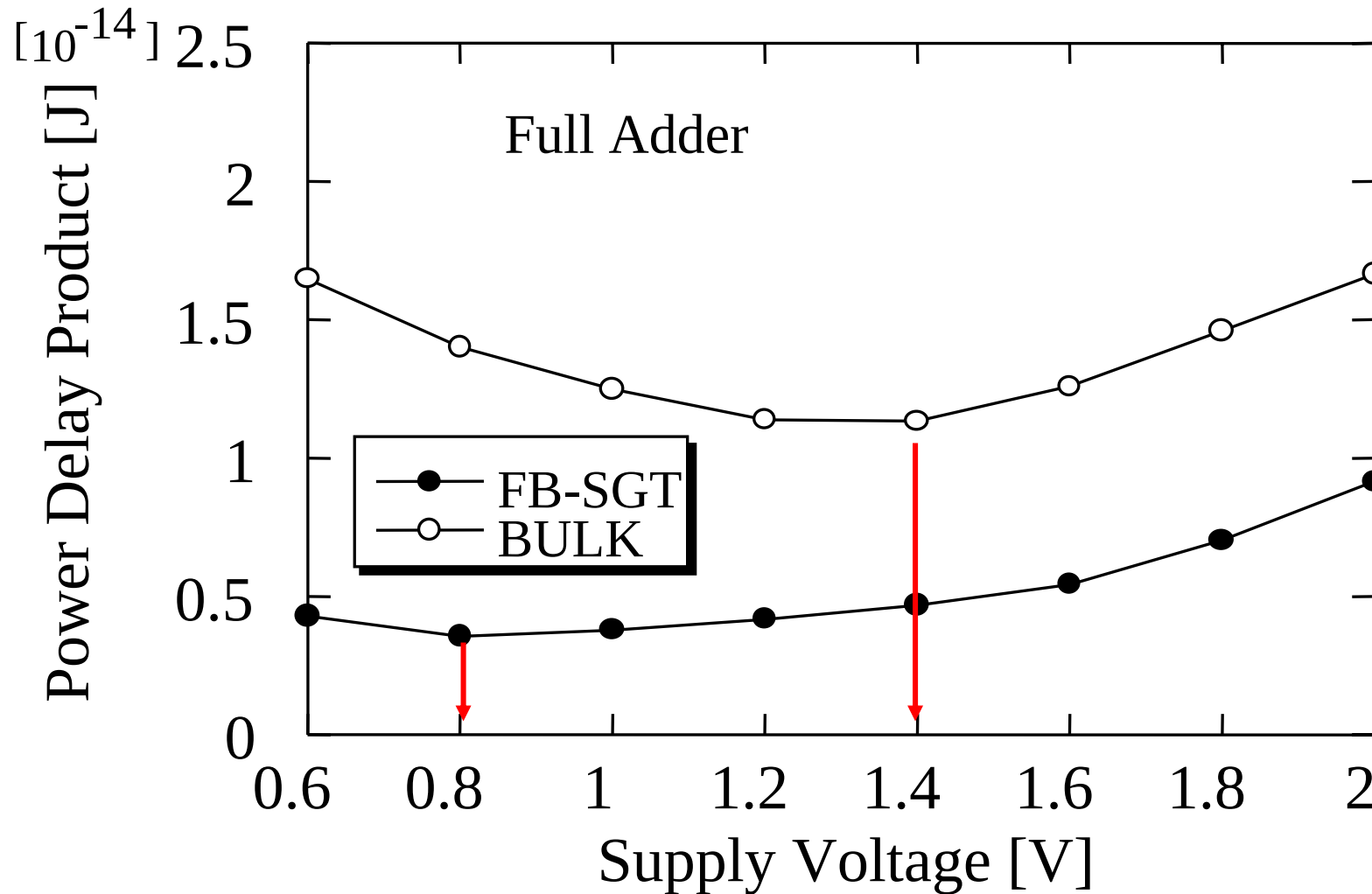


(a) Vertical MOSFET (FB-SGT) Layout Pattern

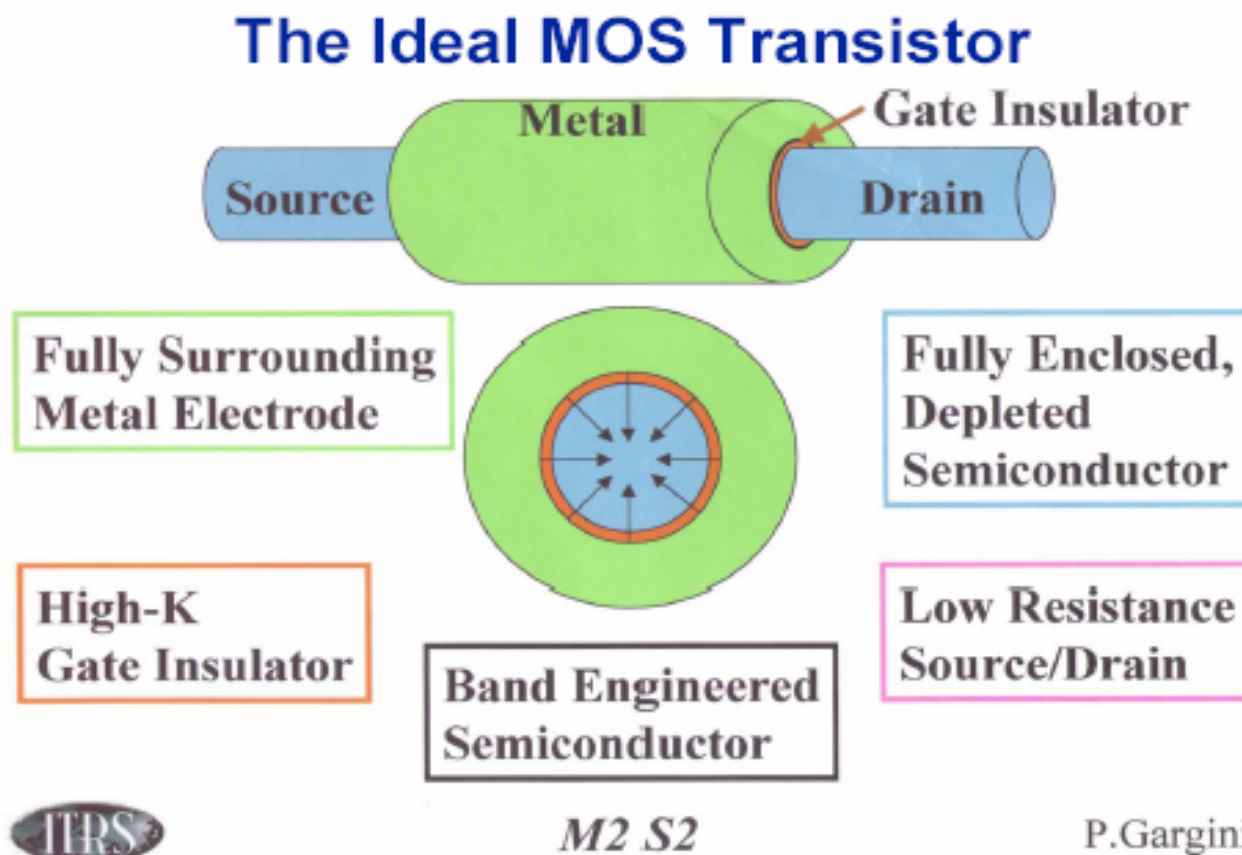


(b) Planar MOSFET Layout Pattern

Improved Power Delay Product by Vertical MOSFET (FB-SGT)



Evaluation of the Vertical MOSFET (FB-SGT)



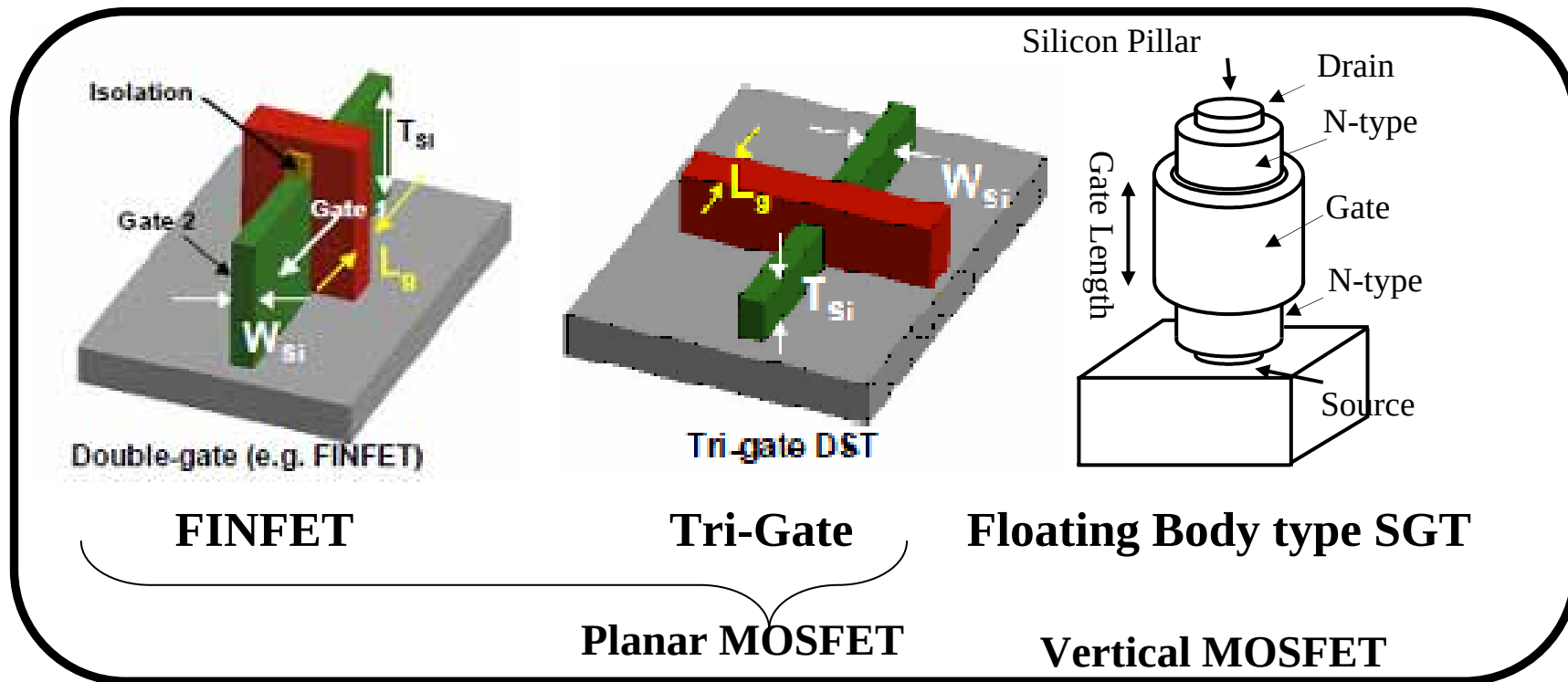
Mar 25, 2003

2003 International Conference on Characterization and Metrology for ULSI Technology

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Impact of Vertical MOSFET for High Performance Logic

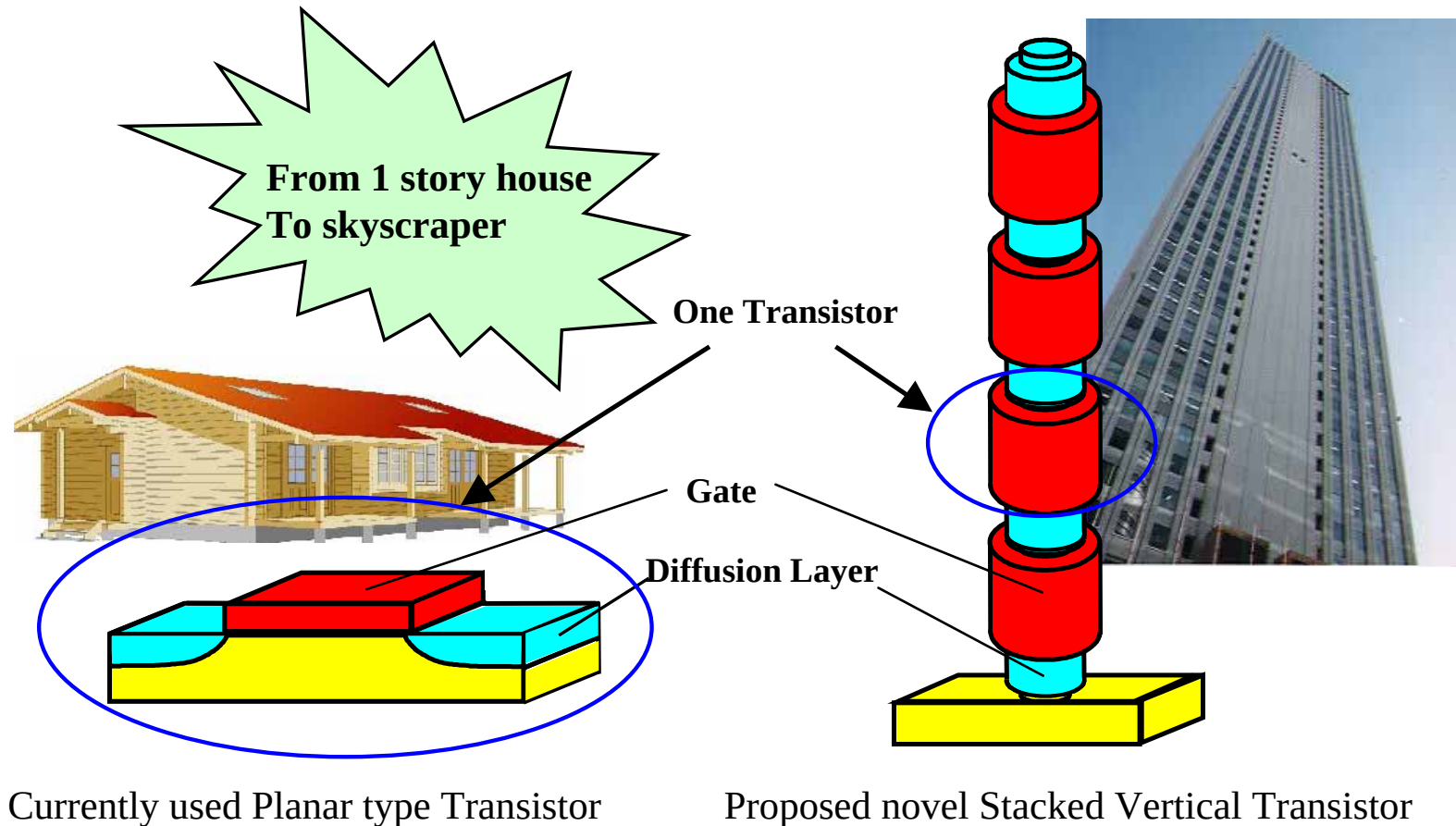
⇒ Multi-gate & Floating Body type



Tr. Performance
Wiring Problem
Packing Density



Even Higher Integration by Stacked Vertical MOSFET

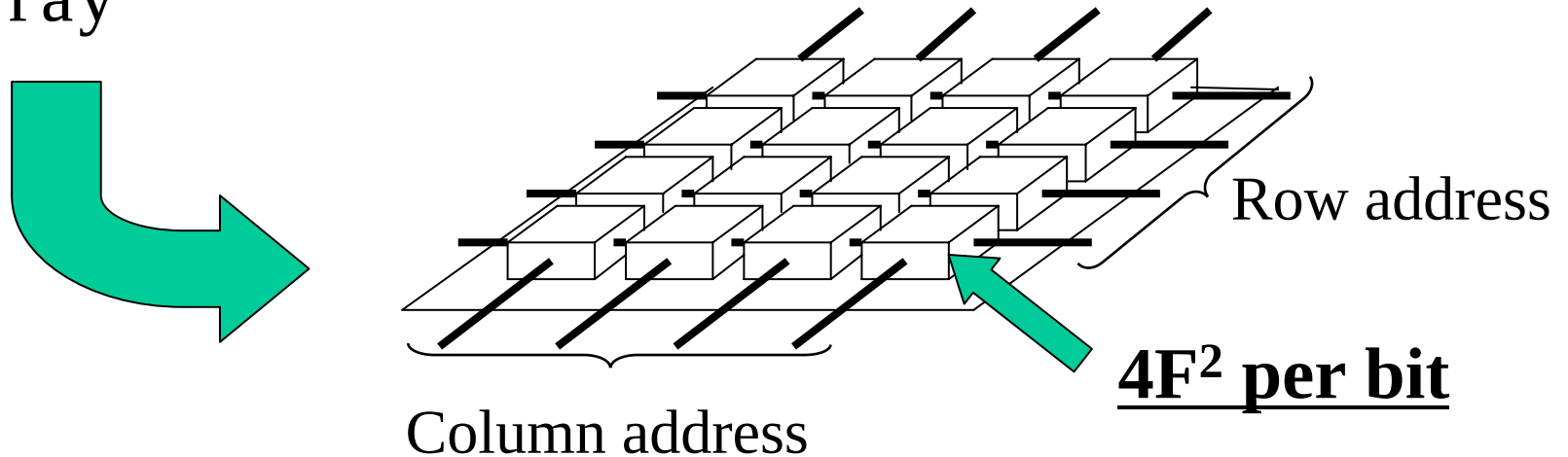


Impact of Vertical MOSFET for High Density Memory



The limitation of conventional cell size

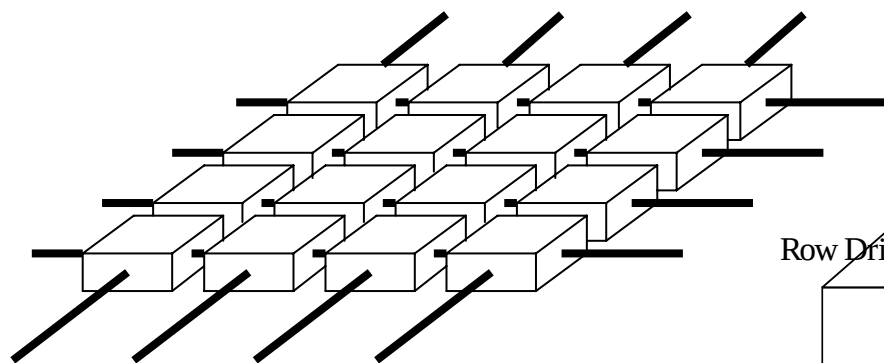
Conventional 2 Dimensional
cell array



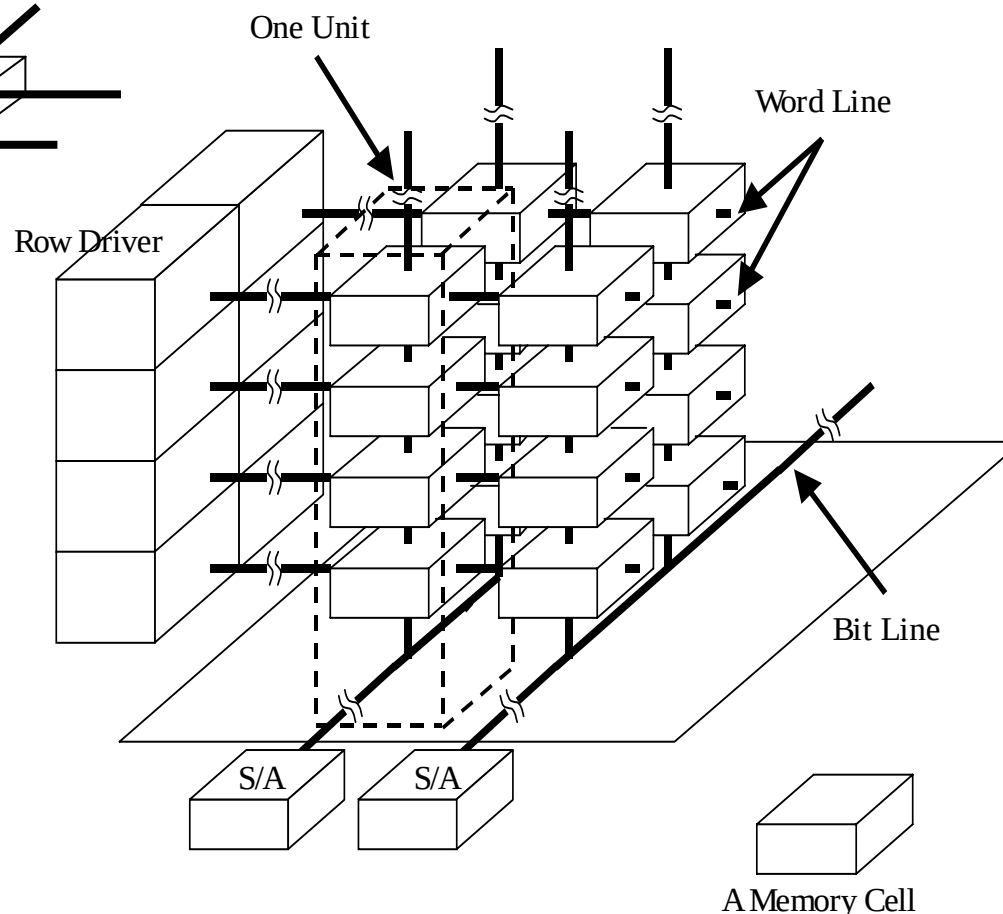
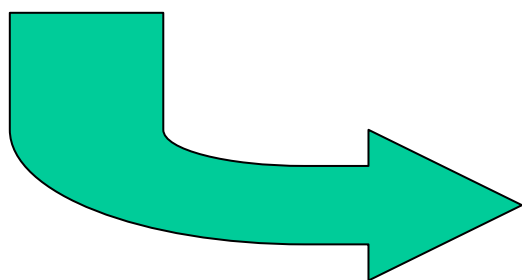
F : a minimum feature size

These conventional Flash memories have the limitation of cell area of $4F^2$ per bit.

New 3 Dimensional Memory Array Architecture



(a) Conventional 2D cell array



(b) New 3D-memory array architecture

Requirements for future Flash Memory

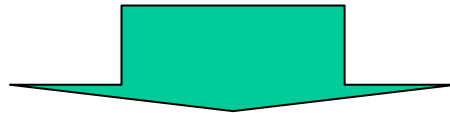
Shrinking cell size

<Reported technologies>

- * Shrinking of design rule
- * Self-aligned floating gate structure
- * Self-aligned STI structure
- * Scaled dielectric

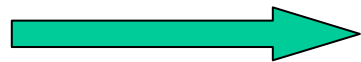
< Limitation factor for reduction of cell size>

- * Memory cell area per bit
- * Spacing between neighboring memory cells
- * Spacing between gate electrode and drain contact hole
- * Contact hole size and source line size



NAND structured Flash Memories

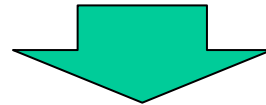
Demand for Flash Memory



Conventional NOR Flash Memory

Unipolarity program and erase operation

Programming speed & reliability = not sufficient



NAND structured Flash Memory

- (1) High speed programming
- (2) High reliability

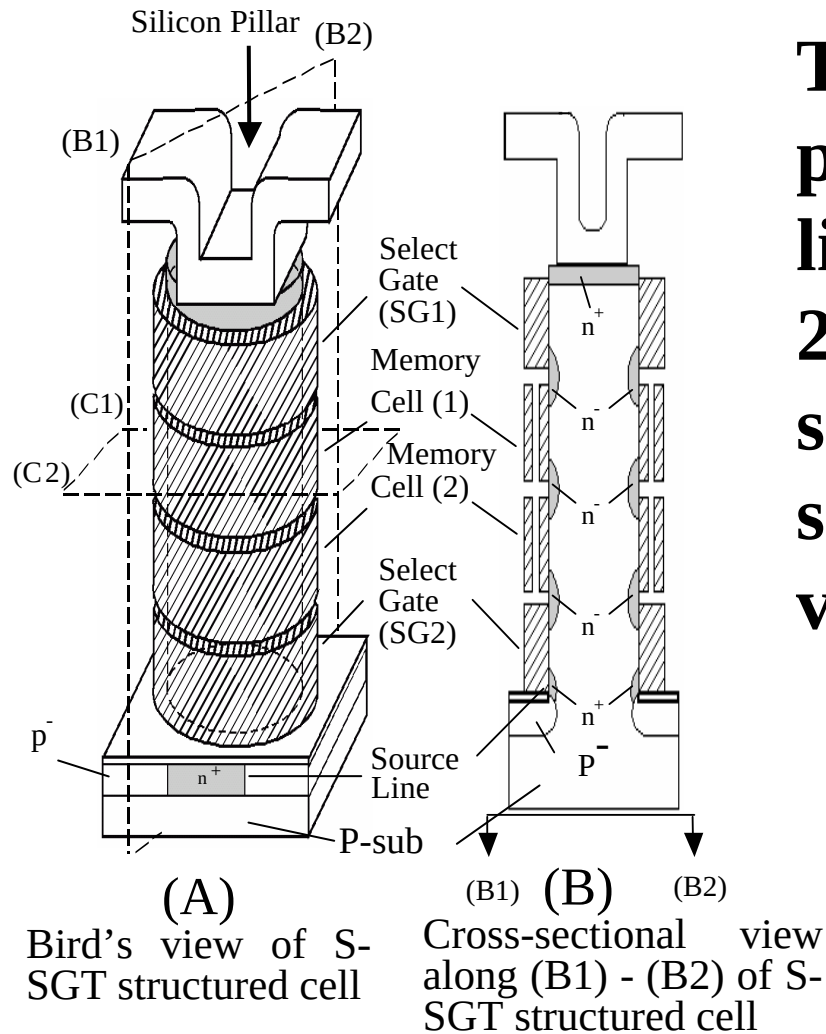
Bipolarity program
and erase operation

NAND structured Flash Memory

- * small cell size
- * High speed programming
- * High reliability



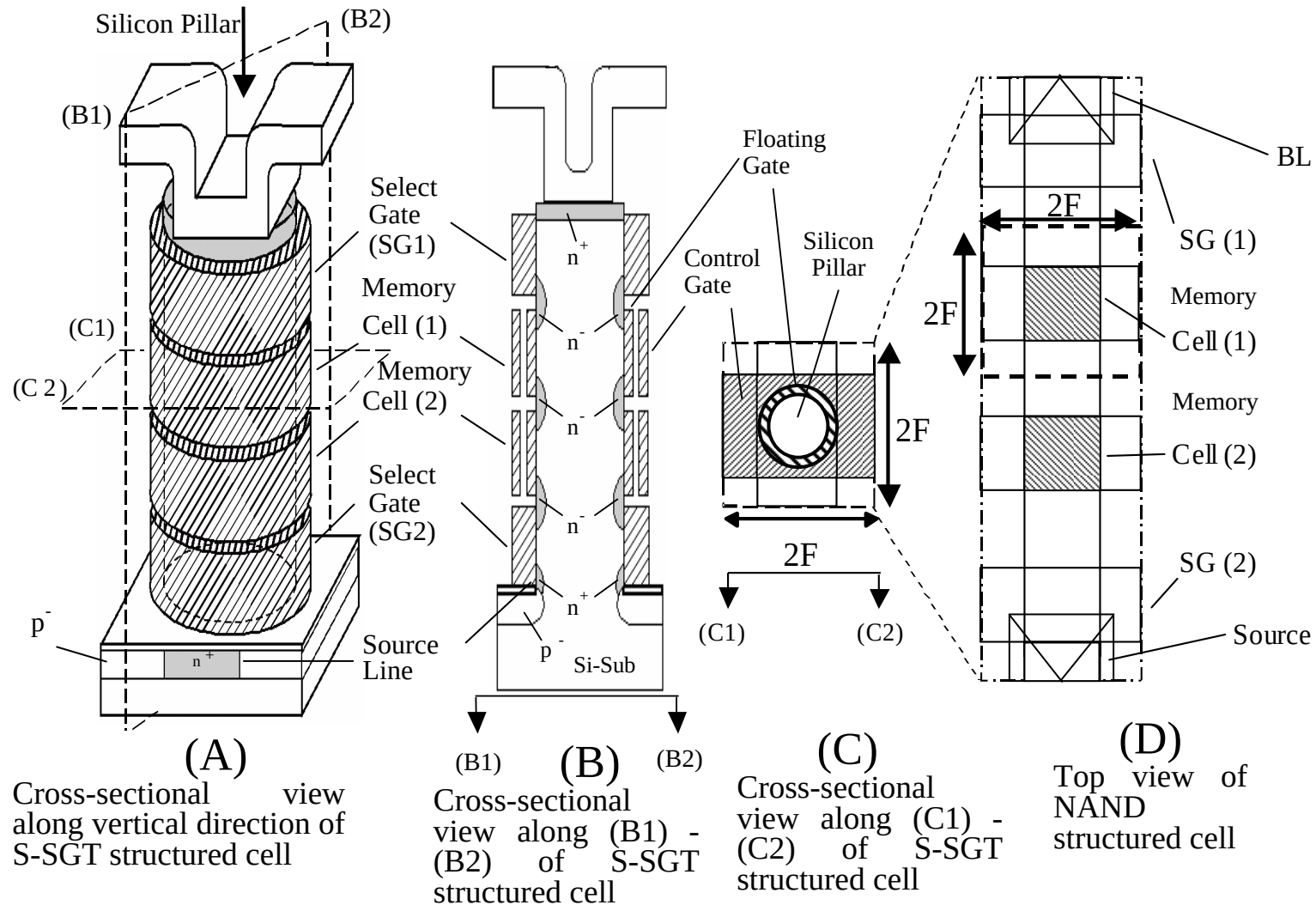
Concept of S-SGT structured cell



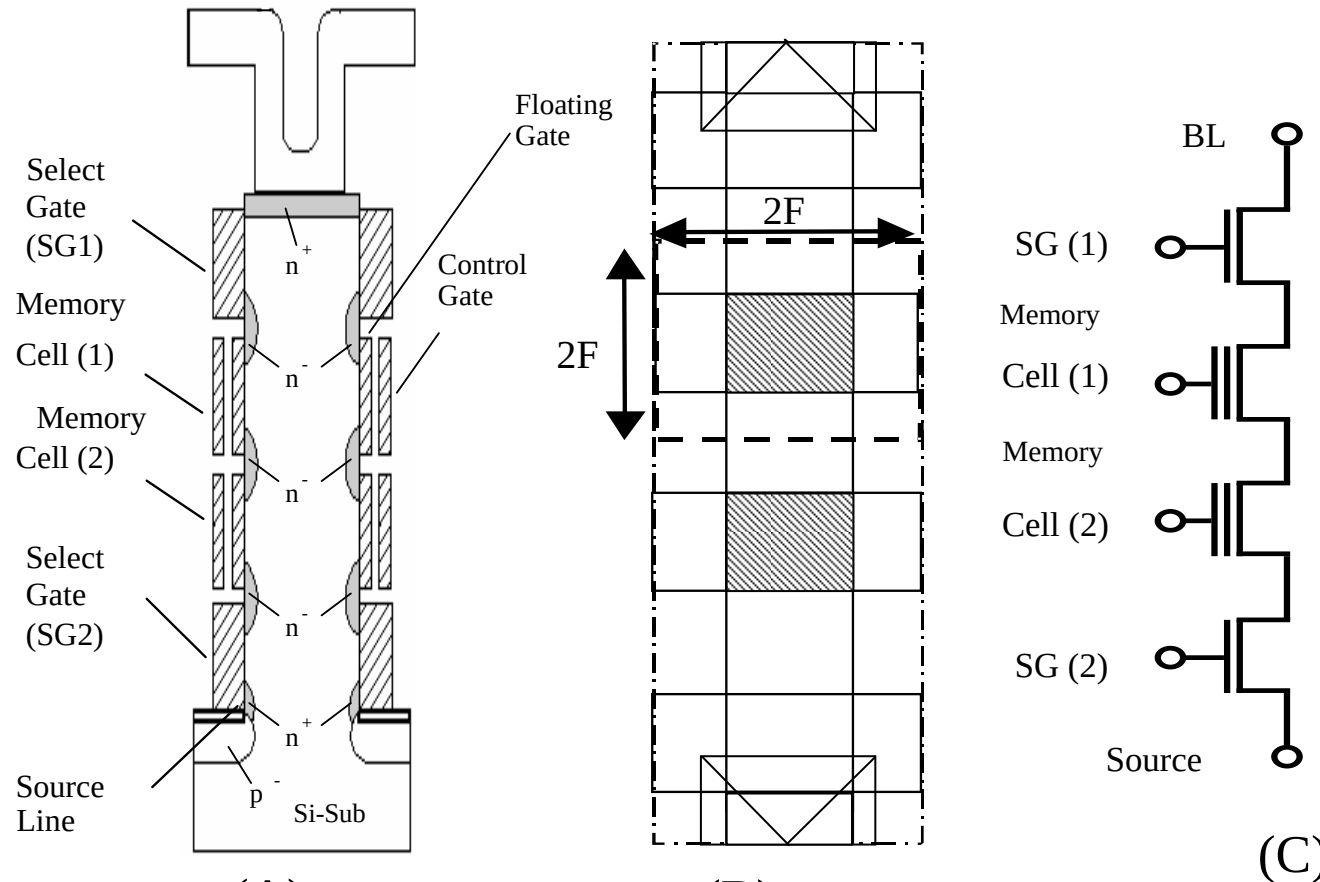
The structure of the proposed cell arranges bit line contact, first select gate, 2 SGT type memory cells[2], second select gate and source line in series vertically in one silicon pillar.

[2] T. Endoh, M. Hioki, H. Sakuraba, M. Lenski, and F. Masuoka, "Floating Channel Type SGT Flash Memory", 196th Meeting of The Electrochemical Society, 1999 Fall Meeting of The Electrochemical Society of Japan, Vol.99-2, Abstract No.1323, Hawaii, October 17 - 22, 1999..

Concept of S-SGT structured cell



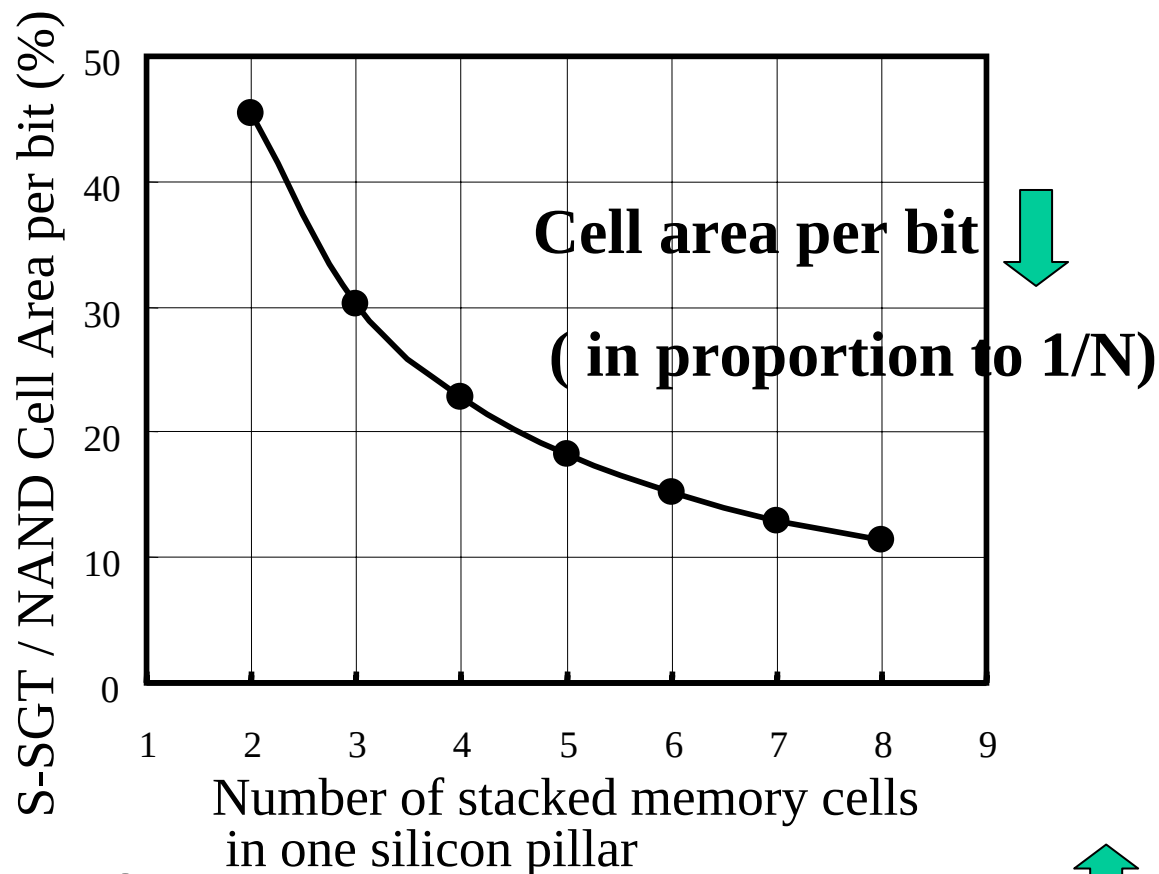
Equivalent circuit of S-SGT structured cell



The equivalent circuit of S-SGT structured cell is the same as that of conventional NAND structured cell.

(A) S-SGT structured cell (B) NAND structured cell (C) Equivalent circuit of S-SGT structured cell and NAND structured cell

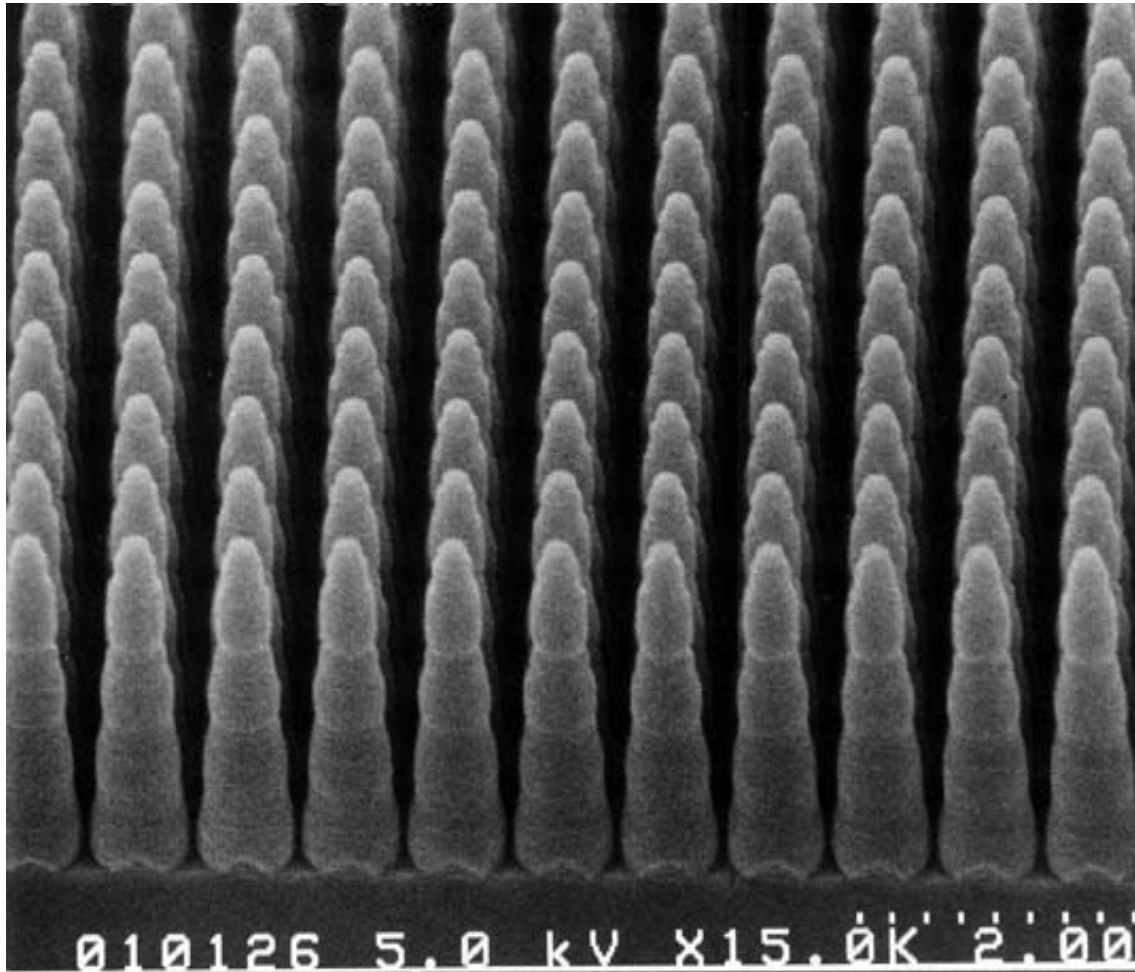
Cell size of S-SGT structured cell



The number (N) of stacked memory cells in one silicon pillar

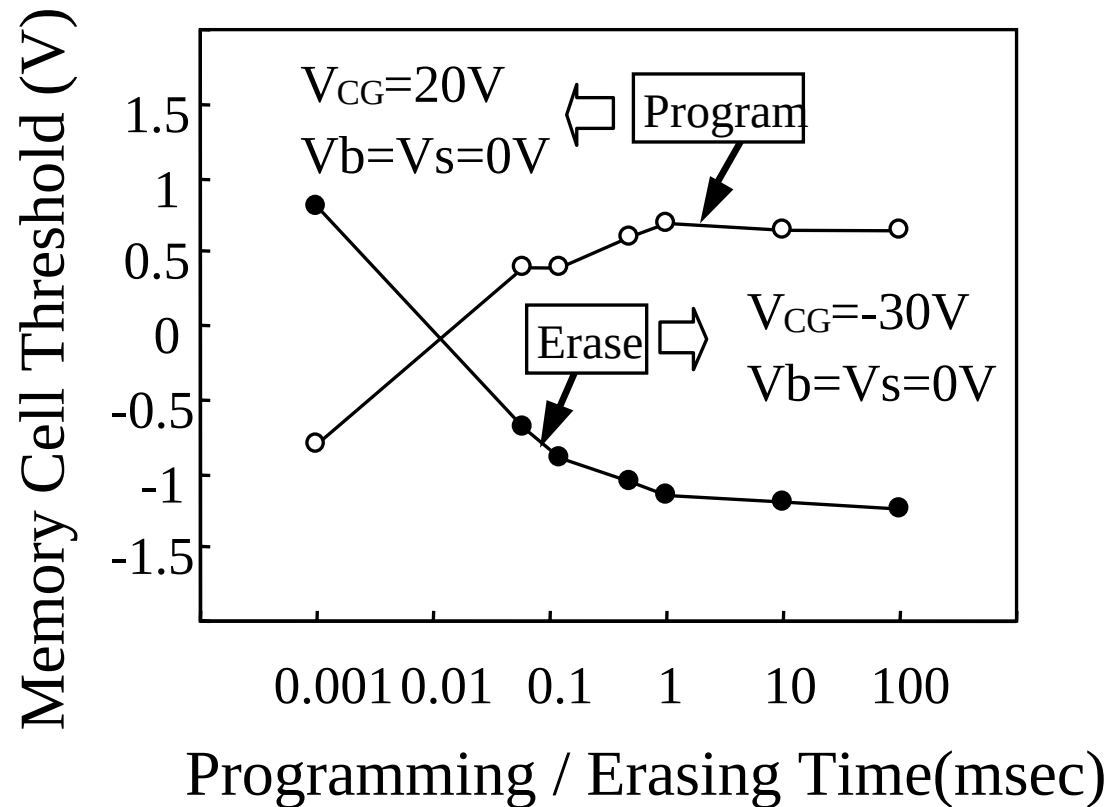
Cell area per bit of the S-SGT structured cell

SEM Photograph of S-SGT structured cell



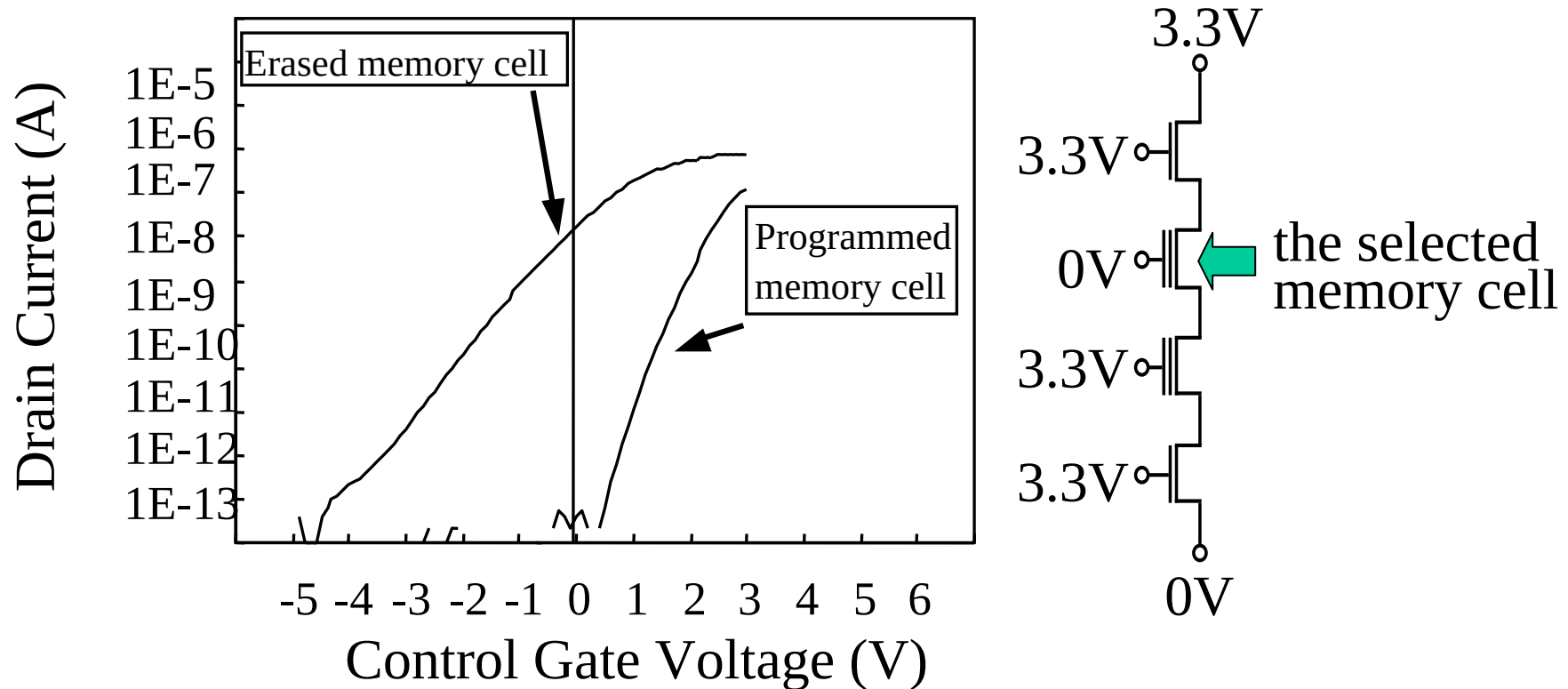
The S-SGT structured cell consisting of 2 stacked memory cells is fabricated using a 0.2μm process.

Programming and erasing characteristics



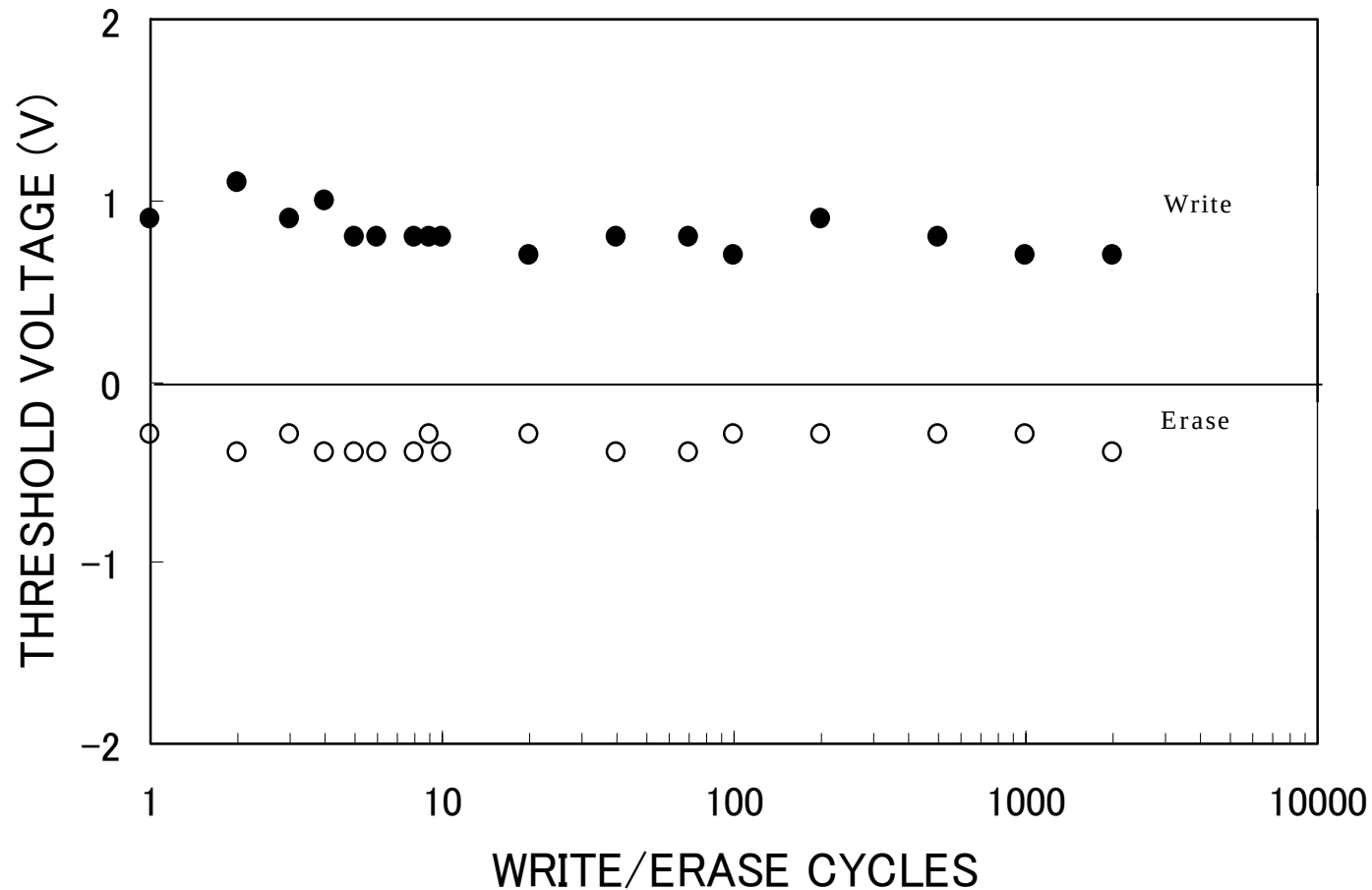
Programming and erasing can be accomplished by uniform F-N tunneling.

Id-Vg characteristics



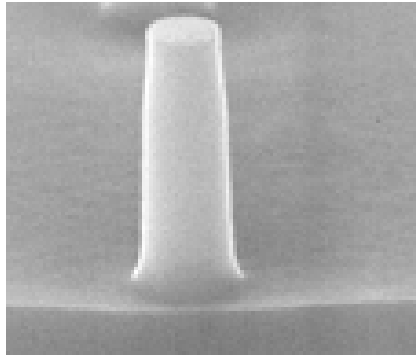
A drain current flows when the selected memory cell is in erased state, while the drain current does not flow at all when the selected memory cell is in programmed state.

Endurance Characteristics of Stacked SGT Flash Memory



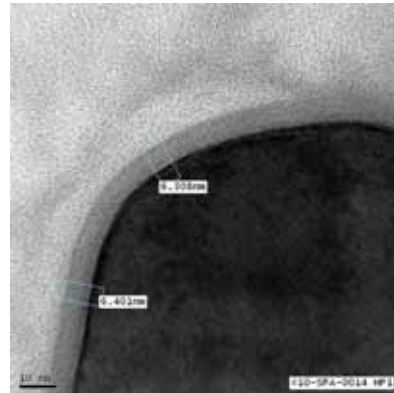
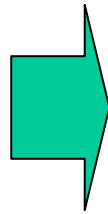
New Process technology for improving Endurance Characteristics of Stacked SGT Flash Memory

[1] Low damage Etching Process



**Collaborating work
with Tokyo Electron Ltd.**

[2] Uniform gate insulator films on any crystal orientation Si surface



By using SPA OX system, gate insulator films can be fabricated uniformly, on any crystal orientation Si surface.

Conventional OX. Process

SPA OX. Process

Impact of Stacked Vertical MOSFET for Flash Memory

- (1) Novel Flash Memory with S-SGT structured cell has been developed.
- (2) Proposed cell achieves cell area of $4F^2/N$ per bit without multi bit per memory cell technology.
- (3) The fabricated novel S-SGT structured cell consisting of 2 stacked memory cells achieves a smaller cell area per bit less than 50% of the conventional NAND structured cell.
- (4) The S-SGT structured cell can be successfully applied to over 16G / 64G bit Flash Memory and beyond.