
From: Scott DeBoer (sdeboer)
Sent: Tuesday, October 10, 2017 2:12 PM
To: Russ Meyer (rlmeyer); Jeff VerHeul (jverheul)
Subject: Re: [EXT] EE Times - Limitation of 3D NAND Scaling

I guess he has given up on sending everyone in the company notes about 3D DRAM and moved to this 😊 We actually spent time going over his 3D DRAM concept a couple years ago and it was flawed at a Jr engineering level. Maybe eventually after everyone told him that he focused his technical prowess on NAND replacement!

From: Russ Meyer <rlmeyer@micron.com>
Date: Tuesday, October 10, 2017 at 9:48 AM
To: Jeff VerHeul <jverheul@micron.com>, Scott Deboer <sdeboer@micron.com>
Subject: RE: [EXT] EE Times - Limitation of 3D NAND Scaling

Good thing he's not your TD guy ;-) We'll see if we can get a 4Tb on 150s (QLC + ~230 tiers)

From: Jeff VerHeul (jverheul)
Sent: Tuesday, October 10, 2017 9:33 AM
To: Scott DeBoer (sdeboer) <sdeboer@micron.com>; Russ Meyer (rlmeyer) <rlmeyer@micron.com>
Subject: FW: [EXT] EE Times - Limitation of 3D NAND Scaling

Not sure why these guys continue to send me mail, but thought I would pass this on to you... - Jeff -

From: Kay Lee [<mailto:kay.lee@besang.com>]
Sent: Tuesday, October 10, 2017 8:17 AM
To: Jeff VerHeul (jverheul) <jverheul@micron.com>
Subject: [EXT] EE Times - Limitation of 3D NAND Scaling

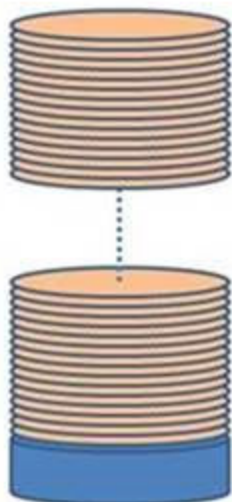
Dear Jeff VerHeul

“The life span of 3D NAND might be a lot shorter than most people think.”

At the Flash Memory Summit this year, Samsung announced its development of 1Tb 3D NAND, which would be used for commercial products launching next year. How about 4Tb and 16Tb 3D NAND? When will they hit the market? Based on the information available on TLC 512Gb 3D NAND with 64-layer and assuming string stacking of 64-layer, in order to implement the 4Tb NAND chip:

- Eight string stacks of 64-layer are needed. Which will make $(512\text{Gb} \times 8) = 4\text{Tb}$
- The total layer then becomes 512-layer
- It will take about a year to process a wafer, 5 weeks for memory logic plus 8 times (i.e. 8 string stack of 64-layer) 5 to 6 weeks for a 64-layer cell layer implementation. Therefore, the wafer processing time for a 512-layer will be about 45 to 53 weeks.

It is practically impossible to implement 4Tb or 16Tb NAND using 3D NAND technology.



For **4Tb** 3D NAND

- 8 string stacks of 64-layer
- So, it should be 512-layer
- About 1 year wafer processing time

For **16Tb** 3D NAND

- 32 string stacks of 64-layer
- So, it should be 2,048-layer
- About 4 year wafer processing time

Please find out this article at EE Times.

https://www.eetimes.com/author.asp?section_id=36&doc_id=1332422&piddl_msgid=374214&piddl_msgposted=yes#msg_374214

Thank you!

Best regards,

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