

History and Trend of 3-Dimensional Integrated Circuit

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Abstract—This paper discusses the history and trend of 3D IC, for better understanding of various 3D ICs.

I. INTRODUCTION

For many decades, 3-Dimensional (3D) Integrated Circuits (IC) have been studied and developed as an alternative solution to conventional 2D ICs. Even though 2D ICs followed Moore's Law without delay and discontinuity for the last several decades, the semiconductor industry is now facing tough challenges due to difficulties of device shrinking as well as the delay and high cost of next generation lithography tools. Therefore, the demand for and importance of 3D IC has increased sharply. As shown in Figure 1, there are many different approaches for the implementation of 3D ICs and each of them have unique technical approaches, applications, and limitations. Some of them have been well known for a long time and others are fairly new to the semiconductor industry. This paper discusses the history and trend of 3D IC, for better understanding of various 3D ICs.

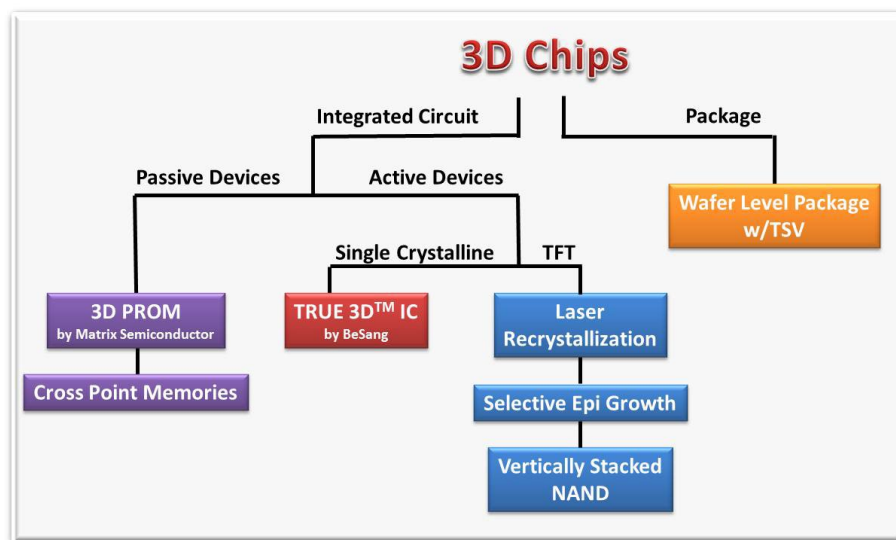


Figure 1. Tree of 3D Chips which includes 3D IC and 3D Package with TSV.

II. TSV

TSVs were developed for vertical stacking of chips in wafer level packages. The interconnection capability of TSV is limited to a few thousand per millimeter square, which is far less in comparison to IC level integration. ICs are implemented during in-line processing and have roughly more than 100,000 interconnects per millimeter square. Another important difference between 3D IC and 3D package comes from the existence of driver circuits for 3D interconnects. TSV is much bigger than conventional vias and requires an internal landing pad, which has a large parasitic capacitance. Therefore, each TSV needs a driver and consumes power to drive signals through TSV. Nevertheless, TSVs are good for small form factor for mobile applications and fast operation with reduced interconnects between microprocessor and stand-alone memories for servers. TSVs for System-in-a-Package (SiP) have been considered an important alternative solution to System-on-a-Chip (SoC) because it is difficult for SoC to integrate many different functions into a single chip and it may increase the cost of a chip. One thing for certain is that TSVs are in the package domain, which is different from the IC domain.

III. MOTIVATIONS FOR 3D IC

There are several motivations for 3D IC. One is the low cost of chip production because more die-per-wafer can be produced from a given wafer. This is especially important for memory products because cost-per-bit is generally the number of dies per wafer. Short distance routing for fast operation from the design of 3D IC is another important consideration for logic products, such as CPU, DSP, GPU and ASIC. SoC in 3D is also another important motivation of 3D IC. As system complexity increases, semiconductor companies have a desire to combine multiple chips into a single chip for better performance, lower production cost, and smaller form factor. Conflictingly, SoC faces high production costs and low yield due to severe process incompatibility between different functional blocks, such as logic and embedded memories. Therefore, SoC in 3D could separate functional blocks and optimize each of them independently as shown in Figure 2.

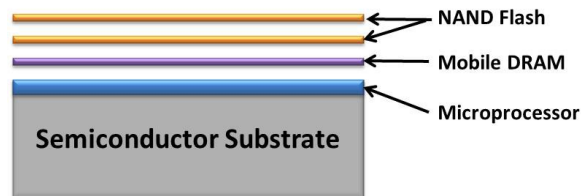


Figure 2. An example of SoC in 3D.

IV. HISTORY OF 3D IC

In earlier years, 3D IC was studied and developed based on 3D semiconductor layer formation on top of the interlayer dielectric, where devices were pre-formed on the surface of the semiconductor wafer and underneath the interlayer dielectric. Well-known 3D semiconductor layer formation methods are recrystallization of deposited amorphous semiconductors using laser and selective epitaxial growth (SEG). The scanned laser melts and recrystallizes amorphous semiconductors. As the power of lasers and the number of laser scanning increase, the size of crystalline also increases. However, it is not practically possible to eliminate grain boundaries as shown in Figure 3. Therefore, 3D IC based on laser recrystallization becomes a form of Thin Film Transistor (TFT) and device performances are limited compared to devices on single crystalline semiconductor substrates [1]. SEG generates a 3D crystalline semiconductor layer on top of the dielectric layer from the growth of an epitaxial layer through multiple pin holes on the single crystalline semiconductor substrate. A major drawback of this method is that there is no practical method to eliminate protrusion defects as shown in Figure 4.

Figure3. SEM image of recrystallized amorphous silicon by laser scanning [1]	Figure4. SEM image of local epitaxial growth and protrusion defects

V. TFT

These TFT methods have many fundamental issues. One major drawback is high temperature processing (>900 degree Celsius), which may alter device performance including metal interconnect lines in the underlying layer. Defect control is another important issue [2]. Even though the 3D layer can be formed at low temperatures without defects, there are still many questions regarding low temperature processing for transistor formation including impurity junction formation and reliable gate oxide formation. Therefore, these TFT methods still have many challenges.

There is another TFT method for 3D IC. 3D stacked vertical NANDs are being developed [3] using multi-layer polysilicon deposition on top of dielectric layers. These approaches are well designed in terms of process integration because multi stacking polysilicon and dielectric layers, and sequentially making holes to generate vertically connected transistors are

conventional CMOS processes. Considering cost-per-bit, these approaches have many advantages because material costs are low and memory bit can be expanded vertically if these become available in the market. However, one expected major challenge associated with 3D stacked NAND is the quality of polysilicon as a device substrate. TFT is a proven device and has been used as an LCD driver for a long time. However, the size of a TFT LCD driver (i.e. length and width of MOSFET) is about a few micrometers and the gate oxide thickness is a few hundred nanometers. Because of the size, the TFT LCD driver is less sensitive to leakage currents. In comparison to that, the size of advanced memory cells (i.e. 20nm to 15nm gate length and a few nanometers of gate oxide) is much smaller. Therefore, it is interesting to see how 3D stacked vertical NANDs will progress in the development stage and serve the market in the future.

VI. 3D PROM AND 3D CPM

Matrix Semiconductor successfully introduced to market high density 3D memory using antifuse-based programmable ROM (PROM) as shown in Figure 5. Unlike TFT 3D IC, the cell in 3D does not require 3D semiconductor layers to form devices, and it only utilizes electrodes and a thin dielectric in between the electrodes to form antifuse. Compared to TFT 3D ICs, this approach does not have the challenges of the formation of 3D semiconductor layer and low temperature processing. One major downside of 3D PROM is the limitation of its application to OTP. Unfortunately, it has not evolved into 3D flash memory yet.

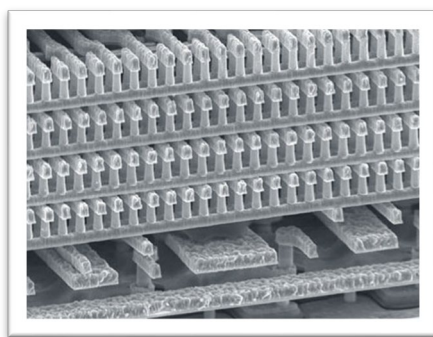


Figure 5. SEM image of 3D PROM by Matrix Semiconductor

Cross point memories (CPM) are currently being developed. Similar to 3D PROM by Matrix Semiconductor, CPM does not require 3D semiconductor layer formation. Process integration of CPM is relatively simple compared to 3D TFT because it does not require high temperatures or complex processing for transistor formation. If CPM works, it could provide high density non-volatile memory at a low cost because the memory cell density can be easily expanded vertically at a low cost. Intel introduced CPM using phase change memory (PCM) in 2009 as shown in Figure 6, and Micron and Unity Semiconductor are also working on CPM. One expected challenge comes from emerging materials (i.e. PCM and Resistive RAM), which are used for CPM formation. It will also be interesting to see how CPM solves this challenge and competes with high density NAND flash when it comes to market.

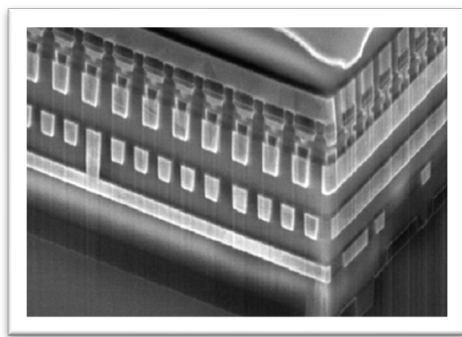


Figure 6. SEM image of 3D CPM by Intel

Considering cell density and its expandability, 3D PROM and 3D CPM have excellent structures for non-volatile memories. However, these devices are either fuse or resistor and, therefore, might be not suitable for dynamic memories.

VII. CHALLENGES ASSOCIATED WITH 3D IC

Single crystalline silicon layer formation on top of interlayer dielectrics using the wafer bonding and detaching method has been developed by BeSang [4], where devices are pre-formed on the surface of the semiconductor wafer and underneath the interlayer dielectric. The formation of 3D semiconductor layers is similar to well-known silicon-on-insulator technologies. However, technical challenges associated with this 3D IC are far different due to wafer bonding with uneven surfaces, low temperature processing restrictions, and device formation using 3D semiconductor layers as shown in Figure 7.



Figure 7. Challenges associated with 3D IC using wafer bonding

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