

Integration of Plasma-Assisted and Rapid Thermal Processing for Low-Thermal Budget Preparation of Ultra-Thin Dielectrics for Stacked-Gate Device Structures

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This paper discusses a new approach to the formation of ultra-thin gate dielectrics for Si-ULSI applications in which separately controlled plasma-assisted and/or rapid thermal processing steps are combined to fix the chemical bonding and minimize the defect structure at the Si-SiO₂ interface, and within the dielectric layers. One example of this approach combines (i) low-temperature (300°C) plasma-assisted processing to control the initial bonding chemistries at (a) the Si-SiO₂ interface, and (b) in homogeneous oxide, or composite dielectrics with nitride or oxynitride layers, with (ii) higher temperature (900°C), but low-thermal budget, rapid thermal annealing to promote physical and/or chemical relaxations that minimize both interfacial and bulk dielectric defects, thereby improving device performance.

KEYWORDS: low-temperature processing, low-thermal budget processing, plasma-assisted oxidation, remote plasma-enhanced chemical-vapor deposition, rapid thermal chemical-vapor deposition, rapid thermal annealing, Si-SiO₂ intertaces, field effect transistors, silicon oxide, silicon nitride, silicon oxynitrides

1. Introduction

As semiconductor device dimensions shrink into the deep sub-micron regime, $\sim 0.25\ \mu\text{m}$ or less, the *equivalent oxide thicknesses* of gate dielectrics in field effect transistors (FETs) must be reduced proportionally to dimensions of 5–6 nm and less. This has stimulated a search for low-temperature/low-thermal budget processes for forming Si-dielectric heterostructures that can replace (i) conventional high temperature furnace oxidations, and/or (ii) post deposition nitridations and re-oxidations which must also be performed at high temperatures, and with significant expenditures in the available thermal budget. To date, several potentially viable processing approaches have been identified: (i) rapid thermal oxidation (RTO),¹⁾ and (ii) rapid-thermal and/or plasma-enhanced chemical-vapor deposition (CVD) for the formation of oxide and/or nitrogen-containing thin film dielectrics.^{2–4)} Each of these methods has potential advantages and challenging problems. However to eventually be useful in manufacturing, any new approach for forming the Si-dielectric heterostructure must also be capable of being integrated into the sequence of processing steps used to fabricate the remainder of the transistor structure, as well as the complete integrated circuit. Recently, we have focused on a hybrid approach for the fabrication of gate stacks that replaces conventional batch processing with single wafer processing, and integrates into a single chamber and/or cluster tool, the capabilities for the following independently controlled *in-situ* processing: (i) the final cleaning and passivation of the Si surface; (ii) the formation of the Si-SiO₂ interface; (iii) the deposition of a single layer or composite oxide, oxynitride or nitride dielectric material; (iv) the deposition a polycrystalline Si gate electrode, and (v) rapid thermal annealing (RTA),

as required at intermediate and/or final stages of the processing sequence for the gate stack.^{5,6)} This paper discusses the processing of MOS devices with (i) homogeneous silicon dioxide dielectrics,⁶⁾ and (ii) composite dielectrics in which silicon oxynitride or nitride layers are sandwiched between ultra-thin silicon oxide layers, as for example in oxide-nitride-oxide (ONO) structures.^{7,8)}

2. Processing of Semiconductor Device Structures

2.1 General considerations

The formation of deposited dielectrics in MOS devices can include up to five distinct types of process steps (see Fig. 1): (i) *ex-situ* preparation of the Si surface to remove field, native, or chemically-produced oxides, along with other common impurities such as hydrocarbons and trace metals, (ii) additional *in-situ* pre-deposition surface cleaning and passivation, (iii) the formation of the Si-SiO₂ interface, (iv) the deposition of the dielectric layers by low-temperature (300°C) remote plasma-enhanced CVD and/or intermediate-temperature (800°C) rapid thermal CVD, and (v) mid- or end-of process post-deposition annealing (a) as separate rapid thermal anneals (RTAs), and/or (b) during electrode deposition and dopant activation, as for example in the CVD deposition of polycrystalline Si followed by a 900°C POCl₃ doping process. Note that the number of separate steps can be reduced, for example, by combining steps (ii) and (iii), or (iii) and (iv) into a single process step. Finally, device structures, capacitors with Al or doped polycrystalline Si electrodes, and insulated gate FETs with doped polycrystalline Si electrodes, can then be completed by using conventional processing techniques such as photolithography and dryetching.⁶⁾ The *in-situ* processing steps described below have been performed in multi-chamber integrated

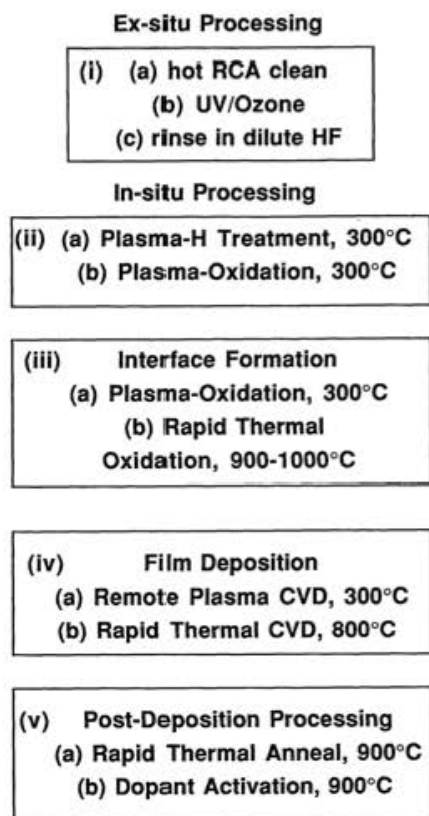


Fig. 1. *Ex-situ* and *in-situ* processing steps for deposited gate dielectrics.

clusters that include (i) on-line chemical and structural surface diagnostics, *e.g.*, Auger electron spectroscopy (AES) and low-energy electron diffraction (LEED), and (ii) multi-function processing chambers for (a) plasma-assisted-oxidation and film depositions by remote PECVD, or rapid thermal CVD, or (b) rapid thermal oxidation and rapid thermal CVD film depositions.

2.2 Homogeneous oxide dielectrics

Pre-deposition treatment of the Si surface that will in contact with the deposited gate dielectric is crucial to obtaining high levels of performance and reliability. This treatment typically includes two steps: (i) an *ex-situ* process, which, for the majority of the work reported in this paper, has been a hot RCA clean (80°C) followed by a rinse in dilute (1:30) HF; and (ii) an *in-situ* plasma-assisted surface cleaning and passivation step, where two different *in-situ* 300°C passivation approaches have been compared and evaluated.^{3,5)} One process was based on removal of residual O and C-contaminants by exposure to plasma-generated atomic-H and the formation of a H-passivated Si-surface,¹¹⁾ and the second on a pre-deposition plasma-assisted oxidation which also removed residual C-contaminants, but instead of generating a H-passivated surface, formed a superficial layer of SiO₂ (~0.5–0.6 nm thick), and hence included the formation of the Si–SiO₂ interface as well.³⁾ The 300°C H-process was abandoned because

(i) it did not effectively remove C and O-contaminants, (ii) it roughened the Si surface, (iii) H-atoms permeated the bulk Si, reducing minority carrier lifetimes, and (iv) all of the above contributed to marginal device performance, *e.g.*, Dit levels in the range of $5\text{--}10 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ (from analysis of capacitance-voltage (*C-V*) data), and breakdown fields (E_b) $< 10 \text{ MV cm}^{-1}$ (from ramped current-voltage (*I-V*) measurements). This paper focuses on devices in which the Si–SiO₂ interface is formed during an *in-situ* plasma-assisted, pre-deposition oxidation.³⁾ The paper also includes comparisons for devices where the Si–SiO₂ interface was formed in other ways; *e.g.*, (i) by the final oxide of the RCA clean, (ii) during the initial stages of film deposition by rapid thermal CVD, or (iii) by a pre-deposition RTO step.^{6,12)}

The pre-deposition oxidation is a remote process in which a He/O₂ mixture is excited upstream from the processing chamber so that the Si substrate is not immersed within the plasma glows, and does not serve as an electrode as in conventional capacitively-coupled plasma reactors. To evaluate the effectiveness of the pre-deposition plasma-assisted oxidation, the surfaces of *ex-situ* RCA-cleaned Si(100) wafers were characterized upon insertion the Si(100) wafer into a UHV-compatible processing system. These H-terminated Si(100) surfaces typically displayed a 1×1 symmetry, and showed residual C-atom and O-atom contamination at surface coverages of ~2–10 atomic percent (at.%). Combining *in-situ* AES and LEED measurements, with off-line SIMS and *C-V* analyses, the plasma-assisted oxidation was shown to (i) reduce C-atom levels to $\sim 10^{12} \text{ cm}^{-2}$ (SIMS), (ii) form ~0.5 to 0.6 nm of SiO₂ which served as a *platform* for the oxide depositions, (iii) prevent *uncontrollable* incorporation of N-atoms at the Si–SiO₂ interface during oxide deposition from an N₂O source gas, (iv) yield low trap densities at the Si–SiO₂ interface, $D_{it} \sim 1\text{--}3 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$, that were not increased by downstream processing at temperatures up to at least 900°C, and finally to support breakdown fields $> 10 \text{ MV cm}^{-1}$.¹³⁾ The same predeposition oxidation has been used for multi-layer dielectrics that include remote PECVD silicon oxynitride alloys,⁸⁾ and silicon nitrides as in SiO₂/Si₃N₄/SiO₂ (ONO) composites.⁹⁾ However, these multi-layer dielectrics require a 30 s RTA at 900°C to promote properties similar to those quoted above for homogeneous oxides that have been processed at temperatures up to at most 400–450°C; *i.e.*, the temperature of a post metallization anneal (PMA). An additional refinement of the pre-deposition oxidation process has been to replace the O₂ source gas with N₂O, or with an N₂O/O₂ mixture, and in this way change the bonded N-content at the Si–SiO₂ interface. Bonded-N concentrations, as determined from an analysis of SIMS data as an areal density, could be increased controllably and continuously from approximately $1.5 \times 10^{14} \text{ cm}^{-2}$ to $8.5 \times 10^{14} \text{ cm}^{-2}$ with essentially the same electrical properties; *e.g.*, $D_{it} \sim 1\text{--}2 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$, and breakdown fields $> 10 \text{ MV cm}^{-1}$. Increases in bonded-N at the Si–SiO₂ interface may also lead to systematic increases in device reliability, and this aspect of the device performance is currently un-

der investigation in our laboratory.

The thin film oxide depositions were performed using two CVD techniques: (i) remote PECVD at 300°C,^{3,11)} and (ii) rapid thermal CVD at 800°C.^{6,12)} For the remote PECVD, the Si-source gas, silane (SiH₄), was injected downstream from the plasma, and the O-source gas, N₂O, was pre-mixed with He and injected through the plasma generation tube. The plasma was powered by a 13.56 MHz RF source, typically at ~15 W. Deposition rates could be increased from 2.5 to 10 nm/min by increasing gas flows, and/or increasing plasma power, but without any significant changes in film properties or device performance. The rapid thermal CVD depositions were performed in an ultra-clean system with the same source gases, SiH₄ and N₂O, and at a temperature of ~800°C.^{6,12)} The deposition rate was typically 6 nm/min. The remote PECVD and rapid thermal CVD processes yielded homogeneous, stoichiometric oxide films with Si:O ratios of 1:2, as determined by AES, Rutherford back scattering (RBS) and/or secondary mass spectrometry (SIMS).

MOS devices were fabricated using different combinations of plasma-assisted and rapid thermal processing: for example (i) all devices incorporating remote PECVD oxides used the plasma-assisted oxidation pre-deposition process; whereas, (ii) devices incorporating rapid thermal CVD oxides used several different pre-deposition steps: (a) the *in-situ* plasma oxidation process, (c) *ex-situ* RCA cleans *with*, and *without* a final rinse in dilute HF, and (c) a pre-deposition rapid thermal oxidation (RTO). For the devices with remote PECVD oxides, the maximum processing temperature was determined by the processing required to form the gate electrode: (i) 400°C for Al electrodes (the PMA temperature), and (ii) 900°C for n-type polycrystalline Si electrodes as required for the POCl₃ doping process. For devices employing rapid thermal CVD oxides, the maximum temperature was (i) 800°C for devices with Al electrodes, (b) 900°C for doped polycrystalline Si electrodes, when not using a pre-deposition RTO, and (c) up to 950°C for devices with doped polycrystalline electrodes, when including a pre-deposition RTO.

2.3 Oxynitride and ONO dielectrics

Nitride films, prepared by remote PECVD at 300°C, were characterized by (i) on-line Auger electron spectroscopy (AES), and (ii) off-line infra-red (IR) absorption to determine an stoichiometry (Si-Si and/or Si-N bonding), and the bonded-H content. Source gases for these depositions were SiH₄ and ammonia (NH₃). The bonded-H concentrations were determined from the reduced IR absorbance spectra using well-established scaling relationships between the integrated absorbance and the H-content for each of the respective bond types; i.e., Si-H and SiN-H. The performance of nitride films as gate dielectrics has been found to vary significantly with the flow ratio (*R*) of the NH₃ to SiH₄ source gases.^{1,6)} As shown in Fig. 2, *R* has a strong influence on the local bonding arrangements, and hence, on the electrical properties in devices. Figures 2(a) and 2(b) summarize results of AES and IR studies,

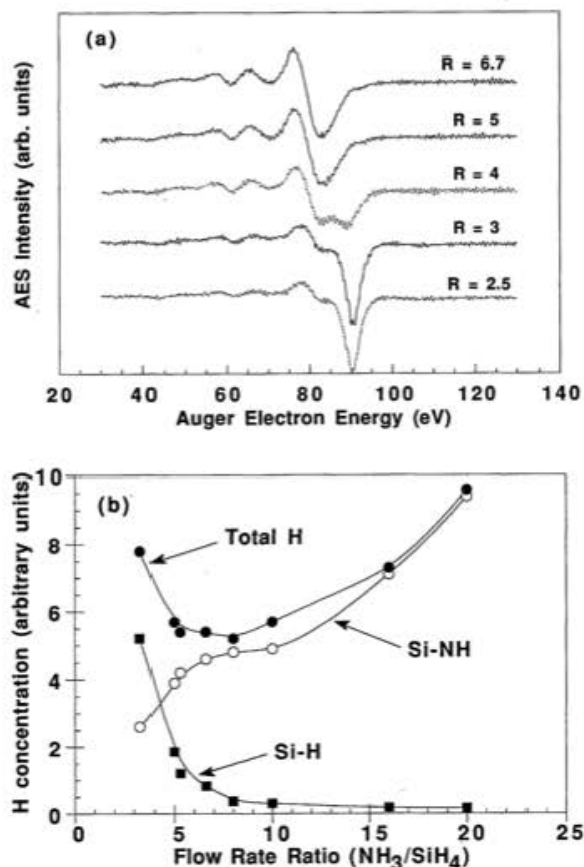


Fig. 2. (a) Auger electron spectra in SiLVV region for remote PECVD nitride films as a function of *R*, the flow rate ratio of NH₃ to SiH₄; (b) Infra-red (IR) absorption strengths for Si-H, SiN-H and total bonded-H as a function of *R*, the flow rate ratio of NH₃ to SiH₄.

respectively, for depositions in which the NH₃ and SiH₄ are injected downstream from a He plasma.²⁾ Similar results have been obtained when NH₃ is mixed with He, and the mixture is injected upstream and subjected to direct plasma excitation. However, the values of *R* that mark demarcation points between different local bonding arrangements are changed. Returning to the downstream source gas injection, as *R* is increased there are systematic changes in (i) the SiLVV features of the AES spectra in Fig. 2(a) indicative of a transition from a dominance of Si-Si bonding (~91 eV) to Si-N bonding (~83 eV); and (ii) the IR absorption strengths in Fig. 2(b) indicative of a transition from a dominance of Si-H to SiN-H bonding. The implementation of these nitride films into composite dielectrics for thin film transistors (TFTs) and MOS capacitors is subject to two materials constraints; *R* must be (i) sufficiently high so there is no AES-detectable Si-Si bonding, and (ii) not so high that the SiN-H concentration becomes excessively large, *e.g.*, >25 at.% of bonded-H. The Si-Si bonds are precursors for the formation of Si dangling bonds, whilst, excess SiN-H makes it difficult to reform idealized heteropolar network bonding arrangements after H-evolution has occurred during post-depo-

sition steps performed at temperatures higher than the deposition temperature, *e.g.*, as in a 400 to 450°C PMA, or as in 900°C gate electrode doping process. For downstream injection of the atomic source gases, the range of R for device-grade nitride films is from about 8 to 11.^{2,4-6)} Up until recently, we were not able to account for an observation that even though similar ratios of R were used to optimize nitride layers in c-Si-MOS devices with ONO dielectrics, and a-Si TFT's with ON structures, the c-Si MOS devices required a 30 s RTA at 900°C to promote good electrical properties,^{1,2)} whereas the TFTs, processed at 300°C, did not require any post deposition thermal annealing.³⁻⁵⁾ The IR results presented below identify the origin of this significant difference in processing requirements.

Analysis of the IR absorption data as a function of post-deposition isochronal (30 s) RTAs has indicated that the Si-H and SiN-H absorption strengths, and hence the concentrations of the respective bonding groups, are reduced as the annealing temperature is increased (see Fig. 3). There are at most small decreases in the absorption strengths for both types of vibrations for temperatures below about 400°C, while there are significantly larger decreases, by factors from ~5 to 20, if the temperature of the 30 s anneal is increased to between 500°C and 1000°C. The Si-H and N-H bond energies are large, ~3.5 eV and ~4.0 eV, respectively, so that significant H-evolution at temperatures as low as 500°C ($kT \sim 0.07$ eV) must be a cooperative effect involving for example the formation of molecular hydrogen, H₂. The low temperature release of H in these nitride films is similar to what has been observed for H-evolution from hydrogenated amorphous Si, where the Si-H bond energy is approximately 4 eV, and where the microscopic basis for the low-temperature evolution of H from these bonds has not as yet been unambiguously identified. Returning to the nitride and oxynitride films, it is assumed that release of bonded-H by thermal exposures higher than the deposition temperature of 300°C, as in a 400°C PMA, leads to defect formation within the nitride materials, and at the internal interfaces within the dielectric heterostruc-

tures (*e.g.*, at the O/N and N/O interfaces an ONO multilayer dielectric), which in turn degrade device performance. This assumption assumes that the release of H in gate dielectrics in the devices takes place at the same temperatures as H-atom release from homogeneous bulk films, and that this process generates dangling bonds on Si and/or N atoms. It is further assumed that temperatures of 400°C are too low to allow for structural relaxations which can lead to recombination of the dangling bonds created by the H-atom release.

3. Performance of Devices with Oxide Dielectrics

The properties of MOS capacitors and FETs with deposited oxides are now discussed, and FET performance for different processing techniques is compared in Figs. 4, 5 and 6. To converge toward the identification of the essential elements of a *generic processing sequence* for optimizing the electrical performance of FETs with deposited oxides, the properties of groups of devices processed in different ways have been compared.

3.1 MOS capacitors with Al electrodes, remote PECVD oxides, and H and O plasma cleans (300°C processing with 400°C PMA)

As noted above, these comparisons have established the superiority of the plasma oxidation process to the plasma-H clean. The combination of a pre-deposition plasma-assisted oxidation and a remote PECVD oxide deposition provides *separate and independent* control of interface formation and oxide deposition, and this results in superior electrical properties as compared to a plasma-H clean and remote PECVD deposition wherein interface formation takes place during film deposition by a *subcutaneous oxidation process* that is not under separate and independent processing control. In particular, D_{it} values decreased from $8 \pm 5 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ to $1.5 \pm 0.5 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$, and E_b values increased from 5–8 MV cm⁻¹ to 9–11 MV cm⁻¹, when the plasma-assisted oxidation was used instead of the plasma-H step.^{3,9)} Additional experiments have shown that replacement of the O₂ by N₂O as the O-atom source is an effective means of controlling the N-atom concentration at the Si-SiO₂ interface without reducing the levels of device performance as monitored in MOS capacitors. Proceeding in this way the N-atom concentration can be varied from about 0.2 to ~1 monolayer as determined by SIMS, by varying the ratio of N₂O to O₂ in the source gas mixture.

3.2 MOS capacitors and FITs with phosphorus-doped polycrystalline Si electrodes with oxides formed by remote PECVD and rapid thermal CVD

This comparison has established a functional equivalence between oxides deposited by remote PECVD at 300°C and rapid thermal CVD at 800°C, when used in devices with doped polycrystalline Si electrodes, which require processing temperatures to 900°C. Based on this comparison, the conclusion is that post-deposition annealing at 900°C during the ~30 minute POCl₃ doping process is sufficient to render both types of

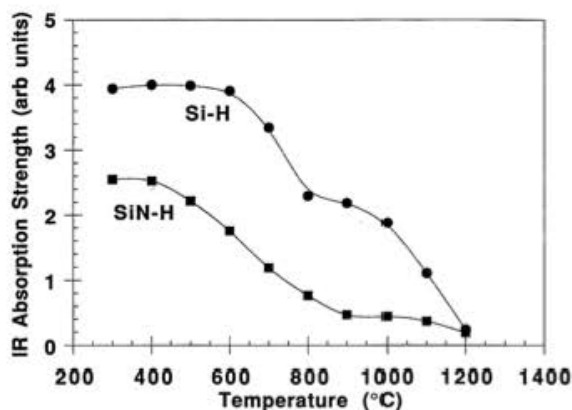


Fig. 3. IR absorption as a function of annealing temperature for Si-H and SiN-H bonds in a hydrogenated Si, N alloy film deposited from a source gas ratio $R=2$.

deposited oxides and their interfaces with Si, *indistinguishable* to the extent that fixed oxide charge (Q_f), and D_{it} levels are essentially the same; i.e., $Q_f < 10^{11} \text{ cm}^{-2}$ and $D_{it} \sim 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$.⁹⁾ This result has lead us to study the combination of 300°C plasma-assisted oxidation for Si-SiO₂ interface formation, and 800°C rapid thermal CVD for oxide deposition. Performance data for transistors is shown in Fig. 4, and supports the results on the electrical characteristics of MOS capacitors relative to the functional equivalence of the remote PECVD and rapid thermal CVD oxides after the 900°C thermal exposures used in doping of the gate electrodes and formation of the source and drain junctions.

3.3 MOS capacitors with Al contacts and rapid thermal CVD oxides⁷⁾

These studies confirmed that separate control of interface formation and film deposition via the integration of a plasma-assisted oxidation and rapid thermal CVD oxide deposition leads to better electrical properties than rapid thermal CVD deposition following an RCA clean with, or without a rinse in dilute HF. Note that when the plasma-assisted oxidation was not used, interface formation was not independently controlled during an *in-situ* process. Values of D_{it} for the MOS capacitors without the plasma-assisted oxidation were typically about 2–4 times higher, and the values of the flat-band voltages corresponded to fixed charge levels $> 10^{11} \text{ cm}^{-2}$, whereas the values of Q_f for the plasma-oxidized interfaces were typically $< 10^{11} \text{ cm}^{-2}$. The D_{it} and Q_f values for the devices with plasma-generated interfaces were essentially the same as those obtained for control devices that incorporated conventional furnace oxides.

3.4 FETs with doped polycrystalline Si gate electrodes and rapid thermal CVD oxides^{8–10)}

These comparisons for FETs reinforced the conclusions drawn in (iii) relative to pre-deposition treat-

ments. However, the plots Fig. 5 indicate a difference in performance with respect to FETs with thermally-grown oxides in the rate at which the channel mobility falls off with the electrical field at the Si surface of the channel region.

3.5 FETs with doped polycrystalline Si gate electrodes (900°C) and rapid thermal CVD oxides and 900–1000°C pre-deposition RTOs

These comparisons demonstrated that a process sequence which provides separate control for interface formation through a pre-deposition RTO step, and for oxide quality through a rapid thermal CVD deposition yields electrical performance that approaches that obtained for thermally-grown oxides. In particular, this includes a decreased rate of channel mobility fall off with the electrical field at the Si surface of the channel region (see Fig. 6).

Finally, studies to be reported elsewhere have shown that the rate of channel mobility fall off with electrical field at the Si surface of the channel region is strongly influenced by pre-deposition *ex-situ* surface cleaning. For example, there are differences in this fall off rate for FETs produced by a process sequence that includes: (i) a 300°C plasma-assisted oxidation, (ii) a 300°C remote PECVD oxide deposition, and (iii) a 900°C formation of doped polycrystalline gate electrodes, when different pre-deposition processes are employed. Specifically, the fall off rate is faster than for a thermal oxide, when a hot RCA clean is employed prior to the oxidation step, but these differences in fall-off rate are reduced significantly when a UV-ozone oxidation and rinse in dilute HF are substituted for the conventional RCA clean process.

4. Performance of Devices with Nitrogen-Containing Dielectrics

To illustrate the effect of different post-deposition processing temperatures on the performance of devices that include the 300°C remote PECVD nitrides in composite ON and ONO structures, we first discuss the per-

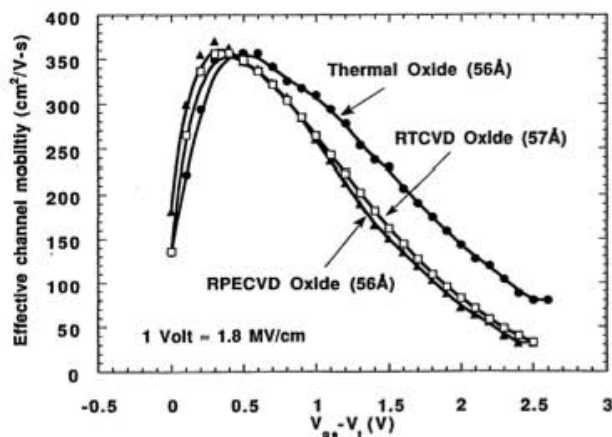


Fig. 4. Channel mobility as a function of the field at the Si surface potential of the channel material for FETs with ultra-thin oxides formed by thermal oxidation, remote PECVD (RPECVD) and rapid thermal CVD (RTCVD).

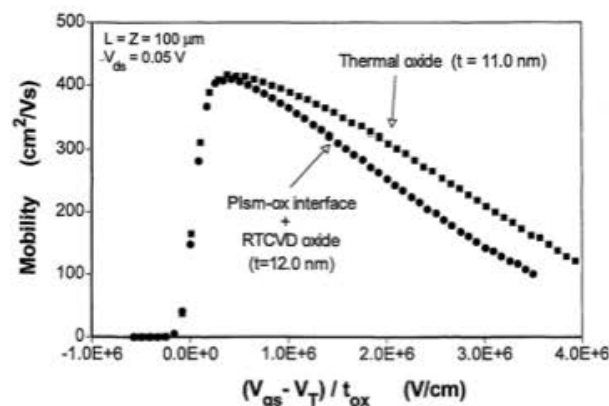


Fig. 5. Channel mobility as a function of the field at the Si surface potential of the channel material for FETs with ultra-thin oxides formed by thermal oxidation, remote PECVD (RPECVD) and rapid thermal CVD (RTCVD).

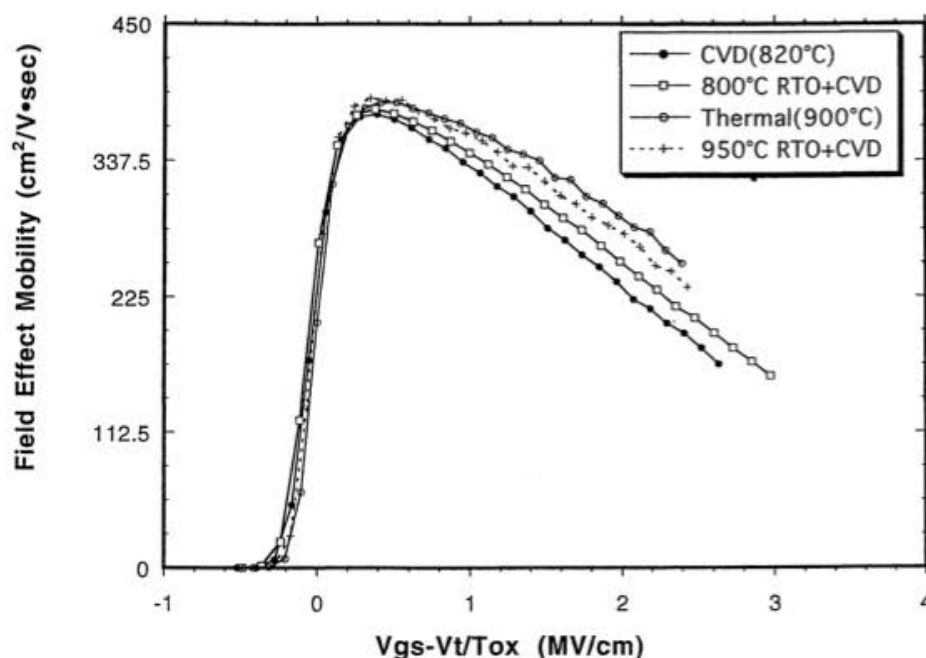


Fig. 6. Channel mobility as a function of the field at the Si surface potential of the channel material for FETs transistors in which the interface was formed by thermal and plasma-assisted oxidation processes.

formance of TFTs, processed at temperatures no higher than the deposition temperature of 300°C, and then the performance of metal-insulator-semiconductor (MIS) capacitors processed at temperatures in excess of the dielectric deposition temperature of 300°C.

4.1 Thin film transistors (TFTs)

Determinations of (i) the effective electron channel mobilities, and (ii) the threshold voltages for bottom gate a-Si TFTs as a function of R indicate that TFT performance is optimized for $R \sim 10$. This value of R is a flow ratio at which Si-Si bonds cannot be detected by AES, and where both Si-H and SiN-H bonds are detected, but where the SiN-H absorption is stronger than the Si-H (see Figs. 2(a) and 2(b)). TFTs were fabricated using a 300°C process that included: (i) sequential remote plasma enhanced CVD depositions of silicon oxide, silicon nitride, hydrogenated amorphous silicon (a-Si:H), and n^+ a-Si or n^+ microcrystalline Si (μ c-Si) onto a glass substrates with pre-deposited W-gate electrodes; (ii) deposition of Al onto the n^+ regions for the source and drain contacts; (iii) selective etching to define the TFT geometry (i.e., the channel, and the source and drain contacts); and (iv) formation of a thin Si oxynitride passivation layer over the exposed back portion of the channel.⁴⁾ In addition, note that (i) the back channel passivation step was essential to maximize the drive current, which corresponded to an electron channel mobility of $\sim 1.5 \text{ cm}^2/\text{V}\cdot\text{s}$; and (ii) the threshold voltage was reduced from $>2 \text{ V}$ to values of $\sim 1\text{--}1.5 \text{ V}$ by substituting $n^+ \mu$ c-Si for n^+ a-Si source and drain contacts. The $n^+ \mu$ c-Si material is about 3–4 orders of more conducting than the n^+ a-Si. The properties of these a-Si:H TFTs are at, or above the manufac-

turing state of the art for flat panel displays. Further increases in the TFT drive current, corresponding to channel mobilities up to $\sim 6.5 \text{ cm}^2/\text{V}\cdot\text{s}$, have been achieved by substituting B-compensated, quasi-intrinsic μ c-Si for a-Si:H for the channel material;⁵⁾ however, as with polycrystalline Si TFTs, this increase in drive current is accomplished at the expense of a reduced $I_{\text{on}}/I_{\text{off}}$ ratio, from at least $10^8:1$ to $\sim 10^6\text{--}10^5:1$.

4.2 MIS capacitors

Figures 7(a) and 7(b), respectively, display D_{it} and V_{fb} plots for MIS capacitors with ONO dielectrics (all layers $\sim 5 \text{ nm}$ thick). The as-deposited values for D_{it} are higher than for MOS capacitors with deposited oxides even though both types of devices have been subjected to exactly the same processing temperatures: 300°C for the oxidation and deposition steps, and 400°C for the PMAs. In addition, the flatband shifts (V_{fb}) are significantly more negative in the MIS devices, indicating a higher concentration of trapped positive charge (Q_{f}) in the vicinity of the Si-SiO₂ interface. However, after a 30 s 900°C RTA in Ar with a partial pressure of O₂ sufficient to prevent formation and evolution of gaseous SiO at the Si-SiO₂ interface, (i) the values of D_{it} approach those of devices with oxide dielectrics; whilst (ii) the values of Q_{f} are still about a factor of 2–3 higher than for homogeneous plasma-deposited oxides. The best electrical performance after the RTAs is obtained for values of R of ~ 8 to 10, essentially the same R values as for optimized performance in the a-Si TFTs. Breakdown fields (E_{b}) are typically in excess of 10 MV/cm, both before and after the 900°C RTAs. MIS devices with ONO dielectrics having oxide equivalent thicknesses in the range of 4.5 to 6.0 nm

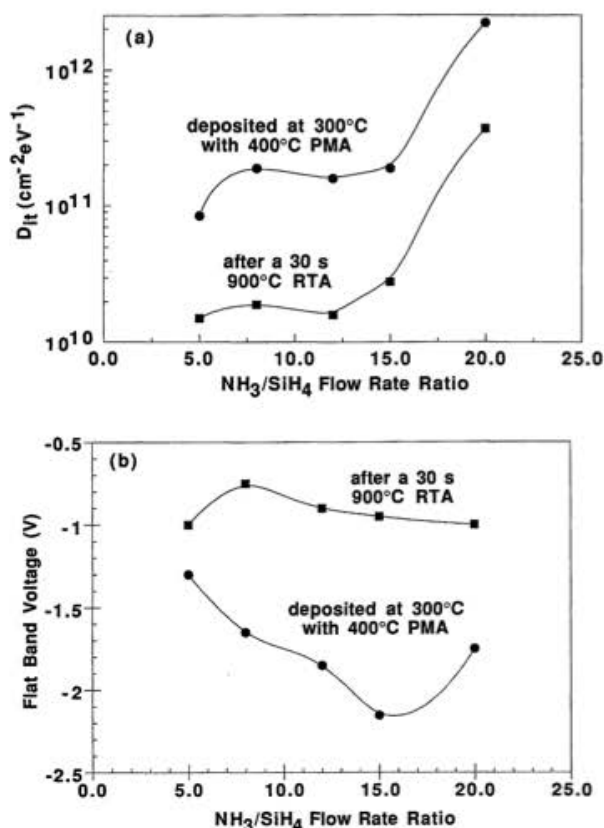


Fig. 7. (a) D_{it} at mid-gap and (b) flat band voltage (V_{fb}) as a functions of the NH_3/SiH_4 flow ratio for MIS capacitors with ONO dielectrics (i) deposited at 300°C and subjected to a 400°C PMA and (ii) subjected to a 30 s 900°C before metallization and a 400°C PMA.

have also been fabricated. The electrical properties of these devices; *e.g.*, V_{fb} , D_{it} and E_b , are essentially the same as those discussed above and displayed in Figs. 7(a) and 7(b). Finally, Figs. 8(a) and 8(b) indicate similar behaviors for MIS devices with oxynitride dielectrics deposited at 300°C. Note that there is also a significant improvement in electrical performance after a 30 s 900°C RTA. The MIS devices with oxynitride dielectrics, also include a Si-SiO₂ interface that is formed by the 300°C plasma-assisted oxidation process.

5. Discussion

5.1 H-evolution from nitride films

The differences in the processing requirements for optimized electrical performance in TFTs and MIS devices are explained by combining the temperature dependent IR absorption results of Fig. 3 with the results of the device studies. This explanation is based on an assumption (supported by the IR and the device data) that release of bonded-H at temperatures between 400 and 800°C results in defect generation via the creation of Si and/or N-atom dangling bond defects, and that these defects are annealed at higher temperatures ~900°C. In this model, the achievement of optimized performance in TFTs, where the post-deposition proc-

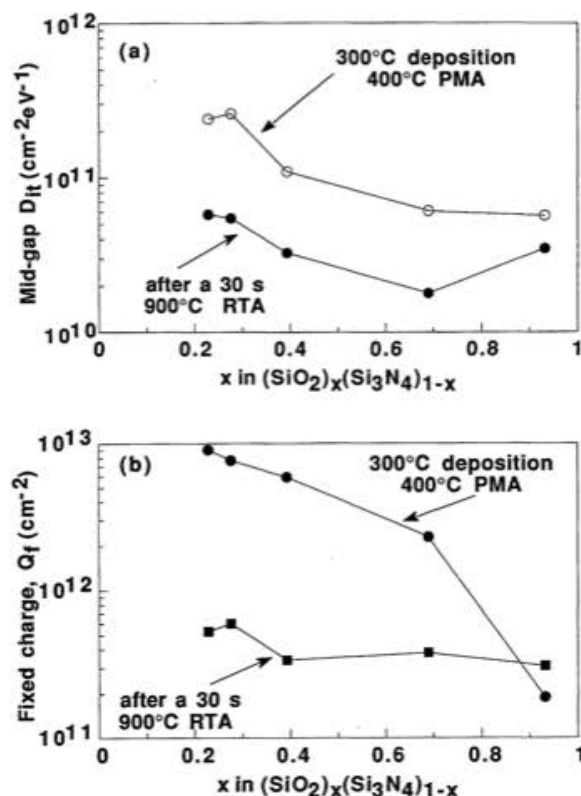


Fig. 8. (a) D_{it} at mid-gap and (b) Q_f as determined from V_{fb} for MIS capacitors with oxynitride dielectrics (i) deposited at 300°C and subjected to a 400°C PMA and (ii) subjected to a 30 s 900°C before metallization and a 400°C PMA.

essing temperatures are no higher than the 300°C deposition temperatures, also correlates with the IR results which indicate that 300°C is below the threshold for detectable H-atom release from the Si-H and SiN-H sites. In contrast, the MIS structures with Al electrodes require a PMA at 400–450°C, a temperature range in which there is measurable release of H-atoms from the Si-H bonding sites (see Fig. 3). The fact that IR absorptions for both bonding groups decrease together over most of the temperature range between 450°C and 1000°C studied suggests the release of H from these sites is a cooperative phenomenon involving for example the generation of H₂ molecules. This would have to be the case considering the high bond energies of ~3.4 and 4.1 eV, respectively, for H-attachment in the Si-N and SiN-H groups.

Figure 9 indicates a bonding model that shows how this defect generation and subsequent annealing process can proceed. Figure 9(a) indicates a region of the nitride film that contains near-neighbor Si-H and SiN-H groups prior to thermally-generated H-release. The close proximity of these bonding groups is consistent with constraints imposed by network topology. For Fig. 9(d), the temperature has been raised sufficiently (*e.g.*, to 500°C to 800°C) to promote H-atom release from both bonding sites creating two dangling bonds, and an H₂ molecule that eventually evolves out of the material.⁷⁾ In Fig. 9(e), the temperature has been raised

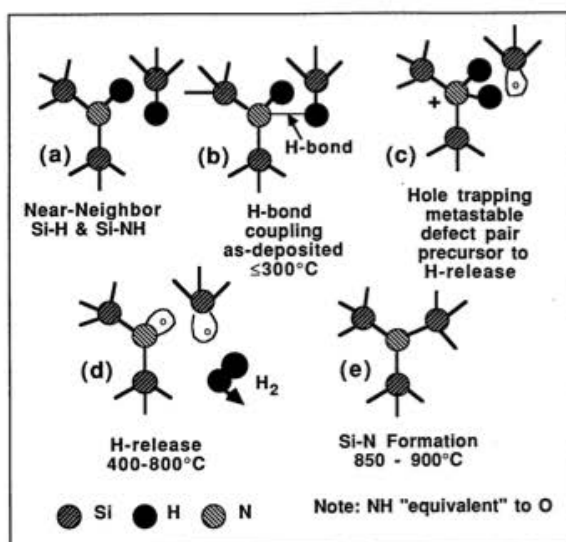
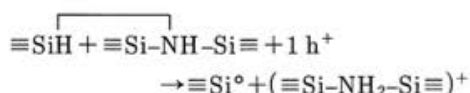


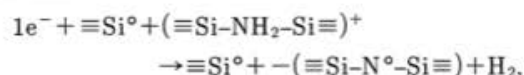
Fig. 9. Bonding model for H_2 evolution from near-neighbor Si-N and SiN-H groups.

still further to a regime where atomic relaxations can occur (*e.g.*, to 900°C), and the near neighbor Si-atom and N-atom dangling bonds can combine to produce an additional Si-N bond, which is detected in the IR measurements. This is the aspect of the 900°C RTA that then serves to eliminate the electrically-active bonding defects produced by the H-evolution that occurs during the PMA step. Other studies that we have performed indicate that it is likely that there is a precursor state to this cooperative H_2 release, and this is illustrated in Fig. 9(c). This portion of the figure illustrates an *intimate valence alternation pair* is created via the trapping of a hole, following a mechanism that has been proposed for the Staebler-Wronski effect in a-Si, N:H alloys prepared from NH_3 .⁸⁾ The model in ref. 8 is based on the observation that near-neighbor Si-H and SiN-H groups are invariably linked through the H-bonding interaction shown in Fig. 9(b). This is simply a manifestation of their close proximity in the solid state, and the availability of participating orbitals on the N-atom of the N-H group. Trapping of a thermally released hole at this center will result in the production of a defect pair (a Si-atom dangling bond, and a positively-charged ammonium center) as shown in Fig. 9(c), and is represented by the reaction equation presented below:



where $\equiv\text{Si}^\circ$ denotes a Si-atom dangling bond. In a-Si, N:H this reaction can be reversed by trapping of a thermally-released electron during a low temperature anneal at $175\text{--}200^\circ\text{C}$; the activation energy for this process is $\sim 0.85\text{--}0.9\text{ eV}$ consistent with a mid-gap Fermi level position in the light-soaked a-Si:H. In contrast, for the hydrogenated silicon nitride films, heating the material to temperatures in excess of 400°C is

sufficient to release H_2 molecules, where the release process may also involve trapping of a thermally-generated electron at the $(\equiv\text{Si-NH}_2\text{-Si}\equiv)^+$ center as an intermediate step in the process, which is then followed by creation and evolution of an H_2 molecule. A mechanism whereby hole trapping initiates the formation of a metastable center, and trapping of an electron plays a role in the release of bonded-H would then help to account for the energy balance necessary for the H-evolution process to proceed. The equations presented below indicate the final two steps of the proposed intermediate steps in this process of H_2 evolution, and eventual bond healing of the Si-atom and N-atom dangling bond defects:



and



Studies of nitride films prepared from deuterated ammonia (ND_3) are currently underway. Nitride films prepared from ND_3 and SiH_4 contain SiN-D groups, as well as Si-H and Si-D groups, so that evolution of HD species from films prepared in this way would reinforce the proposed model.

5.2 Defects at the Si-SiO₂ interface

The results reported in this paper regarding N-atom build-up at the Si-SiO₂ interface resulting from a pre-deposition oxidation in N_2O , seemed initially to be conflict with other studies we reported in which N-atom build-up resulting from processing with plasma-activated NH_3 yielded significantly increased levels of interfacial defects.⁷⁾ The N-atom concentrations at the Si-SiO₂ interface for the pre-oxidation with N_2O , and after processing with NH_3 were comparable as determined from AES measurements; however, for processing steps that utilized plasma-excited NH_3 , the active N-species migrating to the Si-SiO₂ interface is NH rather than N. These observations have lead us to conclude that (i) N-atom incorporation at the interface can maintain levels of D_{it} comparable to interfaces with O-atoms, whilst (ii) NH groups, generated in plasma processing of NH_3 , promote significantly increased levels of D_{it} . We propose that these differences are due to aspects of the local bonding arrangements that involve H-bond formation;¹⁴⁾ that bonding configurations which include H-bonds as in parts (a) and (b) of Fig. 10, are precursor sites for defect formation. The arrangements in Fig. 10(a) can occur at Si-SiO₂ interfaces in the absence of any N-atom bonding. For Si-SiO₂ interfaces that include N-atoms, H-bond formation that involves N-atoms is when (i) NH groups bridge Si-atoms (as in Si-NH-Si linkages), and are also in close proximity to Si-H groups, but not when (ii) N atoms are bonded only to Si-atoms, even if these N-atoms are also in close proximity to Si-H bonds at Si-SiO₂ interfaces. These differences in N-atom bonding arrangements are a

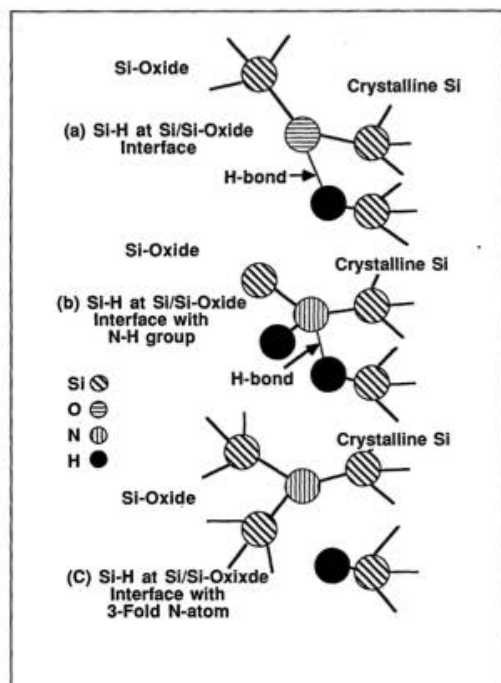


Fig. 10. Bonding at Si-SiO₂ interfaces. H-bonds are formed between the H-atoms of Si-H groups and (a) O-atoms and (b) NH groups (b), but not between H-atoms of Si-H groups and (c) N-atoms.

manifestation of the different symmetries of the non-bonding pair on the N-atoms which are in (i) a planar configuration for a N-atom with three-Si neighbors and (ii) an approximate tetrahedral arrangement for an NH group that bridges two Si atoms. In bonding arrangement (i), a back donation from the non-bonding pairs on the N-atoms to the three Si-neighbors forces the planar geometry, eliminating a concentrated negative charge distribution in a specific direction that promotes the H-bonding interactions, whilst in (ii) the nearly tetrahedral arrangement concentrates the negative charge of the non-bonding pair in a specific direction that can promote H-bonding interactions with the N-atom of that group. Alternatively, the H-atom of the N-H group can also participate in H-bonding interactions with near-neighbor O-atoms of the SiO₂ material. A specific model for metastable defect formation involving H-bonding arrangements at Si-SiO₂ interfaces that include N, and NH groups will be presented elsewhere.¹⁵⁾

6. Discussion

The combination of experimental results discussed above establishes that three processing steps are essential for the fabrication of FETs with deposited oxides in order for their electrical properties to be equivalent to those of state of the art FETs with thermally-grown oxides. These are (i) an oxide deposition process that yields a stoichiometric oxide; (ii) distinct and separately controllable processes for Si-SiO₂ interface formation and oxide deposition; (iii) relaxation of the Si-SiO₂ structure at elevated temperatures, $\sim 900^\circ\text{C}$ for at

least 30 s. The properties of the remote PECVD and rapid thermal CVD oxides are essentially the same if both are subjected to a 900°C anneal during the gate electrode doping process; however, it is not possible to perform plasma-assisted depositions and rapid thermal processes (RTP) in the same chamber due to the fact that plasma-assisted deposition occurs not only on the film substrate, but also on chamber walls and fixtures, including the optical access windows required for RTP processing. This then allows for two processing options that combine plasma and rapid thermal processing in a single chamber: (i) the combination of the 300°C plasma-oxidation, and the 800°C oxide deposition by rapid thermal CVD; and (ii) the combination of the 300°C plasma-assisted oxidation and remote PECVD steps. In either instance, an exposure to a temperature of 900°C for at least 30 s is required to optimize electrical properties.

As noted above, the properties of FETs formed in this way will not be completely equivalent to those of FETs employing thermally-grown oxides with regard to the rate of channel mobility fall off as a function of the field at the Si-surface of the channel region if the pre-oxidation process is a conventional hot RCA clean that is terminated by a rinse in dilute HF. On the other hand, substitution of a UV/O₃ clean and rinse in dilute HE can remedy this deficiency in performance.¹⁰⁾ Alternatively, a higher thermal budget process that includes (i) a pre-deposition RTO to form the Si-SiO₂ interface and a thin oxide that serves as a platform for subsequent oxide deposition, and (ii) a rapid thermal CVD oxide deposition also produces performance equivalent to FETs with thermally grown oxides. If it becomes necessary to use oxynitride alloys and/or ONO structures, then remote PECVD deposition must be considered as a potentially important processing option in light of the high-quality oxynitride and ONO dielectrics that have been formed by the combination of (i) a 300°C plasma-assisted oxidation; (ii) remote PECVD 300°C film depositions; and (iii) the 30 s, 900°C RTA.^{4,5)} These processes can also be combined with *ex-situ* process that uses a UV/O₃ clean and a rinse in dilute HF in place of the hot RCA clean and rinse in dilute HE that has been discussed above.

Additional device studies are necessary to fully evaluate the potential of deposited dielectrics. These include studies of FET performance for devices that include oxynitride and/or nitride layers, as well as studies of FET reliability for all of the various processing alternatives discussed above.

In summary, each of the processing alternatives identified above includes three distinct *in-situ* process steps that can be independently controlled, and that impact on the device performance. These are (i) the formation of the Si-SiO₂ interface (by either plasma-assisted oxidation, or a pre-deposition RTO step); (ii) the deposition of a single layer oxide dielectric by either remote PECVD or rapid thermal CVD, or a multi-layer dielectric by remote PECVD; and (iii) post-deposition thermal annealing for at least 30 s at a temperature of 900°C . The important points to note here are that

these three process steps can be accomplished at a significantly reduced thermal budget as compared to conventional processing techniques including rapid thermal oxidation, thermal nitridation, and thermal re-oxidation. The device properties so far explored indicate that performance levels comparable to those obtained by conventional processing approaches, such as those identified above, can then be achieved at significantly reduced thermal budgets (for example, see Table I of ref. 16).

Acknowledgments

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