

In the Matter Of:

Micron Technology vs

Besang Inc.

STEVEN PRZYBYLSKI

April 05, 2024



1 UNITED STATES PATENT AND TRADEMARK OFFICE
2 BEFORE THE PATENT TRIAL AND APPEALS BOARD

3

4 IN RE MATTER OF:)

5 MICRON TECHNOLOGY, INC.;)

6 MICRON SEMICONDUCTOR PRODUCTS,)

7 INC.; and MICRON TECHNOLOGY)

8 TEXAS, LLC)

9)

10 Petitioner,)

11 vs.)

12)

13 BESANG INC.,)

14)

15 Patent Owner.)

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CASE NO. IPR2023-00900

14 VIDEOTAPED DEPOSITION OF DR. STEVEN A. PRZYBYLSKI

15 NEWPORT BEACH, CALIFORNIA

16 Friday, April 5, 2024

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20 Stenographically Reported by:

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23 California CSR License #11600

24 Oregon CSR License #21-0005

25 Washington License #21009491

Nevada CCR License #980

Texas CSR License #10725

Job No. 2024-931405

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UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEALS BOARD

IN RE MATTER OF:	)	
	)	
MICRON TECHNOLOGY, INC.;	)	
MICRON SEMICONDUCTOR PRODUCTS,	)	
INC.; and MICRON TECHNOLOGY	)	
TEXAS, LLC	)	
	)	
Petitioner,	)	
	)	
vs.	)	CASE NO. IPR2023-00900
	)	
BESANG INC.,	)	
	)	
Patent Owner.	)	
	)	

VIDEOTAPED DEPOSITION of DR. STEVEN A.
PRZYBYLSKI, taken before Heather J. Bautista, CSR No.
11600, a Certified Shorthand Reporter for the state of
California, with principal office in the county of Santa
Clara, commencing on Friday, April 5, 2024, 9:01 a.m.,
at 4685 MacArthur Court, Suite 390, Newport Beach,
California 92660.

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1 Friday, April 5, 2024

2 9:01 a.m.

3 --oOo--

4 THE VIDEOGRAPHER: We are now on the record.

5 My name is Saxon Christin. I'm the videographer
6 representing Lexitas. This is the video deposition for
7 the United States Patent and Trademark Office before the
8 Patent Trial and Appeal Board. Today's date is April
9 5th, 2024. The time is 9:01 a.m.

10 This deposition is being held at 4685 MacArthur
11 Court, Suite 390, Newport Beach, California 92660 in the
12 matter of Micron Technology, Inc. et al., versus BeSang,
13 Inc. The case number is IPR2023-00900. The deponent is
14 Dr. Steven A. Przybylski.

15 Would all counsel please identify yourselves
16 for the record.

17 MR. KAPPOS: John Kappos of O'Melveny & Myers
18 representing Petitioner Micron Entities.

19 And with me by telephone is Patric Reinbold of
20 O'Melveny and Myers and Jan Bissey of Micron's in-house
21 legal department.

22 MS. ARMOND: Michelle Armond of Armond Wilson
23 representing Patent Owner BeSang and the witness.

24 MR. ZHOU: Xu Zhou from Caldwell Cassady &
25 Curry representing BeSang.

1 THE VIDEOGRAPHER: Thank you, Counsel.

2 The court reporter is -- is Heather Bautista
3 and will now swear in the witness.

4 THE STENOGRAPHER: Good morning.

5 My name is Heather Bautista, and I am a
6 certified stenographer licensed by the State of
7 California. My license number is 11600.

8 This deposition and any transcript produced
9 therefrom will be handled pursuant to Federal Rule of
10 Civil Procedure Section 30.

11 As the deposition officer, I will be retaining
12 my duties and responsibilities under the Code.

13 Please raise your right hand so I can swear you
14 in.

15 DR. STEVEN A. PRZYBYLSKI,
16 having been first duly sworn, was examined and testified
17 as follows:

18 THE WITNESS: I do.

19 THE STENOGRAPHER: Thank you.

20 Please state your full name for the record.

21 THE WITNESS: Steven Alan Przybylski.

22 THE STENOGRAPHER: Thank you.

23 Counsel, you can begin.

24 ///

25 ///

DIRECT EXAMINATION

BY MR. KAPPOS:

Q. Dr. Przybylski, where do you currently work?

A. Ann Arbor, Michigan.

Q. And what's the name of your business?

A. Verdande Group Incorporated.

Q. What's the address of Verdande Group?

A. 5630 Meadow Lane, Ann Arbor, Michigan.

Q. And what is your occupation?

A. I'm a consultant.

Q. Are you a professional expert witness?

A. I don't call myself a professional expert witness, although I do do litigation support as part of my consulting practice.

Q. About how many times have you testified as an expert witness?

A. By deposition, about 15 or 20, in that range.

Q. Is there any reason you cannot give truthful testimony today?

A. No.

MR. KAPPOS: I'm going to hand you a copy of Exhibit 2029.

MS. ARMOND: John, the witness has a copy of that in front of him.

Q. (By Mr. Kappos) And I'm fine if you want to

1 use your copy or my copy, whichever you prefer. The
2 copy that you have in front of you, does it have any
3 notes in it?

4 A. Not at all. Clean copy.

5 Q. Okay. All right.

6 You can use either one, as I said.

7 Can you please confirm that this is your
8 declaration filed in this matter.

9 A. Yes, I can confirm that. Let me make sure your
10 copy is identical to mine, but it appears to be. Yes.

11 Q. Are there any corrections that you wish to
12 make?

13 A. Not at this time.

14 Q. Who drafted your declaration?

15 A. I drafted the first draft of my declaration.

16 Q. What role did counsel play in that?

17 A. Counsel and I worked collaboratively to produce
18 the final declaration after my initial draft. Prior to
19 that, there were discussions as to --

20 MS. ARMOND: I would just like to caution the
21 witness not to reveal any attorney-client privilege
22 communications in your response.

23 THE WITNESS: Thank you.

24 Prior to that, we -- we worked together to
25 understand the nature of the matter and allowed me to go

1 off and -- and formulate my opinions.

2 Q. (By Mr. Kappos) Okay.

3 I'm handing you a document that's been marked
4 as Exhibit 2-0-3-0, so 2030. Do you recognize this
5 as your curriculum vitae that was attached to your
6 declaration in this matter?

7 A. Yes, I do.

8 Q. Your CV indicates that you provide litigation
9 support services in PTAB cases; is that correct?

10 A. I am doing so now, and I have done so in the
11 past.

12 Q. Approximately how many PTAB cases have you
13 testified in?

14 A. I don't know the exact number. It's
15 probably -- more than ten, certainly. I don't know how
16 much more.

17 Q. And out of that number, how many times did you
18 testify for the patent owner?

19 A. I don't have any specific recollection on what
20 the mix is between patent owner and -- and petitioner.

21 Q. Do you recall how many times you've testified
22 for the petitioner?

23 A. No, I don't.

24 Q. Have you ever testified for a petitioner?

25 A. I don't recall any specific instances, but

1 there may have been one. I don't know.

2 Q. And so you've always reached the conclusion
3 that the challenged patent is valid; is that correct?

4 A. For the cases that I have -- I'm sorry. Would
5 you repeat the question.

6 Q. You've always reached the conclusion that the
7 challenged patent is valid; is that correct?

8 A. No.

9 Q. In what case did you testify that the patent
10 was not valid?

11 A. I don't recall any formal opinions that a
12 patent is not valid. There are certainly been cases
13 where individual claims have been defended and not
14 others so that I've had no opinion on other -- whether
15 claims that I did not opine on were valid or invalid.

16 Q. Looking at your CV, you mention NAND in Other
17 Articles on Page 3. I think it's the second article
18 that's listed.

19 A. Yes.

20 Q. I didn't find any other mention of NAND in your
21 CV. Do you recall that I might have missed any?

22 A. Certainly with regard to the professional
23 experience, the first item under Verdande Group, it
24 lists the various topics that I have been involved in,
25 and one of the categories in -- under the Semiconductor

1 column is Flash and that includes NAND flash. So there
2 have been at least several cases that involved NAND
3 flash as the principal technology at issue.

4 Q. So going back to the Other Articles on Page 3,
5 the title refers to NAND Flash Architecture; correct?

6 A. The title of that article is "Hyperlink NAND
7 Flash Architecture for Mass Storage Applications."

8 Q. And so that article is about circuit design;
9 correct?

10 A. I don't remember exactly what is in that
11 article. It was written quite a long time ago, so I
12 don't know if it was -- it certainly was about
13 architecture that indicates the -- as indicated by the
14 title, but the detailed subject matter, you would have
15 to put it in front of me to refresh my memory.

16 Q. The fact that the title mentions architecture
17 indicates that the article was about circuit design, as
18 opposed to fabrication processes for memory cells;
19 correct?

20 A. Again, I don't remember the content of that
21 article in detail, so I can't say whether or not
22 fabrication methods and methodologies are addressed in
23 any -- to any degree in that article.

24 Q. Do you recall whether that article was about 2D
25 NAND or 3D NAND?

13

1 A. Again, it was a while ago, and I don't remember
2 the contents of the article, and so I can't answer that
3 question with any certainty.

4 Q. Given the date of August 2007, does that help
5 you answer that question?

6 A. Again, I don't remember the content of that
7 article, and so I can't answer that question with any
8 certainty.

9 Q. So going back to Page 1 under Semiconductor
10 Services for which you retained -- were retained, it
11 says "Flash." Do you see that on the right side?

12 A. Yes, I do.

13 Q. Was that a case -- or what was the nature of
14 that matter?

15 A. As I indicated, there have been several matters
16 related to flash memory over time. One in particular
17 that I remember was related to circuit design and
18 internal architecture of a NAND flash memory.

19 Q. Does the term "architecture," as you just used
20 it, does that typically refer to circuit design?

21 A. My understanding -- and this is not necessarily
22 uniformly used across the industry, but my understanding
23 is that circuit design is a lower level -- level of
24 abstraction than architecture.

25 Q. As you used the term "circuit design," are you

1 focused more -- I'm sorry. Let me start over.

2 As you use the term "architecture," are you
3 more focused on circuit design or memory cell
4 fabrication?

5 A. Memory cell fabrication is another area of art
6 within the general topic of semiconductor design and
7 manufacture separate from, but closely related to, both
8 circuit design and architecture; so they -- all three of
9 those are distinct, yet closely coupled.

10 Q. And the matter -- so you said the matter that
11 you recall that's listed as "Flash" under Retained
12 Experience at the top of Page 1 of your CV, which is
13 Exhibit 2030, do you recall whether that was a
14 litigation? What was the nature of that?

15 MS. ARMOND: I'd like to caution the witness
16 not to reveal any confidential information that you may
17 not be at -- you know, able to speak about.

18 THE WITNESS: Thank you.

19 I'm sorry. Please repeat the question.

20 (Record read.)

21 THE WITNESS: I believe I testified previously
22 that the "Flash" item under semiconductors refers to a
23 number of different matters relating to flash. Then
24 subsequently, I identified one in particular that I
25 remembered. And that one in particular that I was

15

1 referring to in my previous answer was a district court
2 case, if I remember correctly.

3 Q. (By Mr. Kappos) Do you remember what case or
4 who were the parties involved in that district court
5 case?

6 A. I -- my recollection is only that I was
7 retained indirectly for --

8 (Stenographer clarification.)

9 THE WITNESS: -- Hyundai, H-y-u-n-d-a-i.

10 Beyond that, I don't remember who the other
11 party was.

12 Q. (By Mr. Kappos) What type of flash memory was
13 involved in that case?

14 A. That case involved both DRAMs and flashes in
15 different aspects, and the flash memory that I was
16 analyzing was a NAND flash memory.

17 Q. Do you recall whether it was 2D NAND or 3D
18 NAND?

19 A. I believe it was 2D, but, again, it was a long
20 time ago. I don't remember specifically.

21 Q. And do you recall whether that matter -- that
22 case was focused on circuit design, as opposed to
23 fabrication of memory cells?

24 A. What I do remember of my involvement with that
25 case was that it relate -- my principal activity was

1 related to circuit design. I do not recall whether
2 there was a semiconductor fabrication aspect to the case
3 that I may have been directly or tangentially involved
4 in.

5 Q. And I think earlier you referred to -- Page 1,
6 the entry at the bottom that says "President and
7 Principal Consultant" and this is the Verdande Group
8 reference on your CV?

9 A. Correct.

10 Q. So it states there that you consulted on system
11 level design in the area of flash. What type of flash
12 memory was involved in that matter?

13 A. The period -- the -- let me start again.

14 The item on the bottom of Page 1 of my CV
15 relating to the time period 1991 to 2000 was principally
16 a technical consulting, not a litigation support, so
17 there was no matter as the term is typically used in
18 these environments, at least not that I recall. There
19 may have been. But principally, that -- during that
20 time frame I was doing technical and business
21 consulting.

22 Q. So in that technical and business consulting
23 that you did on flash memory, do you recall whether it
24 was NAND flash or some other type of flash?

25 A. That would have been -- I don't have any

17

1 specific recollection for a client engagement that --
2 that would allow me to differentiate whether it was NOR
3 or NAND or both or -- but I was providing general
4 consulting services relating to the application of
5 memories generally in systems and the design of those
6 memories; so they may have included EPROM, EEPROM, NOR
7 flash. I don't have any specific recollection for that
8 older period of time.

9 Q. Did that matter involve circuit design, as
10 opposed to fabrication of memory cells?

11 A. Again, for that previous period, 1991 to 2000,
12 I don't have a specific recollection of an engagement
13 that I can describe to you in detail that -- but in
14 general, the -- my -- the focus of my consulting
15 practice during that time frame was the design at a
16 circuit level and architecture of memory devices and the
17 use of those memory devices in systems.

18 My knowledge and familiarity, fluency, in the
19 fabrication of those devices was a necessary precursor,
20 in my mind, to being able to help my clients understand
21 the problems facing them, regardless of whether I was
22 actually involved in developing a fabrication process.

23 Q. Do you have any experience with 3D NAND?

24 A. I certainly have a great deal of knowledge
25 about 3D NAND, how it's fabricated, how it's -- how it

18

1 operates internally and how it's used in systems.

2 I'm not quite sure what you mean by experience
3 in your question.

4 Q. Do you have any experience with the fabrication
5 of memory cells?

6 A. Again, I know a great deal about how they're
7 fabricated. I've been in clean rooms. I've never been,
8 you know, on a manufacturing line employed to operate
9 the machinery, if that's what you're asking.

10 Q. No, I'm not asking about operating machinery.
11 I'm asking whether you've ever been consulted or had
12 direct involvement in the development of fabrication of
13 memory cells.

14 A. I don't recall any specific technical or
15 business clients that involved the fabrication of the
16 development of semiconductor manufacturing processes at
17 the level that you're describing. My involvements
18 required understanding those things but not necessarily
19 participating in their development.

20 Again, there have been many clients over the
21 years, and I can't articulate any specific one, that may
22 have been closer to what you're asking about.

23 Q. And would your answer be the same if I asked
24 about your experience with the fabrication of 3D NAND
25 memory cells?

19

1 A. Yes. I don't have any specific recollection of
2 an involvement at a detailed level of the development of
3 semiconductor manufacturing processes for 3D NAND flash.

4 Q. Other than the one paper that we looked at
5 that's listed in your CV that mentions NAND, have you
6 published any papers on NAND memory?

7 A. I haven't done very much publication for the
8 last couple of decades, over which most of my consulting
9 and litigation support services relating to NAND flash
10 have occurred. So there -- I'm not -- I don't remember
11 whether any of these papers reference indirectly NAND
12 flash. I do know that the -- couple of my patents do
13 relate to memory systems involving NAND flash.

14 Q. Have you taught any courses on NAND flash
15 memory cells?

16 Let me withdraw that. Let me ask it
17 differently.

18 Have you taught any courses on NAND flash
19 memory?

20 A. At least in part, yes.

21 Q. What courses have you taught on NAND flash
22 memory?

23 A. I have taught -- on Page 4 of my CV, Exhibit
24 2030, under Seminars, Tutorials, and Session Chairs, the
25 second item there is "An introduction to semiconductor

1 memories" that I presented in Taiwan to a variety of --
2 of industry professional and managers; and that covered
3 all varieties of memories, including NAND flash as it
4 existed at that time.

5 Q. That entry that you pointed to says "in
6 cooperation with Citibank." Was that -- was that more
7 of an economic analysis of semiconductor memory, or was
8 it a technical course that you taught?

9 A. It was a technical course. It was an -- the
10 audience ranged from laypeople in the financial sector
11 through engineers and managers from the various
12 electronics companies in Taiwan that sent their
13 employees to this session. I mentioned Citibank,
14 because they were the organizers of this -- this
15 seminar.

16 Q. Is that the only course that you recall that
17 concerned NAND flash memory?

18 A. I believe -- my recollection -- it's vague, but
19 my recollection is that the full-day tutorial I taught
20 with Norman Jouppi and Mark Horowitz at the ISSCC in
21 1993, it's the third to last item in the Seminars,
22 Tutorials, and Session Chairs section of my CV, that
23 that course taught -- touched on a variety of memory
24 device types and memory architecture -- I'm sorry --
25 memory system architecture issues and that flash or

1 non-volatile memories generally were considered -- were
2 part of the subject matter of my portion of that
3 presentation.

4 Q. Those are the only two courses that you recall
5 from this list that had something to do with NAND flash?

6 A. Those are the only two in this list that I can
7 recall. There may have been other in-house tutorials
8 and seminars that I gave to clients that may have
9 touched on NAND flash to some degree. I don't recall,
10 and I did not list all of the proprietary in-house
11 presentations that I gave.

12 Q. The two that you mentioned here, the one in
13 1993 and the other one in 1998, those did not relate to
14 three-dimensional NAND; correct?

15 MS. ARMOND: Misstates prior testimony.

16 THE WITNESS: I don't have a specific
17 recollection of whether there was any 3D component to
18 those presentations. It seems unlikely, but I don't
19 recall.

20 Q. (By Mr. Kappos) And of all the presentations
21 that are not listed, did any of those concern 3D NAND?

22 MS. ARMOND: Again, I would like to caution the
23 witness that to the extent the question calls for
24 confidential consulting matters that you're not at
25 liberty to disclose, you should exclude that from

1 your answer.

2 Q. (By Mr. Kappos) Yeah, that's just a yes-or-no
3 question, so it shouldn't -- I'm not asking for any of
4 the information that you talked about. I'm just asking
5 you to confirm that none of those had anything to do
6 with 3D NAND; is that correct?

7 MS. ARMOND: Same instruction.

8 THE WITNESS: I don't recall specifically each
9 and every one of those presentations and what the
10 subject matter of them was. I don't recall any
11 specifically that do meet your criteria, but I can't say
12 for certain --

13 (Stenographer clarification.)

14 THE WITNESS: -- one way or the other. I think
15 that's what I said.

16 (Stenographer clarification.)

17 Q. (By Mr. Kappos) So you don't recall any
18 presentation that you've given specifically that
19 concerns 3D NAND; correct?

20 MS. ARMOND: Misstates prior testimony.

21 MR. KAPPOS: And, Counsel, I would caution you
22 to stick to "form of the question" because I don't think
23 you're supposed to make speaking objections.

24 MS. ARMOND: That's not a form-of-the-question
25 objection.

1 THE WITNESS: Please repeat the question.

2 (Record read.)

3 THE WITNESS: That's correct. I don't recall
4 any specifically, but there may have been some. I don't
5 know.

6 Q. (By Mr. Kappos) Have you received any awards
7 related to work that you've done on 3D NAND memory?

8 A. No. The awards that are listed in the Honors
9 and Publications section of my CV were not related to
10 NAND flash memory. And I don't recall any others that
11 might have been.

12 Q. Do you -- have you ever had occasion to referee
13 any journals?

14 A. I have referee -- I have been a referee for
15 journals and conferences in the past, but not much --
16 not recently.

17 Q. Have you refereed any journal articles directed
18 to 3D NAND flash memory?

19 A. Again, I haven't done refereeing of papers or
20 conferences for a long time, and I don't recall the
21 nature of the subject matter of the papers that I
22 reviewed. It's unlikely that any of those referred to
23 3D NAND flash memory.

24 Q. Do you recall whether any of those articles
25 that you refereed were directed to NAND flash memory?

1 MS. ARMOND: Asked and answered.

2 THE WITNESS: Is that the same question?

3 Q. (By Mr. Kappos) No. I left 3D out. Let's
4 re-ask it so it's clean.

5 A. Yes, please.

6 Q. Do you recall whether any of those articles
7 that you referred to were directed to NAND flash memory?

8 A. I don't recall. There were a great many papers
9 that I refereed in the early portion of my career. I
10 have no -- no -- I'm sorry. I have no memory of their
11 particular contents.

12 Q. So you have no memory of any papers that you've
13 refereed that relate to NAND flash memory; correct?

14 A. I have no memory; that's correct.

15 Q. Did you conduct research at some time during
16 your career?

17 A. Yes.

18 Q. When was the last time that you were active --
19 actively involved in research?

20 A. Are you differentiating research from
21 development? And how are you using that term?

22 Q. Let me -- let me rephrase. Thank you for that.
23 When was the last time that you were actively
24 involved in research and development?

25 A. The last engagement that I recall was in the

1 late 2000s where I was -- I had a client that was --
2 over many years that I was involved with their research
3 and development team. There may have been other clients
4 since then where my involvement was less significant
5 that I don't recall.

6 Q. Did that engagement that you're talking about
7 involve 3D NAND flash memory?

8 A. Yes, I think it did.

9 Q. When did you first learn about non-volatile
10 memory design?

11 A. Certainly, I learned about non-volatile
12 memories generally before I was even in undergrad, so
13 that would have been in the 1970s, early 1970s.

14 Q. And when did you first learn about NAND flash
15 memory?

16 A. I can't give you a specific date on that. It
17 was certainly relatively early in my career as NAND
18 flash became a thing, whenever that was.

19 Q. Did you learn about it in college?

20 A. I can't say one way or the other. Whenever
21 NAND flash became a product that was available, that's
22 when I learned about it.

23 Q. Can you say whether you learned about it in
24 grad school?

25 A. No, I can't say one way or another.

1 Q. And is it the same answer for NOR memory?

2 A. Yes, whenever -- I can't give you a specific
3 date on that.

4 Q. When were these technologies first introduced
5 commercially? And I'm talking about non-volatile
6 memory.

7 A. Non-volatile memories were introduced in the
8 '60s, if not earlier. I mean, non-volatile memories
9 date all the way back to ferrite core memories that
10 were -- predate the development of integrated circuits,
11 so they -- the concept of non-volatile memories is very
12 old.

13 Q. What about NAND memory? When does that date
14 back to?

15 A. Again, as I mentioned earlier, I don't recall
16 specifically when that became a term of art and when
17 products characterized as NAND memory -- NAND flash
18 memory were introduced.

19 Q. Do you recall whether that technology, the NAND
20 technology, was developed by at least the 1990s?

21 A. Again, I can't give you a specific date when
22 the term "NAND flash" was -- became -- was introduced
23 into the marketplace.

24 Q. I'm not -- and just to clarify, I'm not asking
25 for a specific date. I'm asking whether your

1 recollection and understanding is that that technology
2 existed by the 1990s?

3 A. Again, I don't have a specific recollection
4 whether it was in the 1990s or the 2000s when that term
5 was introduced.

6 Q. But your recollection is that whenever that
7 date is that the term was introduced, that's when you
8 became aware of it; is that correct?

9 A. It was certainly the focal point of my
10 professional career to be on top of, and fluent with,
11 the broad spectrum of memory devices that were available
12 in the marketplace and that as soon as that -- those
13 products were imminent, that's when I would have learned
14 about them.

15 Q. And would that date when those products were
16 known to the industry, would that have been before 2004?

17 A. I believe so. But, again, I can't give you a
18 specific or even a broad range of -- of dates when that
19 term was introduced. Certainly, we have that term in
20 the references in this matter prior to 2004, and so I
21 presume so, but I can't give you any specific
22 information on that.

23 Q. And so a person of skill in the art would have
24 known about these circuit design technologies, NOR and
25 NAND, by at least the 2004 time frame; is that correct?

1 A. Yes, certainly based on the filing dates of
2 some of the references in the present matter, we can
3 come to the conclusion that a POSITA would have heard of
4 those terms before 2004.

5 Q. And the POSITA would not only have heard of the
6 terms, but they would have known about the circuit
7 design that's implemented in the NAND and NOR memory
8 technology; correct?

9 A. And you're referring to a POSITA as defined in
10 the petition?

11 Q. Yes, or any way that you want to define a
12 POSITA.

13 A. Okay.

14 Is there a question pending?

15 Q. There is. Let me repeat it.

16 And the person skilled in the art would not
17 only have heard of those terms, but they would have
18 known about the circuit design that's implemented in
19 NAND and NOR memory technology by 2004; correct?

20 A. Okay.

21 So as the POSITA in -- as been defined in this
22 matter to be a practitioner with a bachelor's degree
23 in --

24 (Stenographer clarification.)

25 THE WITNESS: -- electrical engineering,

1 computer engineering, or a related field and at least
2 two years of experience in the research, design, or
3 development of semiconductor memory device structures or
4 the equivalent, with additional education substituting
5 for experience and vice versa, that POSITA would have a
6 familiarity with the circuit designs -- the circuit
7 structures found in NAND flash and NOR flash
8 semiconductor memory devices.

9 Q. (By Mr. Kappos) By 2004; correct?

10 A. By 2004. Thank you.

11 Q. I'm handing you a copy of Exhibit 1001.

12 A. Are we done with the CV?

13 Q. We might come back to it, but you can put it
14 aside for now.

15 A. Very good.

16 Q. I've handed you Exhibit 1001. This is the '702
17 patent that's at issue in this matter. Are you familiar
18 with the '702 patent?

19 A. Yes, I am familiar with the '702 patent.

20 Q. You reviewed the patent to prepare your
21 declaration; correct?

22 A. Generally speaking, I did review the patent
23 principally to understand the claims as -- that -- as
24 they were issued.

25 Q. And you are aware that the claims that are

1 challenged in this case are Claims 13 to 17; correct?

2 A. I do understand that.

3 Q. Claim 13 requires a stackable add-on layer
4 having a plurality of vertically oriented semiconductor
5 memory cells; correct?

6 A. Yes. That's the element we've been referring
7 to as Element 13[b]. It requires a stackable add-on
8 layer having a plurality of vertically oriented
9 semiconductor memory cells.

10 Q. In your declaration, which is Exhibit 2029, you
11 did not offer any opinion on the meaning of stackable
12 add-on layer; correct?

13 A. Correct. I was not asked to form an opinion on
14 the term "stackable add-on layer."

15 Q. Okay.

16 I'm handing you a copy of Exhibit 1005. Do
17 you recognize Exhibit 1005 as the Watanabe patent?

18 A. Yes, I do.

19 Q. Watanabe describes a stackable add-on layer;
20 correct?

21 A. Watanabe describes a stacking method by which
22 it describes a sequence of steps for creating a memory
23 integrated circuit with a plurality of layers. It does
24 not refer to them as stackable add-on layers to my
25 recollection.

31

1 Q. But the stacking method that Watanabe describes
2 uses a structure that would meet the requirement of a
3 stackable add-on layer; correct?

4 A. I don't think I've offered an opinion to
5 whether those layers of Watanabe meet the first portion
6 of Element 13[b], the stackable add-on layer of Claim 13
7 of the '702 patent.

8 Q. So my question is: Do you believe that the
9 structure described in Watanabe meets the requirement of
10 a stackable add-on layer?

11 A. Again, I think -- I do not recall having
12 offered an opinion to that effect. If you want to point
13 me to a place in my declaration where I say that, I
14 would be happy to review that.

15 Q. That's not an answer to my question. I'm not
16 asking whether you offered an opinion.

17 I'm asking: Do you have an opinion, as you sit
18 here today -- let me rephrase the question.

19 Does Watanabe describe a structure that meets
20 the requirements of the stackable add-on layer as you
21 understand that term?

22 A. And, again, I've not been asked to form an
23 opinion as to what is and what is not a stackable add-on
24 layer, so I can't confirm or deny whether those layers
25 meet the requirements, as you say, of the first portion

1 of the Element 13[b].

2 Q. Okay.

3 And so your testimony is that you have no
4 opinion; correct?

5 A. My testimony is that I've not been asked to
6 form such an opinion.

7 Q. Do you have an opinion on this question as you
8 sit here today?

9 A. Again, I've not been asked to form such
10 opinion, and I have not formed such an opinion.

11 Q. Watanabe describes two manufacturing methods
12 for making semiconductor memory cells; correct?

13 A. Generally speaking, Watanabe describes a
14 lamination method and a stacking method.

15 Q. And the lamination method that you just
16 referred to involves the sequential deposition of thin
17 films to build memory cells vertically; is that correct?

18 A. So as described in Column 5 of Watanabe,
19 beginning in -- on Line 3, it says, "The first method of
20 forming the wires plurality of" --

21 (Stenographer clarification.)

22 THE WITNESS: -- "planar members are formed and
23 are laminated and holes are formed in the laminated
24 planar members through which the wiring passes. This
25 method is naturally called a laminating method."

1 So the individual layers that constitute the
2 integrated circuits are formed and laminated.

3 Q. (By Mr. Kappos) And do you understand that
4 formation process to be a process that involves
5 sequential deposition of thin films to build memory
6 cells vertically?

7 A. Yes. Generally speaking, in Column 5, Watanabe
8 describes the creation of a DRAM memory device through
9 the lamination or sequential deposition of layers to
10 build up a final memory device.

11 Q. So if I use the term "sequential deposition
12 method" today, will you understand that I'm referring to
13 the fabrication method that uses the sequential
14 deposition of thin films to build memory cells
15 vertically?

16 A. If we're talking about Watanabe, we should use
17 Watanabe's term "laminating method."

18 If you're referring generally to semiconductor
19 manufacturing, then that's a reasonable definition.

20 Q. Okay.

21 And we can agree that that's what that term
22 means, then; correct?

23 A. I understand what you mean by that term.

24 Q. Okay.

25 And Watanabe, I think you also said that it

1 refers to a second method, and I think they call it the
2 stacking method; correct?

3 A. Yes. Beginning in Column 5 at Line 45,
4 Watanabe says that "another method for manufacturing a
5 semiconductor memory device, according to the present
6 invention, is called a stacking method," and then it
7 goes on to describe that method and differentiating it
8 from the laminating method described previously in --
9 higher up in Column 5.

10 MS. ARMOND: Counsel, we've been going for
11 about an hour.

12 MR. KAPPOS: Do you want to take a break?

13 MS. ARMOND: It's up to him.

14 THE WITNESS: Yes, please.

15 MR. KAPPOS: Okay.

16 Sure. We'll take a break.

17 THE VIDEOGRAPHER: The time is 10:00 a.m., and
18 we are now going off the record.

19 (Recess taken from 10:00 a.m. to 10:13 a.m.)

20 THE VIDEOGRAPHER: The time is 10:13 a.m. We
21 are now back on the record.

22 Q. (By Mr. Kappos) Welcome back.

23 So before the break, we were talking about
24 Watanabe and the stacking method. And in the stacking
25 method, Watanabe teaches to separately fabricate a layer

35

1 of memory cells and then stack that layer of separately
2 fabricated memory cells on top of the substrate or on
3 top of memory cells; correct?

4 A. Yes. Generally speaking, in Watanabe in Column
5 5, beginning at Line 45, it describes the stacking
6 member of where it forms a layer and then the planar
7 members are thus formed and stacked and wired as the
8 final steps, per Lines 54 and 55 of Watanabe.

9 Q. And then Watanabe teaches bonding of that
10 separately fabricated structure to the top of the
11 substrate or the top layer of the memory cells; correct?

12 A. Please repeat the question.

13 (Record read.)

14 THE WITNESS: Yes. In Column 6, starting at
15 Line 6, Watanabe recites that the planar members that
16 were previously formed -- let me start again.

17 As Watanabe discloses in Column 6, starting at
18 Line 6, "As shown in Figure 6C, the planar members thus
19 formed are bonded together. The bonding is made by a
20 thermal process of 900 degrees to 1,000 degrees
21 Celsius."

22 Q. (By Mr. Kappos) So if I use the term "stacking
23 method" today, will you understand that I'm referring to
24 the fabrication method that uses a separately fabricated
25 structure of memory cells and then stacks and bonds that

1 structure on top of the substrate or on top of the layer
2 of memory cells?

3 A. If you make it clear that you're referring to
4 the stacking method of Watanabe, then, yes, that will be
5 understood.

6 Q. Is there another term that you think more
7 accurately describes the stacking method? In other
8 words, independent of Watanabe, is there some other term
9 that you would describe -- use to describe that process?

10 A. Not that I can think of right now, but since
11 you're referring specifically to the method of Watanabe
12 when using the term "stacking method," you should be
13 clear that you're talking about the stacking method of
14 Watanabe.

15 If you're talking about a method similar to
16 Watanabe's that's different -- related to but different
17 in some respect to Watanabe, we should not use
18 Watanabe's term.

19 Q. Okay.

20 Well, what term should we use if we're talking
21 about a method that's independent of Watanabe?

22 A. It -- it doesn't matter to me what term we use
23 other than -- so long as we make clear that it's not the
24 stacking method of Watanabe.

25 Q. I'm handing you a copy of Exhibit 1007. This

1 is the Lee '994 patent. Are you familiar with this
2 patent?

3 A. Yes, I am.

4 Q. Does Lee describe a stackable add-on layer?

5 Let me replace that question with a different
6 question.

7 You reviewed Lee in connection with preparing
8 your declaration; correct?

9 A. Yes, I did.

10 Q. And you reviewed it in preparation for your
11 deposition; correct?

12 A. In part, yes.

13 Q. Okay.

14 So now let me go back to my question. Does Lee
15 describe a stackable add-on layer?

16 A. As I testified earlier, I've not been asked to
17 form an opinion on what is and what is not a stackable
18 add-on layer, so I do not have an -- have not formed an
19 opinion as to whether Lee discloses a stackable add-on
20 layer as that term is used within the claims of the '702
21 patent.

22 Q. Okay.

23 Let's refer again to the '702 patent, which is
24 Exhibit 1001. The priority date is September 3rd, 2004;
25 correct?

1 A. So on the front page of the '702 patent,
2 Item 63 says that -- that "this application was a
3 continuation in part of Application No. 10/873,969 filed
4 on June 21, 2004." I believe it's indicating that it is
5 drawing priority to that application.

6 Q. Let me ask this, then: What date did you use
7 as the priority date in conducting your analysis for
8 this case?

9 A. I don't believe the priority date ever came
10 into discussion or became an issue with regard to my
11 opinions, because I was asked to assume that Lee,
12 Watanabe, and Endoh were prior art as a matter of
13 assumption for my analysis.

14 Q. Are you familiar with the term -- with any of
15 the terms, "technology node" or "process node" or
16 "series" in the semiconductor industry?

17 MS. ARMOND: Objection. Form.

18 THE WITNESS: The first two terms that you used
19 have generally understood meanings within the industry.

20 The term "series" is used in many different
21 contexts, so I don't know what you mean by "series."

22 Q. (By Mr. Kappos) Okay.

23 What does the term "technology node" mean?

24 A. I don't think that I have rendered any opinions
25 that relate to technology node. If there's some -- if

1 that term exists in my declaration, would you please
2 point it to -- point it out to me.

3 Q. Yeah, I'm not asking about your declaration.
4 I'm asking whether you have an understanding of what the
5 term "technology node" means as a person skilled in the
6 art.

7 A. I have a general understanding of what that
8 means, but I'm here today to answer questions about my
9 declaration and the opinions therein. So if I didn't
10 use the term "technology node" within it, I don't
11 understand the relevance of the question.

12 Q. What is your general understanding of the
13 meaning of technology node?

14 A. Again, I'm here today to answer questions about
15 my declaration and the opinions therein. If I did not
16 use the term "technology node" in my declaration or in
17 my opinions, I don't see the relevance of that question.

18 Q. So you won't answer the question?

19 MS. ARMOND: Objection.

20 (Stenographer clarification.)

21 MS. ARMOND: Misstates prior testimony.

22 THE WITNESS: I do not understand the relevance
23 of the -- of the idea of technology node, given that
24 I've not opined anything relating to technology node.

25 Q. (By Mr. Kappos) This deposition is not limited

1 to your declaration. I'm free to ask questions about
2 your general understanding.

3 Do you understand that?

4 A. My understanding is that my purpose here is to
5 answer questions about my declaration and my opinions
6 therein.

7 Q. So you refuse to tell me what your
8 understanding as a person of skill in the art is of the
9 term "technology node"; is that correct?

10 A. My answer to your question is that I did not
11 use that term anywhere in my declaration. It's not
12 relevant to my opinions; and, therefore, I don't
13 understand the relevance of the question.

14 Q. What about the term "process node"? Do you
15 refuse to answer any questions about your understanding
16 of that term?

17 A. Did I use that term anywhere in my declaration?

18 Q. I don't know.

19 Do you have an understanding of what the term
20 means?

21 A. I have a general understanding of what the term
22 means, but, again, this -- I don't believe I used that
23 term in my declaration, I don't recall having used it,
24 and, therefore, it's not relevant to my opinions in this
25 matter.

1 Q. Okay.

2 Please tell us your general understanding of
3 the term "process node."

4 A. Again, I don't understand the relevance of this
5 line of questioning, given that I didn't use the term
6 "process node" anywhere within my opinions in this
7 matter.

8 Q. Sir, your -- your function here today is not to
9 tell us what you think is relevant and not relevant.
10 You're to answer questions if you have an understanding
11 of what those questions are.

12 Do you understand that?

13 MS. ARMOND: Counsel, stop badgering the
14 witness.

15 THE WITNESS: My understanding of my role here
16 today is to answer questions about my opinions as they
17 are articulated in my declaration. And --

18 Q. (By Mr. Kappos) You used the term "minimum
19 feature size" in your declaration. Do you recall that?

20 A. Yes, I do.

21 Q. What is a minimum feature size?

22 A. Do you know the paragraph in which I described
23 that?

24 Q. 79.

25 A. Thank you.

1 To paraphrase my Paragraph 79, the minimum
2 feature size of a process is a general indicator of
3 the -- the size of the features, the smallest features
4 within the manufacturing process of the semiconductor
5 devices. It traditionally has been the size of the
6 transistor -- the width of the transistor gates formed
7 in the substrate. Over time, as processes have become
8 more complicated, that is not necessarily always the
9 smallest feature, but it is -- still remains an
10 indicator of the general size of the transistors and the
11 features fabricated on the substrate.

12 Q. In 2004, the year that the '702 patent was
13 filed, what was the feature size in the semiconductor
14 industry?

15 A. Certainly, at any one point -- any point in
16 time, there is a leading edge process, and -- but all
17 older processes are still in active use, so there is no
18 one minimum feature size in the industry at any given
19 point in time.

20 Q. Okay.

21 So what was the leading edge process feature
22 size in 2004?

23 A. Do you know whether I've given a specific
24 number for that in my declaration?

25 Q. I don't recall.

1 A. I don't recall either. I think -- let me try
2 and find a specific reference to a feature size.

3 Q. I might be able to help, though, by introducing
4 another exhibit, so I'm going to hand you a copy of
5 what's been marked as Exhibit 2022, and I'll refer
6 you -- well, first let me ask: Have you seen this
7 document before?

8 A. I know I referenced the 2007 version of this
9 series of documents. I don't -- let me see if I refer
10 to the 2003 version in my list of materials.

11 I may have seen the 2003 edition of the
12 "International Technology Roadmap for Semiconductors
13 Executive Summary" before either in connection with this
14 case or otherwise. I don't recall a specific date in
15 which I've reviewed it.

16 Q. Okay.

17 Let me refer you to Page 7 and it's actually
18 several pages in. It says "Page 7" at the bottom
19 right-hand corner of Exhibit 2022. Do you see Table B
20 on that page?

21 A. I do see Table B on Page 7 of Exhibit 2022.

22 Q. Okay.

23 And the top -- the top table -- there's two
24 tables. There's one at the top that says "Near Term
25 Years." Do you see where it says "2004"?

1 A. Yes, I do.

2 Q. And so in 2004, does this indicate that the
3 DRAM half pitch was 90 nanometers?

4 A. So this document does indicate that in 2004,
5 the DRAM half pitch is going to be 90 nanometers for
6 some processes in use at that time or -- it's not clear
7 whether this is the introduction date of those processes
8 or the mass production of those processes. I'd have to
9 read the surrounding paragraphs to properly interpret
10 Table B.

11 Q. Is this consistent with your knowledge that the
12 leading edge process would have been 90 nanometers in
13 the 2004 time frame?

14 A. Well, to quote from the paragraph above, Table
15 B in Page 7 of Exhibit 2022, "Commercially used numbers
16 for the technology generation typically differ from the
17 ITRS technology node numbers."

18 So it's indicating that this DRAM half pitch of
19 90 nanometers indicated in Table B is perhaps not
20 actually used, but is in the same general ballpark.

21 Q. Okay.

22 Do you have any reason to doubt -- well, let me
23 ask it differently.

24 You have no reason to doubt that the industry
25 was in the 90 nanometer DRAM half pitch, as indicated in

1 Table B, in 2004; right?

2 A. Qualified as you have in your question, I would
3 agree with that.

4 Q. Is the DRAM half pitch, is that the same thing,
5 to your understanding, as the feature size that you
6 talked about?

7 A. Those two concepts are related. Within -- but
8 they are not identical. Within the ITRS 2003 document
9 that you have put in front of me, it describes, in the
10 paragraph above Table B, what it defines as an ITRS
11 technology node and how it's different for DRAMs as
12 opposed to other types of the semiconductor memories.

13 My concept of a minimum feature size, the use
14 of which predates this -- this version of the ITRS is
15 again, as I said, related to the DRAM half pitch, but is
16 not the same as.

17 Q. How does it differ?

18 A. The DRAM half pitch is related to the pitch of
19 a specific DRAM cell structure and is one-half of that
20 pitch as it was typically practiced in the industry at
21 that time.

22 The minimum feature size that I refer to in my
23 Paragraph 79, I think it was -- is that correct? -- is a
24 more generic concept that applies not just to DRAMs but
25 to semiconductor manufacturing processes generally, as

1 I've indicated in my declaration at Paragraph 79.

2 Q. And the feature size that you talked about in
3 your declaration, would that have been the feature size
4 of the leading edge process?

5 A. The minimum feature size concept that I
6 articulate in my declaration Paragraph 79 is a general
7 concept not related specifically to a leading edge
8 process. It relates to any process.

9 Q. In 2004, if the industry for DRAM was in the 90
10 nanometer half pitch, does that also indicate that the
11 industry would be in the 90 nanometer for NAND?

12 A. Generally speaking, the process -- processes
13 for the manufacture of NAND flash memories are
14 substantially different from the processes that are used
15 to build DRAMs. However, at a gross level, the -- the
16 minimum feature size or the scale of the processes would
17 be roughly comparable, but they're not the same.

18 Q. So the feature size for NAND flash and for DRAM
19 in 2004 would have been approximately the same?

20 A. When you say "feature size," you mean the
21 minimum feature size.

22 Q. Correct.

23 A. Would you rephrase the question.

24 Q. Yeah, let me -- let me restate that.

25 So the minimum feature size for NAND flash

1 memory and for DRAM in 2004 would have been
2 approximately the same; correct?

3 A. Given a loose enough definition of
4 approximately, yes. They -- they are -- both sets of
5 processes, DRAM processes and NAND flash processes, make
6 use of the equipment that is able to resolve smaller and
7 smaller feature sizes from one generation of machines to
8 the next. So they -- they both decline or are reduced
9 year by year or generation by generation, more
10 precisely.

11 But they're not always identical based on the
12 particular challenges in making DRAMs and the particular
13 challenges in making NAND flash memories.

14 Q. So if the DRAM minimum feature size were
15 90 nanometers, what would the NAND flash feature size
16 be -- in other words, can you give me an idea of the
17 plus/minus? What's the range that you think
18 differentiates the two?

19 A. I can't give you anything along those lines. I
20 haven't studied that issue. I -- certainly not for
21 this, for this matter, for this expert report. Those
22 sorts of differences are highly company-specific. Each
23 company will have its own specific fabrication
24 technologies that it puts into manufacturing and into
25 high-volume production of memory integrated circuits and

1 so it's impossible for me, without access to those
2 company-specific processes, to characterize what you're
3 asking for.

4 Q. Do you understand -- let me start again.

5 Would a person of skill in the art understand
6 that minimum feature size is the same or roughly the
7 same as the technology node?

8 A. Well, to be clear, what the ITRS -- ITRS 2003
9 and other editions of this document define technology
10 node as the columns in these tables. And on Page 6,
11 it -- technology node is defined and put in quotes to
12 help the reader understand that that's what this
13 organization means by technology node in this document.

14 The -- it's -- the purpose of the document is
15 to help the industry coalesce around specific goals for
16 future processes across the industry. Individual
17 processes at individual specific companies will deviate
18 from these nodes -- technology nodes as it's used within
19 these -- this document to a greater or lesser extent
20 depending on the particulars of the manufacturing
21 processes at a specific company.

22 I think that answered your question.

23 Q. Well, you used the term "minimum feature size."
24 I'm trying to get an understanding of how that relates
25 to the terminology that's used in Exhibit 2022. Is it

1 roughly the same thing?

2 A. I've defined the minimum feature size as it
3 would be understood by a POSITA in light of his training
4 at -- in -- in his experience and his training at
5 undergraduate level as being roughly -- being defined as
6 the -- generally, the size of the transistor gate.

7 Now, the art -- and so it's a very general
8 concept as I've articulated it in Paragraph 79 and use
9 it elsewhere within my report.

10 The technology nodes as they're defined within
11 the ITRS document are specific, but, again, don't
12 correspond to any particular process. They are targets
13 for the industry at large.

14 So there is a correlation between the minimum
15 feature size that I write about in my report and the
16 technology nodes that is articulated within the ITRS
17 2003 document, but they are not the same. If they were
18 the same, there would be a single row in each of the
19 first and second Table Bs, but there's a plurality of
20 different characteristics depending on the type of
21 device and the type of process, all of which represent a
22 goal for a future set of technologies that the industry
23 can aim towards.

24 Q. So Exhibit 2022 is teaching that in 2004 the
25 industry was in the 90 nanometer technology node and

1 you, I believe, indicated -- and I'll ask this as a
2 question -- the feature size in 2004 -- the minimum
3 feature size was roughly 90 nanometers; is that correct?

4 A. So to answer that question, we'd have to look
5 at the layout of a specific DRAM from that era and
6 understand what -- how the pitch of the DRAM cell
7 relates to the gate -- the size of the gate of the
8 access transistor which per my definition corresponds to
9 a minimum feature size as would be understood by a
10 POSITA at that time as a general concept; that there is
11 a relationship there between the DRAM half pitch and the
12 size of the gate of the access transistor, but I'm --
13 have not looked at that recently. I've not opined upon
14 that in my report. I don't know. I can't answer your
15 question specifically.

16 Q. And you can't answer it because you don't know
17 what that relationship is as you sit here today?

18 A. It's the specific structure of the DRAM cells,
19 as I've shown in a later paragraph when we're talking
20 about -- when I'm talking about Watanabe's DRAM
21 implementation, that the structure of DRAM cells varies
22 greatly from generation to generation and from
23 manufacturer to manufacturer and so the relationship
24 between the DRAM cell pitch size and the access
25 transistor width is not clear to me and would depend on

1 a specific process.

2 If you'll just hold on for a second, I will
3 find those figures for you. Here we go.

4 So in Paragraph 86 of my expert report, I show
5 a number of different actual DRAM cells and they show
6 access transistors and capacitor structures and the
7 pitch of these DRAM cells vary relative to the size of
8 the access transistor gate so there's no one answer to
9 your question. It depends on the specifics of the DRAM
10 process.

11 Q. So you referred a number of times to the size
12 of the gate in talking about the minimum feature size.
13 Is that the size of the gate measured horizontally, in
14 other words, left to right, not vertically; correct?

15 A. Certainly left to right is not appropriate, but
16 horizontally versus vertically, yes. So, for example,
17 if you look at the figures of the '702, we have Figure
18 1, for example, in Paragraph 39 of my expert report, it
19 shows transistors formed in the base substrate, Item
20 143, with the gates of those transistors formed in the
21 dielectric Layer 133, and so the width of that gate
22 horizontally is the drawn width of the X of that
23 transistor and that would be in -- a representation of
24 or correlated with the -- what a POSITA would understand
25 is the minimum feature size for that process.

1 (Stenographer clarification.)

2 THE WITNESS: It's the drawn width of the gate.

3 Q. (By Mr. Kappos) So you referred to Figure 1 in
4 Paragraph 39. Can you just point out what specifically
5 is the gate that you're referring to the dimension of.

6 A. All right. Certainly.

7 Give me a moment.

8 Q. And I mean in the figure.

9 A. Yes.

10 Q. Okay.

11 A. I'm attempting to find the unit number for the
12 gate whether 114 was specifically referring to the gate,
13 then I could be specific. Otherwise, if I can't find
14 that, I'll have to describe with words instead of with
15 unit numbers what I'm referring to. So give me a
16 moment, please.

17 Okay. So Item 114 is the logic circuit in --

18 (Stenographer clarification.)

19 THE WITNESS: Okay.

20 Let me start again so I'll go more slowly.

21 In Column 5 of the '702 patent beginning at
22 Line 60, it describes that in Figure 1, Logic Circuit
23 114 includes a sense amplifier and so on and so forth.
24 So if you look in Figure 1, Item No. 114 has an arrow
25 generally pointing down and to the left, pointing

1 towards a horizontal structure that's hash-marked
2 diagonally top right to bottom left; that is the gate of
3 a transistor. It is the width of that gate that a
4 POSITA would talk about when referring to the minimum
5 feature size of that gate as a general indicator of the
6 scale of the process.

7 Q. (By Mr. Kappos) Do you see a structure above
8 what you've highlighted as the blue structure, one
9 that's indicated with the Brackets 101?

10 A. Yes, I do.

11 Q. Is there a gate in the structure that's
12 designated with the Bracket 101?

13 A. I don't believe I've really opined about the
14 internal structure of Figure 101. If I have, could you
15 point me to a particular paragraph.

16 Q. I don't know if you have said this in a
17 paragraph. I'm asking for your understanding as you sit
18 here looking at the figure which you included in your
19 declaration.

20 MS. ARMOND: Is there a question pending?

21 MR. KAPPOS: There is. I'll repeat the
22 question.

23 THE WITNESS: Give me a moment, please, then
24 repeat the question.

25 Please repeat the question.

1 Q. (By Mr. Kappos) In Figure 1 is there a gate
2 that's designated with the Bracket 101?

3 A. Looking at the '702 patent, Columns 5 and 6, in
4 which Column 1 is described, I'm not seeing any
5 reference to a gate anywhere within that text.

6 I've not opined whether or not there are gates
7 within the Structure 101 and I'm not willing to form an
8 opinion to that effect sitting here today.

9 Q. Now, you understand that patent figures are not
10 necessarily drawn to scale; correct?

11 A. I believe I've opined to that effect. Can you
12 point me to the paragraph in which I do that.

13 Q. Paragraph 80.

14 A. Thank you.

15 Yes. In Paragraph 80, I say that "while I
16 understand that patent figures are not necessarily drawn
17 to scale, that the landing pads are much larger than the
18 minimum metal spacing or the minimum via spacing, the
19 pitch and area of each of Watanabe's non-volatile memory
20 cells would have to increase accordingly, substantially
21 impacting Watanabe's stated goal of improved" --

22 (Stenographer clarification.)

23 THE WITNESS: -- "integration density."

24 Q. (By Mr. Kappos) Okay.

25 And so you understand that patent figures are

1 not necessarily drawn to scale; correct?

2 A. That is what I just read, yes.

3 Q. And so the figures in the '702 patent are not
4 drawn to scale; correct?

5 A. What I say in my Paragraph 80 is that they are
6 not necessarily drawn to scale. This may be drawn to
7 scale. It may not be drawn to scale. We do not assume
8 that patent figures are drawn to scale. I've not formed
9 an opinion as to whether this particular figure is drawn
10 to scale or not. I've just -- that's not been a
11 question that has come up in my analysis of the -- this
12 present matter.

13 Q. And so you would not assume that the figures of
14 the '702 patent are drawn to scale; correct?

15 A. As a matter of process, personal process, you
16 begin by looking at a figure assuming it's not drawn to
17 scale. If there are indications in the text or in the
18 figure that indicate otherwise, then you change your
19 assumptions.

20 But, again, that's not something I've done with
21 regard to Figure 1, so I would still, looking at Figure
22 1, assume that it's not necessarily drawn to scale.

23 Q. And the same would be true for the remaining
24 figures in the '702 patent; correct?

25 A. Yes. Since I've not opined on any of the

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1 figures of the '702, I've not analyzed them to determine
2 whether the presumption of not necessarily drawn to
3 scale needs to be modified for any of them.

4 Q. You've considered the '702 patent in connection
5 with forming your opinions in this case; correct?

6 A. Certainly, the '702 patent is listed among the
7 documents that I have reviewed and considered in Section
8 3 of my expert report. It's listed as -- yes, quoting
9 from my Paragraph 12, I say, "I reviewed '702 patent and
10 its file history. Additionally and in addition to any
11 other documents cited or referenced herein, I reviewed
12 the following materials."

13 So I have reviewed '702, specifically the
14 claims therein especially. I'm not sure that I relied
15 on the '702 in forming my opinions about the other
16 references and their relationship to the claims at issue
17 here.

18 Q. So the '702 patent is the main patent that's
19 involved in this case. You understand that; right?

20 A. It is the claims of the '702 that are being
21 challenged, yes.

22 Q. Right.

23 And so you would have reviewed the '702 patent
24 very carefully in connection with doing your
25 declaration; correct?

1 A. As I stated in Paragraph 12, I have reviewed
2 the '702 patent.

3 Q. And did you see anything in the text of the
4 '702 patent that stated that the figures were drawn to
5 scale?

6 A. I don't recall anything to that effect.

7 Q. So in the '702 patent, it uses the term "SOI
8 pillar"; you recall that?

9 A. Yeah, for example, Claim 14 refer -- relates
10 to -- recites an SOI pillar.

11 Q. Okay.

12 And what does SOI pillar mean, in your opinion?

13 A. So to -- in conclusion of my Section 10- --
14 Point A on SOI pillar starting in Paragraph 58 and
15 concluding in Paragraph 63, I state that "Thus, in the
16 context of the present proceeding and the '702 patent,
17 in my opinion an SOI pillar is a silicon-on-insulator
18 structure taller than it is wide."

19 Q. How did you come up with that definition?

20 A. I -- well, beginning in Paragraph 58, at the
21 start of that section and proceeding through Paragraph
22 63, I outline the rationale for that proposed -- for
23 that opinion on what an SOI pillar means in this matter.
24 I can read that all into the record if you would like.

25 Q. No, you don't need to do that.

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1 Did -- did counsel come up with this definition
2 or did you come up with it?

3 MS. ARMOND: I would caution the witness not to
4 reveal any attorney-client privileged communications in
5 answering that question.

6 THE WITNESS: I think what I've testified
7 previously is that to a degree the preparation of the
8 declaration was a collaborative effect -- effort, and
9 that the -- the core idea behind this definition was
10 mine. The actual final terminology may have changed
11 over the -- between the first draft and the final draft.
12 I don't recall specifically.

13 Q. (By Mr. Kappos) Can you tell me what evidence
14 supports your definition. And I don't mean to have you
15 read in 58 to 63, but at a high level do you recall what
16 evidence you relied on that supports your definition?

17 A. Well, there were dictionaries cited vis-a-vis
18 what a pillar is. There were references to various
19 patents that use the term and for SOI, we relied
20 specifically on -- or I relied specifically on the '702
21 patent at Column 4, Lines 45 to 46, as explained in my
22 declaration in Paragraph 59.

23 Q. A pillar as that term is used in the '702
24 patent can have one or more than one memory cell;
25 correct?

1 A. Sitting here today, I do not recall the term
2 "SOI pillar" being referred to a structure with more
3 than one cell in it in the '702 patent. Perhaps you
4 could point me at something within that patent that
5 would clarify.

6 Q. Okay.

7 MS. ARMOND: We've been going for about an
8 hour.

9 MR. KAPPOS: Can I just finish this line? I'll
10 cut it --

11 MS. ARMOND: If the witness is okay with it.

12 Q. (By Mr. Kappos) Are you okay going a little
13 bit longer?

14 A. How many -- how much longer?

15 Q. I just want to give you an example.

16 A. Okay.

17 Q. Okay.

18 In Figure 4 of the '702 patent, would you agree
19 with me that there are two vertical DRAM memory cells?

20 MS. ARMOND: Objection. Outside the scope.

21 THE WITNESS: Well, referring to Column 2,
22 Lines 21 to 24, the '702 patent summarizes Figure 4 as a
23 cross-sectional view of an embodiment --

24 (Stenographer clarification.)

25 THE WITNESS: -- of the present invention

1 having two vertical DRAM cells with vertical connection
2 of a capacitor and a MOSFET --

3 (Stenographer clarification.)

4 THE WITNESS: -- MOSFET, M-O-S-F-E-T, all caps,
5 respectively in the SOI layer. It does not refer to it
6 as a pillar. Perhaps it does in text. Regardless, this
7 is not a figure that I've analyzed or opined on in my
8 declaration and so if it doesn't actually call it a
9 pillar in the specification somewhere, I would hesitate
10 to characterize it otherwise.

11 Q. (By Mr. Kappos) Okay.

12 Take a look at Column 8, Lines 5 to 11.

13 MS. ARMOND: Is there a question pending?

14 MR. KAPPOS: There will be as soon as he looks
15 at that part.

16 Q. (By Mr. Kappos) Have you looked at that?

17 A. I'm still reading. Thank you.

18 I've read that section.

19 Q. Okay.

20 And so Figure 4 of the '702 patent shows two
21 vertical DRAM memory cells on one pillar; correct?

22 A. What it says in Column 8, Lines 5 through 11,
23 is that "there are two vertical DRAM cells in vertical
24 connection with a capacitor and a MOSFET, respectively,
25 in the stackable add-on layer. The structure shares a

1 single bit line; therefore, the density of the DRAM
2 cells increases by factor of two while the aspect
3 ratio" --

4 (Stenographer clarification.)

5 THE WITNESS: -- "of SOI Pillar 124 remains
6 relatively small."

7 So it's referring to Item 124 as an SOI pillar.
8 Whether that is in the context of the '702, the entire
9 stack or just the top portion of that, is not clear to
10 me today. I've not rendered an opinion on this figure
11 and I hesitate to do so on the fly.

12 Q. (By Mr. Kappos) So Figure 4 shows two vertical
13 DRAM memory cells on one pillar; correct?

14 A. What the patent says in the portion that I just
15 read into the record is that Item 124 is an SOI pillar
16 and, as I said, I've not analyzed this figure in detail.
17 I've not rendered an opinion on it. And I'm not willing
18 to say definitively whether 124 refers to the entire
19 collection of doped silicon structures or whether it's
20 just referring to the top. I haven't performed that
21 analysis, and I'm not going to -- willing to do that
22 now.

23 MR. KAPPOS: Okay.

24 Let's take a break.

25 THE VIDEOGRAPHER: The time is 11:20 a.m. We

1 are now going off the record.

2 (Recess taken from 11:20 a.m. to 11:32 a.m.)

3 THE VIDEOGRAPHER: The time is 11:32 a.m. We
4 are now back on the record.

5 Q. (By Mr. Kappos) Welcome back, Dr. Przybylski.

6 A. Thank you.

7 Q. Before the break, we were talking about Figure
8 4 and I believe that you testified that you had not
9 rendered an opinion on Figure 4. Is that what you said?

10 MS. ARMOND: Objection. Misstates prior
11 testimony.

12 Q. (By Mr. Kappos) Okay.

13 Then you tell us what you said about Figure 4.

14 A. Can we have the court reporter read it back.

15 Q. Okay.

16 Let me just ask the question. Did you render
17 an opinion on Figure 4?

18 A. I don't recall rendering opinion on Figure 4 at
19 all.

20 Q. Okay.

21 Let me refer you to Page 28 in your
22 declaration. Do you see at the top of the page
23 Figure 4?

24 A. Yes, I see Figure 4 on the top of Page 28.

25 Q. Okay.

1 So let me ask my question again.

2 The '702 patent at Figure 4 shows two vertical
3 DRAM memory cells on one pillar; correct?

4 A. So in my Paragraph 61, also on Page 28, I say
5 that "for Figure 4, the '702 patent explains that the
6 aspect ratio of the SOI Pillar 124 remains relatively
7 small." So same language that I read from the patent
8 prior to the break.

9 And given -- I do not, in this paragraph, opine
10 whether the pillar that's being referred to as Item 124
11 is the entire structure or just the top half.

12 Q. Okay.

13 But you do render an opinion about Figure 4;
14 correct?

15 A. Certainly in Paragraph 61 I'm commenting on
16 Figure 4 and reiterating some of the text in the '702
17 patent. I'm not seeing there an opinion as to what Item
18 124 is in the '702 patent.

19 Q. Okay.

20 Do you see the text immediately below the
21 figure, Figure 4, where you have it reproduced?

22 A. Yes, I do.

23 Q. Do you see that it says, "After Figure 4
24 depicting SOI pillars"?

25 A. Yes, I do.

1 Q. Can you tell me what are the SOI pillars that
2 are being depicted in Figures 4, 20, and 27?

3 A. In general, the vertically oriented collections
4 of doped silicon --

5 (Stenographer clarification.)

6 THE WITNESS: -- Ns, Ps, or N+ or P+,
7 constitute SOI pillars. But, again, I'm not opining
8 whether SOI Pillar 124 constitutes the entire collection
9 of regions shaded purple in the annotated Figure 4 or
10 just the top half as indicated by the arrow attached to
11 Item 124 in figure -- the annotated Figure 4 on Page 28.

12 Q. (By Mr. Kappos) So just focusing on Figure 4
13 alone, is there one pillar or is there more than one
14 pillar?

15 A. In my Paragraph 61, again referring to
16 Figure 4, I don't say whether there is one pillar or
17 more than one pillar annotated there in purple. I'm
18 merely reciting the text of the '702 patent that
19 indicates that SOI pillars, in its understanding, has a
20 small aspect ratio and that would apply equally to the
21 top half or the entire structure.

22 Q. Okay.

23 I know you didn't address this in Paragraph 61.
24 Independent of 61, I'm asking you as you sit here today:
25 Does Figure 4 alone have one pillar or is there more

1 than one pillar?

2 A. And as you just noted, in Paragraph 61, I don't
3 say one way or the other and that -- so I have not
4 rendered an opinion one way or the other whether that is
5 one pillar or two pillars and without significant
6 thought and effort, I would not want to form that
7 opinion on the fly here today.

8 Q. So in Paragraph 60, however, you do say
9 "depicting SOI pillars," plural, so you have expressed
10 an opinion about that and so I think the question is
11 entirely relevant. In Figure 4, is there one pillar or
12 is there more than one pillar?

13 MS. ARMOND: Objection. Asked and answered.

14 THE WITNESS: Paragraph 60, the plurality there
15 refers to the plurality of figures being referenced. It
16 does not articulate whether each of those figures
17 depict, as would be understood by a POSITA reading '702,
18 whether that constitutes -- each of those constitutes a
19 single pillar or a plurality of pillars. Again, it's
20 not a subject that I have opined upon here or elsewhere
21 in the report.

22 Q. (By Mr. Kappos) How do you define the
23 beginning and the end of a memory cell reference to
24 Figure 4?

25 A. Since Figure 4 is talking about DRAMs, a POSITA

1 would understand that a memory cell for a DRAM memory
2 device includes an access transistor and a capacitor.
3 So you would look at what elements within Figure 4
4 constitute an access transistor and a capacitor and
5 understand that those elements together form a memory
6 cell.

7 Q. Okay.

8 So tell me which elements in Figure 4 form a
9 single memory cell. Where is the first memory cell and
10 where's the second memory cell using your definition?

11 A. Again, this is not a figure that I've opined
12 upon or analyzed in detail, but judging by the
13 annotations in Figure 4, the -- there's the bit line in
14 the middle that connects to an N+ region and above that
15 is an access transistor controlled by a word line "WL2"
16 and above that a capacitor CAP 2 -- C-A-P, all caps,
17 digit 2 -- so that constitutes one memory cell and there
18 is a -- another memory cell below that.

19 Q. And how do you define the beginning and the end
20 of a pillar with reference to Figure 4?

21 A. So the pillar as -- in the definition of or the
22 proposed construction of a SOI pillar is taken from the
23 plain and ordinary meaning of pillar as articulated in a
24 couple of dictionaries and is summarized by the phrase
25 that "it is taller than it is wide" and that is the only

1 indication of what constitutes a pillar or not.

2 Q. And so you -- you cannot tell me where the
3 pillar begins and ends in Figure 4?

4 A. I can tell you where the memory cells begin and
5 end and any structure that is taller than it is wide per
6 my proposed -- per the plain and ordinary meaning of
7 pillar as articulated in Paragraphs 62 of my report.

8 Q. Okay.

9 But you understand that's not my question. I'm
10 asking where does the pillar begin and end.

11 MS. ARMOND: Objection. Asked and answered.

12 MR. KAPPOS: And, Counsel, I'd keep the
13 speaking objections out of it. Just object to form,
14 please. That's a speaking objection. Okay? You don't
15 need to say that and that's against the rules and you
16 know it; right?

17 MS. ARMOND: Look, I -- I'm not objecting to
18 the form. Your question is not confusing. You're
19 badgering the witness. So if you don't want to ask
20 questions that don't badger, then I don't have to object
21 to them.

22 Q. (By Mr. Kappos) Can you answer my question,
23 please.

24 THE WITNESS: Miss Court Reporter, please read
25 the question.

1 (Record read.)

2 Q. (By Mr. Kappos) The question is: Where does
3 the pillar begin and end in Figure 4?

4 A. I have not articulated an opinion as to where
5 in Figure 4 there is a pillar. There is a definition of
6 pillar that's the plain and ordinary meaning in the
7 English language of a structure that's taller than it is
8 wide and -- but I've not offered an opinion as to Figure
9 4 or Figure 20 or Figure 27 with regard to where pillars
10 start and end.

11 Q. Okay.

12 In Column 8, the section that we read earlier,
13 I think you looked at Lines 5 to 11. Let me just direct
14 you to Line 9. Tell me when you're there.

15 A. I'm there.

16 Q. Okay.

17 It uses the term "SOI Pillar 124." Do you see
18 that?

19 A. Yes. We read that into the record earlier.

20 Q. Right.

21 And that's pillar singular, not plural;
22 correct?

23 A. 124 is a singular pillar.

24 Q. Okay.

25 And that's with reference to Figure 4; correct?

1 A. In Figure 4, Item 124 is referred to as a
2 singular pillar.

3 Q. Okay.

4 And then Figure -- well, let's look further
5 down in Column 8, starting at Line 43, it's talking
6 about Figure 12 and at Line 46, it says, "The SOI Pillar
7 124."

8 Do you see that?

9 I'm only asking you if you've found the
10 place --

11 A. Yeah.

12 Q. -- where I'm referring to.

13 A. Oh, yes, I have found the place you're
14 referring to.

15 Q. And the SOI Pillar 124 is again a singular
16 pillar; correct?

17 A. Again, yes, 124 in Figure 4 and in this case in
18 Figure 12 is referred to as a singular SOI pillar.

19 Q. Okay.

20 And then let's look at Column 9 starting at
21 Line 10 which refers to Figure 20 and it says that "this
22 is a cross-sectional view of an embodiment of the
23 present invention having a negative differential
24 resistance-based vertical SRAM cell, including the
25 vertical connections of two thyristor MOSFET pairs in

1 the stackable add-on layer."

2 So would you agree with me that there are two
3 memory cells that are depicted in Figure 20 which you
4 have on Page 28 of your declaration?

5 A. Yes, that's what it says in Column 9.

6 Q. And further down in that paragraph at Line 16,
7 it says, "of SOI Pillar 124."

8 Do you see that?

9 A. That's what it says on -- in Line 16 of
10 Column 9.

11 Q. And that's singular pillar; correct?

12 A. Yes, that's singular pillar.

13 Q. And so, again, the '702 patent is referring to
14 multiple memory cells, more than one memory cell, on a
15 single pillar; correct?

16 A. What it's saying in paragraph -- in the Column
17 9, the paragraph starting at Line 10 and concluding in
18 Line 18, is that there are two thyristor type SRAM cells
19 stacked in a vertical direction and in the middle there
20 is a bit line that is shared between them. It does not
21 say that both of those memory cells are within SOI
22 Pillar 24. It's just saying that the bit line is
23 between the two SRAM cells.

24 But, again, this is not a subject matter
25 that's -- I've opined upon within my declaration and,

1 you know, this is -- I've said previously that I don't
2 know in Figure 4 whether 124 is referring to the top
3 half or the whole thing. I've not opined to that effect
4 and not willing to make a formal opinion to that effect
5 one way or another.

6 We can continue reading passages from the '702
7 and saying what it says. What it actually means is
8 another -- is for the board to determine.

9 Q. Just one more that I'd like to look at at the
10 bottom of Column 9 starting at Line 51 referring to
11 Figure 27 which you've reproduced on Page 28 of your
12 declaration, the patent says, "Figure 27 shows two
13 vertical memory cells."

14 Did I read that correctly?

15 A. Yes.

16 Q. And then further down in that paragraph, at
17 Line 55, it talks about SOI Pillar 124.

18 Did I read that correctly?

19 A. The sentence you're referring to is: "This
20 structure shares a bit line and reduced the aspect ratio
21 of SOI Pillar 124."

22 Q. And so "pillar" is being used in the singular
23 at Line 55; correct?

24 A. In Line 55 it is SOI Pillar, singular, 124.

25 Q. And so despite all these examples that I've

1 shown you, you still do not have an opinion on whether
2 the term "pillar" as used in the '702 patent can have
3 more than one memory cell; is that correct?

4 A. As I've indicated previously, I've not been
5 asked to render an opinion on these embodiments of the
6 '702 and I've not done so and do not intend to do so
7 today.

8 Q. Okay.

9 The text of the specification of the '702
10 patent does not state a quantitative value of an aspect
11 ratio of a pillar; correct?

12 A. I don't recall such an aspect ratio other
13 than -- if there's a particular passage within the '702
14 you'd want me to review, I'll be happy to do so.

15 Q. Well, I can represent to you that I didn't find
16 one and so I'm asking if you're aware of any statement
17 in the '702 patent that gives an actual aspect ratio for
18 the pillar.

19 A. I'm not aware of any specific characterization
20 of a minimum aspect ratio within the '702 patent, but,
21 again, I haven't opined on that.

22 What I have opined on is that the plain and
23 ordinary meaning of a pillar is that it is taller than
24 it is wide and that is consistent with the figures that
25 I have included in my declaration on Page 28.

1 Q. Okay.

2 Let me refer again now to the Lee '994 patent
3 which is Exhibit 1007.

4 A. I have it in front of me.

5 Q. Okay.

6 So I'd like to refer you to Figure 12 and 12B
7 in particular.

8 A. Okay.

9 I have Figure 12B in front of me.

10 Q. Okay.

11 And let's focus on the right half of that
12 figure. So in the right half of Figure 12B and starting
13 at the bottom, the structure N+P-N+, would you agree
14 that that is one memory cell?

15 A. As I indicated in my declaration at Paragraph
16 132 referring to the annotated version of Figure 12B
17 above, there are two flash -- NOR flash memory cells
18 comprising Floating Gate Transistors A and B or the
19 lower half that you're referring to is -- is Floating
20 Gate Transistor B. So that's -- that floating gate
21 transistor constitutes a memory cell, yes.

22 Q. And above that first memory cell, there's a
23 second memory cell shown by the structure N+P-N+;
24 correct?

25 A. Yes, that constitutes a second NOR flash memory

1 cell constituting a Floating Gate Transistor A,
2 Annotated A in this case.

3 Q. And both of those memory cells are on the same
4 pillar; correct?

5 A. Reading from Column 20 of the '994 patent
6 starting at Line 44 talking about Figures 12A and 12B,
7 it says, "... between adjacent cells after two or more
8 levels of pillar are formed as shown in Figure 12A and
9 12B."

10 Elsewhere, for example, up in Column 20, Line
11 9, Pillar 1000 is referenced and that is a reference to
12 Figure 10A which shows a single N+P-N+ stack. So what I
13 would presume is that from Lee's perspective, an N+P-N+
14 stack is a pillar and this Figure 12B shows two levels
15 of pillars.

16 Q. And so your testimony is that Level 1 and Level
17 2 are two separate pillars; is that -- am I
18 understanding you correctly?

19 MS. ARMOND: Objection. Misstates prior
20 testimony.

21 THE WITNESS: Please read the question back.
22 (Record read.)

23 THE WITNESS: I'm not finding an opinion to
24 that effect within my declaration, but certainly from
25 the passages of the '994 Lee patent that we've just

1 looked at, it would appear that that's Lee's
2 interpretation of Figure 12B.

3 Q. (By Mr. Kappos) Is that your interpretation
4 rehabilitation of Figure 12B as well?

5 A. Again, I've not rendered an opinion whether 12B
6 constitutes one pillar or two pillars, but I'm saying
7 that that's what Lee appears to say with regard to
8 Figure 12B in those passages I read previously.

9 Q. Okay.

10 MR. KAPPOS: I'd like to mark a new exhibit.
11 (Exhibit 1037 was marked for identification.)

12 Q. (By Mr. Kappos) I'm handing you a document
13 that's been marked as Exhibit 1037.

14 And I'll represent to you that this is an SEM
15 cross section of an SSD memory device. You know what an
16 SEM cross section is; correct?

17 MS. ARMOND: Hold on. Counsel, I need to
18 object. Since this is a new exhibit for the record, I
19 will object based on relevance. I'll object based on
20 authentication. And I might have more objections based
21 on how you are going to use this.

22 Q. (By Mr. Kappos) You understand what an SEM
23 image is; correct, sir?

24 A. I do understand that SEM stands for scanning
25 electron microscope and that it -- if that is how this

1 image was produced, then it is as you described.

2 Q. Okay.

3 I'll represent to you that this is an SEM cross
4 section of an SSD memory device and that each of the
5 orange boxes indicates a nonvolatile memory cell that's
6 fabricated on or above an -- an insulating layer.

7 So my question to you is: With those
8 assumptions, do these three memory cells as indicated by
9 orange boxes form one pillar or are there three separate
10 pillars?

11 A. Well, each one of these orange boxes are wider
12 than they are tall so none of the three orange boxes are
13 pillars.

14 Q. Okay.

15 Thank you. You can put that aside.

16 MR. KAPPOS: Can I get -- mark a new exhibit,
17 another new one.

18 Okay. I'm going to need another one as well
19 so.

20 (Exhibits 1038 and 1039 were marked for
21 identification.)

22 Q. (By Mr. Kappos) Okay.

23 I'm handing you a document that's been labeled
24 on one side, on the front side as 1038 and on the back
25 side it's labeled Exhibit 1039. And I want to ask some

1 questions about each of them.

2 MS. ARMOND: This is 1038?

3 MR. KAPPOS: Yes.

4 MS. ARMOND: And this is 1039?

5 MR. KAPPOS: Correct.

6 MS. ARMOND: Okay.

7 Q. (By Mr. Kappos) So can you look at 1038 first,
8 sir, the other side. Okay.

9 And so what this is, this figure was created --

10 MS. ARMOND: Oh, wait. Sorry. I will just
11 object. This is a new exhibit. I'd like to object that
12 it's outside the scope of his opinions. It hasn't been
13 authenticated and it's not relevant. Thank you.

14 MR. KAPPOS: Okay.

15 MS. ARMOND: And that's for both Exhibit 1038
16 and 1039.

17 Q. (By Mr. Kappos) Okay.

18 So may I refer you -- I haven't asked a
19 question yet.

20 A. I'm listening.

21 Q. Okay.

22 So I'd like you to look at Watanabe which is
23 Exhibit 1005.

24 A. I have 1005.

25 Q. Okay.

1 Figure 7 of Watanabe.

2 A. I am looking at Figure 7.

3 Q. Okay.

4 So Exhibit 1038 is two Figure 7s from Watanabe
5 stacked one over the other.

6 Do you recognize it as such?

7 A. I recognize Exhibit 1038 as two instances of
8 Figure 7 placed beside each other with some overlap
9 between the two vis-a-vis Item 106.

10 Q. Well, they're not placed beside each other.
11 They're placed above and below; correct? It's a
12 vertical stack, in other words.

13 MS. ARMOND: Is there's a question pending?

14 MR. KAPPOS: Yeah.

15 Q. (By Mr. Kappos) The question is: Do you
16 recognize them as a vertical stack above and below?

17 A. On this piece of paper, they're shown as beside
18 each other on this piece of paper.

19 Q. Okay.

20 So let's turn the piece of paper so that
21 they're -- it's oriented vertically the way you have it.

22 A. Okay.

23 Q. Okay.

24 Now, would you agree with me that the vertical
25 stack of memory cells would be taller than it is wide?

1 A. Well, it's the first time I've seen this
2 figure. It's not something I have opined upon and --
3 and reluctant to do so without further consideration of
4 the -- all the implications of this hypothetical that
5 you're putting in front of me.

6 Q. Is that the end of your answer?

7 A. Yes.

8 Q. Okay.

9 So you cannot tell me whether the vertical
10 stack of memory cells that's shown in Exhibit 1038 is
11 taller than it is wide?

12 A. Given that this is a slice -- a vertical slice
13 of a larger structure that we don't know what's on
14 either side, as shown here at least, that this is not a
15 figure I've opined upon or have seen before, and so I'm
16 not willing to form the opinion on the fly with regard
17 to this.

18 Q. And would your answer be the same for Exhibit
19 1039, again, oriented vertically with four memory cells
20 as shown in Watanabe's Figure 7?

21 A. Again, this is not a figure that's part of
22 Watanabe. It's not a figure I have seen before or
23 opined on, and so I'm reluctant to make any comment on
24 it at all.

25 Q. Okay.

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1 And so you cannot tell me whether Exhibit 1039
2 oriented in the vertical direction has memory cells -- a
3 memory cell stack that is taller than it is wide.
4 That's your testimony; correct?

5 MS. ARMOND: Objection. Asked and answered.

6 THE WITNESS: It's my testimony today that this
7 is new to me. I've not opined upon it. I'm here to
8 answer questions on my pre-existing opinions as
9 articulated in my declaration. This is not in my
10 declaration. I'm not willing to -- to -- to opine upon
11 it on the fly.

12 Q. (By Mr. Kappos) Okay.

13 Let's go back to your declaration. I think
14 we've spent a significant amount of time looking at
15 Paragraph 59, 60, 61. You referred to those several
16 times.

17 I want to start with Figure 1 that is in your
18 Paragraph 59 and -- yeah, you're there. Okay.

19 This is at Page 27. Is the SOI pillar
20 everything highlighted in purple in the Figure 1 that
21 you've annotated?

22 A. So the patent -- '702 patent refers to SIO
23 Pillar 124, as we've referred to many times already in
24 Figure 1. 124 is, again, referring to -- it points to
25 the middle portion of a three-region stack being an N+,

1 P and N+ and that, as I've noted in my Paragraph 59,
2 is -- refers to an SIO pillar [sic].

3 Q. Did you mean SOI pillar?

4 A. Yes. Thank you.

5 Q. So what about the Metal Contacts 121 and 122,
6 are those shaded purple?

7 A. It's hard to tell whether they were shaded
8 purple or just orange underneath. Does it matter?

9 Q. Well, are they part of the SOI pillar?

10 A. Again, this is not a figure that I've opined on
11 in any detail other than to -- for the purposes of
12 justifying or motivating my construction -- proposed
13 construction of SOI pillar.

14 But in this case, they are numbered 121 and 122
15 in Figure 1. They're not part of 124 in this --
16 apparently in this rendition. I don't find any support
17 in the '702 to indicate that that would be considered by
18 the author of the '702 patent to be part of the pillar.
19 Again, but it's not a -- it's not something that I've
20 opined on in my expert report.

21 Q. So your testimony is that you've not opined
22 about Figure 1 even though it's right there on Page 27
23 of your report and you've talked about it in your
24 report; is that correct?

25 A. I've not opined what constitutes a pillar in

1 Figure 701 [sic] and certainly what not -- I noted that
2 the figure -- that the '702 patent calls Item 124 an SOI
3 pillar and it points to that structure. I acknowledge
4 that.

5 I've not opined whether SOI Pillar 124
6 encompasses Metal Contacts 122 and 121 or not. That's
7 just not something that has been important for -- or
8 came up in my analysis of the other references that are
9 central to this matter.

10 Q. Okay.

11 I'm handing you Paper No. 9 in this
12 proceeding which is the Institution Decision in this
13 case. Are you familiar with the Institution Decision,
14 Paper 9?

15 A. I have seen it before, yes.

16 Q. Did you consider this Institution Decision in
17 forming your opinions expressed in your declaration?

18 A. Yes, decision granting institution of per inter
19 partes review, Institution Decision, Paper 9, is listed
20 as Item B in Paragraph 12, Materials Considered.

21 Q. And you understand this is the decision from
22 the Patent Trial and Appeals Board; correct?

23 A. I understand that.

24 Q. And they're sometimes abbreviated or referred
25 to as the PTAB; correct?

1 A. I understand that.

2 Q. Okay.

3 And so do you understand that the PTAB asked
4 whether a stackable add-on layer made by the stacking
5 method is structurally distinguishable from a layer that
6 is subsequently deposited or made by sequential
7 deposition?

8 Let me restate the question. Let me start
9 over.

10 Do you understand that the PTAB asked whether a
11 stackable add-on layer made by the stacking method is
12 structurally distinguishable from a layer that is
13 sequentially deposited or made by sequential deposition?
14 Do you recall that?

15 A. Not specifically. Can you point me at a
16 particular paragraph.

17 Q. Yes. Footnote 5.

18 A. Page?

19 Q. 9.

20 I'll read it to you. The last sentence says,
21 "The parties are encouraged to expressly construe this
22 term" -- referring to the term "stackable add-on
23 layer" -- "during trial and" -- and here's the part that
24 I'm referring to -- "to explain how a stackable add-on
25 layer is structurally distinguishable from a layer that

1 is sequentially deposited."

2 Did I read that correctly?

3 A. Yes, you did.

4 Q. Okay.

5 And so you did not address the issue of
6 structural distinctions anywhere in your declaration;
7 correct?

8 A. Yes, I was not asked to address that issue in
9 my expert report and I did not.

10 Q. Okay.

11 And in your opinion, are there structural
12 distinctions between a stackable add-on layer made by
13 the stacking method and a layer that is sequentially
14 deposited?

15 A. Again, I've not been asked to consider this
16 question and I did not and have not formed an opinion on
17 whether there is a structurally distinguishable aspect
18 between those two things.

19 Q. Back to your declaration, which is Exhibit
20 2029, we spoke earlier about Paragraph 79 and 80 so I'll
21 let you refer back to that portion. And in particular,
22 I want to ask about Paragraph 80.

23 In Paragraph 80, you refer to the landing pad
24 at the top of each layer. Do you see that?

25 A. More precisely I say in Paragraph 80 of my

1 declaration that "from Watanabe's Figure 6A to 6D, the
2 landing pads at the top of each layer to which the vias
3 from the next layer above have to make contact are
4 small" --

5 (Stenographer clarification.)

6 THE WITNESS: Vias.

7 -- "colon, less than 2x the minimum feature
8 size."

9 Q. (By Mr. Kappos) Okay.

10 So if we look at Figure 6A in Watanabe, is the
11 fanned-out region, is that what you're referring to as
12 the landing pads?

13 A. Yes. That's not a term that Watanabe uses, but
14 it is something that a POSITA would recognize as landing
15 pads vis-a-vis for Figure 6C or 6D. It is the points at
16 which there is a connection between vertical wires
17 through one layer and connecting to a vertical wire in
18 the adjacent layer.

19 Q. And the fanned-out region I'm referring to is
20 right where the numeral 91 is pointing to in Figure 6A.

21 Do you see that?

22 A. Yes. Although 91 is actually referring to the
23 hole that is subsequently filled with metal, 93, in --
24 prior to the aggregation of the layers together by
25 bonding.

1 Q. Okay.

2 So the top of that -- of that -- of 91 is
3 fanned out. Do you -- is there a better term to use
4 than it's -- it's wider? Do you see how the dimension
5 increases?

6 A. Yes, I understand fanned out. Your question is
7 clear.

8 Q. Okay.

9 You understand. Okay.

10 So is the -- the landing pad that is formed
11 using the stacking method, is that different from the
12 contacts that are formed in the sequential deposition
13 method, in particular insofar as the fanned-out region
14 exists for the stacking method?

15 A. In the laminating method as illustrated by
16 Figures 5A through 5E, the metalization is only
17 performed after all of the other layers are manufactured
18 as shown in Figure 5C and then holes are created as
19 shown in 5D.

20 THE WITNESS: Your phone's beeping.

21 MR. KAPPOS: Yeah, just ignore it.

22 THE WITNESS: I'll try.

23 MR. KAPPOS: Do you want to pause for a minute?

24 THE WITNESS: Is it going to stop beeping?

25 MR. KAPPOS: I can disconnect and reconnect.

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1 MS. ARMOND: We're almost to lunch.

2 MR. KAPPOS: Why don't we -- do we want to just
3 go off the record here and I'll make a new connection
4 for after lunch?

5 THE WITNESS: Sure.

6 MR. KAPPOS: Is it here yet?

7 MS. ARMOND: I think it is, I'm told.

8 MR. KAPPOS: Okay.

9 All right. Let's take a lunch break and I'll
10 ask this question again.

11 THE WITNESS: That works for me.

12 MR. KAPPOS: Thanks.

13 THE VIDEOGRAPHER: The time is 12:30 p.m. We
14 are now off the record.

15 (Lunch recess taken 12:30 p.m. to 1:26 p.m.)

16 THE VIDEOGRAPHER: The time is 1:26 p.m. We
17 are now back on the record.

18 Q. (By Mr. Kappos) Welcome back.

19 A. Thank you.

20 Q. Before the lunch break, we were talking about
21 Watanabe's Figure 6A and Paragraph 80 in your
22 declaration which is Exhibit 2029, and I believe that we
23 were discussing the landing pads in the stacking method
24 being fanned out.

25 Do you remember that discussion?

1 A. Yes.

2 Q. And this characteristic of the landing pads of
3 the electrical connections being fanned out is different
4 from the contacts that are formed using the sequential
5 deposition method; correct?

6 THE WITNESS: Could you please repeat the
7 question.

8 (Record read.)

9 THE WITNESS: Well, if we look at the
10 lamination method of Watanabe, we don't find anything
11 comparable, because the vertical --

12 (Stenographer clarification.)

13 THE WITNESS: -- via holes are, for example, 83
14 and 84 in Figure 5D are formed at the very end and so
15 there are no intermediate landing pads or contacts, to
16 use your term, in the laminating method.

17 Q. (By Mr. Kappos) And that means that the
18 fanned-out landing pads is, in fact, a structural
19 distinction between the stacking method and the
20 sequential deposition method; correct?

21 A. The landing pads of the stacking method that I
22 talk about in my declaration in Paragraph 80 have no
23 comparable structures in the figures associated with the
24 lamination method of Watanabe.

25 Q. And so in your declaration, you talk about the

1 landing pad being less than two times the minimum
2 feature size.

3 Do you recall that discussion?

4 A. Yes. In particular in the first sentence of my
5 Paragraph 80 of my declaration, I say that "the landing
6 pads at the top of each layer to which the vias from the
7 next layer above have to make contact are small, less
8 than 2x the minimum feature size."

9 Q. So in your opinion, the horizontal dimension of
10 the landing pad would be less than two times the
11 horizontal dimension of the feature which is Item 72; is
12 that correct?

13 A. Did you mean the word "feature" in your
14 question?

15 Q. Yeah, because your Paragraph 79 refers to
16 minimum feature size and then it refers to Item 72. Is
17 Item 72 the feature?

18 A. Item 72 in Figure 6A of Watanabe points to the
19 gate of a transistor in the substrate that is, as I
20 describe in my declaration in Paragraph 79, what a
21 POSITA would recognize as the minimum feature size.
22 It's just a way of characterizing the -- the horizontal
23 dimensions within the integrated circuit.

24 And that as shown in Figure 6B, for example, or
25 rather 6D better, the landing pad dimensions are shown

1 to be less than twice the gate width of those
2 transistors in the substrate.

3 Q. Okay.

4 And so I want to make sure I understand what
5 dimension you're measuring that in. And so the
6 horizontal dimension of the landing pad would be less
7 than two times the horizontal dimension of Item 72 which
8 is the feature; is that correct?

9 A. Yes. The -- the horizontal dimension of the
10 top of the landing pad is shown in Figure 6D as being
11 less than twice the horizontal dimension of the gate of
12 the transistor which is best identified as Item 72.

13 Q. So and then you say in your declaration, "If
14 the landing pads are much larger than the minimum metal
15 spacing or the minimum via spacing," what is the
16 "minimum metal spacing" to which you're referring?

17 A. In any integrated circuit, there are -- in the
18 fabrication of the integrated circuit there are design
19 rules which specify minimum and in some rare cases
20 maximum separations between certain items. One such
21 design rule is the minimum spacing between separate
22 pieces of metal on a -- on the same layer of
23 metalization.

24 Q. Okay.

25 So can you give me an example of what that

1 dimension would be with reference to Watanabe's figures.

2 A. Watanabe does not include any figures that
3 illustrate effectively the minimum wire separation on a
4 given layer of metal.

5 Q. So looking at Watanabe's Figure 6A through 6D,
6 for example, do any of those show metal spacing?

7 A. Figures 6A through 6D of Watanabe do show
8 metal, in particular in the form of vias and with regard
9 to horizontal metal connections at -- indicated by Item
10 95 in Figure 6D. But the Item 95 which is shown --
11 which is listed as the Second Interconnect Wire 95, is
12 one piece of wire and it's not -- it does not show two
13 pieces of wire that are minimally close together without
14 touching.

15 Q. Is there anywhere in Figures 6A to 6D that
16 shows spacing between wires that are not touching?

17 A. No. There is a showing of minimum via spacing
18 but not minimum metal spacing.

19 Q. And there's no showing of metal spacing?
20 Setting aside whether it's minimum or not, does it show
21 metal spacing?

22 A. I don't believe so. I don't see any multiple
23 pieces of metal on a single planar level. As, for
24 example, Item 95 is the only piece of metal that's
25 deposited horizontally and is -- would be considered

1 subject to a minimum metal spacing relative to another
2 piece of metal.

3 Q. And would your answer be the same for the
4 remaining figures of the Watanabe patent?

5 A. With regard to Figure 4, in both the top view
6 and the cross-section view, Item 13 is a -- described as
7 a data line and there are two data lines running
8 parallel to each other in Figure 4A. It doesn't say
9 that it is metal. It's probably polysilicon. If it
10 were metal -- no, it can't be metal. I'm sorry. I
11 retract my answer. Let me start again.

12 No, I'm not seeing any in any of the figures
13 metal-to-metal spacing shown as part of one of the
14 figures.

15 Q. But you mentioned that via spacing is shown?

16 A. Yes, there are many vias shown in the figures.
17 Some of them are close together. Some of them are
18 further apart.

19 Q. What's the best figure for us to look at to
20 understand the via spacing?

21 A. An example showing via spacing would be
22 Figure 6D --

23 Q. Okay.

24 A. -- where you have Second Interconnect 95
25 connecting several vias that communicate signals

1 vertically down to -- from the top layer of interconnect
2 down to different layers further below. Those vias,
3 some of them are closer together and some of them are
4 further apart. There are four in particular.

5 Do you see the four that I'm referring to?

6 Q. I do.

7 A. So the middle two of them are close together
8 and appear to be probably minimally spaced, but there's
9 no actual textual representation that those vias are, in
10 fact, separated by the minimum allowed via spacing for
11 this process.

12 Q. And so the via spacing refers to the horizontal
13 distance between two of those vertical lines; is that
14 correct?

15 A. The hor- -- the via spacing refers to the
16 horizontal spacing between two adjacent vias.

17 Q. In your declaration, we spoke earlier about
18 Figure 4 from the '702 patent which you reproduced on
19 Page 28 of your declaration.

20 A. I'm on Page 28.

21 Q. Okay.

22 And you recall we discussed Figure 4 earlier in
23 connection with our pillar discussion; correct?

24 A. Yes, we did.

25 Q. And I think you referred to something that you

1 called the top half. Can you explain to me what is the
2 top half.

3 A. I was referring to the -- let me start again.

4 In our discussion this morning with regard to
5 Figure 4, I was noting that the Item 124 is pointing to
6 an N doped region and below it is a P doped region and
7 below that is an N+ dope region that is connected to the
8 bit line and we agreed that that portion was a memory
9 cell, a DRAM memory cell, not a very good one but a DRAM
10 memory cell, and that that portion was what I was
11 referring to as the top half.

12 Q. Is there a minimum structure that you need to
13 have in order to constitute a pillar?

14 A. As I discuss in my declaration with regard to
15 the proposed construction of SIO pillar [sic], I note
16 that the plain and ordinary meaning of pillar is
17 something that is taller than wide and that is the only
18 aspect for the plain and ordinary meaning of pillar.

19 Q. Okay.

20 So could a single N region, the one that's at
21 the top that you just pointed to a moment ago, let's say
22 I had a structure that only had that N region, in your
23 opinion would that constitute an SOI pillar?

24 A. As I said many times this morning, I've not
25 formed any opinions about the details of these figures

1 from the '702. I was using them as an example in my
2 articulation of the rationale for the proposed
3 construction of SIO pillar [sic]. I was not willing to
4 say whether the SIO pillar [sic] was top half or the
5 whole thing because I hadn't formed an opinion to that
6 effect.

7 Similarly, I have not formed an opinion as to
8 whether just the N portion, the source of that top
9 transistor by itself would be considered an SIO pillar
10 [sic]. It's not something I was asked to opine on and
11 did not.

12 Q. And do you have any opinion on that matter as
13 you sit here right now?

14 A. As I just said, I was not asked to form any
15 opinions with regard to the structures shown in the
16 figures of the '702 patent and I have not done so.

17 Q. And you've referred a number of times to "SIO
18 pillar." I assume you mean SOI pillar when you've done
19 that?

20 A. Yes, that is a consistent brain freeze on my
21 part. I apologize.

22 Q. In order to have an SOI pillar, do you have to
23 have at least one memory cell?

24 A. As I opined in Paragraph 63 of my declaration,
25 for the context of the present proceeding, the S -- and

1 the '702 patent, in my opinion, an SOI pillar is a
2 silicon-on-insulator structure that is taller than it is
3 wide. There is no specific mention of -- of memory
4 cells within that proposed construction.

5 Q. And therefore a memory cell is not required to
6 have an SOI pillar in your opinion; correct?

7 A. As I just said, in -- as I've articulated in
8 Paragraph 63, my opinion is that an SOI pillar is a
9 silicon-on-insulator structure that is taller than it is
10 wide and that proposed construction does not include the
11 concept of a memory cell.

12 Q. In your declaration, you state that "the
13 essential challenge of making high-density, low-cost
14 DRAMs is to make the ratio of the capacitance of the
15 storage capacitor to that of the bit line as large as
16 possible."

17 Do you recall that discussion?

18 A. Yes. What paragraph is it in, please?

19 Q. I believe it's in 84.

20 A. I am there.

21 Q. Okay.

22 And do you recall the discussion that you had
23 that I just read concerning the essential challenge?

24 A. Yes.

25 Q. Now for NAND architecture as opposed to DRAM,

1 for NAND architecture, there is no storage capacitor
2 needed; correct?

3 A. Yes. The mechanism by which information is
4 stored is dramatically different in DRAM than in a NAND
5 flash or other EEPROM organization.

6 Q. And so the ratio that you discussed in
7 Paragraph 84 is not a consideration for NAND
8 architecture; correct?

9 A. That ratio being the ratio of the storage
10 capacitor to the bit line capacitance in DRAMs does not
11 have a direct analogous ratio for NAND flash memory
12 arrays because there is no storage capacitor. There are
13 other capacitance ratios that are critical for ensuring
14 that the speed of the device is -- meets specification,
15 but there's not been a need to opine on those aspects of
16 NAND flash integrated circuit design in my declaration.

17 Q. And so because there is no analog to the ratio
18 of the capacitance of the storage capacitor to the bit
19 line, there is no analog to that ratio in NAND flash,
20 this consideration is not an issue for NAND
21 architecture; correct?

22 MS. ARMOND: Asked and answered.

23 THE WITNESS: As I said just a moment ago,
24 there is no analog, as you suggest, between -- for the
25 capacitance ratio of the storage capacitance to the bit

1 line that exists in DRAMs.

2 In NAND flash, there are other ratios, other
3 capacitances that are critical -- as critical to NAND
4 flash design as that ratio is to DRAM design.

5 Q. (By Mr. Kappos) And because there is no
6 analog, the ratio is not a consideration for NAND
7 architecture; correct?

8 MS. ARMOND: Same objection.

9 THE WITNESS: That particular ratio does not
10 exist in the -- for the design of a NAND flash, but
11 there are other ratios and other design considerations
12 that are comparably significant.

13 Q. (By Mr. Kappos) And so the ratio that we've
14 been talking about, that specific ratio that does not
15 exist, is not a consideration for NAND architecture;
16 correct?

17 A. As I've said several times already, that ratio
18 has no analogous ratio within the design of NAND flash
19 memory devices.

20 Q. And, therefore, that ratio is not a
21 consideration in the design of NAND flash; correct?

22 A. Nothing that exists in the design can be of
23 consideration so --

24 Q. In other words --

25 A. -- my answer stands.

1 Q. In other words, if it doesn't exist, it can't
2 be a consideration in the design of NAND flash; correct?

3 MS. ARMOND: Counsel, please don't interrupt
4 the witness when he's answering a question.

5 THE WITNESS: I believe I've answered your
6 question. That ratio has no analog in the design of
7 NAND flash memory design -- memory circuits.

8 Q. (By Mr. Kappos) So, referring again to the
9 '702 patent, which is Exhibit 1001, you understand that
10 Claim 1 recites DRAM memory; correct?

11 A. Yes. The last element of Claim 1 reads,
12 "Wherein the memory cell is a DRAM having at least one
13 transistor."

14 Q. And Claim 8 recites SRAM memory cells; correct?

15 A. Similarly, the last element of Claim 8 reads,
16 "Wherein the memory cell is an SRAM having at least one
17 negative differential resistance device."

18 Q. And Claim 13 recites non-volatile memory cells;
19 correct?

20 A. Similarly, the last element of Claim 13
21 recites, "Wherein the memory cells are non-volatile
22 memory cells having at least one transistor."

23 Q. The '702 specification describes a fabrication
24 process to make a stackable add-on layer; correct?

25 A. Well, for example, the -- in Column 4 of the

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1 '702 patent, starting at Line 53, it reads, "In this
2 context the SIO" -- "SOI layer may be thought of as an
3 attachment layer or stackable add-on structure which is
4 suitable for bonding to a semiconductor structure
5 already containing devices and/or interconnections."

6 And then subsequently to that, there are
7 further discussions as to examples of such layers.

8 Q. And that process, performing a stackable add-on
9 layer, would be applicable to all three of DRAM, SRAM,
10 and non-volatile memory; correct?

11 A. There are certainly embodiments within the '702
12 that relate to all three of those memory types. And in
13 general, they are aggregated similarly. There are
14 going -- obviously going to be some differences between
15 those processes to build each one of those that is
16 specific to the memory type so that those processes that
17 you refer to are not identical.

18 Q. And a person of skill in the art would know how
19 to apply those manufacturing processes to make all three
20 of DRAM, SRAM, and non-volatile memory; in other words,
21 they could take into account those differences; correct?

22 A. I haven't opined on the enablement of those
23 processes in the '702 patent. A POSITA would be able to
24 read the '702 patent and respectively build the three
25 types of memory devices according to the teachings of

1 the '702 patent.

2 Q. In both DRAM and non-volatile memory, each cell
3 is individually addressed; correct?

4 A. What do you mean by "individually addressed"?

5 Q. Have you heard the term in connection with
6 memory cells of addressing the memory cells?

7 A. Yes.

8 Q. What does that term mean?

9 A. I don't believe it's shown up in my
10 declaration. If it has, will you point me at it.

11 Q. I don't know if it has either. I'm just asking
12 whether you have a general understanding of what the
13 term "address" means in the context of memory.

14 A. Yes, I do.

15 Q. Okay.

16 What is your understanding?

17 A. Every memory cell or collection of memory cells
18 has an address that allows it to be accessed in most
19 memory devices. There are many memory devices where
20 that concept doesn't exist, but certainly in -- in many
21 it does.

22 Q. And in DRAM, are the memory cells addressed
23 individually? In other words, does each memory cell
24 have his own unique address?

25 A. No, generally not. In the olden times, yes,

1 but not recently.

2 Q. What about a non-volatile memory?

3 A. Similarly.

4 Q. And so you're saying in both DRAM and
5 non-volatile memory, the memory cells are not separately
6 addressed?

7 A. Yes, that's true.

8 Q. And you mentioned that it used to be different.

9 A. Long time ago.

10 Q. How long ago?

11 A. Three decades at least.

12 Q. At that time DRAM contained memory cells that
13 were individually addressed; is that correct?

14 A. There were some DRAM at that time that were
15 every DRAM cell had a unique address.

16 Q. And the same goes for non-volatile memory at
17 that time?

18 A. No, I don't think that's necessarily true. I
19 can't think of an example of a non-volatile memory that
20 where every cell was individually addressed in that time
21 frame. But I could be wrong. It was a long time ago.
22 It's not a subject that was important for the creation
23 of my declaration. I have not opined on that.

24 Q. In the '702 specification at Column 4, Lines 1
25 to 4, let me direct you to that text and tell me when

1 you're there.

2 A. '702 patent?

3 Q. Yes.

4 A. I'm at Column 4.

5 Q. Okay.

6 At the very beginning, the first line, do you
7 see the statement that reads, "Furthermore, various
8 particular features, structures, operations, or
9 characteristics may be combined in any suitable manner
10 in one or more embodiments"?

11 Did I read that correctly?

12 A. Yes, you did.

13 Q. And this means that features illustrated for
14 any one embodiment would be understood by a person
15 skilled in the art to be applicable to all the other
16 embodiments; correct?

17 A. No. I think that's an overstatement and
18 putting way too much weight on the word "may." These
19 memory types are sufficiently different that there is a
20 great deal that does not transfer from one memory type
21 to another.

22 Q. Well, let me give you a specific example then.
23 If we look at Figure 23 in the '702 patent --

24 A. I'm looking at Figure 23.

25 Q. Figure 23 illustrates a memory cell that can be

1 used as DRAM or as non-volatile memory; correct?

2 A. Knowing what I do about how DRAMs work, I do
3 not understand and disbelieve the articulation in Column
4 9 of the '702 patent with regard to the DRAM operation
5 of the embodiment of Figures 23 and 25. These would not
6 work effectively as a DRAM device as described in Column
7 9, Lines 23 through 50.

8 Q. Column 9, Line 27 which refers to Figure 23,
9 states that this embodiment in here, I'll quote "could
10 work as a DRAM and/or a non-volatile memory device."

11 Did I read that correctly?

12 A. Yes, that's what it says there.

13 Q. And with reference to Figure 25, Column 9,
14 Lines 40 to 41 say "such a device could work as a DRAM
15 or as a non-volatile memory device."

16 Did I read that correctly?

17 A. Yes.

18 Q. And then further down, with reference to Figure
19 27, it states at Line 51 that "Figure 27 shows two
20 vertical memory cells of the type shown in Figure 23";
21 correct?

22 A. That's what it says there.

23 Q. And, therefore, because Figure 23 notes that
24 the device could work as a DRAM and/or non-volatile
25 memory, the same is applicable to Figure 27 as well;

1 correct?

2 A. That's what it says. But referring back to
3 what it says in the previous paragraph with regard to
4 Figures -- Figure 23 and its circuit diagram, 24, about
5 how in a, quote, "DRAM," close quote, operation it
6 stores charge in the P doped region. That would not
7 make for an effective DRAM. If that were the case,
8 there would -- we would not build DRAMs with capacitors
9 because the capacitors are irrelevant and not necessary
10 for the operation of DRAM.

11 So this statement here in Column 9 is -- would
12 be viewed with great skepticism by a POSITA with regard
13 solely to DRAM operation of the embodiments of Figure 23
14 and 25.

15 Q. So are you saying the '702 patent is
16 inoperative with respect to DRAM?

17 A. What I'm saying is that this -- these two
18 particular embodiments of Figure 23 and 25, to the
19 extent that they are described as operable as DRAMs
20 solely, that that portion of the disclosure of Column 9
21 would not ring true for a POSITA because there's not
22 sufficient charge storage capacity within the P doped
23 region as described, for example, in Column 32 [sic] of
24 Column 9.

25 Q. The next column over, Column 10, starting at

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1 Line 29 states, "Since the body of SOI pillar is usually
2 floating, the non-volatile could work as a DRAM device."

3 Did I read that correctly?

4 A. What line again, please?

5 Q. Line 29 of Column 10.

6 A. So this Column 10 paragraph is reiterating as a
7 conclusion the statements of Column 9. And as I've just
8 spoken, a POSITA would find that to be highly suspect in
9 terms of the ability of that structure to operate
10 effectively as a DRAM.

11 Q. And just so I get the record correct, the
12 sentence begins on Column 10, Line 31, which says,
13 "Since the body of SOI pillar is usually floating, the
14 non-volatile could work as a DRAM device."

15 Did I read that correctly?

16 A. You read that correctly. But, again, the body
17 of the SIO pillar of, for example, the embodiment of
18 Figure 23 is -- is not purely floating, but it's
19 connected through the source and drain to other nodes.
20 So it -- and regardless of that, the amount of charge
21 that can be stored in that P -- floating P region is
22 very small in comparison to the capacitors that we have
23 in DRAMs or, for example, in the embodiments -- other
24 embodiments.

25 But I want to reiterate that, you know, I've

1 not opined on this -- these embodiments of the '702 or
2 their operation. It's not been central to or even
3 tangential to my analysis of the references at issue
4 here and --

5 Q. Okay.

6 Let me direct your attention to Column 2,
7 starting at Line 4. There it states, and I quote, "In
8 another aspect of the present invention, dynamic random
9 access memory (DRAM) cells, static random access memory
10 (SRAM) cells, non-volatile memory cells, and similar
11 structures may be formed in a stackable add-on layer for
12 use in conjunction with the separately fabricated
13 substrate."

14 Did I read that correctly?

15 A. Yes, you did.

16 Q. So, for example, a process step illustrated
17 specifically for DRAM could be applied by a person of
18 skill in the art to non-volatile memory; correct?

19 A. Again, I want to reiterate that this is not a
20 subject matter that I've opined upon in my declaration.
21 Regardless of that, your statement is not true.

22 Q. Why not?

23 A. Because there are many steps in the fabrication
24 of DRAM cells as would be understood by a POSITA that
25 are not applicable to non-volatile and flash memory

1 devices in particular.

2 Q. But a POSITA would know which of those steps is
3 not applicable; correct?

4 Let me rephrase the question.

5 A person skilled in the art in 2004 reading the
6 '702 patent would know which of those process steps are
7 not applicable to non-volatile memory; correct?

8 A. Presumably, but, again, I've not formed an
9 opinion on this subject matter and that may or may not
10 be true.

11 Q. At the time of the '702 patent, so in 2004, it
12 was well known how to fabricate a DRAM cell, an SRAM
13 cell, or a non-volatile memory cell; correct?

14 A. The design and manufacture of each of those
15 different types of memories were their own and separate
16 bodies of art and were generally considered distinct
17 but --

18 Q. And -- and were well known.

19 MS. ARMOND: Wait. Do not interrupt the
20 witness. He's still answering, Counsel.

21 Q. (By Mr. Kappos) Go ahead. I didn't mean to
22 interrupt you. Sorry.

23 THE WITNESS: Read back my answer as far as I
24 got, please.

25 MS. ARMOND: Would you read the question and

1 answer, please.

2 (Record read.)

3 THE WITNESS: They were generally considered
4 distinct, but there were overlap. Individual POSITAS
5 would be specialized in one or another of these arts and
6 would have limited exposure to the other memory types as
7 a matter of their day-to-day activities.

8 Q. (By Mr. Kappos) A person skilled in the art in
9 2004 would have known the distinctions that you're
10 referring to between DRAM and non-volatile memory;
11 correct?

12 A. A -- a person of ordinary skill in the art
13 would have knowledge of the differences at various
14 different levels of abstraction between those different
15 memory types.

16 Q. And the architecture to implement DRAM versus
17 SRAM versus non-volatile memory was also well known in
18 2004; correct?

19 A. A POSITA in 2004 would know that there are
20 differences in architecture and circuit design and
21 process across those three different types of memories,
22 would have facility in and greater knowledge in one of
23 the three, would be aware of differences between them
24 but not necessarily have competence in all of them.

25 Q. The '702 patent discusses NAND among other

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1 types of memory cells; correct?

2 A. You want to point me in a particular place?

3 Q. I don't know. I'm just talking about in
4 general. I mean, I think, at the very least some of the
5 later figures do.

6 A. Yes, there's a reference to NAND architecture
7 flash memory products in Column 10, paragraph starting
8 Line 3 going through Line 11.

9 Q. Okay.

10 And so once a person skilled in the art has
11 decided to implement memory using NAND architecture,
12 they would know how to implement the -- any of the
13 memory cells described in the '702 patent in that NAND
14 architecture; correct?

15 THE WITNESS: Can you repeat the question,
16 please.

17 (Record read.)

18 (Stenographer clarification.)

19 Q. (By Mr. Kappos) So once a person skilled in
20 the art has decided to implement memory using NAND
21 architecture, they would know how to implement that
22 architecture using any of the memory cells described in
23 the '702 patent; correct?

24 A. Again, this is not a subject matter that I've
25 opined upon as far as the detailed implications of the

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1 disclosure of the '702 patent and what a POSITA would or
2 would not have been able to do as far as combining
3 different embodiments thereof.

4 That said, no, that a POSITA knowing --
5 deciding to do something in a NAND architecture would
6 not be able to use any of the memory device types or
7 storage cells in order to implement that NAND flash
8 architecture. That's a nonsensical idea.

9 MS. ARMOND: We've been going about an hour.

10 THE WITNESS: Yeah, let's take a break, please.

11 MR. KAPPOS: Okay.

12 THE VIDEOGRAPHER: The time is 2:31 p.m. We
13 are now going off the record.

14 (Recess taken from 2:31 p.m. to 2:42 p.m.)

15 THE VIDEOGRAPHER: The time is 2:42 p.m. We
16 are now back on the record.

17 Q. (By Mr. Kappos) Welcome back.

18 A. Thank you.

19 Q. Staying within the '702 patent, I'd like to
20 direct your attention to Column 6, Lines 13 to 25, which
21 addresses wafer alignment.

22 Do you see that?

23 A. I see that.

24 Q. The '702 patent mentions wafer alignment marks,
25 bump-type alignment structures, and notch alignment;

1 correct?

2 A. All of those phrases exist within that
3 paragraph, yes.

4 Q. But the patent -- the '702 patent does not give
5 details about how to implement these techniques for
6 wafer alignment; correct?

7 A. I don't recall whether there's additional
8 detail about these structures and techniques elsewhere
9 within the patents or whether there is -- a POSITA would
10 need additional details in order to implement these
11 structures. It's not a subject matter of my
12 declaration. I have not opined on the adequacy of this
13 description.

14 Q. And because a person skilled in the art would
15 have known how to perform wafer alignment by these
16 techniques without additional details, the '702 patent
17 didn't need to give additional details; correct?

18 A. Again, this is not a subject matter of my
19 declaration. I've not considered whether additional
20 details would be necessary for a POSITA to perform these
21 operations to perform this alignment and so I can't
22 really answer that question.

23 Q. As you noted, the phrases that I mentioned
24 appear in that paragraph, but there are no additional
25 details about how to implement those techniques;

1 correct?

2 A. As I just testified a moment ago, I don't know
3 if there are additional details elsewhere. It's not a
4 subject matter of my declaration. I've not considered
5 whether these -- this description is sufficient for a
6 POSITA to perform the necessary alignment.

7 Q. Are you familiar with alignment marks,
8 bump-type alignment structures and notch alignment from
9 your work in the semiconductor field?

10 A. Generally speaking, yes.

11 Q. When did you become familiar with these
12 techniques?

13 A. I don't remember specifically when the -- I
14 became familiar with alignment techniques. I mean, I
15 have been following semiconductor manufacture processing
16 techniques generally for decades. At what point
17 individual concepts came into my possession, I -- I
18 couldn't tell you.

19 Q. But the alignment techniques, you were familiar
20 with these techniques by at least 2004; correct?

21 A. I presume so. But I have no recollection
22 specifically one way or the other. It might have been
23 afterwards. It might have been before. I can't tell
24 you.

25 Q. The techniques of using wafer alignment marks,

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1 bump-type alignment structures, and notch alignment were
2 known before the 2004 filing date of the '702 patent;
3 correct?

4 A. Again, it's not a subject matter of my
5 declaration. I haven't researched when those techniques
6 became into the common knowledge of a POSITA in the
7 field and so I really can't answer your question.

8 Q. What is notch alignment?

9 A. My understanding of notch alignment is that
10 there's a notch on the edge of a wafer that's used to
11 align one wafer to the other. But, again, this is not a
12 subject matter of my declaration and I haven't refreshed
13 my memory as to notch alignment techniques and that's
14 all.

15 Q. What about bump alignment? Can you explain
16 what that is?

17 A. That is rare. My understanding is that it
18 relates to having a -- a bump on one of -- one surface
19 of a wafer in order to allow it to be aligned with
20 another.

21 Q. Is that different from notch alignment?

22 A. Yes, I believe it's a different technique.
23 But, again, it's not a subject matter that I have
24 reviewed recently, have not opined upon in my
25 declaration. I really am not certain of -- to what

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1 extent it's different or to what extent one is used over
2 the other in -- and in what circumstances.

3 Q. Is it different in that a bump refers to a
4 protrusion, whereas a notch refers to a recess?

5 A. Again, it's not a subject matter in my
6 declaration. I haven't researched these things. That's
7 generally my understanding, but I have not opined on
8 that.

9 Q. What is the difference between wafer alignment
10 marks versus notch alignment or bump alignment?

11 A. So in the paragraph that you're referring to in
12 the '702, Column 6, Lines 13 through 26, it refers to
13 wafer alignment structures as used in photolithographic
14 processes and, as such, those are directed towards
15 aligning photolithographic masks to either a wafer or to
16 a particular die placed on the wafer and that's a -- an
17 entirely different alignment problem than we're talking
18 about here with wafer alignment.

19 But, again, this is not the subject matter of
20 my declaration. I have not researched these topics
21 recently, and so I'm going strictly by the -- my general
22 knowledge and this paragraph in Column 6 of '702 patent.

23 Q. So the alignment marks are used in an entirely
24 different process relating to photolithography; is that
25 correct?

1 A. That's what it says in Column 6, yes.

2 Q. Do you agree with that?

3 A. I certainly understand how, as part of
4 photolithographic processes, you have to align masks to
5 wafers or to die positions on a wafer. That is an
6 intrinsic part of semiconductor processing generally.

7 Q. And you refer to that as an entirely different
8 process because the '702 patent does not relate to the
9 photolithic -- photolithographic process of sequential
10 deposition; correct?

11 A. Again, this is not a subject matter that I've
12 researched or opined upon in this matter. But, no,
13 the -- those are different processes because they are
14 different processes, not because of what the '702
15 mentions or does not mention in the rest of the
16 specification.

17 Q. The '702 patent requires bonding between the
18 stackable add-on layer and the dielectric layer of the
19 substrate; correct?

20 A. Certainly the claims that we are discussing
21 today, Claim 13 in particular, requires in Element 13D,
22 I believe, a stackable add-on layer being bonded to the
23 dielectric layer. So to that extent, the answer is yes.

24 Q. Have you heard of a process called
25 electromagnetic induction heating?

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1 A. I've certainly not opined on it with -- in
2 regards to this -- this declaration of this matter.

3 Q. Have you ever heard of that process?

4 A. I have heard of it, but that's about the extent
5 of it.

6 Q. Do you know if that's a process that could be
7 used for bonding?

8 A. I'm not willing to opine on whether it's useful
9 for anything in particular to today because I've just
10 not reviewed that in recent times.

11 Q. When were you first contacted about appearing
12 as an expert in this case?

13 A. Sometime late last year. Don't remember the
14 exact date.

15 Q. Do you remember what month it was?

16 A. I think it was December, but I'm not sure.
17 Might have been earlier.

18 Q. Before that date, had you ever heard of BeSang?

19 A. I have no recollection of having heard of
20 BeSang, but, you know, there's so many companies in the
21 electronics world I -- I might have and had forgotten.
22 I don't know.

23 Q. Had you ever heard of the '702 inventor
24 Sang-Yun Lee?

25 A. Again, great many people have eminence within

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1 the field. I may have read a paper or had some contact
2 indirectly. I have no recollection of such a contact.

3 Q. Does BeSang have a commercial semiconductor
4 memory product on the market?

5 A. I don't know.

6 Q. Do you know if BeSang has any product on the
7 market?

8 A. I don't know. It's not relevant to my opinion
9 in this matter.

10 Q. Has BeSang licensed the '702 patent to any
11 company?

12 A. I am not purview to any of their licensing
13 arrangements. It's outside the scope of my declaration
14 and opinions in this matter.

15 Q. But you're not aware of any licenses; correct?

16 A. No, I'm not aware of any licenses one way or
17 the other, inbound or outbound, involving BeSang.

18 MR. KAPPOS: I'm handing a document that's been
19 marked Exhibit 1040.

20 (Exhibit 1040 was marked for identification.)

21 MS. ARMOND: I'll object on the grounds of
22 relevance.

23 Q. (By Mr. Kappos) This is an order from an
24 International Trade Commission case in the matter of
25 certain semiconductor chips and products containing

1 same. Initial determination is the case that involved
2 Rambus.

3 Did you appear in this matter, Dr. Przybylski?

4 A. Give me a moment.

5 (Stenographer clarification.)

6 THE WITNESS: Yes, I apparently was.

7 Q. (By Mr. Kappos) And this determination is
8 dated March of 2012; correct?

9 A. Yes, on the front page it says "March 2nd,
10 2012."

11 Q. Okay.

12 Let me direct your attention to Page 146.

13 A. I'm on 146.

14 Q. Okay.

15 And do you see where it says "Rambus'
16 Misrepresentations"?

17 A. I see Section G, Rambus' Misrepresentations,
18 yes.

19 Q. Okay.

20 I want to look at the paragraph just above that
21 heading that you just referred to. In the paragraph
22 just above, the judge found, in effect, and I quote,
23 "Dr. Przybylski does not remember the claim construction
24 and as such cannot tell if the prior art meets it or
25 not."

1 Did I read that correctly?

2 A. Yes, you did.

3 Q. And then the judge goes on to say in that same
4 paragraph, quote, "In the end, Dr. Przybylski
5 discredited his own testimony to the point that it could
6 not be relied upon."

7 Did I read that correctly?

8 A. Yes, you did.

9 Q. And then the judge goes on to say, "He was
10 evasive, forgetful, contradictory and offered set
11 statements with no explanation."

12 Did I read that correctly?

13 A. Yes, you did.

14 Q. And by "he," the ALJ was referring to you, sir;
15 is that correct?

16 A. Yes, he was.

17 Q. And the judge goes on to say that he found you,
18 quote, "so unreliable overall that your testimony in
19 this matter could not assist him."

20 Did I read that correctly?

21 A. That is his last sentence of that paragraph.

22 Q. On the previous page, if you could turn back a
23 page, in the middle of the page, the judge states that
24 you had -- I'm sorry -- it's about two-thirds of the way
25 down. The statement where the judge says that "you had

1 shaped your testimony in ways that were not consistent
2 with his claim construction."

3 Did I read that correctly?

4 A. That's what he wrote.

5 Q. And a little bit above that, about in the
6 middle of the page, the judge stated, "He," referring to
7 you, "is able to see things in claims that are not in
8 the claims and to argue with the attorney without
9 grounding his testimony in science."

10 Did I read that correctly?

11 MS. ARMOND: I'm sorry. Counsel, where are you
12 reading from?

13 MR. KAPPOS: About in the middle of the page.

14 MS. ARMOND: And you're still on 145?

15 MR. KAPPOS: That's correct.

16 MS. ARMOND: Okay.

17 THE WITNESS: So is there a pending question?

18 MR. KAPPOS: There is not. I think you
19 answered "that's correct."

20 THE WITNESS: I thought that was for the
21 previous quotation.

22 Q. (By Mr. Kappos) Okay.

23 Well, let me -- let me do it again.

24 And the judge goes on to say, about in the
25 middle of Page 145, that "he," meaning you, "is able to

1 see things in claims that are not in the claims and to
2 argue with the attorney without grounding his," meaning
3 your, "testimony in science."

4 Did I read that correctly?

5 A. Yes, you read that correctly.

6 Q. Now I want to refer one page back to 144. In
7 the middle of the page where the -- the section entitled
8 "Dr. Steven Przybylski" starts.

9 Do you see that?

10 A. I see Section F, yes.

11 Q. And the second sentence in that section, the
12 judge said, quote, "While a written record can never
13 capture the full dynamic of a witness on the stand,
14 there are instances where the cold word on paper cannot
15 even convey the smallest sense of what goes on live. In
16 the testimony of Dr. Steven Przybylski we had such an
17 experience. The doctor's testimony was inconsistent
18 with that which he gave in the '661 investigation and
19 his demeanor on the stand as he was confronted with
20 prior art, previous statements he and others had made
21 and diagrams of the evidence was remarkable: He would
22 have long periods of silence, punctuated with heavy
23 sighs, conveyed the impression that he had run out of
24 answers and was making statements that he himself did
25 not believe. He often merely disputed the words on the

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1 paper, rather than offering an explanation or argument
2 for the Court to consider. Where an expert no longer
3 can explain apparent inconsistencies or contradictions,
4 but merely asserts that his answer is what a person of
5 ordinary skill in the art would give, the witness causes
6 to" -- "the witness ceases to act as an expert. He
7 provides no useful testimony to the ALJ or to the
8 Commission." End of quote.

9 Did I read that correctly?

10 A. Yes.

11 Q. And the ALJ, the judge was referring to your
12 testimony in that case; correct?

13 A. That's what he wrote, yes.

14 Q. How did you prepare for your deposition today?

15 A. I reviewed the -- my declaration a number of
16 times. I reviewed the -- several of the documents
17 involved and I had two meetings with counsel.

18 Q. At any of the breaks today, did you discuss the
19 substance of the deposition or any of the questions or
20 your testimony with anyone?

21 A. No.

22 MR. KAPPOS: Can we take a ten-minute break?

23 MS. ARMOND: Yes.

24 THE VIDEOGRAPHER: The time is 3:05 p.m. We
25 are now off the record.

1 (Recess taken from 3:05 p.m. to 3:14 p.m.)

2 THE VIDEOGRAPHER: The time is 3:14 p.m. We
3 are now back on the record.

4 MR. KAPPOS: Okay.

5 No further questions from me.

6 MS. ARMOND: No further questions.

7 THE VIDEOGRAPHER: This concludes today's
8 deposition of Dr. Steven A. Przybylski. The time is
9 3:15 p.m. We are now off the record.

10 (Whereupon, the videotaped deposition of DR.
11 STEVEN A. PRZYBYLSKI concluded at 3:15 p.m.)

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1 I, HEATHER J. BAUTISTA, CSR No. 11600, Certified
2 Shorthand Reporter, certify:

3 That the foregoing proceedings were taken before
4 me at the time and place therein set forth, at which
5 time the witness declared under penalty of perjury; that
6 the testimony of the witness and all objections made at
7 the time of the examination were recorded
8 stenographically by me and were thereafter transcribed
9 under my direction and supervision;

10 That the foregoing is a full, true, and correct
11 transcript of my shorthand notes so taken and of the
12 testimony so given;

13 () Reading and signing was requested/offered.

14 (XX) Reading and signing was not requested/offered.

15 () Reading and signing was waived.

16 I further certify that I am not financially
17 interested in the action, and I am not a relative or
18 employee of any attorney of the parties, nor of any of
19 the parties.

20 I declare under penalty of perjury under the laws
21 of California that the foregoing is true and correct.
22

23 Dated: April 19, 2024

24 

25 HEATHER J. BAUTISTA, CSR, CRR, RPR, CLR

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