

WILL THERMAL BUDGET REALLY MATTER IN THE FUTURE?

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As the industry races down Moore's Law, the ability to quickly and accurately develop new processes becomes increasingly important. Simultaneously, as devices have shrunk, process development has become more complex. This paper examines the inputs and decision criteria used to design new processes, and demonstrates the increasing complexity of process development. The first metric examined thoroughly is the thermal budget. Both the classic definition of thermal budget (time-temperature) and the more accurate method of activation energy analysis are considered. It is shown that activation energy, while a useful methodology for thermal budget considerations, is not the sole decision criteria for designing a process. Other metrics of importance are proposed and examples given. Special issues for high- κ gate dielectrics are considered to demonstrate how some of the criteria may change as future nodes are worked. The complexities of balancing technical and manufacturing goals are shown to be necessary in order to achieve the desired process.

INTRODUCTION

The need to quickly develop and introduce new processes into production in order to fulfill Moore's Law has achieved considerable attention in the International Technology Roadmap for Semiconductors. However, the specifics of how one actually accomplishes this goal are not always discussed in the open literature. One concept that has been discussed is thermal budget and the need to reduce thermal budget each technology node. In fact, it would appear that the only inputs to be considered in developing a process are thermal budget and equipment access. However, this approach is too simplistic. For one, the typical concept of thermal budget in itself is too simplistic. A discussion of how one defines thermal budget and its application to process development will be presented first in order to demonstrate the inadequacies of using a too simple definition of thermal budget. As part of the discussion, a more accurate method of accessing thermal considerations, activation energy analysis, is reviewed. It is shown that activation energy, while a useful methodology for thermal budget considerations, is still not the sole technical decision criteria for designing a process. Further metrics for accessing technical inputs will subsequently be introduced to demonstrate the complexities in process design today. Examples are provided to illustrate these complexities and the challenges faced in actual application. Finally, the reality inputs are introduced, i.e., the inputs related to actual production of a device and the considerations that must be made in manufacturing.

Before presenting and discussing the various input metrics, the driving force behind increasing process development complexity should be quickly analyzed. As devices have shrunk, the ability for any single mechanism to largely control a significant transistor metric is no longer possible. Mechanisms that were once considered only second order

factors now have the same influence as traditional first order factors. In other words, instead of only a few significant mechanisms, there are many mechanisms with smaller influences. For example, a mechanism that causes a mere 3 % improvement in I_{drive} is now considered to be significant. Consequently, in this paper, some of the metrics introduced might have been judged as unimportant second order factors five years ago, but today must be carefully utilized in order to achieve *every last percentage point* of improvement in device performance. This increasing complexity is occurring while the industry is decreasing the time between nodes from 3 years to 2, i.e., the slope of Moore's Curve is becoming steeper. Therefore, one must identify all important metrics and ascertain their impact almost simultaneously in order to develop new processes quickly enough. The goal of this paper is to quickly summarize all the various mechanisms that now must be considered when designing a process and to encourage the reader to analyze the situation carefully to identify the many mechanisms involved.

THERMAL BUDGET

When integrating thermal processes, there is a need to be able to assess their total impact upon the existing dopant distributions and final device performance. This need led to development of the concept of thermal budget. There are different metrics used for accessing thermal budget. One such metric is based upon the case of simple diffusion (Fick's Law). Fick's law provides a relationship for diffusion as a function of time:

$$\text{Depth of Diffusion} \sim \sqrt{Dt}, \quad (1)$$

where

t = time

D = diffusion coefficient.

If one knows the relationship of the diffusion coefficient with temperature, material, and diffusing species, than one can determine the depth of diffusion with time.

While Eq. (1) is a more accurate representation of the impact of temperature and time upon diffusion, the more traditional metric is:

$$\text{Thermal Budget} = T \cdot t. \quad (2)$$

This metric is equal to the area under the temperature versus time curve [1]. While the diffusion coefficient (D) is not proportional to temperature (rather, it is proportional to $\exp(-1/T)$), one can see how the simple metric of Eq. (2) might appear to capture the inherent behavior of diffusion with temperature and time. In other words, Eq. (2) reflects that diffusion increases when either time or temperature increase. However, in practice, the actual temperature profile may be very complicated, and comparing two very different profiles utilizing Eq. (2) can lead one to make incorrect conclusions. For example, Figure 1 demonstrates how a specific spike anneal process may have the same thermal budget as a two minute soak at room temperature. Obviously, the results achieved will be vastly different.

Thus, a more accurate method for considering the specific temperature vs. time profile is needed. What is also needed is a method that considers the temperature and time effects

on both desired mechanisms, such as activation, and undesired mechanisms, such as Transient Enhanced Diffusion (TED).

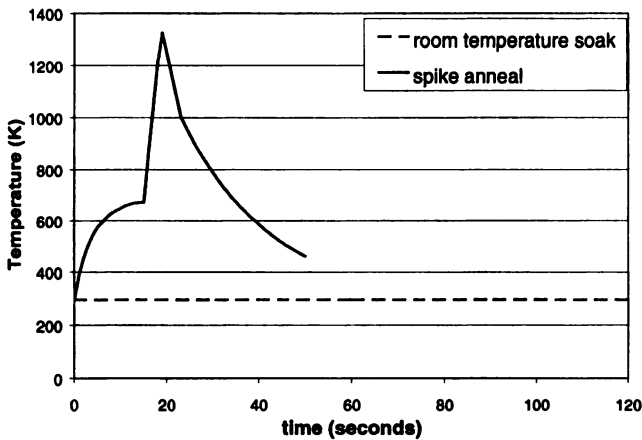


Fig. 1. The area under the T-t curves for a spike RTA process is approximately the same as a two-minute soak at room temperature.

ACTIVATION ENERGY

One method for assessing thermal budget is to consider the rate at which competing reactions occur. Ditchfield and Seebauer [2] discuss a method considering the activation energies of both desired and undesired processes based upon the basic reaction rate equation (Arrhenius' Law):

rate = $k \exp\left(\frac{-E_a}{k_b T}\right)$ (3)

where

- E_a = Activation Energy
- k_b = Boltzmann Constant
- k = rate at infinite temperature (the asymptotic rate).

In addition to chemical reactions, diffusion also follows Eq. (3) through the diffusion coefficient D, with k normally represented as D₀. By considering the activation energies (E_a) of the desired and undesired processes, one can find a temperature versus time profile that maximizes the selectivity of the desired to the undesired processes. Low activation energy processes are less temperature dependent than high activation energy processes. Thus, at low temperatures, the rate of a low activation energy processes will be much higher than that of a high activation energy process. Ditchfield and Seebauer

If Activation Energy:	Temperature Profile Should Be:
E _{a,desired} > E _{a,undesired}	high temperature, short time process.
E _{a,desired} < E _{a,undesired}	low temperature, long time process.

Table 1: Activation Energy Analysis Rule of Thumb

created a rule of thumb for accessing thermal budget to design a process, which is illustrated in Table 1.

CASE STUDY: SPIKE ANNEALING

We have developed a convenient formalism for estimating the amount of diffusion in the presence of TED when ramping up temperature at a known ramp rate [3]. The diffusion length during ramping up from, say, 600 °C to temperature T_f (if TED is over at an intermediate temperature y , before it reaches the temperature T_f) is given by

$$(D_{ob}/\text{ramprate}) \left[\int_{873}^{y(\text{ramprate})} \exp\{-(E_{mb} + E_{ls})/kT\} dT + \int_{y(\text{ramprate})}^{T_f} \exp\{-E_{mb}/kT\} dT \right], \quad (4)$$

where

D_{ob} = Pre-exponential constant for boron diffusion

E_{mb} = Migration energy for boron diffusion

E_{ls} = Change in the energy of a loop when an interstitial is emitted. This is negative because the energy of the loop decreases.

The temperature y is obtained by solving the following,

$$\alpha(y) \left[1 - (1/\text{ramprate}) \int_{873}^y (1/\alpha(T)) dT \right] = 0 \quad (5)$$

$\alpha(T)$ is the TED duration at temperature T , and a simple expression given by Stolk et al. may be used in deriving trends [4]. The method is easily extended to include the effects of varying cool-down rate and varying spike anneal sharpness and can be used to predict what might be expected from various advanced anneal processes.

Figure 2 compares diffusion during a perfect spike anneal to one that is blunted by inserting a one second step at constant temperature at the peak using our method. The reduction of junction depth with increasing ramp rate is stronger in the case of the perfect spike, demonstrating the importance of spike sharpness. By increasing the ramp rate sufficiently it is possible to use a higher peak temperature without significant increase in junction depth by going to a sharper spike. This provides the possibility of obtaining increased activation levels of implanted boron and improving the sheet resistance – junction depth trade-off.

Figure 3 shows expected trends as cool down rate is varied for various ramp up rates (TED is over before the peak temperature is reached in all cases shown). It is clear that

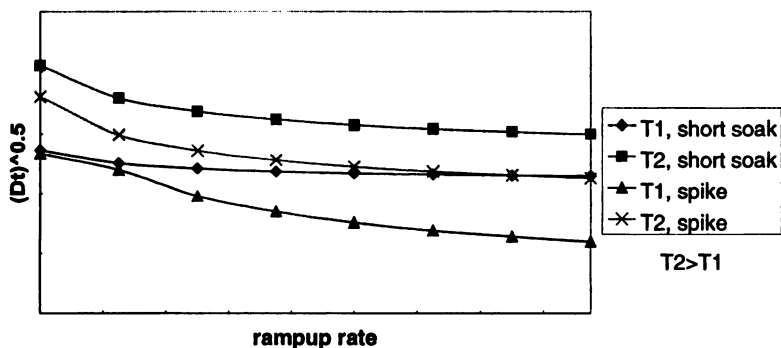


Fig. 2. Comparison of junction spreading between a spike anneal process and a 1 second soak process as a function of ramp up rate using the method of Eq. (4). Cool-down has not been included [3].

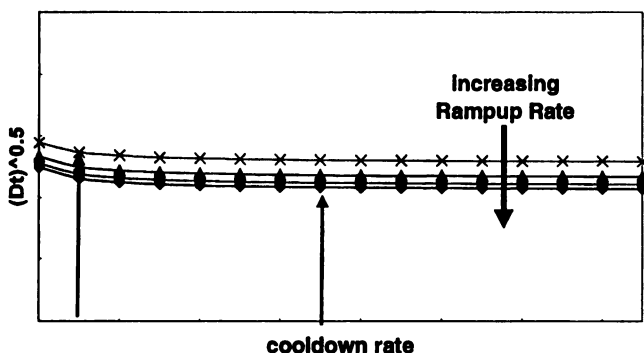


Fig. 3. Junction spreading as a function of cool down rate using the method of Eq. (4). The arrows that extend from the cooldown rate axis are positioned at cooldown rates equal to the rampup rates that are indicated.

there is substantial advantage in increasing both ramp up and ramp down rate up to a point beyond which there are rapidly diminishing returns.

In a similar vein, Fiory and Bourdelle have examined electrical activation in relation to diffusion for B (non amorphizing) implants [5], and Mayur et al. have examined this for BF_2 (amorphizing) implants [6]. In both cases, it is found that there is a higher barrier for electrical activation compared to diffusion and this favors the use of higher temperature spikes with increased sharpness.

WHAT HAPPENS IN PRACTICE?

Figure 4 shows the SIMS profiles for boron for spike recipes with two different levels of sharpness. The implant consisted of pre-damage by Sb to a dose of $3 \times 10^{13}/\text{cm}^2$ at 25 keV followed by BF_2 to a dose of $1.6 \times 10^{15}/\text{cm}^2$ at 5 keV, both at 0° tilt. The sharpness is

assessed by the shortness of time spent within 50 °C of the peak temperature (1050 °C in this example). The ramp rate is 180 °C/s. The resulting junction profiles show that the different spike widths, 1.7s vs. 2.7 s, cause a significant difference in diffusion depth. The

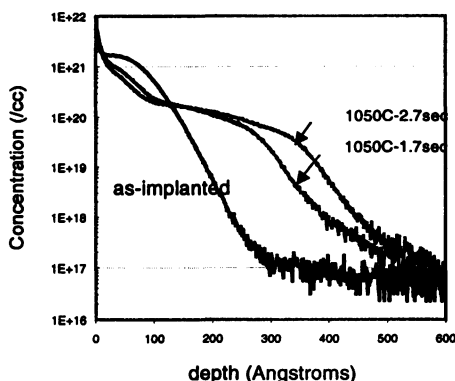


Fig. 4. SIMS boron depth profiles resulting from a 5 keV, $1.6 \times 10^{15} \text{ cm}^{-2}$ BF_2 implant into a substrate pre-amorphized with a 25 keV, $3 \times 10^{13} \text{ cm}^{-2}$ Sb implant, followed by 1050 °C anneals with 1.7 and 2.7 s spike widths [7].

results clearly show that as the time in the higher temperature regimes increases, so does junction depth. However, the abruptness is compromised as the junction becomes shallower. Exposure to high temperature results in concentration enhanced diffusion that flattens the top of the profile and increases abruptness by “overrunning” the low temperature TED tail, which is still evident even for an optimized spike process. The degraded slope is therefore a side consequence of reduced exposure to high temperature and is an additional factor to be reckoned with in junction engineering. While the activation analysis provides a means to optimize the junction depth vs. sheet resistance tradeoff, all of the relevant figures of merit, including abruptness, must be considered.

SECONDARY EFFECTS MUST BE CONSIDERED

The case of spike annealing illustrates that, while a comparison of activation energies of the relevant mechanisms provides a good rule of thumb for guiding thermal process development, even the best rule of thumb can prove misleading. The details matter, even for well-characterized processes; and the impact of an undesired effect may still be significant even when minimized. A number of other factors must be taken into account when employing an activation analysis in addition to those identified in the example. While the relevant mechanisms may be thermally activated, the associated parameters may be, as yet, undetermined. Parameter values may be extremely sensitive to processing conditions, particularly during deposition processes. Moreover, the relevant processes in competition may be too numerous to comprehend outside a detailed process simulation environment, even if all are adequately characterized. Much of the remainder of this paper will focus on the processes and reactions that typically take place in parallel with, subsequent to, and, at times, in competition with, those that we intend to effect.

These issues are becoming more and more critical as device dimensions shrink, doping levels rise, and thermal sensitivity of the materials employed increases.

AMBIENT REACTIONS

Figure 5 shows the impact of processing ambient on a shallow boron profile under processing conditions appropriate for RTCVD or furnace processing. Concentrating on the non-oxidizing conditions for the moment, Natusuaki et al. observe considerable loss of dose that varies with the particular annealing ambient [8]. While dopants may react chemically with the ambient gas to form volatile species at the free silicon surface, dopant loss can easily occur in inert annealing environments as well. Dopants may leave

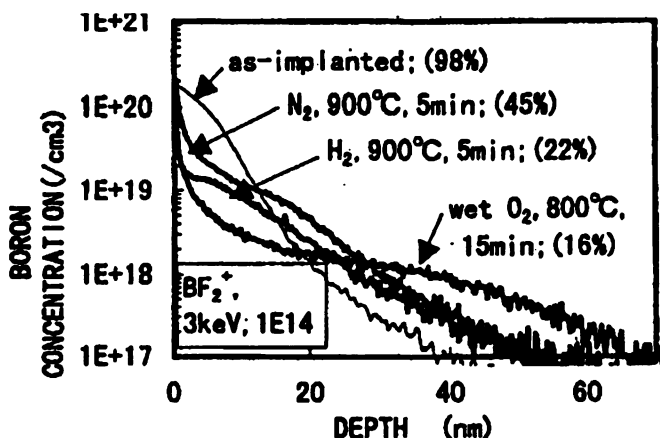


Fig. 5. SIMS depth profiles illustrating the impact of ambient on boron redistribution. Reproduced with permission from Natusuaki et al., © 1999 IEEE [8].

the substrate via reaction with impurities present, such as fluorine in the case of BF_2 implants [9]; or they may simply evolve on their own based on their equilibrium vapor pressures [10]. At higher temperatures, a formerly inert annealing ambient such as nitrogen may begin to react with the silicon surface itself, pitting it and undermining the matrix containing the dopant. All of these are activated reactions that will compete with any intended diffusion of implanted dopants.

Thermal processing in ambients containing oxygen introduces some additional and well-characterized effects that depend on the partial pressure of oxygen as well as the temperature and time. At low pressures, the preferential reaction to form volatile SiO at the silicon surface causes surface etching, even at moderate temperatures. At pressures sufficiently high to favor SiO_2 growth over etching, the injection of silicon interstitial reaction products into the substrate leads to oxidation enhanced dopant diffusion (OED) far in excess of equilibrium diffusion rates. While OED is generally undesirable in advanced CMOS fabrication, some authors have found value in selecting annealing ambients with oxygen partial pressures above, but in the vicinity of, the etching/growth transition [11,12]. In addition, dopant will segregate into the growing oxide at the growth

interface and diffuse into the oxide, possibly evolving from the oxide surface just as in the case of a free silicon surface. The details of the annealing ambient are critically important for determining how many activated processes must be considered when proposing to thermally process dopants below a clean silicon surface.

INTERACTIONS WITH CAPPING OXIDES

One obvious approach to interactions with the ambient during dopant annealing consists of capping the bare silicon surface. Grown or deposited oxide layers are most commonly employed for capping during high temperature annealing, as the stress mismatch of nitride films in direct contact with the silicon substrate renders them impractical at high temperatures despite their superior diffusion barrier capabilities. Screen oxides are commonly grown prior to dopant implantation to minimize ion channeling, and often remain during annealing. As indicated in the preceding section, however, the presence of an oxide film can have a substantial impact on the diffusion kinetics beneath it.

Dopant diffusion in the substrate and cap are coupled through the segregation coefficient. The segregation of dopants from silicon into oxide during thermal oxide growth has been very well characterized for temperatures above 900 °C [13]. The associated activation parameters have been determined; however, they were found to vary significantly between dry and wet oxidation processes, even when only slight amounts of moisture were present. Unfortunately, little published data exists for the case of deposited oxides. Given the variety of growth chemistries and the lower densities of the deposited films relative to grown ones, however, modification of the activation energies of segregation when deposited oxide capping layers are used would seem likely.

Dopant diffusion kinetics within a thin oxide layer can be impacted by a host of factors. The apparent activation energy for boron diffusion has been shown to vary, not only with the presence numerous impurities, but even the film thickness as it falls below 100 Å [14,15,16]. Hydrogen, in particular, reduces the activation energy for boron diffusion, while nitrogen, in turn, raises it. Fluorine doesn't have a different activation energy associated with it; however, its presence will enhance boron diffusion and modify the relative impact of the other impurities. Figure 6 shows the change in apparent activation energy for boron diffusion as the thickness of a grown oxide layer decreases. Fair proposes that this dependence stems from the formation of peroxy linkage defects as SiO formed during oxidation diffuses away from the growth interface into the oxide [14]. This mechanism would continue to apply if the oxide erodes during subsequent cleaning or etching, which would lead to decreasing activation energy for boron diffusion in the same oxide as it undergoes repeated processing. Control of the thickness of a screen oxide layer both during growth and in subsequent processing can be critical to obtaining consistent junction profiles.

Figure 7 shows the variation in the diffused boron profile for different grown screen oxide thicknesses present during anneal. The implant conditions are pre-damage by Sb to a dose of $3 \times 10^{13}/\text{cm}^2$ at 25 keV followed by BF_2 to a dose of $8 \times 10^{14}/\text{cm}^2$ at 5 keV, both at 0° tilt. The profiles shown correspond to a final anneal of 1050 °C, and all profiles are measured from the silicon surface. It is seen that junction depth increases with oxide thickness even though the as-implanted depth from the silicon surface is obviously shallowest for the thickest oxide. This suggests that the oxide influences TED behavior.

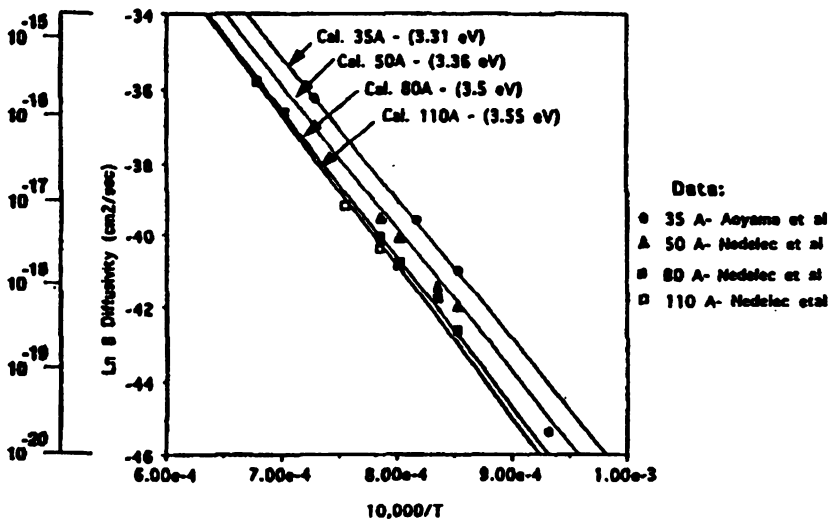


Fig. 6. Calculated B diffusivity in pure SiO₂ vs. oxide thickness, compared with measured data. Reproduced with permission from Fair, © 1995 IEEE [14].

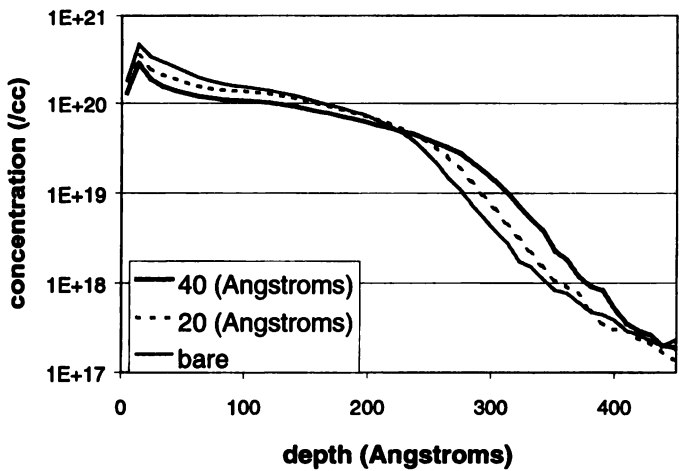


Fig. 7. SIMS boron depth profile resulting from a 5 keV, $8 \times 10^{14} \text{ cm}^{-2}$ BF₂ implant through three different screen oxide thicknesses into a substrate pre-amorphized with a 25 keV, $3 \times 10^{13} \text{ cm}^{-2}$ Sb implant, followed by a 1050 °C spike anneal [17].

In the case of no oxide the surface can be expected to be an effective sink for silicon interstitials. With oxide present excess silicon atoms must diffuse to the gas interface

where they can escape as (volatile) Si-O species [18]. Thus, greater oxide thickness would have the effect of extending the duration of TED.

The use of deposited, rather than grown, oxide films further complicates the analysis. As with segregation, little or no published data exists. Since film growth proceeds at the oxide/ambient interface rather than the oxide/silicon interface, the peroxy defect distribution tailing away from the oxide/silicon interface that has been proposed as the source of the activation energy variation with grown oxide thickness is not likely to exist. However, the impurity effects should be even larger, given the higher overall defectivity of deposited oxide films, and other defect mediated diffusion mechanisms insignificant for grown oxides may play a larger role.

IMPACT OF POST-PROCESSING

While most of the preceding discussion concerns itself with parasitic reactions occurring in parallel with intended dopant diffusion processing, thermal processes that follow the intended process are also critical, and have typically been the primary targets of thermal budget analyses. Specifically, thermal budget arguments were used when considering the impact of the process to be effected on the equilibrium diffusion of the existing dopant profiles. With the highly metastable active doping concentrations produced via rapid thermal processing, however, dopant deactivation following junction formation must also be comprehended. Deactivation readily lends itself to an activation energy analysis, although the detailed kinetics of the process continue to generate debate [19,20].

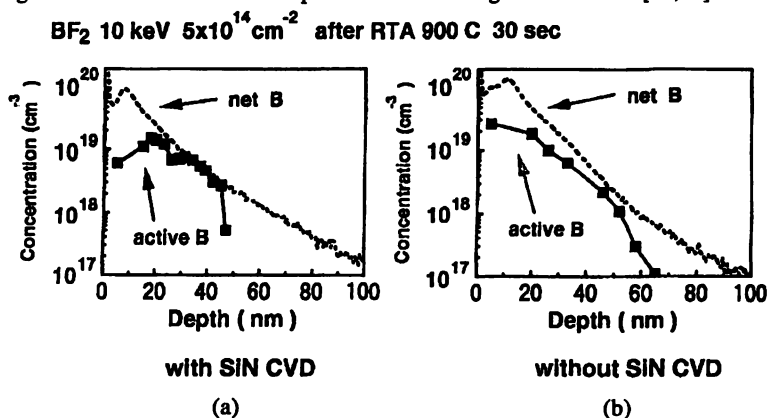


Fig. 8. Depth profiles of net and active boron concentration of p+ extension regions (a) or (b) without SiN CVD after RTA 900 °C, 30s, respectively. Reproduced with permission from Inaba et al., © 1999 IEEE [21].

Far less discussed, but increasingly important, are the effects of subsequent processing chemistries on dopant distributions. Earlier in this article, data from Natsuaki et al. illustrated the sizable impact of a hydrogen annealing ambient on boron diffusion [8]. Hydrogen moves freely through most of the materials currently used in front-end silicon

processing, so encapsulating the surface may matter little. Hydrogen is both used and produced as a byproduct in deposition processes, including sidewall nitride, providing ample opportunity for exposure following source/drain extension formation. Figure 8 shows the change in the electrically active boron profile during LPCVD deposition of silicon nitride. While dopant is, indeed, lost from the substrate during the deposition process, the chemical profile near the surface remains in excess of the equilibrium value. FTIR data supports the hypothesis of boron deactivation via silicon-boron-hydrogen complex formation [21]. Chemical interactions such as this constitute one more factor that must be considered in thermal process design. Reactions involving hydrogen and other active species introduced during deposition and etching are almost certainly activated processes, but are less likely than most others that have been discussed to be fully characterized. In addition, as they are frequently byproducts, their concentration and the uniformity of their exposure may be difficult to control.

MECHANICAL STRESS

Wafers in process, especially those undergoing rapid thermal processing, are subjected to a variety of sources of mechanical stress over a range of dimensional scale. Transistor level features, such as the sidewall spacer, contact silicide, and shallow trench isolation, can produce local dislocations and piezoresistive changes in drive currents [22,23,24]; while die and wafer scale stresses resulting from temperature nonuniformity, large area thin film stresses, and gravity can result in plastic deformation and slip over large areas of a wafer [25,26]. Although the yield stress of silicon is a thermally activated parameter and amenable to an activation analysis, the stresses actually present depend on the material layers added to the wafer, the specific growth or deposition conditions during thin film formation, the geometries present, the ability of the processing tools to control temperature uniformity, and the manner in which wafers are supported. In addition, the yield stress does not depend solely on the temperature at which the stress is applied. While the dependence on oxygen content and strain rate is not exponential, as it is with temperature, the strain rate can vary over several orders of magnitude when considering both furnace and rapid thermal processes and can significantly increase the yield stress for high strain rate processes.

HIGH- κ DIELECTRICS

The industry presently faces the unprecedented challenge of changing the gate dielectric, begging the question of what role thermal budget considerations will assume in the process development. Originally, there was a belief that a new high- κ material could be found that would be thermodynamically stable, especially with respect to silicon. However, even for the high- κ materials that are thermodynamically favorable, phase separation, crystallization, and interfacial reactions appear to be some of the largest obstacles. Since kinetics appear to be playing a large role, the same considerations previously discussed in the paper will be applicable in the high- κ case as well. The process used to deposit the material, as well as both the immediately prior and subsequent processing, may have a huge role in determining the material's sensitivity to further downstream processing. Thus, the greatest issue facing high- κ may be to determine how to reduce the material's sensitivity to subsequent thermal processing. Obviously, the material choice itself may be the greatest factor in determining that sensitivity. The

industry is only just discovering how materials which theoretically are expected to behave similarly may, in fact, act very differently in their sensitivities to ambients and thermal processing [27,28].

FACTORS RELATED TO PRODUCTION

The factors and decision criteria examined so far relate to the technical issues to be addressed in achieving a desired process result. However, at some point, the process must be assigned to a piece of equipment to be operated with a given manufacturing philosophy in a particular production fab producing a specific product mix. In an overly simplistic world, one would only need equipment to demonstrate a particular process once. However, production issues must be addressed, too. Table II lists the factors generally associated with production.

Table II: Production Factors.

Load Size
Cycle Time vs. Throughput
Cost (CoO)
Controllability
Clustering (technical need vs. operation need)

Most of the factors listed in Table II are self-explanatory, so they will only be discussed briefly. Load size and the cycle time versus throughput tradeoff are primarily determined by the product mix. ASIC-like factories may emphasize cycle time and small loads while microprocessor and memory fabs may focus on large load sizes and throughput. Cost, usually represented as CoO, may be heavily influenced by overhead, such as qual wafers and chamber cleans. Thus, a thorough assessment of cost is required. One issue related to cost, but to which it may be difficult to actually assign a dollar value, is controllability. Controllability is the ability of the equipment to achieve the desired process result wafer to wafer, across the wafer, and, hopefully, independent of wafer state. Finally, clustering of different process (and metrology) chambers together may be driven by either technical issues (such as undesired interfacial growth) or operational issues (such as constraints on time between processes). While mini-environments may provide another approach, the challenge may be in finding a single minienvironment that provides the correct ambient conditions needed for all processes, from oxidation to lithography.

CONCLUSIONS

While the complexity of process development has increased; at the same time, the required rate of development has also increased due to the acceleration of Moore's Law. This paper illustrated how no single metric or simple set of criteria can dictate the development process. The various metrics and decision criteria that must be considered were examined. In order to speed development, one must comprehend all of these possible mechanisms early in the development cycle, and decide how the various trade-offs will impact equipment design.

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