

AN ANALYTICAL APPROACH TO QUANTIFY THE THERMAL BUDGET IN CONSIDERATION OF CONSECUTIVE THERMAL PROCESS STEPS

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For characterizing the susceptibility of processes or process flows to diffusion effects, usually the term „Thermal Budget“ (*TB*) is used. However, even though there are several definitions of the *TB*, still no quantitative and manageable description of the *TB* of several consecutive process steps exists due to the Arrhenius-nature of diffusion processes. This paper presents an analytical approach to quantify the *TB* of a given CMOS process flow based on the shift of a pn-junction due to thermal process steps. Furthermore, classification numbers for each process step were introduced which allow to rate their significance with regard to the *TB*. In conjunction with a device specification dependent diffusion limit, it then is possible to determine the remaining temperature-time-window at each stage of the process flow.

INTRODUCTION AND OVERVIEW

For more than 25 years an impressive development can be observed in the semiconductor industry commonly known as „Moore's Law“: the number of transistors on a single chip doubles every 18 months. This is mainly reached by new technology generations, which cause a 30% decrease of the smallest feature sizes every three years [1].

As a consequence of this decrease, the amount of outdiffusion of dopant regions, e.g. source and drain for CMOS devices, caused by thermal process steps has a more and more increasing impact on the geometrical device structure, which clearly affects the electrical properties of the devices.

For characterizing the susceptibility of processes or process flows to diffusion effects, the term „Thermal Budget“ (*TB*) was created [2]. Commonly, this term is referred to the area under a temperature-time-curve (*T-t*-curve) given for a certain process or process sequence:

$$TB = \int T dt. \quad (1)$$

However, this definition does not lead to an accurate characterization of the diffusion effects, because the diffusion coefficient *D* of

dopants in semiconductors obeys the Arrhenius-relationship

$$D = D_0 \cdot e^{-\frac{E_a}{k_B \cdot T}}. \quad (2)$$

Hereby are the frequency factor *D*₀ and the activation energy *E*_a two material specific parameters; *k*_B is the Boltzmann constant and *T* the process temperature in K. As a consequence, following the definition given in (1), different temperature-time-combinations might result in the same value for *TB* but show totally different dopant diffusion [3].

Osburn and Reisman redefined the *TB* as the process time allowed for a given process temperature [4]. However, this concept is also insufficient because only one temperature step is considered whereas usually many different temperatures are combined in one process sequence. Taking into account ramp up and down phases, even single processes combine many temperatures. These and other problems resulted in the fact that despite its increasing importance still no quantitative description of the *TB* exists.

In this work a new approach is shown to reach quantitative results for the susceptibility

lity of processes to diffusion effects in a simple manner. First, an analytical description for the shift of a pn-junction depending on the process parameters temperature and time is deduced. Then, this formula is modified which makes it applicable to whole process sequences rather than only single steps. In order to set the obtained junction shift in relationship to the specifications of a CMOS transistor, the minimum effective channel length L_{Cmin} for a given technology is determined. Then it is possible to specify an allowed temperature-time-window which can be interpreted as the remaining thermal budget for the examined process flow.

DIFFUSION BUDGET

The one-dimensional dopant diffusion in a semiconductor can be described by Fick's equation [5],

$$\frac{\partial}{\partial t} N(x, t) = D \cdot \frac{\partial^2}{\partial x^2} N(x, t), \quad (3)$$

which relates the dopant concentration per unit volume N to the parameters diffusion time t and distance x from the location of the maximum dopant concentration. In the case of doping by ion implantation, the solution to this diffusion equation is given by

$$N(x, t) = \frac{N_D}{\sqrt{2 \cdot \pi \cdot (\Delta R_p^2 + 2 \cdot D \cdot t)}} \cdot \exp\left(-\frac{(x - R_p)^2}{2 \cdot (\Delta R_p^2 + 2 \cdot D \cdot t)}\right). \quad (4)$$

In this formula, the implantation dose N_D , projected range R_p and projected straggle ΔR_p are characteristic parameters for the ion implantation, where R_p and ΔR_p are related to the implantation energy and known from experimental implant tables.

Similar to the diffusion length definition for minority carriers in semiconductors [5], the dif-

fusion length definition for dopants is usually given by $\sqrt{Dt}$. Whereas this diffusion length is a characteristic term for the average distance a dopant can move in a semiconductor during a given time t , the more interesting question is how much a pn-junction moves during a process step, because this directly affects the structure and therefore the electrical performance of a semiconductor device.

In order to calculate the shift of the pn-junction, it is first necessary to determine the original location of the junction directly after it's creation which normally is done by implanting carriers with a charge opposite to the substrate doping. Therefore, we obtain the location of the resulting pn-junction x_{j0} by solving equation (4) for x and setting N to the value of the substrate doping concentration, N_S , as well as $t = 0$; the location of the pn-junction x_j after a process step is obtained in the same way when t is set to the process time. The resulting shift of the pn-junction, which we define as diffusion budget D_B of this process step, is then given by

$$D_B = \sqrt{-2A \cdot \ln\left(\frac{N_S}{N_D} \cdot \sqrt{2\pi \cdot A}\right)} - B \quad (5)$$

$$A = \Delta R_p^2 + 2 \cdot D \cdot t$$

$$B = \sqrt{-2\Delta R_p^2 \cdot \ln\left(\sqrt{2\pi} \cdot \Delta R_p \cdot \frac{N_S}{N_D}\right)}.$$

This definition for the diffusion budget allows, in contrast to the usual definition for the diffusion length, a more direct assessment of the consequences of a process step for the doping profile and takes into account implantation parameters, diffusion parameters and the substrate doping concentration. To evaluate equation (5), results are compared to simulated data obtained by the industry standard process simulation tool ATHENA [6] in fig.1. As can be seen, there is good accordance for longer process times, whereas for shorter process times the calculated values for the diffusion budget are noticeable smaller than the simulated values. This is due to the fact that the implantation-

induced damage, i.e. point defects, causes transient enhanced diffusion (TED) of the dopants, because in the presence of point defects the activation energy E_a in equation (2) is smaller than usual for a certain time (table 1, table 2). Therefore, to correctly model D_B , it is necessary to divide the diffusion step in a fraction with an enhanced activation energy and a fraction with the usual activation energy. However, this leads to the problem of combining several process steps, which is described in the next section.

PROCESS SEQUENCES

Equation (5) only allows statements about a single diffusion process step after the implantation, with certain diffusion time and temperature; in practice, however, there are always several steps. Moreover, even a single process step combines many different temperatures because there are ramp up and down phases, which are especially important at annealing steps. And after all, as described in the section before, point defects can lead to different activation energies within the same diffusion step. In order to take this into account, we take a deeper look at equation (5). The diffusion-related parameters time t and temperature T appear only in the term $D \cdot t$, which is the square of the diffusion length L_D . Therefore, it is possible to express the diffusion budget of several consecutive process steps by substituting the term $D \cdot t = L_D^2$ in equation (5) with an equivalent diffusion length L_{Deq} , which takes into account the aforesaid effects and which we propose to

$$L_{Deq} = \sqrt{\sum_{i=1}^n \left(D_{0i} \cdot e^{\frac{-E_{ai}}{k_B \cdot T_i}} \cdot t_i \right)} \quad (6)$$

Hereby describes the index i one certain of n consecutive process steps with time t_i and temperature T_i . With this approach, the diffusion budget from fig. 1 was calculated again with the modified equation (5) by using two different activation energies according to tables 1 and 2.

As can be seen in fig. 2, now there is a good accordance between simulated and calculated data throughout the whole time range. In the same way, process steps with variable temperatures, i.e. ramp up and down phases, can be considered by dividing the ramp phases in several subsections with constant time and average temperature; and, last but not least, the diffusion budget of whole process sequences can be calculated using this method. In practice, because of the Arrhenius-relationship given in equation (2), certainly not all process steps but only processes with temperatures greater than 700°C have to be considered in terms of diffusion (fig. 3), which simplifies the application of equations (5) and (6).

DIFFUSION LIMIT

An important question is, how long a certain temperature can be applied to a dopant region without violating the electrical specifications. For example, we again look at the source-drain region. Diffusion, i.e. shift of the pn-junctions is only as long allowed, as long as the remaining channel length falls not under a certain minimum channel length L_{Cmin} . Therefore, in a first-order approach we can determine a maximum allowed diffusion budget D_{Bmax} , to

$$D_{Bmax} = \frac{1}{2} \cdot (L_G - L_{Cmin}), \quad (7)$$

where L_G is the printed gate length.

Hereby, the minimum channel length is determined by the specified electrical properties of the transistor and is a limit for the source-drain dopant diffusion. For example, according to [7] the threshold voltage shift ΔV_T , whose maximum allowed value is usually included in the specifications, can be set in relation to the minimum channel length according to

$$\frac{L_{Cmin}}{2l} = \ln \left(\frac{2 \cdot C_1}{-C_2 + \sqrt{C_2^2 + 4C_1 \Delta V_T}} \right) \quad (8)$$

Hereby the characteristic length l and the constants C_1 and C_2 can be expressed as

$$l = (t_{ox} \cdot x_{dep} \cdot x_j)^{1/3} \quad (9)$$

$$C_1 = 3 \cdot (V_{bi} - \Phi_S) + V_{DS} \quad (10)$$

$$\frac{C_2}{2} = \sqrt{(V_{bi} - \Phi_S) \cdot (V_{bi} - \Phi_S + V_{DS})} \quad (11)$$

where t_{ox} is the gate-oxide thickness, x_{dep} is the depletion layer thickness, x_j is the pn-junction depth, V_{bi} is the built-in potential between the source-substrate and the drain-substrate junctions, Φ_S is the surface potential at the onset of surface inversion and V_{DS} is the source-drain voltage. Another, more simple way is to directly specify the minimum channel length as a fraction of the initial gate length.

By setting $D_B = D_{Bmax}$ in equation (5) with the modification given in equation (6) and numerically solving for L_{Deg} , we obtain the maximum allowed value for the equivalent diffusion length, L_{Dmax} . According to equation (2), we then can scribe

$$L_{Dmax}^2 = D_0 \cdot e^{-\frac{E_a}{k_B \cdot T_{max}}} \cdot t_{max} \quad (12)$$

and define L_{Dmax}^2 as the maximum thermal budget TB_{max} , because it allows to determine maximum time-temperature combinations with respect to device specifications according to

$$t_{max} = \frac{TB_{max} \cdot \exp\left[\frac{E_a}{k \cdot T_{max}}\right]}{D_0} \quad (13)$$

Similar to the definition of TB_{max} , the thermal budget TB_i of a certain process step i is defined as

$$TB_i = D_0 \cdot e^{-\frac{E_a}{k_B \cdot T_i}} \cdot t_i, \quad (14)$$

which is a characteristic measure for the contribution of a certain process step to the diffusion budget of a process sequence.

RESULTS AND DISCUSSION

As an application of this method we were interested in finding the limits for the anneal step after source-drain implantation when taking into account two more process steps with temperatures greater than 700°C, namely contact silicidation and reflow. Therefore, we calculated the remaining ΔTB for the anneal by subtracting the TB_i 's of the silicidation and the reflow from TB_{max} and obtained the temperature-time curve given in fig. 4, which shows an allowed and a forbidden region for temperature-time combinations of the anneal step.

To estimate the contributions of different process steps to the thermal budget, we propose to assign classification numbers to each step, as shown in table 1. The maximum allowed TB_{max} is normalized to 1.00. The normalized TB_i 's (= classification numbers) of the several process steps can be summed up to obtain the total thermal budget of the chosen process sequence. This approach is particularly suitable to evaluate different settings for a process flow with respect to dopant diffusion. E.g., in table 1 there is a comparison of two different anneal steps, an RTA step and a more conventional furnace anneal, followed by two high temperature steps. The advantage of the RTA step is clearly seen and rated in a simple manner.

CONCLUSION

We introduced the diffusion budget of a given process flow and proposed a new method to quantify its thermal budget. The derived formula can be useful to make fast and simple predictions about the potential of processes and to determine the allowed temperature-time-window of process steps. By assigning classification numbers, the signifi-

cance of single processes or process sequences with regard to the thermal budget can be clearly seen taking into account the electrical specification of the device. Therefore, it will be a very useful tool for developing and analyzing process flows as well as for educational purposes.

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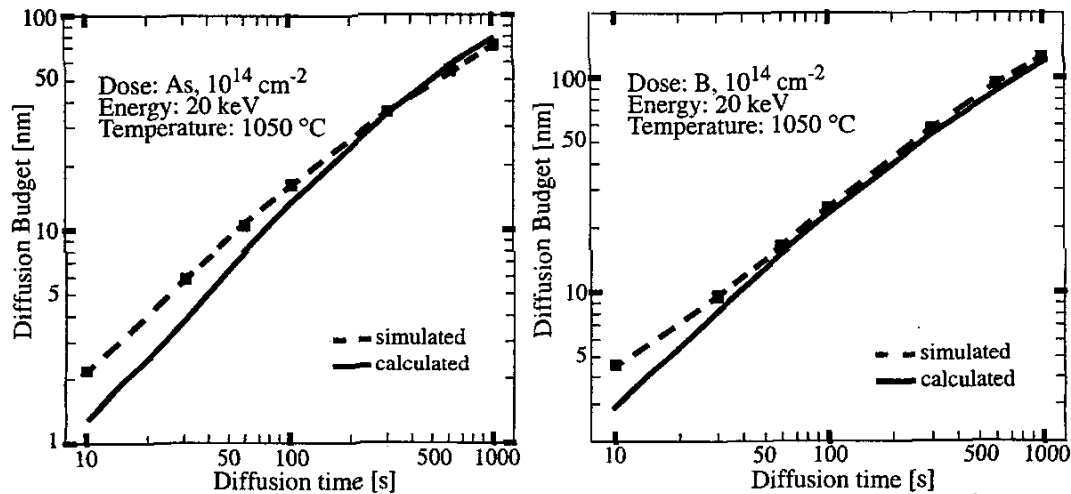


fig. 1: Comparison of calculated and simulated values for D_B for a diffusion step after ion implantation (equation (5)).

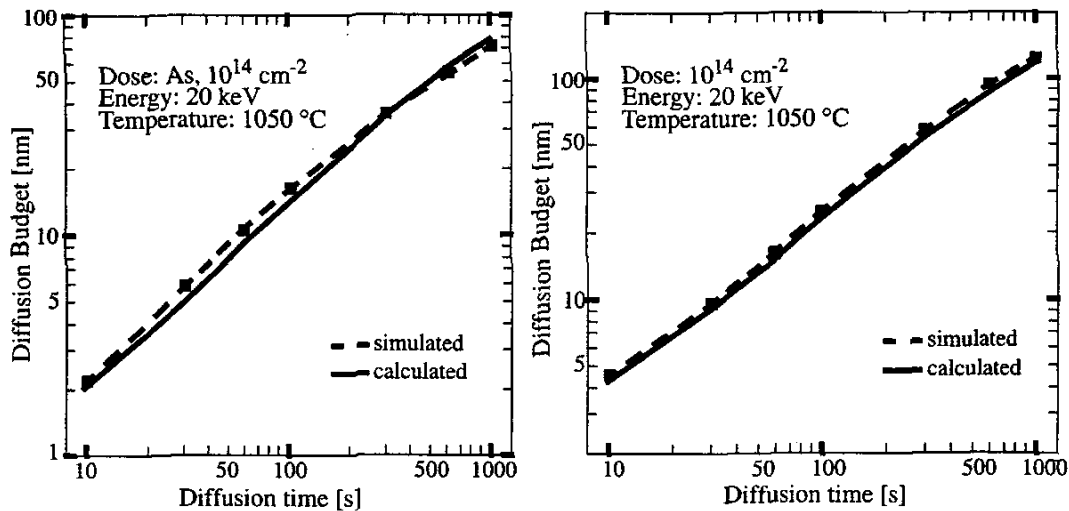


fig. 2: Comparison of calculated and simulated values for D_B for a diffusion step after ion implantation with regard to different activation energies due to TED (equations (5) and (6)).

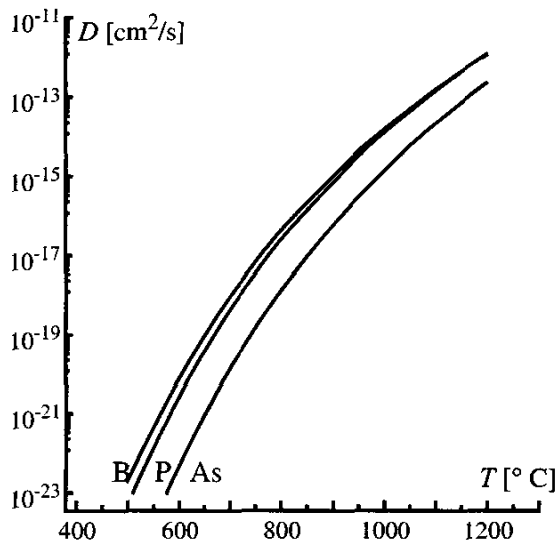


fig. 3: Temperature dependence of the diffusion coefficient D [5].

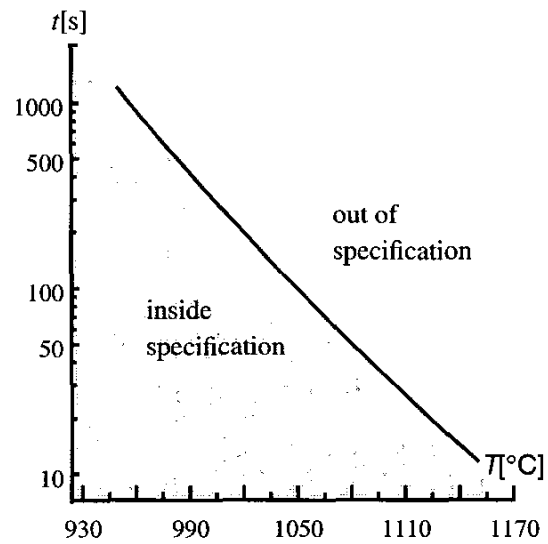


fig. 4: Allowed and forbidden temperature-time-combinations.

Annealing temperature [° C]	Time for completion of 95% of TED
700	3.3 hours
750	30 minutes
800	3.7 minutes
850	43 seconds
900	8.3 seconds
950	1.9 seconds
1000	0.48 seconds
1050	0.13 seconds

table 1: Approximate duration of TED at various annealing temperatures [8].

Dopant	usual	TED
Boron	3.46	1.8
Arsenic	4.1	1.8
Phosphorous	3.66	2.2

table 2: Activation energies E_{ai} [eV] for dopant diffusion in silicon [9].

	Anneal	TiSi ₂	BPSG	ΣTB	TB_{max}	ΔTB
case I		0.156	0.009	0.165	1.00	0.835
case II	0.766	0.156	0.009	0.931	1.00	0.069
casse III	0.356	0.156	0.009	0.521	1.00	0.479

table 3: Remaining ΔTB and assignment of classification numbers (TB_i 's) in order to rate the contribution of each process step. (E.g.: Annealstep followed by two more high-temperature steps)
case I: no anneal; silicidation: TiSi₂, 900 ° C, 15 min.; reflow: BPSG, 800 ° C, 20 min.
case II: 5 min. anneal at 1000 ° C
case III: 5 sec. anneal at 1150 ° C