

Filed on behalf of BeSang Inc.

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UNITED STATES PATENT AND TRADEMARK OFFICE

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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MICRON TECHNOLOGY, INC.,  
MICRON SEMICONDUCTOR PRODUCTS, INC., and  
MICRON TECHNOLOGY TEXAS, LLC,  
Petitioners,

v.

BESANG INC.,  
Patent Owner.

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Case No. IPR2023-00900  
U.S. Patent No. 7,378,702

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**PATENT OWNER'S SUR-REPLY**

## TABLE OF CONTENTS

|                                                                                                                                          | Page No. |
|------------------------------------------------------------------------------------------------------------------------------------------|----------|
| I. INTRODUCTION.....                                                                                                                     | 1        |
| II. CLAIM CONSTRUCTION .....                                                                                                             | 4        |
| A. “stackable add-on layer” .....                                                                                                        | 4        |
| B. “SOI pillar” .....                                                                                                                    | 4        |
| III. THE PETITION FAILED TO ESTABLISH UNPATENTABILITY<br>BASED ON LEE AND WATANABE (GROUNDS 5-6).....                                    | 8        |
| A. Watanabe’s High-Temperature Processing Entirely<br>Unravels Grounds 5-6 .....                                                         | 10       |
| B. Watanabe Offers Nothing To Pull Off Its High-Precision<br>Alignment For Grounds 5-6 .....                                             | 15       |
| C. The Petition Did Not Establish A Motivation To Combine<br>And Reasonable Expectation Of Success For Lee,<br>Watanabe, And Endoh ..... | 17       |
| D. The Petition Failed To Show A Motivation To Combine<br>Under Controlling Precedent .....                                              | 22       |
| IV. THE PETITION FAILED TO ESTABLISH UNPATENTABILITY<br>BASED ON LEE (GROUNDS 3-4) .....                                                 | 23       |
| V. THE PETITION FAILED TO ESTABLISH UNPATENTABILITY<br>BASED ON WATANABE (GROUNDS 1-2).....                                              | 24       |
| A. The Petition Did Not Establish That Watanabe Disclosed<br>The “Nonvolatile” Limitation 13[b] .....                                    | 24       |
| B. Watanabe Did Not Disclose A “SOI Pillar” .....                                                                                        | 25       |
| C. Watanabe’s Stacking Method Is Not Enabled .....                                                                                       | 27       |
| VI. CONCLUSION .....                                                                                                                     | 27       |

## TABLE OF AUTHORITIES

|                                                                                                                               | Page No(s).    |
|-------------------------------------------------------------------------------------------------------------------------------|----------------|
| <i>Ashland Oil v. Delta</i> ,<br>776 F.2d 281, 297 (Fed. Cir. 1985) .....                                                     | 27             |
| <i>Belden v. Berk-Tek</i> ,<br>805 F.3d 1064 (Fed. Cir. 2015) .....                                                           | 25             |
| <i>Berkeley Lights v. Univ. of British Columbia</i> ,<br>IPR2021-01249, 2023 WL 5155816 (P.T.A.B. July 20, 2023) .....        | 17             |
| <i>Certain Semiconductor Chips with DRAM Circuitry</i> ,<br>Inv. No. 337-TA-819, 2013 WL 1494382 (I.T.C. Mar. 26, 2013) ..... | 3              |
| <i>CoolIT Sys. v. Vidal</i> ,<br>No. 2022-1221, 2024 WL 981364 (Fed. Cir. Mar. 7, 2024) .....                                 | 5              |
| <i>Corephotonics v. Apple Inc.</i> ,<br>84 F.4th 990 (Fed. Cir. 2023) .....                                                   | 1, 26          |
| <i>Dexcom v. Waveform Techs.</i> ,<br>IPR2016-01680, 2018 WL 1137089 (P.T.A.B. Feb. 28, 2018) .....                           | 11, 12, 14, 15 |
| <i>Henny Penny v. Frymaster</i> ,<br>938 F.3d 1324 (Fed. Cir. 2019) .....                                                     | 18, 19         |
| <i>Hockerson-Halberstadt v. Avia</i> ,<br>222 F.3d 951 (Fed. Cir. 2000) .....                                                 | 7              |
| <i>Icon Health &amp; Fitness v. Strava</i> ,<br>849 F.3d 1034 (Fed. Cir. 2017) .....                                          | 22             |
| <i>Intel v. PACT</i> ,<br>61 F.4th 1373 (Fed. Cir. 2023) .....                                                                | 22             |
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Micron Technology v. BeSang Inc.  
Patent No. 7,378,702 – IPR2023-00900

*Juniper Networks v. Swarm Tech.*,  
IPR2021-01445, Paper 64 (P.T.A.B. Apr. 20, 2023) ..... 11, 14, 15

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667 F.3d 1261 (Fed. Cir. 2012) ..... 6

*In re Magnum Oil Tools Int’l*,  
829 F.3d 1364 (Fed. Cir. 2016) ..... 18

*Netflix v. DivX*,  
84 F.4th 1371 (Fed. Cir. 2023) ..... 8

*New U Life v. Axxess Global*,  
IPR2019-01141, 2020 WL 6260644 (P.T.A.B. Oct. 23, 2020)..... 16, 19, 25

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IPR2014-01079, Paper 30 (P.T.A.B. Jan. 12, 2016) ..... 13

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IPR2018-00182, 2019 WL 2866032 (P.T.A.B. July 2, 2019)..... 26

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*Samsung Elecs. v. Elm 3DS Innovations*,  
925 F.3d 1373 (Fed. Cir. 2019) ..... 21, 23

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IPR2015-00459, 2016 WL 1534753 (P.T.A.B. Apr. 14, 2016) ..... 6

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IPR2017-01674, 2019 WL 1154156 (P.T.A.B. Mar. 7, 2019)..... 16, 19, 25

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407 F.3d 1326 (Fed. Cir. 2005) ..... 4

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IPR2022-01544, 2024 WL 1513349 (P.T.A.B. Apr. 8, 2024) ..... 13, 19

*Virtek Vision v. Assembly Guidance Sys.*,  
97 F.4th 882 (Fed. Cir. 2024) ..... 9, 22

Micron Technology v. BeSang Inc.  
Patent No. 7,378,702 – IPR2023-00900

*Western Digital v. Longitude Licensing*,  
IPR2023-01123, 2024 WL 85417 (P.T.A.B. Jan. 8, 2024) ..... 3

#### **OTHER AUTHORITIES**

37 C.F.R. § 42.23..... 4, 11, 18

37 C.F.R. § 42.100..... 5

**TABLE OF EXHIBITS**

| <b>Exhibit No.</b> | <b>Description</b>                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2001               | First Amended Docket Control Order, <i>BeSang Inc. v. Micron Tech., Inc.</i> , Case No. 2:23-cv-00028, Dkt. 54 (E.D. Tex. June 21, 2023)                                                                                                                                                                                                                                                                                                                        |
| 2002               | Docket for <i>BeSang Inc. v. Micron Tech., Inc.</i> , Case No. 2:23-cv-00028 (E.D. Tex.) (as of Aug. 28, 2023)                                                                                                                                                                                                                                                                                                                                                  |
| 2003               | RESERVED                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 2004               | Defendants' Patent Local Rule 3-3 Disclosure of Invalidity Contentions, <i>BeSang Inc. v. Micron Tech., Inc.</i> , Case No. 2:23-cv-00028 (E.D. Tex. July 11, 2023) (cover pleading)                                                                                                                                                                                                                                                                            |
| 2005               | Ann S. Mutschler, <i>Stanford, Korean nanofab center, Oregon-based semi startup claim 3D IC breakthrough</i> , EDN (Aug. 13, 2008), <a href="https://www.edn.com/stanford-korean-nanofab-center-oregon-based-semi-startup-claim-3d-ic-breakthrough/">https://www.edn.com/stanford-korean-nanofab-center-oregon-based-semi-startup-claim-3d-ic-breakthrough/</a>                                                                                                 |
| 2006               | Press Release, <i>Micron and Intel Unveil New 3D NAND Flash Memory Technology Advancements Enable Three Times More Capacity than Other NAND Technologies</i> , Intel (Mar. 26, 2015), <a href="https://download.intel.com/newsroom/2021/archive/2015-03-26-news-releases-micron-and-intelunveil-new-3d-nand-flash-memory.pdf">https://download.intel.com/newsroom/2021/archive/2015-03-26-news-releases-micron-and-intelunveil-new-3d-nand-flash-memory.pdf</a> |
| 2007               | Peter Clarke, <i>EE Times updates list of emerging startups to version 8.0</i> , EE Times (Feb. 2, 2009), <a href="https://www.eetimes.com/ee-times-updates-list-of-emerging-startups-to-version-8-0/">https://www.eetimes.com/ee-times-updates-list-of-emerging-startups-to-version-8-0/</a>                                                                                                                                                                   |
| 2008               | <i>Exploring the Potential of Emerging Semiconductor Technology</i> , Global Semiconductor Alliance Forum, Vol. 18, No. 2 (June 2011), <a href="https://www.gsaglobal.org/wp-content/uploads/2019/04/201102_GSA_Forum.pdf">https://www.gsaglobal.org/wp-content/uploads/2019/04/201102_GSA_Forum.pdf</a>                                                                                                                                                        |
| 2009               | <i>Looking Beyond TSV For 3D IC Technology</i> , Frost & Sullivan (Mar. 2009), <a href="http://www.growthconsulting.frost.com/web/images.nsf/0/EF8B206A32BBD551652575B4002F3CD5/\$File/TIAAlert.htm">http://www.growthconsulting.frost.com/web/images.nsf/0/EF8B206A32BBD551652575B4002F3CD5/\$File/TIAAlert.htm</a>                                                                                                                                            |

| Exhibit No. | Description                                                                                                                                                                                                                                                                                                                                                                                                                      |
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| 2010        | Press Release, <i>Micron and Intel Extend their Leadership in 3D NAND Flash memory</i> , Globe News Wire (May 21, 2018), <a href="https://www.globenewswire.com/news-release/2018/05/21/1509614/14450/en/Micron-and-Intel-Extend-their-Leadership-in-3D-NAND-Flash-memory.html">https://www.globenewswire.com/news-release/2018/05/21/1509614/14450/en/Micron-and-Intel-Extend-their-Leadership-in-3D-NAND-Flash-memory.html</a> |
| 2011        | Micron Unveils 3D NAND (Mar. 26, 2015), <a href="https://www.youtube.com/watch?v=Lo-rsZ0vznw">https://www.youtube.com/watch?v=Lo-rsZ0vznw</a>                                                                                                                                                                                                                                                                                    |
| 2012        | <i>Radar Scope</i> , Semiconductor Times, Vol. 12, No. 4 (Apr. 2007)                                                                                                                                                                                                                                                                                                                                                             |
| 2013        | RESERVED                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 2014        | 1/29/2007 Email from Peter Feeley to BeSang                                                                                                                                                                                                                                                                                                                                                                                      |
| 2015        | 7/30/2007 Email exchange between Tom Arnold, Sang-Yun Lee, and others                                                                                                                                                                                                                                                                                                                                                            |
| 2016        | RESERVED                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 2017        | RESERVED                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 2018        | RESERVED                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 2019        | U.S. District Courts – Combined Civil and Criminal Federal Court Management Statistics (June 30, 2023), <a href="https://www.uscourts.gov/statistics-reports/federal-court-management-statistics-june-2023">https://www.uscourts.gov/statistics-reports/federal-court-management-statistics-june-2023</a>                                                                                                                        |
| 2020        | 9/14/2023 Email from Board to Counsel of Record Authorizing Preliminary Reply and Sur-Reply Briefing                                                                                                                                                                                                                                                                                                                             |
| 2021        | Roberto Bez et al., <i>Introduction to Flash Memory</i> , Proceedings of the IEEE, Vol. 91, No. 4 (April 2003)                                                                                                                                                                                                                                                                                                                   |
| 2022        | Executive Summary, <i>International Technology Roadmap for Semiconductors</i> , Semiconductor Industry Ass’n (2003), <a href="https://www.semiconductors.org/wp-content/uploads/2018/08/20031_ExecSum.pdf">https://www.semiconductors.org/wp-content/uploads/2018/08/20031_ExecSum.pdf</a>                                                                                                                                       |
| 2023        | U.S. Patent No. 6,881,994, Fig. 12B (annotated by Dr. Jack C. Lee)                                                                                                                                                                                                                                                                                                                                                               |
| 2024        | U.S. Patent No. 6,881,994, Fig. 12B (annotated by Dr. Jack C. Lee)                                                                                                                                                                                                                                                                                                                                                               |

| Exhibit No. | Description                                                                                                                                                                                                                                                                                 |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2025        | U.S. Patent No. 6,881,994, Fig. 12B (annotated by Dr. Jack C. Lee)                                                                                                                                                                                                                          |
| 2026        | U.S. Patent No. 6,881,994, Fig. 12B (annotated by Dr. Jack C. Lee)                                                                                                                                                                                                                          |
| 2027        | <u>Petitioners' Deposition Exhibit 1034</u> : Perrine Batude, et al., <i>3-D Sequential Integration: A Key Enabling Technology for Heterogeneous Co-Integration of New Function with CMOS</i> , IEEE J. on Emerging & Selected Topics in Circuits and Systems, Vol. 2, No. 4 (Dec. 2012)    |
| 2028        | Transcript of Deposition of Dr. Jack C. Lee (Feb. 6, 2024)                                                                                                                                                                                                                                  |
| 2029        | Declaration of Steven A. Przybylski                                                                                                                                                                                                                                                         |
| 2030        | CV of Steven A. Przybylski                                                                                                                                                                                                                                                                  |
| 2031        | <i>Webster's New Universal Unabridged Dictionary</i> (Barnes & Noble Publ'g 2003) (excerpt)                                                                                                                                                                                                 |
| 2032        | <i>Random House Webster's College Dictionary</i> (2d ed. 1997) (excerpt)                                                                                                                                                                                                                    |
| 2033        | Gary S. May, Ph.D. & Costas J. Spanos, Ph.D., <i>Fundamentals of Semiconductor Manufacturing and Process Control</i> (2006) (excerpts)                                                                                                                                                      |
| 2034        | Brent Keeth et al., <i>DRAM Circuit Design Fundamental and High-Speed Topics</i> (IEEE Press Editorial Board eds., 2008) (excerpts)                                                                                                                                                         |
| 2035        | Brent Keeth & R. Jacob Baker, <i>DRAM Circuit Design: A Tutorial</i> (Stuart K. Tewksbury & Joe E. Brewer eds., 2001) (excerpts)                                                                                                                                                            |
| 2036        | Kiyoo Itoh, <i>VLSI Memory Chip Design</i> (Kiyoo Itoh & Takayasu Sakurai eds., 1st ed. 2001) (excerpts)                                                                                                                                                                                    |
| 2037        | Interconnect, <i>International Technology Roadmap for Semiconductors</i> , Semiconductor Industry Ass'n (2007), <a href="https://www.semiconductors.org/wp-content/uploads/2018/08/2007Interconnect.pdf">https://www.semiconductors.org/wp-content/uploads/2018/08/2007Interconnect.pdf</a> |
| 2038        | 2/16/2024 Email from Board to Counsel of Record Denying Patent Owner's Request for Authorization to File a Motion to Strike                                                                                                                                                                 |

Micron Technology v. BeSang Inc.  
Patent No. 7,378,702 – IPR2023-00900

| Exhibit No. | Description                                                                                                                                                                 |
|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2039–2050   | RESERVED                                                                                                                                                                    |
| 2051        | [Not Filed] Declaration of Dr. Jack. C. Lee in <i>Western Digital Technologies, Inc. v. Longitude Licensing Ltd.</i> , IPR2023-01123, Exhibit 1003 (P.T.A.B. June 21, 2023) |
| 2052        | Transcript of Deposition of Dr. Jack C. Lee (June 12, 2024)                                                                                                                 |

## I. INTRODUCTION

The Petition promised combining Lee and Watanabe would be straightforward. Paper 1 (“Pet.”) at 69-71. After BeSang showed that Micron never grappled with the reality of its proposed combinations, Micron’s Reply with its litany of new theories, new expert testimony, and 30 new exhibits only confirms that the Petition failed to meet its burden on any ground in the first place. The Board may assuredly decline to consider these new theories. *Corephotonics v. Apple*, 84 F.4th 990, 1002 (Fed. Cir. 2023) (“the Board is not permitted to entertain shifting arguments” post-petition).

The Petition pointed to Watanabe’s high-temperature bonding as its motivation to combine Watanabe with Lee. Micron and Dr. Lee doubled down after institution, but now seek to disavow the Petition and his first declaration. The Reply refers to Keith Thompson’s graduate research and seven new exhibits to urge microwaving (EMIH) the wafers to 1000°C instead of Watanabe’s high-temperature processing at 900-1000°C. Not only is none of this in the Petition, but the Reply still offers nothing about how, exactly, one would microwave to 1000°C without also burning the wafers (or why microwaving wafers with embedded metal is a good idea).



Micron’s further effort to salvage Grounds 5-6 by urging the Board to deploy hindsight to align the wafers with new exhibits purporting to show methods proposed by the ’702 Patent itself also falls flat. With no answer to Dr. Przybylski’s refutation of the Petition’s theory of combining NOR and NAND architectures in Ground 6, Micron reverses itself to starting with Endoh in place of its original ground of obviousness over Lee in view of Watanabe and Endoh. None of this changes that Micron’s own expert did not know how to do it at his deposition and still doesn’t understand the Lee reference even after submitting two declarations.

The Reply gives short-shrift and effectively forfeits its Grounds 3-4 challenge based on Lee alone.

For Grounds 1-2, the Reply’s hand-waving doesn’t change that the Petition failed to meet its burden to show a motivation to combine Watanabe’s DRAM and EPROM embodiments, that Watanabe’s capacitor design does not satisfy the claimed “SOI pillar,” or how Watanabe’s high-temperature processing is at all enabled.

Instead of establishing that the Petition satisfied its burden, Micron lowers itself to attacking BeSang and its expert. Micron never addresses BeSang’s industry recognition or licensing. Paper 6 at 1, 5-6. Citing Micron’s internal emails about BeSang tellingly reveals that Micron thinks the right way to do business is ridiculing someone behind their back while stealing their ideas. Paper 20 (“Reply”) at 1 (citing EX1044-EX1045).

Memory industry veteran Dr. Przybylski prepared his own declaration with thorough and supported technical explanations. EX1051 at 9:14-10:1. He certainly is no parrot. *Western Digital v. Longitude Licensing*, IPR2023-01123, 2024 WL 85417, at \*8-9, \*12 (P.T.A.B. Jan. 8, 2024) (Board: Dr. Lee merely “repeats the argument[s] in the Petition”). Micron flagged not a single question Dr. Przybylski was unable to answer about his declaration. Reply at 3-4. Rather than questioning Dr. Przybylski about his opinions on Endoh or thermal budgets, for instance, Micron chose to use its cross-examination to explore other matters, like the district court infringement contentions. EX1037; EX1051 at 75:10-76:15. Micron’s complaints are not well-taken.

If one critical ITC decision from a decade ago permanently disqualifies an expert as Micron suggests, Reply at 4, then Micron will find itself without an expert and assuredly cannot meet its burden, *see Certain Semiconductor Chips with DRAM Circuitry*, Inv. No. 337-TA-819, 2013 WL 1494382, at \*29 (I.T.C. Mar. 26, 2013) (Dr. Jack Lee’s “conclusions were flawed.”); *id.* at \*30 (Dr. Lee’s claim “doubtful”); *id.* at \*31 (Dr. Lee’s testimony “lacks merit in light of his other questionable testimony”); EX2052 at 8:20-9:4, 20:19-26:6.

## **II. CLAIM CONSTRUCTION**

### **A. “stackable add-on layer”**

The Reply submits pages of arguments on the construction of “stackable add-on layer” with no justification why the Petition said nothing. Reply at 4-9. Because BeSang took no position in its response brief, Paper 18 (“POR”) at 13, all of Micron’s arguments plainly exceed the proper scope of a reply under Board rules, *see* 37 C.F.R. § 42.23(b). The Board cannot overturn its own regulations and allow Micron to initiate claim construction on reply. *Tunik v. Merit Sys. Protection Bd.*, 407 F.3d 1326, 1341 (Fed. Cir. 2005) (“[T]he Board’s regulation is the governing law and may not be overturned by the Board outside the procedural requirements of section 553” requiring notice and comment rulemaking.).

Micron argues that BeSang relies on the Board’s construction of “stackable add-on layer” to distinguish Lee in Grounds 3-4. Reply at 9. Micron provides no explanation or citation supporting its assertion, *id.*, perhaps because BeSang affirmatively stated it “does not concur with, nor is it relying upon” Micron’s proposed claim construction including for these grounds, POR at 49 n.1.

### **B. “SOI pillar”**

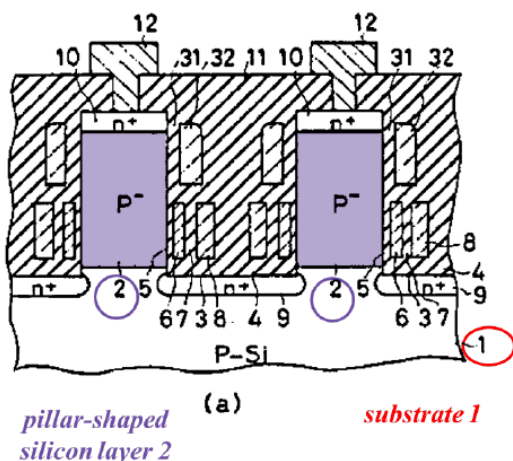
The construction of “SOI pillar” supports one argument in Ground 2 for challenged Claims 14-17.

It is not seriously disputed that the acronym “SOI” means silicon-on-insulator to one of skill, EX2029 ¶59; EX2028 at 79:20-80:3, or that “pillar” means structures taller than they are wide, EX2029 ¶62; EX1002 ¶64 (Lee: “pillar-form” means “vertical *columnar*-shaped” (emphasis added)).

Micron and its expert, now advocating for a fourth iteration of their construction of “SOI pillar,” still miss the mark. Reply at 9-10. Their 27-word construction does not resolve the dispute here over the shape of “SOI pillar.” *CoolIT Sys. v. Vidal*, No. 2022-1221, 2024 WL 981364, at \*5 (Fed. Cir. Mar. 7, 2024) (reversing Board claim construction that “may cause more confusion than clarity”).

The incorrect premise for Micron’s construction is the ’702 Patent’s description of an “unpattened, SOI layer,” Reply at 9-10 (citing EX1001 at 6:13-25). However, the claims don’t require a “SOI layer” but a “SOI pillar,” and the column 6:13-25 passage about unpatterned wafers does not pertain to the specific “memory cell[s]” on a “SOI pillar” required by Claims 14-17, EX1001 at 12:35-52.

Micron’s Reply instead relies on seven pages of testimony about the construction of “SOI pillar,” EX1041 ¶¶24-33, in an effort to undo Dr. Lee’s admission that “I don’t know what the plain and ordinary meaning is for ‘pillar,’” EX2028 at 66:22-67:13. Dr. Lee’s admission renders useless his thoughts on the construction of “pillar.” POR at 17; 37 C.F.R. § 42.100(b). And his latest construction incorrectly seeking to read “pillar” out of the claims is just not credible.



EX1008, Endoh, FIG. 7(a), annotated

EX1041 ¶¶24-25; Paper 24 at 8-9. Dr. Lee had no difficulty identifying a “pillar-shaped silicon layer 2” as a structure taller than it is wide (purple, at left) in a June 2023 IPR declaration signed the month after submitting his EX1002 declaration here. *Western Digital v. Longitude*

*Licensing*, IPR2023-01123, EX1003 ¶78 (annotations in original); EX2052 at 26:7-27:22 (Dr. Lee acknowledging prior declaration).

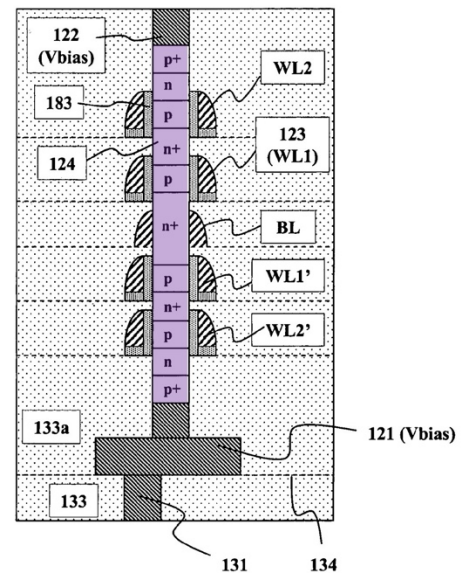
The Reply asks the Board to ignore the '702 Patent drawings, but even Micron's own cited caselaw doesn't support that. Reply at 11. *Krippelz v. Ford* is not instructive because BeSang is not relying on specific measurements from the patent figures. 667 F.3d 1261, 1268 (Fed. Cir. 2012); *see also Samsung v. Home Semiconductor*, IPR2015-00459, 2016 WL 1534753, at \*16 (P.T.A.B. Apr. 14, 2016) (distinguishing *Krippelz*).

*Hockerson-Halberstadt v. Avia* observed that patent drawings don’t define “precise proportions” but only “if the specification is completely silent on the issue.” 222 F.3d 951, 956 (Fed. Cir. 2000). The ’702 Patent specification is far from completely silent. It talks about the “aspect ratio of the SOI pillar 124” in Figure 4, EX1001 at 8:5-10, and column 9:19-20 warns

Fig. 20

Fig. 20

“[o]ne drawback of the structure in FIG. 20 is its high aspect ratio, which may cause toppling during processing,” *id.* at 9:19-20. Dr. Lee agreed that column 9:19-20’s teaching confirmed that “one can safely assume that its height is greater than its width” in Figure 20 (annotated at right). EX2052 at 56:1-16; *id.* at 55:3-22.



Micron’s conjecture about aspect ratios in the specification is a red herring; there is no serious debate here that the pillar in Figure 20 has a height greater than its width. EX1001 at Fig. 20; EX2029 ¶¶60-63; EX2052 at 56:1-16. Micron’s complaints about indefiniteness of “relatively small” is another red herring, Reply at 11, because that isn’t part of BeSang’s construction at all, POR at 13-17.

Dr. Przybylski does not support Micron's construction. Micron never explains what he "conceded" in his deposition testimony (EX1051) at page 64:3-7. Reply at 11. His exchange with Micron about how many memory cells are in one pillar,

EX1051 at 63:1-64:21, never departed from his opinion that the plain and ordinary meaning of “SOI pillar” is a structure taller than it is wide, EX2029 ¶¶59-63; EX1051 at 94:12-18.

Micron has no answer for BeSang’s overwhelming intrinsic and extrinsic evidence confirming the plain and ordinary meaning of a “pillar.” POR at 14-17; EX2029 ¶¶59-63. It attacks dictionary definitions of “pillar” but never provides its own definitions or establishes “pillar” has a different plain and ordinary meaning in the art. Reply at 12.

“SOI pillar” means “a silicon-on-insulator structure taller than it is wide.”

### **III. THE PETITION FAILED TO ESTABLISH UNPATENTABILITY BASED ON LEE AND WATANABE (GROUNDS 5-6)**

Micron’s new unpatentability theories for Grounds 5-6 confirm the Petition never met its burden. Its failure to address the Petition’s inadequate cross-referencing in Grounds 5-6, *see* POR at 37-38, 41-42, shows these grounds were inadequate and requires confirming patentability, *Netflix v. DivX*, 84 F.4th 1371, 1377 (Fed. Cir. 2023) (“A petitioner may not rely on a vague, generic, and/or meandering petition and later fault the Board for failing to understand what the petition really meant.”).

Micron asserts a motivation to combine because “Watanabe contemplates both stacking and sequential deposition” and that one of skill would have understood

that “Lee’s memory structures” could be “formed using Watanabe’s alternative stacking method.” Reply at 13-14. Simply disclosing “two alternative arrangements... does not provide a reason that a skilled artisan would have substituted” one for the other. *Virtek Vision v. Assembly Guidance*, 97 F.4th 882, 886-87 (Fed. Cir. 2024).

Micron’s combination never grapples with how, exactly, Lee’s memory cells

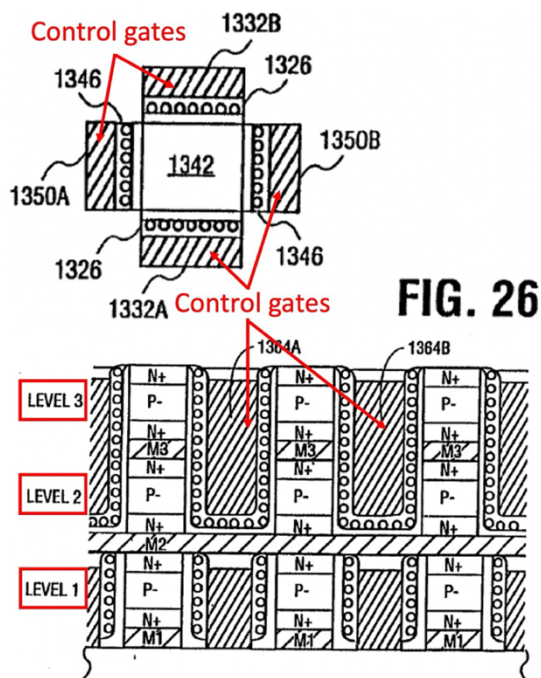


**FIG. 27A**

properly aligned. Reply at 13-17. At his reply deposition, Dr. Lee remained unsure whether levels d/b/e in Figure 12B (right) were insulators or conductors. EX1041 ¶57; EX2052 at 33:4-34:10. Even as trial concludes, Dr. Lee still lacks

could be implemented by stacking. Reply at 13-17. Lee’s interleaved levels have memory cells sharing control gates and use higher levels to pattern the lower ones. EX1007 at 25:32-41; *id.* at 24:66-25:31, 25:42-56, Figs. 24-27A. Micron points to no clear partition point in Lee’s array where the memory cells could be separately fabricated on different layers, let alone

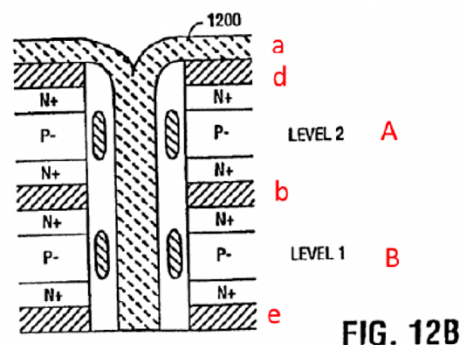


**FIG. 12B**

a basic understanding of Lee’s memory device, and his opinions cannot be credited. *See id.*

**A. Watanabe’s High-Temperature Processing Entirely Unravels Grounds 5-6**

The Petition affirmatively relied on Watanabe’s high-temperature processing to assert a motivation to combine, arguing a “POSITA would have found it obvious to combine Lee with Watanabe *because* Watanabe discloses... high-temperature bonding.” Pet. at 72 (emphasis added) (citing EX1005 at 5:1-6:14; EX1002 ¶149). Dr. Lee doubled down at his deposition, introducing three more exhibits and saying the thermal budget supported his opinion. EX2028 at 119:7-134:5 (testimony about EX1033-1035), 122:19-123:12 (Dr. Lee: Watanabe’s “upper layer... can withstand high temperature” unlike Lee’s “sequential deposition.”). Under questioning by Micron’s counsel, Dr. Lee unequivocally testified that “the processing of the upper layer transistors cannot go above 650 degrees C” due to the thermal budget. *Id.* at 123:13-124:7; EX1034/EX2027 at 715.

After BeSang’s response pointed out the glaring problem with Watanabe’s over-baking, POR at 24-27, Micron tucked away Dr. Lee’s original declaration and his three deposition exhibits, EX1002 ¶149; Reply at 6-8 (citing EX1033-EX1035 for claim construction); Paper 25 at 4 (Micron: thermal budget “Exhibits 1033-1035” only “identifying structural distinctions”).

Micron’s Reply acknowledges that the Petition’s motivation to combine Lee and Watanabe was infeasible, *see* Reply at 14-15, 25 (“Despite Watanabe’s bonding process at 900-1000°C....”). Micron jettisoning its prior testimony and evidence with a new reply theory on motivation to combine only underscores that its Petition fell short of its burden. *Intelligent Bio-Sys. v. Illumina Cambridge*, 821 F.3d 1359, 1369-70 (Fed. Cir. 2016) (affirming Board’s exclusion of reply arguments/exhibits presenting “an entirely new rationale” on motivation to combine).

Micron tries again with a brand-new reply declaration and seven reply exhibits refuting the Petition’s motivation to combine and Dr. Lee’s prior testimony. Reply at 14-15 (citing EX1048-1050, EX1052-1053, EX1059-1060); EX1041 ¶¶35-44. Micron now asserts that one of skill would have used “electromagnetic induction heating” (EMIH) for “bond[ing] stacked wafers at 900-1000°C.” Reply at 14-15.

“A reply may only respond to arguments raised in the corresponding... patent owner response.” 37 C.F.R. § 42.23(b). Micron’s decision to instead refute its own Petition, expert testimony, and evidence plainly exceeds the proper scope of reply and should be disregarded. *Illumina*, 821 F.3d at 1369-70; *Juniper Networks v. Swarm Tech.*, IPR2021-01445, Paper 64 at 12-14 (P.T.A.B. Apr. 20, 2023) (“[T]he ability to respond does not give Petitioner free reign to expand and revise its arguments by adding new features and configurations not... in the Petition.”); *Dexcom v. Waveform Techs.*, IPR2016-01680, 2018 WL 1137089, at \*13 (P.T.A.B.

Feb. 28, 2018) (excluding six reply exhibits petitioner filed “to fill a gap in its prima facie case”); Paper 24 at 3-4.

Regardless, Micron’s new reply argument still fails to establish a supported motivation to combine Watanabe and Lee. It argues that one of skill was aware of “several methods of bonding.” Reply at 15 (citing EX1059-EX1060). But the Reply only discusses one: EMIH. *Id.* Of the seven reply exhibits,<sup>1</sup> only three discuss EMIH for bonding, and they all originate from then-graduate student Keith Thompson: his patent, Ph.D. thesis, and an article. EX1048; EX1059-EX1060. None of these provide the solution Micron claims.

Thompson’s bonding experiments microwaved silicon wafers at 1000°C and then tested if they would separate. EX1059 at 93-94 (“Several <100> silicon wafers were bonded in the microwave.... Excellent bonds were obtained in only 5 minutes at 1000°C in both systems.”).

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<sup>1</sup> Two of Micron’s seven exhibits generally discuss the thermal budget, *see* EX1052-1053, and only confirm the thermal budget is “an integral of temperature over time” that BeSang and Dr. Przybylski already flagged. POR at 25. The last two discuss other applications of EMIH and never mention bonding layers. EX1049 (chemical vapor deposition); EX1050 (annealing).

Micron and Dr. Lee have no answer for how, exactly, Thompson’s microwaving at 1000°C would solve the thermal budget quandary. *Verance Corp. v. MZ Audio*, IPR2022-01544, 2024 WL 1513349, at \*11 (P.T.A.B. Apr. 8, 2024) (petitioner does “not address how Cabot’s allegedly inaudible small phase shifts work in combination with the large phase shifts involved in Srinivasan to achieve low audibility watermarks”). Dr. Lee opined that because of the thermal budget “processing of the upper layer transistors *cannot go above 650 degrees C.*” EX2028 at 123:13-124:7 (emphasis added); EX1034 at 715 (same).<sup>2</sup> Whether heated as Watanabe instructs, or microwaved by Thompson, the layers are heated to 1000°C. EX1005 at 6:6-8; EX1059 at 93-94; EX1041 ¶41 (Dr. Lee: Thompson microwaved wafers “typically between 950°C and 1050°C”). Both experts agree that exposing Lee’s levels to those temperatures risked destroying Lee’s memory. EX2028 at 123:13-124:7; EX2029 ¶¶70-77. Micron’s Reply hasn’t established *any* amount of

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<sup>2</sup> Dr. Lee’s reply declaration baldly contradicts his prior testimony that Lee’s transistors cannot go above 650°C, EX2028 at 123:13-124:7, now disagreeing that “Watanabe’s high-temperature bonding would damage Lee’s memory transistors,” EX1041 ¶35. His “additional declaration contradicts his deposition testimony and is therefore entitled to little if any weight.” *NHK Seating v. Lear*, IPR2014-01079, Paper 30 at 37 (P.T.A.B. Jan. 12, 2016).

time Lee’s memory could safely withstand those high temperatures within the constraints of the thermal budget. Reply at 14-15.

Micron doesn’t acknowledge a second shortcoming in its improper quest to meet its burden on reply: Thompson only microwaved “silicon wafers.” EX1048 at 5:30 (describing how “to heat silicon wafers 20 utilizing EMIH”); EX1059 at 93-94; EX1060 at 285. None of the Thompson exhibits microwaved wafers containing fabricated transistors with metal wiring or contacts like those in Watanabe or Lee. EX2029 ¶¶50-54; POR at 24-27. Anyone who has memorably placed their metal fork in a microwave oven would wonder how Thompson’s EMIH could be pulled off in Lee/Watanabe’s devices. Micron’s oversimplification of semiconductor processing again comes up short. Micron also doesn’t dispute that repeatedly baking Lee’s transistors is a bad idea. Reply at 15; POR at 25-26. On reply, it rewrites the Petition and Watanabe’s disclosure to assert its stacking could be accomplished “during a single bonding step.” Reply at 15. This is yet another improper new reply theory that need not be considered. *Juniper*, Paper 64 at 12-14; *Dexcom*, 2018 WL 1137089, at \*13. Because Dr. Lee testified that ever exceeding 650°C risked overbaking the embedded transistors, EX2028 at 123:13-124:7, even Micron’s re-imagined single high-temperature bonding step is risky.

Micron’s hypothetical single bonding step also finds no support in Watanabe, which instead instructs that “a number of process steps is increased” for each layer

because each layer is first bonded, then wired. EX1005 at 6:6-14; EX2029 ¶¶75-76.

Micron has no answer for how Watanabe’s 100-layer memory device could adhere to the thermal budget of its transistors in the base substrate, Reply at 15, which, as Dr. Przybylski explained, potentially required 100 high-temperature bonding steps because “[e]ach time an additional planar member is added to the existing stack, the collection to that point is necessarily heated again,” EX2029 ¶76; EX1005 at 4:35-38.

**B. Watanabe Offers Nothing To Pull Off Its High-Precision Alignment For Grounds 5-6**

Micron does not dispute that alignment was a significant issue and Watanabe offered nothing on alignment. Reply at 15-16; EX2028 at 109:20-110:16.

Instead, the Reply tries to cobble together a solution to Micron’s flawed combination, belatedly presenting two new exhibits to argue use of mechanical or optical alignment. Reply at 16 (citing EX1054-EX1055). This new rationale and Exhibits 1045-1055 are properly disregarded. *Juniper*, Paper 64 at 12-14; *Dexcom*, 2018 WL 1137089, at \*13.

Micron’s solutions to alignment are mechanically aligning grooves or optical “alignment marks,” EX1041 ¶46, essentially the same methods taught in the ’702 Patent: aligning “notch[es]” or “a wafer alignment mark,” EX1001 at 6:13-25. Micron using the challenged patent itself to find missing solutions is the epitome of

impermissible hindsight. *New U Life v. Axxess Global*, IPR2019-01141, 2020 WL 6260644, at \*14 (P.T.A.B. Oct. 23, 2020); *SPTS Techs. v. Plasma-Therm*, IPR2017-01674, 2019 WL 1154156, at \*3 (P.T.A.B. Mar. 7, 2019).

Even if considered, Micron still fails to show that one of skill would have achieved the delicate alignment required by Watanabe. Micron's new exhibits confirm that "wafer-to-wafer alignment is not at present a routine process." EX1054 at 315. It's undisputed that Watanabe required high-precision alignment within two feature sizes, EX2029 ¶¶78-80; EX2028 at 111:15-114:2, and Dr. Lee explained that the feature size was around 90nm in 2003, EX2028 at 46:4-13. Yet Micron's new exhibits are not that precise. Exhibit 1054 merely "provides  $\pm 5 \mu\text{m}$  [5,000 nm] alignment precision," EX1054 at 315, and Exhibit 1055 is not much better with an "alignment accuracy of 2-5  $\mu\text{m}$ ," or 2,000-5,000 nm, EX1055 at 273. Considering that Watanabe uses tiny wires that had to be aligned within two feature sizes (about 180 nm in 2004), references showing alignment precision of 2,000 nm or more are not good enough to achieve the needed interconnects by a factor of at least 10. Reply at 12 ("state-of-art process technology was at the 90-nanometer node" in 2004); EX2029 ¶¶78-80.

Micron and its expert say nothing about how EX1054-1055 could be successfully applied to Watanabe, let alone why one of skill would have looked to these particular references in the first place. Reply at 16; EX1041 ¶46. Without

such a showing, Micron cannot establish obviousness. *Berkeley Lights v. Univ. of British Columbia*, IPR2021-01249, 2023 WL 5155816, at \*2 (P.T.A.B. July 20, 2023) (Petitioner failed to show “how to apply the techniques such as ‘laser tweezers’ that Dimov mentions briefly, in a way that would have allowed further analyses of cells outside Dimov’s device.”). Micron argues Watanabe need not be self-enabling under *Raytheon v. Gen. Elec.*, but *Raytheon* only undermines Micron’s argument. Reply at 15-16. As in *Raytheon*, Micron presents no “prior art or other evidence” showing how to align Watanabe’s layers. 993 F.3d 1374, 1381 (Fed. Cir. 2021).

**C. The Petition Did Not Establish A Motivation To Combine And Reasonable Expectation Of Success For Lee, Watanabe, And Endoh**

The Reply also turns Ground 6 on its head. The Petition originally alleged Claims 16-17 were “Obvious over Lee in View of Watanabe and Endoh” because a “POSITA would have been motivated to combine Lee with Watanabe and Endoh.” Pet. at 73. But the modification was not “similar and predictable” as Micron promised in its two-paragraph writeup, and Micron is left scrambling on reply. *Id.* at 74; *id.* at 61 (ditto for Ground 4).

There’s no dispute that Lee’s NOR and Endoh’s NAND were different architectures. Pet. at 62-63; EX2028 at 75:9-76:14. BeSang pointed out that changing Lee’s NOR architecture into Endoh’s NAND flash required designing an

entirely new memory, and Micron never established how to pull off its modification. Reply at 17-19. Indeed, Dr. Lee couldn't explain how to do it at his deposition. EX2028 at 94:6-98:11. Nothing Micron presents on reply salvages the Petition's motivation.

Over four pages of briefing, Reply at 17-20, the Reply rewrites Ground 6 to use Endoh as its starting point: "Rather, a POSITA *would have begun with the teachings of NAND architecture, such as Endoh's*" to use the "memory cells of Watanabe's or Lee's array in series within that architecture." *Id.* at 19 (emphasis added), 17 (Micron: "construct Lee's and Watanabe's memory array using Endoh's NAND architecture"), 18 (similar). But arguing obviousness over C in view of A+B, is a different combination than the Petition's assertion of obviousness over A in view of B+C. *In re Magnum Oil Tools*, 829 F.3d 1364, 1380 (Fed. Cir. 2016); Pet. at 63 (Ground 4: "modify Lee's pillar structure to use the NAND architecture... as taught by Endoh"); *id.* at 65 (similar), 73 (Ground 6 relying on Ground 4).

First, Micron's reinvention of Ground 6, presenting "an entirely new rationale" and combination, impermissibly exceeds the proper scope of reply. 37 C.F.R. § 42.23(b); *Henny Penny v. Frymaster*, 938 F.3d 1324, 1330-31 (Fed. Cir. 2019).

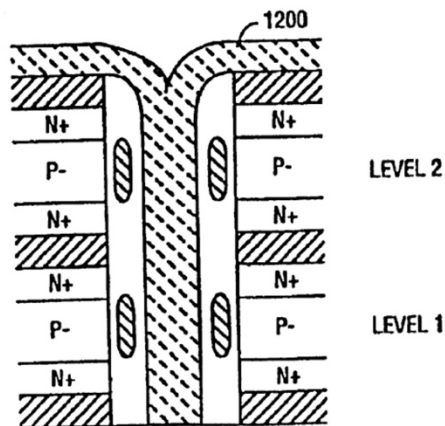
Second, Micron doesn't dispute that one of skill would not have been motivated to modify Lee's NOR with Endoh's NAND architecture. Reply at 17-19.

Everyone agrees there are “differences between NOR and NAND architectures.” *Id.* at 17; EX1041 ¶52 (Dr. Lee: ditto). Micron’s last-minute effort to rewrite Ground 6 with a new base reference is not just improper, but confirms the Petition failed to meet its burden. *Verance*, 2024 WL 1513349, at \*22 (confirming patentability: rejecting petitioner’s reliance “on Kudumakis as the base reference” and arguments to modify it because “the Petition relies on Tilki as the base reference”); *Henny Penny*, 938 F.3d at 1330-31.

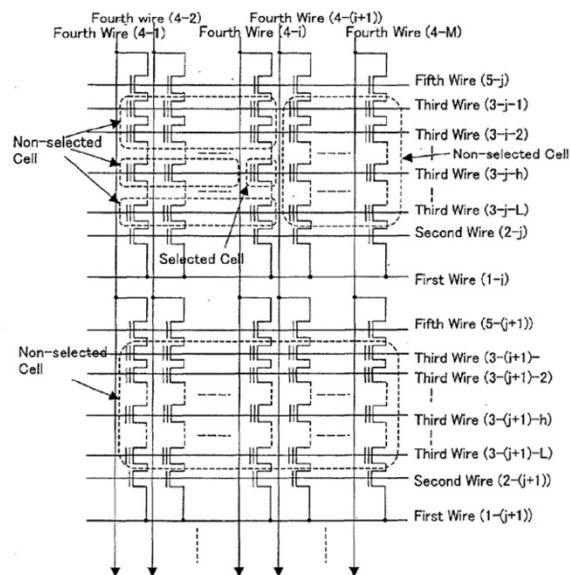
Third, the Petition never included an unpatentability theory premised on implementing *Watanabe*’s memory cells in a NAND architecture. Pet. at 73-74. Instead, Micron cross-referenced to Ground 4 and argued that “Lee in view of Endoh discloses Claims 16-17.” *Id.* at 73. The Petition’s Ground 4 theory was to “modify Lee’s pillar structure to use the NAND architecture and a serial connection as taught by Endoh.” *Id.* at 63, 65 (“modify Lee’s pillar structures... as taught by Endoh”); EX2028 at 92:22-94:11.

Micron obfuscates, arguing that the ’702 Patent and cited art are not “directed to a particular circuit design.” Reply at 17. First, resorting to the ’702 Patent only reveals Micron’s challenge is riddled with “improper hindsight.” *New U*, 2020 WL 6260644, at \*14; *SPTS*, 2019 WL 1154156, at \*3. Second, Micron is also wrong. Claims 16-17 claim a “memory structure” with specific circuitry, requiring “at least two nonvolatile memory cells” that “are vertically oriented and serially connected

together,” with Claim 17 providing further requirements including an “interconnect line.” EX1001 at 12:43-52. Recognizing this in the Petition, Micron relied on the following circuit designs in its own cited art to argue unpatentability of Claims 16-17:



Lee Fig. 12B



Endoh Fig. 65

Pet. at 62-64.

Citing Dr. Lee, Micron argues that one of skill would have implemented “the nonvolatile memory cells” in Watanabe or Lee in Endoh’s “NAND architecture.” Reply at 19 (citing EX1041 ¶¶55-56). Dr. Lee speculates, without any evidence or analysis, “the memory cells were interchangeable.” EX1041 ¶55. But as Dr. Przybylski pointed out, Lee’s Figure 12B memory cell taught a specific, interleaved structure with a shared control gate 1200 that was well-suited to Lee’s NOR VGA

array, but not a NAND memory that requires separate control gates for each transistor. EX2029 ¶129. Dr. Lee, again, has no response. EX1041 ¶¶51-59.

Dr. Przybylski’s ten-page analysis established Lee and Endoh’s fundamental incompatibility, including that converting Lee’s NOR into a NAND structure would require a “wholesale change” of “every physical, structural, electrical, and logical aspect” of the device. EX2029 ¶140; *id.* ¶¶128-43. Dr. Lee’s only response is a cursory one-sentence denial. EX1041 ¶55 (Dr. Lee: combining Lee with Endoh would have “no incompatible data flows, bit lines, sensing amplifiers, read and write protocols, or control circuitry”). Micron confirms it failed to carry its burden to explain why and how one of skill would have combined Lee and Endoh’s incompatible designs. *Samsung v. Elm 3DS Innovations*, 925 F.3d 1373, 1382-83 (Fed. Cir. 2019) (“complexity” of semiconductor manufacturing requires “specific evidence that a person of ordinary skill in the art would have reasonably expected success”).

Dr. Lee now says “[i]mplementing Lee’s memory cells in the NAND” architecture “was within the technical ability of a skilled artisan,” EX1041 ¶56, but could not himself do it at deposition, EX2028 at 94:6-98:11. Now he says that “[c]ounsel’s questions missed the point,” EX1041 ¶56, but his actions speak for themselves and show that modifying Lee into a NAND architecture was non-obvious. EX2029 ¶¶128-43.

**D. The Petition Failed To Show A Motivation To Combine Under Controlling Precedent**

Micron’s claim that any “suitable option” will suffice to meet its burden to establish a motivation to combine is “inconsistent with current caselaw.” Reply at 20. “It does not suffice to meet the motivation to combine requirement to recognize that two alternative[s]... were both known in the art.” *Virtek*, 97 F.4th at 886. Simply having multiple options “does not provide a reason that a skilled artisan would have substituted” one alternative for another. *Id.* at 887.

Micron’s citation to *Intel* is inapposite because it was undisputed the secondary reference would solve a problem in the primary reference, while using the primary reference’s memory “according to their established functions.” *Intel v. PACT*, 61 F.4th 1373, 1380-81 (Fed. Cir. 2023) (cleaned up). Here all of that is disputed. Micron baldly claims that combining Lee, Watanabe and Endoh would “improve[] integration density.” Reply at 20. This unsupported “[a]ttorney argument is not evidence” and offers nothing showing that replacing Lee’s shared NOR memory cell with Endoh’s NAND memory would work, let alone improve density. *Icon Health & Fitness v. Strava*, 849 F.3d 1034, 1043 (Fed. Cir. 2017). Because Lee’s dense NOR device shared four memory cells among each transistor structure, *see* EX1007 at 25:14-31, Fig. 26 (1332A-B, 1350A-B), but Endoh only had one, Reply at 19; EX1041 ¶55, replacing Lee’s memory cells with Endoh’s

would actually reduce Lee’s device density by up to a factor of four. Adding Watanabe’s stacking to the mix would only further degrade density, compared with Lee’s sequential deposition. EX2029 ¶¶80, 82-88.

Micron has no response to BeSang’s cited authority in *Samsung* that it needs to provide “specific evidence” showing a reasonable expectation of success because of the “complexity” of semiconductor manufacturing. *Samsung*, 925 F.3d at 1382-83 (cited in POR at 36).

Without a motivation to combine or reasonable expectation of success, patentability should be confirmed over Grounds 5-6.

#### **IV. THE PETITION FAILED TO ESTABLISH UNPATENTABILITY BASED ON LEE (GROUNDS 3-4)**

Micron does not seriously dispute that it is curtain closed on Grounds 3-4 based on Lee.

First, it claims BeSang “implicitly” adopts the Board’s construction of “stackable add-on layer” without pointing to a single instance, Reply at 21, and despite the fact that BeSang already stated it disagreed, POR at 13, 49 n.1. BeSang provided extensive argument showing how the Petition failed to meet its burden, including for Claim 13. POR at 49-56; *see also* EX2028 at 18:21-20:1.

Micron’s single-sentence argument that it “does not combine disparate embodiments” in Lee, offers no substance to refute BeSang’s response that the

Petition mixed and matched Lee’s pillar and rail stack embodiments in Figures 1A and 83A, respectively. *Compare* Reply at 21 *with* POR at 50-53.

Micron’s insistence that one of skill would know how to implement Lee in Endoh’s NAND architecture, Reply at 21, rings hollow when Micron’s own expert could not, EX2028 at 94:6-98:11, and similarly reimagines Grounds 3-4 but starts from Endoh’s architecture, instead of Lee as articulated in the Petition, Pet. at 63, 65; *supra* §III.C.

Finally, Micron cannot divest itself of its expert’s admission that Lee’s Figure 12B showed pillars with a single memory cell. Reply at 21-22. Its discussion of the construction of “SOI pillar” is mere misdirection, *see id.*, because Claims 16-17 both expressly require “at least two nonvolatile memory cells” in the claimed SOI pillar as previously explained, EX1001 at 12:45-47; POR at 54-55. Micron has no response to that. Reply at 21-22.

Patentability should be confirmed over Grounds 3-4.

## **V. THE PETITION FAILED TO ESTABLISH UNPATENTABILITY BASED ON WATANABE (GROUNDS 1-2)**

### **A. The Petition Did Not Establish That Watanabe Disclosed The “Nonvolatile” Limitation 13[b]**

Micron insists that its “Ground 1 does not combine Watanabe’s DRAM and EPROM embodiments,” Reply at 22, and then on the next page does exactly that: asserting that Watanabe’s “EPROM nonvolatile memory cell depicted in Figure 7”

could be manufactured like the DRAM in Figures 5-6, or could replace the DRAM memory cell in Figure 2A, *id.* at 23-24.

None of this is in the Petition, which expressly relied on Watanabe’s Figures 1 and 2A for limitation 13[b] and never argued that one of skill could replace the contents of Figure 2A’s cell. *Compare* Reply at 23 with Pet. at 16-18. The Board and BeSang already explained why the Petition fell short. POR at 58-59; Paper 9 (“I.D.”) at 15.

The Reply provides no motivation for its proposed modification to Watanabe’s Figure 2A. *Belden v. Berk-Tek*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (arguing one of skill “could” have made combination is insufficient). Micron’s resort to the ’702 Patent only confirms its Watanabe combination is riddled with “improper hindsight” and properly rejected. *New U*, 2020 WL 6260644, at \*14; *SPTS*, 2019 WL 1154156, at \*3. And the ’702 Patent does not support Micron’s oversimplified assertion that “Watanabe’s teachings... apply equally to any type of memory cell.” Reply at 23-24 (citing EX1001 at 9:24-28, Fig. 23). The full paragraph including the sentence Micron cites explains exactly how to change the non-volatile memory cell’s structure in Figure 23 for DRAM. EX1001 at 9:28-35.

#### **B. Watanabe Did Not Disclose A “SOI Pillar”**

The Board correctly recognized at institution that the Petition failed to demonstrate a “pillar” as used in the ’702 Patent. I.D. at 17. Under the correct

construction, Watanabe plainly lacks the claimed “SOI pillar.” POR at 60-62; *supra* §II.B.

Micron’s argument that Watanabe’s Figure 6C satisfies “pillar,” under BeSang’s construction, is deeply flawed. Reply at 25. As the Board correctly recognized, the Petition relied on Figure 2A to assert Watanabe disclosed a “pillar,” I.D. at 17; Pet. at 28-30, not Figure 6C, Reply at 25. Micron cannot switch embodiments on reply. *Corephotonics*, 84 F.4th at 1009 (“pointing to any new embodiments of a prior art reference not previously identified in the petition” is improper on reply (cleaned up)); *Provepharm v. WisTa Labs.*, IPR2018-00182, 2019 WL 2866032, at \*17 n.24 (P.T.A.B. July 2, 2019) (declining to consider “new figure” identified on reply).

Even considering Figure 6C, Micron fails to identify any silicon-on-insulator pillar taller than it is wide. Reply at 25; EX1005 at Fig. 6C. And Micron’s pivot to Endoh on reply also improperly rewrites the Petition. Pet. at 33 (“forming Watanabe’s pillar... as described in Endoh”); I.D. at 17 n.6 (recognizing Micron’s “argument to be that one of ordinary skill in the art would have formed Watanabe’s pillar structure on a SOI wafer”).

Patentability over Ground 2 should be confirmed.

**C. Watanabe’s Stacking Method Is Not Enabled**

Both experts agree that subjecting transistors to temperatures over 650°C exceeds their thermal budget. *Supra* §III.A. Micron now argues that “[d]espite Watanabe’s bonding process of 900-1000°C,” Watanabe was enabled. Reply at 25-26. Watanabe teaches no other method, and nothing in Watanabe shows its overbaking is enabled. EX1005 at 5:56-6:14; *Raytheon*, 993 F.3d at 1382 (“GE does not contend that the ’751 patent’s turbofan engine is enabled by other prior art or evidence of record. Instead, GE relies solely on Knip’s disclosure.”); *Ashland Oil v. Delta*, 776 F.2d 281, 297 (Fed. Cir. 1985).

Micron invokes Thompson’s EMIH wafer microwaving, Reply at 26 (citing EX1048), but that theory isn’t in the Petition, nor does Micron ever explain how it could be successfully deployed in Watanabe. Reply at 14-15, 26. As explained, whether Watanabe is baked in a furnace, or microwaved, the memory device is still burned. *Supra* §III.A. Watanabe’s non-enablement shows Grounds 1-2 are toast.

**VI. CONCLUSION**

BeSang respectfully requests the Board confirm patentability of all challenged claims.

ARMOND WILSON LLP

Dated: June 21, 2024

By: /Joseph Li/  
Michelle E. Armond (Reg. No. 53,954)

Micron Technology v. BeSang Inc.  
Patent No. 7,378,702 – IPR2023-00900

Douglas R. Wilson (Reg. No. 54,542)  
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Yue Han (Reg. No. 80,950)  
Attorneys for BeSang Inc.

**CERTIFICATE OF COMPLIANCE**

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that foregoing **PATENT OWNER’S SUR-REPLY**, exclusive of the parts exempted as provided in 37 C.F.R. § 42.24, contains 5,562 words and therefore complies with the type-volume limitations of 37 C.F.R. § 42.24.

ARMOND WILSON LLP

Dated: June 21, 2024

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Attorneys for BeSang Inc.

**CERTIFICATE OF SERVICE**

The undersigned certifies that pursuant to 37 C.F.R. § 42.6(e), a true copy of the foregoing **PATENT OWNER’S SUR-REPLY** and **EXHIBIT 2052** are being served electronically on June 21, 2024 to the following lead and backup counsel for Petitioners to the following email addresses:

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