Micron Technology v. BeSang Inc.

Patent Owner's Demonstratives

U.S. Patent No. 7,378,702 – IPR2023-00900

August 22, 2024

Judges Tornquist, McGraw, and Roesel

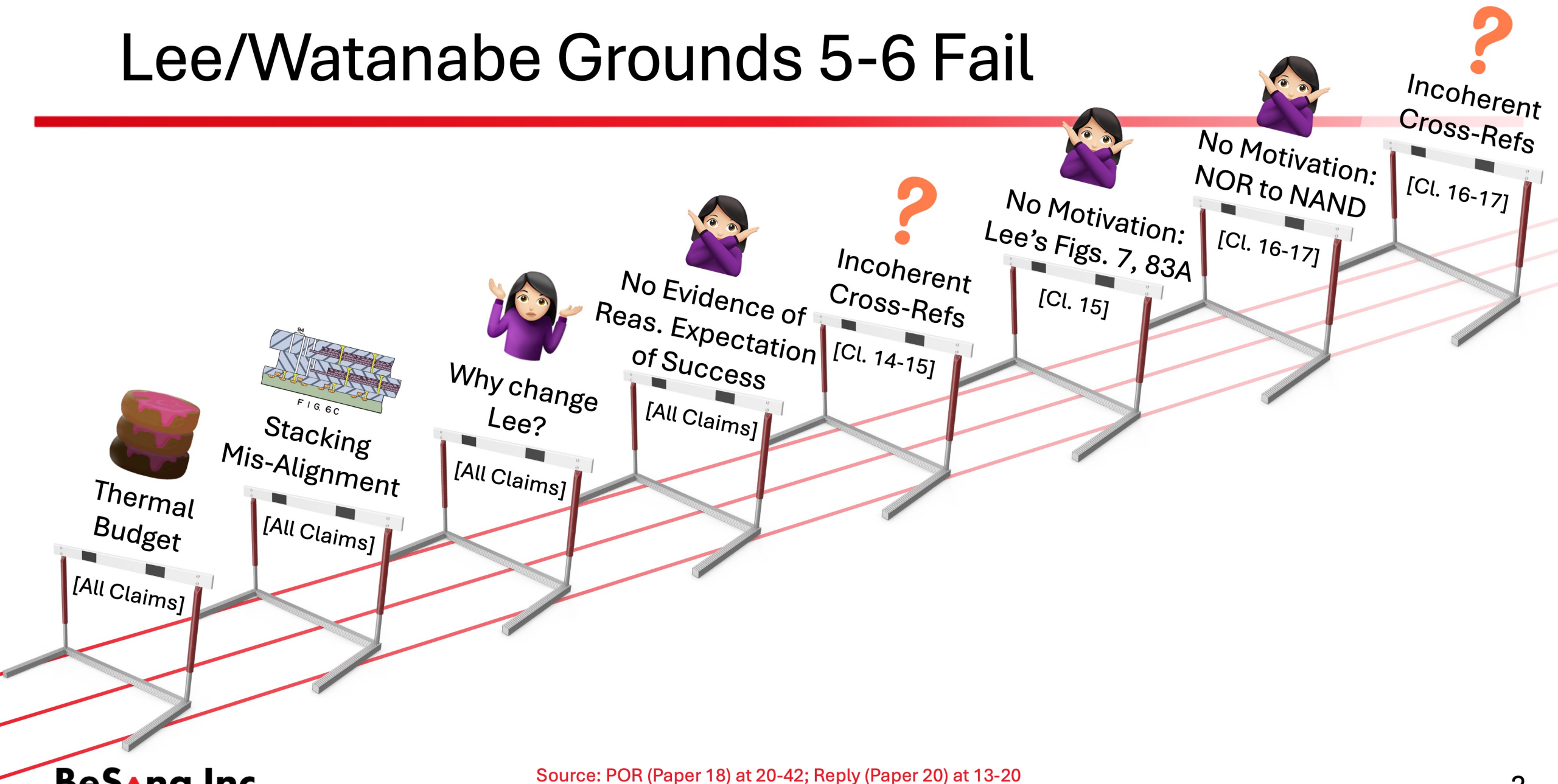
Demonstrative Exhibit - Not Evidence

IPR Grounds

Ground	Summary
1	Claim 13 is obvious over Watanabe (Ex-1005).
2	Claims 14-17 are obvious over Watanabe in view of Endoh (Ex-1006).
3	Claims 13-15 are obvious over Lee (Ex-1007).
4	Claims 16 and 17 are obvious over Lee in view of Endoh.
5	Claims 13-15 are obvious over Lee in view of Watanabe.
6	Claims 16 and 17 are obvious over Lee in view of Watanabe and Endoh.

Source: Petition (Paper 1) at 3-4
Demonstrative Exhibit - Not Evidence

Lee/Watanabe Grounds 5-6 Fail



BeSang Inc.

Source: POR (Paper 18) at 20-42; Reply (Paper 20) at 13-20
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Watanabe's Stacking Method

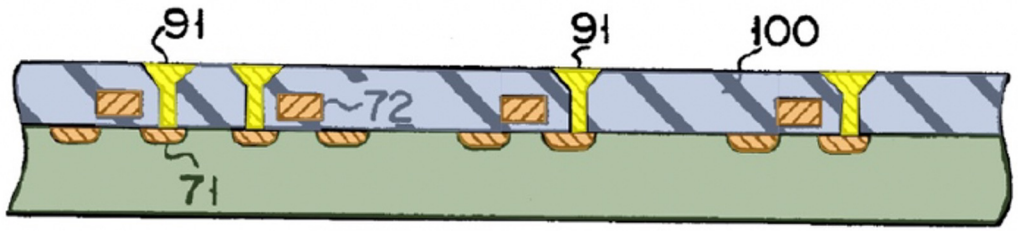


FIG. 6A

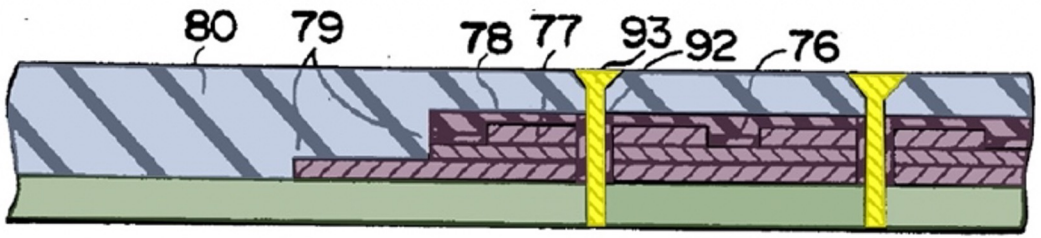


FIG. 6B

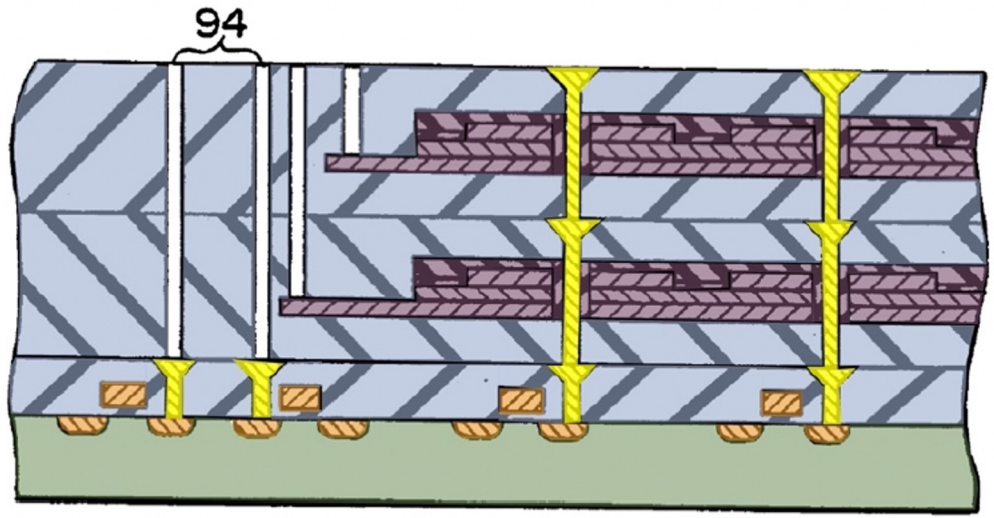


FIG. 6C

BeSang Inc.

Source: POR (Paper 18) at 8-9; EX1005 at Figs. 6A-6C
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Grounds 5-6: Thermal Budget

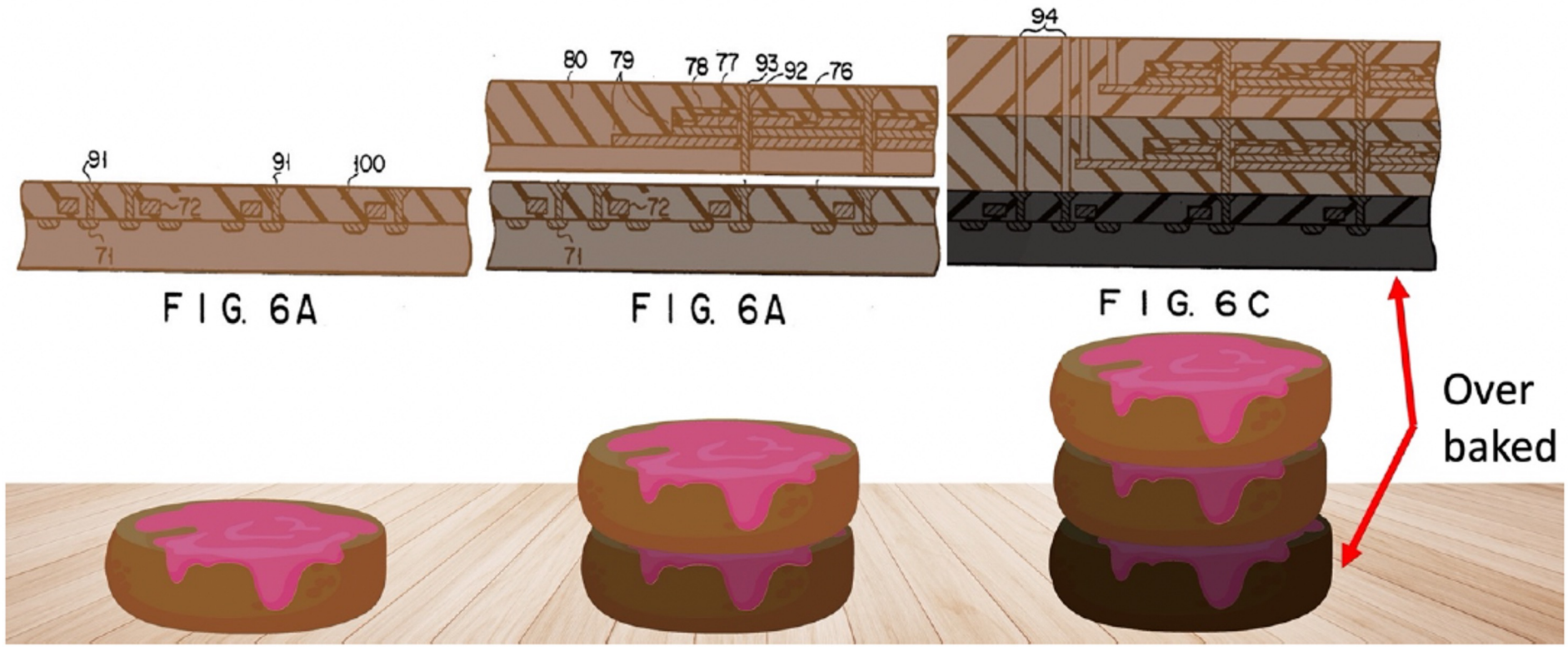


FIG. 6A FIG. 6A FIG. 6C

Source: POR (Paper 18) at 25-26; EX1005 at Figs. 6A-6C
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Dr. Lee: Thermal budget – can't go > 650 °C

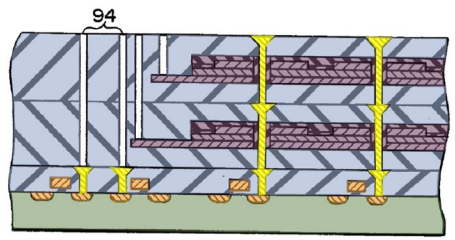


FIG. 6C

As shown in FIG. 6C, the planar members thus formed are bonded together. The bonding is made by thermal process of 900° to 1000° C. Thereafter, contact holes **94** are further formed, and a second interconnection wire **95** is buried thereinto as shown in FIG. **6D**, to complete a semiconductor memory device. In the stacking method, a number of process steps is increased, but a wiring accuracy is improved because the wiring is made every planar member.

13 In other words, the processing
14 of the upper layer transistors cannot go
15 above 650 degrees C, as described in this
16 reference. And the reason for that is
17 because if you do that, if you use anything
18 higher than 650 degrees C, then the
19 transistor at the lower layers, particularly
20 the CMOS transistor in the -- in the
21 substrate level --

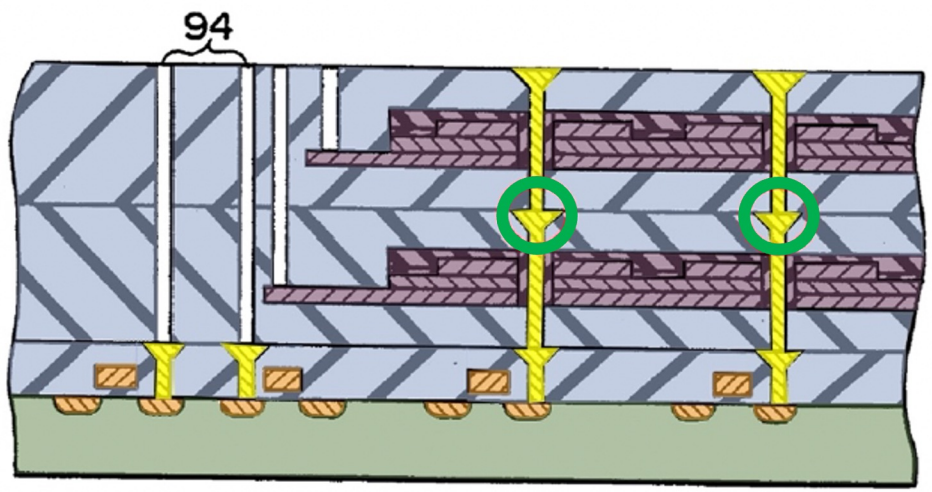
* * *

THE WITNESS: -- would experience dopant diffusion and interfacial oxide glow, which is detrimental to the characteristics of the transistors.

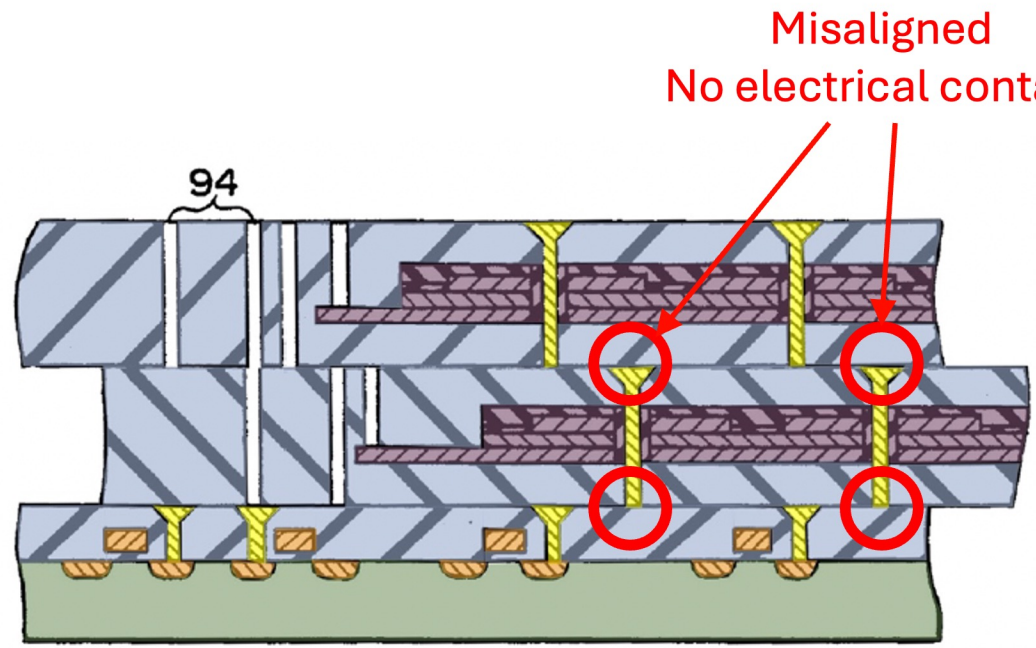


Source: POR (Paper 18) at 24-27; EX1005 at 6:6-8; EX2028 at 123:13-124:7
Demonstrative Exhibit - Not Evidence

Grounds 5-6: Watanabe's Alignment Rqmts



F I G. 6 C



F I G. 6 C

Source: POR (Paper 18) at 28-30; EX1005 at Fig. 6C
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Grounds 5-6: Can't Stack Lee's Layers

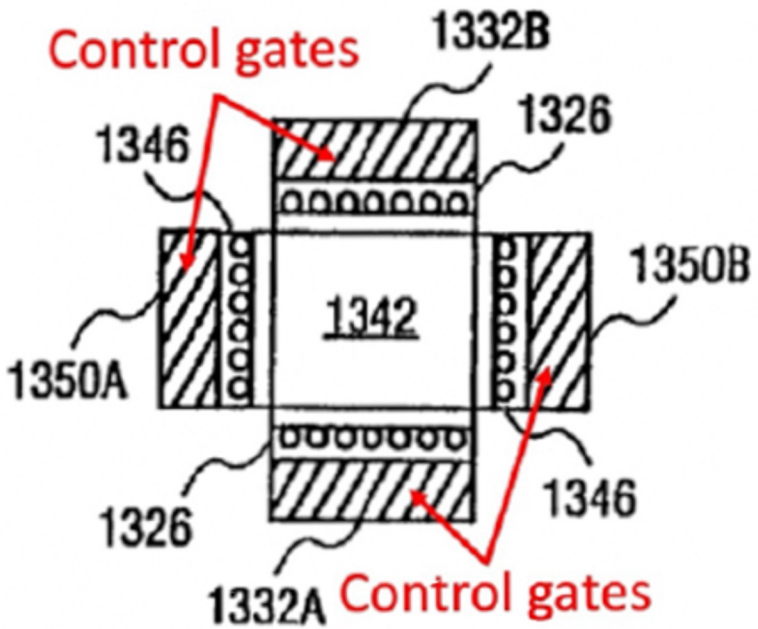


FIG. 26

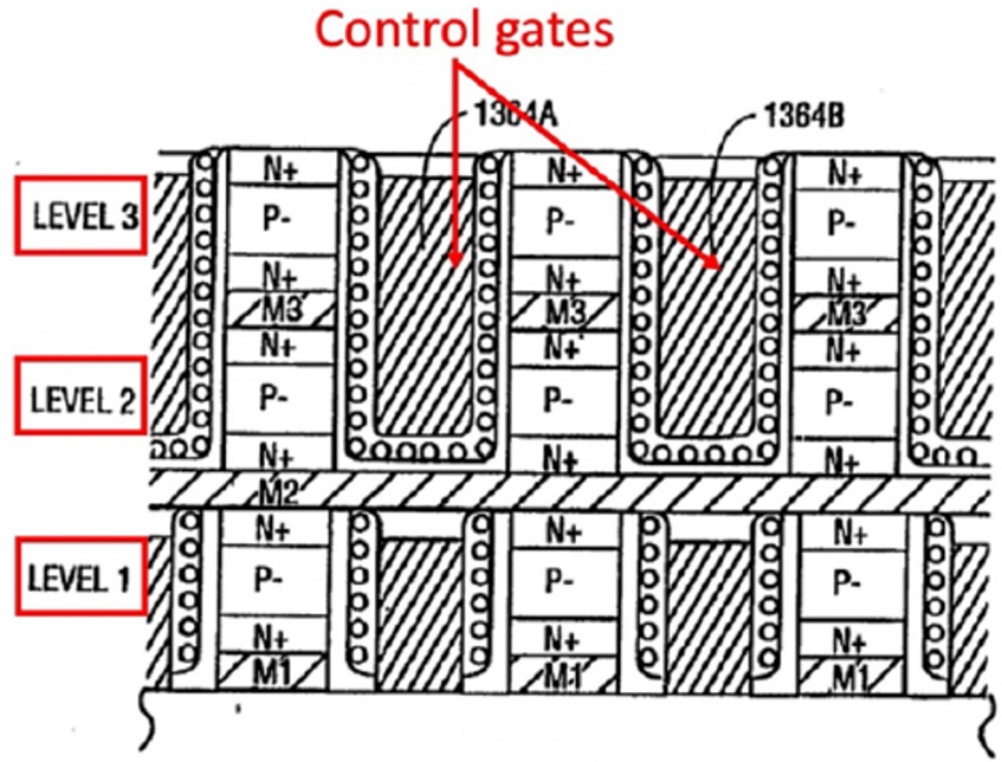
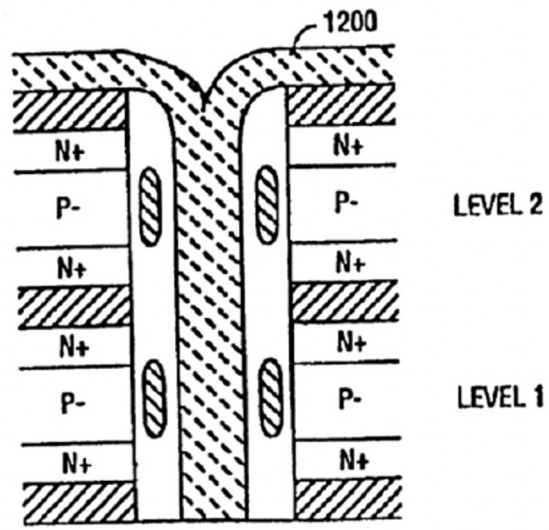


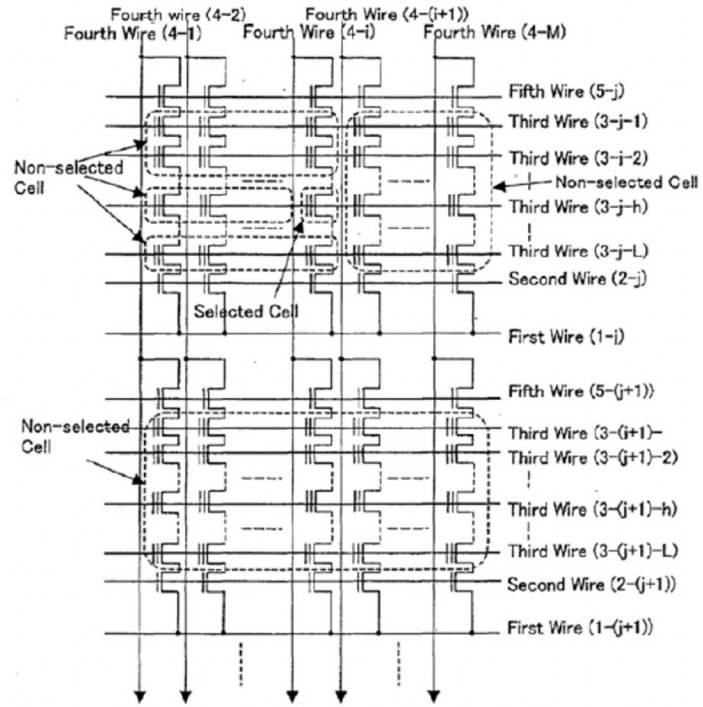
FIG. 27A

Source: POR (Paper 18) at 28-30; Sur-Reply (Paper 26) at 9; EX1007 at 25:32-41, 24:66-25:31, 25:42-56, Figs. 24-27A
Demonstrative Exhibit - Not Evidence

Grounds 5-6: No Motivation NOR → NAND



Lee Fig. 12B



Endoh Fig. 65

BeSang Inc.

Source: POR (Paper 18) at 42-48; Sur-Reply (Paper 26) at 19-21; Petition (Paper 1) at 62-64; EX1007 at Fig. 12B; EX1006 at Fig. 65
Demonstrative Exhibit - Not Evidence

Grounds 5-6: Dr. Lee doesn't understand Lee

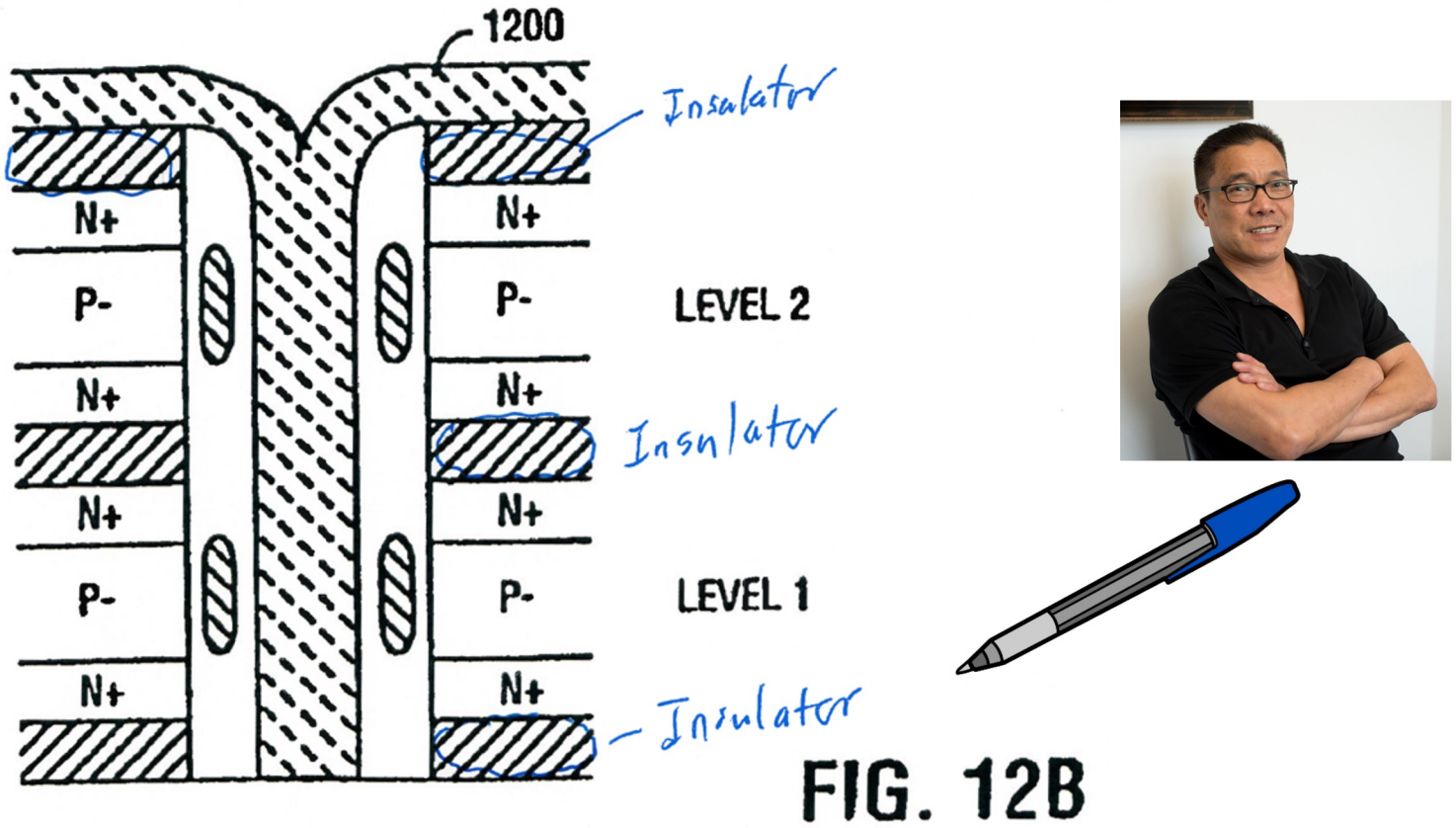


FIG. 12B

BeSang Inc.

Source: POR (Paper 18) at 44; EX2028 at 81:3-82:6; EX2025 (Dr. Lee's annotations)
Demonstrative Exhibit - Not Evidence

Grounds 3-4 (Lee): Dr. Lee admits no “SOI pillar”

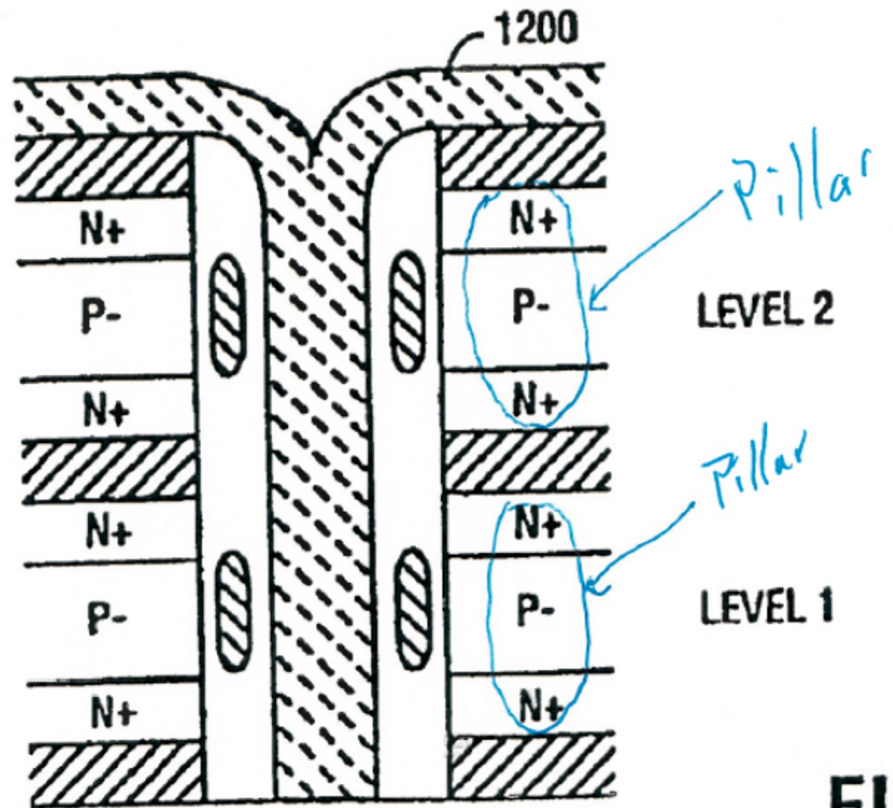
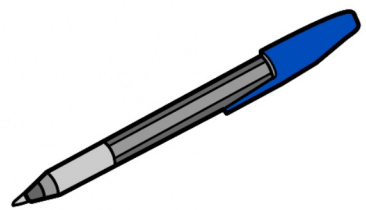


FIG. 12B

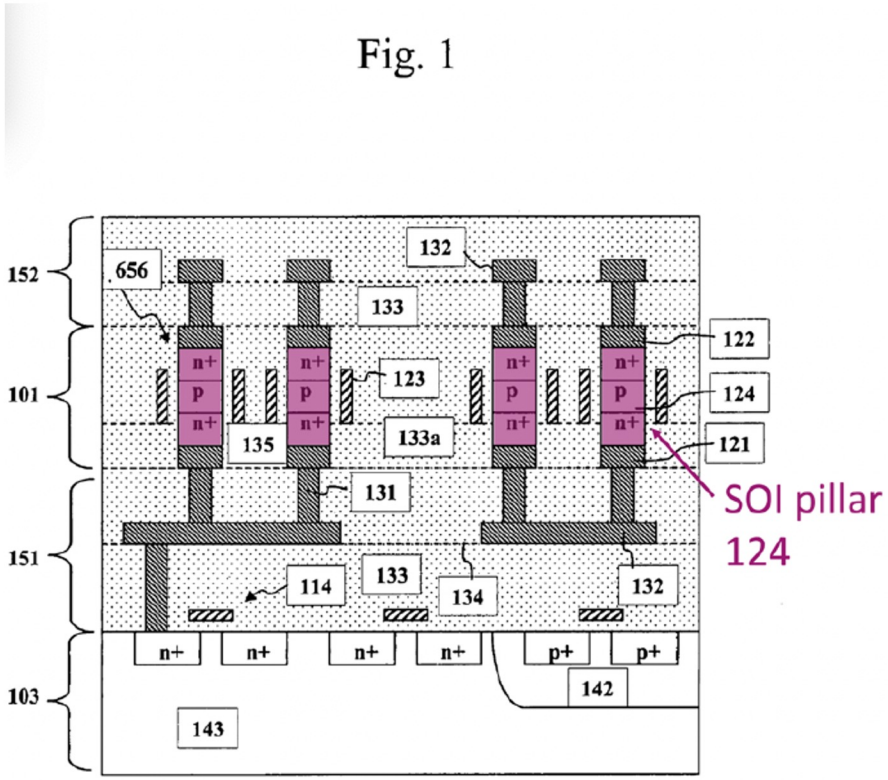
Claims 16-17 claim an “SOI pillar” with two memory cells.



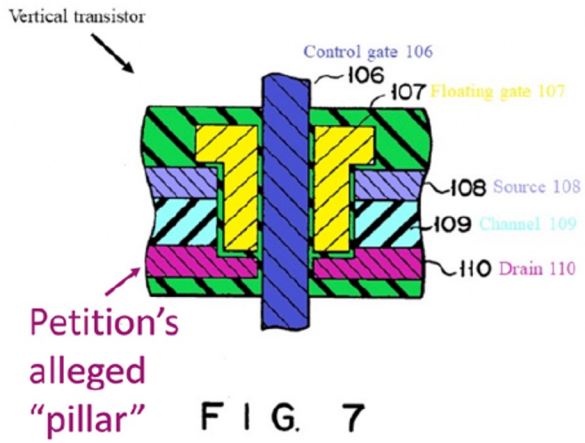


Source: POR (Paper 18) at 54-55; EX2024 (Dr. Lee’s annotations)
Demonstrative Exhibit - Not Evidence

Grounds 1-2 (Watanabe): No “SOI Pillar”



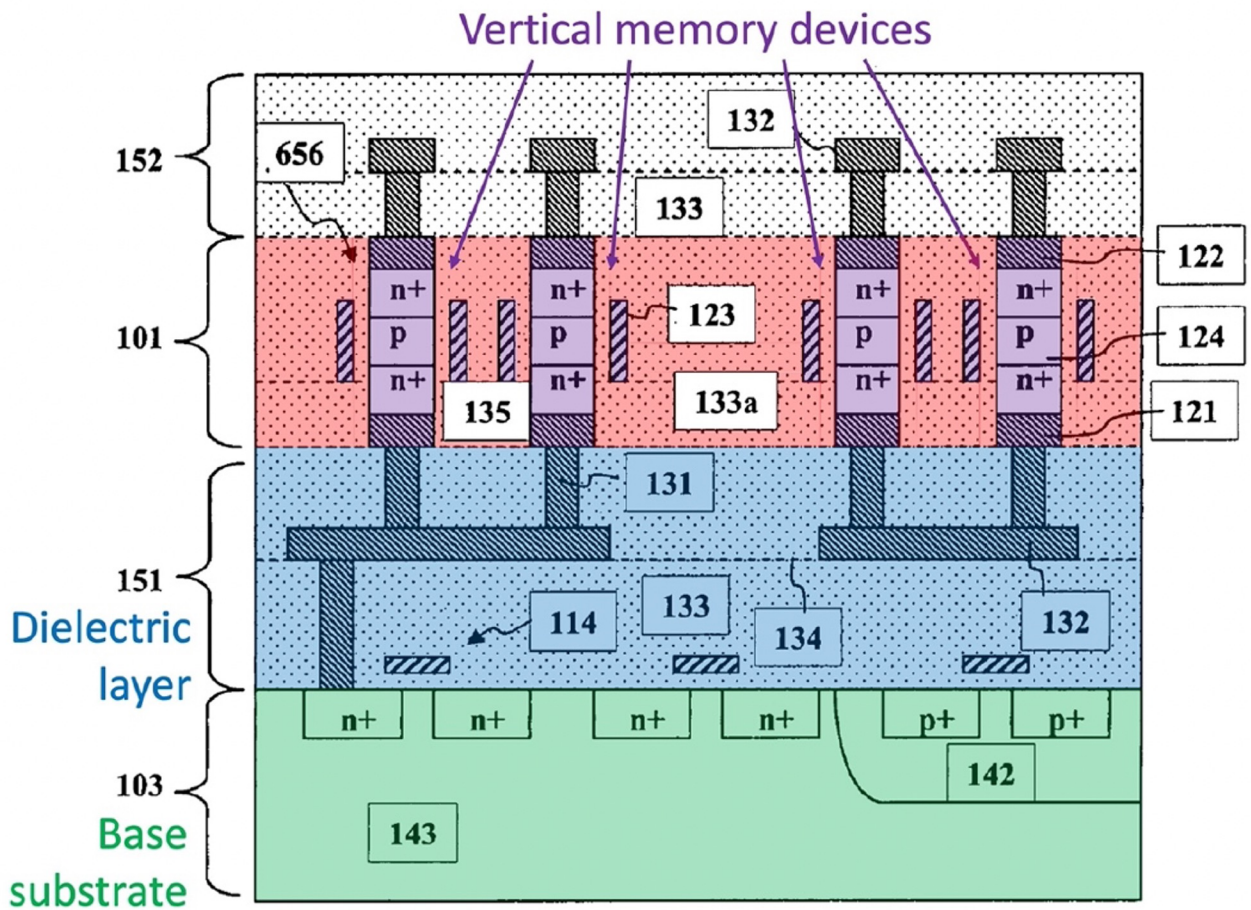
’702 Patent, Fig. 1 (annotated)



Pet. at 29 (label added)

Source: POR (Paper 18) at 60; EX1001 at Fig. 1; Petition (Paper 1) at 29.
Demonstrative Exhibit - Not Evidence

’702 Patent – Fig. 1



Source: POR (Paper 18) at 5-6; EX1001 at Fig. 1
Demonstrative Exhibit - Not Evidence

Pillars in the ’702 Patent

Fig. 4

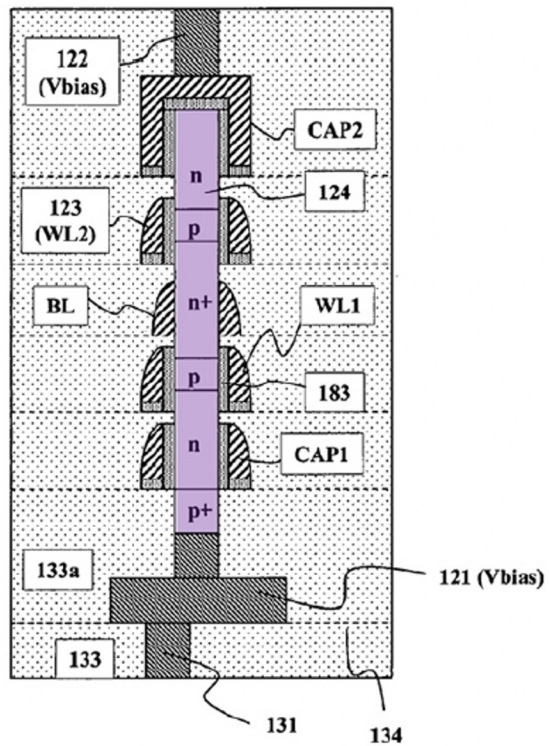


Fig. 20

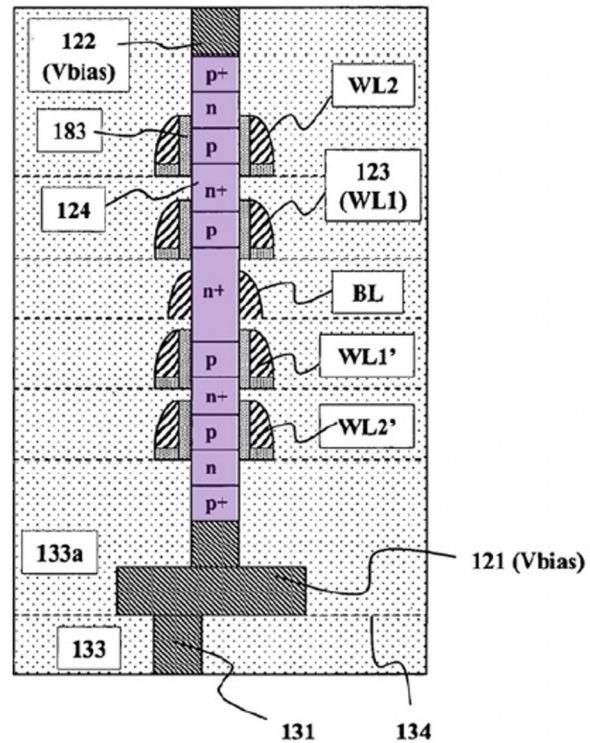
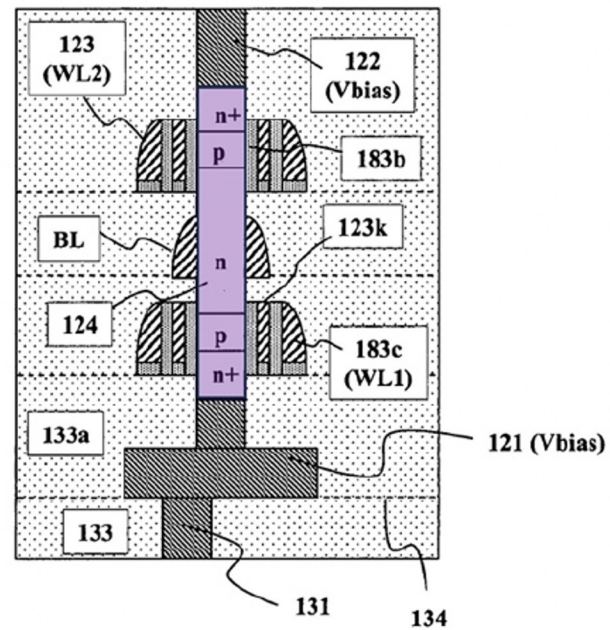


Fig. 27



Source: POR (Paper 18) at 14-15; EX1001 at Figs. 4, 20, 27
Demonstrative Exhibit - Not Evidence

’702 Patent - Claim 13

13. A semiconductor memory structure, comprising:

a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices;

a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells; and

the stackable add-on layer being bonded to the dielectric layer; and

wherein the memory cells are nonvolatile memory cells having at least one transistor.

Source: EX1001 at 12:24-34
Demonstrative Exhibit - Not Evidence

’702 Patent - Claim 14

14. The semiconductor memory structure of claim **13**, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a floating gate and a control gate on a SOI pillar.

Source: EX1001 at 12:35-38
Demonstrative Exhibit - Not Evidence

’702 Patent - Claim 15

15. The semiconductor memory structure of claim **13**, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a charge-trapping gate insulator and a gate on a SOI pillar.

Source: EX1001 at 12:39-42
Demonstrative Exhibit - Not Evidence

’702 Patent - Claim 16

16. The semiconductor memory structure of claim **13**, wherein at least two nonvolatile memory cells are vertically oriented and serially connected together and formed with a first SOI pillar.

Source: EX1001 at 12:43-46
Demonstrative Exhibit - Not Evidence

’702 Patent - Claim 17

17. The semiconductor memory structure of claim **16**, wherein the at least two nonvolatile memory cells on the first SOI pillar are serially connected with an interconnect line disposed on a dielectric layer, to a nonvolatile memory cell formed with a second SOI pillar.

Source: EX1001 at 12:47-51
Demonstrative Exhibit - Not Evidence