

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS, LLC,
Petitioner

v.

BESANG INC.,
Patent Owner.

Case No. IPR2023-00900
U.S. Patent No. 7,378,702

PETITIONER'S UPDATED LIST OF EXHIBITS

UPDATED LIST OF EXHIBITS

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Ex-1009	G. Groeseneken et al., <i>Basics of Nonvolatile Semiconductor Memory Devices</i> , in <i>Nonvolatile Semiconductor Memory Technology: A Comprehensive Guide to Understanding and Using NVSM Devices</i> (William D. Brown & Joe Brewer eds., 1997)
Ex-1010	Philip M. Sailer et al., <i>Creating 3D Circuits Using Transferred Films</i> , IEEE Circuits & Devices (1997)
Ex-1011	U.S. Patent No. 5,808,938 (“Tran”)
Ex-1012	U.S. Patent No. 6,982,905 (“Nguyen”)
Ex-1013	U.S. Patent No. 6,807,098 (“Jeong”)
Ex-1014	Kee-Ho Yu et al., <i>Real-Time Microvision System with Three-Dimensional Integration Structure</i> , IEEE Int’l Conference on Multisensor Fusion and Integration for Intelligent Sys. (1996)
Ex-1015	U.S. Patent No. 5,374,564 (“Bruel”)
Ex-1016	Horacio Mendez, <i>Silicon-on-Insulator: SOI Technology and Ecosystem – Emerging SOI Applications</i> , SOI Indus. Consortium (2009)
Ex-1017	U.S. District Courts – Combined Civil and Criminal Federal Court Management Statistics (Dec. 31, 2022), available at: https://www.uscourts.gov/statistics-reports/federal-court-management-statistics-december-2022
Ex-1018	T. Mikolajick et al., <i>The Future of Charge Trapping Memories</i> , 2007 IEEE Int’l Symposium on VLSI Tech., Sys. & Applications (2007)
Ex-1019	Complaint, <i>BeSang Inc. v. Micron Tech., Inc.</i> , No. 2:23-cv-00028 (E.D. Tex. Jan. 23, 2023)
Ex-1020	Jim Handy, <i>3D NAND: Benefits of Charge Traps over Floating Gates</i> , The Memory Guy Blog (Nov. 22, 2013)
Ex-1021	E. Bertagnolli et al., <i>ROS: An Extremely High Density MASK ROM Technology Based on Vertical Transistor Cells</i> , IEEE (1996)

Ex-1022	Tetsuo Endoh et al., <i>Novel Ultrahigh-Density Flash memory with A Stacked-Surrounding Gate Transistor (S-SGT) Structured Cell</i> , 50 IEEE Transactions on Electron Devices 945 (2003)
Ex-1023	F. Nemati & J.D. Plummer, <i>A Novel High Density, Low Voltage SRAM Cell with A Vertical NDR Device</i> , IEEE (1998)
Ex-1024	K.W. Lee et al., <i>Three-Dimensional Shared Memory Fabricated Using Wafer Stacking Technology</i> , IEEE (2000)
Ex-1025	<i>NAND vs. NOR Flash Memory</i> , Toshiba America Electronic Components, Inc. (2006)
Ex-1026	G.K. Celler & Sorin Crisoloveanu, <i>Frontiers of Silicon-on-Insulator</i> , 93 J. Applied Physics 4955 (2003)
Ex-1027	Timeline, Soitec, available at: https://www.soitec.com/en/company/soitec-activity/history (last visited Apr. 25, 2023)
Ex-1028	G. Shahidi et al., <i>Fabrication of CMOS on Ultrathin SOI Obtained by Epitaxial Lateral Overgrowth and Chemical-Mechanical Polishing</i> , IEEE (1991)
Ex-1029	MicroChemicals, Further Processing of Silicon Wafers: SiO_2 , Si_3N_4 , Metallization, Epitaxy and Dicing, available at: https://www.microchemicals.com/technical_information/silicon_wafer_sio2_si3n4_metallization_epitaxy_soi.pdf (last visited Apr. 28, 2023)
Ex-1030	Hiroshi Sakuraba et al., <i>New Three-Dimensional High-Density Stacked-Surrounding Gate Transistor (S-SGT) Flash Memory Architecture Using Self-Aligned Interconnection Fabrication Technology Without Photolithography Process for Tera-Bits and Beyond</i> , 43 Japanese J. Applied Physics 2217 (2004)
Ex-1031	Letter dated September 21, 2023 to counsel for Patent Owner from John Kappos
Ex-1032	<i>BeSang, Inc. v. Micron Technology Inc. et al.</i> , 2:23-CV-00028-JRG-RSP, D.I. 95 (E.D. Tex. Dec. 20, 2023), Order Granting Stipulation and Joint Motion to Stay Pending <i>Inter Partes</i> Review (“Order Granting Stay”)
Ex-1033	Y. Beilliard et al., <i>Advances Toward Reliable High Density Cu–Cu Interconnects by Cu-SiO₂ Direct Hybrid Bonding</i> , 2014 International 3D Systems Integration Conference (3DIC) (2014)
Ex-1034	Perrine Batude et al., <i>3-D Sequential Integration: A Key Enabling Technology for Heterogeneous Co-Integration of New Function With CMOS</i> , 2 IEEE J. Emerging and Selected

	Topics in Circuits and Systems 714-22 (2012)
Ex-1035	Rafael Reif et al., <i>Technology and Applications of Three-Dimensional Integration</i> , 2004 Electrochemical Society Proceedings Volume 261-76 (2004)
Ex-1036	Dr. Lee's Deposition Errata Sheet
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Ex-1041	Declaration of Dr. Jack C. Lee in Support of Petitioner's Reply to Patent Owner's Response
Ex-1042	Email thread from Sang-Yun Lee, dated Nov. 8-26, 2007
Ex-1043	Sang-Yun Lee & Junil Park, <i>Architecture of 3D Memory Cell Array on 3D IC</i> , IEEE (2012)
Ex-1044	Email thread from Scott DeBoer (Micron), dated Oct. 10, 2017
Ex-1045	Email from Scott DeBoer (Micron), dated July 19, 2016
Ex-1046	Sang-Yun Lee & Junil Park, <i>History and Trend of 3-Dimensional Integrated Circuit</i>
Ex-1047	International Technology Roadmap for Semiconductors: Front End Processes (2003)
Ex-1048	U.S. Patent No. 6,951,798
Ex-1049	Gerald Lucovsky et al., <i>Integration of Plasma-Assisted and Rapid Thermal Processing for Low-Thermal Budget Preparation of Ultra-Thin Dielectrics for Stacked-Gate Device Structures</i> , 33 Jpn. J. Appl. Phys. Vol. 7061-70 (1994)
Ex-1050	J. Wong et al., <i>Rapid Thermal Annealing of Deposited SiO₂ Films</i> , 35 Mat. Res. Soc. Symp. Proc. 514-20 (1985)
Ex-1051	Dr. Steven A. Przybylski Deposition Transcript (Apr. 5, 2024)
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Ex-1054	R. L. Smith & S. D. Collins, <i>A Wafer-to-wafer Alignment Technique</i> , 20 Sensors & Actuators 315-16 (1989)
Ex-1055	Frank Niklaus et al., <i>A Method to Maintain Wafer Alignment Precision During Adhesive Wafer Bonding</i> , 107 Sensors & Actuators

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Ex-1059	Keith Thompson, <i>Electromagnetic Fast-Firing for the Rapid Thermal Processing of Silicon</i> (Feb. 25, 2003) (Ph.D. dissertation, University of Wisconsin-Madison)
Ex-1060	Keith Thompson et al., <i>Direct Silicon-Silicon Bonding by Electromagnetic Induction Heating</i> , 11 J. Microelectromechanical Sys. 285-92 (2002)
Ex-1061	U.S. Patent No. 5,519,236
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CERTIFICATE OF SERVICE

I hereby certify that on August 19, 2024, I caused a true and correct copy of the foregoing **PETITIONER'S UPDATED LIST OF EXHIBITS** to be served electronically on counsel for Patent Owner at the following addresses:

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