

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC AND
MICRON TECHNOLOGY TEXAS, LLC,
Petitioner,

v.

BESANG INC.,
Patent Owner.

IPR2023-00900
Patent 7,378,702 B2

Record of Oral Hearing
Held: August 22, 2024

Before JON B. TORNQUIST, KIMBERLY McGRAW, and
ELIZABETH M. ROESEL, *Administrative Patent Judges*.

APPEARANCES:

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The above-entitled matter came on for hearing on Thursday, August 22, 2024, commencing at 1:00 p.m., via video teleconference.

P R O C E E D I N G S

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JUDGE TORNQUIST: Good afternoon. We are here for an oral hearing on IPR2023-900, Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology in Texas, LLC v. BESANG. I'm Judge Tornquist, and with me are Judges Roesel, and McGraw.

Who do we have from Petitioner? Petitioner, I think you might be on mute.

MR. KAPPOS: Good afternoon, Your Honors. My name is John Kappos, and I'm joined today by my colleague, Patric Reinbold. We represent the Micron Petitioners, and we'll be presenting on behalf of Petitioners today. I'm also joined on the public line by members of Micron's In House Legal Department.

JUDGE TORNQUIST: Okay. Welcome. And who do we have from Patent Owner?

MS. ARMOND: Good morning, Your Honor. This is Michelle Armond representing Patent Owner BESANG, Inc. I'm joined by my partner, Joseph Li, and we also have representatives from BESANG on the public line.

JUDGE TORNQUIST: Okay. Welcome. Per our oral hearing order, each party will have 60 minutes to present argument here today. And also, Petitioner, you have a LEAP practitioner, so you'll have an extra 15 minutes today. Petitioner, bearing the burden of proof will go first, and you may reserve time for rebuttal. Then we'll hear from Patent Owner, who could also reserve a short period of time for sur-rebuttal. And then we'll hear the rebuttal and sur-rebuttal arguments.

1 We have the parties' demonstratives, but as you go through those
2 demonstratives, you can make sure you identify each slide that you're using.
3 It makes for a much clearer record. With that, Petitioner, when you're ready.

4 MR. KAPPOS: Thank you, Your Honor.

5 JUDGE TORNQUIST: Just before you start, if you let us know
6 how much time you to reserve for your rebuttal?

7 MR. KAPPOS: I think it's going to be about 30 minutes reserve.

8 JUDGE TORNQUIST: Okay.

9 MR. KAPPOS: So, moving to slide 2, the grounds are shown here.
10 Claims 13 to 17 are the challenged claims. Watanabe, Lee 994, and Endoh
11 are the applied references.

12 Now moving to slide 3, before we discuss the grounds, there are
13 two claim construction issues that this Board asked the parties to address.
14 And the first relates to the term stackable add-on layer shown here in Claim
15 13. And we can see that the stackable add-on layer has vertically oriented its
16 semiconductor memory cells and must be bonded to the dielectric layer. But
17 we also see here that there is no requirement for low temperature processing
18 and no requirement for precision alignment.

19 Moving to slide 4, the Board made an initial construction of the
20 term stackable add-on layer to mean a layer that is formed separately from
21 the substrate and then bonded as whole to the dielectric layer positioned
22 above the substrate. The Board also noted we do not understand a stackable
23 add-on layer to include memory cells that are formed by sequential
24 deposition on or above a substrate without being added to a separately
25 formed substrate. Now, that construction requires the stackable add-on layer
26 to be formed separately from the substrate. In other words, not sequentially

1 deposited on the substrate. The Board then used that construction in its
2 tentative ruling that the Lee '994 prior art does not meet the challenged
3 claims as applied in Grounds 3 and 4.

4 Patent Owner did not address whether Lee 994 discloses all
5 elements of Claim 13 if the Board were to construe stackable add-on layer to
6 encompass sequential deposition. In other words, if not limited to require
7 the stackable add-on layer to be formed separately from the substrate, Patent
8 Owner gives no reason why Lee `994 does not invalidate Claim 13.
9 Therefore, it's now plain that the term stackable add-on layer needs to be
10 construed. And we agree with the Board's construction. Otherwise, Lee
11 alone renders obvious Claims 13 to 15.

12 Now, expert Lee, our expert witness, offered an opinion that
13 stackable add-on layer means a structure formed separately from the
14 substrate suitable to be bonded to the dielectric layer positioned above the
15 substrate. This interpretation is only slightly different from the Board's
16 interpretation. Patent Owner did not propose a construction.

17 JUDGE TORNQUIST: So, counsel, can we go back to that for
18 just a second?

19 MR. KAPPOS: Yes, Your Honor.

20 JUDGE TORNQUIST: Why are you changing layer, which is in
21 the actual structure -- in the actual term that we're construing? And why are
22 you changing that to structure?

23 MR. KAPPOS: Because the layer that's formed separately, it is
24 actually a composite of many constituent layers. So, there's an ambiguity if
25 we use the term layer to talk about the composite as well as the individual
26 layers that make up the composite. Expert Lee therefore recommended to

1 differentiate that by calling the composite a structure that's formed
2 separately.

3 JUDGE TORNQUIST: Okay. But you would agree that that
4 structure ultimately is a layer, although it may be composed of multiple
5 layers?

6 MR. KAPPOS: That's correct.

7 JUDGE TORNQUIST: Okay. Okay. Thank you.

8 MR. KAPPOS: Moving to slide 5, as the institution decision
9 notes, this construction is mandated by the intrinsic evidence. The '702
10 specification repeatedly states that the stackable add-on layer is used with a
11 separately fabricated substrate. And here in slide 6, even the '702 abstract
12 clearly states that the substrate and the stackable add-on layer are separately
13 fabricated, and then the stackable add-on layer is added or bonded to the
14 substrate.

15 Moving to slide 7, the second term at issue is SOI pillar, and this
16 term appears only in Dependent Claims 14 to 17, but not in Claim 13. So,
17 interpretation of this term has no relevance to Patentability of Claim 13.
18 And for the dependent claims, you can see there's no requirement for the
19 pillar to be taller than it is wide.

20 Moving to slide 8, Petitioner's construction is a doped stack
21 structure formed from a single crystal portion of a semiconductor wafer
22 transferred from one wafer to another previously fabricated wafer or similar
23 type of substrate. And this construction is again based on the intrinsic
24 evidence. At column 6, the '702 specification equates the term pillar with
25 doped stack structure. And at column 4, the '702 specification defines SOI
26 layer as a single crystal portion of a semiconductor wafer cleaved and

1 bonded, in other words, transferred from one wafer to another previously
2 fabricated wafer or similar type of substrate.

3 And slide 10, here is additional intrinsic evidence for the term
4 transferred.

5 Moving to slide 11, Patent Owner's construction is shown here as a
6 silicon on insulator structure taller than it is wide. But the '702 specification
7 does not support the notion that a pillar must be a structure that's taller than
8 it is wide. The '702 specification instead states that the aspect ratio, which in
9 this field means height to width, is relatively small. If small means less than
10 one, then the width would be greater than the height. Moreover, the '702
11 specification actually expresses a preference for the pillar to be wider than it
12 is tall for any one memory cell. The '702 specification states one drawback
13 of the structure in Figure 20, which is shown here, is its high aspect ratio,
14 which may cause toppling during processing. Now, while Patent Owner
15 argued that the '702 figures show the pillar as taller than they are wide,
16 figures are not assumed to be drawn to scale where the specification does not
17 so state and here it does not.

18 JUDGE TORNQUIST: Counsel, this is Judge Tornquist. If I
19 could just ask a question. Independent Claim 13 requires a vertically
20 oriented semiconductor memory cell. Then we go to the dependent claims
21 and now we have a pillar. What work is pillar doing in those claims versus
22 what's allowed in Claim 13?

23 MR. KAPPOS: Well, the term that's in the dependent claims is
24 SOI pillar. So, Claim 13 is not limited to an SOI pillar.

25 JUDGE TORNQUIST: But you all agree what SOI generally
26 means. It seems like the issue is what does a pillar mean versus what's

1 allowed in Claim 13 with a vertically oriented memory cell.

2 MR. KAPPOS: I think that's right that there's no dispute that SOI
3 means silicon on insulator but Claim 13 is broader. It doesn't require
4 necessarily a silicon based semiconductor.

5 JUDGE TORNQUIST: Okay. But then what is pillar doing in 13
6 and 14 that is differentiating beyond SOI over what's in Claim 13?

7 MR. KAPPOS: Well, the term pillar as explained in the intrinsic
8 evidence is a dope stack structure that is within this SOI layer. And that's
9 not a requirement of Claim 13.

10 JUDGE TORNQUIST: Okay. Thank you.

11 MR. KAPPOS: Moving on to slide 12, there is expert testimony
12 shown here explaining that in the 90 nanometer technology node, which is
13 the node that existed in 2004, the horizontal dimension of 90 nanometers
14 was much larger than the vertical dimension. So, the pillars were, as a
15 practical matter, wider than they were tall, the exact opposite of Patent
16 Owner's proposed construction.

17 Okay. Now, I'm going to move to slide 13, which shows the
18 grounds. And I want to start with the grounds based on Lee 994 in view of
19 Watanabe. And Lee 994 in view of Watanabe and Endoh, and those are
20 Grounds 5 and 6.

21 Moving to slide 14, in the Lee Watanabe combination, Lee 994
22 teaches 3D integration of memory cells in Figure 35, which is the high level
23 view. Figures 2 and 7 show more detail of the memory cells that are used in
24 layers 3104 within the structure 3101 in Figure 35. Figure 2 of Lee 994
25 illustrates a floating gate memory cell, which is pertinent to Claim 14, while
26 Figure 7 illustrates a charge trap gate memory cell pertinent to Claim 15.

1 The Lee 994 memory cells are, however, made by sequential deposition.
2 And moving to Slide 15, Watanabe teaches that memory cells can be made
3 by sequential deposition, as shown in Watanabe's Figure 5, or by stacking
4 structures formed separately from the substrate, as shown in Figure 6. Now,
5 under a proper construction of stackable add-on layer, it would have been
6 obvious to make Lee 994's 3D structure using the well-known alternative of
7 stacking structures formed separately from the substrate, as described in
8 Watanabe.

9 Moving to slide 16, Patent Owner's papers do not dispute that Lee
10 and Watanabe describe all limitations of Claims 13 to 15. Instead, they
11 dispute only the motivation to combine the prior art, and Patent Owner raises
12 two points in its response, and one new argument in its sur-reply. First,
13 Patent Owner argues that Watanabe requires bonding by heating to over 900
14 centigrade, which Patent Owner argues will exceed the thermal budget if
15 repeated numerous times. But note that thermal budget is related to the
16 product of temperature and time.

17 Moving to slide 17, Patent Owner argues that expert Lee testified
18 that transistors cannot go above 650 degrees centigrade for any amount of
19 time. But expert Lee then clarified in the same line of questioning at his
20 deposition that thermal budget is temperatures times time that is allowed for
21 processing.

22 JUDGE ROESEL: Counsel, this is Judge Roesel. Could I
23 interrupt you there? And before you turn to Patent Owner's arguments on
24 combinability of Lee and Watanabe, can you first explain why a person of
25 ordinary skill in the art would have combined these references?

26 MR. KAPPOS: Yes. The reason that you would combine these

1 references, I think you're referring, Judge, to the motivation to combine and
2 the reason to do that is because Watanabe teaches that you improve
3 integration density by stacking. Watanabe also teaches that wiring
4 alignment with electronic components is improved by stacking. Watanabe
5 further teaches that stacking reduces interconnection wire resistance. And
6 finally, stacking allows for the use of monocrystalline silicon whereas you
7 can't use that in a sequential deposition process. And these are all detailed in
8 the papers and in expert Lee's declaration as well. Did that answer your
9 question?

10 JUDGE ROESEL: Yes.

11 MR. KAPPOS: So, expert Lee further testified in his declaration
12 that you can perform bonding at 900 to 1000 centigrade without exceeding
13 thermal budget if the process time is controlled. And Patent Owner's expert,
14 Dr. Przybylski, also testified in his declaration that thermal budget is the
15 total amount of time spent at high temperature. So, all the experts therefore
16 agree that thermal budget is dependent on temperature and time, not
17 temperature alone. That means higher temperatures are tolerable for a
18 shorter period of time.

19 Moving to slide 18. It's incorrect to argue that Watanabe
20 necessarily exceeds thermal budget because it was known before 2004 the
21 effective filing date of the '702 Patent that electromagnetic induction
22 heating, also referred to as EMIH as disclosed, for example, by Thompson,
23 was available for rapid heating at 900 centigrade. If high temperature
24 heating is only for a brief time, and Thompson gives the example of five
25 minutes at 1,000 centigrade, then you do not exceed thermal budget.
26 Thermal budget is also not an issue for electromagnetic induction heating

1 because bonding multiple stackable add-on layers can be accomplished with
2 a single EMIH heating step.

3 Patent Owner's second argument is that Watanabe does not teach
4 wafer alignment, but by --

5 JUDGE TORNQUIST: Sorry, I'm sorry to interrupt you. Could
6 we step back to that previous argument? Watanabe issued in 1992; Dr.
7 Thompson's work appeared in 2003. Are you saying then that Watanabe
8 wasn't enabled until about what, 11 years later?

9 MR. KAPPOS: No, we're not saying that. We're giving an
10 example of a heating technique that could have been used to add multiple
11 stackable add-on layers. We believe Watanabe was enabled as of its initial
12 filing. Keep in mind that there's no requirement on the number of stackable
13 layers that you add on. And there's no evidence in the record that would
14 indicate that adding one stackable add-on layer would exceed thermal
15 budget or even a few. So, we think that persons skilled in the art would have
16 known how to operate Watanabe at the time Watanabe issued.

17 JUDGE TORNQUIST: Okay.

18 JUDGE MCGRAW: Doesn't show that Watanabe had about a
19 hundred layers? So, you would have to repeat the process a hundred times
20 and that might cause the process to last long enough to cause a problem with
21 the thermal budget?

22 MR. KAPPOS: Watanabe mentions that, but they don't require a
23 hundred layers. And so, a person skilled in the art would know, given the
24 number of layers that they're adding, what needs to be done to control for
25 thermal budget. And if you want more layers, perhaps using Watanabe, you
26 would use the sequential deposition method. So, these are stated to be two

1 alternatives that could be used depending on the optimization that the person
2 skilled in the art is seeking.

3 JUDGE TORNQUIST: Okay. So, let me follow up. One of
4 Patent Owner's arguments is that all the evidence for this type of heating
5 comes from, I think, three sources, a Ph.D. thesis, a Patent, and then the
6 other piece. But -- I'm going to -- let me come back to that question. Go
7 ahead.

8 MR. KAPPOS: Okay. I was proceeding into the alignment
9 argument where Patent Owner argues that Watanabe does not teach wafer
10 alignment. Again, by 2004, there were numerous alignment techniques that
11 were known to persons skilled in the art. For example, mechanical
12 alignment as described by Smith, and Smith dates all the way back to 1989.
13 Niklaus, which was a later publication, talks about optical alignment as well
14 as mechanical alignment. And we note here also that this '702 specification
15 itself lacks description of alignment techniques. The `702 merely refers to
16 wafer alignment marks, bump type alignment, and notch alignment, but
17 gives no details on how to perform these techniques. So, it's clear that the
18 '702 specification likewise relies on the knowledge of a person skilled in the
19 art. It would be unfair we submit to demand more from the prior art
20 description than what we demand from the challenged Patent on written
21 description.

22 And now in its sur-reply, Patent Owner argued that the 994 has
23 interleaved levels where memory cells share a control gate and use higher
24 levels to pattern lower ones. And shown here is a page with figures directly
25 from Exhibit 1007 at page 25 from the present record. This argument about
26 interleaved layers is entirely attorney argument. There is no expert who

1 testified that this interleave structure would be an obstacle to forming Lee
2 994's memory cells using Watanabe's stacking. Moreover, the petition does
3 not rely on Lee 994 Figures 26 or 27A. We focused as the Board will recall
4 on Figure 35 for the high level view of 3D integration. That figure shows
5 levels 3104 with vertical memory cells being formed on the interlayer
6 insulating layer, in other words, the claimed dielectric layer. So, pointing to
7 Figures 26 and 27 is misdirection in our view.

8 Now, moving to slide 20, Patent Owner also challenged whether a
9 person skilled in the art could have used the Lee 994 memory cells in
10 NAND architecture. There are only two options for making flash memory,
11 NOR and NAND circuit architecture. Both were well known and known to
12 be alternatives before 2004. The same memory cells can be used in either
13 NOR or NAND. Whether these memory cells result in NOR or NAND just
14 depends on how the memory cells are connected, the so-called architecture.
15 Therefore, we submit this situation falls squarely within the KSR precedent
16 where the Supreme Court has stated that when there are a finite number of
17 alternatives, any would be obvious. NAND and NOR are obvious
18 alternatives to a person skilled in the art.

19 Now, moving to slide 21, despite these being obvious alternatives,
20 we also provided the Endoh reference and noted Figure 65, just to give a
21 specific example of a circuit diagram for serial connection of memory cells.

22 Moving to slide 22, expert Lee testified, a person would have
23 found it obvious to use the NAND architecture because doing so increases
24 integration density. And expert Lee noted that Lee 994's memory cells can
25 be implemented in NAND or NOR architecture as taught by Endoh, where
26 Endoh provides the NAND flash circuit diagram. Expertly explained that

1 you simply drop in the Lee 994 memory cells into the NAND circuit
2 architecture. Now much was made of the cached regions labeled D, B, and
3 E in Figure 12, shown on slide 22. Expert Lee noted that these regions are
4 unlabeled, so it's unclear whether they are conductors or insulators.

5 Moving to slide 23, but either way, expert Lee testified that a
6 person skilled in the art would know how to arrange the Lee 994 memory
7 cells in series within NAND flash architecture by omitting the insulator and
8 incorporating control gates, or if the hashed regions are conductors, keeping
9 those regions which connect the transistors in series and incorporating
10 control gates.

11 Now, moving to slide 24, I want to transition back to the grounds
12 and now focus on the grounds based on Watanabe as primary reference, and
13 that's Grounds 1 and 2. Moving to slide 25, Watanabe's Figure 1 shows the
14 high level 3D integrated structure. The Watanabe specification states that
15 the memory cell of the present invention is applicable to any type of memory
16 device, i.e., a SRAM, a PROM, or a DRAM. The specification goes on to
17 say, moving to slide 26, the specification goes on to say, however, in the
18 description that follows the memory cell is depicted as incorporated in a
19 DRAM. Watanabe's Figure 7 shows EPROM, a non-volatile memory cell.
20 Figure 2A has a dotted box where you can plainly implement the EPROM
21 memory cell of Figure 7. Therefore, we submit that Grounds 1 and 2 do not
22 combine embodiments from Watanabe. Instead, Grounds 1 and 2 are
23 entirely consistent with Watanabe's teaching.

24 JUDGE TORNQUIST: So, counsel, this is Judge Tornquist. What
25 is the substrate when we use the EPROM of Figure 7?

26 MR. KAPPOS: The substrate would be, I believe, a layer that is

1 below 49, which is shown in the figure. So, it's not depicted here. This is
2 Figure 2A is focusing on the memory cells.

3 JUDGE TORNQUIST: Right. And so, in Figures 5 and 6, we
4 have them building up. But in those figures, we know what the substrate is
5 and that there's devices within them. How do we know that's true for an
6 EPROM device?

7 MR. KAPPOS: Well, because what Watanabe is saying is that you
8 would build the structure, the high-level structure of Figure 1 by swapping in
9 any of the various types of memory cells, SRAM, EPROM, or DRAM. And
10 so, it is, we believe within the person of skill in the art would know that
11 you're going to have a substrate layer below similar to what is depicted in
12 Figures 5 and 6. The only thing that you're changing are the memory cells
13 themselves.

14 JUDGE TORNQUIST: Is there any evidence to support that in the
15 record about the substrate with devices formed therein?

16 MR. KAPPOS: Yeah, I believe there's expert testimony to the
17 effect that you're putting in the EPROM memory cells and implementing
18 them within the same type of structures that Watanabe illustrates for DRAM,
19 right? Because Watanabe says up front, this is all applicable to any of the
20 memory cell types.

21 JUDGE TORNQUIST: Right. And the question we had, I think,
22 at the institution stage is, yes, it's applicable to those types, but would the
23 structures be exactly the same? So, if you have a chance and you can pull up
24 evidence that the substrates will be the same as what's shown in Figures 5
25 and 6 when you apply Figure 7 EPROM, I'd appreciate that.

26 MR. KAPPOS: Okay. Should I proceed?

1 JUDGE TORNQUIST: Yeah, you can proceed. Just when you
2 have a chance, I'd like those cites.

3 MR. KAPPOS: The specification goes on to say that you can
4 implement these within the description that follows the memory cells
5 depicted as incorporated in DRAM, right? And so, that was the point that
6 we were just moving on from. Grounds 1 and 2 do not combine
7 embodiments. They are entirely consistent, we believe, with the teaching of
8 Watanabe. Now, Patent Owner argues that Watanabe does not show an SOI
9 pillar because Watanabe's Figure 7 EPROM is not taller than it is wide. But
10 we submit that this is incorrect. Watanabe's figures first are not drawn to
11 scale, and the '702 Patent does not require an SOI pillar to be taller than it is
12 wide. So, Watanabe meets this limitation under a proper construction.

13 We very much appreciate the Board's thoughtful consideration of
14 this matter and I'd like to pass control to my colleague, Mr. Reinbold, who
15 will address the issues raised in the Patent Owner's motion to strike.

16 JUDGE TORNQUIST: Okay. Thank you.

17 MR. REINBOLD: Good afternoon. My name is Patric Reinbold
18 and I also represent Petitioner. As my colleague noted, I'll now address
19 Patent Owner's motion to strike. As shown here on slide 27, 37 C.F.R. §
20 42.23(b) permits a reply to respond to arguments raised in, among other
21 things, the Patent Owner preliminary response, Patent Owner response, or
22 decision on institution. Indeed, the need to rely on new evidence in response
23 may not arise until a particular point has been raised in the Patent Owner
24 response or decision on institution. So, the Federal Circuit has held that
25 there's no blanket prohibition against the introduction of new evidence
26 during an IPR, especially where it's a legitimate reply to evidence introduced

1 by Patent Owner. Here, each of the exhibits and portions of Petitioner's
2 reply that Patent Owner challenges were responsive to arguments raised
3 either by a Patent Owner or by the Board.

4 Moving to slide 28. To illustrate the responsiveness of each
5 argument, we grouped the challenge exhibits identified in the right column
6 of the table into seven topics and then identified in the left column the point
7 in the record at which the Board or Patent Owner previously raised each
8 argument to which the challenge exhibits are responsive. For example,
9 Patent Owner challenged the Petitioner's discussion and evidence supporting
10 its construction of the claim terms stackable add-on layer and SOI pillar,
11 which are shown here as Topics 1 and 2. But the Board requested that the
12 parties address these terms in the Board's decision on institution. In
13 addition, Patent Owner previously raised in its Patent Owner response
14 arguments that the high temperature bonding and multiple bonding steps,
15 Topic 3, would exceed the thermal budget and damage transistors in the
16 devices.

17 Moving to slide 29. Similarly, Patent Owner previously raised in
18 its Patent Owner response arguments that the prior art does not enable
19 precise wafer alignment, Topic 4, and interchangeability of NAND nor
20 architecture, Topic 5, nor provide motivations to combine Lee and Watanabe
21 and Lee, Watanabe, and Endoh as proposed in the petition, Topic 6.

22 Finally, both the Board and its decision on institution and Patent
23 Owner in its response raised arguments related to whether the petition
24 combines separate embodiments of Lee and Watanabe, Topic 7. Moreover,
25 Petitioner provided these responsive arguments and evidence to Patent
26 Owner as soon as possible. For example, Petitioner made Exhibits 1033 to

1 1035, available five days before expert Lee's first deposition. But despite
2 having the opportunity to depose Dr. Lee on February 6th, and then again on
3 June 12th, and address these issues in its response, Patent Owner declined to
4 do so. And notably, Patent Owner did not object to Exhibit 1034, and even
5 cited it in their response, evidencing that Patent Owner's issue with the
6 evidence is selective.

7 JUDGE TORNQUIST: Counsel, this is Judge Tornquist. Can I
8 ask a quick question? One argument they make in their motion to strike on
9 page six is that you're actually switching to start with Endoh's NAND
10 structure, and then bringing in the memory cells. Do you have a response to
11 that?

12 MR. REINBOLD: Thank you, Your Honor. Our response is that
13 we're not switching the order of prior art references, rather as Dr. Lee
14 explained in both his deposition and his declaration, that rather NAND and
15 NOR were interchangeable, and were both known techniques, and rather
16 any -- a person of ordinary skill would have known to drop in the memory
17 cells of Lee into NAND or NOR architecture. Patent Owner's argument is
18 rather a combinability, a physical combinability of the prior art references,
19 which is not required.

20 JUDGE TORNQUIST: Okay.

21 MR. REINBOLD: Moving on, the remaining challenged exhibits
22 were provided to Patent Owner on May 3rd when Petitioner filed its reply.
23 And even after that date, Patent Owner had the opportunity to depose Dr.
24 Lee on June 12 and address these arguments and evidence in its sur-reply
25 filed June 21. Thus, each exhibit was at least presented to Patent Owner
26 before Dr. Lee's second deposition was taken and before Patent Owner's sur-

1 reply was due. So, not only were the challenged arguments and evidence
2 properly responsive to arguments raised previously by the Board or Patent
3 Owner, but also Petitioner did not revise the grounds of the petition or recant
4 any of Dr. Lee's testimony as Patent Owner argues. Each exhibit and
5 portion of Petitioner's reply relying on those exhibits properly responded to
6 Patent Owner's arguments and the requests from the Board. Thus, the Board
7 should deny the motion to strike Petitioner's arguments and evidence
8 responding to Patent Owner and the Board. Thank you for your time.
9 Petitioner reserves any remaining time for rebuttal.

10 JUDGE TORNQUIST: Okay. Thank you very much. Okay.
11 With that, we will shift to Patent Owner.

12 MS. ARMOND: Good morning, Your Honor. I believe you
13 already have all of our demonstratives.

14 JUDGE TORNQUIST: Yes.

15 MS. ARMOND: So, I won't clutter up the screen with them. All
16 right. Let's --

17 JUDGE TORNQUIST: Just before you start, if you'll let us know
18 how much sur-rebuttal time you'd like to reserve.

19 MS. ARMOND: Fifteen minutes.

20 JUDGE TORNQUIST: Okay. Thank you.

21 MS. ARMOND: All right. Thank you, Your Honor. So, let's start
22 with the Lee Watanabe ground. The thermal budget issue is a complete
23 basis to confirm Patentability of all of the challenged claims over both
24 Grounds 5 and 6, which is the Lee Watanabe combination, as well as
25 Grounds 1 and 2, which is the Watanabe combination.

26 So, as we're all familiar with, Watanabe teaches bonding at 900 to

1 1,000 degrees Celsius. Now, we just heard from Petitioner, and they are
2 claiming that our theory relies on multiple bonding processes at this
3 temperature. So, Watanabe does teach that, but let's assume that Petitioner
4 is right. And there's only a single bonding at 900 to 1,000 degrees Celsius,
5 as Watanabe teaches. That still exceeds the thermal budget and provides --
6 nullifies any motivation to combine Lee and Watanabe. And this is our
7 record evidence. We have both experts on the record testifying that you
8 cannot take transistors above 650 degrees Celsius safely, or you risk
9 destroying them. Full stop. We have Micron's own Exhibit 1034, that says
10 the exact same thing and corroborates that expert testimony. So, on this
11 record, we have no evidence that there is any amount of time that you can go
12 above 650, certainly not to 900 to 1,000 degrees Celsius, without risking
13 destroying the transistors. And so, what Micron is asking you to do, because
14 of course Micron bears the burden here, is to find that a chip designer who is
15 designing these super complicated chips is going to then say let's throw it in
16 the oven, or I guess now the microwave and burn it. And no one would do
17 that. There's no motivation to combine. This is a complete basis to confirm
18 Patentability and we can really just stop right there.

19 JUDGE TORNQUIST: So, counsel, let me ask you a question.
20 When Dr. Lee came back in reply on paragraph 42, he said in these
21 references that he gave, that they were actually able to do this within five
22 minutes and that the FETs did not degrade in performance. You've argued
23 that there's no transistors, I believe, in these silicon wafers. So, where is the
24 discrepancy?

25 MS. ARMOND: So, remember Lee and Watanabe have transistors
26 at the bottom that are the control, right? That are controlling these memory

1 arrays. So, those transistors cannot go above 650 degrees C. So, that's the
2 transistors we're talking about. The pattern wafers above, there's an
3 additional consideration, you know, because you're going to be forming
4 transistors for memory cells. And then, if you go about them, there's the
5 additional concern that you're going to make that dope and start diffusing
6 and you're going to get performance that's not within the spec of your
7 transistors. So, there's actually two things going on, but, you know, there is
8 no dispute, and Micron is not disputing that those control transistors that are
9 in the bottom and the substrate cannot go above 650 degrees C.

10 JUDGE TORNQUIST: Okay. So, maybe I didn't phrase that
11 clearly enough. Let me break it down. In your sur-reply, you argued that
12 the Thompson references actually are only bonding silicon wafers, if I
13 understood you correct. Is that correct?

14 MS. ARMOND: That Thompson only talks about silicon wafers
15 unpatterned ones.

16 JUDGE TORNQUIST: Okay. And so, if I understood that right,
17 Thompson wafers, at least according to you, did not have transistors within
18 them when they were bonded with this technique?

19 MS. ARMOND: Exactly. And that's another reason why this
20 whole microwave theory that we're hearing about at the last minute would
21 not work. Correct.

22 JUDGE TORNQUIST: Okay. And that's what I was trying to get
23 at because Dr. Lee in that paragraph 42 says, no, there were FETs in there,
24 which are field effect transistors, right? So, I'm trying to see, is he correct
25 that there actually were transistors here when Thompson's were.

26 MS. ARMOND: So, here's the problem with Thompson, right?

1 Whether there were or were not transistors in there, and again, they've given
2 us just all of these pages at the last possible minute in reply and switched up
3 their theory, which is of course improper because we don't get a chance to
4 submit our own expert testimony or rebuttal evidence or whatever. But like
5 whether there were or not, it doesn't matter. There is no safe temperature
6 you can take it up to from 900 to 1,000, and both experts agree to that. So,
7 and again, like Thompson is not building these super complicated 3D
8 structures.

9 JUDGE TORNQUIST: Okay. It's not your burden to show that
10 you can do this at necessarily --

11 MR. ARMOND: No, it's not -- it's -- like --

12 JUDGE TORNQUIST: And this time, but I did see that it --

13 MS. ARMOND: -- to show that this is going to work.

14 JUDGE TORNQUIST: It seemed to be contradictory to something
15 you were saying.

16 MS. ARMOND: Yeah, yeah, yeah, no. So, they have the burden.
17 Their petition says Watanabe and Lee. And it's not like this is some little
18 gotcha. If you read their petition, the motivation to put these together is you
19 would put them together because Watanabe uses the high temperature
20 bonding, like that is their motivation. And then when Dr. Lee showed up at
21 his deposition, he affirmatively said that under questioning by counsel. It
22 wasn't under cross-examination, like they, they said the support of them and
23 it totally doesn't. And there's no dispute that you cannot take these devices
24 that hot without destroying them. And so, now we're seeing the pivot to
25 EMIH. And again, that's all and properly brief that. But even, even then
26 there's still, they have the burden. They still have not established any

1 amount of time you can go that hot. And the only thing I heard counsel talk
2 about this morning is they pulled up their slide and I will get the number so
3 we can all be on the same page. Hold on a second. They had a site from
4 Thompson that talks about -- slide 18, five minutes at a thousand degrees
5 Centigrade. But that is not in the record. They never talk about that. It's not
6 in the petition. It's not even in the reply. Didn't come up at the deposition.
7 That's not a record. So, they can't rely on it now for the first time this
8 morning at the hearing. So, and they also bear the burden to show that that
9 would have worked with the system we're talking about here, which is
10 Watanabe and Lee, and they have not done that.

11 JUDGE TORNQUIST: Okay.

12 MS. ARMOND: And so, for that reason this would --

13 JUDGE TORNQUIST: Well, you have two arguments here.
14 One's about the motivation to combine and like that's their burden. Would
15 you agree it's your burden, if you're trying to go all the way to show this is
16 not enabled?

17 MS. ARMOND: Yes.

18 JUDGE TORNQUIST: Okay. And when satisfying that burden,
19 what date do we look at? The date that the Patent was filed or when
20 Watanabe was filed?

21 MS. ARMOND: I'm not sure I know the answer to that off the top
22 of my head. I'd have to get back to on that one.

23 JUDGE TORNQUIST: Okay. If you can. You can go ahead and
24 move forward. Thank you.

25 JUDGE ROESEL: So, this is Judge Roesel. Before you move
26 away from the motivation to combine, I asked Petitioner's counsel for the

1 affirmative reasons why a person of ordinary skill in the art would have
2 combined these two references, and he gave me a whole list. Some of them
3 sounded unfamiliar to me, so could you respond to that list?

4 MS. ARMOND: So, we -- if you look at the petition they just say
5 there would be benefits, like it's very, very vague. And so, we did address
6 that in our briefing. But, you know, if you look at for Ground 6 the benefit
7 was the high temperature bonding. So, I honestly can't remember exactly
8 what counsel said today about this, but, you know, it's not in his petition, so
9 we can't be making arguments for him that he didn't make at the get go
10 under Magnum Oil, and the motivation in the petition was we want to put
11 these together because of the high temperature bonding because, you know,
12 of course for some reason the theory was taking this ultra dense very specific
13 we, NOR array with the shared control gates, you know, that was all about
14 very, very tight memory cells that were like four to one. Yeah, we would
15 suddenly want to make that be a stacking which is of course a much less
16 dense fabrication method. I mean it doesn't make any sense to me, but, you
17 know, but that was the motivation in the petition. And as we've explained in
18 the briefing, there's no reason to do that. So, okay. So, do we have any
19 more questions about thermal budget -- (INAUDIBLE 00:46:03).

20 JUDGE TORNQUIST: I just have one comment. Your volume is
21 going down and up as you kind of move away. Just to make sure that the
22 court reporter can hear you fully and you can just check it. As you go if you
23 can make sure.

24 MS. ARMOND: My microphone might have moved. Can you
25 hear me?

26 JUDGE TORNQUIST: I can.

1 MS. ARMOND: Okay. All right. Usually I'm like a loud talker
2 and it's not hard to hear. Okay. Let's talk about the alignment. Okay. So,
3 on alignment counsel was talking about well, you know, it would have been
4 obvious to do alignment because you could have used these mark bumps or
5 like mechanical optical alignment techniques. Okay. So, again Micron
6 bears the burden to show that again somebody would have taken leave with
7 its own, you know, monolithic structure with these intertwined and used the
8 stacking method where instead of depositing the layers up, you're like
9 literally wiring transistors like layer to layer which is very precise. So,
10 alignment is a very, very significant issue in semiconductor manufacturing,
11 and they don't show any reason why you would depart from this -- the
12 method that Lee teaches which worked for him and then go down and start
13 using different layers and wiring. So, again they haven't met their burden,
14 there's no showing that one would have just gone from this ultra dense
15 technique to something a lot less, you know, with the stacking tolerances
16 you need just a lot more, you know, as a general matter you need greater
17 tolerances and you're going to end up with a less dense device. So, they're
18 pointing to these two techniques, one was the optical and one was the
19 mechanical. But the problem with that is that's what our Patent said to do.
20 So, you can't use that as your motivation to combine because now you're
21 using the '702 Patent as a roadmap, and they don't show any, you know,
22 anything beyond that. And then if you look at the two references they cite
23 belatedly on reply very late in the game, you'll notice that, you know, these
24 have very large tolerances. We're around about 5,000, 2,000 to 5,000
25 nanometers, and I'm talking about their Exhibits 1054 and 1055 which they
26 improperly brought on reply. Well, their own expert, Dr. Lee, said that, you

1 know, the average feature size which is a transistor back at the time of the
2 Patent 2003, that would have been like 90 nanometers. So, why are you
3 going to take a 90 nanometer, you know, array of memory cells, and
4 suddenly introduce like tolerances of like plus or minus like 5,000
5 nanometers. Like why would you want your array spaced out that much? It
6 makes no sense. So, again it was on them, it was incumbent on them on this
7 important issue to show that when they depart from Lee and it's technique to
8 go to this more primitive 1992 stacking technique that you're going to be
9 able to align these stacked layers and they don't do it.

10 The other argument I heard is they were criticizing our expert Dr.
11 Przybylski pointed out that there's a very specific arrangement here and it
12 would be -- be difficult to stack in his declaration. And they said, well, we
13 don't rely on that. We're relying on other things. Well, again, you can't use
14 your hindsight and pick the parts of leave that you like and then discard the
15 parts that are inconvenient because they undo your combination. So, that's
16 what I have on alignment. Any questions, or we can move on to NAND and
17 NOR. NOR to NAND. Okay.

18 JUDGE TORNQUIST: You can move on. I just have one
19 question.

20 MS. ARMOND: Yes.

21 JUDGE TORNQUIST: For stackable add-on layer, you said our
22 construction was wrong, but you didn't say why. So, would you contest? I
23 mean, is there any reason that we should change our construction from what
24 we had a DI?

25 MS. ARMOND: Well, as we said in our briefing, we have not
26 offered a construction of stackable add-on layer. And we don't believe that

1 the Board even needs to go there to resolve this. Like stackable add-on layer
2 only is an issue for Grounds 3 and 4, which are the Lee only grounds. And,
3 you know, we have other reasons that we put forward in our briefing,
4 including, you know, there are missing limitations. You know, the -- so the
5 fundamental problem here is that Micron bears the burden, right? And so,
6 part of their burden is they need to set forth claim constructions of terms that
7 they have good reason to know might be disputed in the petition. And then
8 they need to show that they're, you know, satisfied by the prior art. And
9 here, Micron like drops footnotes in its petition and says, there's something
10 wonky going on here, but they don't provide construction. And so, they
11 leave the Board to just sort of try to deal with this, okay? So, that doesn't
12 meet their burden. And they're expert said that construction is wrong. He
13 doesn't agree with it. So, they haven't met their burden on that ground. I
14 think it can just be dispatched and the Board doesn't need to construe it. So,
15 that's where we are. And then we have this whole other thing, which sort of
16 showed up on the motion to strike, which is that, you know, now on reply,
17 Micron is presenting all of these arguments about claim construction for the
18 first time. Well, we didn't provide, and we have not provided a construction.
19 You can't do that. Like it's not responsive. Like they're not responding to us
20 because these things didn't put forward a construction, and they're not
21 responding to you, the Board, because you agreed essentially with their
22 construction. So, all of this stuff and trying to do claim construction at the
23 last minute is, it's just like way outside the proper scope of reply, especially
24 in an expedited hearing like this. So, that's what I have on that.

25 JUDGE TORNQUIST: Okay. So, if we started addressing
26 claim -- or Ground 3, we disagree with Patent Owner, but we get to the end,

1 now we have to construe it, correct? We have to construe stackable add-on
2 layer.

3 MS. ARMOND: If you disagree with our arguments?

4 JUDGE TORNQUIST: You said you have -- we don't need to
5 address stackable add-on layer for Grounds 3 and 4 because you have other
6 arguments about those grounds.

7 MS. ARMOND: Yes.

8 JUDGE TORNQUIST: What if we disagree with you, and now we
9 get to that point in the write-up? What do we do? Do we have to -- and
10 you're saying we're wrong, we need to get it right. The Federal Circuit says
11 we have to get it right as a matter of law. So, what do we do?

12 MS. ARMOND: Well, you have to construe it, obviously, if
13 there's a dispute and you need to, but you only need to construe terms
14 enough to resolve the dispute. And here, they didn't meet their burden.
15 They were supposed to put the claim construction in. They didn't do it.
16 Instead, they offer an expert opinion based on the claim construction they
17 don't even agree with. Like they're done. And then, you know, there's a
18 whole bunch of other stuff like, you know, there's no, even under
19 construction, there's no SOI pillar. So, I mean, look, you guys need to do
20 what you got to do. But we don't think you need to construe this. It only
21 relates to one ground where they haven't met their burden in any way.

22 JUDGE TORNQUIST: Okay. Thank you.

23 MS. ARMOND: Okay. So, let's talk about Lee and Watanabe.
24 That was another topic counsel addressed. So, the petition said that, and this
25 is, this impacts both Grounds 6, which is the Lee Watanabe ground that
26 we're talking about, as well as the Lee Endoh combination in Ground 4.

1 And actually, let me just step back a second, Your Honor. But you bring up
2 a good point. Like if you noticed counsel did not actually provide any
3 substantive argument on, you know, Grounds 3 and 4, which are the Lee
4 only grounds. I don't really even feel like they're in play. They're not even
5 defending them at this point. So again, I think that's just another indication
6 that even Petitioner acknowledges they have not met their burden on those
7 grounds. So, again, I don't think claim construction is necessary.

8 But anyway, let's, let's talk about NAND and NOR. So, really this
9 comes in for Ground 6. But if you do want to go there for Ground 4, you
10 can too, because it equally applies. So, the original petition said that one of
11 skill would take Lee, which is an undisputed a NOR memory array, and
12 switch it up to NAND. So, Micron is not seriously disputing that this is a
13 big deal. Like this isn't just swap out the memory cell. You're making a
14 fundamentally new device and there is no motivation to do that. They have
15 not met their burden. So, our expert Dr. Przybylski has a very long
16 discussion about all the things that you would need to do to do this. Okay,
17 which is you would need to use different chip architectures, the data flow
18 would change. The read rights or protocols are different. The control
19 circuitry is different. And you don't have to believe me, you can just
20 literally look at Micron's slide 20 that they just showed you. If you look
21 there's a figure on there from a Toshiba reference and Exhibit 1025. And
22 this is like contrasting different features of NOR and NAND. These are
23 really different chip designs. So, there is no dispute that one of skill would
24 not have had a motivation to redesign Lee into this completely different
25 architecture, particularly when Lee has this very specific, you know, dense
26 design where they're sharing control gates between levels like, so. And the

1 other thing that kind of tells you there's a problem there is we asked Micron's
2 expert at the deposition, well, how do you do this? And he could not. So, if
3 their own expert can't do this, then it's a lot to ask from a person of ordinary
4 skill in the art. So, the fact -- counsel said there's two obvious alternatives.
5 So, why wouldn't you just do the other one? Well, there's a lot. And Dr.
6 Przybylski pointed this out in his declaration. And if you look at Dr. Lee's
7 declaration, all he said was, oh, I disagree. Like it's a one sentence, like I
8 don't think this would be a problem. So, you know, again, they have not met
9 their burden to show this fundamentally different change. This stuff is
10 really, really complicated. Chip design, you know, you have to come up
11 with the design. You have to lay it out and then you have to figure out how
12 to manufacture it. It's all intertwined. And so, when you do what Micron
13 does and you're just using hindsight and you're picking and choosing
14 different features and then waving your magic wand, it doesn't -- it's not that
15 simple. Like when you change one thing, it can screw everything else up.
16 Like, you know, you can't just swap out a memory cell. You can't just bond
17 something at whatever temperature you feel about. You have to think
18 through this whole process and they have not met their burden on these
19 grounds for many, many different reasons.

20 Okay. So, lastly I'm going to end kind of where counsel started,
21 which is on the claim construction. So, we already talked about stackable
22 add-on layer. So, let's talk a little bit about SOI pillar. Now, again, that
23 term only is in dispute for like one ground. It's only coming into play on
24 Ground 2, which is the Watanabe Endoh ground. So, the meaning of SOI is
25 not disputed and counsel agree. SOI means silicon on insulator. So, the
26 question is, what is pillar mean? And the intrinsic and extrinsic evidence all

1 support that a pillar is a structure that is taller than it is wide. So, not only if
2 you look at the '702 Patent, you know, you look at the -- the various figures,
3 they're Figure 4, 20, 27, they're all showing SOI pillars taller than they are
4 wide. And counsel said that what we're trying to do is like take
5 measurements from or, you know, rely on measurements from Patent
6 figures. We are not taking out like our ruler and trying to measure
7 something here. But you know, the Patent actually does talk about what the
8 shape is. If you look at the description for Figure 20, and so I'm going to
9 turn to the Patent here, it's at column 9. So, column 9, and I am looking, this
10 is Exhibit 1001, but it's '702 pattern at 49. So, if you look around lines 14, it
11 says, it's talking about Figure 20, it says, in this embodiment of the present
12 invention, the two thyristor type estrums are stacked in vertical, the
13 direction, there's a little grammar issue there, and a bit line is shared in the
14 middle of the SOI pillar. Okay. And then the Patent says, one drawback of
15 the structure in Figure 20 is its high aspect ratio, which may cause toppling
16 during processing. So, we're not relying on the figures, the figures are
17 illustrating this thing in the Patent. It's all complimentary that we're talking
18 about a columnar structure, something that is taller than it is wide. And at
19 Dr. Lee's deposition, the second time around, you know, he agreed that a one
20 of skill, looking at Figure 20, could safely assume that its height is greater
21 than its width. And that is at, in his depot transcript, Exhibit 2052, page 56,
22 lines 1 through 16. So, we don't have any dispute here about what SOI pillar
23 means. And all of this stuff about like dope stack and whatever, you know,
24 they are kind of going through the Patent specification and doing what the
25 Federal Circuit has said we shouldn't do, which is like grabbing words that
26 they like, but they're principally grabbing like lines from the description of a

1 SOI layer. Well, an SOI layer is not our claim term here, our claim term is
2 SOI pillar. And if we're going to give effect to pillar, the undisputed
3 evidence is -- is a pillar does need to be a structure that is taller than it is
4 wide.

5 JUDGE ROESEL: Counsel, this is Judge Roesel. Can I interrupt
6 you there? How does Patent Owner respond to Petitioner's argument that
7 Patent Owner is relying on the wrong definition of aspect ratio, width over
8 height versus height over width?

9 MS. ARMOND: Oh, so that to me seems like kind of confusing in
10 view of that and just like a red herring and view of what we just read. Like
11 the Patent is clear, whether you look at a, like a dictionary or not, like they're
12 talking about the toppling. So, we are talking about something taller than it
13 is wide. And that was what the Patent was drawing and trying to convey.

14 So, you know, in terms of the motion to strike, this reply brief was
15 an entirely new petition. And so, we're not just, you know, this isn't
16 responsive. They're coming back with brand new combinations. The new
17 Thompson references, reordering. Basically, instead of responding to our
18 arguments, retracting their expert, revising the petition, all the stuff that is
19 not allowed under the Board rules. So, you know, if you have questions
20 about that, I'm happy to answer it, but that is why we moved to strike, and I
21 think our papers are pretty clear on that. So, if you have any more questions.

22 JUDGE TORNQUIST: Yes. I have a question on a couple, at
23 least a couple of these on the motion to strike. We actually asked them to
24 provide some things. Would it be strange for them not to do so? How can
25 we strike something we asked for?

26 MS. ARMOND: Well, as I recall the Board only asked for some

1 input on the claims constructions that my friend did not provide. But again,
2 the -- for stackable add on layer the Board adopted stuff, you know,
3 basically what Micron wanted. So, there was nothing for them to respond to
4 there. And we didn't respond to it, so there was nothing to respond to at all.
5 On SOI pillar like we did respond and they responded and we're not, you
6 know, we don't have a beef with that. But like, again, there's an order to this
7 and, you know, inviting parties to develop the record. Like, it would be a
8 different story if we had provided a claim construction, but we didn't. And
9 so, there was nothing to respond to. It's outside the proper scope of reply,
10 and, you know, the rules are really clear about that. And under the Tunik
11 case, which we cite in our case, we can't have like a special rule for just this
12 IPR like, you know, that, you know, there's the APA, there are the rules
13 there, you know, like what they did was out of bounds.

14 JUDGE TORNQUIST: Okay. So, the other question is, Patents
15 are presumed enabled. I mean, I don't understand why they would have put
16 in the electromagnetic induction heating or the alignment issues response
17 until you made those arguments.

18 MS. ARMOND: So again, on the EMIH, their motivation to
19 combine was the temperature, right? It's the high temperature bonding. So,
20 if they had some like fancy way that they wanted Watanabe to work, that
21 should have been in their petition. So, now they're coming back and instead
22 of trying to enable Watanabe, they actually have an entirely new
23 combination, which is Lee, Watanabe, but don't do Watanabe says and
24 instead microwave it to 900 degrees Celsius. Like that's a new combination.
25 So --

26 JUDGE TORNQUIST: Does Watanabe say exactly how it's

1 heating to 900 to 1,000?

2 MS. ARMOND: It says just high temperature bond at those
3 temperatures.

4 JUDGE TORNQUIST: Right. So, it doesn't say what method they
5 were using?

6 MS. ARMOND: I don't think it does. But remember, Thompson's,
7 this is a graduate student, like he didn't come around with his graduate
8 research till 10 years later. So, I don't really think that Watanabe or what a
9 skill would understand that Watanabe was talking about. Mr. Thompson's
10 graduate research that hadn't been invented until 10 years later.

11 JUDGE TORNQUIST: Okay.

12 MS. ARMOND: Like, you know, and again, however you get to
13 1,000 degrees, it's still real. I mean these temperatures are really hot, like
14 1,000 degrees Celsius, like that's where you start melting copper and bronze,
15 right, like I can see maybe I can put my finger on something that's like 40
16 degrees Celsius for a little bit and not getting burned. Like I can't imagine
17 any amount of time you would touch something that's 1,000 degrees Celsius
18 that would like melt your entire finger off. Like, this is really hot and it was
19 a big problem and it was an obvious problem. And, you know, this is kind
20 of a silly combination. So again, it's a -- the claims can be confirmed over
21 almost all of this, 1, 2, 5, and 6 for that reason alone.

22 JUDGE TORNQUIST: Okay.

23 MS. ARMOND: I will cede the rest of my time unless you have a
24 question.

25 JUDGE ROESEL: Before you go on counsel, I wonder if Patent
26 Owner could please respond to Petitioner's argument based on Petitioner's

1 slide 26 about combining the Figure 7 and Figure 2A of Watanabe. They're
2 trying to, I think, respond to what the institution decision said about non-
3 volatile memory, and whether Watanabe taught these particular stacked
4 structures for a non-volatile memory.

5 MS. ARMOND: Okay. Thank you for bringing that up because I
6 actually did mean to address that and I had almost forgot. So, let's, yes, let's
7 talk about that. So, if you look at Watanabe's Figure 2 which is the DRAM
8 embodiment, pull that up. So, Figure 2A is this, you know, it's volatile
9 memory. And so, they are actually using if you look at the one, hold on a
10 second, let me get my numbers right here. So, they're using a capacitive
11 type memory, you know, Watanabe is like not a very dense memory, and we
12 explain this in our papers. So, you know, that's one type of memory cell
13 where you're using your storing charge in kind of a capacitor between plates.
14 But if you look at Figure 7 of Watanabe, they're doing something different
15 there. They're actually using a transistor. So, you can see in the description,
16 you have a source, a gate, and a drain. And they're storing the charge not in
17 the capacitor, but in the transistor, the switch. So, porting this SRAM
18 configuration back into a transistor base, that's a fundamentally different
19 architecture. And if you look at the petition, Micron never addresses that.
20 They never grapple with that at all. So, you know, again, it was an
21 afterthought. There's no motivation to combine to put these two different
22 configurations together. It's kind of a similar situation to what we saw with
23 like Lee and Endoh, where you can't just like swap something out. And they
24 don't provide a motivation. They don't meet their burden on that either.

25 JUDGE TORNQUIST: Okay. Seeing no further questions, we
26 will move to rebuttal time from Petitioner.

1 MR. KAPPOS: Thank you, Your Honors. Let me start with the
2 term stackable add-on layer. It must be construed and counsel took the
3 position that Grounds 3 and 4 are not in play. They absolutely are in play.
4 In fact, we've met our burden to show that the claims are unPatentable in
5 Grounds 3 and 4, and Patent Owner gives no reason why Lee 994 does not
6 invalidate Claim 13 under a construction that would allow for a sequential
7 deposition. So, our view is that it is unassailably the case that those grounds
8 are in play and they've gone essentially unrebutted in this proceeding.

9 JUDGE TORNQUIST: I'm confused by that. What do you want
10 us to do if the claim construction is a stackable add-on layer? That it can't
11 be sequential and Lee is clearly sequential?

12 MR. KAPPOS: Well, in that case, then the Grounds 3 and 4 are
13 overcome and we would go back to 1, 2, 5 and 6, right, which are the ones
14 that we discussed. The point that I'm raising is that under a broad
15 construction, 3 and 4 still are in play. We don't think that construction is
16 correct, but we do believe that the claim term needs to be construed at this
17 point. It wasn't construed initially because our view was the prior art met
18 the term under any construction, and we were aware that Patent Owner had a
19 different construction. But the way the record has now evolved, the claims
20 would be unPatentable if the term were construed more broadly than to
21 require that the layer, or that the structure be formed separately.

22 JUDGE TORNQUIST: Okay. I understand.

23 MR. KAPPOS: Your Honor asked a question about Watanabe and
24 where we have addressed the substrate issue in Watanabe. And so, I wanted
25 to give you, Your Honor, a reference to that. It is discussed in Exhibit 1002,
26 which is expert Lee's opening declaration in paragraph 71. Okay, there was

1 a --

2 JUDGE TORNQUIST: I'm sorry, I wasn't -- I hit the mute thing.
3 Anywhere in your briefing besides the expert report?

4 MR. KAPPOS: Well, I believe that the briefing refers to those
5 paragraphs, but I would need to go back and find exactly where that is.

6 JUDGE TORNQUIST: We can double check. I appreciate at least
7 having that cite.

8 MR. KAPPOS: Okay. A question was raised about the definition
9 of aspect ratio, and I just wanted to clarify that Dr. Przybylski had the
10 definition wrong. In fact, in his declaration, he states that with reference to
11 Figure 4, that it has a small aspect ratio given its larger height relative to its
12 width. That statement would only make sense if aspect ratio were defined as
13 width over height. It's exactly the opposite. Aspect ratio in this context
14 means height over width. And we know that the '702 Patent uses the height
15 over width definition because with reference to Figure 20, the toppling issue,
16 the Patent says you risk toppling with high aspect ratio.

17 Patent Owner's counsel argued that Figure 20 in the '702 Patent
18 supports its construction because it shows a pillar that is taller than it is
19 wide. But if we just look at the description it says that that type of a
20 structure is disfavored because of the risk of toppling. So, Patent Owner's
21 construction would effectively exclude all or most of the embodiments of the
22 '702 Patent except for Figure 20 which is said to be disadvantageous.

23 There was discussion of motivation to combine Lee in view of
24 Watanabe and it is very much in the petition the basis that I discussed in the
25 earlier session, and it has nothing to do with an increase -- with doing high
26 temperature bonding. That was not the motivation to combine. The

1 motivation is to improve integration density by stacking. That's discussed in
2 paper one, the petition at page 70. It's also discussed in Watanabe, Exhibit
3 1005, which is in the record. It's also discussed in the Lee declaration,
4 Exhibit 1002. I'm providing the cites because I believe that there may have
5 been a statement earlier that these were not found in the record. And so, I'm
6 just giving you where they are in the record. The second --

7 JUDGE ROESEL: Counsel, on that point, this is Judge Roesel. I
8 heard Patent Owner argued the stacked method produces a less dense
9 structure than the monolithic or sequentially deposited structure. Is there
10 anything from Petitioner in the record to dispute that?

11 MR. KAPPOS: Yes. The cites that I just read a moment ago are
12 expert Lee testifying that the stacking method can improve the density of the
13 stacking, the integration density.

14 JUDGE TORNQUIST: But that's over a different type of chip,
15 right? Isn't your argument that Lee and Watanabe both increase integration
16 density, and therefore they're equivalent? But they're alternatives?

17 MR. KAPPOS: They are alternatives, and they would increase
18 integration density as compared with two dimensional memory. But there's
19 testimony in the record indicating that the stacking method improves
20 integration density over sequential deposition. And those were the cites that
21 I was just reading a moment ago. Watanabe teaches that wiring alignment
22 with electronic components is improved by stacking. That's in expert Lee's
23 first declaration, Exhibit 1002 at paragraph 146. Watanabe teaches that
24 stacking reduces interconnection wire resistance. That was in expert Lee's
25 declaration, first declaration, at paragraph 149. And the fact that stacking
26 allows for the use of monocrystalline silicon, that was discussed in expert

1 Lee's deposition, which is Exhibit 202A at page 141 to 142. And it was also
2 referred to in paper 20, Petitioner's reply at page 6.

3 We do very much dispute the proposition that transistors cannot go
4 above 650. As I explained earlier, the deposition testimony from expert Lee
5 was almost immediately clarified in the same line of questioning where he
6 said that thermal budget is temperature times time. And all the experts agree
7 that that is in fact the case. Expert Lee also testified that high temperature
8 processes even up to 900 to 1,000 Centigrade for a short time may have less
9 thermal effect than low temperature processes. And I'd like to show that
10 discussion from him. This is in his expert report at paragraph 39. This was
11 Exhibit 1041. It is important to note that high temperature processes, e.g.,
12 900 to 1,000 Centigrade for a short time, may have less thermal effect than
13 low temperature processes.

14 JUDGE TORNQUIST: So, counsel, this is Judge Tornquist. Is
15 there evidence of how long you needed to bring it up to 1,000 degrees to
16 bond Watanabe's layers, and that that time would not cause damage to the
17 materials on the wafer?

18 MR. KAPPOS: There's no evidence in Watanabe about that
19 because Watanabe was leaving all that, those choices to the person of skill in
20 the art. But the Thompson dissertation and abstract is very much in the
21 record here. And in Thompson, they say that they were able to accomplish
22 wafer bonding at five minutes at 1,000 degrees Centigrade. So, Thompson
23 also gives, you know, he mentions that hours long anneals are required for
24 conventional heating techniques, so his improvement is shortening that time.

25 JUDGE TORNQUIST: And the wafers that he was bonding, did
26 they have transistors on them and electrical devices, memory, et cetera?

1 MR. KAPPOS: That's -- that's unclear, but there was definitely
2 metal involved in the process. So, this argument that you can't use the type
3 of radiation that Thompson was using without causing, you know, sparking
4 or a meltdown is incorrect. The dissertation plainly says, first of all that you
5 can use RF energy which is not microwave, and then they also talk about
6 having something called a seceptor, which is made out of metal in the
7 process. I wanted to show you the part that I was referring to from the
8 Thompson dissertation here, which is in the record and says, EMIH was
9 applied to silicon-silicon and silicon-silicon dioxide bonding to illustrate that
10 rapid bonding of silicon wafers is possible. Full-strength, void-free silicon-
11 silicon bonds were achieved in five minutes at a 1,000 degrees. So, EMIH,
12 there's no question that it was applied to this type of bonding. And if you
13 step back and think about it for a minute, this is the entire point of
14 Thompson's Ph.D. work, was to do wafer bonding. So, it's nonsense to say
15 you can't use Thompson's EMIH technique to bond Watanabe's silicon
16 wafers.

17 JUDGE ROESEL: Counsel, this is Judge Roesel. So, Petitioner
18 agrees the person of ordinary skill in the art would not have combined
19 Watanabe with the other reference without first modifying Watanabe in view
20 of the Thompson teaching about EMIH. Is that right?

21 MR. KAPPOS: I'm sorry, that was directed to me as a
22 characterization of Patent Owner's argument?

23 JUDGE ROESEL: No, no. The question is whether Petitioner
24 agrees that the person of ordinary skill in the art would not have combined
25 Lee and Watanabe without first modifying Watanabe in view of Thompson's
26 teaching of EMIH.

1 MR. KAPPOS: I think the right way to look at it is a person
2 skilled in the art would know, depending on how many wafer bonding steps
3 they wanted to do, whether or not modifications needed to be made. So,
4 yeah, we would agree that there were modifications that we submit were
5 well within the skill of the art that would need be made if you were going to
6 do stacking of many, many layers. But again, there's no requirement in the
7 claims for that. And so, this is the thermal budget, which is temperature
8 times time, is going to necessarily be dependent on the number of bonding
9 steps. And it's something that a person skilled in the art would have known
10 how to modify.

11 And again, I'd like to just remind the tribunal here that bodily
12 incorporation is not the test, right? There are cases *Allied Erecting v.*
13 *Genesis*, being one, where the Federal Circuit has said, it's not necessary that
14 the references be physically combinable to render obvious the Patent. The
15 criterion is whether the claimed subject matter is rendered obvious by the
16 teachings of the prior art as a whole.

17 I'd like to move on to the points that were made about alignment.
18 Our view is that we have fully met the burden to show that a person skilled
19 in the art would have known how to do alignment. Petitioner's reliance on
20 the knowledge of a person skilled in the art is not, by any means, hindsight
21 reconstruction using the Patent. We're relying on well-known techniques
22 that were used by persons skilled in the art during the relevant timeframe to
23 accomplish alignment. Now, Patent Owner has questioned whether the
24 alignment could be performed to a sufficient level of accuracy, but the
25 alignment that's needed is alignment for the stackable add-on layers. It's not
26 at the feature size level, right? And so, in the back end of line, the contacts

1 that you're trying to align are more like four to six microns. So, that would
2 be 4,000 to 6,000 nanometers. This is definitely within the level of precision
3 that the Niklaus and Smith references deal with. And I'd also like to note
4 that for the optical alignment, which is the Smith reference shown on the
5 right, if you can etch the feature size to within 90 nanometers, then you can
6 certainly etch the alignment grooves to Smith -- in Smith to the same level
7 of accuracy because both of these use the same etching and lithography
8 techniques.

9 Okay. There was discussion about the interleaved embodiment in
10 the Lee reference, and as I noted initially, this is attorney argument and our
11 petition does not rely on the Lee 994's Figures 26 or 27. I would also note
12 that the challenged claims in the '702 Patent do not require interleave
13 structures, and Lee 994 does not require that its structure be interleaved. In
14 the Lee 994, the figures that Patent Owner focuses on are the end of a
15 sequence that starts at Figure 13, Figures 13 to 27 describing one possible
16 manufacturing process. And the way that that sequence of figures is
17 introduced is shown on this evidence, Exhibit 1007 at column 20 near the
18 bottom, which states that this is a method for making pillar memory devices.
19 The statement doesn't say that it's the only method or the exclusive method.
20 And so, Lee leaves open the possibility that a person skilled in the art would
21 employ other known methods, such as Watanabe's stacking method, where
22 the vertical memory cells are not interleaved but connected as per
23 Watanabe's wiring method.

24 There was discussion about motivation to implement Lee's
25 memory cells in NAND architecture. And the rationale that was provided,
26 there absolutely is a motivation to do so and it is stated in Petitioner's papers

1 that NAND facilitates high integration density. This is discussed in paper
2 one at page 73. It was also addressed and expert Lee's first declaration,
3 Exhibit 1002 at paragraph 136. And what expert Lee said is that NAND
4 increases the integration density of a memory design by reducing the number
5 of contacts per memory cell and thus reducing the chip area per memory
6 cell. So, motivation to combine was absolutely dealt with in the papers as
7 initially filed. Expert Lee testified that a person skilled in the art would have
8 known how to arrange the Lee 994 memory cells in series within NAND
9 flash architecture by omitting the insulators. So, let me go to slide 23 again.
10 Yeah, and what expert Lee explained here is that whether or not the hash
11 regions are insulators or conductors, he took it both ways and explained that
12 it was -- it would have been easy for a person skilled in the art to arrange
13 Lee's memory cells in series within NAND flash architecture by omitting the
14 insulators and incorporating control gates. That's the option on the left, or if
15 the hash regions are conductors, keeping those regions which connect the
16 transistors in series and incorporating control gates. Counsel for Patent
17 Owner referred to I think what the paper is characterized as a cascading set
18 of modifications that are needed to convert NOR to NAND. Various
19 changes including redesigning pillars, replacing control gates, creating new
20 routing paths. None of those changes need to be made if you know you're
21 going into NAND architecture because the NAND architecture as explained
22 by Endoh, met all of those requirements. So, again the memory cells of Lee
23 and Watanabe, they can be dropped in to any architecture. The architecture
24 is just the wiring, it's the schematic. You don't need to do this complete
25 redesign that Patent Owner submits that you would need to make.

26 And with that I will ask Mr. Reinbold to respond to the points

1 about the motion to strike. Patric, are you on mute?

2 MR. REINBOLD: I think I just unmuted. Hopefully, you can hear
3 me now. So, all of the -- all of the evidence and arguments that Petitioner
4 presented were properly responsive to arguments either as the Board noted
5 raised by the Board itself or Patent Owner, and the Petitioner didn't revise
6 any of the grounds as Patent Owner contends. In fact, all of the grounds as
7 discussed here today remain the same. Rather, Petitioner was merely
8 responding to arguments that Patent Owner raised about enabling the prior
9 art references and other extrinsic evidence that Patent Owner raised. In
10 addition, Petitioner doesn't recant any of Dr. Lee's testimony as presented
11 previously. Each of the exhibits and the portions of the reply brief were
12 responding to those arguments or raised previously.

13 If the Board has any specific questions about any of the additional
14 motions to strike, including the specific evidence challenged, I'd be happy to
15 answer those.

16 MR. KAPPOS: And can I just add, Judge Roesel, you had asked
17 where is paragraph 71 of the Lee Declaration, Exhibit 102, where is that
18 cited in the papers? That is in our petition at pages 14 to 15.

19 JUDGE TORNQUIST: Okay. I don't see any other further
20 questions. So, thank you, Petitioner. Now, we'll hear from Patent Owner
21 and their sur-rebuttal.

22 MS. ARMOND: Thank you, Your Honor. To answer the question
23 you asked me the last round about what date do we determine enablement of
24 a reference. There is the Raytheon v. GE case that's cited, I think, in both
25 parties papers and that suggests that you evaluate enablement at the time of
26 the invention. So, in this case, it would be around 2003, and the pin site for

1 that would be 993 F.3d at 1376 if you need that.

2 JUDGE TORNQUIST: Okay. So, that allows us then to look at
3 the Thompson references and what they would provide to one of skill in the
4 art at that time?

5 MS. ARMOND: Well, no, because, again, that should have been
6 in the petition. And second of all, they need to show a motivation to modify
7 Watanabe. And again, on this record, they haven't shown that one of skill
8 would have departed from Watanabe and gone to this Ph.D. student's
9 research about microwaving wafers like they needed to do that. And they
10 still didn't do it even on reply. So, they need to show a motivation for this
11 new combination that they made that's not in their petition and they're not
12 allowed to make at this point. So, there's a lot of --

13 JUDGE TORNQUIST: Can I -- it's sort of two questions. One is
14 the motivation and one is the enablement of the reference?

15 MS. ARMOND: Correct. Yes. Yes, exactly.

16 JUDGE TORNQUIST: Okay. Thank you.

17 MS. ARMOND: So, but again, that's not in the petition. So, like,
18 you know, anyway. So, counsel said that it is unrebutted that Lee alone
19 invalidates Claim 13. So, that's based on the claim construction of stackable
20 add-on layer that no one is advocating. Counsel isn't advocating that; we're
21 not advocating that here. No one's advocating that in District Court. That
22 case is stayed. So, that one didn't make a lot of sense to me. So -- okay. So,
23 I heard an argument from counsel about how the stacking methods somehow
24 improves integration density. That's a new one to me. I think that one may
25 have just showed up here at the hearing. Again, that is not in the petition.
26 And, you know, you can't change now like it's -- it's kind of too late to be

1 offering this like live right here.

2 Let's talk about thermal budget again. I still have not heard a safe
3 time that one can subject the transistors and Lee and Watanabe to 1,000
4 degrees Celsius, especially when that, you know, all of the experts agree you
5 can't go over 650. You know, these BESANG's own Patent says don't go
6 over 650. This is just a bad idea. And the one thing that counsel points to,
7 and I am going to share my screen here. So, oh, I'm sharing my whole
8 screen. Oh, my God, what a bad idea. Let's try that again. I'm just trying to
9 share the screen. All right. Okay. Can you see the slide now? So, I am at
10 slide 18 of Petitioner slides, so not my slides, Petitioner's slides. So, they
11 have these two cites that they're pulling out of a more than 100 page
12 dissertation of Thompson. Again, this is not in the record, like they did not
13 discuss this at all in their briefing. And so, pulling it out now like, you
14 know, there's no evidence to support this. So, and further, they still haven't
15 shown that what Thompson was doing with the wafers he's throwing in the
16 microwave are going to work with the Lee and Watanabe combination.

17 So, Let's move on to alignment. Again, now we have a new
18 combination for alignment, which is that one of skill would have modified
19 Watanabe to use an optical or mechanical alignment that can get somewhere
20 between 4,000 to 6,000 microns. But again, we have these like super small
21 90 nanometer feature sizes and -- and Lee and the other references. So,
22 again, this is a new combination. It's not in the petition. Watanabe is
23 entirely silent about how you align properly, which is really critical in
24 Watanabe because they are literally wiring in between like memory cells in
25 each layer. So, now we're modifying Watanabe. It again shows that the
26 Petitioner has not met the burden in the petition.

1 The next point counsel made was --

2 JUDGE ROESEL: So, before you, sorry. Before you move off
3 alignment, would you respond to the Petitioner's argument that improved
4 wiring alignment is actually a benefit that would have motivated this
5 combination? And I think they're referring to what they're quoting in the
6 petition, which talks about improving accuracy of the wiring. Is that the
7 same thing? Accuracy of the wiring and alignment?

8 MS. ARMOND: Hold on a second. Let me let me pull up what
9 you are looking at. I'm sorry, the petition at page 72?

10 JUDGE ROESEL: The petition at page 72, and they're quoting
11 from Watanabe column 6.

12 MS. ARMOND: Okay. Give me one sec. So, this is all -- so this
13 combination again doesn't make a lot of sense to me because if you look at
14 Watanabe, which, sorry, I'm going to pull it up, give me one second, you
15 know Watanabe, one second. I will pull up our demonstratives on this one.
16 Okay. Can you see my slide -- Patent Owner's slide 3? So, here Watanabe
17 you can see is actually forming wires here between each individual memory
18 cell, and they're talking about this method improves that. So, I'm not really
19 sure how this argument that we're hearing now at the hearing today and, you
20 know, the spin of the petition has anything to do with Lee, where they're
21 depositing the memory cells, you know, they're not individually wiring
22 them. So, I really don't understand how Watanabe's method is going to
23 improve Lee, particularly when Lee is using these specialized NOR memory
24 cells where you have a control gate that is shared, like each memory cell has
25 four control gates on it. So, it's this super dense thing. Like, you know,
26 Watanabe, this is a much more primitive structure. So, if you look Lee's

1 Figure 12B, you can see here there's that shaded vision part and I'm on
2 Patent Owner's slide 8 right now, 1200. Like that is the shared control gate
3 between all of these different, you know, it kind of surrounds it three
4 dimensionally. You can see it if you go back and you look at Figure 26 of
5 Lee, which shows that a little bit more explicitly. So, anyway, I don't see
6 how they've met their burden on using Watanabe's like memory cell by
7 memory cell thing to improve the density. You know, like, especially with
8 the tolerance of what we are talking about, which are so much bigger than
9 the memory cells.

10 Okay. So, then the -- while we're on Lee, counsel said that this
11 whole point about the fact that Lee has a unique structure and it's sharing
12 memory cells, like each memory cell is kind of like four because they have
13 these shared control gates. Like that's not a, that's attorney argument.
14 There's no support for that. It's actually not. Dr. Przybylski has a very
15 detailed declaration. And if you look at his declaration, which is Exhibit
16 2029, paragraphs 129 to 133, he talks about this structure. And it's not just
17 in these Figures 26 and 27. It's also in figure 12B, which Micron is relying
18 on. So, you know, this is a really important consideration for Lee. And
19 again, I mentioned, and now we're jumping over to the Watanabe and Lee
20 and Endoh combination. You know, again, Dr. Lee, and they're not
21 disputing this, could not tell you how to take a NOR array and make it into
22 an NAND array at the deposition. And so, now in this reply declaration,
23 which we can't, of course, respond to with our own expert, you know, he has
24 come up with a new idea. So, he's taken Figure 12B from Lee, which you
25 can see here on our Patent Owner, slide 8. And if we go back, hold on a
26 second. If we go back to Petitioner's slide, they have this new solution here.

1 I'm looking at Petitioner's slide 23. And so, first of all, and this is in our
2 briefing, but, you know, Dr. Lee has no idea how the Lee reference works.
3 So, his solutions are, I guess, take out the metal contacts, which you see
4 shaded here in the left. Like those are gone now. So, I'm not even sure how
5 this is going to work because those are the word lines and bit lines and they
6 don't work now. But, you know, he's like blowing away like the shared
7 control gate. Like, is there any explanation on why or how you would do
8 this? I mean, again, you know, I heard counsel say, you don't need to do a
9 complete redesign to make this happen. I don't even think this will work,
10 but that's what they're doing. Like they're taking out the word and bit lines
11 and yeah, that's called changing the wiring. They're like redoing the control
12 gates. Yes, you know, he said that they didn't have to do that. That's exactly
13 what they're redoing here. It's like this again shows that they have not met
14 their burden to show why any one of skill would do any of this, let alone
15 (INDISCERNIBLE).

16 And with that, I will cede my time unless you have more questions.

17 JUDGE TORNQUIST: I see no further questions. That concludes
18 our hearing for today. We thank both parties and we will take this under
19 advisement and we'll issue a decision in due course. But I'd ask the parties
20 to stay on the line in case the court reporter has any need for spellings and
21 the like while the panel will leave the call. Thank you very much.

22 MR. KAPPOS: Thank you, Your Honors.

23 COURT REPORTERS: Yes, I actually have one question for Ms.
24 Armond, counsel. There was a case you cited.

25 MS. ARMOND: Was it the Raytheon case.

26 COURT REPORTER: There was the Tunic case.

1 MS. ARMOND: Oh, T-U-N-I-K.

2 COURT REPORTER: I have T. So, I heard T at the end. Perfect.
3 And you know what, if you could please actually give me the spelling for the
4 Raytheon case as well over here.

5 MS. ARMOND: Sure. R-A-Y-T-H-E-O-N.

6 COURT REPORTER: Okay. That's what I thought, but I wanted
7 to be sure. All right. I believe that is it. I have no further clarifying
8 questions. Thank you.

9 MS. ARMOND: Thank you.

10 MR. KAPPOS: Thank you very much.

11 MS. ARMOND: Bye, everybody.

12 MR. KAPPOS: Bye.

13 COURT REPORTER: Bye.

14 (Whereupon the above-entitled matter went off the record at 2:46
15 p.m.)

IPR2023-00900
Patent 7,378,702 B2

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