

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR
PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS, LLC,
Petitioners

v.

BESANG, INC.,
Patent Owner.

Case No. IPR2023-00900
U.S. Patent No. 7,378,702

PETITIONERS' NOTICE OF APPEAL

Pursuant to 37 C.F.R. § 90.2(a) and 35 U.S.C. § 142, Petitioners Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC (“Micron” or “Petitioners”) hereby give notice that Petitioners appeal the Patent Trial and Appeal Board’s (“Board’s”) Final Written Decision, entered on November 13, 2024 (Paper No. 35) in the above-captioned *inter partes* review of United States Patent No. 7,378,702 (“the ’702 Patent”) to the United States Court of Appeals for the Federal Circuit, including all underlying orders, decisions, rulings, and opinions that are adverse to Petitioners.

For the limited purpose of providing the Director with the information requested in 37 C.F.R. § 90.2(a)(3)(ii), Petitioners’ issues on appeal may include, but are not limited to: (1) the Board’s determination of no unpatentability of Claim 13 of the ’702 Patent under 35 U.S.C. § 103 in view of Watanabe; (2) the Board’s determination of no unpatentability of Claims 14-17 of the ’702 Patent under 35 U.S.C. § 103 in view of Watanabe and Endoh; (3) the Board’s determination of no unpatentability of Claims 13-15 of the ’702 Patent under 35 U.S.C. § 103 in view of Lee and Watanabe; (4) the Board’s determination of no unpatentability of Claims 16-17 of the ’702 Patent under 35 U.S.C. § 103 in view of Lee, Watanabe, and Endoh; (5) the Board’s legal errors in undertaking its application of the Board’s rules and procedures, the application of controlling Federal Circuit precedent, and its obviousness analyses and application of the

claim language to the prior art of record; (6) the Board's findings that conflict with the evidence of record and are not supported by substantial evidence; and (7) and findings or determinations supporting or related to the aforementioned issues as well as all other issues decided adversely to Micron in any orders, decisions, rulings, phone conference decisions, and/or opinions.

Simultaneously with the submission, Petitioners are mailing a true and correct copy of this Notice of Appeal to the Director of the United States Patent and Trademark Office, and filing a true and correct copy of the same, along with the required docketing fee, with the Clerk of the United States Court of Appeals for the Federal Circuit.

Dated: December 20, 2024

Respectfully submitted,

/s/ Ben Haber

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CERTIFICATE OF SERVICE

In accordance with 37 C.F.R. § 90.2(a)(1) and § 104.2, I hereby certify that on December 20, 2024, in addition to being filed electronically through the Board's P-TACTS System, a true and correct copy of the foregoing PETITIONER'S NOTICE OF APPEAL was served by express overnight mail on the Director of the United States Patent and Trademark office, at the following address:

Director of the United States Patent and Trademark Office
c/o Office of the General Counsel
P.O. Box 1450
Alexandria, Virginia 22313-1450

CERTIFICATE OF SERVICE

I hereby certify that on December 20, 2024, a true and correct copy of the foregoing PETITIONER'S NOTICE OF APPEAL, along with a copy of the Final Written Decision, was filed electronically with the Clerk's Office of the United States Court of Appeals for the Federal Circuit, at the following address:

United States Court of Appeals for the Federal Circuit
717 Madison Place, N.W., Suite 401
Washington DC 20005

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e)(1), the undersigned certifies that on December 20, 2024, a true and correct copy of the foregoing PETITIONER’S NOTICE OF APPEAL was served via email to the Patent Owner by serving mail correspondence addresses of record as follows:

Michelle E. Armond michelle.armond@armondwilson.com ARMOND WILSON LLP 4685 MacArthur Court, Suite 390 Newport Beach, CA 92660	Douglas R. Wilson doug.wilson@armondwilson.com ARMOND WILSON LLP 13785 Research Blvd., Suite 125 Austin, TX 78750 Joseph Li josepher.li@armondwilson.com Yue Han amy.han@armondwilson.com
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Dated: December 20, 2024

Respectfully submitted,

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FINAL WRITTEN DECISION

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS, LLC,
Petitioner,

v.

BESANG INC.,
Patent Owner.

IPR2023-00900
Patent 7,378,702 B2

Before JON B. TORNQUIST, KIMBERLY McGRAW, and
ELIZABETH M. ROESEL, *Administrative Patent Judges*.

TORNQUIST, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining No Challenged Claims Unpatentable
35 U.S.C. § 318(a)
Denying-in-Part and Dismissing-in-Part
Patent Owner's Motion to Strike
37 C.F.R. § 42.71

I. INTRODUCTION

Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting an *inter partes* review of claims 13–17 of U.S. Patent No. 7,378,702 B2 (Ex. 1001, “the ’702 patent”). BeSang Inc. (“Patent Owner”) filed a Preliminary Response to the Petition. Paper 6. We instituted review with respect to all grounds and claims set forth in the Petition. Paper 9 (“Institution Decision” or “Inst. Dec.”). After institution, Patent Owner filed a Response (Paper 18, “PO Resp.”), to which Petitioner filed a Reply (Paper 20, “Pet. Reply”), and Patent Owner filed a Sur-reply (Paper 26, “Sur-reply”).

Petitioner relies, *inter alia*, upon two declarations from Dr. Jack C. Lee, Ph. D. (Ex. 1002 (original declaration); Ex. 1041 (reply declaration)), and Patent Owner relies upon a declaration from Steven A. Przybylski, Ph.D. (Ex. 2029).

Patent Owner filed a Motion to Strike (Paper 24, “Motion” or “Mot.”), to which Petitioner filed an Opposition (Paper 25, “Opp.”).

An oral hearing was held on August 22, 2024, and a transcript of the hearing is included in the record (Paper 34, “Tr.”).

For the reasons that follow, we conclude that Petitioner has not demonstrated by a preponderance of the evidence that claims 13–17 of the ’702 are unpatentable on any asserted ground set forth in the Petition.

II. BACKGROUND

A. Related Matters

The parties identify the following district court proceeding as a related matter: *BeSang Inc. v. Micron Tech., Inc.*, No. 2:23-cv-00028 (E.D. Tex.).

Pet. 1; Paper 3, 1. Patent Owner also identifies *BeSang Inc. v. Intel Corp.*, No. 3:23-cv-00113 (D. Or.) as a related matter. Paper 3, 1.

B. Real Parties in Interest

Petitioner identifies itself (the three parties identified in the caption) as the real party in interest. Pet. 1.

Patent Owner identifies itself as the real party in interest. Paper 3, 1.

C. The '702 patent

The '702 patent is titled “Vertical Memory Device Structures” and issued May 27, 2008, from an application filed September 3, 2004, which is a continuation-in-part of an application filed June 21, 2004. Ex. 1001, codes (22), (45), (54), (63).

The '702 patent explains that “integrated circuits contain transistors that are primarily implemented on a single major surface of a substrate, such as a semiconductor wafer.” Ex. 1001, 1:27–30. “These laterally oriented devices,” however, “consume significant amounts of chip area.” *Id.* at 1:30–31. The '702 patent explains that one method of reducing the lateral area consumed by the transistors was to reduce the lateral dimensions of the transistors and interconnects, but the equipment and technology needed to support the manufacture of such chips “becomes increasingly expensive with each new generation of smaller devices.” *Id.* at 1:31–39. To address this problem, the '702 patent discloses the use of “a plurality of vertically oriented semiconductor memory devices, or cells,” that “may be added to a separately fabricated substrate that includes electrical devices and/or interconnect lines.” *Id.* at 1:40–50; *see id.* at code (57) (“Vertically oriented semiconductor memory cells are added to a separately fabricated substrate that includes electrical devices and/or interconnect.”).

Figure 1 of the '702 patent is reproduced below:

Fig. 1

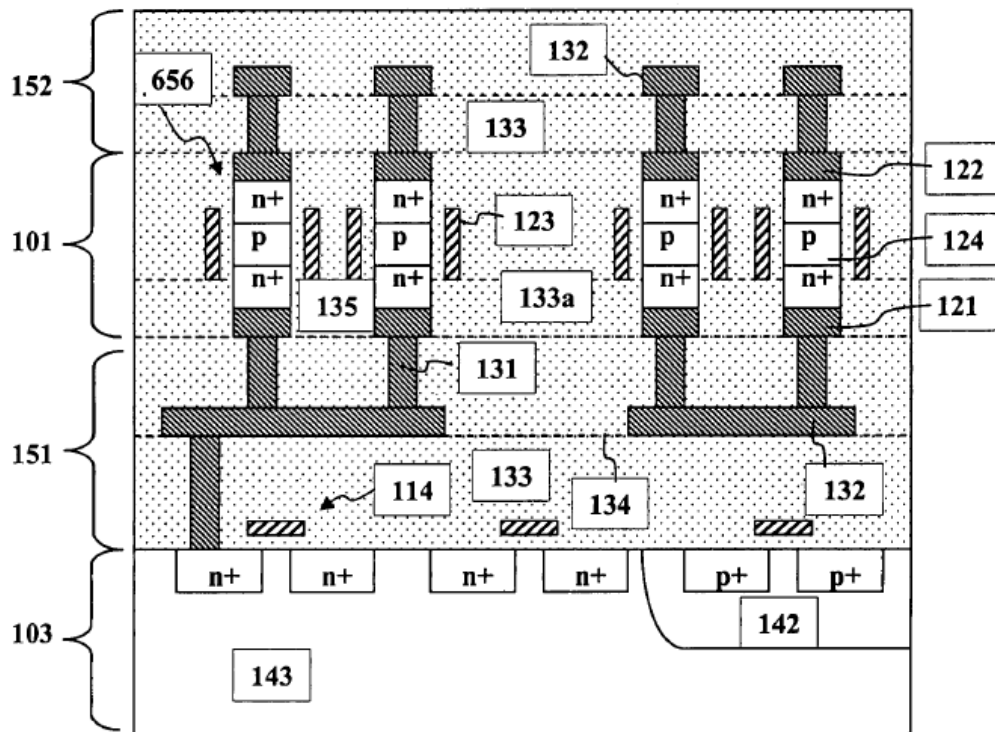


Figure 1 is a cross-sectional view of an embodiment that includes “a base semiconductor substrate and add-on vertical memory devices.” Ex. 1001, 2:13–15. As shown in Figure 1, vertical memory devices 656 are separated by isolation 135 and have floating structures in filled dielectric materials 133a. *Id.* at 5:18–21. These vertical memory devices are referred to in the '702 patent as floating devices (FLD). *Id.* at 5:21–22. Inter-layer dielectric (ILD) layers 133 are disposed above and below FLD layer 101. *Id.* at 5:29–32. Interconnect lines 132 and vias 131 connect FLDs directly or indirectly within an FLD layer, or to another FLD layer, or to a base substrate. *Id.* at 5:32–36.

In the embodiment shown in Figure 1, base substrate 103 is bonded to lower dielectric layer 151. Ex. 1001, 5:37–38. Dashed line 134 denotes a border, or interface, between two ILD layers. *Id.* at 5:43–44. First ILD layer 151 has interconnections and vias, and base substrate 103 shares these interconnections and vias with first FLD layer 101. *Id.* at 5:44–47. The bottom of the FLD layer is connected to metal layer 121, which is also directly connected to vias 131 in ILD layer 151, thereby forming a preformed electrode and contact. *Id.* at 6:35–38. The top of the FLD layer may be connected to metal layer 122, which is also directly connected to vias 131 in ILD layer 152. *Id.* at 6:38–40. The '702 patent notes that multiple FLD layers can be stacked, thereby increasing the effective device density. *Id.* at 6:41–42; *see also id* at 5:38–41, 5:47–50 (disclosing a “second FLD layer” not shown in Figure 1).

According to the '702 patent, “[t]he plurality of vertically oriented semiconductor memory cells can be added to the separately fabricated substrate as a thin layer including several doped semiconductor regions which, subsequent to attachment, are etched to produce individual doped stack structures.” Ex. 1001, code (57), 1:57–62. “Alternatively, the plurality of vertically oriented semiconductor memory cells may be completely fabricated prior to attachment” to the separately fabricated substrate. *Id.* at code (57), 1:67–2:3.

The '702 patent explains that the “FLDs may, but are not required to, have a pillar structure.” Ex. 1001, 6:43. The FLD of the '702 patent also “has a gate dielectric layer which may be implemented with process operations at temperatures below 650° C.” *Id.* at 7:15–17, 7:20–22 (“Any

suitable dielectric material could be used except films requiring processing at temperatures more than 650° C.”).

D. Illustrative Claim

Petitioner challenges claims 13–17 of the ’702 patent. Pet. 3–4. Independent claim 13, reproduced below, is illustrative of the challenged claims:

13. A semiconductor memory structure, comprising:
 - [a] a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices;
 - [b] a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells; and
 - [c] the stackable add-on layer being bonded to the dielectric layer; and
 - [d] wherein the memory cells are nonvolatile memory cells having at least one transistor.

Ex. 1001, 12:24–34 (paragraph identifications [a]–[d] are added to align with the parties’ arguments).

E. Asserted Grounds of Unpatentability

Petitioner asserts that claims 13–17 of the ’702 patent are unpatentable in view of the following grounds (Pet. 3–4):

Claim(s) Challenged	35 U.S.C. §¹	Reference(s)/Basis
13	103(a)	Watanabe ²
14–17	103(a)	Watanabe, Endoh ³
13–15	103(a)	Lee ⁴
16, 17	103(a)	Lee, Endoh
13–15	103(a)	Lee, Watanabe
16, 17	103(a)	Lee, Watanabe, Endoh

III. ANALYSIS

A. Legal Standard

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and “the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103, effective March 16, 2013. The ’702 patent issued May 27, 2008. Ex. 1001, code (45). Accordingly, we apply the pre-AIA version of § 103. *See* 35 U.S.C. § 100(i)(1)(B).

² US 5,091,762, issued February 25, 1992. Ex. 1005 (“Watanabe”).

³ US 2002/0154556 A1, published October 24, 2002. Ex. 1006 (“Endoh”).

⁴ US 6,881,994 B2, filed August 13, 2001, and published April 19, 2005. Ex. 1007 (“Lee”).

factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

The parties agree that one of ordinary skill in the art “would have had a bachelor’s degree in electrical engineering, computer engineering, or a related field, and at least two years of experience in the research, design, or development of semiconductor memory device structures, or the equivalent, with additional education substituting for experience and vice versa.” Pet. 8; PO Resp. 12; Ex. 1002 ¶ 34; Ex. 2029 ¶¶ 33–37.

C. Claim Construction

In this proceeding, the claims of the ’702 patent are construed “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b).” 37 C.F.R. § 42.100(b). Under that standard, the words of a claim are generally given their “ordinary and customary meaning,” which is the meaning the term would have had to a person of ordinary skill at the time of the invention, in the context of the entire patent including the specification. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc).

Upon review of the prior art and the parties’ arguments, we determine that only the term “a stackable add-on layer” requires express construction. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (“[O]nly those terms need be

construed that are in controversy, and only to the extent necessary to resolve the controversy.”)).

“stackable add-on layer”

Claim 13 requires “a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells,” that is “bonded to the dielectric layer.” Ex. 1001, 12:29–32. Petitioner contends that Patent Owner’s district court complaint appears to interpret this claim term to cover forming the “stackable add-on layer” by sequential deposition directly on the substrate, but argues the intrinsic record of the ’702 patent does not support such a construction. Pet. 6 n.2 (citing Ex. 1019 ¶¶ 71–76). According to Petitioner, “a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells” and “the stackable add-on layer being bonded to the dielectric layer” in combination require “vertically oriented semiconductor memory cells” to be formed in a separately fabricated “stackable add-on layer,” which is then “bonded [to] the dielectric layer.” *Id.* at 13 n.3.

In the Institution Decision, we preliminarily construed “stackable add-on layer” to be “a layer that is formed separately from the substrate and then bonded as [a] whole to the dielectric layer positioned above the substrate.” Inst. Dec. 9. We further noted that “[w]e do not understand a ‘stackable add-on layer’ to include memory cells that are formed by sequential deposition on or above a substrate without being added to a separately formed substrate.” *Id.*

Petitioner “agrees in substance” with our preliminary construction but would modify the construction to be “a layer structure ~~that is~~ formed separately from the substrate ~~and then~~ suitable to be bonded ~~as whole~~ to the

dielectric layer positioned above the substrate.” Pet. Reply 4. Petitioner also agrees that a “stackable add-on layer” should not be read to include memory cells formed by sequential deposition without being added to a separately formed substrate. *Id.*

Patent Owner contends our preliminary construction “is incorrect” but does not explain why and does not provide its own construction of this term. PO Resp. 13. Rather, Patent Owner contends “the Board may confirm the patentability of the Challenged Claims for reasons unrelated to ‘stackable add-on layer.’” *Id.*; *see also* Sur-reply 4 (asserting that Petitioner’s claim construction arguments “plainly exceed the proper scope of reply under Board rules”).

Neither party asserts that “stackable add-on layer” has an accepted meaning in the art. *See Irdeto Access, Inc. v. Echostar Satellite Corp.*, 383 F.3d 1295, 1300 (Fed. Cir. 2004) (stating that, absent an accepted meaning in the art, “we construe a claim term only as broadly as provided for by the patent itself”). Thus, we must attempt to discern the meaning of this term from the claim language itself and from the remainder of the intrinsic record. *See Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996) (“It is well-settled that, in interpreting an asserted claim, the court should look first to the intrinsic evidence of record, *i.e.*, the patent itself, including the claims, the specification and, if in evidence, the prosecution history.”). Upon review of the parties’ arguments and the intrinsic record, we agree with Petitioner that the ’702 patent does not support a construction of “stackable add-on layer” that encompasses memory cells formed by sequential deposition on a substrate without being formed and then added to a separately formed substrate.

First, the plain language of the claim does not require merely a “layer” having a plurality of vertically oriented semiconductor memory cells, but rather “a stackable add-on layer” having a plurality of vertically oriented semiconductor memory cells; that plurality is bonded to the dielectric layer. Ex. 1001, 12:29–32. A construction that gives meaning to all words of the claim is preferred. *Merck & Co., Inc. v. Teva Pharm. USA, Inc.*, 395 F.3d 1364, 1372 (Fed. Cir. 2005) (“A claim construction that gives meaning to all the terms of the claim is preferred over one that does not do so.”).

The written description of the ’702 patent summarizes the invention by stating that “a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells” is formed separately from the substrate and then stacked on and bonded to the substrate. Ex. 1001, 1:47–50 (“Briefly, a plurality of vertically oriented semiconductor memory devices, or cells, may be ***added to a separately fabricated substrate*** that includes electrical devices and/or interconnect lines.”) (emphasis added). The ’702 patent discloses two ways of adding a memory cell layer. First, “[t]he plurality of vertically oriented semiconductor memory cells can be added to the separately fabricated substrate as a thin layer including several doped semiconductor regions which, subsequent to attachment, are etched to produce individual doped stack structures.” *Id.* at code (57), 1:57–62. “Alternatively, the plurality of vertically oriented semiconductor memory cells may be completely fabricated prior to attachment” to the separately fabricated substrate. *Id.* at code (57), 1:67–2:3. In both of these methods, the memory cells are added as a layer to a separately fabricated substrate.

Generally supporting this understanding, the specification explains that a Silicon-on-Insulator (“SOI”) layer refers to “a relatively thin, single

crystal portion of a semiconductor wafer that can be cleaved and bonded to another previously fabricated wafer, or similar type of substrate, such that a three dimensional stack is formed from the SOI layer and the previously fabricated wafer or similar type of substrate.” Ex. 1001, 4:47–53.

According to the ’702 patent, “[i]n this context, the SOI layer may be thought of as an attachment layer, or stackable add-on structure which is suitable for bonding to a semiconductor substrate already containing devices and/or interconnections.” *Id.* at 4:53–57. Consistent with the summary of the invention discussed above, this description in the ’702 patent suggests that a “stackable add-on layer” is a layer that is formed separately from the semiconductor substrate and then bonded to the substrate that already contains devices and/or interconnections, i.e., a separately fabricated substrate. We further note that we are directed to no embodiment of the ’702 patent wherein layers that are sequentially deposited on the substrate are identified as a “stackable add-on layer.”

Based on the language of the claims and the disclosures found in the written description, we understand that a “stackable add-on layer” is a layer that is formed separately from the substrate and then bonded to the dielectric layer positioned above the substrate. We do not understand a “stackable add-on layer” to include memory cells that are formed by sequential deposition on or above a substrate without being added to a separately formed substrate.

As to the precise language of our construction, we agree with most of Petitioner’s proposed modifications. We decline, however, to change “layer” to “structure,” as proposed by Petitioner. The term “layer” is part of the term “stackable add-on layer,” and removing it would therefore be

inappropriate. Petitioner does not generally disagree but wishes to make clear that a single “stackable add-on layer” could be comprised of several layers. Tr. 5:17–6:6. On that point, we agree that the term “a layer” could include one or more layers. *See ABS Global, Inc. v. Cytonome/St, LLC.*, 84 F.4th 1034, 1040 (Fed. Cir. 2023) (noting that in a “comprising claim” the use of “a” or “an” is generally construed to mean “one or more”); Ex. 1001, code (57) (explaining that the vertically oriented semiconductor memory cells may be attached as a thin layer containing “several doped semiconductor regions”); *see also id.* at 6:23–25 (stating the “transferred, unpatterned, SOI layer has only a vertically oriented stack of layers”).

In view of the foregoing, we construe “stackable add-on layer” to mean “a layer formed separately from the substrate suitable to be bonded to the dielectric layer positioned above the substrate.” Our construction also provides that a “stackable add-on layer” should not be read to include memory cells that are formed by sequential deposition on or above a substrate without being added to a separately formed substrate.

D. Claims 13–15 over Lee

Petitioner contends the subject matter of claims 13–15 would have been obvious over the disclosures of Lee. Pet. 46–59.

1. Lee

Lee is titled “Monolithic Three Dimensional Array of Charge Storage Devices Containing a Planarized Surface” and issued April 19, 2005. Ex. 1007, codes (45), (54).

Lee notes that the cost of memory and logic devices is decreased by increasing device density and that one method of increasing device density “is to arrange the devices in a monolithic three dimensional array of charge

storage devices comprising a plurality of device levels.” Ex. 1007, 11:18–27. In this context, “monolithic” means that the layers of each level of the array are directly deposited on the layers of each underlying level of the array. *Id.* at 11:27–30. This is in contrast to two-dimensional arrays, which “may be formed separately and then packaged together to form a non-monolithic memory device.” *Id.* at 11:30–32.

Figure 35 is reproduced below:

FIG. 35

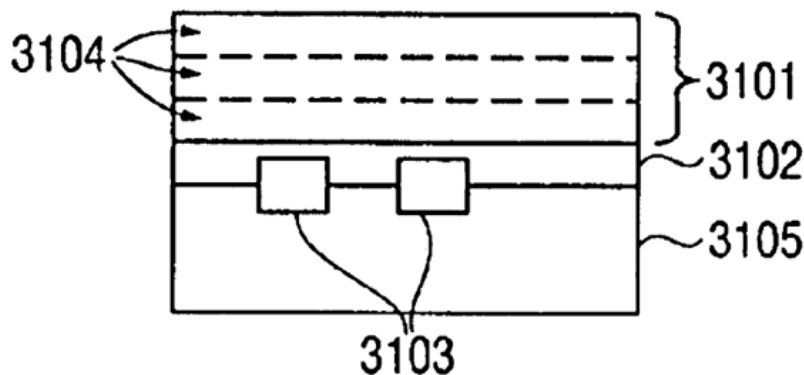


Figure 35 is a schematic of a three-dimensional array of devices. Ex. 1007, 9:12–13. In the device of Figure 35, driver circuits 3103, such as sense amps and charge pumps, are disposed in monocrystalline substrate 3105, as CMOS or other transistors. *Id.* at 12:25–27. Interlayer insulating layer 3102 is then disposed on monocrystalline substrate 3105. *Id.* at 12:16–19. Charge storage logic or memory devices 3101 have a plurality of device levels 3104 that are preferably separated by interlayer insulating layers. *Id.* at 12:23–25.

Lee explains that “[t]he charge storage devices of the array may be any type of semiconductor devices which store charge, such as EPROMs or EEPROMs.” Ex. 1007, 12:50–52. Such charge storage devices may be

formed in various configurations, “such as a pillar TFT EEPROM, a pillar diode with a charge storage region, a self aligned TFT EEPROM, a rail stack TFT EEPROM, and various other configurations.” *Id.* at 12:52–57.

Figure 1A of Lee is reproduced below:

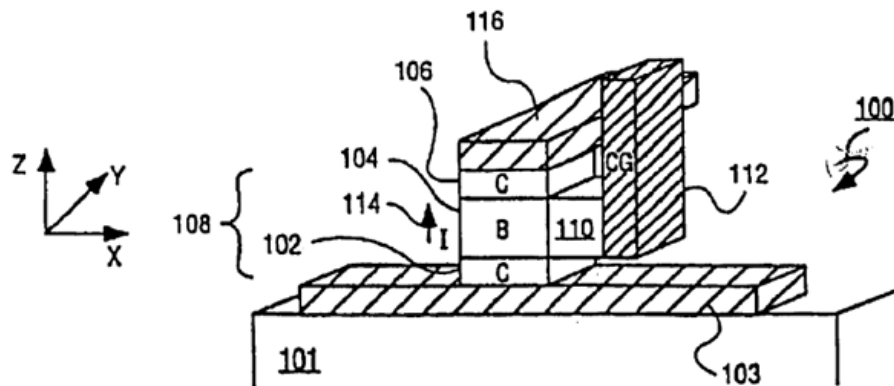


FIG. 1A

Figure 1A is an illustration of a pillar memory. Ex. 1007, 8:17–18. In Figure 1A, “[p]illar memory device 100 includes a first contact region 102 formed on a first input/output (I/O) 103 conductor formed on or above a plane (x-y) of a single crystal substate 101.” *Id.* at 14:13–16.

Semiconductor body 104 is formed directly on first contact region 102 and second contact region 106 is formed on body 104. *Id.* at 14:16–19. Second I/O region 116 is formed on second contact region 106. *Id.* at 14:19–20.

Lee explains that first contact region 102, body 104, and second contact region 106 are each vertically aligned to form pillar 108. *Id.* at 14:20–23.

“Adjacent to and in contact with body 104 is a charge storage medium 110,” with control gate 112 formed adjacent to and in direct contact with charge storage medium 110. *Id.* at 14:23–26.

Lee explains that:

The programmed and unprogrammed state of the pillar memory device is determined by whether or not charge is stored

in charge storage medium 110. The charge stored in the charge storage medium adds or subtracts from the voltage applied to the control gate, thereby altering the voltage required to form a conducting channel in body 104 to enable a current (e.g., read current I_R) to flow between the first and second contact (source/drain) regions.

Ex. 1007, 14:32–39.

Figure 2 is reproduced below:

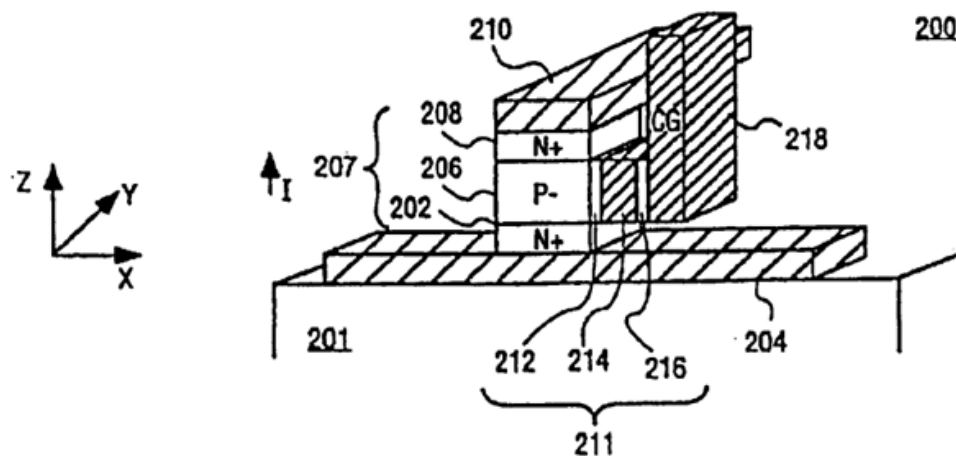


FIG. 2

Figure 2 is an illustration of a pillar memory. Ex. 1007, 8:27–28. In this embodiment, pillar 207 includes first source/drain contact region 202 comprising a heavily doped N+ silicon film that is formed on a first input/output 204 (e.g. bit line) that is formed on or above substrate 201. *Id.* at 15:16–22. Body 206 is composed of lightly doped P- type silicon film 206 that is formed on and in direct contact with N+ source/drain contact region 202. *Id.* at 15:22–25. Second drain region 208 is composed of a heavily doped N+ silicon film and is formed on and in direct contact with P- type silicon film 206. *Id.* at 15:25–30. “A second conductive input/output (e.g. word line/bit line) 210 is formed on the second N+

source/drain region 208.” *Id.* at 15:30–31. Charge storage medium 211 comprises tunnel dielectric 212, floating gate 214, and control gate dielectric 216. *Id.* at 15:41–43. Control gate 218 is formed adjacent to, and in direct contact with, control gate dielectric 216. *Id.* at 15:50–52. “Control gate 218 is formed of a conductor such as but not limited to doped silicon or a metal such as tungsten.” *Id.* at 15:52–54.

2. Claim 13

Petitioner contends that Lee discloses every limitation of independent claim 13. Pet. 46–54. With respect to the preamble and element 13[a], Petitioner contends Lee is directed to a semiconductor memory structure, Figure 35 of Lee depicts driver circuits 3103 formed in monocrystalline substrate 3105, and a dielectric layer (interlayer insulating layer 3102) is disposed on substrate 3105 and above the electrical devices. *Id.* at 46–47 (citing Ex. 1007, 1:25–26, 12:17–27, Fig. 35; Ex. 1002 ¶ 116).

With respect to element 13[b], Petitioner contends Figure 1A depicts TFTs and diodes arranged in a pillar configuration, i.e., vertically oriented with respect to the substrate, and Figure 35 shows an array of charge storage logic or memory devices 3101 with a “plurality of device levels 3104.” Pet. 48–50 (citing Ex. 1007, 5:46–56, 12:17–27, Figs. 1A, 35). Petitioner asserts that, “[b]ecause Lee discloses ‘a three dimensional nonvolatile memory array, comprising a plurality of vertically separated device levels,’ in which ‘each level comprise[es] an array of TFT EEPROMs,’ the memory array is a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells,” *as apparently construed by Patent Owner*. *Id.* at 50 (citing Ex. 1007, 5:46–49, Ex. 1002 ¶ 118); *see id.* at 48 n.5 (“Lee

discloses the subject matter [of element 13[b]] of the '702 Patent under the interpretation [Patent Owner] appears to adopt.”).

With respect to element 13[c], Petitioner contends that memory devices 3101 are formed above interlayer insulating layer 3102, and one of ordinary skill in the art would have understood that the memory array of Figure 35 is bonded to interlayer insulating layer 3102. Pet. 50–52 (citing Ex. 1007, 12:17–25; Ex. 1002 ¶ 119). As support for its argument that Lee discloses a stackable add-on layer bonded to an insulating layer, Petitioner points to Lee’s description of a monolithic array, Lee’s disclosures relating to Figure 35, and Lee’s disclosures relating to Figure 83A. *Id.* at 51–52 (citing Ex. 1007, 11:24–31, 55:32–36, Figs. 35, 83A).

With respect to element 13[d], Petitioner contends that Lee generally discloses that its array may contain EEPROMs (a form of nonvolatile memory) and that the memory device of Figure 1A is non-volatile and has at least one transistor. Pet. 53–54 (citing Ex. 1007, 14:10–23; Ex. 1002 ¶ 122).

As discussed above, we construe “stackable add-on layer” to not include memory cells that are formed by sequential deposition on or above a substrate without being added to a separately formed substrate. It is undisputed, and indeed it is Petitioner’s assertion, that Lee’s memory devices are formed by sequential deposition. *See* Pet. 52 (asserting that in Lee “the layers of the array are directly deposited on the layers of each underlying level, and the array is deposited on the interlayer insulating layer formed over a substrate”); *see also id.* at 70 (“Lee discloses forming vertical memory devices through layer-by-layer sequential deposition on the substrate . . .”). Therefore, Petitioner does not show that Lee discloses every limitation of independent claim 13 under our claim construction.

Thus, Petitioner does not demonstrate by a preponderance of the evidence that claim 13 would have been obvious in view of Lee.

3. Claims 14 and 15

Claims 14 and 15 depend from claim 13. Ex. 1001, 12:35–42. Petitioner’s arguments for these claims do not remedy the deficiencies noted above with respect to independent claim 13. Pet. 54–59. Accordingly, Petitioner does not demonstrate by a preponderance of the evidence that claims 14 and 15 would have been obvious in view of Lee alone.

E. Claims 16 and 17 over Lee and Endoh

Petitioner contends the subject matter of claims 16 and 17 would have been obvious over the combined disclosures of Lee and Endoh. Pet. 59–69. Petitioner’s arguments with respect to these claims, however, do not remedy the deficiencies noted above with respect to Lee and its monolithic, sequentially deposited memory array. Accordingly, Petitioner does not demonstrate by a preponderance of the evidence that claims 16 and 17 would have been obvious over Lee and Endoh.

F. Claim 13 over Watanabe

Petitioner contends the subject matter of claim 13 would have been obvious over Watanabe. Pet. 13–26.

1. Watanabe

Watanabe is titled “Semiconductor Memory Device With a 3-Dimensional Structure,” and issued February 25, 1992. Ex. 1005, codes (45), (54).

Watanabe explains that an object of its invention “is to provide a semiconductor memory device in which memory cells are arrayed three-

dimensionally, thereby providing a high integration density.” Ex. 1005, 1:49–52. Figure 1 of Watanabe is reproduced below:

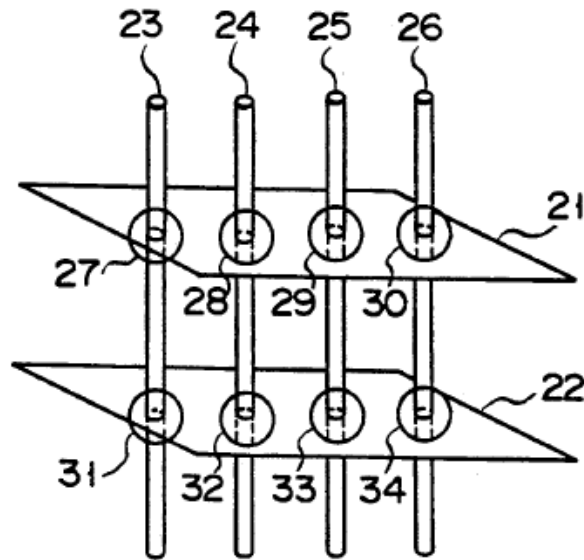
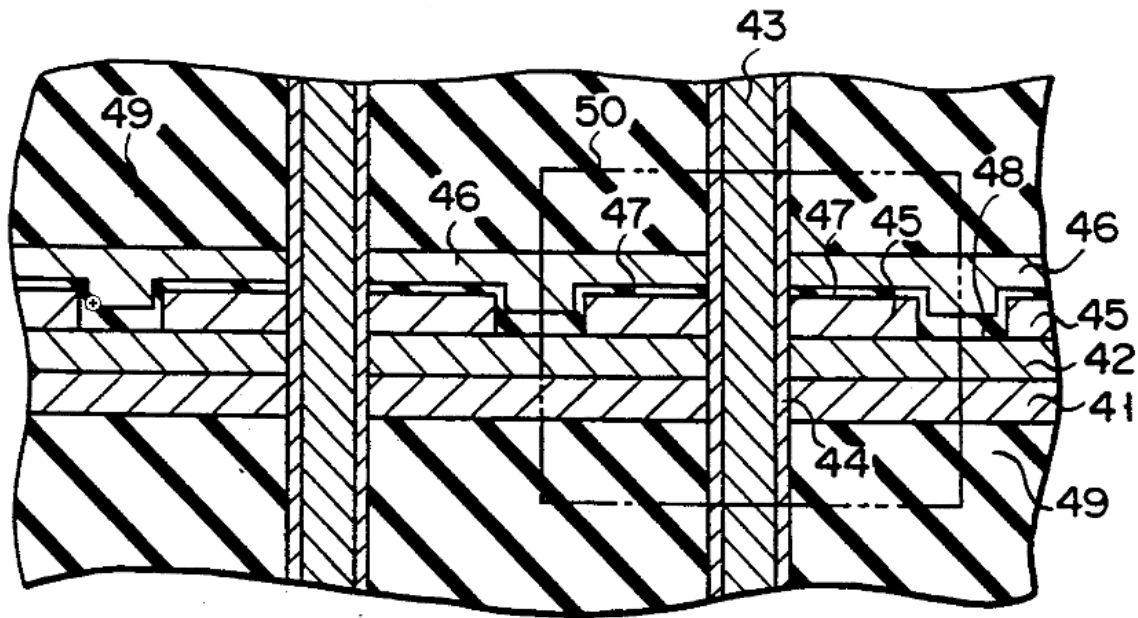


Figure 1 is a rough schematic illustration of a physical arrangement of a semiconductor memory device. Ex. 1005, 2:8–10. In Figure 1, the memory device is made up of two conductive planes 21 and 22 and four wires 23 to 26. *Id.* at 2:44–48. There are eight cross points where wires 23 to 26 pass through planar members 21 and 22. *Id.* at 2:48–51. Watanabe explains that “the conductive planar members 21 and 22 are used for inputting and outputting data (i.e., they serve as data planes), and wires 23 to 26 serve as word lines.” *Id.* at 2:58–61. Watanabe further explains that the memory cell depicted in Figure 1 “is applicable to any type of memory device, i.e., a SRAM, a PROM, or a DRAM,” but that the descriptions that follow in the patent are directed to a DRAM memory cell. *Id.* at 2:51–55.

Figure 2A is reproduced below:



F I G. 2 A

Figure 2A is a sectional view of a part of the semiconductor memory device shown in Figure 1 “and shows details of the structure of the memory device,” in this case, DRAM cell 50. Ex. 1005, 2:11–13, 2:62–63, Fig. 2A. In Figure 2A, conductive planar member 41 is in the form of an N+ type silicon layer and “serves as the source of the MOSFET.” *Id.* at 2:66–3:2. P-type Si layer 42 is above planar member 41. *Id.* at 3:2. N+ type Si layer 45 is above layer 42, with a portion surrounding each associated wire 43, and is overlaid by thin insulating film 47. *Id.* at 3:6–9. Thick insulating film 48 fills the spaces between each portion of layer 45 and is overlaid with conductive layer 46. *Id.* at 3:9–12. Wire 43 is oriented orthogonally to planar member 41 and is separated from layers 41, 42, 45, and 46 by insulating film 44. *Id.* at 3:2–5. Watanabe explains that in this embodiment

“[a]t least two stack structures (two layers) each consisting of layers 41 to 46 are provided, which are insulated from each other by an insulating film 49, and through which the wires 43 pass.” *Id.* at 3:12–15.

In operation, layer 41 serves as a data line for the input and output of data to and from the memory cell. Ex. 1005, 3:16–19. A potential is applied to layer 41 thereby placing wiring 43 in a high potential and inverting the conductivity of the portion of the p-type Si layer 42 that is in contact with the gate insulating film 44. *Id.* at 3:19–23. A charge is then transferred to the charge storage region 45 and stored in a capacitor located between region 45 and capacitor electrode 46. *Id.* at 3:23–27. “Then, if the potential of the wire 43 is decreased, the drain of the n⁺ Si layer 45 is electrically separated from the data plane 41.” *Id.* at 3:27–30.

Watanabe explains that the semiconductor device of “the present invention may lower the resistance of the wires,” because the data plane “is planar, not a thin line,” making its resistance in the order of the “sheet resistance of the material used.” Ex. 1005, 4:52–56. The word, or data, line is a thin line, but its length is at most 1 mm. *Id.* at 4:56–60.

Figure 7 is reproduced below:

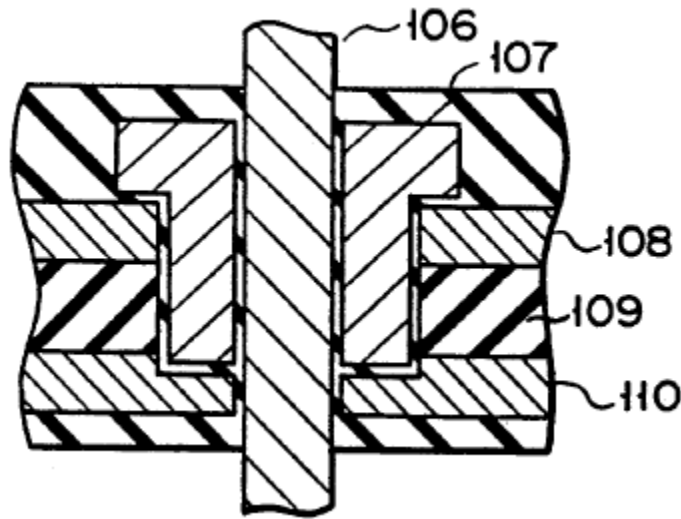


Figure 7 “is a sectional view showing a[n] application of the present invention into an EPROM.” Ex. 1005, 2:36–37. As shown in Figure 7, the disclosed EPROM includes control gate 106, floating gate 107, source 108, channel region 109, and drain region 110. *Id.* at 6:15–19.

Watanabe discloses two different methods of manufacturing its disclosed memory devices: a “laminating method” and a “stacking method.” Ex. 1005, 5:1–7, 5:45–55. In the “laminating method,” “a plurality of planar members are formed and are laminated, and holes are formed in the laminated planar members, through which the wiring passes.” *Id.* at 5:1–7, Figs. 5A to 5E. In this method, a first planar member is completed in a sequence of process steps, and then a second planar member is formed over the first planar member in a sequence of process steps similar to that used to form the first planar member. *Id.* at 5:8–32. After “a desired number of planar members are first formed into a stack of planar members, . . . contact holes are formed and wires buried therein.” *Id.* at 5:41–44.

In the “stacking method,”

a first planar member is formed, and then wires are buried in the contact holes, respectively. A second planar member is formed, and the formed planar member is holed for contact hole, and wires are buried into the holes. The process is repeated by the number of times equal to a necessary number of planar members. Finally, the planar member[s] thus formed are stacked and wired.

Ex. 1005, 5:45–55, Figs. 6A–6D. Watanabe explains that the planar members are bonded together using a thermal process at 900 to 1000° C. *Id.* at 6:6–8. Thereafter, contact holes are formed and a second interconnection wire is buried to complete the semiconductor memory device. *Id.* at 6:8–11. According to Watanabe, “[i]n the stacking method, a number of process steps is increased, but a wiring accuracy is improved because the wiring is made [in] every planar member.” *Id.* at 6:11–14.

2. Claim 13

Petitioner contends the subject matter of claim 13 would have been obvious in view of the disclosures of Watanabe. Pet. 13–26.

With respect to the preamble “[a] semiconductor memory structure, comprising,” Petitioner contends Watanabe expressly states that its invention “relates to a semiconductor memory device.” Pet. 14 (quoting Ex. 1005, 1:10–11).

With respect to element 13[a], Petitioner contends that in each of the “laminating” and “stacking” embodiments of Watanabe, the silicon substrate has “a peripheral circuit and transistors 71 and 72” that are formed in the upper surface thereof, as well as a dielectric layer 100 (“insulating film”) formed over this Si substrate and above the electrical devices. Pet. 14–16 (citing Ex. 1005, 5:11–13, 5:58–61, Figs. 5A, 6A; Ex. 1002 ¶¶ 71–72).

With respect to element 13[b], Petitioner contends that planar members 21 and 22 in Watanabe's Figure 1 correspond to a "stackable add-on layer" and Figure 2A of Watanabe discloses the formation of semiconductor memory cells in which the transistors' source-channel-drain-elements (e.g., elements 41, 42, and 45) are arranged vertically. Pet. 16–21 (citing Ex. 1001, 1:65–2:2, 2:65–3:15, 4:7–9; Ex. 1002 ¶¶ 73–74; Ex. 1005, 5:1–6:14, Figs. 1, 2A, 5A–5E, 6A–6D).

Addressing elements 13[b] and 13[c], Petitioner contends that Watanabe's "stacking method" and "laminating method" teach or suggest a stackable add-on layer that is bonded to the dielectric layer under either Petitioner's ("stacking") or Patent Owner's ("laminating") constructions of "stackable add-on layer." Pet. 18–24 (citing Ex. 1005, 5:1–6:14, Figs. 5A–5E, 6A–6D; Ex. 1002 ¶¶ 76–82). In support of this argument, Petitioner walks through the various disclosed steps of forming the volatile DRAMs depicted in Figures 5A–E and 6A–D. *Id.*

Finally, with respect to element 13[d], Petitioner contends that the EPROM memory device of Figure 7 is a vertically-oriented, "nonvolatile memory" cell having at least one transistor. Pet. 25–26 (citing Ex. 1005, 6:15–19; Ex. 1002 ¶ 84; Ex. 1009, 25–26 ("One floating gate transistor suffices to build an EPROM memory cell.")).

Patent Owner contends the ground based on Watanabe alone fails because Petitioner fails to establish that Watanabe discloses the "non-volatile" requirement of element 13[d] (PO Resp. 56–59) and because Watanabe's stacking method is not enabled (*id.* at 62–63). As discussed below, we determine that Petitioner has not met its burden of proof to show

obviousness of claim 13 over Watanabe for each of these separate and independent reasons advanced by Patent Owner.

a. “*nonvolatile memory cells*”

Patent Owner contends the claims require that the “memory cells” be “nonvolatile memory cells,” yet the majority of Petitioner’s claim mapping for claim 13 is directed to the volatile DRAM memory depicted in Figures 1, 2A, 5, and 6. PO Resp. 56, 58–59. According to Patent Owner, Petitioner provides no explanation as to how the volatile and non-volatile embodiments of Watanabe identified in the Petition would have been combined, nor an explanation as to how the nonvolatile memory of Figure 7 would have been constructed using Watanabe’s stacking method. *Id.* at 59 (“[Petitioner] provided no explanation of how it would be combined with the volatile embodiments, let alone with any reasonable expectation of success.”).

Petitioner argues in reply that, although Figures 5 and 6 of Watanabe illustrate manufacturing methods for volatile DRAM, a person of ordinary skill in the art “would have understood that Watanabe’s teachings regarding the manufacturing methods apply equally to any type of memory cell disclosed in the invention.” Pet. Reply 23. According to Petitioner, it did not “combine Watanabe’s DRAM and EPROM embodiments,” but rather its citations to Figures 2A, 5, and 6 were merely to illustrate how Watanabe’s “stacking” and “laminating” methods apply to the EPROM memory cell structure shown in Figure 7. *Id.* at 22–23. Petitioner contends, for example, that the contents of Figure 2A’s cell 50 could be replaced with the nonvolatile memory cell shown in Figure 7 “because photolithography steps necessary to make an EPROM memory cell were well known and within the

skill of a [person of ordinary skill in the art].” *Id.* at 23–24 (citing Ex. 1041 ¶ 65).

Patent Owner responds that the Petition expressly relied upon Figures 1 and 2A of Watanabe for element 13[b] “and never argued that one of skill could replace the contents of Figure 2A’s cell.” Sur-reply 25 (citing Pet. 16–18; Pet. Reply 23). Patent Owner further contends that the argument that the contents of Figures 2A’s cell could be replaced by the EPROM of Figure 7 was not in the Petition and should not be considered now. *Id.* at 24–25.

We agree with Patent Owner that Petitioner has not met its burden of proof. Watanabe discloses both a laminating and stacking method and that its invention “is applicable to any type of memory device, i.e., a SRAM, a PROM, or a DRAM.” Ex. 1005, 2:51–53. The disclosures of Figures 1–6 expressly relied upon by Petitioner, however, are to the DRAM embodiment, which is a volatile type of memory, not nonvolatile, as recited in claim element 13[d]. *Id.* at 2:53–55 (“[H]owever, in the description to follow, the memory cell is depicted as incorporated in a DRAM.”). The Petition never identifies where Watanabe teaches or suggests elements 13[a]–[c] outside a DRAM embodiment, which lacks the nonvolatile memory cells of element 13[d]. Pet. 14–24. For example, the Petition does not show that Watanabe’s Figure 7 embodiment teaches or suggests elements 13[a]–[c]. *Id.*

Petitioner’s argument that the nonvolatile memory cell depicted in Figure 7 could be substituted in Watanabe Figure 2A is a new theory presented for the first time in reply. Pet. Reply 23–24. “It is of the utmost importance that petitioners in the IPR proceedings adhere to the requirement

that the initial petition identify ‘with particularity’ the ‘evidence that supports the grounds for the challenge to each claim.’” *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3)). Any marked departure from the grounds identified with particularity in the petition would impose “unfair surprise” on the patent owner and, consequently, violate both the Administrative Procedure Act and the *inter partes* review statute. *Arthrex Inc. v. Smith & Nephew, Inc.*, 935 F.3d 1319, 1328 (Fed. Cir. 2019). Here, the Petition never asserted that the structure depicted in Figure 7 could be substituted into the structure depicted in Figure 2A, and considering that new argument now would impose an “unfair surprise” on Patent Owner. Pet. 25–26.

Moreover, even if Petitioner’s new argument were considered, Petitioner fails to show that the combination of Figs. 2A and 7 satisfies claim elements 13[a]–[c]. For example, Petitioner never explains what the complete structure of Watanabe would be if the EPROM depicted in Figure 7 were inserted into the device depicted in Figure 2A. Pet. Reply 22–24. And, Petitioner fails to identify with particularity where every limitation of claim 13 is disclosed in Watanabe.

In view of the foregoing, Petitioner fails to identify where Watanabe teaches or suggests every limitation of independent claim 13. For this reason alone, Petitioner does not demonstrate by a preponderance of the evidence that claim 13 would have been obvious over Watanabe.

b. *Enablement of Watanabe’s Stacking Method*

“To render a claim obvious, the prior art, taken as a whole, must enable a skilled artisan to make and use the claimed invention.” *Raytheon Techs. Corp. v. Gen. Elec. Co.*, 993 F.3d 1374, 1380 (Fed. Cir. 2021). A

prior art reference, however, is presumed enabled, and the patentee has the burden to prove nonenablement. *Apple Inc. v. Corephotonics, Ltd.*, 861 F. App'x 443, 450 (Fed. Cir. 2021) (nonprecedential; *inter partes* review context); *Amgen Inc. v. Hoechst Marion Roussel, Inc.*, 314 F.3d 1313, 1354 (Fed. Cir. 2003). Moreover, “a prior art reference asserted under § 103 does not necessarily have to enable its own disclosure, i.e., be ‘self-enabling,’ to be relevant to the obviousness inquiry.” *Raytheon*, 993 F.3d at 1380. For example, such a reference could provide the motivation to combine, and then be combined with a reference in which the limitation in question is enabled, or the reference could be used to supply the claim elements if it is enabled by another reference. *Id.* But “if an obviousness case is based on a non-self-enabled reference, and no other prior art reference or evidence would have enabled a skilled artisan to make the claimed invention, then the invention cannot be said to have been obvious.” *Id.* at 1377.

1. The Parties' Arguments

Patent Owner contends that Watanabe's stacking method, relied upon by Petitioner to show elements 13[a]–[c], requires a thermal bonding process conducted at 900–1000° C. PO Resp. 62–63 (citing Ex. 1005, 6:6–8; Pet. 14–19, 21–23). Patent Owner further contends that Petitioner's expert, Dr. Lee, confirmed during his deposition that Watanabe's high-temperature bonding technique would exceed the thermal budget of the transistors embedded in the substrate, thereby damaging those transistors. *Id.* at 63 (citing Ex. 2028, 123:13–124:7). This problem is exacerbated, according to Patent Owner, because each layer in Watanabe is individually bonded and wired, and Watanabe “contemplate[s] bonding 100 layers, with 100 high-temperature bonding steps.” PO Resp. 25; PO Sur-reply 14–15 (citing Ex.

1005, 4:35–38, 6:6–14; Ex. 2029 ¶¶ 75–76). Thus, Patent Owner contends Watanabe’s stacking method is not enabled and “a skilled artisan would not have been motivated to use it for fear of over-baking the transistors.” PO Resp. 56, 62–63 (citing Ex. 2027, 715; Ex. 2029 ¶¶ 70–77, 144–146); Sur-Reply 14–15.

Petitioner does not persuasively dispute that at the time Watanabe issued (1992) thermal bonding at 900–1000° C would damage or destroy transistors formed in the various layers of Watanabe’s stackable device. *See* Pet. Reply 14, 25–26. Petitioner asserts, however, that in the relevant time period, i.e., as of the filing date of the ’702 patent, one of ordinary skill in the art would have known how to apply “well-known solutions” to this problem. *Id.* at 14–15, 25–26; *Raytheon*, 993 F.3d at 1380 n.5 (explaining that a non-enabled patent may be used in conjunction with other, later-arising prior art that enables the disputed limitation).

First, Petitioner contends that it was understood in the art that the thermal budget is a measure of both temperature and time, and there existed in the art known methods of applying temperatures of 900–1000° C for short periods of time, such as electromagnetic induction heating (EMIH), that “do not exceed the thermal budget and avoid damage to the lower memory cells.” Pet. Reply 14 (citing Ex. 1041 ¶¶ 35–44; Ex. 1048, 1:26–29, 1:40–43, 1:64–67; Ex. 1049; Ex. 1050, 515–516, 519; Ex. 1053, 15, 17–18, Table 1; Ex. 1059, 9–10).

Second, Petitioner contends that repeated heating to 900–1000° C for each successive layer of Watanabe could be avoided by bonding the various layers in a single step. Pet. Reply 15 (citing Ex. 1060, 285; Ex. 1059, 29). For example, Petitioner contends the art disclosed methods of

simultaneously bonding four pairs of stacked wafers using EMIH in 5 minutes. *Id.*

Patent Owner asserts in its Sur-reply that arguments about other heating methods, such as EMIH, are improper new arguments that should have been in the Petition, but nevertheless these arguments fail to establish that Watanabe is enabled. Sur-reply 11–12, 27. Patent Owner reasons that the EMIH references relied upon by Petitioner all originate from the work of “then-graduate student Keith Thompson: his patent, Ph.D. thesis, and an article,” yet none of those references provide the solution Petitioner claims. *Id.* at 12 (citing Exs. 1048, 1059, 1060).

Patent Owner acknowledges that Thompson’s silicon wafers were bonded using EMIH at 1000° C, with excellent bonds obtained in 5 minutes. Sur-reply 12 (citing Ex. 1059, 93–94). Patent Owner contends, however, that each wafer was still heated to 1000° C, a temperature that Dr. Lee testified could not be exceeded without detrimental effects. *Id.* at 13 (citing Ex. 2028, 123:13–124:7; Ex. 2029 ¶¶ 70–77). And, to the extent the layers of Watanabe could be heated to 900–1000° C for a certain period of time, Patent Owner contends that Petitioner and Dr. Lee never establish the amount of time Watanabe’s layers could be safely exposed to high temperatures and not destroy the underlying electronic devices. *Id.* at 13–14, 27.

2. Analysis

Watanabe discloses bonding its stacked layers using a thermal process at 900–1000° C, and Petitioner expressly relies upon this bonding temperature in its arguments regarding Watanabe. Ex. 1005, 6:6–8; Pet. 22–23; Pet. Reply 25–26. Dr. Lee testified during his deposition, taken

in 2024, that any bonding at a temperature above 650° C would risk destroying the underlying electronic components in the substrate. Ex. 2028, 123:13–124:7 (Dr. Lee testifying that “[i]n other words, the processing of the upper layer transistors cannot go above 650 degrees C” due to the presence of the CMOS transistor in the substrate level). In support of this position, Dr. Lee referenced a publication by Batude,⁵ which explains that when processing upper layer FETs, a low temperature (less than 650° C) “process is mandatory.” Ex. 1034, 715; *see also* Ex. 1036 (errata sheet noting that the “Patude” reference discussed during Dr. Lee’s deposition is actually “Batude”). This is strong evidence that Watanabe’s high temperature bonding at 900–1000° C was not enabled.

We credit the testimony of Dr. Przybylski that one of ordinary skill in the art would have understood that Watanabe’s stacked structure would be severely impacted if bonded at a temperature above 900° C, as disclosed in Watanabe. Ex. 2029 ¶¶ 76–77. Dr. Przybylski’s opinion is supported by Dr. Lee’s testimony (Ex. 2028, 123:13–124:7, 125:6–126:7), as well as Watanabe (Ex. 1005, 6:6–14) and Batude (Ex. 2027, 715). As further discussed below, we find that Petitioner has not rebutted Patent Owner’s showing of nonenablement, and Patent Owner has carried its burden to demonstrate that Watanabe was not enabled for bonding temperatures of 900–1000° C, as of the 2004 filing date of the ’702 patent.

⁵ Perrine Batude, et al., *3-D Sequential Integration: A Key Enabling Technology for Heterogeneous Co-Integration of New Function with CMOS*, IEEE Journal on Emerging and Selected Topics in Circuits and Systems, Vol. 2, No. 4, December 2012 (Ex. 1034, “Batude”).

Despite Dr. Lee's deposition testimony, Petitioner contends that, by the time the '702 patent was filed, one of ordinary skill in the art would have understood how to perform Watanabe's stacking method at 900° C or higher without exceeding the thermal budget of the underlying transistors.

Pet. Reply 14–15, 25–26. In support of this position, Petitioner identifies various bonding disclosures, including the EMIH method of heating discussed above, that allow bonding to be completed over a much shorter time period than prior methods known in the art. *Id.* at 14–15 (citing Ex. 1048, 1:26–29, 1:40–43, 1:64–67; Ex. 1059, 9–10, 29; Ex. 1049; Ex. 1050, 515–516, 519; Ex. 1060, 285).

The EMIH methods relied upon by Petitioner appear to have been first developed by Keith J. Thompson, starting in 2001. *See* Ex. 1059 (Ph.D. dissertation of Keith Thompson: *Electromagnetic Fast-Firing for the Rapid Thermal Processing of Silicon*, 2003); Ex. 1048, code (60) (provisional filing date of June 8, 2001). In his dissertation, Dr. Thompson states that silicon-silicon and silicon-silicon dioxide bonding of wafers was achieved in 5 minutes at 1000° C using the disclosed EMIH heating methods. Ex. 1059, ii. On this record, however, Patent Owner persuasively demonstrates that Petitioner's EMIH evidence does not show that Watanabe's high-temperature bonding method could be used without exceeding the thermal budget of the underlying transistors in the substrate. Sur-Reply 10–15; *see id.* at 13 (“[Petitioner] and Dr. Lee have no answer for how, exactly, Thompson's microwaving at 1000° C would solve the thermal budget quandary.”).

Dr. Lee was clear during his deposition—taken in 2024—that one of ordinary skill in the art would not have heated a substrate containing

transistors above 650° C. Ex. 2028, 123:13–21. Given Dr. Lee’s 2024 testimony, we are persuaded that one of ordinary skill in the art as of the ’702 patent’s filing date (2004) would not have considered EMIH an acceptable method for heating Watanabe’s stacked embodiment. Moreover, even if one of ordinary skill in the art would have considered EMIH’s shortened heating time as a potential solution to the thermal budget problem in Watanabe, Patent Owner persuades us that no length of time has been identified in which Watanabe’s stacked structures could be heated to 900–1000° C without irreparably damaging transistors 71 and 72 formed in Watanabe’s silicon substrate. Sur-reply 13–14, 27; Ex. 1005, 5:58–60.

Petitioner and Dr. Lee point to various disclosures of successfully bonding silicon-silicon or silicon-silicon-oxide wafers at 1000° C and not exceeding the thermal budget of the wafers. Pet. Reply 14–15, 25–26; Ex. 1041 ¶ 44. But as Patent Owner persuasively argues and Petitioner does not dispute, it is unclear whether these wafers included any pre-formed transistors, much less multiple layers of metal wiring or doped stacked structures similar to those disclosed in Watanabe. Sur-reply 14; Tr. 39:25–40:2 (Petitioner’s asserting that it is “unclear” whether the wafers of Thompson had transistors or memory devices).

Petitioner points to a publication by Regner⁶ in which thermal budgets are discussed with respect to a substrate having CMOS devices formed therein. Pet. Reply 14 (citing Ex. 1053, 15, 17–18, Table 1); Ex. 1053,

⁶ Jürgen Regner, *An Analytical Approach to Quantify the Thermal Budget in Consideration of Consecutive Thermal Process Steps*, 10th IEEE International Conference on Advanced Thermal Processing of Semiconductors (2002) (Ex. 1053, “Regner”).

Abstract (“This paper presents an analytical approach to quantify the [Thermal Budget] of a given CMOS process flow . . .”). This reference identifies multiple relevant variables, as well as complex and detailed equations for calculating the thermal budget for a CMOS process. Ex. 1053, 15–18. Petitioner and Dr. Lee do not address these equations or variables, much less use them to estimate the thermal budget for Watanabe’s stacking method. Ex. 1041 ¶ 40. Rather, citing Regner, Dr. Lee testifies that bonding a structure at 900–1000° C could be achieved for a structure containing field-effect-transistors. *Id.* This conclusory testimony, unrelated to the specific structure identified in Watanabe, is not sufficient to refute Patent Owner’s argument and evidence that Watanabe’s stacking and bonding method at 900–1000° C—which is expressly disclosed in Watanabe and relied upon in the Petition (Ex. 1005, 6:6–8; Pet. 22)—could not be used without damaging the underlying electrical devices in the substrate.

Petitioner asserts that the ’702 patent does not explain how to bond its stackable add-on layers and, therefore, that Patent Owner “demands more from the prior art than the teachings of its ’702 Patent.” Pet. Reply 16 (citing Ex. 1001). This argument is not persuasive. The Petition expressly relies upon a bonding temperature at or above 900° C, and Petitioner does not contend that one of ordinary skill in the art would have used a lower bonding temperature in Watanabe. Pet. 22–23; Pet. Reply 25–26. In contrast to Watanabe, the ’702 patent expressly states that its processing temperature must not exceed 650° C. Ex. 1001, 7:15–29. As such, Patent Owner is not demanding more from the Petition than was disclosed in the ’702 patent. Rather, Patent Owner persuades us that Watanabe and the other evidence cited by Petitioner do not disclose a viable method for bonding the

stacked structure of Watanabe at a temperature at or above 900° C, as asserted in the Petition, without damaging or destroying the underlying electric devices in the substrate. *See Raytheon*, 993 F.3d at 1382 (Petitioner “failed to provide an evidence-based case for how the turbofan engine claimed in the [challenged] patent having a particular power density is enabled by [prior art reference]’s disclosure. Thus, the Board’s finding that [the reference] is ‘enabling’ is legal error.”).

In view of the foregoing, we determine that Patent Owner has carried its burden to demonstrate that Watanabe was not enabled for bonding temperatures of 900–1000° C prior to the filing date of the ’702 patent, and that Petitioner does not demonstrate by a preponderance of the evidence that claim 13 would have been obvious in view of Watanabe.

G. Claims 14–17 over Watanabe and Endoh

Petitioner contends the subject matter of claims 14–17 would have been obvious over the combined disclosures of Watanabe and Endoh. Pet. 26–46.

Claims 14–17 depend, directly or indirectly, from independent claim 13. Ex. 1001, 12:35–52. Petitioner’s arguments regarding Watanabe and Endoh do not cure the deficiencies noted above with respect to Watanabe. Accordingly, Petitioner does not demonstrate by a preponderance of the evidence that claims 14–17 would have been obvious over the combined disclosures of Watanabe and Endoh.

H. Claims 13–15 over Lee and Watanabe

Petitioner contends the subject matter of claims 13–15 would have been obvious in the view of the combined disclosures of Lee and Watanabe. Pet. 69–73.

1. *Analysis – Claim 13*

a. *Arguments in the Petition*

Petitioner asserts that, “[t]o the extent Claim 13 is construed to exclude forming a ‘stackable add-on layer’ through sequential deposition directly on a substrate,” the subject matter of claim 13 is disclosed by Lee in view of Watanabe. Pet. 69.

Petitioner contends that Lee discloses the subject matter of the preamble and elements 13[a] and 13[d]. Pet. 71 (relying on same contentions as presented for Lee alone). With respect to claims 13[b] and 13[c], Petitioner contends that Lee and Watanabe both disclose vertically oriented, non-volatile memory cells that are bonded to a dielectric layer that is deposited over the substrate. *Id.* at 71–72. Petitioner further contends that Watanabe and Lee both disclose forming memory devices through layer-by-layer sequential deposition but that Watanabe also discloses an alternative “stacking method” in which stackable memory layers are formed individually and then bonded to a separately-fabricated substrate. *Id.* at 70, 72.

Petitioner contends one of ordinary skill in the art would have combined Watanabe and Lee because both references “provide complementary solutions for arranging memory cells three-dimensionally to provide a high integration density.” Pet. 69 (citing Ex. 1007, 11:18–32; Ex. 1005, 1:49–2:5). According to Petitioner, one of ordinary skill in the art “seeking to increase the integration density of semiconductor memory devices, and specifically nonvolatile memory devices, would have known of and consulted these proposed solutions.” *Id.* at 69–70 (citing Ex. 1002 ¶ 144). Although Lee discloses forming its memory cells through layer-by-

layer sequential deposition on the substrate, Petitioner contends that Watanabe discloses an “alternative method” of construction, and one of ordinary skill in the art would have sought to “obtain the benefits associated with that method.” *Id.* at 70 (citing Ex. 1002 ¶ 145). Petitioner further notes that Watanabe “discloses a benefit of using its ‘bonding method’—it ‘improves the accuracy of the wiring.’” *Id.* at 71 (quoting Ex. 1005, 5:64–6:3).

b. Arguments in Patent Owner’s Response

Patent Owner contends that the Petition does not establish a motivation to combine Watanabe and Lee, asserting only that Watanabe offers “an alternative method” that would provide unspecified “benefits associated with that method.” PO Resp. 32 (quoting Pet. 70). Patent Owner further contends that, because no advantages to the combination have been identified, Petitioner’s simple offering of two “alternative method[s]” falls short of establishing a motivation to combine them. *Id.* at 33 (“[I]f it ain’t broke, don’t fix it.”).

In addition, Patent Owner contends use of Watanabe’s stacking method, with its bonding step at 900–1000° C, would risk destroying the transistors of Lee that are located in Lee’s substrate. PO Resp. 25–26. Patent Owner contends Dr. Lee confirmed this risk when he testified that upper layer transistors cannot be subject to processing temperatures above 650° C without damaging the transistors in the substrate. *Id.* at 26 (citing Ex. 2028, 123:13–124:7).

Patent Owner further contends that Lee actually expresses a preference for “monolithic” structures and contrasts such a method from packaging together two-dimensional arrays. PO Resp. 33–34 (citing

Ex. 1007, 11:25–32). Patent Owner also asserts that Lee and Watanabe use “incompatible data flows” that “were not readily combinable.” *Id.* at 28, 34–35.

c. Petitioner’s Reply Arguments

Petitioner argues in reply that Watanabe discloses both stacking and sequential deposition methods and both approaches may be used to arrange memory cells “three-dimensionally, thereby providing a high integration density.” Pet. Reply 13 (quoting Ex. 1005, 1:49–52). Petitioner further argues that whether you use a stacking method or sequential deposition, either “would improve the device density” because “Lee’s benefits derived from 3-D integration would be obtained if Lee’s memory structures are formed using Watanabe’s alternative stacking method.” *Id.* at 13–14 (quoting Ex. 2028, 62:20–63:4).

With respect to bonding temperature, Petitioner contends that one of ordinary skill in the art would have understood how to bond Lee’s memory layers using Watanabe’s 900–1000° C bonding temperature in a way that does not exceed the thermal budget of the device or damage the lower memory cells. Pet. Reply 14 (citing Ex. 1041 ¶¶ 35–44; Ex. 1053, 15, 17–18, Table 1). For example, Petitioner identifies the EMIH method of bonding a stack of silicon wafers that it contends would not exceed the thermal budget of Lee’s device layers or transistors. *Id.* (citing Ex. 1048, 1:26–29, 1:40–43, 1:64–67; Ex. 1059, 9–10; Ex. 1049).

d. Patent Owner’s Sur-reply Arguments

Patent Owner contends that Petitioner’s argument that one of ordinary skill in the art would have combined Lee and Watanabe because Lee’s memory structure *could* be formed using Watanabe’s alternative stacking

method is not persuasive. Sur-reply 8–9. According to Patent Owner, “[s]imply disclosing ‘two alternative arrangements . . . does not provide a reason that a skilled artisan would have substituted’ one for the other.” *Id.* at 9 (quoting *Virtek Vision Int’l ULC v. Assembly Guidance Systems, Inc.*, 97 F.4th 882, 886–87 (Fed. Cir. 2024)).

Patent Owner also contends that Petitioner “never grapples with how, exactly, Lee’s memory cells could be implemented by stacking.” Sur-reply 9. Patent Owner reasons that Lee’s interleaved levels have memory cells that share control gates and use higher levels to pattern the lower ones, and Petitioner “points to no clear partition point in Lee’s array where the memory cells could be separately fabricated on different layers, let alone properly aligned.” *Id.*

Patent Owner also contends that a “glaring problem” with combining Lee and Watanabe is that Watanabe’s 900–1000° C bonding temperature would exceed the thermal budget of the device and destroy Lee’s memory. Sur-reply 10, 12–13. Patent Owner further contends that Petitioner does not adequately explain how the stacked layers of Lee and Watanabe could be successfully aligned, absent using the disclosures of the ’702 patent as a roadmap. *Id.* at 15–16 (“[Petitioner] using the challenged patent itself to find missing solutions is the epitome of impermissible hindsight.”).

e. Analysis—Motivation to Combine

Petitioner contends that one of ordinary skill in the art would have combined Lee and Watanabe to achieve improved integration density. Pet. 71. Petitioner concedes, however, that the benefits of Lee’s design related to 3-D integration and improved integration density would be obtained if Lee’s memory structures are formed using either Lee’s

monolithic construction method or Watanabe's alternative stacking method. Pet. Reply 13–14 (citing Ex. 1041 ¶ 34). Thus, we are not persuaded that improved integration density provides a sufficient rationale for Petitioner's combination of Lee's memory device and Watanabe's stacking method.

Petitioner argues that Watanabe's stacking method "improves the accuracy of the wiring" because the wiring is made "for each planar member." Pet. 72 (citing Ex. 1005, 6:1–3). Watanabe also states that its disclosed methods provide "a low interconnection wire resistance." Ex. 1005, 6:20–23. Petitioner does not, however, explain sufficiently how Watanabe's stacking method would improve Lee's device. For example, Petitioner does not address whether the alleged wiring benefit already existed in Lee's monolithic array or explain how this benefit would also apply to Lee's particular memory array, which differs in construction and elements from Watanabe's device. This diminishes Petitioner's benefits-based motivation to combine arguments.

In general, a petitioner need not demonstrate that a particular alternate method would *improve* a prior art device in order to show a motivation to combine. *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380–81 (Fed. Cir. 2023); *see* Pet. Reply 20 (citing *Intel*). But here, Petitioner affirmatively invokes improvement of Lee's device as a reason for the combination, and we must evaluate Petitioner's contention. Moreover, any relative lack of improvement or benefits must be weighed against any problems the alternative method would introduce. *See Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 795–96 (Fed. Cir. 2021) (noting that simultaneous advantages and disadvantages to a proposed combination must be analyzed to determine whether the disadvantages "outweighed any reason

to combine”). Here, as discussed above in more detail with respect to the ground based on Watanabe, the evidence shows that one of ordinary skill in the art would have expected Watanabe’s bonding temperature of 900–1000° C to damage the electronic devices in an underlying substrate. Ex. 2029 ¶¶ 75–76; Ex. 2028, 123:13–124:7; Ex. 2027, 715. The expected damage to Lee’s device, when balanced against the limited evidence of a benefit to the combination,⁷ outweighs the reason to combine Lee and Watanabe set forth in the Petition. Accordingly, Petitioner does not demonstrate by a preponderance of the evidence that claim 13 would have been obvious over Lee and Watanabe.

2. Analysis – Claims 14 and 15

Claims 14 and 15 both depend directly from independent claim 13. Ex. 1001, 12:35–42. Petitioner’s arguments with respect to claims 14 and 15 do not remedy the deficiencies noted above with respect to independent claim 13. Pet. 73. Accordingly, Petitioner does not demonstrate by a preponderance of the evidence that these claims would have been obvious over Lee and Watanabe.

1. Claims 16 and 17 over Lee, Watanabe, and Endoh

Claim 16 depends directly from claim 13, and claim 17 depends indirectly from claim 13. Ex. 1001, 12:44–52. Petitioner contends the subject matter of claims 16 and 17 would have been obvious over the combined disclosures of Lee, Watanabe, and Endoh. Pet. 73–74.

⁷ For example, it is unclear how improved wiring between the memory cells and the devices in the substrate, or lower wiring resistance, would be beneficial if the devices in the substrate are destroyed or damaged by the proposed bonding method.

Petitioner's arguments in this ground, however, do not remedy the deficiencies noted above with respect to the combination of Lee and Watanabe. *Id.* Accordingly, Petitioner does not demonstrate by a preponderance of the evidence that challenged claims 16 and 17 would have been obvious over Lee, Watanabe, and Endoh.

IV. PATENT OWNER'S MOTION TO STRIKE

Patent Owner moves to strike Exhibits 1033, 1035, 1041 (¶¶ 12–70), 1047–1050, 1052–1055, and portions of Petitioner's Reply. Mot. 1–10. Petitioner opposes. Opp. 1–10.

Patent Owner contends Petitioner presents new arguments and evidence related to Watanabe and Endoh in its Reply that should have been in the Petition. Mot. 3–8. Patent Owner also contends that Petitioner raises new claim construction arguments, along with new exhibits and expert testimony regarding claim construction, that should have been in the Petition, and not presented for the first time in the Reply. *Id.* at 8–10. We address these arguments below.

A. New Theories

Patent Owner contends that Petitioner presents new theories and supporting evidence for the first time on reply relating to EMIH heating, mechanical alignment, and DRAM embodiments in Watanabe. Mot. 3–7. Patent Owner further contends that Petitioner's Reply relies on a new unpatentability theory regarding Endoh and improperly seeks to recant Dr. Lee's testimony regarding Lee's disclosures. *Id.* at 6–8.

Having considered this evidence and arguments, we found in favor of Patent Owner.⁸ Thus, Patent Owner’s motion to strike allegedly new arguments and evidence related to Watanabe, Endoh, and Lee is dismissed as moot.

B. Claim Construction Arguments

Patent Owner contends Petitioner in its Reply improperly provides claim constructions related to “stackable add-on layer” and “SOI pillar,” as well as three new exhibits (Exs. 1033, 1035, 1060) and twelve paragraphs of new declaration testimony (Ex. 1041 ¶¶ 12–33), that should have been provided in the Petition. Mot. 8–9. Patent Owner also contends that Petitioner relied upon new testimony from Dr. Lee regarding the application of its new claim construction arguments to its unpatentability theories relating to Endoh. *Id.* at 9 (citing Ex. 1041 ¶¶ 60–63, 67–69).

With respect to “stackable add-on layer,” Patent Owner contends that Petitioner and Dr. Lee understood that this term would be determinative for some grounds but waited until the Reply to provide an express construction. Mot. 8. And, because the claim construction arguments were not raised in the Petition, Patent Owner contends Petitioner’s new constructions provided for the first time in reply should be stricken. *Id.* at 8–9; Sur-reply 4

⁸ We agree that Petitioner’s reply arguments with respect to implementing the structure depicted in Figure 7 of Watanabe in Figure 2A is a new theory. The more appropriate course, however, is for us to not consider this new theory, as opposed to striking it from the record. Patent Trial and Appeal Board Consolidated Trial Practice Guide November 19, at 80 (explaining that the Board is capable of identifying and disregarding “any new issues or belatedly presented evidence that exceeds the proper scope of reply or sur-reply”). In any event, for the reasons discussed above, even if we considered this argument, Patent Owner would still prevail.

("[Petitioner's] arguments plainly exceed the proper scope of reply under Board rules."). According to Patent Owner, Petitioner's new claim construction theories prejudice Patent Owner because Patent Owner's only vehicle to respond is an abbreviated sur-reply with no opportunity to present new evidence. Mot. 9–10. We are not persuaded by Patent Owner's arguments.

First, the Petition in fact recognized that the proper construction of "stackable add-on layer" could be in dispute and provided Petitioner's general understanding as to the scope of the claim term. Pet. 6 n.2. The Petition also recognized that the term "stackable add-on layer" might be construed to permit direct deposition of each layer of memory on the substrate or insulating layer, and asserted that the challenged claims were unpatentable under either Petitioner's or Patent Owner's construction of the term. *Id.* at 12, 13 n.3, 16–21, 48 n.5. Thus, both the Board and Patent Owner were on notice as to how Petitioner was interpreting the term "stackable add-on layer" and how Petitioner was applying this construction to the prior art challenges.

The Institution Decision generally adopted Petitioner's understanding of the term "stackable add-on layer" and identified intrinsic evidence supporting this construction. Inst. Dec. 7–9. The Institution Decision also encouraged the parties to expressly construe the term with citation to intrinsic evidence. *Id.* at 9 n.5. Petitioner provided a construction of "stackable add-on layer" at its next available opportunity, supporting its construction with citations to intrinsic evidence. Pet. Reply 4–9; Opp. 3–4. Contrary to Patent Owner's arguments, there is nothing improper with Petitioner providing a requested claim construction in its Reply, or in relying

on new evidence to support that construction, so long as Patent Owner has an adequate opportunity to respond.

For example, in *Hamilton Beach Brands, Inc. v. F'real Foods, LLC*, 908 F.3d 1328, 1338–1339 (Fed. Cir. 2018), the court noted that it was acceptable for the Board to address a claim construction not raised in the Petition, so long as both parties had notice of the contested claim construction issues and an opportunity to respond. And in *Rembrandt Diagnostics, LP v. Alere, Inc.* 76 F.4th 1376, 1383–84 (Fed. Cir. 2023), the court noted that a petitioner is entitled to respond to arguments raised in a “decision on institution” and that the introduction of new evidence during the course of the trial is both to be expected and permissible, “as long as the opposing party is given notice of the evidence and an opportunity to respond.” *Id.* (quoting *Genzyme Therapeutic Prods. Ltd. P'ship v. Biomarin Pharm. Inc.*, 825 F.3d 1360, 1366 (Fed. Cir. 2016)).

Patent Owner had multiple opportunities to provide a construction of the term “stackable add-on layer,” and at least one opportunity to address Petitioner’s reply evidence, but chose not to. Paper 6, 13 (Preliminary Response); PO Resp. 12–13 (asserting that Patent Owner disagrees with the Board’s construction, but electing not to provide its own construction of “stackable add-on layer”); PO Sur-reply 4. Moreover, to the extent Patent Owner felt it required the opportunity to rely on additional evidence in its Sur-reply, it could have requested the Board provide such an opportunity. *See ZyXel Commc’ns Corp. v. UNM Rainforest Innovations*, 107 F.4th 1368, 1382–83 (Fed. Cir. 2024) (noting that a patent owner may request that the Board waive its rule against submitting new evidence with a sur-reply). Instead, Patent Owner chose to avoid engaging in the construction of

“stackable add-on layer” altogether. *See id.* (noting that the patent owner did not identify any evidence it would have provided in the sur-reply had it been given a chance).

In view of the foregoing, we determine that Patent Owner had an adequate opportunity to address the proper construction of “stackable add-on layer” and to address Petitioner’s construction of this term, but simply chose not to. Accordingly, Patent Owner’s request to strike Petitioner’s construction of “stackable add-on layer,” Petitioner’s “unpatentability theories based on them,” and Exhibits 1033, 1035, 1060, and 1047 ¶¶ 12–23, is denied.⁹

With respect to “SOI pillar,” Patent Owner contends Dr. Lee testified under cross-examination that he did not know the “plain and ordinary meaning” of “pillar,” but provided a new construction of this term on reply, along with ten paragraphs of new testimony and four new exhibits. Mot. 8–9. For the reasons set forth above, for purposes of resolving the controversy, we need not address the proper construction of “SOI pillar” or rely on any of Petitioner’s arguments with respect to this term. Accordingly, Patent Owner’s request to strike Petitioner’s construction of “SOI pillar” and the identified documents is dismissed as moot.

⁹ We note that Petitioner’s arguments with respect to the “stackable add-on layer” remained the same throughout this proceeding, i.e., that Watanabe discloses this limitation under either parties’ potential construction and Lee discloses the limitation under Patent Owner’s apparent construction of the term (permitting direct deposition).

V. CONCLUSION

For the foregoing reasons, we determine that Petitioner fails to demonstrate by a preponderance of the evidence that claims 13–17 are unpatentable. Our conclusions are summarized in the following table.

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
13	103(a)	Watanabe		13
14–17	103(a)	Watanabe, Endoh		14–17
13–15	103(a)	Lee		13–15
16, 17	103(a)	Lee, Endoh		16, 17
13–15	103(a)	Lee, Watanabe		13–15
16, 17	103(a)	Lee, Watanabe, Endoh		16, 17
Overall Outcome				13–17

ORDER

For the foregoing reasons, it is:

ORDERED that Petitioner does not demonstrate that any challenged claim of the '702 patent is unpatentable;

FURTHER ORDERED that Patent Owner's Motion to Strike is denied with respect to the proper construction of "stackable add-on layer" and Exhibits 1033, 1035, 1060, and 1047 ¶¶ 12–23, and dismissed as moot with respect to all other issues; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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