IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:	Cloutier et al.	
U.S. Patent No.:	6,920,527	Attorney Docket No.: 36144-0035IP1
Issue Date:	July 19, 2005	
Appl. Serial No.:	10/364,583	
Filing Date:	February 11, 2003	
Title:	PORTABLE RAM DRIVE	

DECLARATION OF DAVID KUAN-YU LIU, Ph.D.

I, David Kuan-Yu Liu, Ph.D., of Fremont, CA, declare that:

I. ASSIGNMENT

1. I have been retained as a technical expert by counsel on behalf of Micron Technology, Inc. ("Micron" or "Petitioner"). I understand that Micron is requesting that the Patent Trial and Appeal Board ("PTAB" or "Board") institute an *inter partes* review ("IPR") proceeding of U.S. Patent No. 6,920,527 ("the '527 patent") (MTI-1001).

2. I have been asked to provide my independent analysis of the '527 patent in light of the prior art publications cited below.

3. I am not currently an employee of Micron. I received no compensation for this declaration beyond my normal hourly compensation based on my time actually spent analyzing the '527 patent, the prior art publications cited below, and the issues related thereto, and I will not receive any added compensation based on the outcome of any IPR or other proceeding involving the '527 patent.

II. QUALIFICATIONS

4. A summary of my background and qualifications as a technical expert for this case is provided below. A complete listing of my qualifications and background are detailed in my curriculum vitae ("CV"), which is attached hereto as Appendix A. Among other things, my CV includes a list of my issued patents and publications for at least the last 30 years. My curriculum vitae also includes information about my expert witness experience, with case numbers where available.

5. I received a Bachelor of Science in Electrical Engineering from the University of California, Berkeley, in 1983. I received a Master of Science and Ph.D. degrees in Electrical Engineering from Stanford University in 1985 and 1989, respectively.

6. From 1989 to 1992, I was a member of technical staff at Texas Instruments, Inc. At Texas Instruments, I researched and developed the 16Mb generation of Flash EPROM technology, as well as a new generation of antifuse-based Field Programmable Gate Arrays (FPGAs). My job responsibilities at Texas Instruments also included process integration, device modeling, high-voltage CMOS process integration, and investigating novel source-side injection mechanisms for Flash EPROM channel hot-electron programming.

7. From 1992 to 1995, I was a member of the technical staff at Advanced Micro Devices, Inc. (AMD) where I was a key contributor in optimizing Flash cell

and periphery devices in AMD's CMOS-based 0.5 μm and 0.35 μm Flash EPROM technology. My job responsibilities at AMD also included process integration, device modeling, and development of triple-well process technology for accommodating x-decoder transistors and high voltage transistors for negative gate erase operation. While at AMD, I was awarded a Spotlight Award for developing a method of manufacturing a self-aligned source (SAS) etch for a NOR flash memory that involved utilizing a spacer on the stacked gate edge to improve the tunnel oxide integrity and source junction implant profile.

8. I spent the next five years of my career in managerial and director roles at several California-based semiconductor companies. I was responsible for increasing yield and for leading teams of engineers working to develop next-generation memory devices.

9. In 2000, I co-founded Progressant Technologies in Fremont, California. Progressant Technologies developed IP for negative differential resistance transistor technology and was eventually acquired by Synopsys, Inc.

10. From 2000 to 2004, I was a Senior Manager at Xilinx, Incorporated, where I was responsible for developing nonvolatile memory process technology for flash and CPLD product applications, as well as advanced CMOS process technology (specifically 75nm CMOS technology node, a half node version between 90nm and 65nm).

11. From 2004 to 2007, I was a Senior Scientist at Maxim Integrated Products where I was responsible for developing Embedded Non-volatile Memory process technology for Power Management product applications.

12. In 2009, I incorporated Jonker, Inc. to develop a set of intellectual property on zero-cost Embedded Flash Memory devices. Tessera Technologies, Inc. eventually acquired Jonker, Inc.'s intellectual property in 2011.

13. Since 2007, I have served as a technical consultant where I have provided expert advice regarding memory technology including Flash memory, CMOS process technology, and semiconductor device physics.

14. I have over 25 years of experience as an engineer and engineering manager/director of Complementary Metal Oxide Semiconductor (CMOS) technology development, with an emphasis on memory technology development. During my career, I have worked at some of the leading technology companies in the world, such as Texas Instruments, Advanced Micro Devices, Altera Corporation (now a subsidiary of Intel Corp.), and Xilinx. At these companies, my work focused on various aspects of CMOS and semiconductor technology.

15. I hold over 95 U.S. patents, a vast majority of which are directly related to memory device technology. For example, U.S. Patent Nos. 5,814,854 and 5,751,631 relate to NAND flash memory device structure and the method of sensing the content of such memory.

16. I have authored several technical papers that have been published in well-respected, peer-reviewed journals, such as the IEEE Electron Device Letters, the IEEE Journal of Solid-State Circuits, and the IEEE Transactions on Electron Devices. I am also the author of several technical papers published in one of the most respected technical conferences in the semiconductor field, the *International Electron Devices Meeting Technical Digest*, such as a "Short Channel Enhanced Degradation During Discharge of Flash Memory Cell" and "Optimization of a Source-side Injection FAMOS Cell for Flash EPROM Applications."

17. Taken as a whole, my academic and practical experience have given me a substantial basis upon which to evaluate the technology that is in question in the claims of the '527 patent. Based on my experience and education, I believe that I am qualified to opine as to the knowledge and level of skill of one of ordinary skill in the art at the time of the alleged invention of the '527 patent (which I further describe below) and what such a person would have understood at that time, and the state of the art during that time. Based on my above-described experience relating to data storage and electronic memory devices, and the acceptance of my publications and professional recognition by peers in my field, I believe that I am qualified to be an expert in the above described area of the '527 patent.

III. LEGAL PRINCIPLES

18. In forming my analysis and conclusions expressed in this declaration, I have applied the legal principles described in the following paragraphs, which were provided to me by counsel for the Petitioner.

A. Anticipation

19. It is my understanding that invalidation by "anticipation" exists only if a single alleged prior art reference discloses each and every limitation of the claim at issue, either expressly or inherently. In other words, every limitation of the claim must appear in a single prior art reference for the reference to anticipate that claim. I also understand that all elements of the claim must be disclosed in the reference as they are arranged in the claim. I also understand that to be considered anticipatory, the prior art reference must be enabling and must describe the patentee's claimed invention sufficiently to have placed it in the possession of a person of ordinary skill in the field of invention. Under the principles of inherency, I understand that if the prior art necessarily functions in accordance with or includes the claimed limitations, it anticipates.

20. I have been informed that a claim is invalid if the claimed invention was known or used by others in the U.S., or was patented or published anywhere, before the Applicant's invention. I further have been informed that a claim is invalid if the invention was patented or published anywhere, or was in public use, on sale,

or offered for sale in this country, more than one year prior to the filing date of the patent application (critical date). I have also been informed that a claim is invalid if an invention described by that claim was described in a U.S. patent granted on an application for a patent (or in a published application for a U.S. patent) that was filed by another in the U.S. before the date of invention for such a claim.

21. I understand that a dependent claim contains all of the limitations of the independent claim from which it depends. Thus, to establish anticipation, every limitation set forth in a dependent claim as well as the independent claim from which it depends must be found in an anticipatory reference.

B. Obviousness

22. I have been informed that a patent claim is invalid as "obvious" in light of one or more prior art references if it would have been obvious to a person of ordinary skill in the art at the time of the alleged invention ("POSITA"), taking into account (1) the scope and content of the prior art, (2) the differences between the prior art and the claims, (3) the level of ordinary skill in the art, and (4) any so called "secondary considerations" of non-obviousness, which include: (i) "long felt need" for the claimed invention, (ii) commercial success attributable to the claimed invention, (iii) unexpected results of the claimed invention, and (iv) "copying" of the claimed invention by others. I understand that a patent cannot be properly granted for subject matter that would have been obvious to a POSITA at the time of

the alleged invention, and that a patent claim directed to such obvious subject matter is invalid under 35 U.S.C. § 103. It is also my current understanding that in assessing the obviousness of claimed subject matter one should evaluate obviousness over the prior art from the perspective of a POSITA at the time the invention was made (and not from the perspective of either a layman or a genius in that art).

23. While I do not know the exact date that the alleged invention claimed in the '527 patent was made, I do know that the '527 patent was filed on February 11, 2003 (MTI-1001, Cover Page). For purposes of my analysis here, I have applied a date of February 11, 2003 as the date of the alleged invention in my obviousness analysis, although in many cases the same analysis would hold true even if the date of the alleged invention occurred earlier than February 11, 2003 (especially given the earlier publication or filing dates of the cited prior art references).

24. I have been informed that a claim can be obvious in light of a single prior art reference or multiple prior art references. To be obvious in light of a single prior art reference or multiple prior art references, there must be a reason that would have prompted a POSITA to modify the single prior art reference, or combine two or more references, in a manner that provides the elements of the claimed invention. This reason may come from a teaching, suggestion, or motivation to combine, or may come from the reference(s) themselves, the knowledge or "common sense" of a POSITA, or from the nature of the problem to be solved, and this reason may be

explicit or implicit from the prior art as a whole. I have been informed that, under the law, the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand it is improper to rely on hindsight in making the obviousness determination.

C. Claim Construction

25. I understand that, for purposes of my analysis in this IPR proceeding, the terms appearing in the patent claims should be interpreted according to their "ordinary and customary meaning." In determining the ordinary and customary meaning, the words of a claim are first given their plain meaning that those words would have had to a POSITA. I understand that the structure of the claims, the specification, and the file history also may be used to better construe a claim insofar as the plain meaning of the claims cannot be understood. Moreover, treatises and dictionaries may be used, albeit under limited circumstances, to determine the meaning attributed by a person of ordinary skill in the art to a claim term at the time of filing. I have followed this approach in my analysis, and for all of the claim terms considered in this declaration, I have applied the plain and ordinary meaning of those terms.

26. I also understand that the words of the claims should be interpreted as they would have been interpreted by a POSITA at the time the alleged invention was made (not today). Because I do not know at what date the alleged invention was

made, I have used the date of February 11, 2003 for reasons explained in ¶23 above. However, the plain meanings/interpretations that I employed in my analysis below would have also been correct if the date of invention was anywhere within the late 1990s to early 2000s.

IV. PERSON OF ORDINARY SKILL IN THE ART

27. Based on my knowledge and experience in the field and my review of the '527 patent and its file history, and my first-hand knowledge of undergraduate electrical engineering curricula at the time of the '527 patent filing in February 2003, I believe a person of ordinary skill in the art ("POSITA") at the time of the earliest possible priority date of the '527 patent would have had a Bachelor of Science in electrical engineering, computer engineering, computer science, or a related discipline, with at least 2 years of experience in a field related to data storage and electronic memory devices. Additional education, e.g., a doctorate in electrical engineering, computer engineering, computer science, or a related discipline, might substitute for some of the experience, and substantial experience might substitute for some of the educational background. I understand that a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

V. MATERIALS CONSIDERED

28. My analyses set forth in this declaration are based on my experience in the field of data storage and electronic memory devices. Based on my above-described experience in the field, I believe that I am considered to be an expert in the field. Also, based on my experience, I understand and know of the capabilities of persons of ordinary skill in this field during the late 1990s to early 2000s and specifically during the time before the filing date (February 11, 2003) for the '527 patent, and I taught, participated in organizations, and worked closely with many persons of such skill level in the field during that time frame.

29. As part of my independent analysis for this declaration, I have considered the following: the background knowledge/technologies that were commonly known to persons of ordinary skill in this field during the time before the filing date for the '527 patent; my own knowledge and experiences gained from my work experience in the field of data storage and electronic memory device development and fabrication generally; my experience in teaching and advising others in such subjects; and my experience in working with others involved in the field of data storage and electronic memory devices or similar fields. In addition, I have analyzed the following publications and materials:

- U.S. Patent No. 6,920,527 to Cloutier et al. ("the '527 patent") (MTI-1001) and its accompanying prosecution history (MTI-1002)

- U.S. Patent Application Publication No. 2003/0028733 to Tsunoda et al. ("Tsunoda") (MTI-1004)
- U.S. Patent No. 7,069,370 to Sukegawa et al. ("Sukegawa") (MTI-1005)
- Certified translation and original document of Japanese Published Patent Application No. 2001-005723 to Tomio Suzuki ("Tomio") (MTI-1006)
- Certified translation and original document of Japanese Published Patent Application No. 2000-112836 to Shigeo Suzuki ("Shigeo") (MTI-1007)
- U.S. Patent No. 6,353,870 to Mills et al. (MTI-1008)
- U.S. Patent No. 6,539,623 to Chen (MTI-1009)
- U.S. Patent No. 6,376,283 to Chen (MTI-1010)
- Acrylonitrile Butadiene Styrene (ABS), Dynalabcorp.com, https://web.archive.org/web/20031118100126/http://dynalabcorp.com/technical_info_abs.asp (MTI-1011)
- U.S. Patent Publication No. 2002/0010827 to Cheng (MTI-1012)
- U.S. Patent Publication No. 2002/0147882 to Pua et al. (MTI-1013)
- Plastic Products for UL-94 Flame Class, Polymershapes.com, https://www.polymershapes.com/regulatory/ul-94-flame-class/ (MTI-1014)
- UL 94 Classification and Flame-Retardant Thermoplastics, Protolabs.com, https://www.protolabs.com/resources/blog/flame-retardant-thermoplastics-and-ul-classifications/ (MTI-1015)

- Common DIMM Memory Form Factors, Simmtester.com, https://www.simmtester.com/News/PublicationArticle/168 (MTI-1016)
- U.S. Patent No. 6,567,273 to Liu et al. (MTI-1017)
- U.S. Patent Application Publication No. 2004/0017634 to Chin-Lung et al. (MTI-1018)
- U.S. Patent No. 6,490,163 to Pua et al. (MTI-1019)
- U.S. Patent Application Publication No. 2004/0017637 to Chang et al. (MTI-1020)
- Complaint For Patent Infringement Against Micron Technology, Inc. in *Sonrai Memory Ltd. v. Micron Technology, Inc.*, Case No. 6:22-cv-00855 (W.D. Tex. Aug. 2022) (MTI-1021)
- U.S. Patent No. 5,887,145 to Harari et al. (MTI-1022)
- Excerpt of Callister, "Materials Science and Engineering, An Introduction," Fifth Edition, John Wiley & Sons, Inc. (2000) (MTI-1023)
- M.2 SSD, TechTarget.com, https://www.techtarget.com/searchstorage/definition/M2-SSD (MTI-1024)

30. Although for the sake of brevity this Declaration refers to selected portions of the cited references, it should be understood that one of ordinary skill in the art would have viewed the references cited herein in their entirety, and in combination with other references cited herein or cited within the references

themselves. The references used in this Declaration, therefore, should be viewed as being incorporated herein in their entirety.

VI. BACKGROUND INFORMATION

A. Background of the Technology

31. Computer memories can be classified as volatile and non-volatile. MTI-1022, 1:21-55. Volatile memories, such as DRAM, SRAM, SDRAM, and DDR-SDRAM, only store data while powered by the system they are in, and lose the data stored therein when the power is turned off. MTI-1004, [0075]; MTI-1006, [0002]; MTI-1007, [0010]; MTI-1022, 1:21-55; MTI-1013, [0005]. Non-volatile memories retain their stored data even without power. MTI-1022, 1:21-55; MTI-1013, [0005]. Examples of non-volatile memories and memory systems include magnetic tape, magnetic and optical drives, read only memories (ROMs), electrically programmable read only memories (EPROMs), and electrically erasable programmable read-only memories (EEPROMs). MTI-1022, 1:21-55.

B. Overview of the ’527 Patent

32. The ’527 patent discloses a portable RAM drive in which data is stored on a non-volatile memory and transferrable to a volatile memory when the portable RAM drive is coupled to a computer system for faster access by the computer system. MTI-1001, Abstract. Portable storage media for computer systems were already known in the art at the time of the ’527 patent, and had been used for purposes like backing up a user’s critical data. MTI-1001, 1:11-15. According to

the ’527 patent, however, the prior art media had drawbacks, such as small capacity and slow speed (e.g., floppy disks), or limited ability to modify data (e.g., compact discs). MTI-1001, 1:15-23. Such prior art portable media could also be relatively large and easily damaged, as in the case of floppy disks, CDs, or other non-volatile memory devices. MTI-1001, 1:25-28.

33. To solve these purported problems, the ’527 patent discloses a portable RAM drive comprising “a housing, a memory controller, a volatile memory, a nonvolatile memory, and a connector to connect the portable RAM drive to the computer system.” MTI-1001, 1:42-45. The non-volatile memory stores data when the portable RAM drive is not connected to a computer system, and the data is transferred to the volatile memory when the portable RAM drive is plugged into the computer system for faster access. MTI-1001, 1:45-54. If the portable RAM drive is unplugged from the computer system, an internal power source powers the portable RAM drive long enough to transfer data from the volatile memory (i.e., RAM) to the non-volatile memory. MTI-1001, 1:54-58.

C. Prosecution History of the ’527 Patent

34. As part of my preparation of this declaration, I reviewed the prosecution history of the ’527 patent (MTI-1002). I understand that Application No. 10/364,583, which led to the ’527 patent, was filed on February 11, 2003. MTI-

1001, cover page. I also understand that the '527 patent was issued on July 19, 2005. *Id.*

35. The application that led to the '527 patent was initially filed with 20 claims. MTI-1002, 16-20. On March 10, 2005, the Examiner issued a notice of allowance with the following reasons for the indication of allowance:

> ***Reasons for Allowance***
>
> 1. The following is an examiner's statement of reasons for allowance: the prior art of record does not teach a portable memory device which connects to a computer system with the portable memory device comprising a memory controller, a volatile memory and a non-volatile memory with the memory controller copying data from the non-volatile memory to the volatile memory for the computer system to access through the connector.

MTI-1002, 43-47.

36. However, as I demonstrate in my detailed analysis of the references below, these features that were alleged to have been missing from the references cited during prosecution were known in other prior art memory devices.

D. Interpretations of the '527 Patent Claims at Issue

37. I understand that, for purposes of my analysis in this IPR proceeding, the terms appearing in the patent claims should be interpreted according to what is referred to as the "*Phillips*" standard. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R. § 42.100. I further understand that the words of the claims should be given their plain meaning unless that meaning is inconsistent with the

patent specification or the patent's history of examination before the Patent Office. I also understand that the words of the claims should be interpreted as they would have been interpreted by a POSITA at the time of the invention (not today). Without further information on what date the invention as claimed was made, I have used the earliest possible priority date of the '527 patent as the point in time for claim interpretation purposes. That date was February 11, 2003.

VII. OVERVIEW OF CONCLUSIONS FORMED

38. I have reviewed the Petition for IPR of the '527 patent, and agree with the analysis contained therein. In summary, it is my opinion that each and every limitation of each and every challenged claim would have been at least obvious to one of ordinary skill in the art at the time of the alleged invention in view of the prior art cited in the Petition and further explained in this declaration. To summarize my conclusions below:

- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 1, 6, 9, 11-12, and 14-15 of the '527 patent are rendered obvious by Tsunoda.
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 2-5 and 16-17 of the '527 patent are rendered obvious by Tsunoda in view of Tomio.
- Based upon my knowledge and experience and my review of the prior art

publications listed above, I believe that claims 13 and 20 of the ’527 patent are rendered obvious by Tsunoda in view of Tomio and Shigeo.

- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 1, 6-7, 9-12, 14-15, and 18 of the ’527 patent are rendered obvious by Tsunoda in view of Sukegawa.
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 2-5 and 16-17 of the ’527 patent are rendered obvious by Tsunoda in view of Sukegawa and Tomio.
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 13 and 20 of the ’527 patent are rendered obvious by Tsunoda in view of Sukegawa, Tomio, and Shigeo.
- Based upon my knowledge and experience, my review of the prior art publications listed above, and my review of Patent Owner’s complaint for infringement, I believe that claims 1-6, 9, 12, and 15-17 of the ’527 patent are rendered obvious by Tomio.
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 13 and 20 of the ’527 patent are rendered obvious by Tomio in view of Shigeo.
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 1-7, 9-12, and 14-18 of the

’527 patent are rendered obvious by Tomio in view of Sukegawa.

- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 13 and 20 of the ’527 patent are rendered obvious by Tomio in view of Sukegawa and Shigeo.

VIII. ANALYSIS OF THE PRIOR ART

A. Analysis of Tsunoda with respect to Claims 1, 6, 9, 11-12, and 14-15

39. For the reasons articulated in detail below, and based on my review of the ’527 patent and the Tsunoda reference, I am confident that a POSITA would have readily understood that Tsunoda renders obvious all elements of claims 1, 6, 9, 11-12, and 14-15.

1. Overview of Tsunoda

40. Tsunoda relates to “a memory apparatus, which uses a volatile memory and a nonvolatile memory.” MTI-1004, [0001]. Tsunoda describes “a configuration example of the memory apparatus” in conjunction with FIG. 24 (below). MTI-1004, [0035]. The “memory apparatus 4000 shown in FIG. 24 can be mounted on an information terminal such as a portable telephone set, personal digital assistants (PDA), a music player, a digital camera, a digital video camera, a set top box, a personal computer, or a car navigation system.” MTI-1004, [0038]. The “host 4040 is an information processor such as a CPU or ASIC incorporated in the information terminal.” MTI-1004, [0040]. “The host 4040 can operate based on the operation

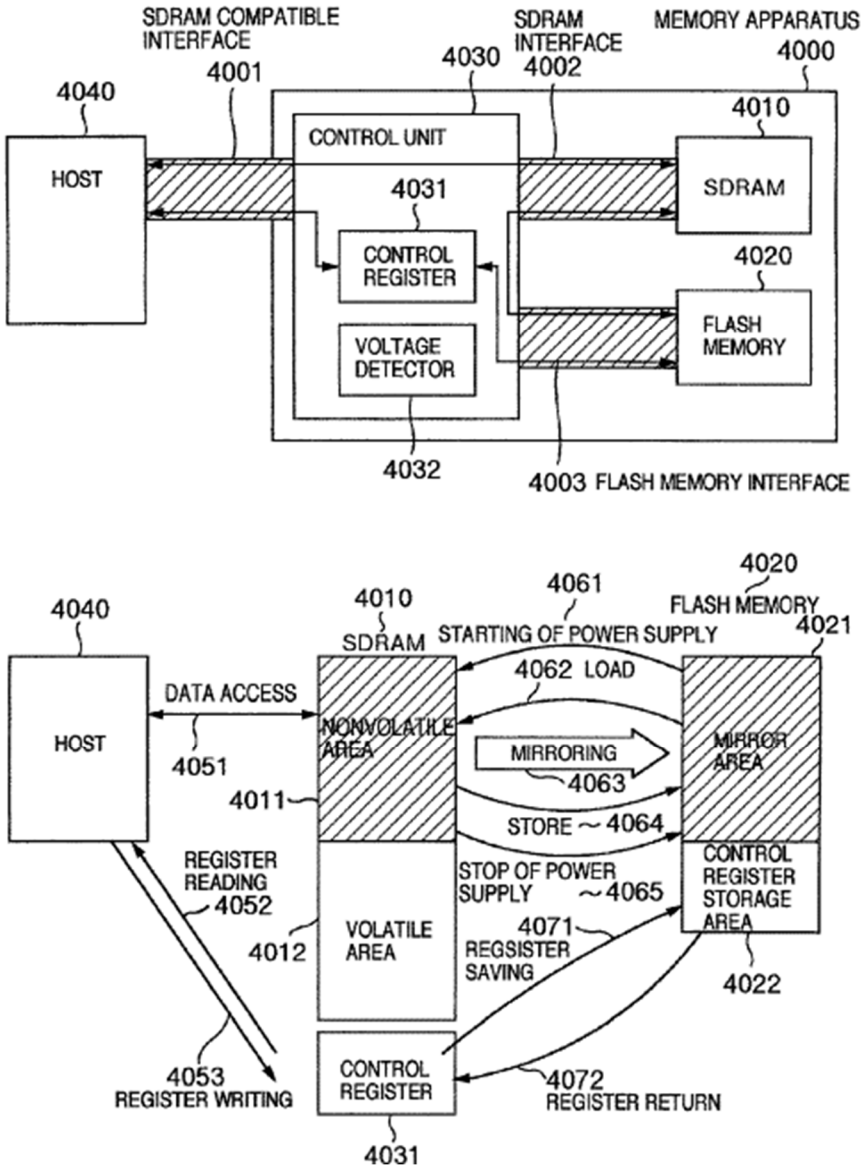
programs stored in the memory apparatus 4000 by using the memory apparatus 4000 as a main memory." MTI-1004, [0041]. "In the memory apparatus 4000, various data for processing by, for example, the operation programs, can also be stored." *Id.* In Tsunoda, "the data are various data such as a text, an image, a voice, a moving image and the like, or operation parameters/setting files of the programs" and "[o]ther data." *Id.*

41. The memory apparatus 4000 includes "an SDRAM 4010 to be accessed randomly, a flash memory 4020 as a nonvolatile memory, [and] SDRAM compatible interface 4001 for enabling the host 4040 to access the memory apparatus 4000." MTI-1004, [0042], [0060]-[0061], [0077], [0090]. Tsunoda's FIG. 24 is an "example of using the SDRAM compatible interface as the interface for interconnecting the memory apparatus 4000 and the host 4040," but Tsunoda discloses that "other interfaces... can be used." MTI-1004, [0094].

42. In FIG. 24, the "SDRAM 4010 and the control unit 4030 are connected to each other through an SDRAM interface 4002." MTI-1004, [0054]. "The control unit 4030 and the flash memory 4020 are connected to each other through a flash memory interface 4003." MTI-1004, [0055]. The control unit 4030 includes functionality for "relaying data transfer between the host [4040] and the SDRAM 4010," for "transferring the data held in the predetermined area of the SDRAM 4010 to a predetermined area of the flash memory 4020," and "transferring the data held

in the predetermined area of the flash memory 4020 to a predetermined area of the SDRAM 4010." MTI-1004, [0062]. The memory apparatus 4000 can be "an LSI package form" and includes "the SDRAM 4010, the flash memory 4020, and the control unit 4030 on different silicon chips, and interconnects terminals of the silicon chips by, for example wire bonding, thereby providing a multichip package, in which the components are sealed in one package." MTI-1004, [0056].

FIG.24



MTI-1004, FIG. 24

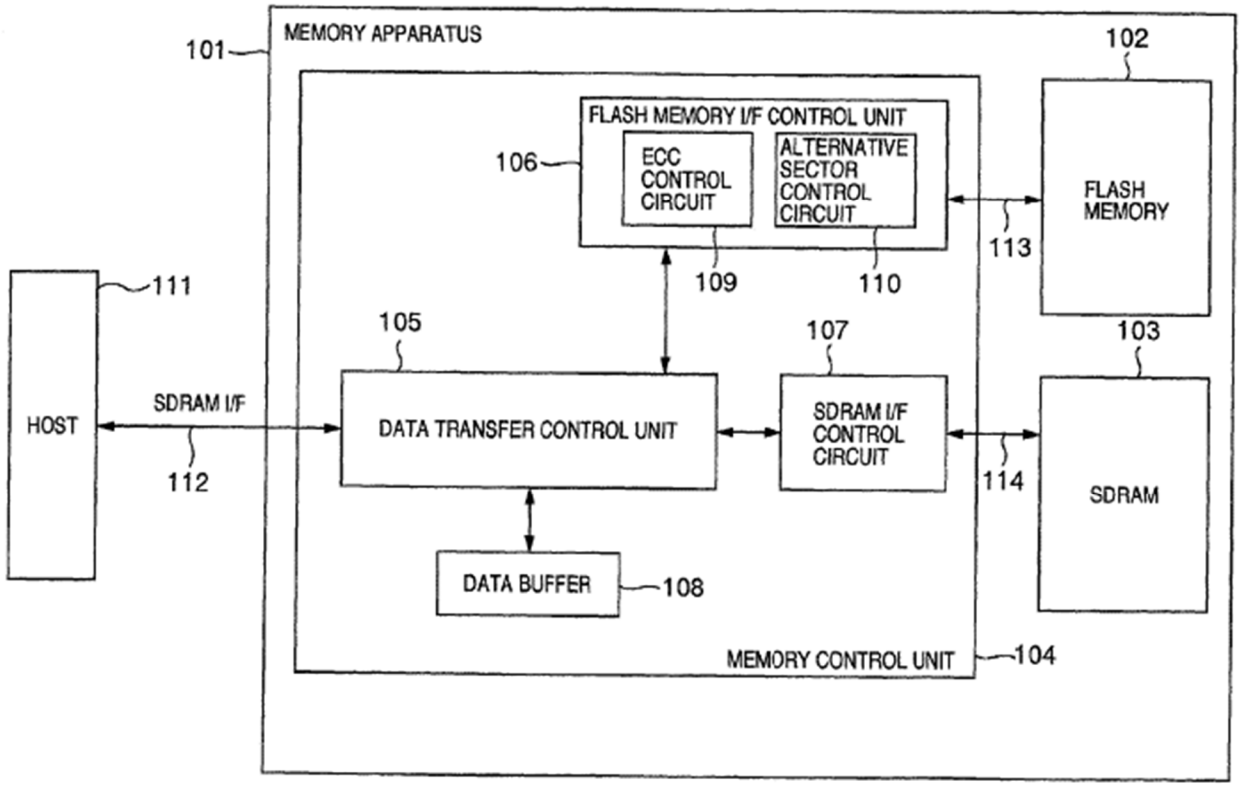
43. In Tsunoda, "the data of the flash memory 4020 is read to the SDRAM 4010 before the host 4040 accesses the memory apparatus 4000 after the power supply to the memory apparatus 4000 is started" so that "the host 4040 can use the memory apparatus 4000 as a nonvolatile SDRAM compatible memory." MTI-1004, [0042], [0048]-[0049], [0068], [0078], [0080]-[0084], FIG. 24 (4061-4062), FIG. 25

(4101-4105). While the host 4040 is connected to the memory apparatus 4000, "memory apparatus 4000 receives various SDRAM operation instructions of reading, writing, refreshing and the like from the host 4040 through the SDRAM [compatible] interface 4001" (MTI-1004, [0090]-[0092], FIG. 24 (4051), FIG. 26 (4201)), and "[t]he host 4040 of the memory apparatus 4000 can instruct the memory apparatus 4000 to transfer the data of the SDRAM 4010 to the flash memory 4020, and the data of the flash memory 4020 to the SDRAM 4010" (MTI-1004, [0043], [0046], [0048]-[0049], [0078], [0093], FIG. 24 (4062, 4064), FIG. 26 (4206)). Additionally, "the data of the SDRAM 4010 is stored in the flash memory 4020 before the power supply to the memory apparatus 4000 is stopped" to prevent "a data loss of the SDRAM 4010 caused by a stop of the power supply." MTI-1004, [0042], [0046]-[0047], [0068], [0078], [0085]-[0088], FIG. 24 (4064-4065), FIG. 25 (4107, 4109-4113).

44. In "a more specific embodiment of the memory apparatus 4000" shown in FIG. 1 (below), the "memory apparatus 101 includes a flash memory 102 as a nonvolatile memory, an SDRAM (synchronous SDRAM) 103 as a volatile memory, and a memory control unit 104 for controlling the memories." MTI-1004, [0096]. "The memory control unit 104 controls data transfer or the like between a host 111 and the memory apparatus 101, and between the flash memory 102 and the SDRAM 103 in response to a request from the host 111." *Id.* "The host 111 may be, for

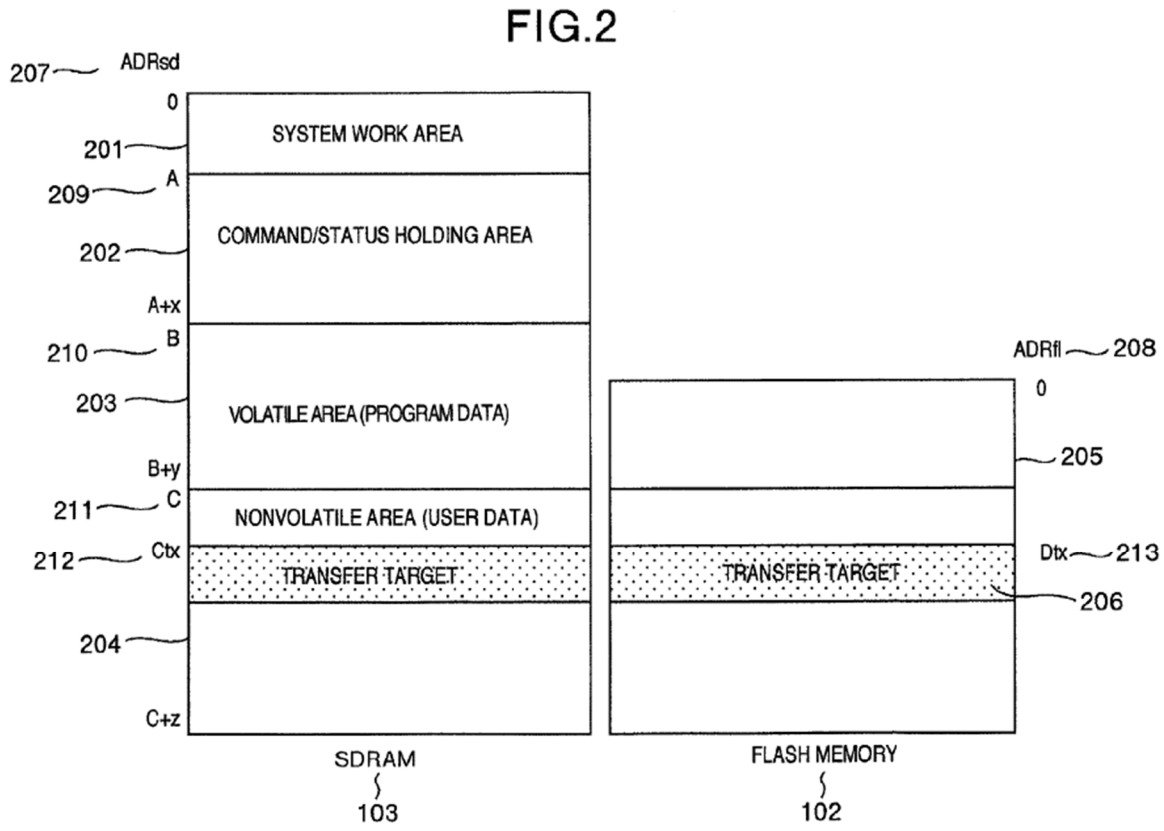
example a portable telephone set, a portable information terminal (PDA), a personal computer, a music player (recorder), a camera, a video camera, a set top box terminal or the like." *Id.*

FIG.1



MTI-1004, FIG. 1

45. Tsunoda's FIG. 2 (below) shows "an example of address spaces of the SDRAM and the flash memory 102." MTI-1004, [0098]. The address space of the SDRAM 103 includes a volatile area 203 and a nonvolatile area 204. *Id.*



MTI-1004, FIG. 2

46. "After the power is turned ON, program data on the flash memory 102 is copied to the volatile area 203 of the SDRAM [103], and the host 111 can use the program by accessing the volatile area 203 on the SDRAM 103." MTI-1004, [0099]. The volatile area 203 thus stores "information necessary for application processing by the host," and "content of the volatile area 203 is erased when power is turned OFF for the memory apparatus 101." MTI-1004, [0098]. Additionally, "user data on the flash memory 102 is copied to the nonvolatile area 204 of the SDRAM 103, and the host 111 can use the user data by accessing the nonvolatile area 204 on the SDRAM [103]." MTI-1004, [0099], [0131], [0139]-[0140], FIGS. 18, 23. The nonvolatile area 204 of the SDRAM 103 thus stores "information that must be held

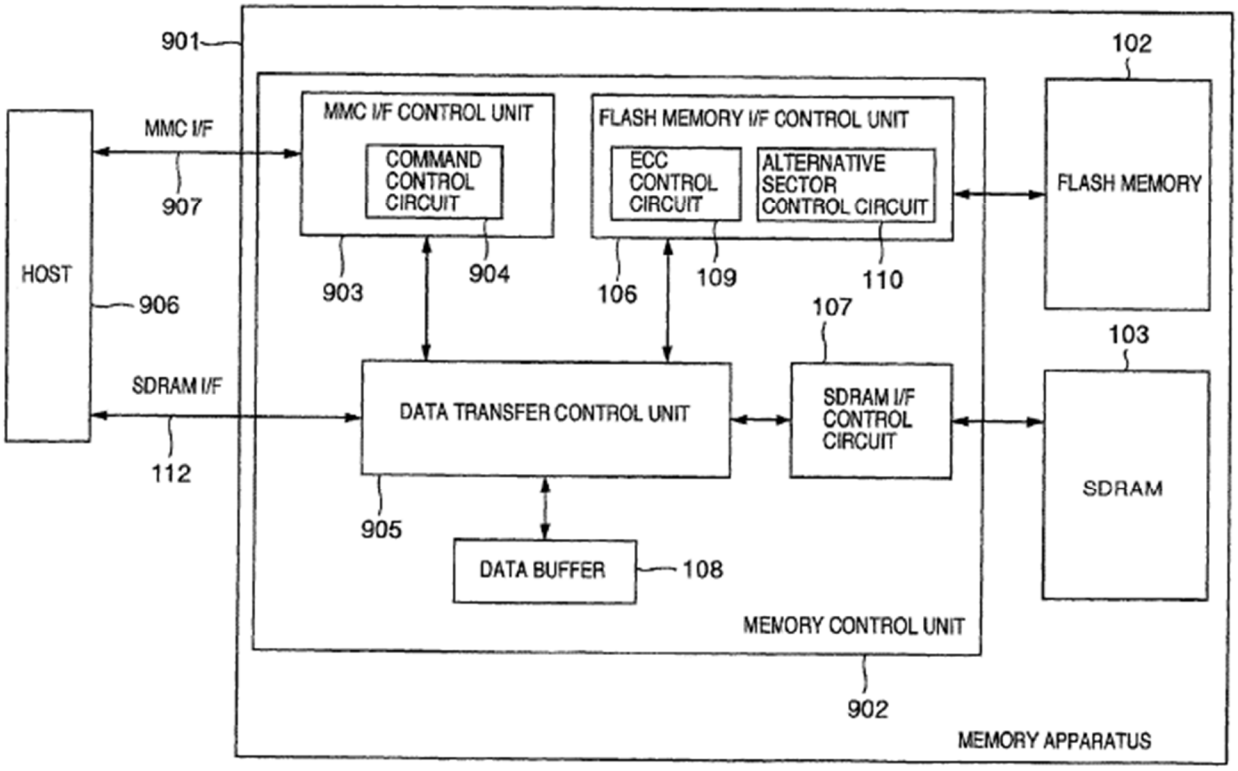
even after the power is turned OFF." MTI-1004, [0098]. Since the SDRAM 103 (and hence the nonvolatile area 204 of the SDRAM 103) is a volatile memory and is erased when power is turned OFF for the memory apparatus 101, "the information stored in the nonvolatile area 204 on the SDRAM 103 is copied to the flash memory 102 before the power is turned OFF, and held on the flash memory 102." MTI-1004, [0098], [0137]-[0138], FIG. 22. "The data written by the host is recorded in the SDRAM 103." MTI-1004, [0133]. "If the user data is slightly changed or contains an addition, the user data is copied to the flash memory 102, and held on the flash memory 102." MTI-1004, [0099], [0133]-[0136], FIGS. 20-21.

47. In Tsunoda, "functions for executing the foregoing processing steps are provided on the memory control unit 104 shown in FIG. 1." MTI-1004, [0104]. Tsunoda explains that "by executing the data transfer from the flash memory 102 to the SDRAM 103 according to the command from the host 111 beforehand, the host 111 can access data on the SDRAM 103 at a high speed," and "by transferring the data on the SDRAM 103 to the flash memory 102, the data can be held even after the power is turned off." MTI-1004, [0112].

48. In a second embodiment shown in FIG. 9 (below), a "memory apparatus 901 includes a MultiMediaCard (MultiMediaCard is a registered trade mark of Infineon Technologies AG, abbreviated to "MMC", hereinafter) interface 907" "as an interface for connection with a host 906, in addition to the SDRAM interface 112

shown in FIG. 1." MTI-1004, [0113]. "The MMC is a memory card using the flash memory 102 as a storage medium," and "the memory apparatus 901 includes a function as an MMC in addition to the foregoing data transfer between the memories." *Id.* In the FIG. 9 embodiment, "the host 906 including the MMC interface 907 and the SDRAM interface 112 can use the memory apparatus 901 not only as the high-speed volatile and nonvolatile memory but also as the MMC." MTI-1004, [0120]. Tsunoda discloses that its "invention is not limited to the foregoing MMC interface 907, but it can be applied to various interfaces" such as "interfaces of an SD card (small memory card having a width of 24 mm, a length of 32 mm, and a thickness of 2.1 mm, nine external terminals, and flash memory loaded), and a memory stick (registered trade mark of Sony Corporation)." MTI-1004, [0117].

FIG.9

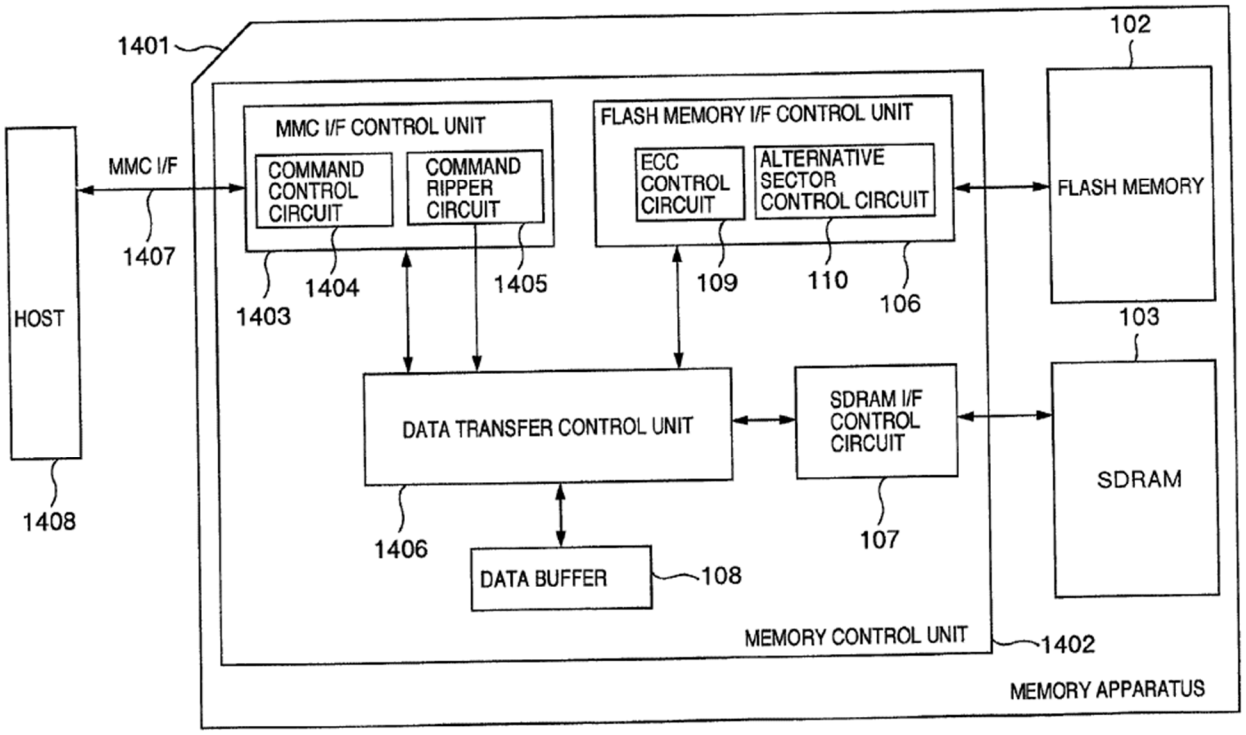


MTI-1004, FIG. 9

49. In a third embodiment shown in FIG. 14 (below), a "memory apparatus 1401 includes an MMC interface 1407 as an interface with a host 1408" and "is card-shaped." MTI-1004, [0121]. In the FIG. 14 embodiment, "a command ripper circuit 1405 is added in an MMC interface control unit 1403, and its output is connected to a data transfer control unit 1406" and "connection with the host 1408 is made not through the SDRAM interface 112, but only through the MMC interface 1407," but otherwise "[o]ther components are similar to those of FIG 9." MTI-1004, [0121]-[0122]. As in the FIG. 9 embodiment, the memory apparatus 1401 "can be used not only as the MMC function but also as a high-speed volatile or nonvolatile memory."

MTI-1004, [0120], [0123]. Tsunoda's memory apparatus 101, 901, and 1401 "can be applied to any shapes," such as "a LSI, in which memory chips and a control chip are sealed in one package," and the "components may be housed in a memory card shape such as an MMC." MTI-1004, [0124].

FIG.14



MTI-1004, FIG. 14

2. Claim 1

(a) Element 1[p]

50. The preamble of claim 1 recites "[a] portable memory apparatus." Tsunoda provides the preamble of claim 1. For example, Tsunoda discloses that:

> A memory apparatus 4000 shown in FIG. 24 can be mounted on an information terminal such as a **portable** telephone set....

MTI-1004, [0038] [1].

> The host 111 may be, for example a **portable** telephone set, a **portable** information terminal (PDA)....

MTI-1004, [0096].

> The **memory apparatus** 101 [FIG. 1], 901 [FIG. 9], 1301 [FIG. 13] and 1401 [FIG. 14] of the present invention **can be applied to any shapes**. For example, the apparatus may be a LSI, in which memory chips and a control chip are sealed in one package, or all the functions may be housed on one semiconductor chip. The components may be housed in **a memory card shape such as an MMC**.

MTI-1004, [0124]. Tsunoda FIG. 14 (below) shows such "a memory apparatus 1401" "in a memory card shape such as an MMC." MTI-1004, [0121], [0124]. As Tsunoda explains, "[t]he MMC is a memory card using the flash memory 102 as a storage medium." MTI-1004, [0113]. From Tsunoda's disclosure, a POSITA would have understood that a memory apparatus "in a memory card shape such as an MMC" that can be mounted on a "portable" information terminal is a portable memory apparatus.

51. Additionally, it would have been well within the general knowledge of a POSITA that a memory card using flash memory enclosed in a housing that

[1] Emphasis added unless otherwise noted.

protects the internal components from damage due to mishandling, dust and debris, moisture, and electrostatic discharge, such as Tsunoda's MMC, is portable. For example, Pua (U.S. Patent Application Publication No. 2002/0147882) confirms that "[f]lash memory has become an important means of storing data which offers portability" and that "[t]he most common type of flash memory is in the form of a removable memory card" which "allows the contents of the flash memory to be transferred easily between devices or computers." MTI-1013, [0004], [0006]. Further, Mills (U.S. Patent No. 6,353,870) illustrates the portability of the MultiMediaCard by showing that the MultiMediaCard form factor has dimensions of 24mm x 32mm x 1.4mm. MTI-1008, 2:1-20, FIGS. 2A, 3A, 6A (below), 6B (below).

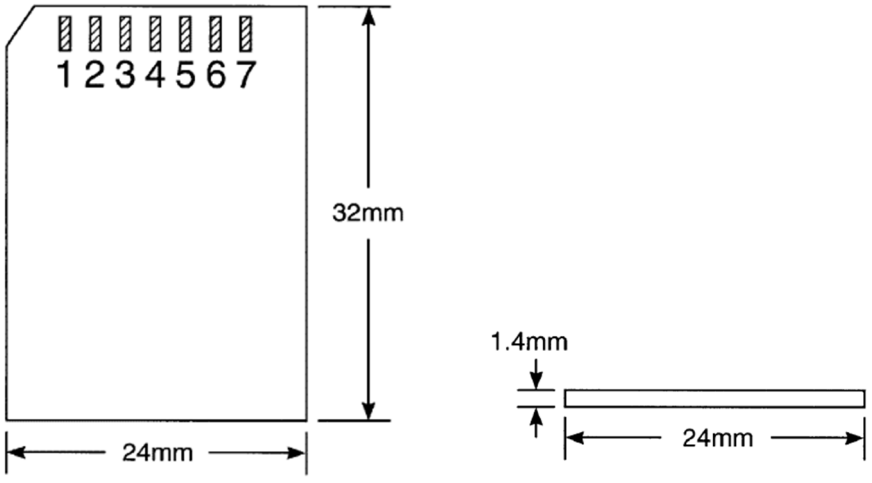
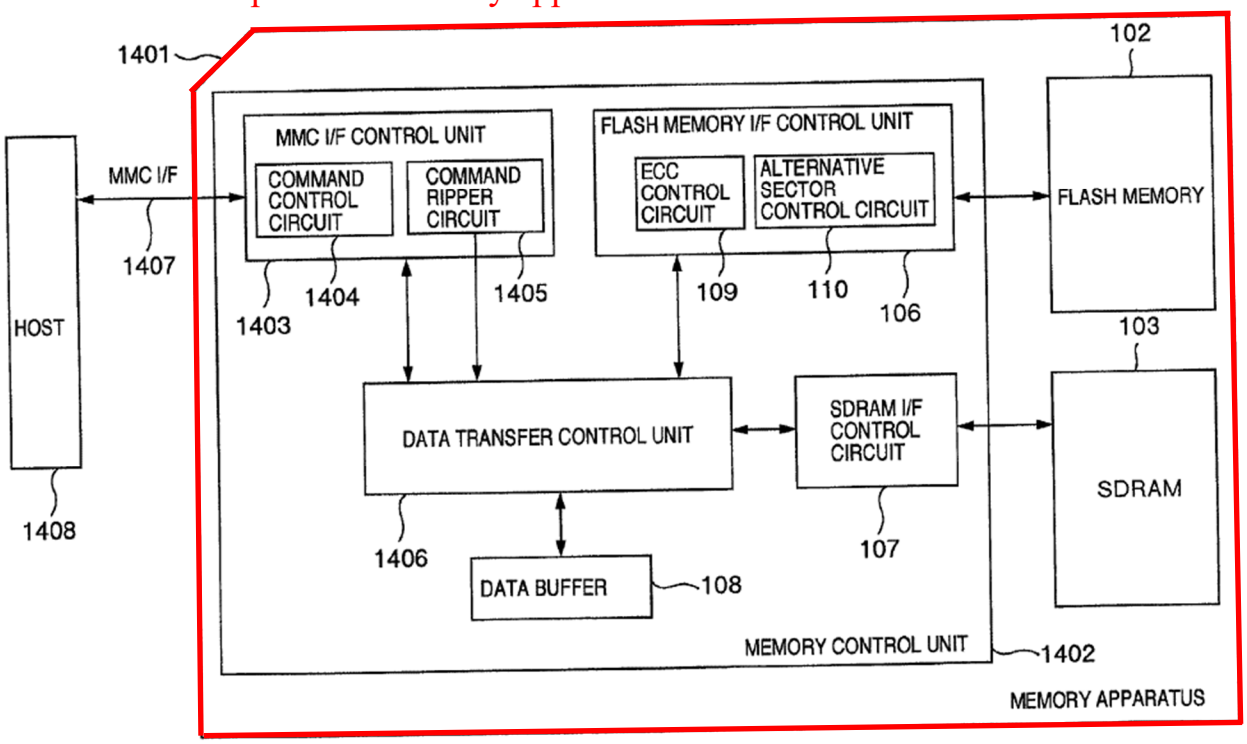


FIG. 6A FIG. 6B

MTI-1008, FIGS. 6A (partial), 6B (partial)

52. Tsunoda further confirms the applicability of its invention to a small portable memory card: "an SD card (small memory card having a width of 24mm, a length of 32mm, and a thickness of 2.1mm...)." MTI-1004, [0117]. Based on my knowledge and experience in this field and my review of Tsunoda, a POSITA would have found it obvious that Tsunoda's MMC 1401 is a portable memory apparatus because it can be mounted on a portable information terminal and beneficially allows the contents of the MMC to be transferred easily between devices or computers.

FIG.14



MTI-1004, FIG. 14[2]

[2] Annotations and color added unless otherwise noted.

(b) Element 1[a]

53. Claim element 1[a] recites "a housing." Tsunoda provides claim element 1[a]. For example, Tsunoda illustrates and describes "an internal configuration" for each memory apparatus of the FIG. 1, 9, and 14 embodiments:

> FIG. 1 shows an example of an **internal configuration** of memory apparatus 101 according to an embodiment of the present invention.

MTI-1004, [0096], [0012].

> FIG. 9 is a view showing an **internal configuration** of another memory apparatus according to the present invention.

MTI-1004, [0020], [0115] ("An internal configuration of the memory apparatus 901").

> FIG. 14 is a view showing an **internal configuration** of yet another memory apparatus according to the present invention.

MTI-1004, [0025], [0121] ("An internal configuration of the memory apparatus 1401 shown in FIG. 14").

54. Tsunoda further discloses that the chips of the memory apparatus are sealed in one package and may be housed in a memory card shape such as an MMC:

> The memory apparatus 4000 [FIG. 24] constructs, for example the SDRAM 4010, the flash memory 4020, and the control unit 4030 on different silicon chips, and interconnects terminals of the silicon chips by, for example wire bonding, thereby providing a multichip

> package, in which the components are **sealed in one package**. Here, the package indicates an LSI package form such as a thin small outline package (TSOP), or a ball grid array (BGA).

MTI-1004, [0056].

> The memory apparatus 101 [FIG. 1], 901 [FIG. 9], 1301 [FIG. 13] and 1401 [FIG. 14] of the present invention can be applied to any shapes. For example, the apparatus may be a LSI, in which memory chips and a control chip are **sealed in one package**, or all the functions may be housed on one semiconductor chip. The components may be **housed in a memory card shape** such as an MMC.

MTI-1004, [0124].

55. It would have been well within the general knowledge of a POSITA that a MMC has a housing. For example, Mills illustrates the housing of a MCC by showing its "form factor" and the "internal architecture" within the housing. MTI-1008, 2:1-20, FIGS. 2A, 3A. Other publications also describe a MMC as having a housing in the form of a "shell" or "card body" formed during the MMC fabrication process, as shown below. MTI-1009, 1:24-27 ("the shell is separately injection-molded from PVC (polyvinyl chloride) or ABS (acrylonitrile-butadiene-styrene)"); MTI-1010, 1:22-24 ("PVC (polyvinyl chloride) or ABS (acrylonitrile-butadiene-styrene) card body preparation").

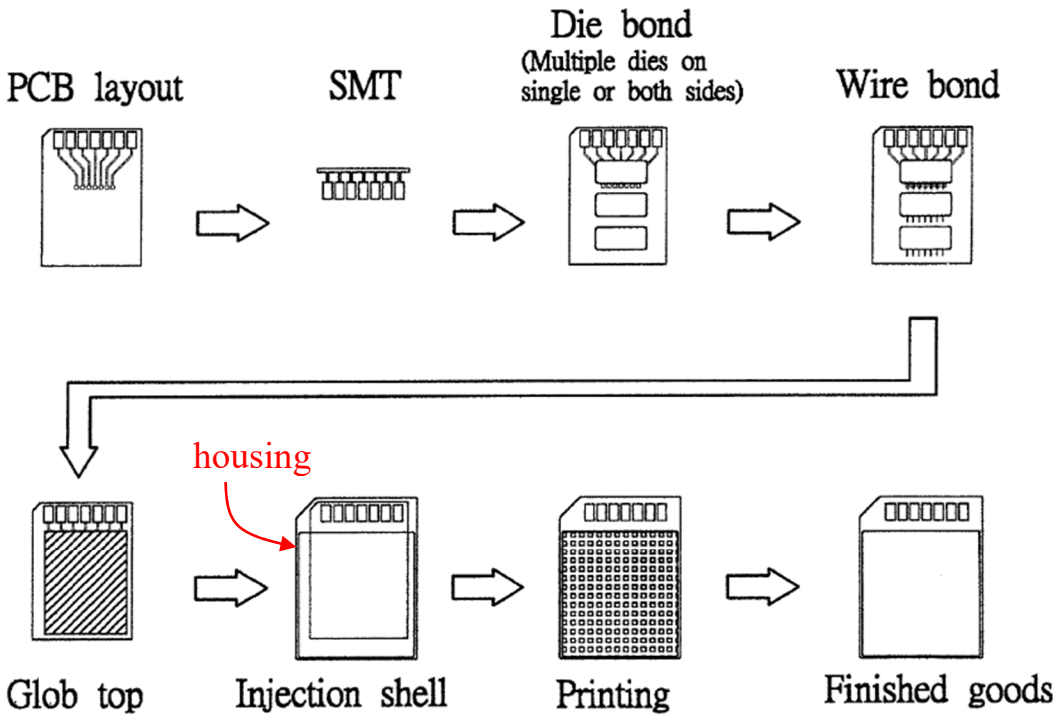
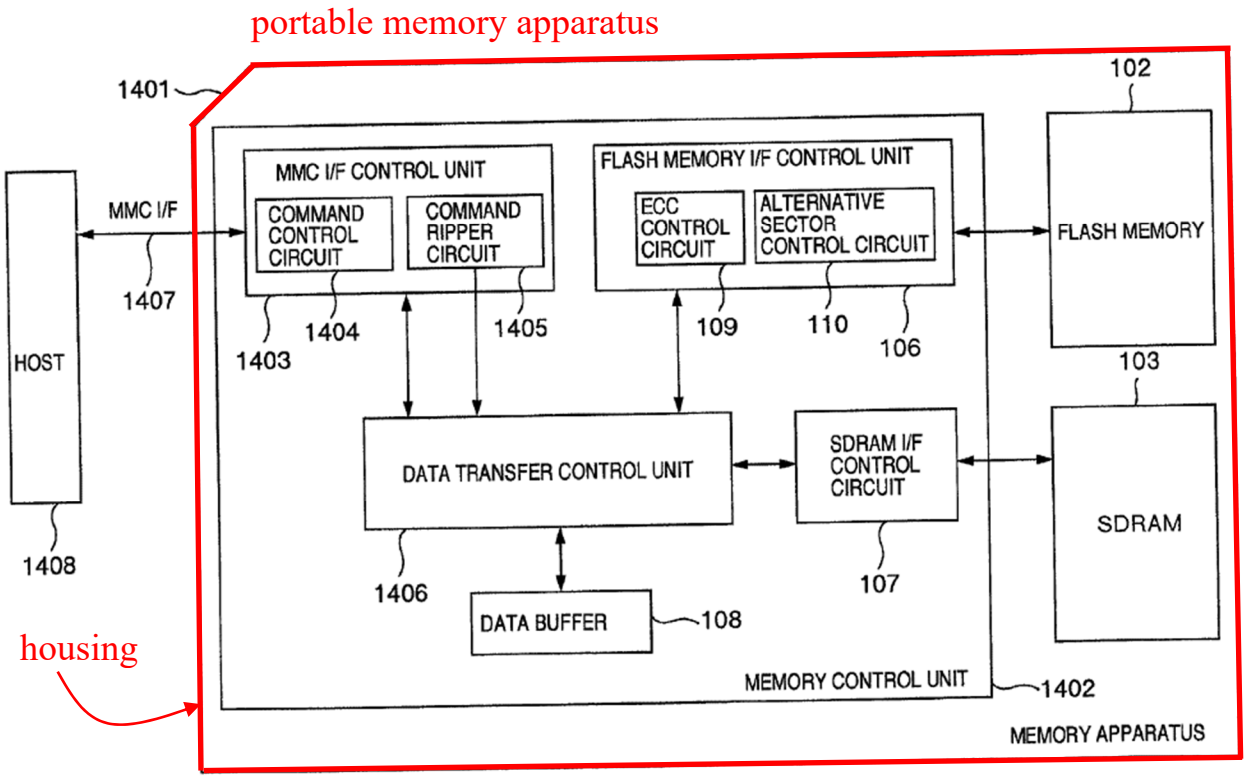


FIG.2

MTI-1009, FIG. 2

56. Based on my knowledge and experience in this field and my review of Tsunoda, a POSITA would have found it obvious that Tsunoda's MMC 1401 has a housing in the form of a shell that encapsulates and protects the memory chips and control chip of the MMC from damage due to mishandling, dust and debris, moisture, and electrostatic discharge to allow the MMC 1401 to be portable.

FIG.14



MTI-1004, FIG. 14

(c) Element 1[b]

57. Claim element 1[b] recites "a memory controller comprised in the housing." Tsunoda provides claim element 1[b]. For example, Tsunoda describes that the FIG. 24 "configuration example" (MTI-1004, [0035]) includes a "control unit" that controls data transfer among the SDRAM, flash memory, and host:

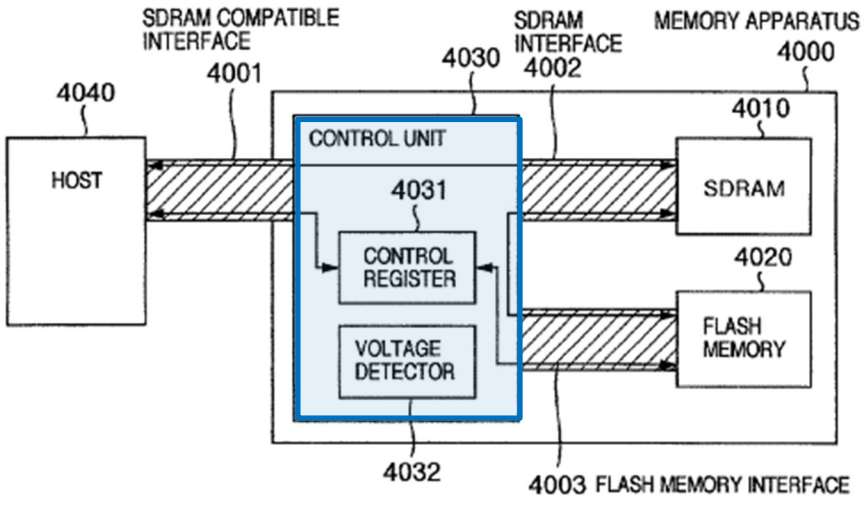
> The memory apparatus 4000 includes at least the SDRAM compatible interface 4001, the SDRAM 4010, the flash memory 4020, and the **control unit 4030**. The SDRAM 4010 and the control unit 4030 are connected to each other through an SDRAM interface 4002.

MTI-1004, [0054].

The control unit 4030 includes a function of controlling the operations of the respective units of the memory apparatus 4000, and realizing functions of the memory apparatus 4000. The control unit 4030 includes a function of interconnecting the SDRAM compatible interface 4001 and the SDRAM interface 4002, and relaying data transfer between the host 4030 and the SDRAM 4010. The control unit 4030 includes a storage function of transferring the data held in the predetermined area of the SDRAM 4010 to a predetermined area of the flash memory 4020. The control unit 4030 includes a load function of transferring the data held in the predetermined area of the flash memory 4020 to a predetermined area of the SDRAM 4010.

MTI-1004, [0062], [0068].

FIG.24



MTI-1004, FIG. 24

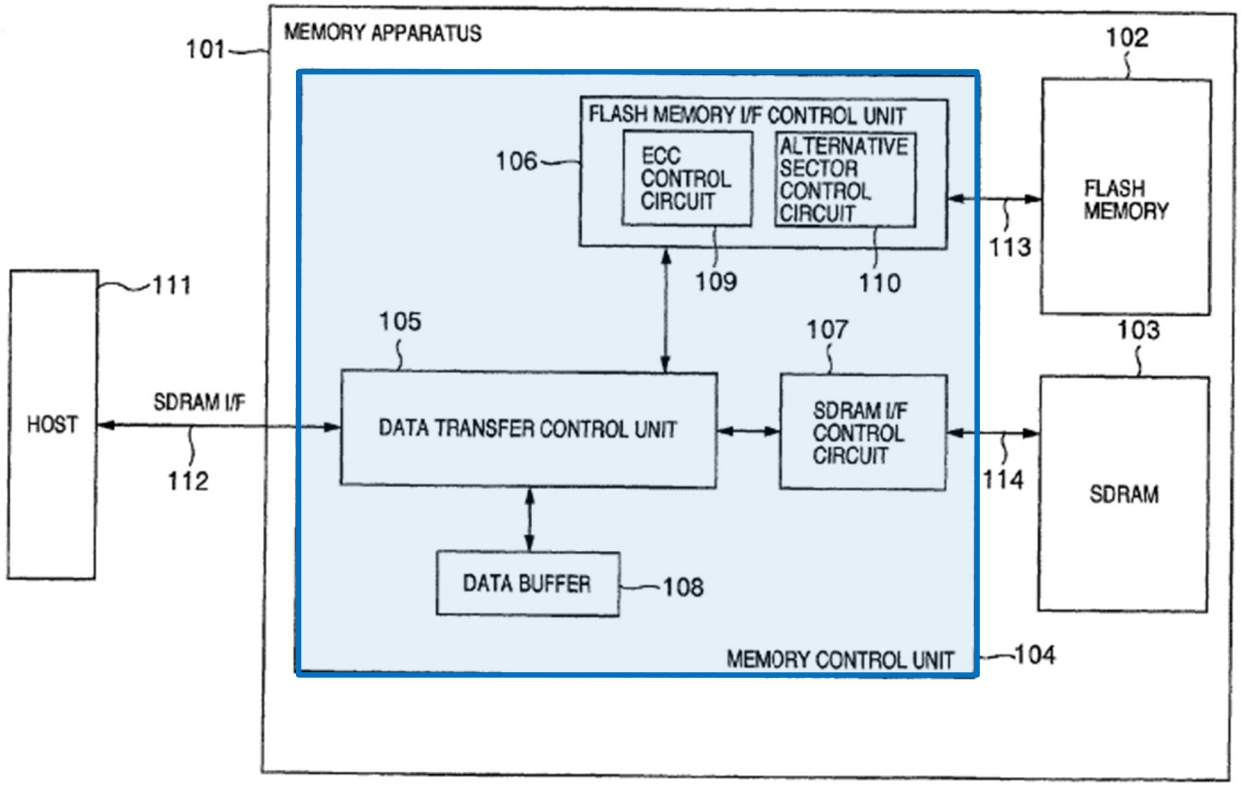
58. Tsunoda illustrates and describes that the "internal configuration" within the housing of each of the FIG. 1, 9, and 14 memory apparatus includes "a

memory control unit" that controls data transfer among the SDRAM, flash memory, and host:

> FIG. 1 shows an example of an **internal configuration** of memory apparatus 101 according to an embodiment of the present invention. The memory apparatus 101 includes a flash memory 102 as a nonvolatile memory, an SDRAM (synchronous SDRAM) 103 as a volatile memory, and **a memory control unit 104 for controlling the memories**. The memory control unit 104 controls data transfer or the like between a host 111 and the memory apparatus 101, and between the flash memory 102 and the SDRAM 103 in response to a request from the host 111.

MTI-1004, [0096]-[0099], [0104]-[0105], [0131], [0133]-[0140], FIGS. 1, 18, 20-24.

FIG.1



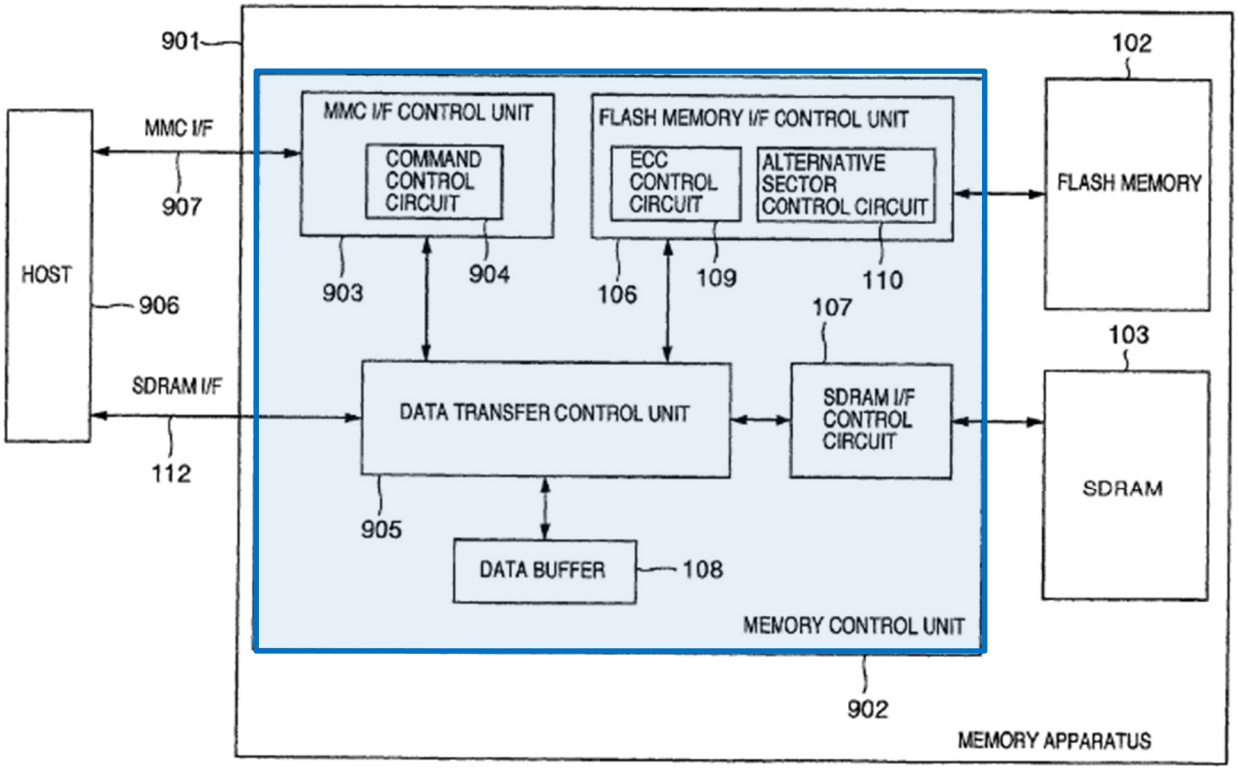
MTI-1004, FIG. 1

Tsunoda highlights the differences between the FIG. 1 memory control unit and the FIG. 9 memory control unit:

> An **internal configuration** of the memory apparatus 901 [of FIG. 9] is different from that of the memory apparatus 101 shown in FIG. 1 in that the MMC interface control unit 903 is added [to memory control unit 902], and the MMC interface control unit 903 is connected to the data transfer control unit 905 [of the memory control unit 902].

MTI-1004, [0115].

FIG.9



MTI-1004, FIG. 9

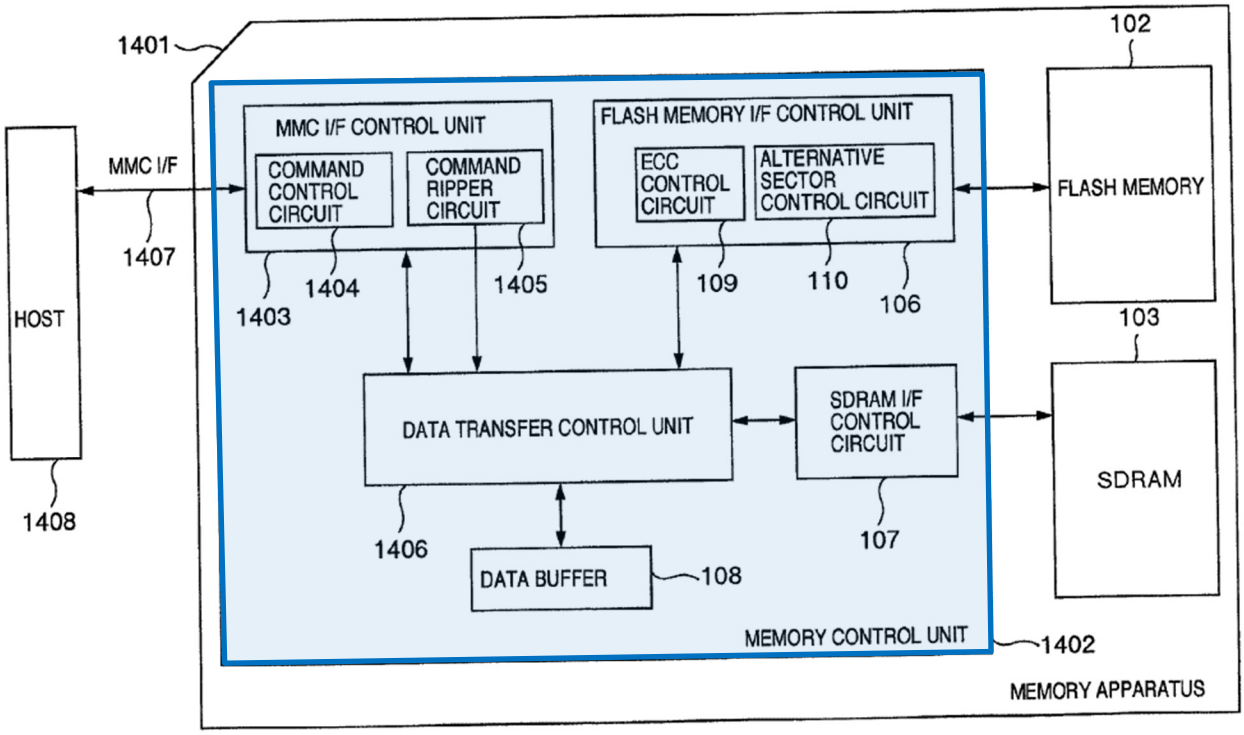
Similarly, in the description of the FIG. 14 embodiment, Tsunoda highlights the differences between the FIG. 9 memory control unit and the FIG. 14 memory control unit:

> FIG. 14 shows a memory apparatus 1401 according to a third embodiment of the present invention... and the apparatus can be treated as in the case of the previous embodiment. An **internal configuration** of the memory apparatus 1401 shown in FIG. 14 is different from that of the memory apparatus 901 shown in FIG. 9 in that a command ripper circuit 1405 is added in an MMC interface control unit 1403 [of the memory control unit 1402], and its output is connected to a data transfer control unit 1406 [of the memory

control unit 1402]. Another difference is that connection with the host 1408 is made not through the SDRAM interface 112, but only through the MMC interface 1407. Other components are similar to those of FIG 9.

MTI-1004, [0121]-[0122] ("Accordingly, as in the case of the previous embodiments, the SDRAM 103 can be accessed from the **memory control unit 1402**.")

FIG.14



MTI-1004, FIG. 14

59. Tsunoda also discloses that the memory control unit is a silicon chip:

The memory apparatus 4000 constructs, for example the SDRAM 4010, the flash memory 4020, and **the control unit 4030** on different **silicon chips**, and interconnects terminals of the silicon

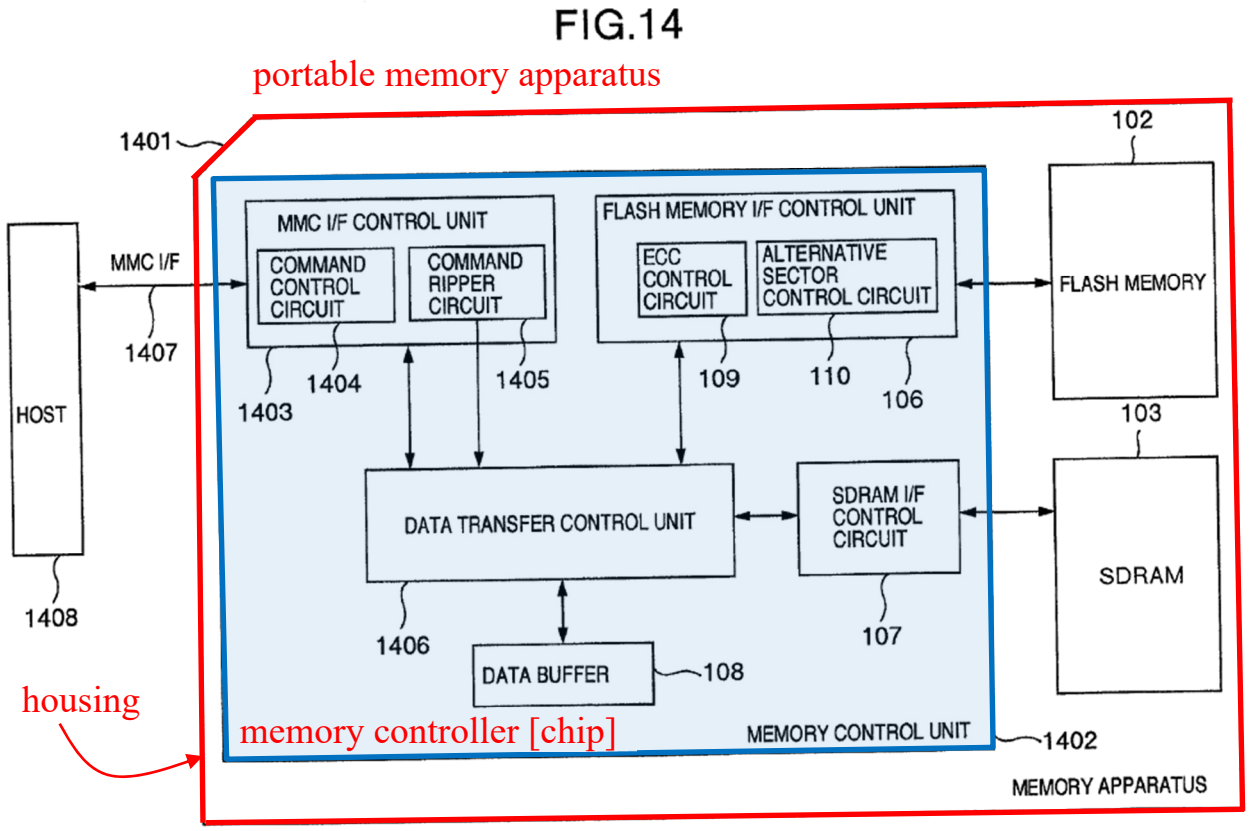
> chips by, for example wire bonding, thereby providing a multichip package, in which the components are sealed in one package. Here, the package indicates an LSI package form such as a thin small outline package (TSOP), or a ball grid array (BGA).

MTI-1004, [0056].

> The memory apparatus 101, 901, 1301 and 1401 of the present invention can be applied to any shapes. For example, the apparatus may be a LSI, in which memory chips and **a control chip** are sealed in one package, or all the functions may be housed on one semiconductor chip. The components may be **housed** in a memory card shape such as an MMC.

MTI-1004, [0124].

60. Based on Tsunoda's disclosures above, Tsunoda's MMC 1401 internal configuration within the housing includes a memory controller chip for controlling the memories and data transfers. Tsunoda's FIG. 14 (below) shows the memory control unit 1402 (memory controller [chip]) (blue) in the housing (outlined red) of the MMC 1401.



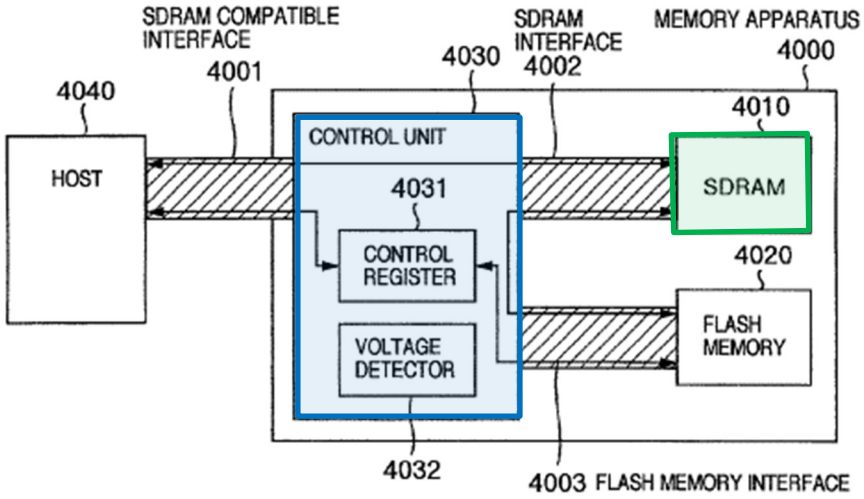
MTI-1004, FIG. 14

(d) Element 1[c]

61. Claim element 1[c] recites "a volatile memory coupled to said memory controller comprised in the housing." Tsunoda provides claim element 1[c]. For example, Tsunoda discloses that "[t]he present invention relates to a memory apparatus, which uses a **volatile memory** and a nonvolatile memory." MTI-1004, [0001]. Tsunoda describes that the FIG. 24 "configuration example" (MTI-1004, [0035]) "is a **volatile memory**" and "includes an SDRAM 4010 to be accessed randomly." MTI-1004, [0042]. Tsunoda further discloses that the "**SDRAM 4010 and the control unit 4030 are connected to each other** through an SDRAM interface 4002." MTI-1004, [0054], [0060], [0062], [0068], [0094]. Tsunoda

discloses that "the **SDRAM 4010 is a volatile memory**" and "data written in the SDRRAM 4010 is lost when the power supply to the memory apparatus 4000 is stopped." MTI-1004, [0075].

FIG.24



MTI-1004, FIG. 24

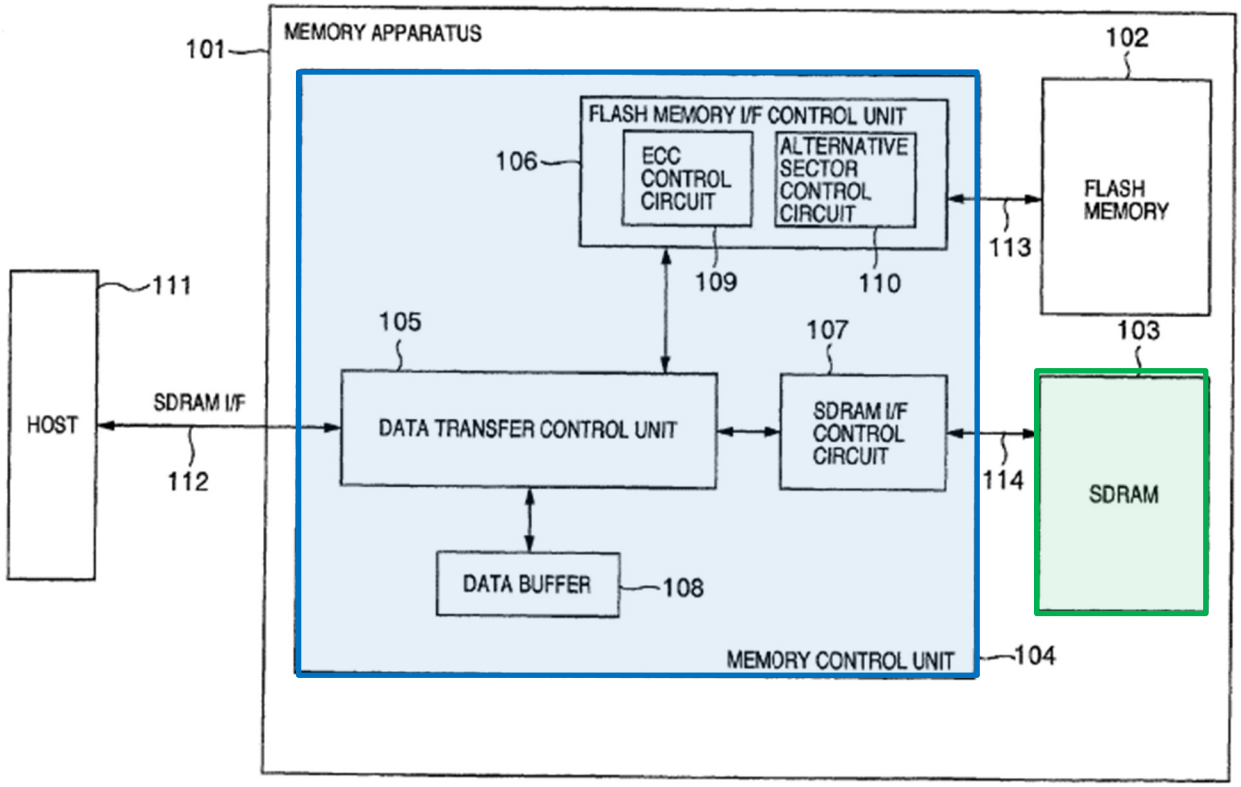
62. Tsunoda similarly illustrates and describes that the "internal configuration" within the housing of each of the FIG. 1, 9, and 14 memory apparatus includes "an SDRAM" as "a volatile memory" coupled to the memory control unit:

> FIG. 1 shows an example of an **internal configuration** of memory apparatus 101 according to an embodiment of the present invention. The memory apparatus 101 includes a flash memory 102 as a nonvolatile memory, **an SDRAM (synchronous SDRAM) 103 as a volatile memory**, and a memory control unit 104 for controlling the memories. The memory control unit 104 controls data transfer or the like between a host 111 and the memory apparatus 101, and between the flash memory 102 and the SDRAM

103 in response to a request from the host 111.

MTI-1004, [0096]-[0099], [0104]-[0105], [0131], [0133]-[0140], FIGS. 18, 20-24.

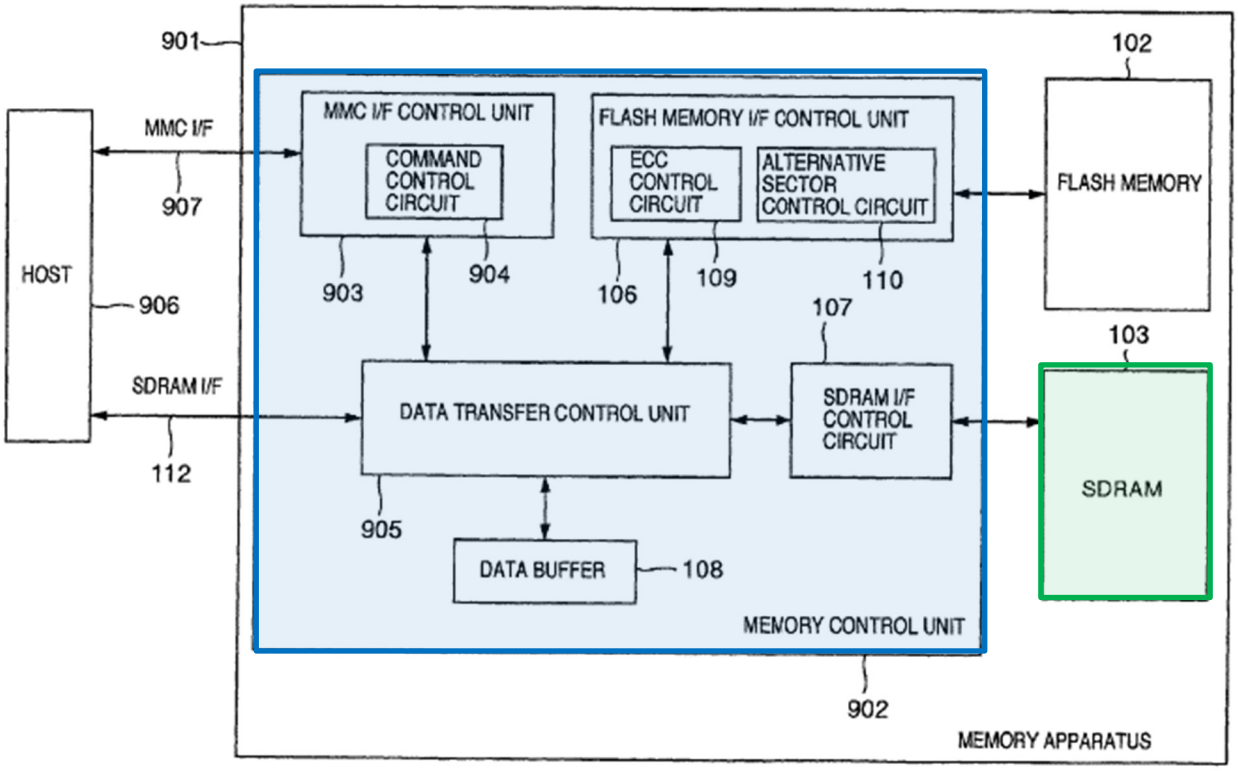
FIG.1



MTI-1004, FIG. 1

The FIG. 9 embodiment includes the same SDRAM 103 as the FIG. 1 embodiment:

FIG.9



MTI-1004, FIG. 9

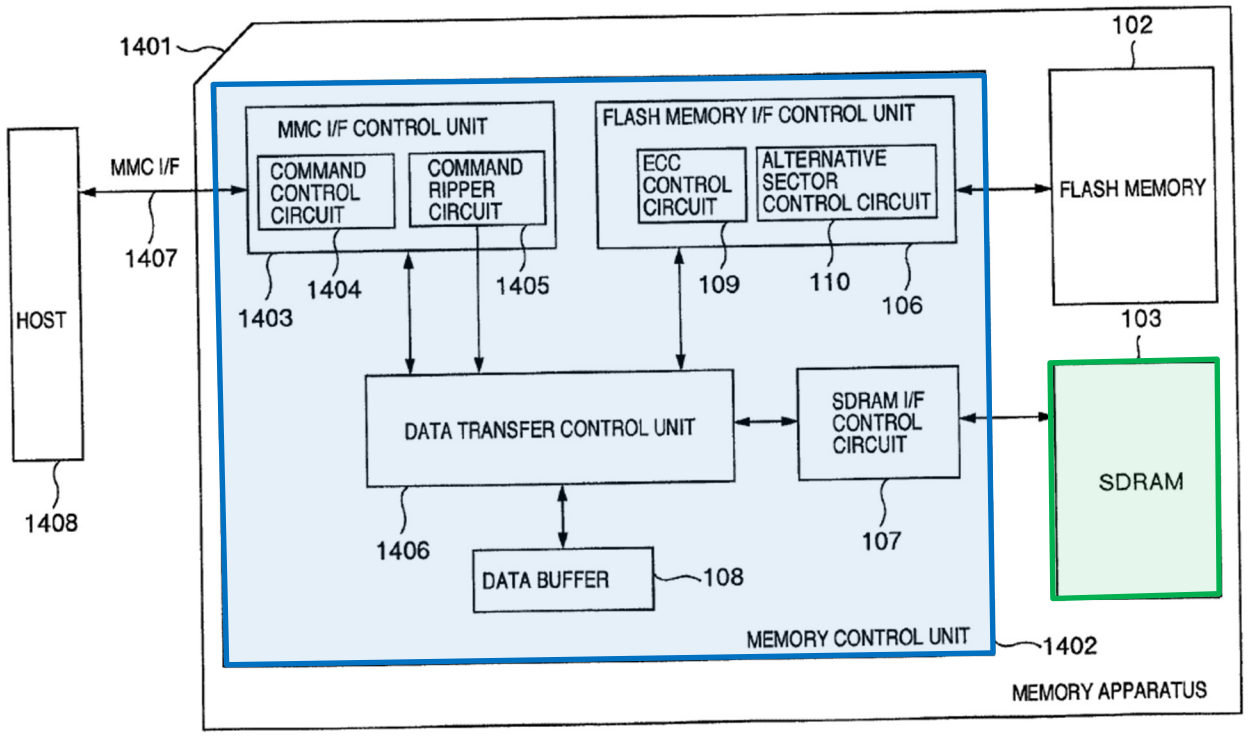
The FIG. 14 embodiment also includes the same SDRAM 103 as the FIG. 1 embodiment:

> As an example of realizing the above access, a command of data writing/reading in the SDRAM 103 may be formed into a capsule in a command area by using a newly defined MMC command, and issued to the MMC 1401. In this case, a command for requesting access to the **SDRAM 103** is detected at the command control circuit 1404 of the MMC interface control unit 1403, access request information is taken out at the command ripper circuit 1405, and sent to the command decoder 601 (see FIG. 6) of the data transfer control unit 1406. Accordingly, as in the case of the previous

embodiments, **the SDRAM 103 can be accessed from the memory control unit 1402**.

MTI-1004, [0122].

FIG.14



MTI-1004, FIG. 14

63. Tsunoda also discloses that the SDRAM and the memory control unit are interconnected by wire bonding:

> The memory apparatus 4000 constructs, for example the **SDRAM 4010**, the flash memory 4020, and the **control unit 4030** on different silicon chips, and **interconnects terminals of the silicon chips by, for example wire bonding**, thereby providing a multichip package, in which the components are sealed in one package. Here, the package indicates an LSI package form such as

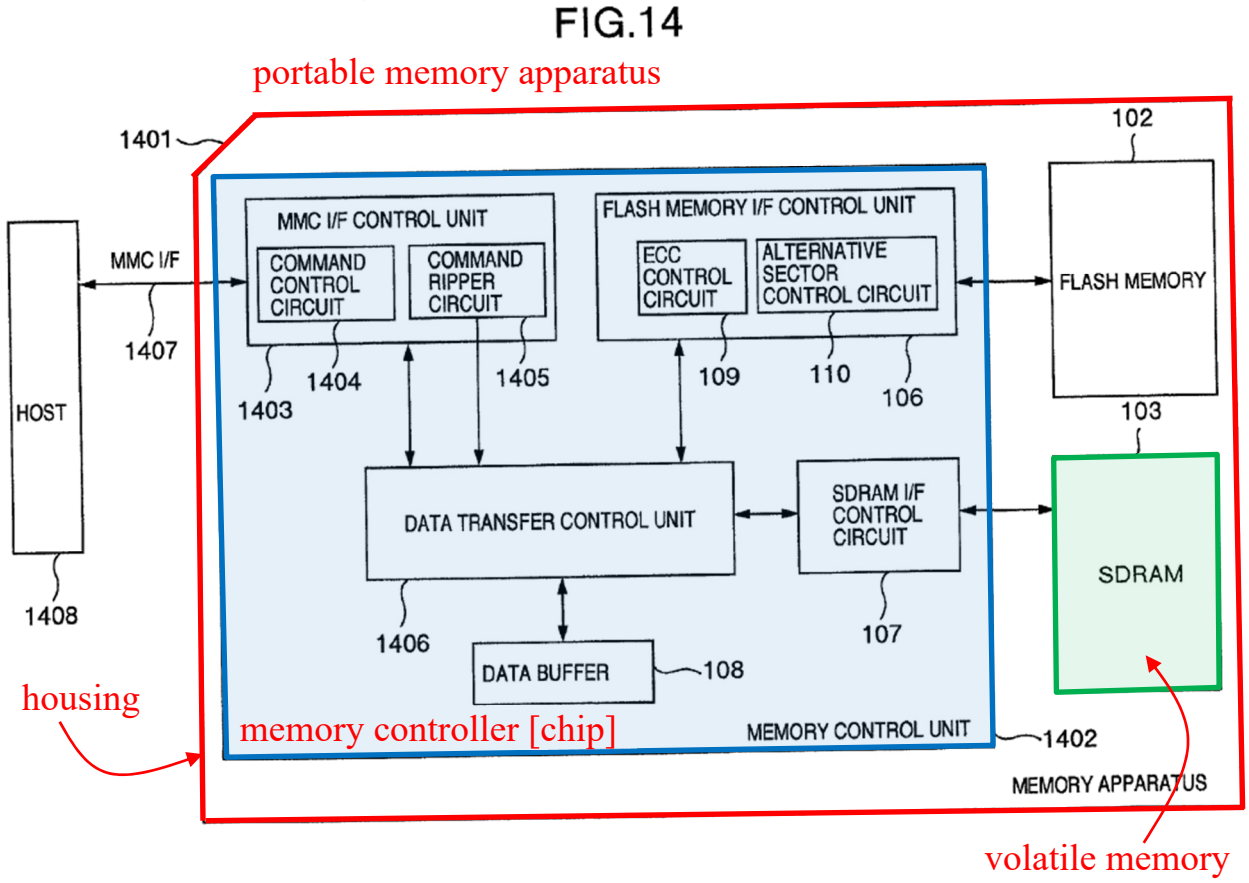
a thin small outline package (TSOP), or a ball grid array (BGA).

MTI-1004, [0056].

> The memory apparatus 101,901, 1301 and 1401 of the present invention can be applied to any shapes. For example, the apparatus may be a LSI, in which **memory chips and a control chip** are sealed in one package, or all the functions may be housed on one semiconductor chip. The components may be housed in a memory card shape such as an MMC.

MTI-1004, [0124].

64. Based on Tsunoda's disclosures above, Tsunoda MMC 1401 internal configuration within the housing includes "a volatile memory," e.g., "SDRAM 103," that "can be accessed from the memory control unit 1402." Tsunoda's FIG. 14 is annotated below to show the SDRAM 103 (volatile memory) (green) coupled to the memory control unit 1402 (memory controller) (blue) in the housing (outlined red) of the MMC 1401.



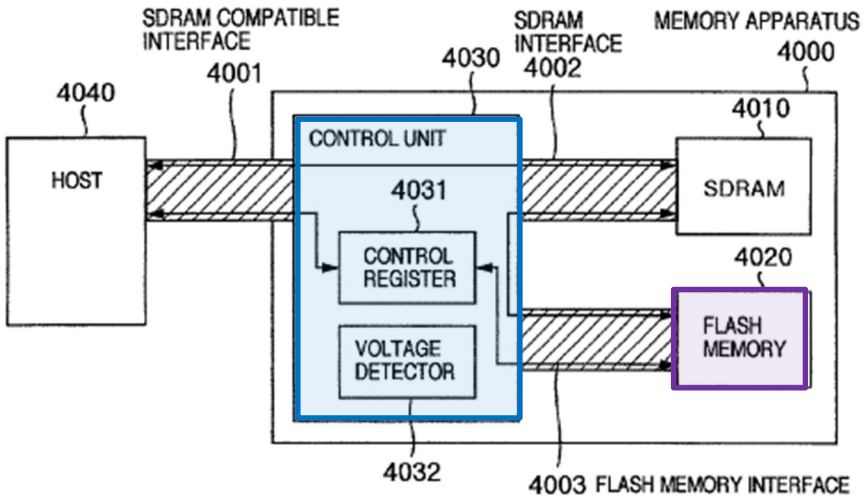
MTI-1004, FIG. 14

(e) Element 1[d]

65. Claim element 1[d] recites "a non-volatile memory coupled to said memory controller comprised in the housing." Tsunoda provides claim element 1[d]. For example, Tsunoda discloses that "[t]he present invention relates to a memory apparatus, which uses a volatile memory and a **nonvolatile memory.**" MTI-1004, [0001]. Tsunoda describes that the FIG. 24 "configuration example" (MTI-1004, [0035]) includes "**a flash memory 4020 as a nonvolatile memory**." MTI-1004, [0042], [0094]. Tsunoda further discloses that the "**control unit 4030 and the flash memory 4020 are connected to each other** through a flash memory

interface 4003." MTI-1004, [0054]-[0055], [0062], [0068]. Tsunoda discloses that the "flash memory 4020 is a memory apparatus, which includes... nonvolatility for holding the written data for at least a fixed period or more even if the power supply is stopped." MTI-1004, [0061].

FIG.24



MTI-1004, FIG. 24

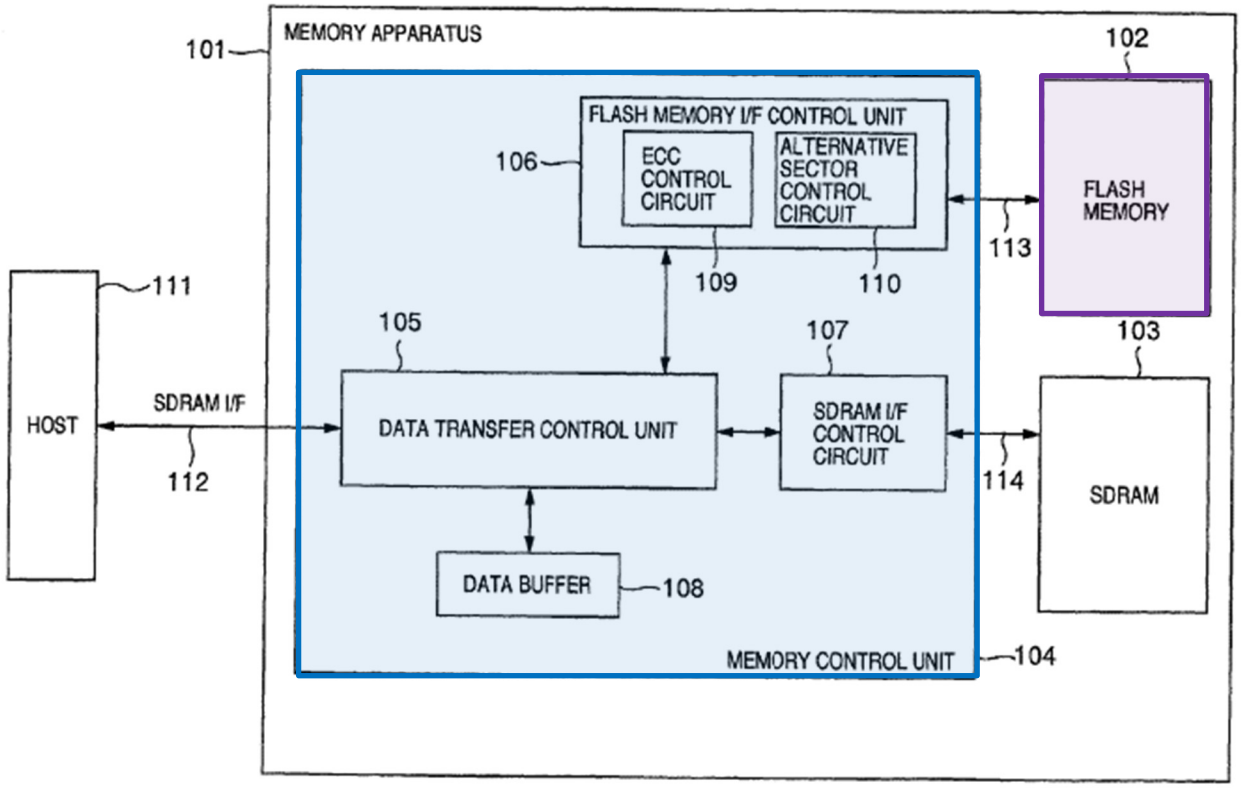
66. Tsunoda similarly illustrates and describes that the "internal configuration" within the housing of each of the FIG. 1, 9, and 14 memory apparatus includes flash memory as a nonvolatile memory coupled to the memory control unit:

> FIG. 1 shows an example of an **internal configuration** of memory apparatus 101 according to an embodiment of the present invention. The memory apparatus 101 includes **a flash memory 102 as a nonvolatile memory**, an SDRAM (synchronous SDRAM) 103 as a volatile memory, and a memory control unit 104 for controlling the memories. The memory control unit 104 controls data transfer or the like between a host 111 and the memory apparatus 101, and

between the flash memory 102 and the SDRAM 103 in response to a request from the host 111.

MTI-1004, [0096]-[0099], [0104]-[0105], [0131]-[0140], FIGS. 18, 20-24.

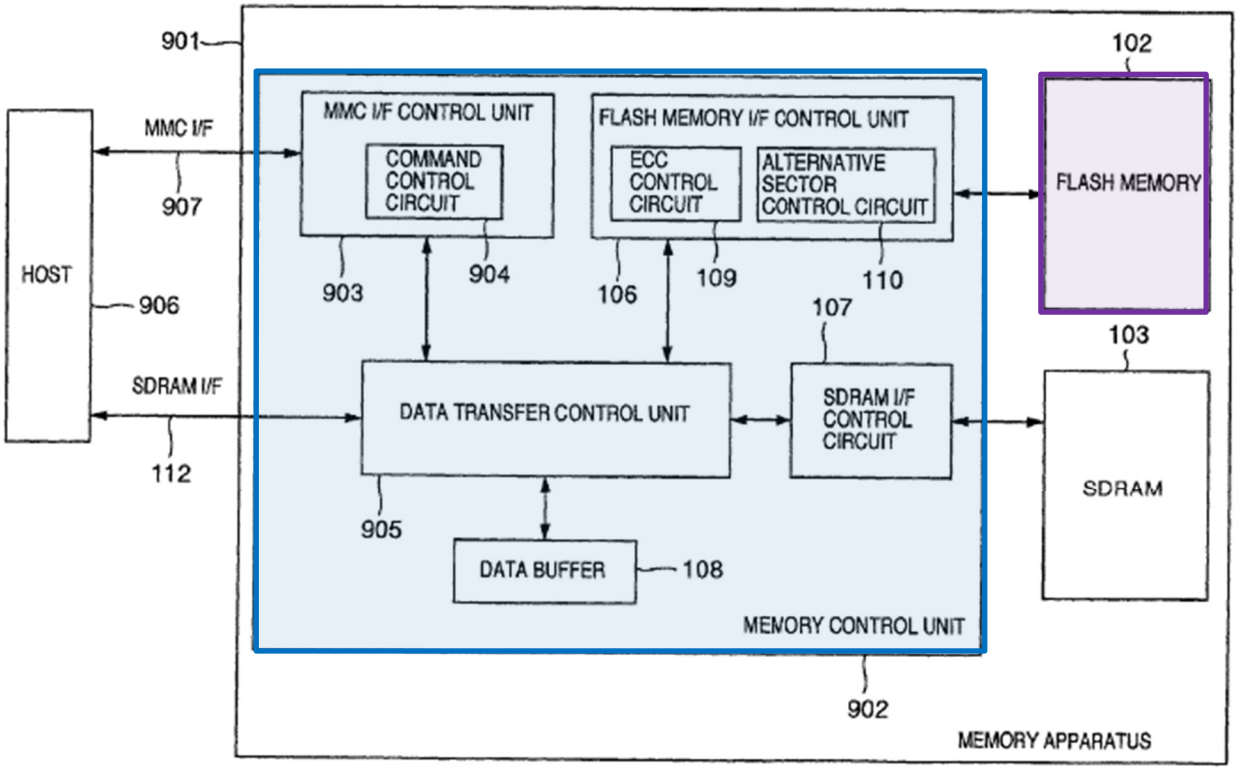
FIG.1



MTI-1004, FIG. 1

The FIG. 9 embodiment includes the same flash memory 102 as the FIG. 1 embodiment:

FIG.9



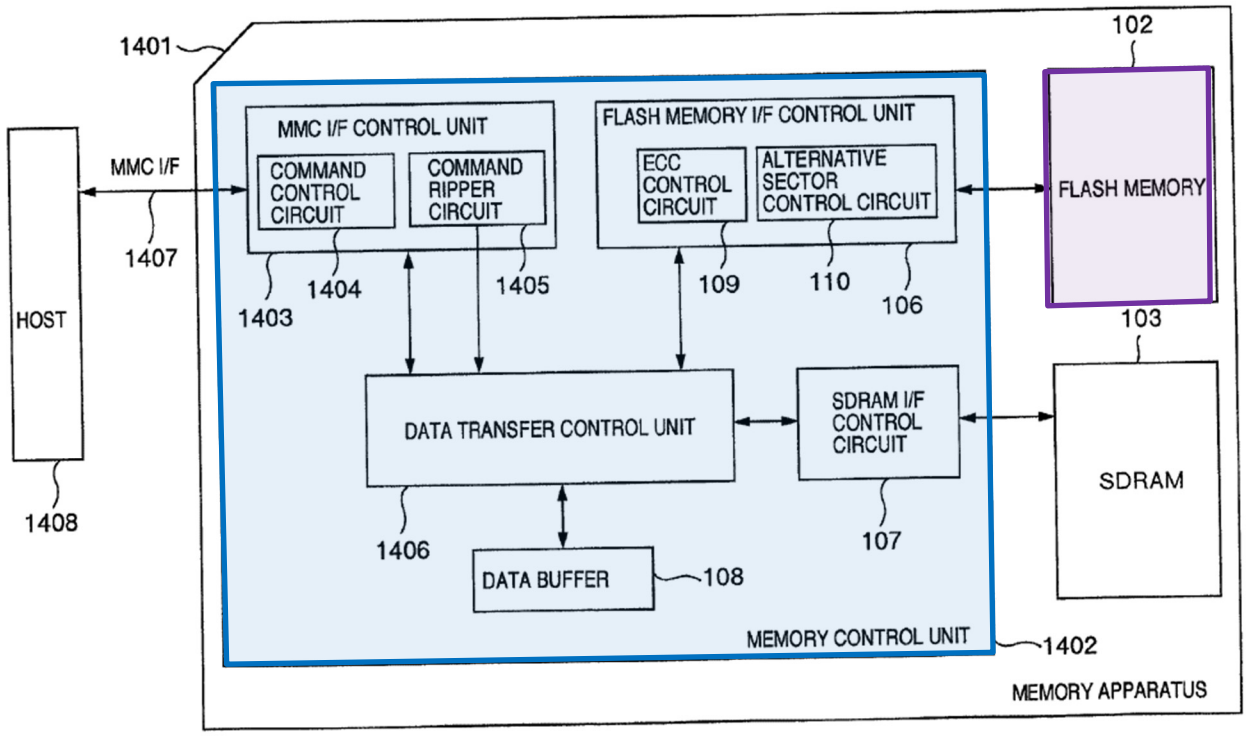
MTI-1004, FIG. 9

The FIG. 14 embodiment also includes the same flash memory 102 as the FIG. 1 embodiment:

> That is, in addition to its function as the MMC, the memory apparatus 1401 can issue a command for instructing data transfer between the **flash memory [102]** and the SDRAM 103, or access the SDRAM 103 from the MMC interface 1407.

MTI-1004, [0122].

FIG.14



MTI-1004, FIG. 14

67. Tsunoda also discloses that the flash memory and the memory control unit are interconnected by wire bonding:

> The memory apparatus 4000 constructs, for example the SDRAM 4010, **the flash memory 4020, and the control unit 4030 on different silicon chips, and interconnects terminals of the silicon chips by, for example wire bonding**, thereby providing a multichip package, in which the components are sealed in one package. Here, the package indicates an LSI package form such as a thin small outline package (TSOP), or a ball grid array (BGA).

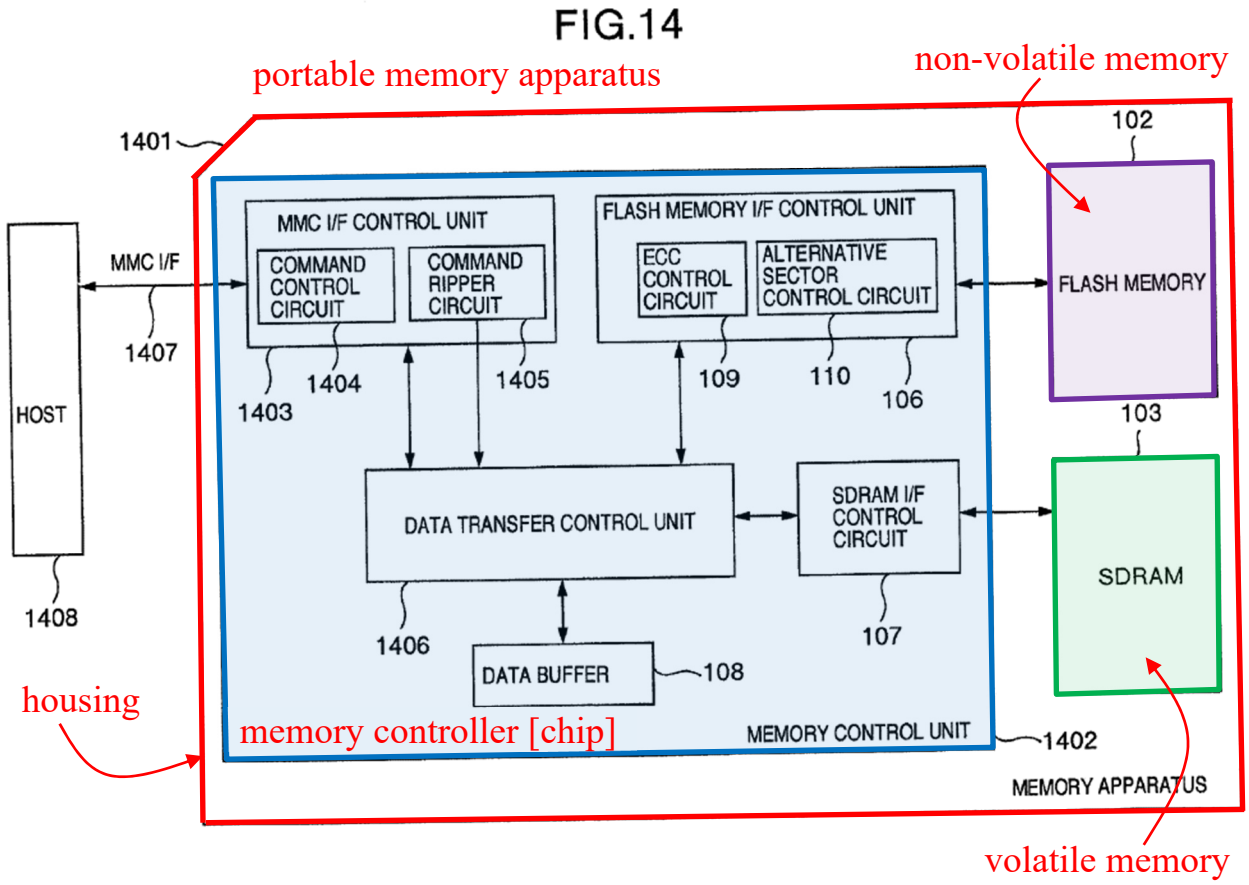
MTI-1004, [0056].

> The memory apparatus 101,901, 1301 and 1401 of the present

> invention can be applied to any shapes. For example, the apparatus may be a LSI, in which **memory chips and a control chip** are sealed in one package, or all the functions may be housed on one semiconductor chip. The components may be housed in a memory card shape such as an MMC.

MTI-1004, [0124].

68. Based on Tsunoda's disclosures above, the Tsunoda MMC 1401 internal configuration within the housing includes "a nonvolatile memory," e.g., "flash memory 102," that is controlled by memory control unit 1402. Tsunoda's FIG. 14 is annotated below to show the flash memory 102 (non-volatile memory) (purple) coupled to the memory control unit 1402 (memory controller) (blue) in the housing (outlined red) of the MMC 1401.



MTI-1004, FIG. 14

(f) Element 1[e]

69. Claim element 1[e] recites "a connector positioned on the housing, wherein said connector couples said portable memory apparatus to a computer system when said connector is plugged into said computer system." Tsunoda provides claim element 1[e]. For example, Tsunoda describes that the FIG. 24 "configuration example" (MTI-1004, [0035]) of the memory apparatus 4000 "can be mounted on an information terminal such as a portable telephone set, personal digital assistants (PDA), a music player, a digital camera, a digital video camera, a

set top box, a personal computer, or a car navigation system." MTI-1004, [0038].

Tsunoda further discloses that:

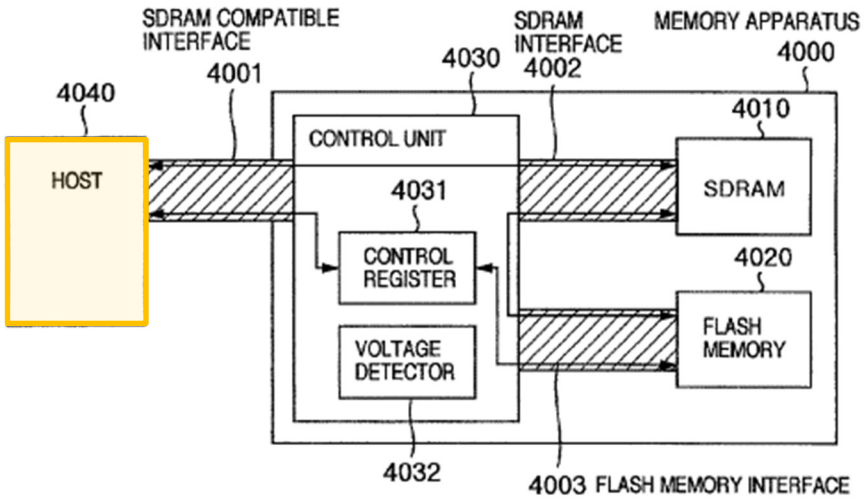
> The memory apparatus 4000 ... includes ... **an SDRAM compatible interface 4001 for enabling the host 4040 to access the memory apparatus 4000**. **The memory apparatus 4000 is connected through the SDRAM compatible interface 4001 to the host 4040**. Since the memory apparatus 4000 operates as an SDRAM compatible memory, the host 4040 can control the memory apparatus 4000 by using the SDRAM compatible interface. ... The memory apparatus 4000 includes a function for enabling the host 4040 to optionally designate data transfer between the SDRAM 4010 and the flash memory 4020. The memory apparatus 4000 also includes an instruction receiving function of receiving its operation instruction from the host 4040, and a status notifying function of notifying a status of the memory apparatus 4000 to the host 4040.

MTI-1004, [0042]-[0043], [0054]-[0055], [0060], [0077], [0090].

> In this case, **the host 4040 is an information processor** such as a CPU or ASIC incorporated in the information terminal. In the memory apparatus 4000, operation programs for, for example, enabling the host 4040 to execute various information processing, can be stored.

MTI-1004, [0040]. The host or computer system of the FIG. 24 configuration example is highlighted below:

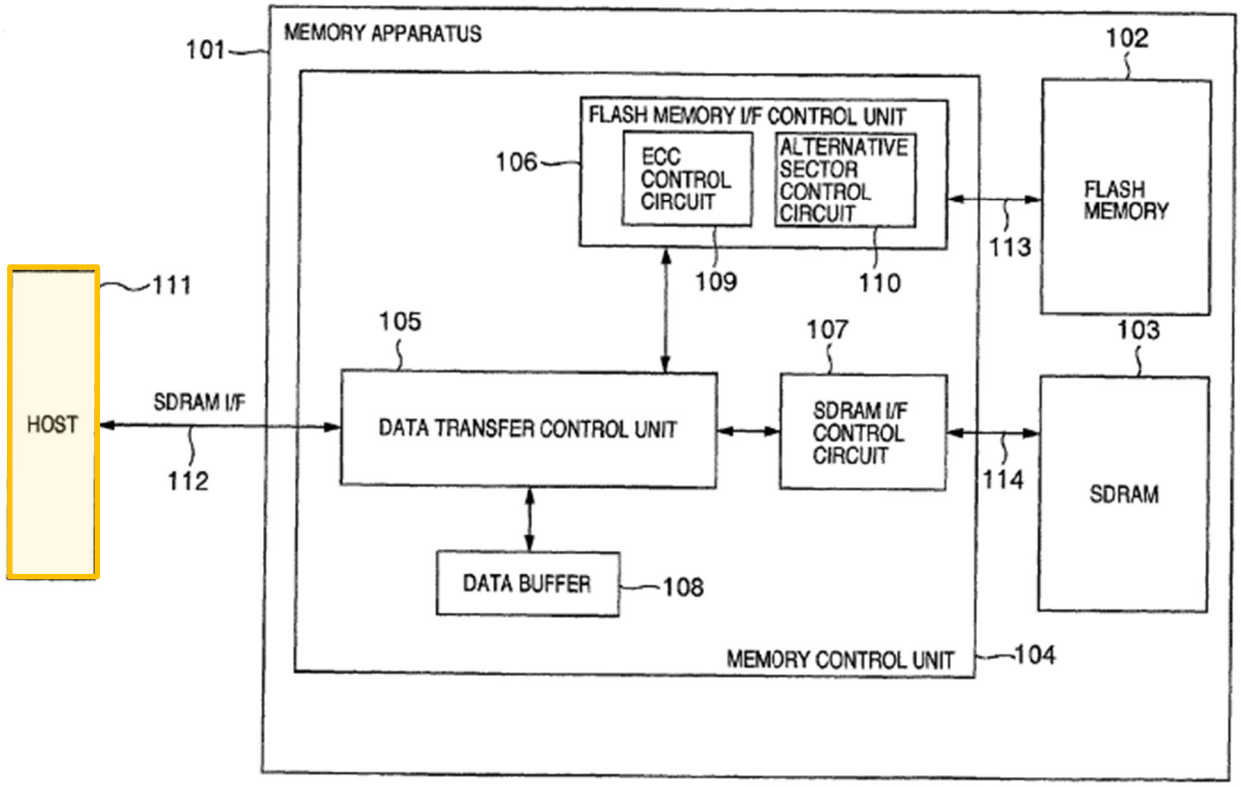
FIG.24



MTI-1004, FIG. 24

Similarly, for the FIG. 1 memory apparatus 101, Tsunoda discloses that the "memory control unit 104 controls data transfer or the like between a host 111 and the memory apparatus 101" and that the "host 111 may be, for example a portable telephone set, a portable information terminal (PDA), a personal computer, a music player (recorder), a camera, a video camera, a set top box terminal or the like." MTI-1004, [0096]. The host or computer system of the FIG. 1 embodiment is highlighted below:

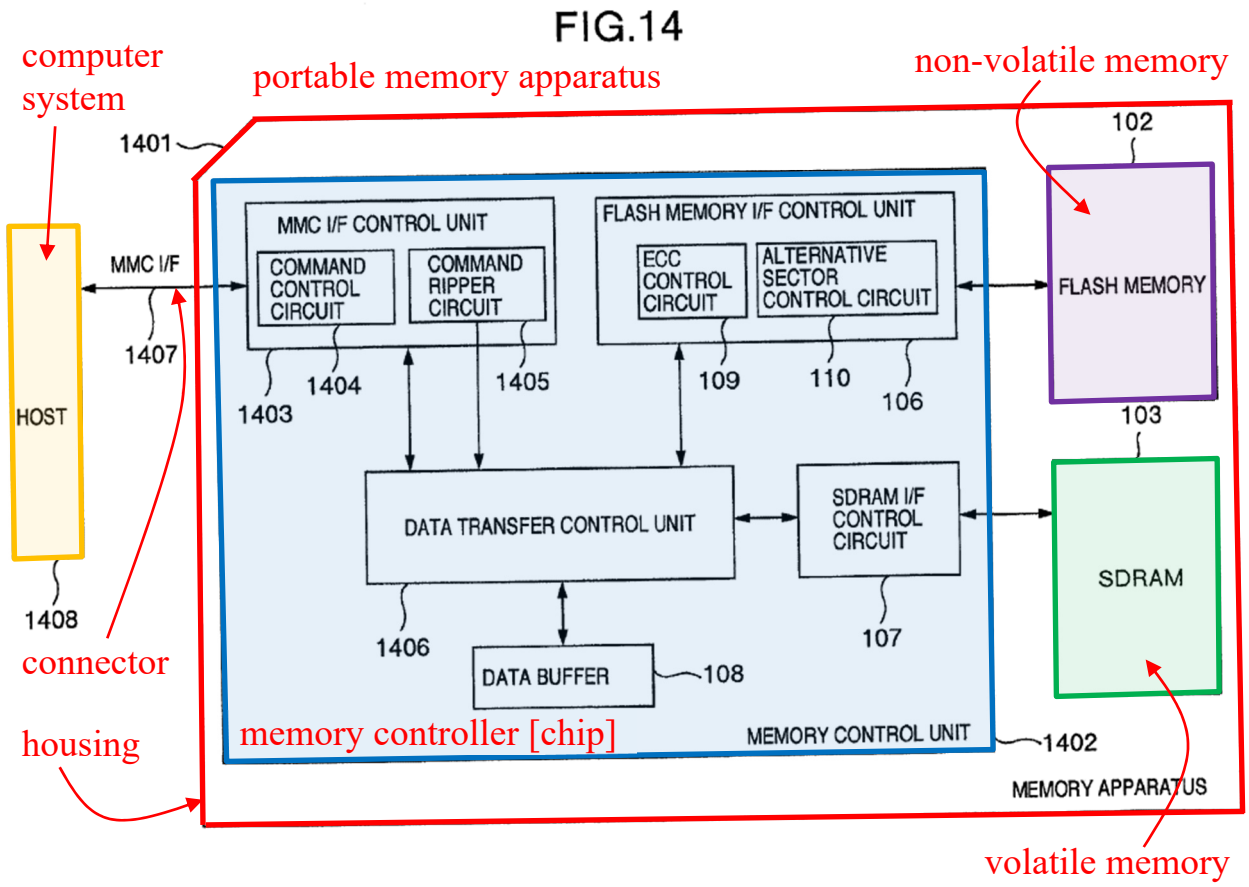
FIG.1



MTI-1004, FIG. 1

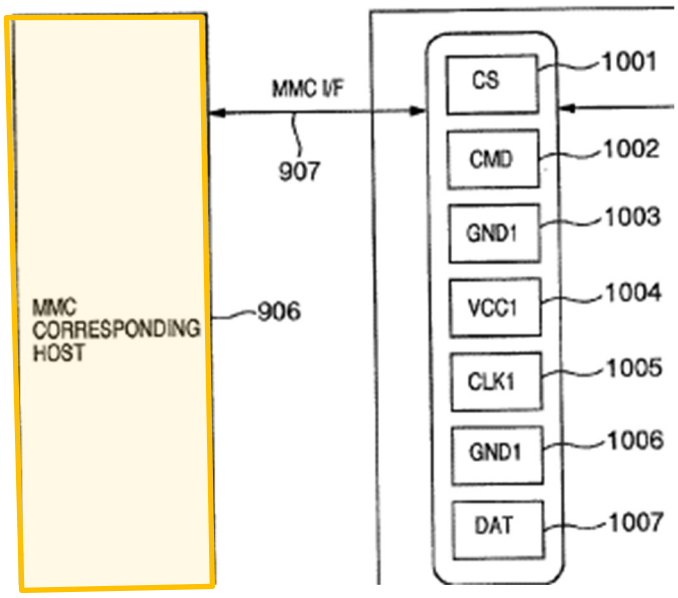
From Tsunoda's description of FIGS. 1 and 24, a POSITA would have found it obvious that Tsunoda's MMC 1401 of FIG. 14 also "can be mounted on an information terminal such as a portable telephone set, personal digital assistants (PDA), a music player, a digital camera, a digital video camera, a set top box, a personal computer, or a car navigation system," and the host is "an information processor such as a CPU or ASIC incorporated in the information terminal" that enables the information terminal to access the contents of the MMC. MTI-1004, [0038], [0096], [0040].

70. Tsunoda additionally discloses that MMC 1401 "includes an MMC interface 1407 as an interface with a host 1408," and "connection with the host 1408 is made not through the SDRAM interface 112 [of FIG. 1], but only through the MMC interface 1407." MTI-1004, [0121]-[0123]. FIG. 14 is annotated below to show the MMC interface 1407 as a connector that couples the MMC 1401 to the host computer system:



MTI-1004, FIG. 14

Tsunoda describes that a MMC interface includes "seven terminals," as shown below, for connecting to and communicating with the host. MTI-1004, [0114]-[0115], [0009].



MTI-1004, FIG. 10 (cropped)

It would have been well within the general knowledge of a POSITA that the terminals of the MMC interface are positioned on the housing of the MMC. For example, Mills's "form factor" illustration (below) shows seven terminals positioned on the housing of the MMC and describes a host interface device with "an internal connector for accepting a MultiMediaCard." MTI-1008, 2:1-20, 4:3-17, FIGS. 2A, 2B, 3A. Based on my knowledge and experience in this field and my review of Tsunoda, a POSITA would have found it obvious that the MMC interface 1407 includes seven terminals positioned on the housing, as shown below, and the terminals are, individually or collectively, a connector that couples the MMC 1401 (portable memory apparatus) to the host (computer system) to enable the host to access the contents of the MMC when the MMC 1401, and thus the connector, is plugged into the host. Tsunoda's disclosure of a connector "positioned on the

housing" is commensurate in scope with the '527 patent's description of this limitation. MTI-1001, 1:42-45 ("The portable RAM drive may comprise a housing... and a connector to connect the portable RAM drive to the computer system."), 2:36-37 ("The portable RAM drive 103 may include a housing 104 and a connector 105."), 2:44-54, 2:57-61 ("the housing 104 of the portable RAM drive 103 may comprise a USB connection 401"), 3:48-52 ("a connector on the portable RAM drive").

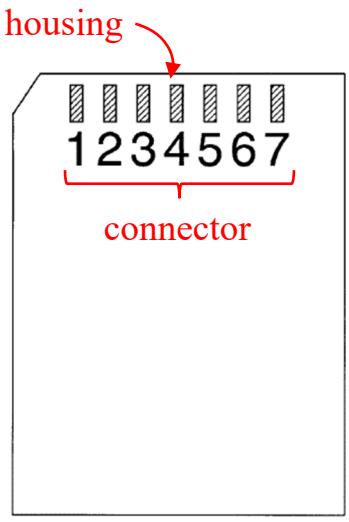


FIG. 2A
MTI-1008, FIG. 2A (partial)

(g) Element 1[f]

71. Claim element 1[f] recites "wherein, when said connector couples said portable memory apparatus to said computer system, said memory controller chip copies data from said non-volatile memory to said volatile memory, and said computer system accesses said data in said volatile memory through said connector."

Tsunoda provides claim element 1[f]. For example, Tsunoda describes that the memory apparatus 4000 of the FIG. 24 "configuration example" (MTI-1004, [0035]) stores various data, and when the host is connected to the memory apparatus 4000, the control unit copies the data from the flash memory to the SDRAM for access by the host:

> The host 4040 can operate based on the operation programs stored in the memory apparatus 4000 by using the memory apparatus 4000 as a main memory. In the memory apparatus 4000, various data for processing by, for example, the operation programs, can also be stored. Here, the data are various data such as a text, an image, a voice, a moving image and the like, or operation parameters/setting files of the programs. Other data can also be stored.

MTI-1004, [0041].

> In addition, for example, if the data of the flash memory 4020 is read to the SDRAM 4010 before the host 4040 accesses the memory apparatus 4000 after the power supply to the memory apparatus 4000 is started, the host 4040 can use the memory apparatus 4000 as a nonvolatile SDRAM compatible memory. The memory apparatus 4000 includes a function for enabling the host 4040 to optionally designate data transfer between the SDRAM 4010 and the flash memory 4020.

MTI-1004, [0042].

> The host 4040 of the memory apparatus 4000 can instruct the memory apparatus 4000 to transfer the data of the SDRAM 4010 to

the flash memory 4020, and the data of the flash memory 4020 to the SDRAM 4010 by the instruction receiving function as occasion demands.

MTI-1004, [0043], [0093], FIG. 24 (4062), FIG. 26 (4206).

The memory apparatus 4000 includes a load function of transferring data held in a predetermined area of the flash memory 4020 to a predetermined area of the SDRAM 4010.

The load function is executed when an operation status of the memory apparatus 4000 satisfies a predetermined load execution condition. One of the load execution conditions is, for example a start of the power supply. One of the load execution conditions is, for example issuance of a load execution instruction from the host 4040.

MTI-1004, [0048]-[0049], [0062] ("The control unit 4030 includes a load function of transferring the data held in the predetermined area of the flash memory 4020 to a predetermined area of the SDRAM 4010."), [0068], [0078], FIG. 24 (4061-4062).

FIG. 25 is a flowchart showing an operation example of the memory apparatus 4000 from a start of the power supply to a stop of the power supply. First, the host 4040 starts supplying of power to the memory apparatus 4000 (4101). The memory apparatus 4000 loads the data held in the mirror area 4021 of the flash memory 4020 to the nonvolatile area 4011 of the SDRAM 4010 when the power supply is started.

MTI-1004, [0080]-[0084], FIG. 24 (4061-4062), FIG. 25 (4101-4105). A POSITA would have understood that the host 4040 starts supplying power to the memory apparatus 4000 when coupling the connector of the memory apparatus to the host 4040.

72. Similarly, for the FIG. 1 memory apparatus 101, Tsunoda describes that when the host is connected to the memory apparatus 101, the memory control unit 104 copies data from the flash memory to the SDRAM for access by the host:

> The memory control unit 104 controls data transfer or the like between a host 111 and the memory apparatus 101, and between the flash memory 102 and the SDRAM 103 in response to a request from the host 111. Normally, the host 111 directly accesses the SDRAM 103 through an SDRAM interface 112. However, by performing writing in a particular address, the host 111 can instruct internal processing of the memory apparatus 101 such as data transfer between the flash memory 102 and the SDRAM 103, or formatting of the flash memory 102.

MTI-1004, [0096], [0104] ("According to the present invention, functions for executing the foregoing processing steps are provided on the memory control unit 104 shown in FIG. 1.").

> After the power is turned ON, program data on the flash memory 102 is copied to the volatile area 203 of the SDRAM 102, and the host 111 can use the program by accessing the volatile area 203 on the SDRAM 103. In this case, the program data stored in the volatile

> area 203 is discarded when the power is turned OFF. However, no problems occur because the program data is held on the flash memory 102. After the power is turned ON, user data on the flash memory 102 is copied to the nonvolatile area 204 of the SDRAM 103, and the host 111 can use the user data by accessing the nonvolatile area 204 on the SDRAM 102. If the user data is slightly changed or contains an addition, the user data is copied to the flash memory 102, and held on the flash memory 102.

MTI-1004, [0099], [0131], [0139]-[0140], FIGS. 18, 23. Tsunoda explains that "by executing the data transfer from the flash memory 102 to the SDRAM 103 according to the command from the host 111 beforehand, the host 111 can access data on the SDRAM 103 at a high speed." MTI-1004, [0112].

73. Based on my knowledge and experience in this field and my review of Tsunoda, the above-described aspects of Tsunoda's FIGS. 1 and 24 embodiments are equally applicable to the FIGS. 9, 10, and 14 embodiments. For example, a POSITA would have found it obvious that the MMC 1401 of FIG. 14 also stores "various data such as a text, an image, a voice, a moving image and the like, or operation parameters/setting files of the programs" or "[o]ther data." MTI-1004, [0041]. As described with respect to FIG. 10, the MMC interface 1407 of FIG. 14, designated as 907 in FIG. 10, of the MMC 1401 includes "a command terminal (CMD) 1002" used by the host "to transmit a memory card command" and "a power supply terminal (VCC 1) 1004 from the host." MTI-1004, [0114]. Additionally, a

POSITA would have found it obvious for the memory control unit 1402 (memory controller chip) to copy the data held in the flash memory 102 (non-volatile memory) to the SDRAM 103 (volatile memory) when one of the load execution conditions are satisfied: (1) when the MMC interface 1407 (connector) couples the MMC 1401 (portable memory apparatus) and the host 1408 (computer system), and the host 1408 starts supplying power to the MMC 1401 through the power supply terminal 1004 of the MMC interface 1407 or (2) when the host 1408 issues a request to copy data from the flash memory 102 to the SDRAM 103 through the command terminal 1002 of the MMC interface 1407. MTI-1004, [0042]-[0043], [0048]-[0049], [0062], [0068], [0078], [0080]-[0084], [0093], [0096], [0099], [0104], [0131], [0139]-[0140], FIGS. 18, 23, FIG. 24 (4061-4062), FIG. 25 (4101-4105), FIG. 26 (4206). A POSITA would have been motivated to do so for several reasons, including to beneficially allow the host 1408 to (1) control data transfer between the flash memory 102 and the SDRAM 103 (MTI-1004, [0004]-[0005]), (2) use the MMC 1401 as a nonvolatile SDRAM compatible memory (MTI-1004, [0042]), and (3) access data on the MMC 1401 via SDRAM 103 at a high speed (MTI-1004, [0112]).

74. For Tsunoda's MMC 1401, Tsunoda discloses that the host accesses the data in the SDRAM 103 through the MMC interface 1407:

> FIG. 14 shows a memory apparatus 1401 according to a third embodiment of the present invention. The memory apparatus 1401 includes an MMC interface 1407 as an interface with a host 1408.

> ... Another difference is that connection with the host 1408 is made not through the SDRAM interface 112, but only through the MMC interface 1407.
>
> In the previous embodiments, access to the SDRAM 103 from the hosts 111 and 906 was carried out through the SDRAM interface 112. In the configuration of the present embodiment, however, access to the SDRAM 103 is also carried out through the MMC interface 1407.

MTI-1004, [0121]-[0123], [0009] ("an interface positioned between the host and the control circuit inputs/outputs data read/written in the volatile memory"), [0039] ("enables the host" to "write data" and "read data" "by an interface" to "SDRAM"), [0042], [0060], [0062], [0075], [0077], [0090]-[0092], [0094], [0099], [0133]-[0134], FIGS. 20 (2001-2003), 24 (4051), 26 (4201). With respect to the MMC interface, Tsunoda discloses that:

> As shown in FIG. 10, the **MMC interface** 907 includes totally seven terminals, i.e., a chip select terminal (CS) 1001, a command terminal (CMD) 1002, two ground terminals (GND 1) 1003 and 1006, a power supply terminal (VCC 1) 1004 from the host 906, a clock terminal (CLK1) 1005, and **data (DAT) 1007**. ... [T]he DAT 1007 is an input-output terminal used by the host 906 to transmits input data of a form compliant with memory card interface specifications to the memory apparatus 901, or receive output data of a form compliant with the same specifications from the memory apparatus 901.

MTI-1004, [0114]. The above-described aspects of the FIGS. 9 and 10 MMC interface are equally applicable to the FIG. 14 MMC interface. MTI-1004, [0121] ("Other components are similar to those of FIG. 9."). Because Tsunoda's MMC 1401 connects with the host 1408 only through the MMC interface 1407 (and not through an SDRAM interface), when the MMC interface 1407 (connector) couples the MMC 1401 (portable memory apparatus) to the host (computer system), the host accesses the data in the SDRAM 103 (volatile memory) through the data terminal 1007 of the MMC interface 1407. *Id*.

3. Claim 6

75. Claim 6 recites:

> The portable memory apparatus of claim 1, wherein said memory controller chip transfers said non-volatile memory with data written to said volatile memory from said computer system while said portable memory apparatus is coupled to said computer system.

The language "said memory controller chip transfers said non-volatile memory with data written to said volatile memory from said computer system" is subject to the following possible constructions: (1) the memory controller chip "transfers *to* said non-volatile memory data written to said volatile memory from said computer system" (*i.e.*, the italicized "to" should be inserted and "with" should be deleted), (2) the memory controller chip "transfers *from* said non-volatile memory data written to said volatile memory from said computer system," or (3) the memory

controller chip "transfers data *from* the non-volatile memory *to* the volatile memory so that it can be accessed by the host computer." Tsunoda provides claim 6 under any of these possible constructions.

76. If "said memory controller chip transfers said non-volatile memory with data written to said volatile memory from said computer system" were construed to mean the memory controller chip "transfers *to* said non-volatile memory data written to said volatile memory from said computer system," Tsunoda describes that the control unit 4030 of the FIG. 24 "configuration example" (MTI-1004, [0035]) transfers to the flash memory data written to the SDRAM from the host while the memory apparatus is coupled to the host:

> The control unit 4030 includes a function of controlling operations of the respective units of the memory apparatus 4000. The control unit 4030 includes a function of controlling the operations of the respective units of the memory apparatus 4000, and realizing functions of the memory apparatus 4000. The **control unit 4030** includes a function of interconnecting the SDRAM compatible interface 4001 and the SDRAM interface 4002, and **relaying data transfer between the host 4030 and the SDRAM 4010**. The control unit 4030 includes a storage function of **transferring the data held in the predetermined area of the SDRAM 4010 to a predetermined area of the flash memory 4020**.

MTI-1004, [0062].

> The memory apparatus 4000 can store a part or all of the data of the SDRAM 4010 in the flash memory 4020. The memory apparatus 4000 can read a part or all of the data of the flash memory 4020. For example, if **the data of the SDRAM 4010 is stored in the flash memory 4020 before the power supply to the memory apparatus 4000 is stopped**, a data loss of the SDRAM 4010 caused by a stop of the power supply can be prevented.

MTI-1004, [0042], [0068], [0078], [0085]-[0088], FIG. 24 (4064-4065), FIG. 25 (4107, 4109-4113).

> The memory apparatus 4000 includes **a storage function of transferring data held in a predetermined area of the SDRAM 4010 to a predetermined area of the flash memory 4020**. By the storage function, the data transferred to the flash memory 4020 can be held on the flash memory 4020 even if it is lost from the SDRAM 4010 because of a stop of the power supply to the memory apparatus 4000.
>
> The storage function is executed when an operation status of the memory apparatus 4000 satisfies predetermined storage execution conditions. One of the storage execution conditions is, for example **a stop of the power supply**. One of the storage conditions is, for example **issuance of a storage execution instruction from the host 4040**.

MTI-1004, [0046]-[0047]. Additionally, while the host 4040 is connected to the memory apparatus 4000, "[t]he host 4040 of the memory apparatus 4000 can instruct the memory apparatus 4000 to transfer the data of the SDRAM 4010 to the

flash memory 4020." MTI-1004, [0043], [0078], [0093], FIG. 24 (4064), FIG. 26 (4206).

77. Similarly, for the FIG. 1 embodiment, Tsunoda describes that the memory control unit 104 transfers to the flash memory data written to the SDRAM from the host while the memory apparatus is coupled to the host:

> FIG. 2 shows an example of address spaces of the SDRAM 103 and the flash memory 102, and a using method thereof. The address space of the SDRAM 103 includes a system work area 201, a command/status holding area 202, a volatile area 203, and a nonvolatile area 204. ... In the nonvolatile area 204, information that must be held even after the power is turned OFF is stored. **Since the SDRAM 103 is a volatile memory, the information stored in the nonvolatile area 204 on the SDRAM 103 is copied to the flash memory 102 before the power is turned OFF, and held on the flash memory 102**.
>
> ... After the power is turned ON, user data on the flash memory 102 is copied to the nonvolatile area 204 of the SDRAM 103, and **the host 111 can use the user data by accessing the nonvolatile area 204 on the SDRAM 102**. **If the user data is slightly changed or contains an addition, the user data is copied to the flash memory 102, and held on the flash memory 102**.

MTI-1004, [0098]-[0099], [0137]-[0138], FIG. 22.

> The host device 111 writes data in the memory apparatus 101 (2001). In this case, the memory control unit 104 detects an access

address of the host 111 (2002). **The data written by the host 111 is recorded in the SDRAM 103** (2003).

MTI-1004, [0134], [0133]-[0136], FIGS. 20-21.

> As described above, by executing the data transfer from the flash memory 102 to the SDRAM 103 according to the command from the host 111 beforehand, **the host 111 can access data on the SDRAM 103** at a high speed. Moreover, by **transferring the data on the SDRAM 103 to the flash memory 102, the data can be held even after the power is turned off**.

MTI-1004, [0112]. In Tsunoda, "functions for executing the foregoing processing steps are provided on the memory control unit 104 shown in FIG. 1." MTI-1004, [0104].

78. Based on my knowledge and experience in this field and my review of Tsunoda, the above-described aspects of Tsunoda's FIGS. 1 and 24 embodiments are equally applicable to the FIGS. 9, 10, and 14 embodiments. For example, a POSITA would have found it obvious for the memory control unit 1402 (memory controller chip) to transfer to the flash memory 102 (non-volatile memory) data written to the SDRAM 103 (volatile memory) from the host 1408 (computer system) while the host 1408 is coupled to the MMC 1401. MTI-1004, [0035], [0042]-[0043], [0046]-[0047], [0062], [0068], [0078], [0085]-[0088], [0093], [0098]-[0099], [0104], [0112], [0133]-[0138], FIGS. 20-22, 24 (4063-4065), 25 (4107, 4109-4113), 26 (4206). A POSITA would have been motivated to do so for several reasons,

including (1) to update any changes or additions to user data to the flash memory, (2) to prevent a data loss of the SDRAM 103 caused by a stop of the power supply, and (3) to hold the data even after the power is turned off. MTI-1004, [0042], [0112].

79. If "said memory controller chip transfers said non-volatile memory with data written to said volatile memory from said computer system" were construed to mean the memory controller chip "transfers *from* said non-volatile memory data written to said volatile memory from said computer system" or "transfers data *from* the non-volatile memory *to* the volatile memory so that it can be accessed by the host computer," Tsunoda renders this obvious for the reasons I explained above in the analysis of claim element 1[f] with respect to Tsunoda.

4. Claim 9

80. Claim 9 recites:

> The portable memory apparatus of claim 1, wherein said volatile memory is selected from a group consisting of FPM DRAM, EDO DRAM, SDRAM, RDRAM, and SRAM.

For the reasons discussed in the analysis of claim element 1[c] with respect to Tsunoda, Tsunoda provides claim 9.

5. Claims 11 and 14

81. Claim 11 recites:

> The portable memory apparatus of claim 1, further comprising an outer impact resistant shell.

Additionally, claim 14 recites:

> The portable memory apparatus of claim 1, wherein said housing comprises a material selected from ABS plastic and polycarbonate.

Tsunoda provides claims 11 and 14. As discussed in the analysis of claim element 1[a] with respect to Tsunoda, a POSITA would have found it obvious that Tsunoda's MMC 1401 has a housing in the form of a shell that encapsulates and protects the memory chips and control chip of the MMC. Additionally, it would have been well within the general knowledge of a POSITA to form a MMC housing using an outer impact resistant shell. For example, publications describe a MMC as having a housing in the form of a "shell" and "the shell is separately injection-molded from PVC (polyvinyl chloride) or ABS (acrylonitrile-butadiene-styrene)." MTI-1009, 1:24-27; *see also* MTI-1010, 1:22-24 ("PVC (polyvinyl chloride) or ABS (acrylonitrile-butadiene-styrene) card body preparation").

82. It also would have been well within the general knowledge of a POSITA that ABS is a plastic that possesses outstanding impact strength and resistance and that a shell injection-molded from ABS forms a rigid impact resistant plastic housing or outer shell. For example, one publication describes that "ABS possesses outstanding impact strength" and is "impact resistant." MTI-1011. Another publication describes the "Major Application Characteristics" of "Acrylonitrile-Butadiene-Styrene (ABS)" as including "Outstanding strength and

toughness." MTI-1023, 10. Based on my knowledge and experience in this field and my review of Tsunoda, a POSITA would have found it an obvious design choice to use ABS to form the housing of Tsunoda's MMC to beneficially provide an outer shell that has outstanding impact strength, toughness, and resistance to protect the components of the MMC from damage due to mishandling, moisture, dust and debris, and electrostatic discharge.

6. Claim 12

83. Claim 12 recites:

> The portable memory apparatus of claim 1, wherein said portable memory apparatus does not have any moving parts.

Tsunoda provides claim 12. As discussed above in the analysis of multiple claim elements with respect to Tsunoda, Tsunoda's memory apparatus includes silicon chips that are sealed in one package and housed in a memory card shape such as an MMC:

> The memory apparatus 4000 [FIG. 24] constructs, for example **the SDRAM 4010, the flash memory 4020, and the control unit 4030 on different silicon chips**, and interconnects terminals of the silicon chips by, for example wire bonding, thereby providing a multichip package, in which the components are **sealed in one package**. Here, the package indicates an LSI package form such as a thin small outline package (TSOP), or a ball grid array (BGA).

MTI-1004, [0056].

> The memory apparatus 101 [FIG. 1], 901 [FIG. 9], 1301 [FIG. 13] and 1401 [FIG. 14] of the present invention can be applied to any shapes. For example, the apparatus may be a LSI, in which **memory chips and a control chip are sealed in one package**, or all the functions may be housed on one semiconductor chip. The components may be **housed in a memory card shape** such as an MMC.

MTI-1004, [0124].

84. It would have been well within the general knowledge of a POSITA that a memory apparatus that includes SDRAM, flash memory, and a memory control unit on different silicon chips housed in a memory card shape does not have any moving parts. For example, Mills's "form factor" illustration (below) shows that a MMC is very compact and not conducive to housing moving parts. MTI-1008, FIGS. 6A (below), 6B (below). Other publications relating to MMC fabrication describe the MMC as including an electronic circuit and dies on a circuit board, which does not have any moving parts. MTI-1009; MTI-1010. Cheng (U.S. Patent Application Publication No. 2002/0010827) confirms that "a portable data storage device comprising a coupling device with an interface device, memory control device and a non-volatile solid-state memory device ... does not include moving parts..." so as "to be more compact than conventional portable data storage devices." MTI-1012, [0005], [0031]. Based on my knowledge and experience in this field and my review of Tsunoda, a POSITA would have found it obvious that Tsunoda's

MMC 1401, which includes the SDRAM 103, flash memory 102, and memory control unit 1402 on different silicon chips housed "in a memory card shape such as an MMC" does not have any moving parts so as to provide a compact portable data storage device. MTI-1004, [0056], [0124]; MTI-1012, [0005], [0031].

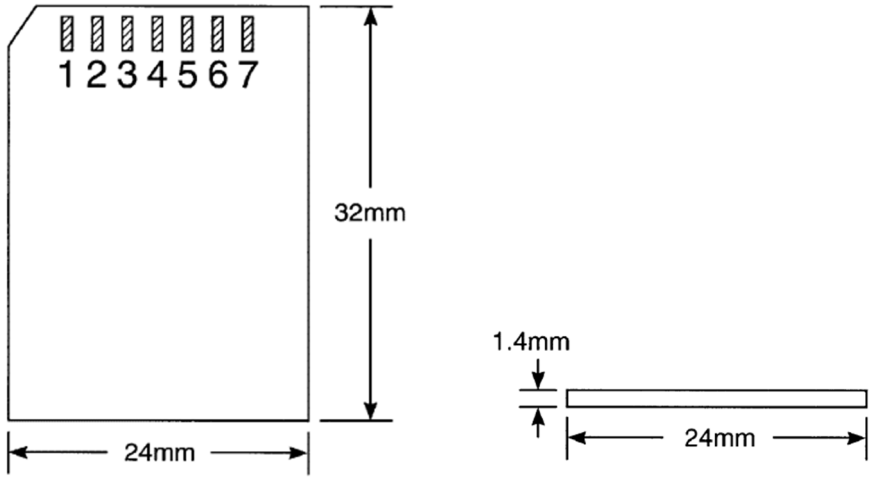


FIG. 6A FIG. 6B

MTI-1008, FIGS. 6A (partial), 6B (partial)

7. Claim 15

(a) Element 15[p]

85. The preamble of claim 15 recites "[a] method." Tsunoda provides a method as recited in the preamble of claim 15 as set forth below in the analysis of claim elements 15[a]-15[e] with respect to Tsunoda.

(b) Element 15[a]

86. Claim element 15[a] recites "coupling a portable memory apparatus to a computer system." For the reasons discussed in the analysis of claim elements 1[p] and 1[e] with respect to Tsunoda, Tsunoda provides claim element 15[a].

(c) Element 15[b]

87. Claim element 15[b] recites "wherein said portable memory apparatus comprises a memory controller chip, a non-volatile memory, and a volatile memory." For the reasons discussed in the analysis of claim elements 1[b], 1[c], 1[d] with respect to Tsunoda, Tsunoda provides claim element 15[b].

(d) Element 15[c]

88. Claim element 15[c] recites "copying data from said non-volatile memory to said volatile memory using said memory controller chip." For the reasons discussed in the analysis of claim element 1[f] with respect to Tsunoda, Tsunoda provides claim element 15[c].

(e) Element 15[d]

89. Claim element 15[d] recites "accessing said data in said volatile memory using said computer system through a connector coupled to said portable memory apparatus and said memory controller chip." For the reasons discussed in the analysis of claim element 1[f] with respect to Tsunoda, Tsunoda provides claim element 15[d].

(f) Element 15[e]

90. Claim element 15[e] recites "updating said non-volatile memory with data from said volatile memory." For the reasons discussed in the analysis of claim 6 with respect to Tsunoda, Tsunoda provides claim element 15[e].

B. Analysis of Tsunoda in view of Sukegawa with respect to Claims 1, 6-7, 9-12, 14-15, and 18

91. For the reasons articulated in detail below, and based on my review of the '527 patent and the Tsunoda and Sukegawa references, I am confident that a POSITA would have readily understood that Tsunoda in view of Sukegawa renders obvious all elements of claims 1, 6-7, 9-12, 14-15, and 18.

1. Overview of Sukegawa

92. Sukegawa relates to a "USB memory storage apparatus that uses an integrated semiconductor device incorporated within a USB connector shield case." MTI-1005, 1:8-11. Sukegawa "implements the electrical components of the USB flash drive apparatus within an integrated semiconductor circuit package that is mounted within the USB connector shield case." MTI-1005, 4:35-38. Sukegawa explains that "the USB flash drive is a small memory storage apparatus that interfaces with a host system through a USB connector." MTI-1005, 1:38-40.

93. Sukegawa's FIG. 1 (below) shows a "USB memory apparatus 100," which is "an integrated flash drive apparatus shown with a USB connector shield case 120." MTI-1005, 4:44-48. In accordance with the USB 2.0 Specification Series

A Plug, the USB connector shield case 120 "extends from an overmold boot" "on an end of the connector opposite the contact terminals." MTI-1005, 7:26-32. "The overmold boot is typically an injection molded thermoplastic insulator material with a minimum UL 94-VO rating." MTI-1005, 7:33-34. "The USB connector shield case 120 for the Series A Plug measure[s] 12 millimeters (mm) wide±0.10 mm, 4.5 mm tall±0.10 mm, and a minimum of 11.75 mm deep." MTI-1005, 7:35-37.

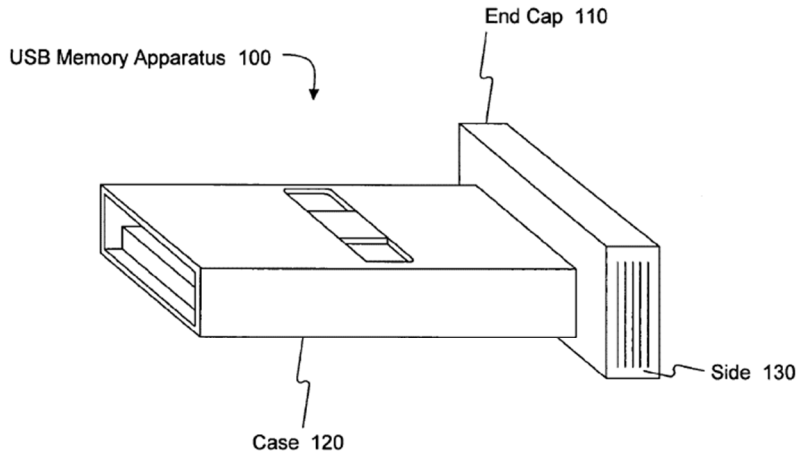


FIG. 1
MTI-1005, FIG. 1

94. The circuit components of the USB memory apparatus include "typical circuits used for accessing data stored in non-volatile flash memory" such as a memory controller, flash memory, USB interface circuit "for handling communications with the USB host," and "other conventional circuit elements." MTI-1005, 5:25-6:41, FIG. 2. An "integrated semiconductor memory device"

includes these electrical circuit components "as one or more interconnected circuit modules" and "can stack multiple interconnected smaller devices (referred to as chips)," or "implement the device in separate modules (each of which may be a multi-chip package [having] one or more chips)." MTI-1005, 6:42-7:18, FIG. 3. "The circuit components of the flash drive apparatus can be mounted within case 120 in various configurations" or "a portion of the active circuitry for the device (e.g., at least one of the circuit modules that implement device 200) may be mounted within the USB connector while the remainder of the active circuitry modules for the device are mounted outside the USB connector." MTI-1005, 4:48-50, 8:6-9:16, FIGS. 5A-5H. "A set of contact terminals (shown in more detail in FIG. 4A-C) is disposed within the connector shield case 120 is in a known configuration to line up with a mating USB connector." MTI-1005, 4:54-57, 7:26-52 ("USB connector is a Series A Plug connector for use in connecting to host systems."). "Attached to the USB connector shield case 120 is an end cap 110" that "may have an opening to expose one or more lights that indicate connection to the host system, access to the apparatus memory or both." MTI-1005, 4:58-59, 4:67-5:2, 5:16-20, 6:21-31.

2. Combination of Tsunoda and Sukegawa

95. As discussed above, Tsunoda discloses that:

> The memory apparatus 101, 901, 1301 and 1401 of the present invention **can be applied to any shapes**. For example, the apparatus may be a LSI, in which memory chips and a control chip are **sealed**

> **in one package**, or all the functions may be housed on one semiconductor chip. The components may be housed in **a memory card shape such as an MMC**.

MTI-1004, [0124], [0056]. Regarding the memory card shape described in Tsunoda, others in the field have recognized that:

> The most common type of flash memory is in the form of a removable memory card. This card allows the contents of the flash memory to be transferred easily between devices or computers.
>
> However, when moving the flash memory card between devices, an additional host or adapter is required in order for the host to communicate with the flash card. Many devices may not have the built-in ability to connect to a flash card, therefore a special adapter or card must be installed in the host device. In addition, the bus architecture can limit the speed of data transfer between the host and flash memory device.
>
> Therefore, there is a need for a flash memory device that can be directly connected to a host device without the need for special cables or adapters.

MTI-1013, [0006]-[0008]. This is achieved by "a flash memory storage device that is connectable to a host via a universal serial bus" (USB). MTI-1013, [0009]. In this regard, Sukegawa explains that:

> The popularity of the USB standard is evident as most computer manufacturers now include one or more USB interfaces for external USB peripherals as part of their systems. Commentators in the computer industry have noted that the USB standard is becoming

the market's dominant I/O connectivity standard.

MTI-1005, 1:19-24. Those in the field have recognized that a USB flash storage device has advantages over a conventional flash memory card:

> The universal serial bus (USB) has become a standard serial interface which allows data to be stored in and read from an external memory device at high speed. Therefore, it is advantageous to combine the benefits of a flash memory device with the speed of the universal serial bus. In addition, by designing the flash memory device with a USB interface, the flash memory device appears as a standard USB storage device which permits the host and flash memory device to connect and interact with ease.

MTI-1013, [0009]-[0010]; MTI-1005, 1:13-44 ("advantage of this quick connectivity standard"); MTI-1017, 1:7-17, 1:39-2:10. A POSITA would have been motivated to apply the teachings of Sukegawa to Tsunoda's memory apparatus to provide a memory apparatus that connects to a host via a USB connector to achieve these advantages. MTI-1005, 1:19-24; MTI-1013, [0006]-[0010].

96. Tsunoda expressly contemplates that its memory apparatus can use interfaces other than a SDRAM compatible interface or a MMC interface for connecting the memory apparatus and the host, and "can be applied to any shapes" other than "a memory card shape." MTI-1004, [0094], [0117] ("not limited to" and "can be applied to various interfaces"), [0124], [0056]. A POSITA implementing

Tsunoda's memory apparatus would have turned to examples of similar memory apparatus to identify suitable interfaces and shapes.

97. Sukegawa provides a suitable interface and shape for a flash memory apparatus. Sukegawa discloses that a flash memory device, such as Tsunoda's memory apparatus, can be implemented as a "USB flash drive apparatus" that "interfaces with a host system through a USB connector." MTI-1005, 1:38-40, 4:35-38. Sukegawa discloses that the USB standard "provides additional bandwidth for multimedia and storage applications and also offers Plug-and-Play capability." MTI-1005, 1:27-30; MTI-1017, 1:7-17, 1:39-2:10. Sukegawa's teachings enable implementation of a memory apparatus, such as that described in Tsunoda, as a USB flash drive apparatus. MTI-1005, 4:48-50, 8:6-9:16, FIGS. 5A-5H. A POSITA would have been motivated to apply the teachings of Sukegawa to Tsunoda's memory apparatus to beneficially provide a USB flash drive apparatus having "additional bandwidth for multimedia and storage applications" and offering "Plug-and-Play capability" between different devices or computers without the need for special cables or adapters. MTI-1005, 1:27-30; MTI-1013, [0006]-[0008]; MTI-1017, 1:7-17, 1:39-2:10.

98. Sukegawa also provides that the USB flash drive apparatus includes lights that indicate when the flash memory is being accessed:

> Additionally, end cap 110 may have an opening to expose one or

more **lights that indicate connection to the host system, access to the apparatus memory or both**.

MTI-1005, 4:67-5:2.

> In a further alternative embodiment, end cap 110 may be made of a visually opaque material capable of reflecting **light** in many directions **when the apparatus is being accessed** or simply when the apparatus has been properly inserted within the host system.

MTI-1005, 5:16-20.

> Additionally, one or more **lights** (not shown) may also be connected to the controller 210 within device 200 to **provide an indication that the device 200 is properly connected to USB host 205 and if NAND flash memory 215 is being accessed**. In one embodiment, the light may be an LED incorporated into the end cap 110 and wired to the controller 210. In other embodiments, the light may be implemented as one or more display devices (e.g., one or more discrete LEDs, an integrated group of LEDs, a small LCD display on the end of the USB connector shield case, etc.) that provides the desired indications to the user.

MTI-1005, 6:21-31. These additional teachings of Sukegawa would further motivate a POSITA to implement a flash memory device, such as Tsunoda's memory apparatus, as a USB flash drive apparatus with indicator lights. A POSITA would have found it obvious that removing a memory apparatus during data transfers is not desirable and would have been motivated to add an indicator light to advantageously provide the user with a visual indication that the USB flash drive

apparatus is transferring data to at least discourage removal of the memory card from a host system during a memory transfer. *Id.*; MTI-1005, 4:67-5:2, 5:16-20, 6:21-31; MTI-1013, [0016], [0072]; MTI-1018, [0005], [0030]; MTI-1019, 3:1-3.

99. Accordingly, a POSITA would have found it obvious and would have been motivated to implement Tsunoda's memory apparatus with a USB connector for connecting the memory apparatus and the host, and with indicator lights to provide a visual indication of the status of the memory apparatus. MTI-1005, 1:19-24, 4:67-5:2, 5:16-20, 6:21-31; MTI-1013, [0006]-[0010], [0016], [0072]. A POSITA would have viewed the implementation of Tsunoda's memory apparatus in a manner that applied Sukegawa's suggested connector configuration as merely the predictable result of combining known prior art elements according to known methods. A POSITA would have had a reasonable expectation of success in doing so as such an implementation was well-known as demonstrated by Sukegawa and commonly utilized in similar memory apparatus. A POSITA would have recognized that the above described modifications would have yielded predictable results, would have been within the ordinary level of skill of a POSITA, and would not have required undue experimentation.

3. Claim 1

(a) Element 1[p]

100. The preamble of claim 1 recites "[a] portable memory apparatus." The combination of Tsunoda and Sukegawa provides the preamble of claim 1. For example, Sukegawa discloses that:

> In general, **the USB flash drive is a small memory storage apparatus** that interfaces with a host system through a USB connector. The apparatus uses low power non-volatile flash memory as its storage media instead of conventional rotating hard disk media.

MTI-1005, 1:38-42.

> FIG. 1 is an exterior illustration of an exemplary USB memory storage apparatus according to an embodiment of the present invention. Referring now to FIG. 1, exemplary USB memory apparatus 100 is an integrated flash drive apparatus shown with a USB connector shield case 120.

MTI-1005, 4:44-48.

> In this embodiment, the USB connector is a Series A Plug connector for use in connecting to host systems on the upstream. As indicated in the USB 2.0 Specification, the Series A Plug includes a Plug Housing (more generally referred to as a USB connector shield case 120) that extends from an overmold boot (not shown) on an end of the connector opposite the contact terminals 400A-D. The overmold boot is typically an injection molded thermoplastic

insulator material with a minimum UL94-VO rating. **The USB connector shield case 120 for the Series A Plug measure 12 millimeters (mm) wide±0.10 mm, 4.5 mm tall±0.10 mm, and a minimum of 11.75 mm deep**.

MTI-1005, 7:26-37.

Those skilled in the art will appreciate that it is still advantageous to incorporate just the controller, the NAND flash memory, or the USB interface circuitry within case 120' as such an alternative embodiment also allows for a reduced size of a USB flash drive apparatus. In other words, by incorporating the electrical circuit components into a reduced size semiconductor device that is capable of being mounted within the USB connector itself or at least partially within the USB connector, embodiments of the present invention allow a USB flash drive apparatus to be implemented in a dramatically reduced physical space. This allows for **a very small, inexpensive, portable and removable storage media** that avoids the break off or damage problem associated with prior art USB flash drives having a majority of their structure being outside the USB connector.

MTI-1005, 9:17-31.

101. Based on my review of Tsunoda and Sukegawa, the combination of Tsunoda and Sukegawa provides a "USB flash drive" which is "a very small, inexpensive, portable and removable storage media" measuring "12 millimeters (mm) wide±0.10 mm, 4.5 mm tall±0.10 mm, and a minimum of 11.75 mm deep."

MTI-1005, 1:38-42, 7:26-37, 9:17-31. Accordingly, Tsunoda-Sukegawa's flash drive is a portable memory apparatus. Other publications relating to USB flash drives confirm that USB flash drives are portable. MTI-1013, [0004] ("Flash memory has become an important means of storing data which offers **portability**."); MTI-1012, [0004]-[0005] ("a **portable** data storage device comprising a coupling device for coupling to a computer serial bus").

portable memory apparatus

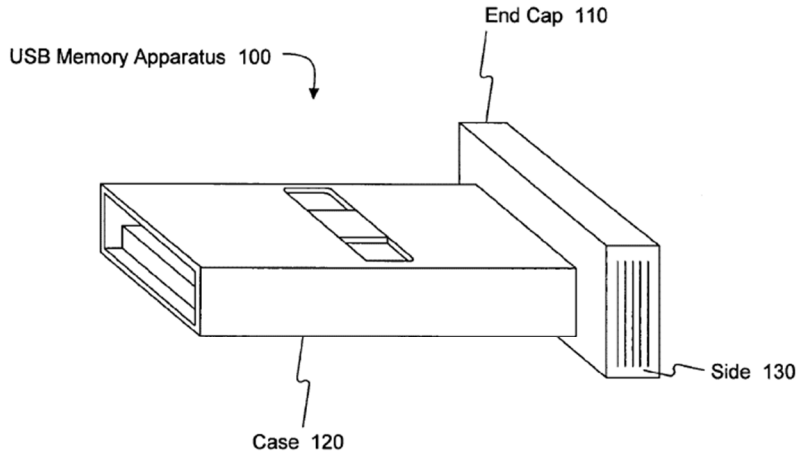


FIG. 1

MTI-1005, FIG. 1

(b) Element 1[a]

102. Claim element 1[a] recites "a housing." The combination of Tsunoda and Sukegawa provides claim element 1[a]. For example, Sukegawa discloses a USB connector shield case, an overmold boot, and an end cap:

FIG. 1 is an exterior illustration of an exemplary USB memory storage apparatus according to an embodiment of the present invention. Referring now to FIG. 1, exemplary USB memory apparatus 100 is an integrated flash drive apparatus shown with a **USB connector shield case 120**. **The circuit components of the flash drive apparatus can be mounted within case 120 in various configurations**. By doing so, there is no need for an external circuit board or substantial structure outside the USB connector shield case 120. In this embodiment, the USB connector shield case 120 is from a USB Series A plug. A set of contact terminals (shown in more detail in FIG. 4A-C) is disposed within the connector shield case 120 is in a known configuration to line up with a mating USB connector.

Attached to the USB connector shield case 120 is an end cap 110. End cap 110 can be used as a handle to pull the apparatus out from the host system's USB connection or interface. In the embodiment illustrated in FIG. 1, ridged side surfaces 130 of end cap 110 provide a gripping surface so that a user can grab hold of the apparatus 110 when inserting or removing it from the host system. In this embodiment, end cap 110 is made of a molded plastic typically with a logo on an exterior surface.

MTI-1005, 4:44-66.

In this manner, the different types of **end caps in embodiments of the invention provide a relatively low-profile, unobtrusive, and compact exterior** for use with reduced size USB flash drive apparatus.

MTI-1005, 5:20-24.

> In this embodiment, the USB connector is a Series A Plug connector for use in connecting to host systems on the upstream. As indicated in the USB 2.0 Specification, the Series A Plug includes a **Plug Housing (more generally referred to as a USB connector shield case 120) that extends from an overmold boot (not shown) on an end of the connector opposite the contact terminals** 400A-D.

MTI-1005, 7:26-37.

> FIGS. 5A-5G show how the device, implemented as one or more **modules, can be mounted within the exemplary USB connector shield case** according to different embodiments of the invention.

MTI-1005, 8:6-62, FIGS. 5A-5G.

> In another embodiment of the present invention, a portion of the active circuitry for the device (e.g., at least one of the circuit modules that implement device 200) may be **mounted within the USB connector** while the remainder of the active circuitry modules for the device are mounted outside the USB connector.

MTI-1005, 8:63-9:16, FIG. 5H.

103. Based on my review of Tsunoda and Sukegawa, the combination of Tsunoda and Sukegawa provides a USB flash drive that includes "a USB connector shield case 120," "an overmold boot," and "an end cap 110." MTI-1005, 4:44-66, 7:26-37. A POSITA would have found it obvious that Tsunoda-Sukegawa's USB flash drive has a housing in the form of the USB connector shield case 120, overmold

boot, and end cap 110 that beneficially provides "a relatively low-profile, unobtrusive, and compact exterior for use with reduced size USB flash drive apparatus" within which the circuit components are mounted. MTI-1005, 5:20-24.

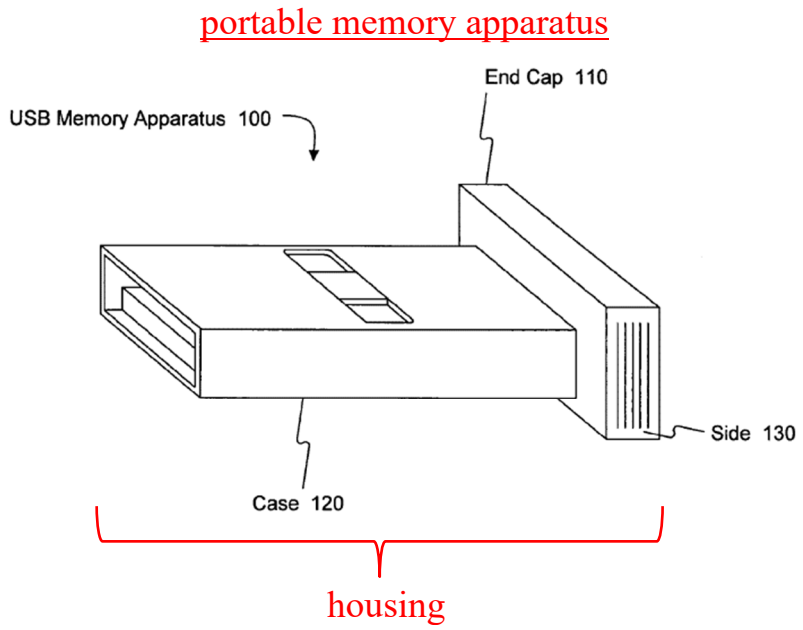


FIG. 1

MTI-1005, FIG. 1

(c) Element 1[b]-1[d]

104. Claim element 1[b] recites "a memory controller comprised in the housing." Claim element 1[c] recites "a volatile memory coupled to said memory controller comprised in the housing." Claim element 1[d] recites "a non-volatile memory coupled to said memory controller comprised in the housing." The combination of Tsunoda and Sukegawa provides claim elements 1[b]-1[d].

105. As discussed in the analysis of claim elements 1[b]-1[d] with respect to Tsunoda, Tsunoda provides a memory apparatus with a memory control unit (memory controller [chip]), a SDRAM (volatile memory) coupled to the memory control unit, and a flash memory (non-volatile memory) coupled to the memory control unit. MTI-1004, [0001], [0035], [0042], [0054]-[0056], [0060]-[0062], [0068], [0075], [0094], [0096]-[0099], [0104]-[0105], [0115], [0121]-[0122], [0124], [0131]-[0140], FIGS. 1, 9, 14, 18, 20-24. For a USB flash drive implementation, as discussed in the analysis of claim element 1[a] with respect to the Tsunoda-Sukegawa combination, Sukegawa teaches that "[t]he circuit components of the flash drive apparatus can be mounted within case 120 in various configurations" or "a portion of the active circuitry for the device (e.g., at least one of the circuit modules that implement device 200) may be mounted within the USB connector while the remainder of the active circuitry modules for the device are mounted outside the USB connector" such as in the overmold boot or end cap 110. MTI-1005, 4:44-66, 5:20-24, 7:26-37, 8:6-9:31, FIGS. 5A-5H. Sukegawa further discloses that:

> Referring now to FIG. 2, **an exemplary semiconductor device 200** is shown connected to a USB host system 205. In this embodiment, the electrical circuits that make up the integrated USB memory apparatus are integrated within the device 200 so that they can fit within a USB connector (or at least have a majority of the

circuits mounted within the USB connector shield case). These circuits **include, but are not necessarily limited to, a memory controller 210, NAND flash memory 215**, and a clock source 220.

MTI-1005, 5:29-37.

However, other conventional and new packages may be used to implement embodiments of the invention depending on the available physical space within the USB connector and the desired functionality of the memory apparatus. **electrical circuit components in distinct and separate circuit modules that can be electrically connected when mounted within different parts of the USB connector**. In other words, alternative embodiments of the present invention may implement the device in separate modules (each of which may be a multi-chip package have one or more chips) to more readily take advantage of the limited available space within the physical confines of the USB connector shield case.

MTI-1005, 7:6-18.

FIGS. 5A-5G show how the device, implemented as one or more modules, can be mounted within the exemplary USB connector shield case according to different embodiments of the invention.

MTI-1005, 8:6-9.

In some situations, it may be advantageous to add a second circuit board for use in mounting certain circuit modules. Typically, the second circuit board is kept within the confines of the USB connector shield case. However, it is contemplated that the second circuit board may be disposed outside the USB connector shield case

> but within close proximity to the case and within the end cap. This is another example of how a majority of the structure for the memory apparatus can be kept within the USB connector shield case.

MTI-1005, 8:26-35.

> FIG. 5G shows a configuration where **the device 200 is implemented with three different modules**. The first is mounted on the bottom of the first circuit board 410, the second is mounted within the block 420, and the third is mounted on the second circuit board 520. Thus, the circuit modules that make up device 200 may be mounted in a variety of locations to keep all or a majority of the apparatus structure within the physical confines of the USB connector shield case.

MTI-1005, 8:54-62.

106. Based on my knowledge and experience in this field and my review of Tsunoda and Sukegawa, a POSITA would have found it obvious to implement, in Tsunoda-Sukegawa's USB flash drive, the memory control unit (memory controller [chip]), the SDRAM (volatile memory), and the flash memory (non-volatile memory) as one, two, or three modules that are mounted within the housing formed by the USB connector shield case 120, overmold boot, and end cap 110 to provide a very small, inexpensive, portable and removable storage media. MTI-1005, 4:44-66, 5:20-24, 5:29-37, 7:6-18, 7:26-37, 8:6-9:31, FIGS. 5A-5H. Based on my knowledge and experience in this field, a POSITA would have been capable of employing ordinary creativity to carry out an implementation of the USB flash drive

with the memory control unit (memory controller [chip]), the SDRAM (volatile memory), and the flash memory (non-volatile memory) mounted within the housing in a manner necessary to achieve the advantages taught by Sukegawa by, for example, varying the size and shape of the housing to accommodate the electronic components, as corroborated by other publications illustrating USB flash drives in varying shapes and sizes. *Id.*; *see, e.g.,* MTI-1013; MTI-1017; MTI-1018; MTI-1019; MTI-1020. An example of an implementation of the USB flash drive with the memory control unit (memory controller [chip]), the SDRAM (volatile memory), and the flash memory (non-volatile memory) as three different modules mounted within the housing is shown below.

portable memory apparatus

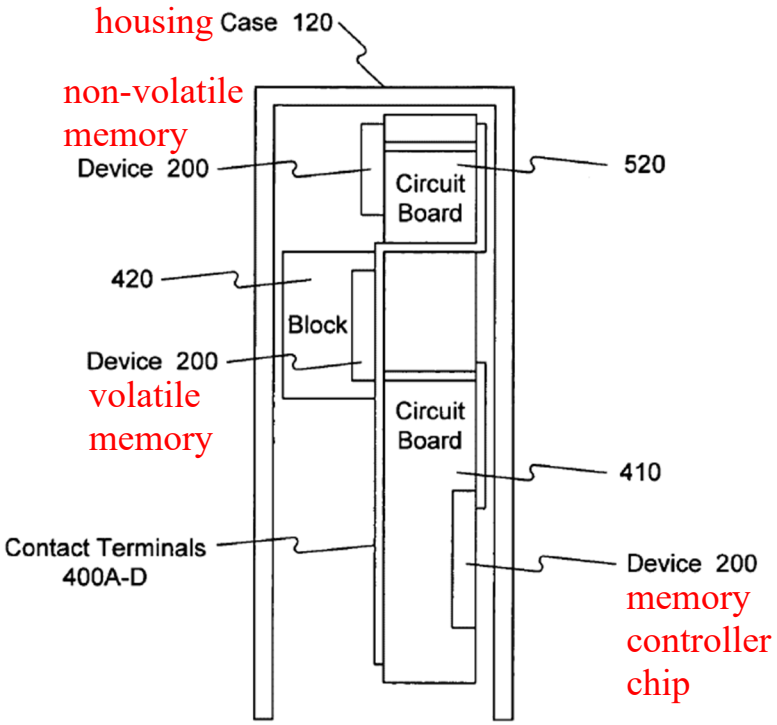


FIG. 5G

MTI-1005, FIG. 5G

(d) Element 1[e]

107. Claim element 1[e] recites "a connector positioned on the housing, wherein said connector couples said portable memory apparatus to a computer system when said connector is plugged into said computer system." The combination of Tsunoda and Sukegawa provides claim element 1[e]. For example, Sukegawa discloses a USB connector in the USB connector shield case:

In general, the USB flash drive is a small memory storage apparatus that **interfaces with a host system through a USB connector**.

MTI-1005, 1:38-40.

A **set of contact terminals** (shown in more detail in FIG. 4A-C) is disposed within the connector shield case 120 is **in a known configuration to line up with a mating USB connector**.

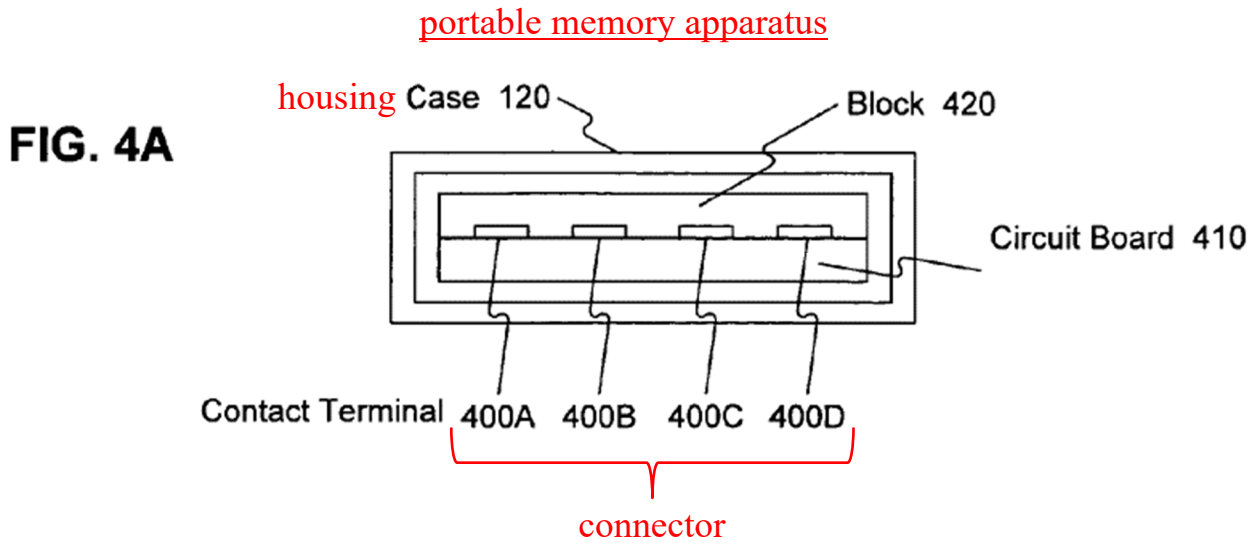
MTI-1005, 4:54-57.

In this embodiment, **the USB connector is a Series A Plug connector for use in connecting to host systems** on the upstream. As indicated in the USB 2.0 Specification, the Series A Plug includes **a Plug Housing (more generally referred to as a USB connector shield case 120)** that extends from an overmold boot (not shown) on an end of the connector opposite the contact terminals 400A-D. The overmold boot is typically an injection molded thermoplastic insulator material with a minimum UL94-VO rating.

....

A set of **contact terminals 400A-D** is shown disposed on a portion of the top side of a first circuit board 410 **within the USB connector shield case 120**. As shown in FIG. 4B, **the set of contact terminals 400A–D are arranged in a standard USB configuration to line up with a mating USB interface or connector**. In this manner, terminal 400A is deemed to be ground, terminal 400B is deemed to be +D, terminal 400C is deemed to be -D, and terminal 400D is deemed to be $+V_{BUS}$ according to the USB standard.

MTI-1005, 7:26-52. Sukegawa's disclosure of a connector "positioned on the housing" is commensurate in scope with the '527 patent's description of this limitation. MTI-1001, 1:42-45 ("The portable RAM drive may comprise a housing... and a connector to connect the portable RAM drive to the computer system."), 2:36-37 ("The portable RAM drive 103 may include a housing 104 and a connector 105."), 2:44-54, 2:57-61 ("the housing 104 of the portable RAM drive 103 may comprise a USB connection 401"), 3:48-52 ("a connector on the portable RAM drive").



MTI-1005, FIG. 4A

108. Based on my knowledge and experience in this field and my review of Tsunoda and Sukegawa, Tsunoda-Sukegawa's USB flash drive "interfaces with a host system through a USB connector." MTI-1005, 1:38-40, 7:26-52 ("USB connector is a Series A Plug connector for use in connecting to host systems."). The USB connector includes a "set of contact terminals (shown in more detail in FIG.

4A-C)... disposed within the connector shield case 120... in a known configuration to line up with a mating USB connector." MTI-1005, 4:54-57. Accordingly, Tsunoda-Sukegawa's USB flash drive (portable memory apparatus) has a USB connector that is positioned on the connector shield case 120 (forming the housing) and that couples the USB flash drive to a host, which is a computer system as discussed in the analysis of claim element 1[e] with respect to Tsunoda and further confirmed by Pua (U.S. Application Publication No. 2002/0147882), when the USB connector is plugged into the host. MTI-1013, [0090] ("USB host 300 such as Windows ME and Windows 2000").

(e) Element 1[f]

109. Claim element 1[f] recites "wherein, when said connector couples said portable memory apparatus to said computer system, said memory controller chip copies data from said non-volatile memory to said volatile memory, and said computer system accesses said data in said volatile memory through said connector." The combination of Tsunoda and Sukegawa provides claim element 1[f]. As discussed in the analysis of claim element 1[e] with respect to the combination of Tsunoda and Sukegawa, Tsunoda-Sukegawa's USB flash drive connects to the host (computer system) via the USB connector. Also as discussed in the analysis of claim element 1[f] with respect to Tsunoda, when the memory apparatus is connected to the host via a connector, the memory control unit (memory controller chip) copies

data from the flash memory (non-volatile memory) to the SDRAM (volatile memory), and the host accesses the data in the SDRAM through the connector. MTI-1004, [0041]-[0043], [0048]-[0049], [0062], [0068], [0078], [0080]-[0084], [0093], [0096], [0099], [0104], [0112], [0131], [0139]-[0140], FIGS. 18, 23, 24 (4061-4062), 25 (4101-4105), 26 (4206). Based on my knowledge and experience in this field and my review of Tsunoda and Sukegawa, when Tsunoda-Sukegawa's USB flash drive is connected to the host (computer system) via the USB connector (as discussed in the analysis of claim element 1[e] with respect to the combination of Tsunoda and Sukegawa), the memory control unit (memory controller chip) copies data from the flash memory (non-volatile memory) to the SDRAM (volatile memory), and the host accesses the data in the SDRAM through the USB connector in a similar manner and for similar reasons as discussed in the analysis of claim element 1[f] with respect to Tsunoda.

4. Claim 6

110. Claim 6 recites:

> The portable memory apparatus of claim 1, wherein said memory controller chip transfers said non-volatile memory with data written to said volatile memory from said computer system while said portable memory apparatus is coupled to said computer system.

For the reasons discussed in the analysis of claim 6 with respect to Tsunoda, the combination of Tsunoda and Sukegawa provides claim 6.

5. Claim 7

111. Claim 7 recites:

> The portable memory apparatus of claim 6, further comprising an indicator coupled to said portable memory apparatus, wherein said indicator indicates when data stored in said volatile memory is being transferred to said non-volatile memory.

The combination of Tsunoda and Sukegawa provides claim 7. For example, Sukegawa discloses lights that indicate when the flash memory is being accessed:

> Additionally, end cap 110 may have an opening to expose one or more **lights that indicate connection to the host system, access to the apparatus memory or both**.

MTI-1005, 4:67-5:2.

> In a further alternative embodiment, end cap 110 may be made of a visually opaque material capable of reflecting **light** in many directions **when the apparatus is being accessed** or simply when the apparatus has been properly inserted within the host system.

MTI-1005, 5:16-20.

> Additionally, one or more **lights** (not shown) may also be connected to the controller 210 within device 200 to **provide an indication that the device 200 is properly connected to USB host 205 and if NAND flash memory 215 is being accessed**. In one embodiment, the light may be an LED incorporated into the end cap 110 and wired to the controller 210. In other embodiments, the light may be implemented as one or more display devices (e.g., one or

> more discrete LEDs, an integrated group of LEDs, a small LCD display on the end of the USB connector shield case, etc.) that provides the desired indications to the user.

MTI-1005, 6:21-31. Based on my knowledge and experience in this field and my review of Tsunoda and Sukegawa, Tsunoda-Sukegawa's USB flash drive includes "one or more lights that indicate connection to the host system, access to the apparatus memory or both." MTI-1005, 4:67-5:2, 5:16-20, 6:21-31. In Tsunoda-Sukegawa's USB flash drive, the lights would indicate when the flash memory is being or has been accessed, for example, when data stored in the SDRAM (volatile memory) is being or has been transferred to the flash memory (non-volatile memory), as this is a typical usage of indicator lights on a USB flash drive. MTI-1013, [0016] ("The flash memory storage device... comprises an indicator, for example an LED indicator, which indicates the status of the memory storage device such as whether it is busy or in standby."), [0072].

6. Claim 9

112. Claim 9 recites:

> The portable memory apparatus of claim 1, wherein said volatile memory is selected from a group consisting of FPM DRAM, EDO DRAM, SDRAM, RDRAM, and SRAM.

For the reasons discussed in the analysis of claim element 1[c] with respect to Tsunoda, the combination of Tsunoda and Sukegawa provides claim 9.

7. Claim 10

113. Claim 10 recites:

> The portable memory apparatus of claim 1, wherein said connection is selected from a group consisting of USB connector, firewire connector, and ATA serial connector.

For the reasons discussed in the analysis of claim element 1[e] with respect to the combination of Tsunoda and Sukegawa, the combination of Tsunoda and Sukegawa provides claim 9.

8. Claims 11 and 14

114. Claim 11 recites:

> The portable memory apparatus of claim 1, further comprising an outer impact resistant shell.

Additionally, claim 14 recites:

> The portable memory apparatus of claim 1, wherein said housing comprises a material selected from ABS plastic and polycarbonate.

The combination of Tsunoda and Sukegawa provides claims 11 and 14. As discussed in the analysis of claim element 1[a] with respect to the combination of Tsunoda and Sukegawa, a POSITA would have found it obvious that Tsunoda-Sukegawa's USB flash drive has a housing in the form of the USB connector shield case 120, overmold boot, and end cap 110. Sukegawa further discloses that:

> **Attached to the USB connector shield case 120 is an end cap 110**. End cap 110 can be used as a handle to pull the apparatus out

> from the host system's USB connection or interface. In the embodiment illustrated in FIG. 1, ridged side surfaces 130 of end cap 110 provide a gripping surface so that a user can grab hold of the apparatus 110 when inserting or removing it from the host system. In this embodiment, **end cap 110 is made of a molded plastic** typically with a logo on an exterior surface.

MTI-1005, 4:58-66.

> In this embodiment, the USB connector is a Series A Plug connector for use in connecting to host systems on the upstream. As indicated in the USB 2.0 Specification, the Series A Plug includes a **Plug Housing (more generally referred to as a USB connector shield case 120) that extends from an overmold boot (not shown)** on an end of the connector opposite the contact terminals 400A-D. **The overmold boot is typically an injection molded thermoplastic insulator material with a minimum UL 94-VO rating**.

MTI-1005, 7:26-37. Based on my knowledge and experience in this field, it would have been well within the general knowledge of a POSITA that the "injection molded thermoplastic insulator material with a minimum UL 94-VO rating" includes materials such as ABS, which possesses outstanding impact strength. For example, one publication discloses that "Plastic Products for UL-94 Flame Class" include "ABS." MTI-1014, 4. Another publication titled "UL 94 Classification and Flame-Retardant Thermoplastics" discloses that "stocked materials with UL 94 V-O or greater" include "ABS." MTI-1015, 2. One publication describes that "ABS

possesses outstanding impact strength" and is "impact resistant." MTI-1011. Another publication describes the "Major Application Characteristics" of "Acrylonitrile-Butadiene-Styrene (ABS)" as including "Outstanding strength and toughness." MTI-1023, 10. Based on my knowledge and experience in this field and my review of Tsunoda and Sukegawa, a POSITA would have found it an obvious design choice to use ABS to form at least a portion of the housing (e.g., the overmold boot and end cap) of Tsunoda-Sukegawa's USB flash drive to beneficially provide an outer shell that has outstanding impact strength, toughness, and resistance to protect the components of the flash drive from damage due to mishandling , moisture, dust and debris, and electrostatic discharge.

9. Claim 12

115. Claim 12 recites:

> The portable memory apparatus of claim 1, wherein said portable memory apparatus does not have any moving parts.

The combination of Tsunoda and Sukegawa provides claim 12. As discussed above in the analysis of multiple claim elements with respect to Tsunoda, Tsunoda's memory apparatus includes silicon chips that are sealed in one package and housed in a memory card shape such as an MMC:

> The memory apparatus 4000 [FIG. 24] constructs, for example **the SDRAM 4010, the flash memory 4020, and the control unit 4030 on different silicon chips**, and interconnects terminals of the

silicon chips by, for example wire bonding, thereby providing a multichip package, in which the components are **sealed in one package**. Here, the package indicates an LSI package form such as a thin small outline package (TSOP), or a ball grid array (BGA).

MTI-1004, [0056].

The memory apparatus 101 [FIG. 1], 901 [FIG. 9], 1301 [FIG. 13] and 1401 [FIG. 14] of the present invention can be applied to any shapes. For example, the apparatus may be a LSI, in which **memory chips and a control chip are sealed in one package**, or all the functions may be housed on one semiconductor chip. The components may be **housed in a memory card shape** such as an MMC.

MTI-1004, [0124]. Further, Sukegawa discloses that:

In the illustrated embodiment of FIGS. 1 and 2, a single semiconductor device 200 can be used to house these electrical circuit components. To accomplish this, the electrical circuit components may be implemented as one or more interconnected circuit modules, which may be held in place with a molding compound 225 or resin within the device. FIG. 3 shows an example of how **an integrated semiconductor memory device**, such as device 200, can stack multiple interconnected smaller devices (referred to as chips) and fill the remaining space within the device with molding compound or resin according to an embodiment of the present invention. Referring now to FIG. 3, device 200 is illustrated as **a multi-chip package 305 where chip A300A is glued on top of chip B 300B, which is then further glued on top of chip C**

300C, Chip C 300C is attached to a substrate layer 310 above the bottom 320 of device 200. Each of chips 300A-C may be insulated from each other and are connected to one or more connection pads 350 using wires 340A-C, respectively. Further, these connections may be in communication with solder connections 330 disposed on the bottom 320 of the device 200. While FIG. 3 shows sires 340A-340C by wire-bonding, those skilled in the art will appreciate that connections from chips A-C to connection pads may be implemented with other **electrical interconnection techniques, such as by through-holes and solder bumps**.

Those skilled in the art will appreciate that the solder connections 330 are solder balls or bumps for use in surface mounting the device 200 and that other connection topologies are contemplated for use in other embodiments of the invention. In one embodiment, the package 305 is implemented by a **conventional P-FBGA package**. However, other conventional and new packages may be used to implement embodiments of the invention depending on the available physical space within the USB connector and the desired functionality of the memory apparatus. electrical circuit components in distinct and separate **circuit modules** that can be electrically connected when mounted within different parts of the USB connector. In other words, alternative embodiments of the present invention may implement the device in separate modules (each of which may be a multichip package have one or more chips) to more readily take advantage of the limited available space within the physical confines of the USB connector shield case.

MTI-1005, 6:42-7:18, 4:48-50, 8:6-9:16, FIGS. 3, 5A-5H.

116. Based on my knowledge and experience in this field and my review of Tsunoda and Sukegawa, Tsunoda-Sukegawa's USB flash drive includes SDRAM, flash memory, and memory control unit on different silicon chips, and interconnects terminals of the silicon chips by, for example, wire bonding, through-holes, or solder bumps. A POSITA would have found it obvious that Tsunoda-Sukegawa's USB flash drive, which includes the SDRAM, flash memory, and memory control unit on different silicon chips housed in a USB connector shield case 120 that "extends from an overmold boot" "on an end of the connector opposite the contact terminals" and an end cap 110, as shown below, does not have any moving parts. MTI-1004, [0124]; MTI-1005, 4:58-59, 7:26-32, FIGS. 1, 5G. Cheng (U.S. Patent Application Publication No. 2002/0010827) confirms that "a portable data storage device comprising a coupling device with an interface device, memory control device and a non-volatile solid-state memory device ... does not include moving parts..." so as "to be more compact than conventional portable data storage devices." MTI-1012, [0005], [0031].

portable memory apparatus

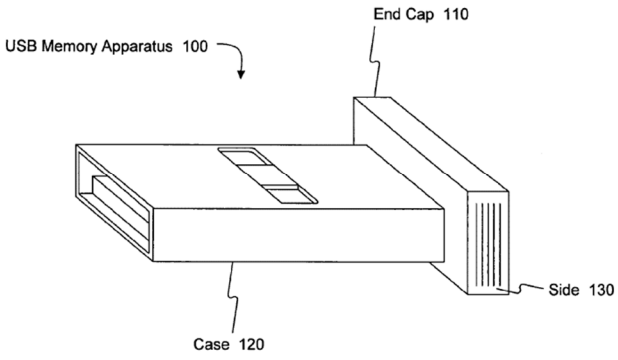


FIG. 1

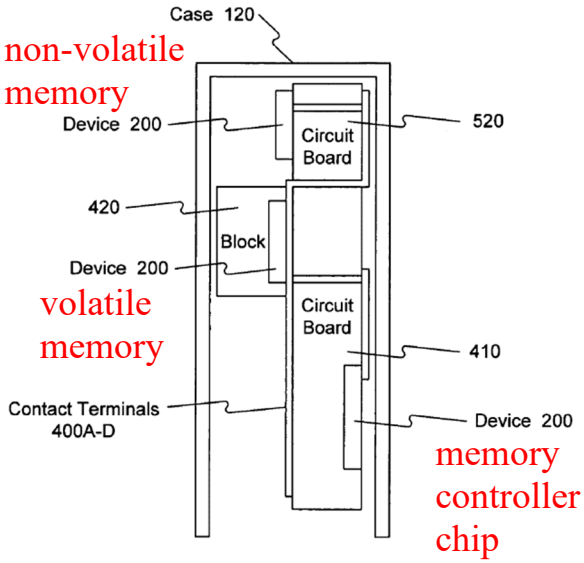


FIG. 5G

MTI-1005, FIGS. 1 , 5G

10. Claim 15

(a) Element 15[p]

117. The preamble of claim 15 recites "[a] method." The combination of Tsunoda and Sukegawa provides a method as recited in the preamble of claim 15 as set forth below in the analysis of claim elements 15[a]-15[e] with respect to the combination of Tsunoda and Sukegawa.

(b) Element 15[a]

118. Claim element 15[a] recites "coupling a portable memory apparatus to a computer system." For the reasons discussed in the analysis of claim elements

1[p] and 1[e] with respect to the combination of Tsunoda and Sukegawa, the combination of Tsunoda and Sukegawa provides claim element 15[a].

(c) Element 15[b]

119. Claim element 15[b] recites "wherein said portable memory apparatus comprises a memory controller chip, a non-volatile memory, and a volatile memory." For the reasons discussed in the analysis of claim elements 1[b], 1[c], 1[d] with respect to the combination of Tsunoda and Sukegawa, the combination of Tsunoda and Sukegawa provides claim element 15[b].

(d) Element 15[c]

120. Claim element 15[c] recites "copying data from said non-volatile memory to said volatile memory using said memory controller chip." For the reasons discussed in the analysis of claim element 1[f] with respect to the combination of Tsunoda and Sukegawa, the combination of Tsunoda and Sukegawa provides claim element 15[c].

(e) Element 15[d]

121. Claim element 15[d] recites "accessing said data in said volatile memory using said computer system through a connector coupled to said portable memory apparatus and said memory controller chip." For the reasons discussed in the analysis of claim element 1[f] with respect to the combination of Tsunoda and Sukegawa, the combination of Tsunoda and Sukegawa provides claim element 15[d].

(f) Element 15[e]

122. Claim element 15[e] recites "updating said non-volatile memory with data from said volatile memory." For the reasons discussed in the analysis of claim 6 with respect to the combination of Tsunoda and Sukegawa, the combination of Tsunoda and Sukegawa provides claim element 15[e].

11. Claim 18

123. Claim 18 recites:

> The method of claim 15, further comprising: indicating when data stored in said volatile memory has been transferred to said non-volatile memory.

For the reasons discussed in the analysis of claim 7 with respect to the combination of Tsunoda and Sukegawa, the combination of Tsunoda and Sukegawa provides claim 18.

C. Analysis of Tsunoda, alone or with Sukegawa, in view of Tomio with respect to Claims 2-5 and 16-17

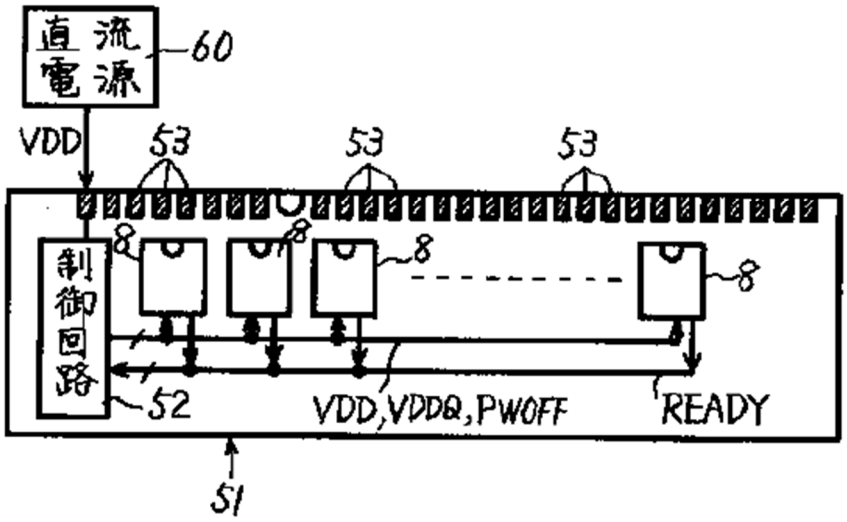
124. For the reasons articulated in detail below, and based on my review of the '527 patent and the Tsunoda, Sukegawa, and Tomio references, I am confident that a POSITA would have readily understood that Tsunoda, alone or with Sukegawa, in view of Tomio renders obvious all elements of claims 2-5 and 16-17.

1. Overview of Tomio

125. Tomio relates to "a semiconductor memory apparatus that can be accessed quickly and that has nonvolatile data." MTI-1006, [0001], [0005], [0045].

Tomio's FIG. 11 (below) shows an example of a memory module 51 that includes semiconductor memories 8 and a control circuit 52. MTI-1006, [0038]. The module 51 "operates as a single memory unit" with semiconductor memories 8 mounted on a substrate such as "a Mitsubishi Electric 256 MB 168 pin unbuffered dual inline module." MTI-1006, [0037]. "This 256 MB module can also be used as the main memory in a personal computer by pre-storing data that is usually stored in ROM in the flash memory 11 of the semiconductor memory 8." MTI-1006, [0037].

【図１１】



MTI-1006, FIG. 11

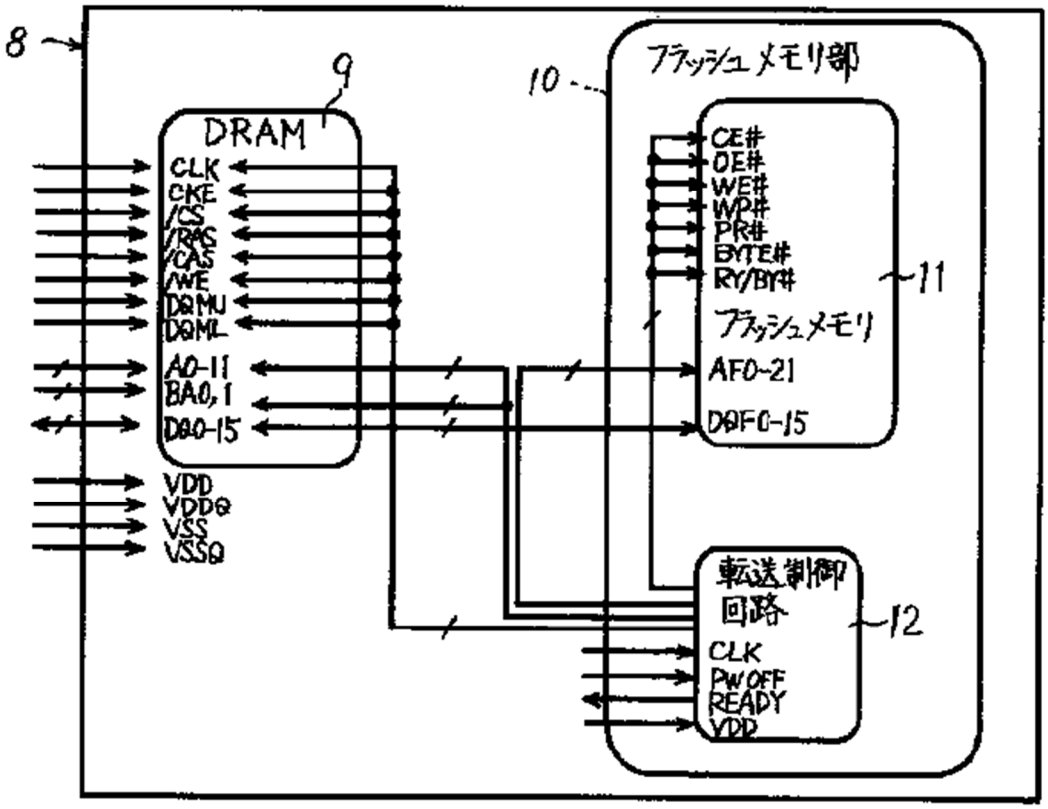
126. "The control circuit 52 receives direct current power supply potential VDD from a direct current power supply 60 outside of the module 51 via an input terminal 53, and supplies direct current power supply potentials VDD and VDDQ to each semiconductor memory 8 in the module 51." MTI-1006, [0038]. "Also, the control circuit 52 supplies a PW OFF signal to each semiconductor memory 8 in

response to the supply of the direct current power supply potential VDD from the direct current power supply 60 being stopped." MTI-1006, [0038]. "The control circuit 52 includes a rechargeable battery 61" (FIG. 12) that "is charged with the direct current power supply potential VDD from the direct current power supply 60 and outputs direct current power supply potentials VDD and VDDQ." MTI-1006, [0039]. "The rechargeable battery 61 continues to output direct current power supply potentials VDD and VDDQ for a predetermined period of time even when supply of the direct current power supply potential VDD from the direct current power supply 60 has been stopped." MTI-1006, [0039], [0027].

127. Each semiconductor memory 8 includes "DRAM 9 and a flash memory unit 10, and the flash memory unit 10 includes flash memory 11 and a transfer control circuit 12," as shown in FIG. 2 (below). MTI-1006, [0018], [0043]. The DRAM 9 stores data supplied from a personal computer during a write operation and supplies read data to the personal computer during a read operation. MTI-1006, [0019], [0025], [0032]. The DRAM 9 also receives signals from the transfer control circuit 12 during data fetching and data storage, stores read data in the flash memory 11 during data fetching, and supplies read data to the flash memory 11 during data storage. MTI-1006, [0020]. The flash memory 11 receives signals from the transfer control circuit 12, stores read data from the DRAM 9 during data storage, and supplies read data to the DRAM 9 during data fetching. MTI-1006, [0021]. "The

transfer control circuit 12 transfers data stored in the flash memory 11 to the DRAM 9 in response to the rising edge of the power supply potential VDD, and erases all of the data in the flash memory 11 after completing the data transfer." MTI-1006, [0022]-[0024], [0032]. "The data in the flash memory 11 is erased in this manner because all data in the memory cells has to be erased in order to write data to a flash memory 11." MTI-1006, [0026]. In addition, the transfer control circuit 12 transfers data in the DRAM 9 to the flash memory 11 in response to a PW OFF signal from the personal computer. MTI-1006, [0022], [0028], [0032].

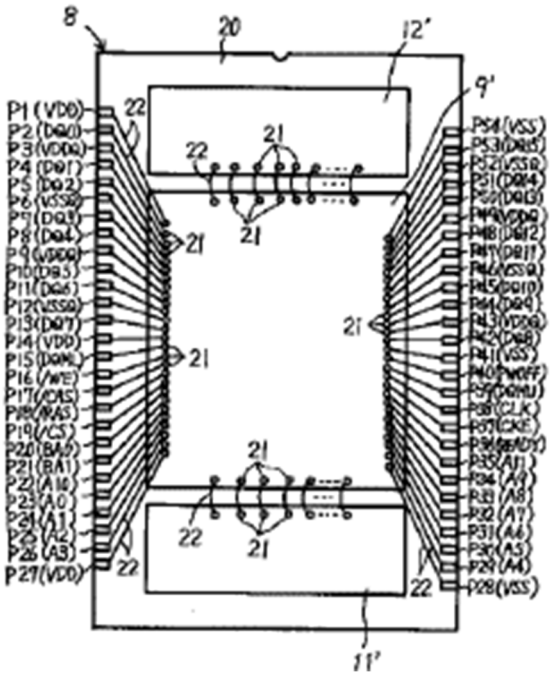
【図２】



MTI-1006, FIG. 2

128. Each semiconductor memory 8 includes "DRAM, flash memory, and transfer control circuit... sealed in a single package." MTI-1006, [0043]. FIG. 7 (below) shows a possible configuration of the semiconductor memory 8 with input/output pins P1-P54, a DRAM chip 9′, a flash memory chip 11′, and a transfer control circuit chip 12′ connected via pads 21 and bonding wires 22 provided in a package 20. MTI-1006, [0030]-[0031]. Tomio also describes other configurations with chips "stacked inside the package" and "sealed with a resin" so that the area occupied by the chips is reduced and the package "can be made smaller." MTI-1006, [0034]-[0035], FIGS. 8-9.

【図7】



MTI-1006, FIG. 7

2. Combination of Tsunoda, alone or with Sukegawa, and Tomio

129. Tsunoda discloses that "when power is turned OFF, a content of the volatile memory is copied in the nonvolatile memory, and a result of its processing is notified through an exclusive line to the host" and consequently, "power is safely turned OFF, and data is held even after the power is OFF." MTI-1004, [0002]. However, Tsunoda does not account for the situation where power is abruptly turned off (by unplugging or power outage) before the transfer starts or before the transfer completes. In this situation, data that is not copied from the volatile memory to the nonvolatile memory will be lost. MTI-1004, [0075] ("Since the SDRAM 4010 is a volatile memory, data written in the SDRRAM 4010 is lost when the power supply to the memory apparatus 4000 is stopped."); MTI-1006, [0002] (DRAMs currently used in a wide variety of applications can be accessed at high speed, but are volatile memories that lose stored information when the power is turned off."), [0032], [0039], [0027]; MTI-1007, [0009]-[0012] ("data stored in the volatile RAM is also lost when the remaining battery power is low and the battery dies."), [0061].

130. In the event that the external power supply is abruptly stopped, Tomio's module includes a "rechargeable battery" that "continues to output direct current power supply potentials VDD and VDDQ for a predetermined period of time even when supply of the direct current power supply potential VDD from the direct current power supply 60 has been stopped," a "control circuit" that "supplies a PW

OFF signal to each semiconductor memory 8 in response to the supply of the direct current power supply potential VDD from the direct current power supply 60 being stopped," and a "transfer control circuit" that "transfers data in the DRAM 9 to the flash memory 11 in response to a PW OFF signal." MTI-1006, [0038]-[0039], [0022], [0027]-[0028], [0032]. A POSITA would have been motivated to apply the teachings of Tomio to Tsunoda's and Tsunoda-Sukegawa's memory apparatus to provide a memory apparatus with a rechargeable battery that continues to supply power long enough for the memory controller to copy data from volatile memory to nonvolatile memory in the event that the external power to the memory apparatus is abruptly stopped. MTI-1004, [0002]; MTI-1006, [0039], [0027].

131. Tsunoda expressly contemplates that its memory apparatus holds data even after the power is OFF using a nonvolatile memory. MTI-1004, [0002], [0039], [0075], [0098], [0112]. A POSITA implementing Tsunoda's and Tsunoda-Sukegawa's memory apparatus would have turned to examples of similar memory apparatus to identify additional suitable techniques for retaining data after the power is off. Tomio's teachings enable implementation of a memory apparatus, such as that described in Tsunoda, where the memory controller includes functionality for copying data from volatile memory to nonvolatile memory using power supplied by a rechargeable battery to achieve Tsunoda's goals of retaining data after the power is off. *Id.*; MTI-1006, [0039], [0027]. A POSITA would have been motivated to

apply the teachings of Tomio regarding the provision of a back-up power supply and corresponding memory controller functionality to Tsunoda's or Tsunoda-Sukegawa's memory apparatus to beneficially provide a memory apparatus that retains data even when the external power supply is abruptly stopped. *Id.*

132. Accordingly, a POSITA would have found it obvious and would have been motivated to implement Tsunoda's and Tsunoda-Sukegawa's memory apparatus with a rechargeable battery that supplies power and functionality in the memory controller for transferring data from volatile memory to nonvolatile memory after the external power supply has been stopped or turned off based on Tomio's teachings. *Id*. A POSITA would have viewed the implementation of Tsunoda's and Tsunoda-Sukegawa's memory apparatus in a manner that applied Tomio's suggestion regarding a rechargeable battery and corresponding memory controller functionality as merely the predictable result of combining known prior art elements according to known methods. A POSITA would have had a reasonable expectation of success in doing so as such an implementation was well-known as demonstrated by Tomio and commonly utilized in similar memory apparatus. *Id.* A POSITA would have recognized that the above described modifications would have yielded predictable results, would have been within the ordinary level of skill of a POSITA, and would not have required undue experimentation, as it is simply the inclusion of a back-up power supply and corresponding memory controller

functionality. *Id.* A POSITA would have been capable of employing ordinary creativity to carry out an implementation of the memory apparatus with the rechargeable battery and corresponding memory controller functionality in a manner necessary to achieve the advantages taught by Tomio by, for example, varying the size and shape of the memory apparatus and housing (as taught by Tsunoda or Sukegawa) to accommodate the electronic components and rechargeable battery, as corroborated by other publications illustrating USB flash drives in varying shapes and sizes. *Id*.; *see, e.g.,* MTI-1013; MTI-1017; MTI-1018; MTI-1019; MTI-1020.

3. Claims 2, 4, and 5

133. Claim 2 recites:

> The portable memory apparatus of claim 1, further comprising an internal power source coupled to said portable memory apparatus.

Claim 4 recites:

> The portable memory apparatus of claim 2, wherein said internal power source is rechargeable through said connector.

Claim 5 recites:

> The portable memory apparatus of claim 4, wherein said internal power source comprises a battery or a capacitor.

The combination of Tsunoda, alone or with Sukegawa, and Tomio provides claims 2, 4, and 5.

134. For example, Tomio describes a memory module that includes a rechargeable battery:

> In the modified example shown in Fig. 11, the module 51 is composed of a plurality of semiconductor memories 8 and a control circuit 52. The **control circuit 52 receives direct current power supply potential VDD from a direct current power supply 60 outside of the module 51 via an input terminal 53**, and supplies direct current power supply potentials VDD and VDDQ to each semiconductor memory 8 in the module 51.
>
> ...
>
> The control circuit 52 includes **a rechargeable battery 61**, an internal power supply switch 62, a signal generating circuit 63, and an AND gate 64. **The rechargeable battery 61 is charged with the direct current power supply potential VDD from the direct current power supply 60** and outputs direct current power supply potentials VDD and VDDQ. The rechargeable battery 61 continues to output direct current power supply potentials VDD and VDDQ for a predetermined period of time even when supply of the direct current power supply potential VDD from the direct current power supply 60 has been stopped.

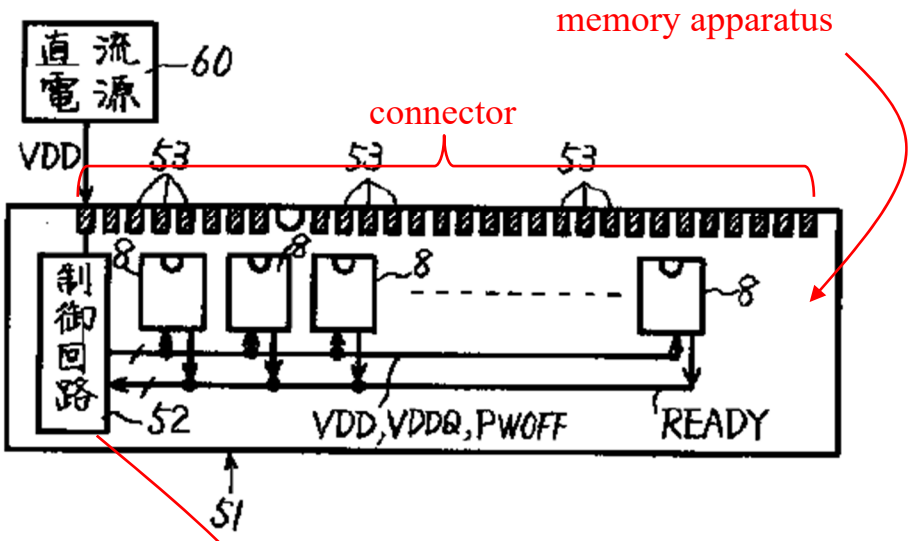
MTI-1006, [0038]-[0039].

> When the external power supply switch 15 is turned off in ③ (time t3), the signal φ1 reaches the "L" level and the supply of the alternating current power supply voltage VAC for the direct current power supply 6 is stopped. Because the direct current power supply

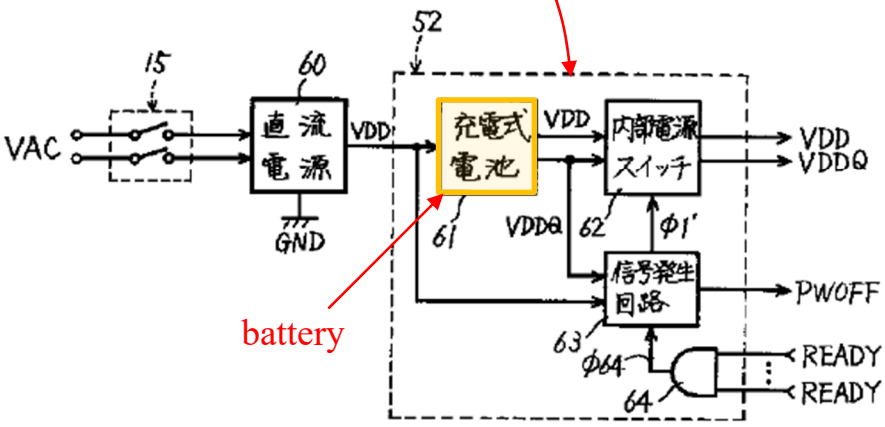
> 6 includes **rechargeable batteries** as described above, it continues to output power supply voltages VCC, VDD, and VDDQ even when the supply of the alternating current power supply voltage VAC is stopped.

MTI-1006, [0027]. As shown in Tomio's FIGS. 11 and 12 (below), "control circuit 52 receives direct current power supply potential VDD from a direct current power supply 60 outside of the module 51 via an input terminal 53" (of the connector). MTI-1006, [0038].

【図１１】



【図１２】



MTI-1006, FIGS. 11, 12 (collated, annotated)

135. For the Tsunoda MMC, the MMC interface provides a terminal for receiving power from the host:

> As shown in FIG. 10, **the MMC interface** 907 includes totally seven terminals, i.e., a chip select terminal (CS) 1001, a command terminal (CMD) 1002, two ground terminals (GND 1) 1003 and 1006, **a power supply terminal (VCC 1) 1004 from the host** 906,

a clock terminal (CLK1) 1005, and data (DAT) 1007.

MTI-1004, [0114]. For the Tsunoda-Sukegawa USB flash drive, the USB interface or connector provides a terminal for receiving power from a host system:

> A set of **contact terminals 400A-D** is shown disposed on a portion of the top side of a first circuit board 410 within the USB connector shield case 120. As shown in FIG. 4B, the set of contact terminals 400A–D are arranged in a standard USB configuration to line up with a mating USB interface or connector. In this manner, terminal 400A is deemed to be ground, terminal 400B is deemed to be +D, terminal 400C is deemed to be -D, and **terminal 400D is deemed to be +V_{BUS} according to the USB standard**.

MTI-1005, 7:26-52. Based on my knowledge and experience in this field and my review of Tsunoda, Sukegawa, and Tomio, a POSITA would have found it obvious to include a rechargeable battery (internal power source) in Tsunoda-Tomio's and Tsunoda-Sukegawa-Tomio's memory apparatus (portable memory apparatus) that is rechargeable through its respective connectors to provide a memory apparatus with a rechargeable battery that continues to supply power long enough to copy data from volatile memory to nonvolatile memory in the event that the external power to the memory apparatus is abruptly stopped. MTI-1004, [0002]; MTI-1006, [0038]-[0039], [0027].

4. Claim 3

136. Claim 3 recites:

> The portable memory apparatus of claim 2, wherein said internal power source powers said portable memory apparatus when said portable memory apparatus is unplugged from said computer system, said portable memory apparatus copies data from said volatile memory to said non-volatile memory when said portable memory apparatus is unplugged from said computer system.

The combination of Tsunoda, alone or with Sukegawa, and Tomio provides claim 3.

For example, Tomio discloses that:

> The rechargeable battery 61 continues to output direct current power supply potentials VDD and VDDQ for a predetermined period of time even when supply of the direct current power supply potential VDD from the direct current power supply 60 has been stopped.

MTI-1006, [0039].

> When the external power supply switch 15 is turned off in ③ (time t3), the signal φ1 reaches the "L" level and the supply of the alternating current power supply voltage VAC for the direct current power supply 6 is stopped. Because the direct current power supply 6 includes **rechargeable batteries** as described above, it **continues to output power supply voltages VCC, VDD, and VDDQ even when the supply of the alternating current power supply voltage VAC is stopped**.

MTI-1006, [0027]. Based on my knowledge and experience in this field, a POSITA would have found it obvious that "supply of the direct current power supply potential VDD from the direct current power supply 60 has been stopped" when the module

51 is unplugged from the personal computer or when the personal computer powers off.

137. Tomio further teaches that:

> The **DRAM** 9 receives a clock signal CLK, control signals CKE, /CS, /RAS, /CAS, /WE, DQMU, and DQML, and address signals A0 to A11, BA0, and BA1 from the memory controller 5 during normal operations, and **stores data DQ0 to DQ15 supplied from the memory controller 5 during a write operation, and supplies read data to the memory controller 5 during a read operation**.

MTI-1006, [0019].

> The transfer control circuit 12 transfers data stored in the flash memory 11 to the DRAM 9 in response to the rising edge of the power supply potential VDD, and erases all of the data in the flash memory 11 after completing the data transfer. In addition, the **transfer control circuit 12 transfers data in the DRAM 9 to the flash memory 11 in response to a PW OFF signal** from the memory controller 5, and sends a READY to signal the memory controller 5 in response to completing the data transfer.

MTI-1006, [0022].

> During normal operations, the semiconductor memory 8 operates as a DRAM 9 from the perspective of the memory controller 5. The DRAM 9 is in an idle state or access standby when not accessed by the memory controller 5 (⑥), and reads and writes data when accessed (⑦).

MTI-1006, [0025].

> In the present embodiment, a DRAM 9, flash memory 11, and transfer control circuit 12 are provided in a semiconductor memory 8, data in the flash memory 11 is transferred to the DRAM 9 in response to the external power supply switch 15 of the personal computer being turned on, the DRAM 9 is used as the semiconductor memory 8 and data in flash memory 11 is erased during normal operations, and **data in the DRAM 9 is stored in the flash memory 11 in response to the external power supply switch 15 being turned off**. **In this way, a semiconductor memory 8 can be realized that enables high-speed access like a DRAM but has data nonvolatility like a flash memory**.

MTI-1006, [0032]. Based on my knowledge and experience in this field and my review of Tsunoda, Sukegawa, and Tomio, a POSITA would have found it obvious to include the rechargeable battery to supply power for Tsunoda-Tomio's and Tsunoda-Sukegawa-Tomio's memory apparatus to copy data from the SDRAM (volatile memory) to the flash memory (non-volatile memory) in response to the external power supply being stopped or turned off, e.g., when the memory apparatus is unplugged from the host (computer system), to beneficially provide a memory apparatus that enables high-speed access like a DRAM but has data nonvolatility like a flash memory. *Id.*

5. Claim 16

138. Claim 16 recites:

> The method of claim 15, further comprising: powering said portable memory apparatus with an internal power source coupled to said portable memory apparatus, when said portable memory apparatus is unplugged from said computer system, to transfer said non-volatile memory with data from said volatile memory.

For the reasons discussed in the analysis of claims 2 and 3 with respect to the combination of Tsunoda, alone or with Sukegawa, and Tomio, the combination of Tsunoda, alone or with Sukegawa, and Tomio provides claim 16.

6. Claim 17

139. Claim 17 recites:

> The method of claim 15, further comprising: recharging an internal power source coupled to said portable memory apparatus.

For the reasons discussed in the analysis of claim 4 with respect to the combination of Tsunoda, alone or with Sukegawa, and Tomio, the combination of Tsunoda, alone or with Sukegawa, and Tomio provides claim 17.

D. Analysis of Tomio with respect to Claims 1-6, 9, 12, and 15-17

140. I have been informed that, in its complaint for infringement, Patent Owner appears to advance a scope for the terms "portable" and "housing" with which Petitioner disagrees. Specifically, Patent Owner identifies Petitioner's memory devices having a M.2 form factor (a specification for internally mounted computer cards) as allegedly infringing claims of the '527 patent. MTI-1021, 3 (listing accused products as including, e.g., 3400 SSD with NVMe, Crucial P5 Plus

with NVMe, Crucial P3 with NVMe, among other M.2 form factor memory devices). Below, I address claims 1-6, 9, 12, and 15-17 under the scope of these claim terms advanced by Patent Owner in its complaint for infringement.

1. Claim 1

(a) Element 1[p]

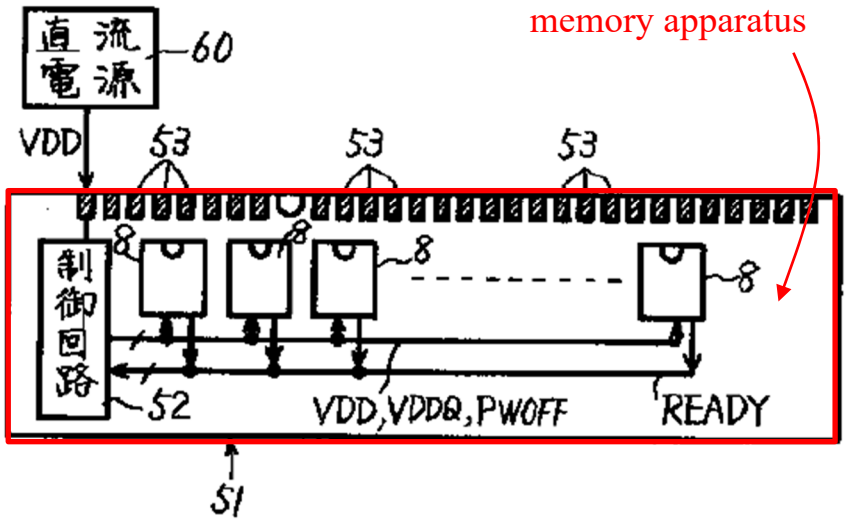
141. The preamble of claim 1 recites "[a] portable memory apparatus." Tomio provides the preamble of claim 1 in accordance with the scope of the term "portable" advanced by Patent Owner in its complaint for infringement. For example, Tomio discloses that:

> Also, as shown in Fig. 10, **a module 50 that operates as a single memory unit may be constructed by assembling a plurality of semiconductor memories 8**. For example, a 256 MB fast access nonvolatile memory can be realized by mounting eight semiconductor memories 8 in the present invention on the substrate of **a Mitsubishi Electric 256 MB 168 pin unbuffered dual inline module**. **This 256 MB module can also be used as the main memory in a personal computer** by pre-storing data that is usually stored in ROM in the flash memory 11 of the semiconductor memory 8. As a result, the data transfer bus between the ROM and the main memory on the motherboard of a conventional personal computer, the bus control circuit, and the ROM become unnecessary. In addition, a module formed using a semiconductor memory 8 of the present invention may be used instead of a conventional floppy disk or CDROM.

> In the modified example shown in Fig. 11, **the module 51 is composed of a plurality of semiconductor memories 8** and a control circuit 52. The control circuit 52 receives direct current power supply potential VDD from a direct current power supply 60 outside of the module 51 via an input terminal 53, and supplies direct current power supply potentials VDD and VDDQ to each semiconductor memory 8 in the module 51. Also, the control circuit 52 supplies a PW OFF signal to each semiconductor memory 8 in response to the supply of the direct current power supply potential VDD from the direct current power supply 60 being stopped, and the supply of the direct current power supply potentials VDD and VDDQ to each semiconductor memory 8 is stopped when a READY signal has been outputted from all of the semiconductor memories 8.

MTI-1006, [0037]-[0038]. Tomio's FIG. 11 (below) shows an example of a memory module 51 that includes semiconductor memories 8. MTI-1006, [0038]. In accordance with the scope of the term "portable" advanced by Patent Owner in its complaint for infringement, Tomio's memory module 51 is labeled as a "portable memory apparatus" in the figure below, as Tomio's 168 pin unbuffered dual inline module is a form factor that is similar to the M.2 form factor that Patent Owner alleges satisfies this claim element. MTI-1021, 3; MTI-1016; MTI-1024.

【図１１】



MTI-1006, FIG. 11

(b) Element 1[a]

142. Claim element 1[a] recites "a housing." Tomio provides claim element 1[a] in accordance with the scope of the term "housing" advanced by Patent Owner in its complaint for infringement. As discussed in the analysis of claim element 1[p] with respect to Tomio, Tomio's memory module 51 includes semiconductor memories 8 and a control circuit 52 mounted on a substrate such as "a Mitsubishi Electric 256 MB 168 pin unbuffered dual inline module," as shown in FIG. 11 (above). MTI-1006, [0037]-[0038]. Tomio further discloses that:

> In the modified example shown in Fig. 11, **the module 51 is composed of a semiconductor memory 8 in which the DRAM, flash memory, and transfer control circuit are sealed in a single package**. However, the present invention is not limited to this modified example, and a chip in which the transfer control circuit is

realized using a conventional DRAM, flash memory, ASIC, etc. may be mounted separately on the module board.

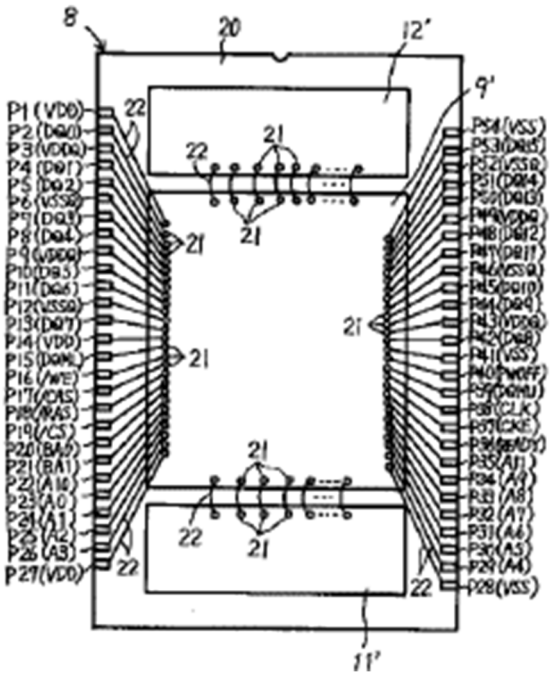
MTI-1006, [0043].

Fig. 7 is a diagram showing the configuration of the semiconductor memory 8. A DRAM chip 9' is provided in the center of the package 20, a flash memory chip 11' is provided on the lower side in the figure, and a transfer control circuit chip 12' is provided on the upper side in the figure. Chips 9', 11' and 12' are connected via pads 21 and bonding wires 22.

A plurality of pins P1 to P54 are arranged at a predetermined pitch along both long sides of the package 20. Each of pins P1 to P54 is connected via a bonding wire 22 to a pad 21 of the DRAM chip 9'. Pins P1 to P54 are used to apply power supply potentials VDD, VDDQ and ground potentials VSS, VSSQ, input clock signal CLK, control signals CKE, /CS, /RAS, /CAS, /WE, DQMU, and DQML, address signals A0 to A11, BA0, and BA1, input and output data DQ0 to DQ15, input the PW OFF signal, and output the READY signal.

MTI-1006, [0030]-[0031]. FIG. 7 shows a possible configuration of the semiconductor memory 8 with input/output pins P1-P54, a DRAM chip 9', a flash memory chip 11', and a transfer control circuit chip 12' connected via pads 21 and bonding wires 22 provided in a package 20.

【図7】



MTI-1006, FIG. 7

Tomio also describes other configurations:

> Modified examples of this embodiment will now be described. In the modified example shown in Fig. 8, a DRAM chip 9' is provided in the central portion of the package 30, and the chip 10' for the flash memory unit 10 is provided on the surface of the DRAM chip 9' in the central portion. These chips 9' and 10' are connected via a plurality of pads 21 and bonding wires 22. Note that the pins have been omitted to simplify the drawing. Because the **chips 9' and 10' are stacked inside the package 30** in this modified example, the area occupied by the chips 9', 10' is reduced, and the package 30 can be made smaller.
>
> In the modified example shown in Fig. 9, a DRAM chip 9' is provided in the central portion of the package 40, and a chip 10' for

> the flash memory unit 10 is provided on the surface of the DRAM chip 9' in the central portion. These chips 9' and 10' are connected via a plurality of balls 41. The pads 21 of the DRAM chip 9' are connected to external pins P via bonding wires 22. These chips 9', 10' are sealed with a resin 42. In this modified example, **the chips 9', 10' are stacked inside the package 40**, and the chips 9', 10' are connected via balls 41. In this way, the area occupied by the chips 9', 10' is reduced, and the package 40 can be made smaller.

MTI-1006, [0034]-[0035], FIGS. 8-9. In accordance with the scope of the term "housing" advanced by Patent Owner in its complaint for infringement, Tomio's memory module 51 includes packages in which the semiconductor memories 8 are provided and a substrate on which the semiconductor memories 8 and the control circuit 52 are mounted similar to the M.2 form factor memory devices that Patent Owner alleges satisfies this claim element. MTI-1021, 3; MTI-1024.

(c) Element 1[b]

143. Claim element 1[b] recites "a memory controller comprised in the housing." Tomio provides claim element 1[b]. For example, Tomio discloses a transfer control circuit that controls the transfer of data between the memories:

> In addition, the **DRAM 9 receives** clock signal CLK, **control signals** CKE, /CS, /RAS, /CAS, /WE, DQMU, and SQML, **and address signals** A0 to A11, BA0, and BA1 **from the transfer control circuit 12 during data fetching and data storage**, stores read data DQF0 to DQF15 in the flash memory 11 during data

fetching, and supplies read data DQ0 to DQ15 to the flash memory 11 during data storage.

The **flash memory 11 receives control signals** CE#, OE#, WE#, WP#, PR#, BYTE#, and RY/BY# **and address signals** AF0 to AF21 **from the transfer control circuit 12**, and stores read data DQ0 to DQ15 from the DRAM 9 during data storage, and supplies read data DQF0 to DQF15 to the DRAM 9 during data fetching.

The transfer control circuit 12 transfers data stored in the flash memory 11 to the DRAM 9 in response to the rising edge of the power supply potential VDD, and erases all of the data in the flash memory 11 after completing the data transfer. In addition, the **transfer control circuit 12 transfers data in the DRAM 9 to the flash memory 11** in response to a PW OFF signal from the memory controller 5, and sends a READY to signal the memory controller 5 in response to completing the data transfer.

MTI-1006, [0020]-[0023].

After a predetermined amount of time has passed since the rising edge of the power supply potential VDD (time t0), **the transfer control circuit 12 fetches data** in ② (times t1 to t2). In other words, as shown in Fig. 5, **read address signals** AF0 to AF21 and **read commands** (with signals CE# and OE# set to the "L" level and signals WE# and PR# set to the "H" level) synchronized with the clock signal CLK **are supplied from the transfer control circuit 12 to the flash memory 11**. Meanwhile, **a write command (WR) and write address signals** A0 to A15 **are supplied from the transfer control circuit 12 to the DRAM 9**, and the data stored in

the flash memory 11 is fetched and stored in the DRAM 9.

MTI-1006, [0024], [0032].

In addition, a PW OFF pulse signal is outputted from the memory controller 5 to the transfer control circuit 12 in response to the falling edge of signal φ1 at the "L" level, and **data storage** in ④ **is performed in response by the transfer control circuit 12** (times t3 to t4). In other words, as shown in Fig. 6, **a read command (RD) and read address signals** A0 to A15 synchronized with the clock signal CLK **are supplied from the transfer control circuit 12 to the DRAM 9**. Meanwhile, **write commands** (with signals CE# and WE# set to the "L" level and signals OE# and PR# are set to the "H" level) **and write address signals** AF0 to AF21 **are transferred from the transfer control circuit 12 to the flash memory 11**. Data stored in the DRAM 9 is fetched and stored in the flash memory 11.

MTI-1006, [0028], [0032].

144. Tomio also discloses that the transfer control circuit is provided inside a package:

In other words, as shown in Fig. 2, the semiconductor memory 8 includes DRAM 9 and a flash memory unit 10, and the flash memory unit 10 includes flash memory 11 and **a transfer control circuit 12**.

MTI-1006, [0018].

Fig. 7 is a diagram showing the configuration of the semiconductor memory 8. A DRAM chip 9' is provided in the center of **the package 20**, a flash memory chip 11' is provided on the lower side in the

figure, and **a transfer control circuit chip 12' is provided on the upper side** in the figure. **Chips 9', 11' and 12' are connected via pads 21 and bonding wires 22**.

A plurality of pins P1 to P54 are arranged at a predetermined pitch along both long sides of the package 20. Each of pins P1 to P54 is connected via a bonding wire 22 to a pad 21 of the DRAM chip 9'. Pins P1 to P54 are used to apply power supply potentials VDD, VDDQ and ground potentials VSS, VSSQ, input clock signal CLK, control signals CKE, /CS, /RAS, /CAS, /WE, DQMU, and DQML, address signals A0 to A11, BA0, and BA1, input and output data DQ0 to DQ15, input the PW OFF signal, and output the READY signal.

MTI-1006, [0030]-[0031].

Modified examples of this embodiment will now be described. In the modified example shown in Fig. 8, a DRAM chip 9' is provided in the central portion of the package 30, and the chip 10' for the flash memory unit 10 is provided on the surface of the DRAM chip 9' in the central portion. These chips 9' and 10' are connected via a plurality of pads 21 and bonding wires 22. Note that the pins have been omitted to simplify the drawing. Because the **chips 9' and 10' are stacked inside the package 30** in this modified example, the area occupied by the chips 9', 10' is reduced, and the package 30 can be made smaller.

In the modified example shown in Fig. 9, a DRAM chip 9' is provided in the central portion of the package 40, and a chip 10' for the flash memory unit 10 is provided on the surface of the DRAM

chip 9' in the central portion. These chips 9' and 10' are connected via a plurality of balls 41. The pads 21 of the DRAM chip 9' are connected to external pins P via bonding wires 22. These chips 9', 10' are sealed with a resin 42. In this modified example, **the chips 9', 10' are stacked inside the package 40, and the chips 9', 10' are connected via balls 41**. In this way, the area occupied by the chips 9', 10' is reduced, and the package 40 can be made smaller.

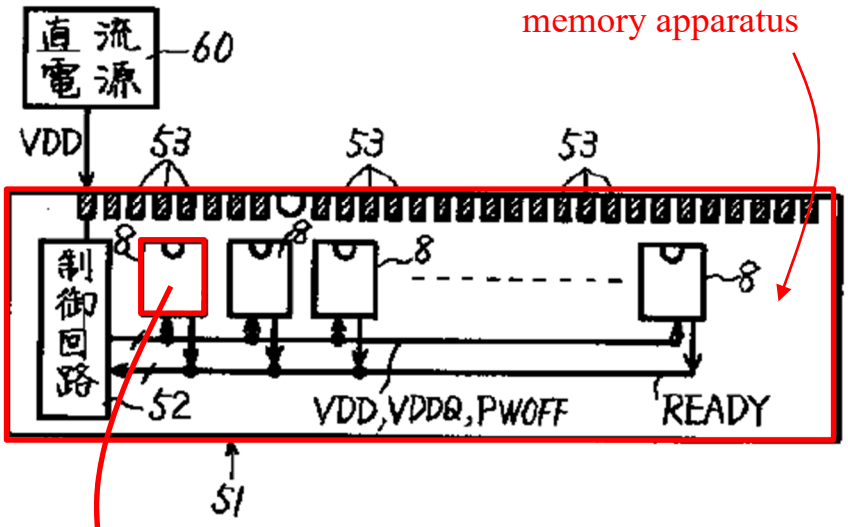
MTI-1006, [0034]-[0035], FIGS. 8-9.

In the modified example shown in Fig. 11, the module 51 is composed of a semiconductor memory 8 in which the DRAM, flash memory, and **transfer control circuit are sealed in a single package**. However, the present invention is not limited to this modified example, and a chip in which the transfer control circuit is realized using a conventional DRAM, flash memory, ASIC, etc. may be mounted separately on the module board.

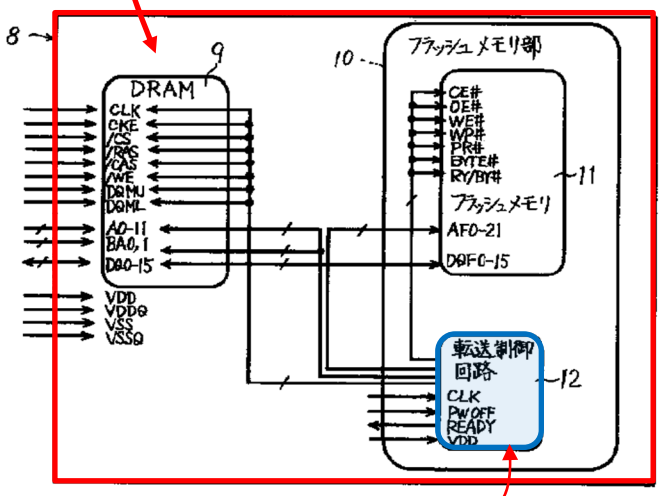
MTI-1006, [0043].

145. Tomio's FIGS. 2 and 7 (below) show the transfer control circuit 12/12′ (memory controller [chip]) (blue) in the package (outlined red) of the semiconductor memory 8. In accordance with the scope of the term "housing" advanced by Patent Owner in its complaint for infringement, Tomio's memory module 51 includes a package in which the transfer control circuit is provided and a substrate on which the package is mounted similar to the M.2 form factor memory devices that Patent Owner alleges satisfies this claim element. MTI-1021, 3; MTI-1024.

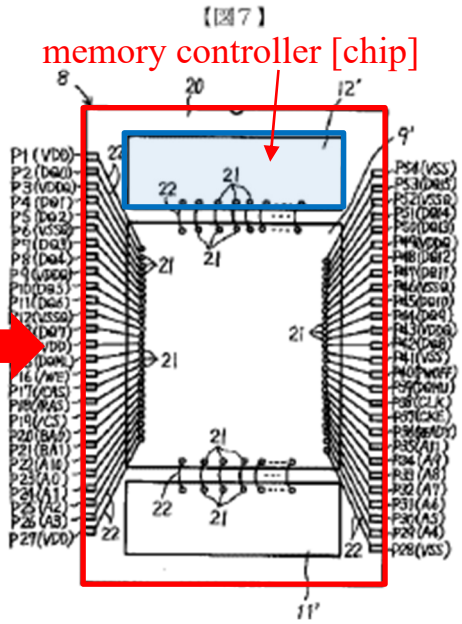
【図１１】



【図２】



【図７】



MTI-1006, FIGS. 11, 2, 7 (collated, annotated)

(d) Element 1[c]

146. Claim element 1[c] recites "a volatile memory coupled to said memory controller comprised in the housing." Tomio provides claim elements 1[c]. For example, Tomio describes a volatile memory, e.g., DRAM:

> **DRAMs** currently used in a wide variety of applications can be accessed at high speed, but **are volatile memories that lose stored information when the power is turned off**. Therefore, power to a DRAM has to be turned off after information in the DRAM has been written to a nonvolatile storage medium such as a hard disk or a flash memory card. Also, when the power is turned on again, some of the data in the nonvolatile storage medium such as a hard disk or flash memory card has to be written to the DRAM.

MTI-1006, [0002].

147. Tomio discloses a transfer control circuit that controls the transfer of data between the memories:

> In addition, the **DRAM 9 receives** clock signal CLK, **control signals** CKE, /CS, /RAS, /CAS, /WE, DQMU, and SQML, **and address signals** A0 to A11, BA0, and BA1 **from the transfer control circuit 12 during data fetching and data storage**, stores read data DQF0 to DQF15 in the flash memory 11 during data fetching, and supplies read data DQ0 to DQ15 to the flash memory 11 during data storage.
>
> The flash memory 11 receives control signals CE#, OE#, WE#, WP#, PR#, BYTE#, and RY/BY# and address signals AF0 to AF21 from the transfer control circuit 12, and stores read data DQ0 to DQ15 from the DRAM 9 during data storage, and supplies read data DQF0 to DQF15 to the DRAM 9 during data fetching.
>
> **The transfer control circuit 12 transfers data stored in the flash memory 11 to the DRAM 9** in response to the rising edge of the

power supply potential VDD, and erases all of the data in the flash memory 11 after completing the data transfer. In addition, the **transfer control circuit 12 transfers data in the DRAM 9 to the flash memory 11** in response to a PW OFF signal from the memory controller 5, and sends a READY to signal the memory controller 5 in response to completing the data transfer.

MTI-1006, [0020]-[0023].

After a predetermined amount of time has passed since the rising edge of the power supply potential VDD (time t0), the transfer control circuit 12 fetches data in ② (times t1 to t2). In other words, as shown in Fig. 5, read address signals AF0 to AF21 and read commands (with signals CE# and OE# set to the "L" level and signals WE# and PR# set to the "H" level) synchronized with the clock signal CLK are supplied from the transfer control circuit 12 to the flash memory 11. Meanwhile, **a write command (WR) and write address signals** A0 to A15 **are supplied from the transfer control circuit 12 to the DRAM 9**, and the data stored in the flash memory 11 is fetched and stored in the DRAM 9.

MTI-1006, [0024], [0032].

In addition, a PW OFF pulse signal is outputted from the memory controller 5 to the transfer control circuit 12 in response to the falling edge of signal φ1 at the "L" level, and **data storage** in ④ **is performed in response by the transfer control circuit 12** (times t3 to t4). In other words, as shown in Fig. 6, **a read command (RD) and read address signals** A0 to A15 synchronized with the clock

signal CLK **are supplied from the transfer control circuit 12 to the DRAM 9**. Meanwhile, write commands (with signals CE# and WE# set to the "L" level and signals OE# and PR# are set to the "H" level) and write address signals AF0 to AF21 are transferred from the transfer control circuit 12 to the flash memory 11. Data stored in the DRAM 9 is fetched and stored in the flash memory 11.

MTI-1006, [0028], [0032].

148. Tomio also discloses that the DRAM and the transfer control circuit are provided inside a package:

> In other words, as shown in Fig. 2, the semiconductor memory 8 includes **DRAM 9** and a flash memory unit 10, and the flash memory unit 10 includes flash memory 11 and a transfer control circuit 12.

MTI-1006, [0018].

> Fig. 7 is a diagram showing the configuration of the semiconductor memory 8. **A DRAM chip 9' is provided in the center of the package 20**, a flash memory chip 11' is provided on the lower side in the figure, **and a transfer control circuit chip 12' is provided on the upper side** in the figure. **Chips 9', 11' and 12' are connected via pads 21 and bonding wires 22**.
>
> A plurality of pins P1 to P54 are arranged at a predetermined pitch along both long sides of the package 20. Each of pins P1 to P54 is connected via a bonding wire 22 to a pad 21 of the DRAM chip 9'. Pins P1 to P54 are used to apply power supply potentials VDD, VDDQ and ground potentials VSS, VSSQ, input clock signal CLK,

control signals CKE, /CS, /RAS, /CAS, /WE, DQMU, and DQML, address signals A0 to A11, BA0, and BA1, input and output data DQ0 to DQ15, input the PW OFF signal, and output the READY signal.

MTI-1006, [0030]-[0031].

Modified examples of this embodiment will now be described. In the modified example shown in Fig. 8, a DRAM chip 9' is provided in the central portion of the package 30, and the chip 10' for the flash memory unit 10 is provided on the surface of the DRAM chip 9' in the central portion. These chips 9' and 10' are connected via a plurality of pads 21 and bonding wires 22. Note that the pins have been omitted to simplify the drawing. Because the **chips 9' and 10' are stacked inside the package 30** in this modified example, the area occupied by the chips 9', 10' is reduced, and the package 30 can be made smaller.

In the modified example shown in Fig. 9, a DRAM chip 9' is provided in the central portion of the package 40, and a chip 10' for the flash memory unit 10 is provided on the surface of the DRAM chip 9' in the central portion. These chips 9' and 10' are connected via a plurality of balls 41. The pads 21 of the DRAM chip 9' are connected to external pins P via bonding wires 22. These chips 9', 10' are sealed with a resin 42. In this modified example, **the chips 9', 10' are stacked inside the package 40, and the chips 9', 10' are connected via balls 41**. In this way, the area occupied by the chips 9', 10' is reduced, and the package 40 can be made smaller.

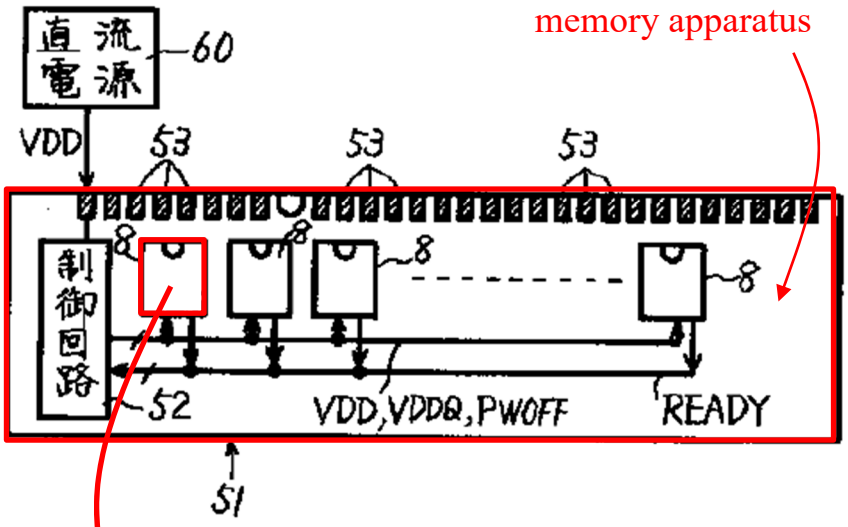
MTI-1006, [0034]-[0035], FIGS. 8-9.

> In the modified example shown in Fig. 11, the module 51 is composed of a semiconductor memory 8 in which **the DRAM**, flash memory, **and transfer control circuit are sealed in a single package**. However, the present invention is not limited to this modified example, and a chip in which the transfer control circuit is realized using a conventional DRAM, flash memory, ASIC, etc. may be mounted separately on the module board.

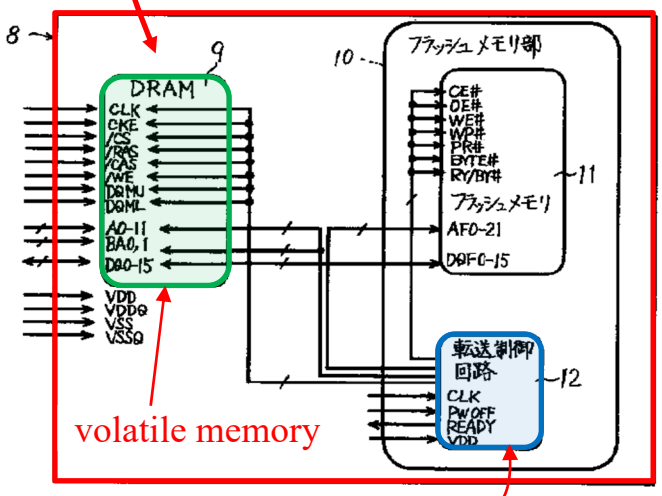
MTI-1006, [0043].

149. Tomio's FIGS. 2 and 7 (below) show the DRAM 9/9′ (volatile memory) (green) coupled to the transfer control circuit 12/12′ (memory controller [chip]) (blue) in the package (outlined red) of the semiconductor memory 8. In accordance with the scope of the term "housing" advanced by Patent Owner in its complaint for infringement, Tomio's memory module 51 includes a package in which the DRAMis provided and a substrate on which the package is mounted similar to the M.2 form factor memory devices that Patent Owner alleges satisfies this claim element. MTI-1021, 3; MTI-1024.

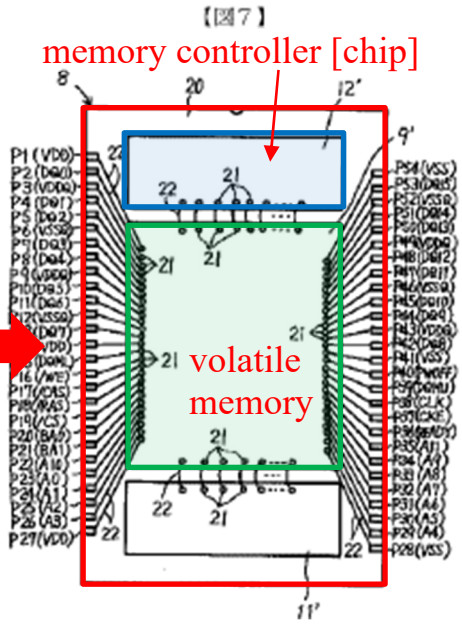
【図１１】



【図２】



【図７】



MTI-1006, FIGS. 11, 2, 7 (collated, annotated)

(e) Element 1[d]

150. Claim element 1[d] recites "a non-volatile memory coupled to said memory controller comprised in the housing." Tomio provides claim element 1[d]. For example, Tomio describes a non-volatile memory, e.g., flash memory:

> DRAMs currently used in a wide variety of applications can be accessed at high speed, but are volatile memories that lose stored information when the power is turned off. Therefore, power to a DRAM has to be turned off after information in the DRAM has been written to **a nonvolatile storage medium such as a hard disk or a flash memory card**. Also, when the power is turned on again, some of the data in the nonvolatile storage medium such as a hard disk or flash memory card has to be written to the DRAM.

MTI-1006, [0002].

151. Tomio discloses a transfer control circuit that controls the transfer of data between the memories:

> The **flash memory 11 receives control signals** CE#, OE#, WE#, WP#, PR#, BYTE#, and RY/BY# **and address signals** AF0 to AF21 **from the transfer control circuit 12**, and stores read data DQ0 to DQ15 from the DRAM 9 during data storage, and supplies read data DQF0 to DQF15 to the DRAM 9 during data fetching.
>
> **The transfer control circuit 12 transfers data stored in the flash memory 11 to the DRAM 9** in response to the rising edge of the power supply potential VDD, and erases all of the data in the flash memory 11 after completing the data transfer. In addition, the **transfer control circuit 12 transfers data in the DRAM 9 to the flash memory 11** in response to a PW OFF signal from the memory controller 5, and sends a READY to signal the memory controller 5 in response to completing the data transfer.

MTI-1006, [0020]-[0023].

After a predetermined amount of time has passed since the rising edge of the power supply potential VDD (time t0), **the transfer control circuit 12 fetches data** in ② (times t1 to t2). In other words, as shown in Fig. 5, **read address signals** AF0 to AF21 and **read commands** (with signals CE# and OE# set to the "L" level and signals WE# and PR# set to the "H" level) synchronized with the clock signal CLK **are supplied from the transfer control circuit 12 to the flash memory 11**. Meanwhile, a write command (WR) and write address signals A0 to A15 are supplied from the transfer control circuit 12 to the DRAM 9, and the data stored in the flash memory 11 is fetched and stored in the DRAM 9.

MTI-1006, [0024], [0032].

In addition, a PW OFF pulse signal is outputted from the memory controller 5 to the transfer control circuit 12 in response to the falling edge of signal φ1 at the "L" level, and data storage in ④ is performed in response by the transfer control circuit 12 (times t3 to t4). In other words, as shown in Fig. 6, a read command (RD) and read address signals A0 to A15 synchronized with the clock signal CLK are supplied from the transfer control circuit 12 to the DRAM 9. Meanwhile, **write commands** (with signals CE# and WE# set to the "L" level and signals OE# and PR# are set to the "H" level) **and write address signals** AF0 to AF21 **are transferred from the transfer control circuit 12 to the flash memory 11**. Data stored in the DRAM 9 is fetched and stored in the flash memory 11.

MTI-1006, [0028], [0032].

152. Tomio also discloses that the flash memory and the transfer control circuit are provided inside a package:

> In other words, as shown in Fig. 2, the semiconductor memory 8 includes DRAM 9 and a flash memory unit 10, and the flash memory unit 10 includes **flash memory 11 and a transfer control circuit 12**.

MTI-1006, [0018].

> Fig. 7 is a diagram showing the configuration of the semiconductor memory 8. A DRAM chip 9' is provided in the center of **the package 20, a flash memory chip 11' is provided on the lower side in the figure, and a transfer control circuit chip 12' is provided on the upper side** in the figure. **Chips 9', 11' and 12' are connected via pads 21 and bonding wires 22**.
>
> A plurality of pins P1 to P54 are arranged at a predetermined pitch along both long sides of the package 20. Each of pins P1 to P54 is connected via a bonding wire 22 to a pad 21 of the DRAM chip 9'. Pins P1 to P54 are used to apply power supply potentials VDD, VDDQ and ground potentials VSS, VSSQ, input clock signal CLK, control signals CKE, /CS, /RAS, /CAS, /WE, DQMU, and DQML, address signals A0 to A11, BA0, and BA1, input and output data DQ0 to DQ15, input the PW OFF signal, and output the READY signal.

MTI-1006, [0030]-[0031].

> Modified examples of this embodiment will now be described. In the modified example shown in Fig. 8, a DRAM chip 9' is provided

in the central portion of the package 30, and the chip 10' for the flash memory unit 10 is provided on the surface of the DRAM chip 9' in the central portion. These chips 9' and 10' are connected via a plurality of pads 21 and bonding wires 22. Note that the pins have been omitted to simplify the drawing. Because the **chips 9' and 10' are stacked inside the package 30** in this modified example, the area occupied by the chips 9', 10' is reduced, and the package 30 can be made smaller.

In the modified example shown in Fig. 9, a DRAM chip 9' is provided in the central portion of the package 40, and a chip 10' for the flash memory unit 10 is provided on the surface of the DRAM chip 9' in the central portion. These chips 9' and 10' are connected via a plurality of balls 41. The pads 21 of the DRAM chip 9' are connected to external pins P via bonding wires 22. These chips 9', 10' are sealed with a resin 42. In this modified example, **the chips 9', 10' are stacked inside the package 40, and the chips 9', 10' are connected via balls 41**. In this way, the area occupied by the chips 9', 10' is reduced, and the package 40 can be made smaller.

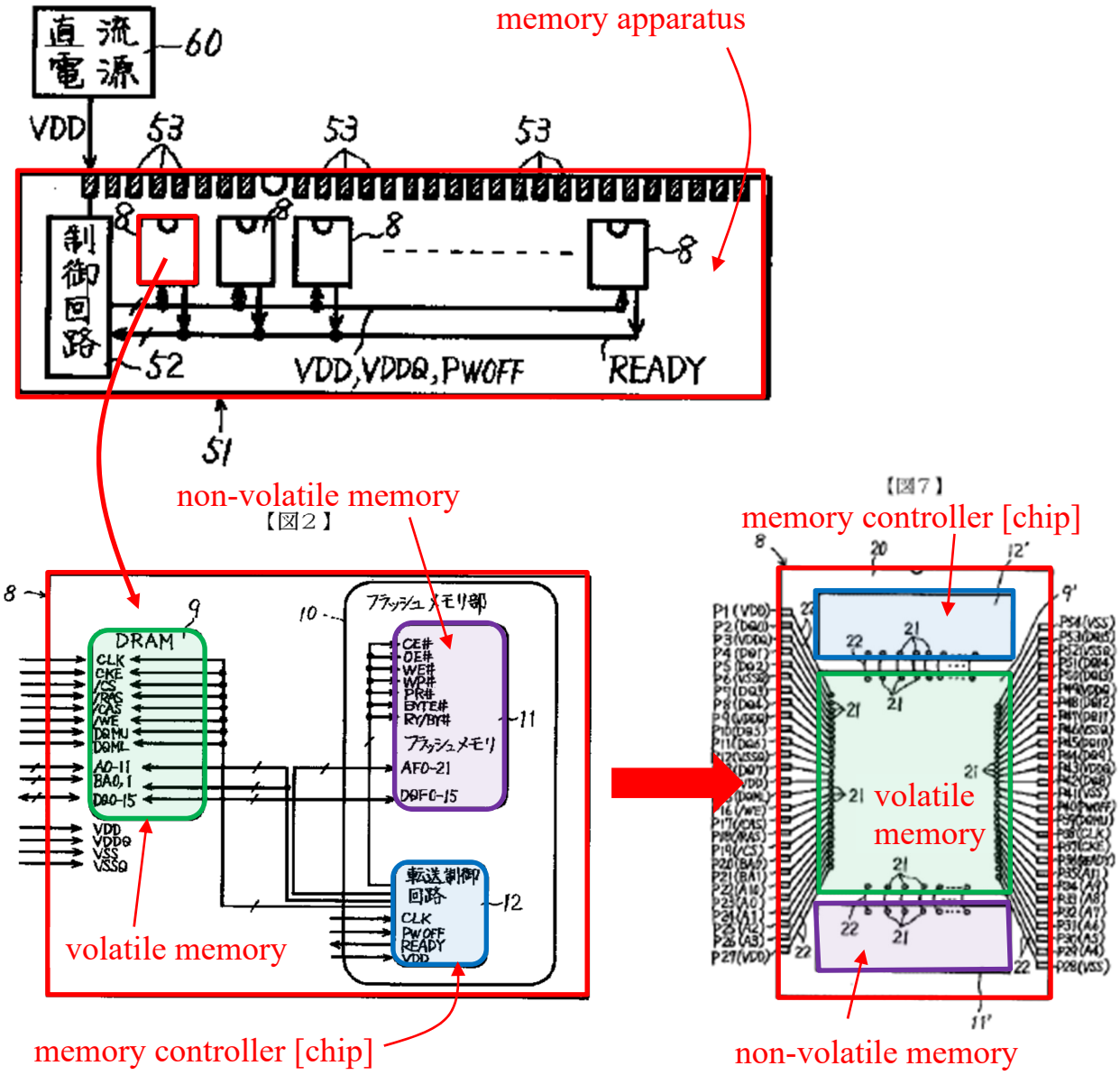
MTI-1006, [0034]-[0035], FIGS. 8-9.

In the modified example shown in Fig. 11, the module 51 is composed of a semiconductor memory 8 in which the DRAM, **flash memory, and transfer control circuit are sealed in a single package**. However, the present invention is not limited to this modified example, and a chip in which the transfer control circuit is realized using a conventional DRAM, flash memory, ASIC, etc. may be mounted separately on the module board.

MTI-1006, [0043].

153. Tomio's FIGS. 2 and 7 (below) show the DRAM 9/9′ (volatile memory) (green) and the flash memory 11/11′ (non-volatile memory) (purple) coupled to the transfer control circuit 12/12′ (memory controller [chip]) (blue) in the package (outlined red) of the semiconductor memory 8. In accordance with the scope of the term "housing" advanced by Patent Owner in its complaint for infringement, Tomio's memory module 51 includes a package in which the DRAM, the flash memory, and the transfer control circuit are provided and a substrate on which the package is mounted similar to the M.2 form factor memory devices that Patent Owner alleges satisfies this claim element. MTI-1021, 3; MTI-1024.

【図１１】



MTI-1006, FIGS. 11, 2, 7 (collated, annotated)

(f) Element 1[e]

154. Claim element 1[e] recites "a connector positioned on the housing, wherein said connector couples said portable memory apparatus to a computer

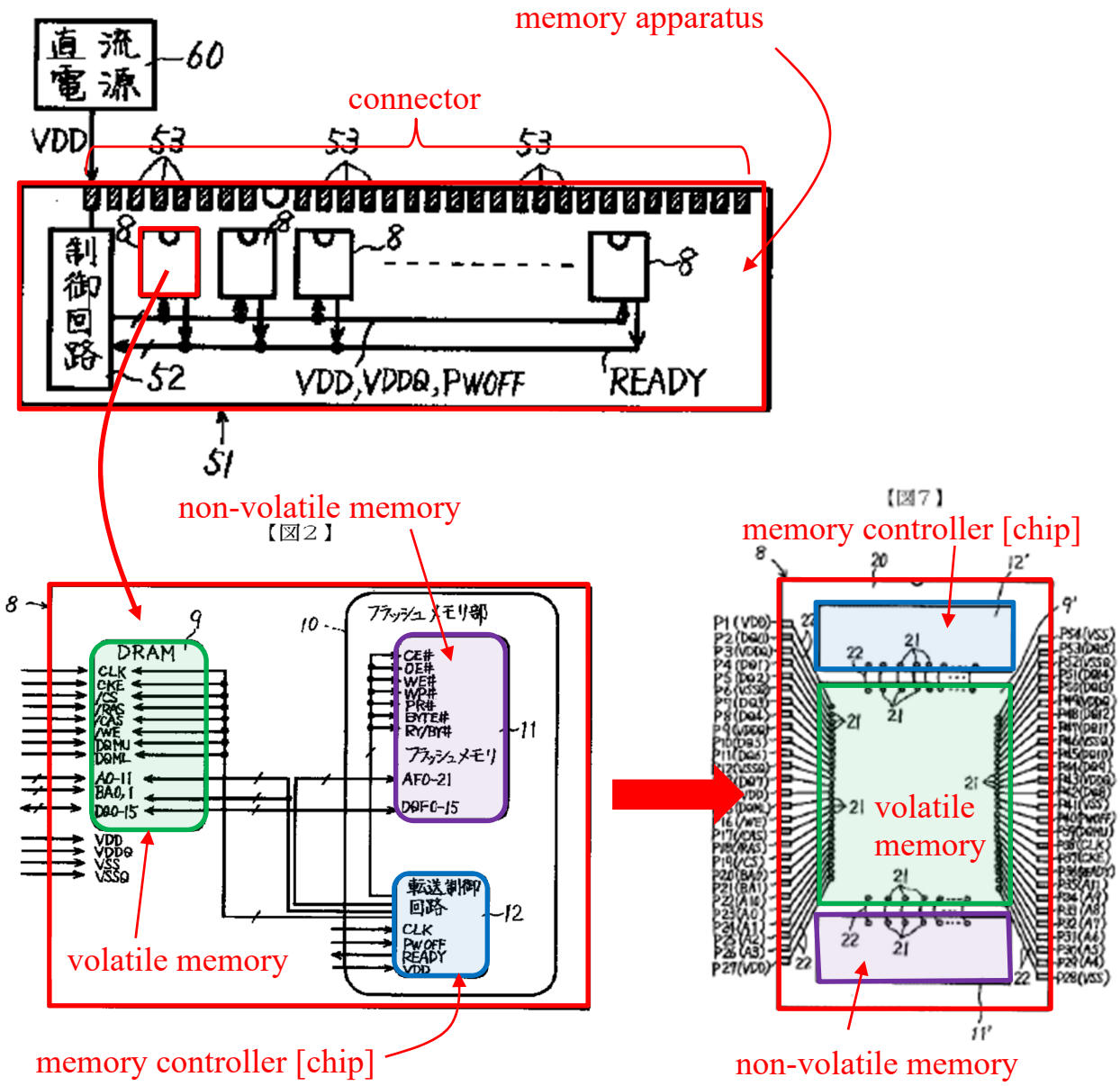
system when said connector is plugged into said computer system." Tomio provides claim element 1[e]. For example, Tomio discloses that:

> Also, as shown in Fig. 10, **a module 50 that operates as a single memory unit may be constructed by assembling a plurality of semiconductor memories 8**. For example, a 256 MB fast access nonvolatile memory can be realized by mounting eight semiconductor memories 8 in the present invention on the substrate of **a Mitsubishi Electric 256 MB 168 pin unbuffered dual inline module**. **This 256 MB module can also be used as the main memory in a personal computer** by pre-storing data that is usually stored in ROM in the flash memory 11 of the semiconductor memory 8. As a result, the data transfer bus between the ROM and the main memory on the motherboard of a conventional personal computer, the bus control circuit, and the ROM become unnecessary. In addition, a module formed using a semiconductor memory 8 of the present invention may be used instead of a conventional floppy disk or CDROM.
>
> In the modified example shown in Fig. 11, the module 51 is composed of a plurality of semiconductor memories 8 and a control circuit 52. The control circuit 52 receives direct current power supply potential VDD from a direct current power supply 60 outside of the module 51 via **an input terminal 53**, and supplies direct current power supply potentials VDD and VDDQ to each semiconductor memory 8 in the module 51. Also, the control circuit 52 supplies a PW OFF signal to each semiconductor memory 8 in response to the supply of the direct current power supply potential

> VDD from the direct current power supply 60 being stopped, and the supply of the direct current power supply potentials VDD and VDDQ to each semiconductor memory 8 is stopped when a READY signal has been outputted from all of the semiconductor memories 8.

MTI-1006, [0037]-[0038]. In accordance with the scope of the term "housing" advanced by Patent Owner in its complaint for infringement, Tomio's FIG. 11 (below) shows terminals 53 (connector) positioned on the substrate (outlined red) of the memory module 51 similar to the M.2 form factor memory devices that Patent Owner alleges satisfies this claim element. MTI-1021, 3; MTI-1024. Based on my knowledge and experience in the field and my review of Tomio, a POSITA would have found it obvious that the terminals 53 couple the memory module 51 to a personal computer (computer system) when the terminals 53 are plugged into the personal computer to enable the memory module 51 to communicate with the personal computer.

【図１１】



MTI-1006, FIGS. 11, 2, 7 (collated, annotated)

(g) Element 1[f]

155. Claim element 1[f] recites "wherein, when said connector couples said portable memory apparatus to said computer system, said memory controller chip copies data from said non-volatile memory to said volatile memory, and said

computer system accesses said data in said volatile memory through said connector."

Tomio provides claim element 1[f]. For example, Tomio discloses that:

> In the modified example shown in Fig. 11, the module 51 is composed of a plurality of semiconductor memories 8 and a control circuit 52. **The control circuit 52 receives direct current power supply potential VDD from a direct current power supply 60 outside of the module 51 via an input terminal 53**, and supplies direct current power supply potentials VDD and VDDQ to each semiconductor memory 8 in the module 51. Also, the control circuit 52 supplies a PW OFF signal to each semiconductor memory 8 in response to the supply of the direct current power supply potential VDD from the direct current power supply 60 being stopped, and the supply of the direct current power supply potentials VDD and VDDQ to each semiconductor memory 8 is stopped when a READY signal has been outputted from all of the semiconductor memories 8.

MTI-1006, [0038].

> **The transfer control circuit 12 transfers data stored in the flash memory 11 to the DRAM 9 in response to the rising edge of the power supply potential VDD, and erases all of the data in the flash memory 11 after completing the data transfer**. In addition, the transfer control circuit 12 transfers data in the DRAM 9 to the flash memory 11 in response to a PW OFF signal from the memory controller 5, and sends a READY to signal the memory controller 5 in response to completing the data transfer.

MTI-1006, [0022]-[0023].

> **After a predetermined amount of time has passed since the rising edge of the power supply potential VDD** (time t0), **the transfer control circuit 12 fetches data** in ② (times t1 to t2). In other words, as shown in Fig. 5, **read address signals** AF0 to AF21 and **read commands** (with signals CE# and OE# set to the "L" level and signals WE# and PR# set to the "H" level) synchronized with the clock signal CLK **are supplied from the transfer control circuit 12 to the flash memory 11**. Meanwhile, **a write command (WR) and write address signals** A0 to A15 **are supplied from the transfer control circuit 12 to the DRAM 9**, **and the data stored in the flash memory 11 is fetched and stored in the DRAM 9**.
>
> **After the data fetching** in ② **has been completed, the normal operations** in ③ **are performed** (times t2 to t3). **During normal operations**, the semiconductor memory 8 operates as a DRAM 9 from the perspective of the memory controller 5. The **DRAM** 9 is in an idle state or access standby when not accessed by the memory controller 5 (⑥), and **reads and writes data when accessed** (⑦).
>
> Meanwhile, the data in the flash memory 11 is erased during this period (④). The data is erased by the transfer control circuit 12. The data in the flash memory 11 is erased in this manner because all data in the memory cells has to be erased in order to write data to a flash memory 11. The flash memory 11 in which the data in all memory cells has been erased enters an idle state or access standby (⑤).

MTI-1006, [0024]-[0026], [0019].

> In the present embodiment, a DRAM 9, flash memory 11, and

> transfer control circuit 12 are provided in a semiconductor memory 8, **data in the flash memory 11 is transferred to the DRAM 9 in response to the external power supply switch 15 of the personal computer being turned on, the DRAM 9 is used as the semiconductor memory 8** and data in flash memory 11 is erased during normal operations, and data in the DRAM 9 is stored in the flash memory 11 in response to the external power supply switch 15 being turned off. In this way, a semiconductor memory 8 can be realized that enables high-speed access like a DRAM but has data nonvolatility like a flash memory.

MTI-1006, [0032].

156. In other words, when the terminals 53 of Tomio's memory module 51 couples the module 51 to a personal computer, "control circuit 52 receives direct current power supply potential VDD from a direct current power supply 60 outside of the module 51 via an input terminal 53, and supplies direct current power supply potentials VDD and VDDQ to each semiconductor memory 8 in the module 51." MTI-1006, [0038]. "The transfer control circuit 12 transfers data stored in the flash memory 11 to the DRAM 9 in response to the rising edge of the power supply potential VDD, and erases all of the data in the flash memory 11 after completing the data transfer." MTI-1006, [0022]-[0024], [0032]. "The data in the flash memory 11 is erased in this manner because all data in the memory cells has to be erased in order to write data to a flash memory 11." MTI-1006, [0026].

157. After the data has been copied from the flash memory 11 to the DRAM 9, normal operations are performed where "the semiconductor memory 8 operates as a DRAM 9" from the perspective of the personal computer. MTI-1006, [0025]. The DRAM 9 is in an idle state or access standby when not accessed by the personal computer, and reads and writes data when accessed by the personal computer. *Id.* The DRAM 9 stores data supplied from a personal computer during a write operation and supplies read data to the personal computer during a read operation. MTI-1006, [0019], [0032]. Based on my review of Tomio, Tomio teaches that when the terminals 53 (connector) couples the module 51 to the personal computer (computer system), the transfer control circuit (memory controller chip) copies data from the flash memory (non-volatile memory) to the DRAM (volatile memory), and the personal computer accesses the data in the DRAM through the terminals 53.

2. Claims 2, 4, and 5

158. Claim 2 recites:

> The portable memory apparatus of claim 1, further comprising an internal power source coupled to said portable memory apparatus.

Claim 4 recites:

> The portable memory apparatus of claim 2, wherein said internal power source is rechargeable through said connector.

Claim 5 recites:

> The portable memory apparatus of claim 4, wherein said internal

power source comprises a battery or a capacitor.

For similar reasons discussed in the analysis of claims 2, 4, and 5 with respect to the combination of Tsunoda, alone or with Sukegawa, and Tomio, Tomio's memory module 51 includes a rechargeable battery (internal power source) that is rechargeable through the terminal 53 (of the connector) and that continues to supply power long enough to copy data from volatile memory to nonvolatile memory in the event that the external power to the memory apparatus is abruptly stopped.

3. Claim 3

159. Claim 3 recites:

> The portable memory apparatus of claim 2, wherein said internal power source powers said portable memory apparatus when said portable memory apparatus is unplugged from said computer system, said portable memory apparatus copies data from said volatile memory to said non-volatile memory when said portable memory apparatus is unplugged from said computer system.

For similar reasons discussed in the analysis of claim 3 with respect to the combination of Tsunoda, alone or with Sukegawa, and Tomio, Tomio's rechargeable battery (internal power source) powers the module 51 and the module 51 copies data from the DRAM (volatile memory) to the flash memory (non-volatile memory) when the module 51 is unplugged from the personal computer (computer system).

4. Claim 6

160. Claim 6 recites:

> The portable memory apparatus of claim 1, wherein said memory controller chip transfers said non-volatile memory with data written to said volatile memory from said computer system while said portable memory apparatus is coupled to said computer system.

The language "said memory controller chip transfers said non-volatile memory with data written to said volatile memory from said computer system" is subject to the following possible constructions: (1) the memory controller chip "transfers *to* said non-volatile memory data written to said volatile memory from said computer system" (*i.e.*, the italicized "to" should be inserted and "with" should be deleted), (2) the memory controller chip "transfers *from* said non-volatile memory data written to said volatile memory from said computer system," or (3) the memory controller chip "transfers data *from* the non-volatile memory *to* the volatile memory so that it can be accessed by the host computer." Tomio provides claim 6 under any of these possible constructions.

161. If "said memory controller chip transfers said non-volatile memory with data written to said volatile memory from said computer system" were construed to mean the memory controller chip "transfers *to* said non-volatile memory data written to said volatile memory from said computer system," Tomio

renders this obvious for the reasons discussed in the analysis of claim 3 with respect to Tomio.

162. If "said memory controller chip transfers said non-volatile memory with data written to said volatile memory from said computer system" were construed to mean "transfers *from* said non-volatile memory data written to said volatile memory from said computer system" or "transfers data *from* the non-volatile memory *to* the volatile memory so that it can be accessed by the host computer," Tomio renders this obvious for the reasons discussed in the analysis of claim element 1[f] with respect to Tomio.

5. Claim 9

163. Claim 9 recites:

> The portable memory apparatus of claim 1, wherein said volatile memory is selected from a group consisting of FPM DRAM, EDO DRAM, SDRAM, RDRAM, and SRAM.

For the reasons discussed in the analysis of claim element 1[c] with respect to Tomio, Tomio provides claim 9.

6. Claim 12

164. Claim 12 recites:

> The portable memory apparatus of claim 1, wherein said portable memory apparatus does not have any moving parts.

Tomio provides claim 12. As discussed in the analysis of claim element 1[p] with respect to Tomio, Tomio's memory module 51 includes semiconductor memories 8 and a control circuit 52 mounted on a substrate such as "a Mitsubishi Electric 256 MB 168 pin unbuffered dual inline module," as shown in FIG. 11 (above). MTI-1006, [0037]-[0038]. Tomio further discloses that:

> In the modified example shown in Fig. 11, **the module 51 is composed of a semiconductor memory 8 in which the DRAM, flash memory, and transfer control circuit are sealed in a single package**. However, the present invention is not limited to this modified example, and a chip in which the transfer control circuit is realized using a conventional DRAM, flash memory, ASIC, etc. may be mounted separately on the module board.

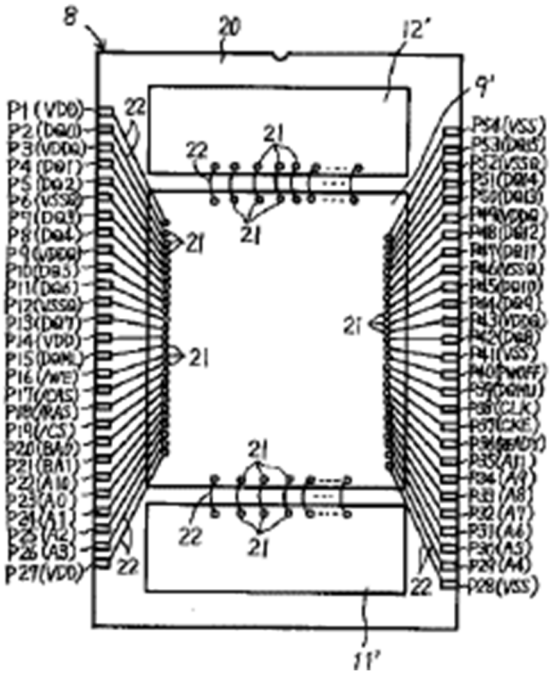
MTI-1006, [0043].

> Fig. 7 is a diagram showing the configuration of the semiconductor memory 8. A DRAM chip 9' is provided in the center of the package 20, a flash memory chip 11' is provided on the lower side in the figure, and a transfer control circuit chip 12' is provided on the upper side in the figure. Chips 9', 11' and 12' are connected via pads 21 and bonding wires 22.
>
> A plurality of pins P1 to P54 are arranged at a predetermined pitch along both long sides of the package 20. Each of pins P1 to P54 is connected via a bonding wire 22 to a pad 21 of the DRAM chip 9'. Pins P1 to P54 are used to apply power supply potentials VDD, VDDQ and ground potentials VSS, VSSQ, input clock signal CLK,

control signals CKE, /CS, /RAS, /CAS, /WE, DQMU, and DQML, address signals A0 to A11, BA0, and BA1, input and output data DQ0 to DQ15, input the PW OFF signal, and output the READY signal.

MTI-1006, [0030]-[0031]. FIG. 7 shows a possible configuration of the semiconductor memory 8 with input/output pins P1-P54, a DRAM chip 9', a flash memory chip 11', and a transfer control circuit chip 12' connected via pads 21 and bonding wires 22 provided in a package 20.

【図7】



MTI-1006, FIG. 7

Tomio also describes other configurations:

Modified examples of this embodiment will now be described. In the modified example shown in Fig. 8, a DRAM chip 9' is provided in the central portion of the package 30, and the chip 10' for the flash

memory unit 10 is provided on the surface of the DRAM chip 9' in the central portion. These chips 9' and 10' are connected via a plurality of pads 21 and bonding wires 22. Note that the pins have been omitted to simplify the drawing. Because the **chips 9' and 10' are stacked inside the package 30** in this modified example, the area occupied by the chips 9', 10' is reduced, and the package 30 can be made smaller.

In the modified example shown in Fig. 9, a DRAM chip 9' is provided in the central portion of the package 40, and a chip 10' for the flash memory unit 10 is provided on the surface of the DRAM chip 9' in the central portion. These chips 9' and 10' are connected via a plurality of balls 41. The pads 21 of the DRAM chip 9' are connected to external pins P via bonding wires 22. These chips 9', 10' are sealed with a resin 42. In this modified example, **the chips 9', 10' are stacked inside the package 40**, and the chips 9', 10' are connected via balls 41. In this way, the area occupied by the chips 9', 10' is reduced, and the package 40 can be made smaller.

MTI-1006, [0034]-[0035], FIGS. 8-9. Based on my knowledge and experience in the field and my review of Tomio, a POSITA would have understood or at least found it obvious that the memory module 51, which includes packaged semiconductor memories 8 and a control circuit 52 mounted on a substrate, does not have any moving parts.

7. Claim 15

(a) Element 15[p]

165. The preamble of claim 15 recites "[a] method." Tomio provides a method as recited in the preamble of claim 15 as set forth below in the analysis of claim elements 15[a]-15[e] with respect to Tomio under the scope of the term "portable" advanced by Patent Owner in its complaint for infringement.

(b) Element 15[a]

166. Claim element 15[a] recites "coupling a portable memory apparatus to a computer system." For the reasons discussed in the analysis of claim elements 1[p] and 1[e] with respect to Tomio, Tomio provides claim element 15[a] under the scope of the term "portable" advanced by Patent Owner in its complaint for infringement.

(c) Element 15[b]

167. Claim element 15[b] recites "wherein said portable memory apparatus comprises a memory controller chip, a non-volatile memory, and a volatile memory." For the reasons discussed in the analysis of claim elements 1[b], 1[c], 1[d] with respect to Tomio, Tomio provides claim element 15[b] under the scope of the term "portable" advanced by Patent Owner in its complaint for infringement.

(d) Element 15[c]

168. Claim element 15[c] recites "copying data from said non-volatile memory to said volatile memory using said memory controller chip." For the

reasons discussed in the analysis of claim element 1[f] with respect to Tomio, Tomio provides claim element 15[c].

(e) Element 15[d]

169. Claim element 15[d] recites "accessing said data in said volatile memory using said computer system through a connector coupled to said portable memory apparatus and said memory controller chip." For the reasons discussed in the analysis of claim element 1[f] with respect to Tomio, Tomio provides claim element 15[d].

(f) Element 15[e]

170. Claim element 15[e] recites "updating said non-volatile memory with data from said volatile memory." For the reasons discussed in the analysis of claim 6 with respect to Tomio, Tomio provides claim element 15[e].

8. Claim 16

171. Claim 16 recites:

> The method of claim 15, further comprising: powering said portable memory apparatus with an internal power source coupled to said portable memory apparatus, when said portable memory apparatus is unplugged from said computer system, to transfer said non-volatile memory with data from said volatile memory.

For the reasons discussed in the analysis of claims 2 and 3 with respect to Tomio, Tomio provides claim 16.

9. Claim 17

172. Claim 17 recites:

> The method of claim 15, further comprising: recharging an internal power source coupled to said portable memory apparatus.

For the reasons discussed in the analysis of claim 4 with respect to Tomio, Tomio provides claim 17.

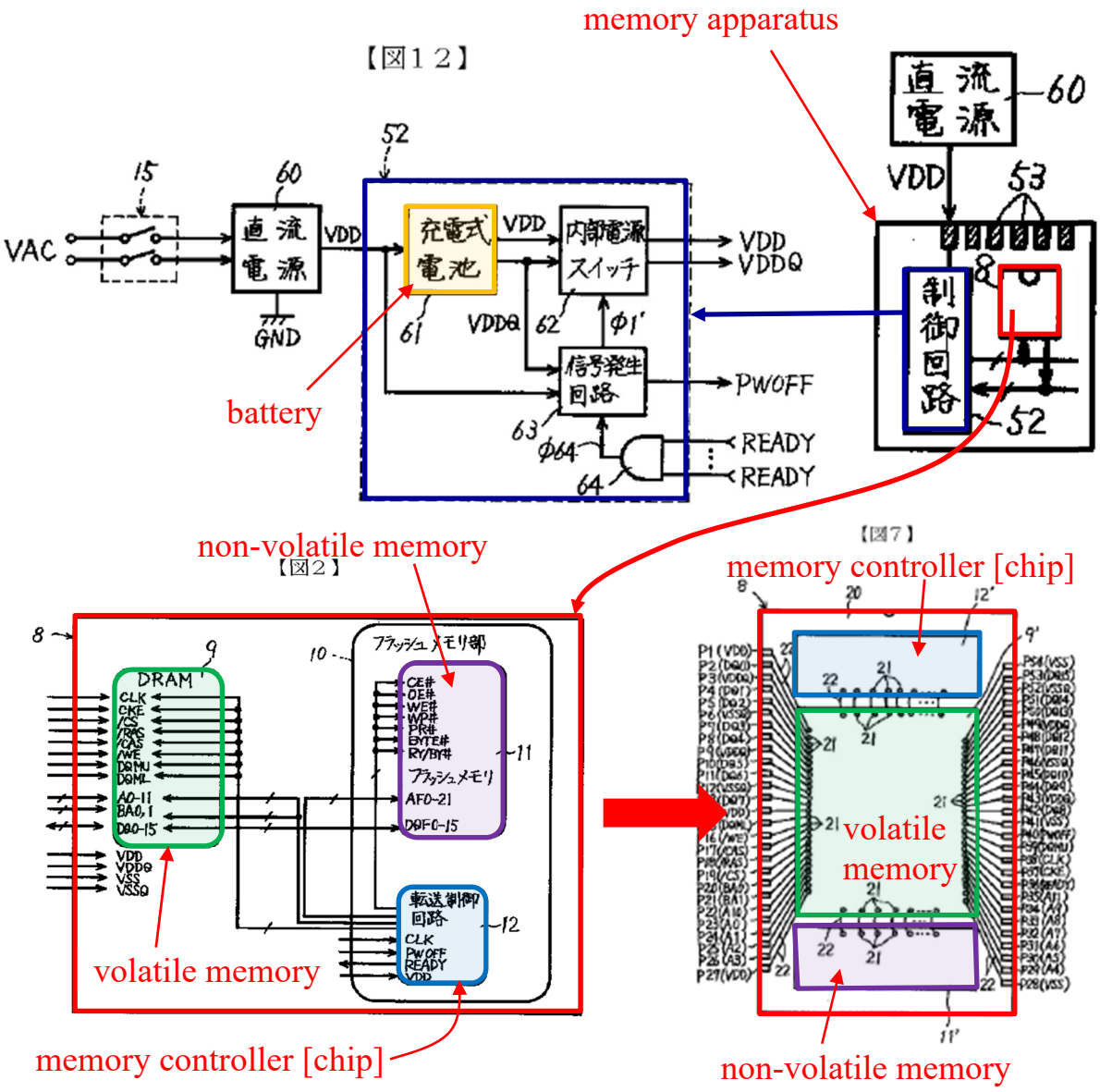
E. Analysis of Tomio in view of Sukegawa with respect to Claims 1-7, 9-12, and 14-18

173. For the reasons articulated in detail below, and based on my review of the '527 patent and the Tomio and Sukegawa references, I am confident that a POSITA would have readily understood that Tomio in view of Sukegawa renders obvious all elements of claims 1-7, 9-12, and 14-18.

1. Combination of Tomio and Sukegawa

174. Although the above description of Tomio relates to a memory module with multiple semiconductor memories and a control circuit mounted on a substrate (MTI-1006, [0037]-[0038], FIG. 11), a POSITA would have found it obvious, from Tomio's explicit teachings, to implement a memory apparatus with one semiconductor memory and a control circuit mounted on a substrate, as shown below. MTI-1006, [0018]-[0024], [0025]-[0026], [0028], [0030]-[0032], [0034]-[0035], [0043]-[0044], [0048], FIGS. 2, 7-9, claims 1-6 (claiming the elements of

one semiconductor memory and a control circuit), [0045]-[0050] (describing the same).



MTI-1006, FIGS. 2, 7, 11, 12
(modified to show one semiconductor memory 8 and collated)

175. A POSITA implementing such a memory apparatus would have turned to examples of similar memory apparatus to identify suitable housings for the electrical components and interfaces for connecting to a computer system.

Sukegawa provides a suitable housing and interface for such a memory apparatus. In that regard, Sukegawa explains that:

> The Universal Serial Bus, conventionally referred to as USB, is a bus standard for inexpensively connecting external peripheral devices to a personal computer. USB provides an expandable, hot-pluggable serial interface that ensures a standard, low-cost connection for peripheral devices such as keyboards, mice, joysticks, printers, scanners, storage devices, modems, and the like. The popularity of the USB standard is evident as most computer manufacturers now include one or more USB interfaces for external USB peripherals as part of their systems. Commentators in the computer industry have noted that the USB standard is becoming the market's dominant I/O connectivity standard.

MTI-1005, 1:13-24. Those in the field have recognized that a USB interface has advantages over other interfaces:

> In addition, a silicon disk card with a USB plug not only has the effect of enabling plug and play without any electric power supply, but also has the advantages of high safety, high data transmission speed (12 mb/sec.), hot swapping, convenient operation, no need of any computer assembling experience or any computer changing device, and of being able to support systems such as Windows 98 and Mac OS 8.6 etc. It is no wonder that consumers and manufacturers get more and more fond of products like Removable Hard Disks and ThumbDrives. The products all have standard interfaces (USB) and large storage capacity, and will in the future

> have even larger storage capacity; they can be quickly connected to communicate with computers having USB plugs, and can easily have data directly transmitted to and from other types of consumer electronic and communication devices.

MTI-1017, 1:53-67; MTI-1005, 1:13-44 ("advantage of this quick connectivity standard"); MTI-1013, [0010]. A POSITA would have been motivated to apply the teachings of Sukegawa to Tomio's suggested memory apparatus to provide a memory apparatus that connects to a host via a USB connector to achieve the above-stated benefits of a USB flash memory device. *Id*.

176. Sukegawa discloses that a flash memory device, such as Tomio's suggested memory apparatus, can be implemented as a "USB flash drive apparatus" that "interfaces with a host system through a USB connector." MTI-1005, 1:38-40, 4:35-38. Sukegawa discloses that the USB standard is "an expandable, hot-pluggable serial interface that ensures a standard, low-cost connection for peripheral devices" and "provides additional bandwidth for multimedia and storage applications and also offers Plug-and-Play capability." MTI-1005, 1:13-30; MTI-1017, 1:53-67 ("hot swapping, convenient operation, no need of any computer assembling experience or any computer changing device").

177. Sukegawa's teachings enable implementation of a memory apparatus, such as that suggested in Tomio, as a USB flash drive apparatus. MTI-1005, 4:48-50, 8:6-9:16, FIGS. 5A-5H. A POSITA would have been motivated to apply the

teachings of Sukegawa to Tomio's suggested memory apparatus to beneficially provide a USB flash drive apparatus having "an expandable, hot-pluggable serial interface that ensures a standard, low-cost connection for peripheral devices" and "provides additional bandwidth for multimedia and storage applications and also offers Plug-and-Play capability." MTI-1005, 1:13-30; MTI-1017, 1:53-67 ("hot swapping, convenient operation, no need of any computer assembling experience or any computer changing device").

178. Sukegawa also provides that the USB flash drive apparatus includes lights that indicate when the flash memory is being accessed:

> Additionally, end cap 110 may have an opening to expose one or more **lights that indicate connection to the host system, access to the apparatus memory or both**.

MTI-1005, 4:67-5:2.

> In a further alternative embodiment, end cap 110 may be made of a visually opaque material capable of reflecting **light** in many directions **when the apparatus is being accessed** or simply when the apparatus has been properly inserted within the host system.

MTI-1005, 5:16-20.

> Additionally, one or more **lights** (not shown) may also be connected to the controller 210 within device 200 to **provide an indication that the device 200 is properly connected to USB host 205 and if NAND flash memory 215 is being accessed**. In one embodiment, the light may be an LED incorporated into the end cap

> 110 and wired to the controller 210. In other embodiments, the light may be implemented as one or more display devices (e.g., one or more discrete LEDs, an integrated group of LEDs, a small LCD display on the end of the USB connector shield case, etc.) that provides the desired indications to the user.

MTI-1005, 6:21-31. These additional teachings of Sukegawa would further motivate a POSITA to implement a flash memory device, such as Tomio's suggested memory apparatus, as a USB flash drive apparatus with indicator lights. *Id*. A POSITA would have found it obvious that removing a USB flash drive apparatus during data transfers is not desirable and would have been motivated to add an indicator light to advantageously provide the user with a visual indication that the USB flash drive apparatus is transferring data to at least discourage removal of the memory card from a host system during a memory transfer. *Id.*; MTI-1005, 4:67-5:2, 5:16-20, 6:21-31; MTI-1013, [0016], [0072]; MTI-1018, [0005], [0030]; MTI-1019, 3:1-3.

179. Accordingly, a POSITA would have found it obvious and would have been motivated to implement Tomio's suggested memory apparatus with a USB connector for connecting the memory apparatus and the host, and with indicator lights to provide a visual indication of the status of the memory apparatus. MTI-1005, 1:13-30, 4:67-5:2, 5:16-20, 6:21-31; MTI-1013, [0006]-[0010], [0016], [0072]; MTI-1017, 1:53-67; MTI-1018, [0005], [0030]; MTI-1019, 3:1-3. A

POSITA would have viewed the implementation of Tomio's memory apparatus in a manner that applied Sukegawa's suggested connector configuration as merely the predictable result of combining known prior art elements according to known methods. *Id.* A POSITA would have had a reasonable expectation of success in doing so as such an implementation was well-known as demonstrated by Sukegawa and commonly utilized in similar memory apparatus. *Id.* A POSITA would have recognized that the above described modifications would have yielded predictable results, would have been within the ordinary level of skill of a POSITA, and would not have required undue experimentation. *Id.*

2. Claim 1

(a) Element 1[p]

180. The preamble of claim 1 recites "[a] portable memory apparatus." The combination of Tomio and Sukegawa provides the preamble of claim 1. For example, Sukegawa discloses that:

> In general, **the USB flash drive is a small memory storage apparatus** that interfaces with a host system through a USB connector. The apparatus uses low power non-volatile flash memory as its storage media instead of conventional rotating hard disk media.

MTI-1005, 1:38-42.

> FIG. 1 is an exterior illustration of an exemplary USB memory storage apparatus according to an embodiment of the present

invention. Referring now to FIG. 1, exemplary USB memory apparatus 100 is an integrated flash drive apparatus shown with a USB connector shield case 120.

MTI-1005, 4:44-48.

In this embodiment, the USB connector is a Series A Plug connector for use in connecting to host systems on the upstream. As indicated in the USB 2.0 Specification, the Series A Plug includes a Plug Housing (more generally referred to as a USB connector shield case 120) that extends from an overmold boot (not shown) on an end of the connector opposite the contact terminals 400A-D. The overmold boot is typically an injection molded thermoplastic insulator material with a minimum UL94-VO rating. **The USB connector shield case 120 for the Series A Plug measure 12 millimeters (mm) wide±0.10 mm, 4.5 mm tall±0.10 mm, and a minimum of 11.75 mm deep**.

MTI-1005, 7:26-37.

Those skilled in the art will appreciate that it is still advantageous to incorporate just the controller, the NAND flash memory, or the USB interface circuitry within case 120' as such an alternative embodiment also allows for a reduced size of a USB flash drive apparatus. In other words, by incorporating the electrical circuit components into a reduced size semiconductor device that is capable of being mounted within the USB connector itself or at least partially within the USB connector, embodiments of the present invention allow a USB flash drive apparatus to be implemented in a dramatically reduced physical space. This allows for **a very small,**

> **inexpensive, portable and removable storage media** that avoids the break off or damage problem associated with prior art USB flash drives having a majority of their structure being outside the USB connector.

MTI-1005, 9:17-31.

181. Based on my review of Tomio and Sukegawa, the combination of Tomio and Sukegawa provides a "USB flash drive" which is "a very small, inexpensive, portable and removable storage media" measuring "12 millimeters (mm) wide±0.10 mm, 4.5 mm tall±0.10 mm, and a minimum of 11.75 mm deep." MTI-1005, 1:38-40, 7:35-37, 9:17-31. Accordingly, a POSITA would have understood or at least found it obvious that Tomio-Sukegawa's flash drive is a portable memory apparatus. Other publications relating to USB flash drives confirm that USB flash drives are portable. MTI-1013, [0004] ("[f]lash memory has become an important means of storing data which offers **portability**."); MTI-1012, [0004]-[0005] ("a **portable** data storage device comprising a coupling device for coupling to a computer serial bus").

portable memory apparatus

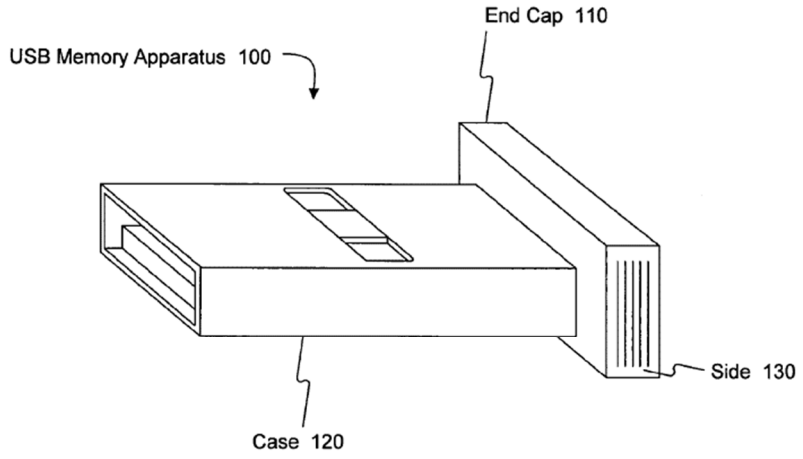


FIG. 1
MTI-1005, FIG. 1

(b) Element 1[a]

182. Claim element 1[a] recites "a housing." The combination of Tomio and Sukegawa provides claim element 1[a]. For example, Sukegawa discloses a USB connector shield case, an overmold boot, and an end cap:

> FIG. 1 is an exterior illustration of an exemplary USB memory storage apparatus according to an embodiment of the present invention. Referring now to FIG. 1, exemplary USB memory apparatus 100 is an integrated flash drive apparatus shown with a **USB connector shield case 120**. **The circuit components of the flash drive apparatus can be mounted within case 120 in various configurations**. By doing so, there is no need for an external circuit board or substantial structure outside the USB connector shield case 120. In this embodiment, the USB connector shield case 120 is from

a USB Series A plug. A set of contact terminals (shown in more detail in FIG. 4A-C) is disposed within the connector shield case 120 is in a known configuration to line up with a mating USB connector.

Attached to the USB connector shield case 120 is an end cap 110. End cap 110 can be used as a handle to pull the apparatus out from the host system's USB connection or interface. In the embodiment illustrated in FIG. 1, ridged side surfaces 130 of end cap 110 provide a gripping surface so that a user can grab hold of the apparatus 110 when inserting or removing it from the host system. In this embodiment, end cap 110 is made of a molded plastic typically with a logo on an exterior surface.

MTI-1005, 4:44-66.

In this manner, the different types of **end caps in embodiments of the invention provide a relatively low-profile, unobtrusive, and compact exterior** for use with reduced size USB flash drive apparatus.

MTI-1005, 5:20-24.

In this embodiment, the USB connector is a Series A Plug connector for use in connecting to host systems on the upstream. As indicated in the USB 2.0 Specification, the Series A Plug includes a **Plug Housing (more generally referred to as a USB connector shield case 120) that extends from an overmold boot (not shown) on an end of the connector opposite the contact terminals** 400A-D.

MTI-1005, 7:26-37.

> FIGS. 5A-5G show how the device, implemented as one or more **modules, can be mounted within the exemplary USB connector shield case** according to different embodiments of the invention.

MTI-1005, 8:6-62, FIGS. 5A-5G.

> In another embodiment of the present invention, a portion of the active circuitry for the device (e.g., at least one of the circuit modules that implement device 200) may be **mounted within the USB connector** while the remainder of the active circuitry modules for the device are mounted outside the USB connector.

MTI-1005, 8:63-9:16, FIG. 5H.

183. Based on my review of Tomio and Sukegawa, the combination of Tomio and Sukegawa provides a USB flash drive that includes "a USB connector shield case 120," "an overmold boot," and "an end cap 110." MTI-1005, 4:44-66, 7:26-37. A POSITA would have found it obvious that Tomio-Sukegawa's USB flash drive has a housing in the form of the USB connector shield case 120, overmold boot, and end cap 110 that beneficially provides "a relatively low-profile, unobtrusive, and compact exterior for use with reduced size USB flash drive apparatus" within which the circuit components are mounted. MTI-1005, 5:20-24.

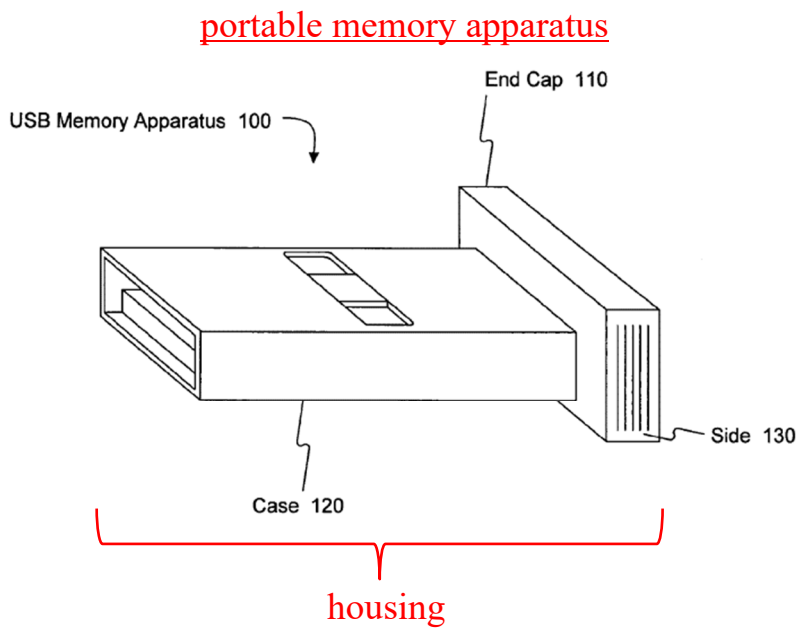


FIG. 1

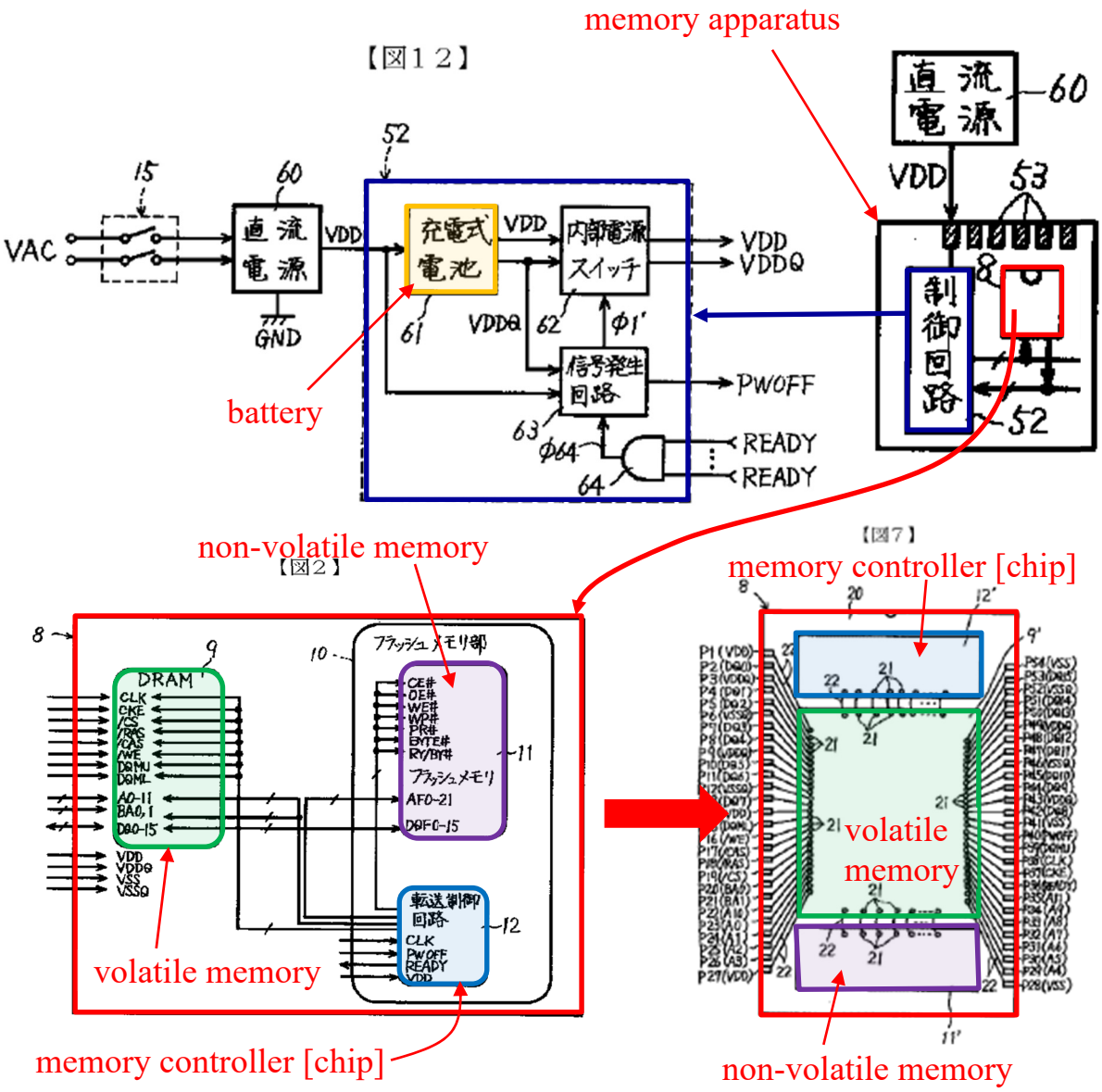
MTI-1005, FIG. 1

(c) Elements 1[b]-1[d]

184. Claim element 1[b] recites "a memory controller comprised in the housing." Claim element 1[c] recites "a volatile memory coupled to said memory controller comprised in the housing." Claim element 1[d] recites "a non-volatile memory coupled to said memory controller comprised in the housing." The combination of Tomio and Sukegawa provides claim elements 1[b]-1[d].

185. As discussed in the analysis of the combination of Tomio and Sukegawa (Section VIII.E.1), a POSITA would have found it obvious, from Tomio's explicit teachings, to implement a memory apparatus with one semiconductor memory and a control circuit mounted on a substrate, as shown below. MTI-1006,

[0018]-[0024], [0025]-[0026], [0028], [0030]-[0032], [0034]-[0035], [0043]-[0044], [0048], FIGS. 2, 7-9, claims 1-6 (claiming the elements of one semiconductor memory and a control circuit), [0045]-[0050] (describing the same). As discussed in the analysis of claim elements 1[b]-1[d] with respect to Tomio, the semiconductor memory includes a DRAM 9/9′ (volatile memory) (green) couple to a transfer control circuit 12/12′ (blue) and a flash memory 11/11′ (non-volatile memory) (purple) couple to the transfer control circuit 12/12′ (blue), as shown below. MTI-1006, [0018], [0030]-[0031], [0034]-[0035], [0043].



MTI-1006, FIGS. 2, 7, 11, 12
(modified to show one semiconductor memory 8 and collated)

186. For a USB flash drive implementation, as discussed in the analysis of claim element 1[a] with respect to the Tomio-Sukegawa combination, Sukegawa teaches that "[t]he circuit components of the flash drive apparatus can be mounted within case 120 in various configurations" or "a portion of the active circuitry for the device (e.g., at least one of the circuit modules that implement device 200) may

be mounted within the USB connector while the remainder of the active circuitry modules for the device are mounted outside the USB connector" such as in the overmold boot or end cap 110. MTI-1005, 4:44-66, 5:20-24, 7:26-37, 8:6-9:31, FIGS. 5A-5H. Sukegawa further discloses that:

> Referring now to FIG. 2, **an exemplary semiconductor device 200** is shown connected to a USB host system 205. In this embodiment, the electrical circuits that make up the integrated USB memory apparatus are integrated within the device 200 so that they can fit within a USB connector (or at least have a majority of the circuits mounted within the USB connector shield case). These circuits **include, but are not necessarily limited to, a memory controller 210, NAND flash memory 215**, and a clock source 220.

MTI-1005, 5:29-37.

> However, other conventional and new packages may be used to implement embodiments of the invention depending on the available physical space within the USB connector and the desired functionality of the memory apparatus. **electrical circuit components in distinct and separate circuit modules that can be electrically connected when mounted within different parts of the USB connector**. In other words, alternative embodiments of the present invention may implement the device in separate modules (each of which may be a multi-chip package have one or more chips) to more readily take advantage of the limited available space within the physical confines of the USB connector shield case.

MTI-1005, 7:6-18.

> FIGS. 5A-5G show how the device, implemented as one or more modules, can be mounted within the exemplary USB connector shield case according to different embodiments of the invention.

MTI-1005, 8:6-9.

> In some situations, it may be advantageous to add a second circuit board for use in mounting certain circuit modules. Typically, the second circuit board is kept within the confines of the USB connector shield case. However, it is contemplated that the second circuit board may be disposed outside the USB connector shield case but within close proximity to the case and within the end cap. This is another example of how a majority of the structure for the memory apparatus can be kept within the USB connector shield case.

MTI-1005, 8:26-35.

> FIG. 5G shows a configuration where **the device 200 is implemented with three different modules**. The first is mounted on the bottom of the first circuit board 410, the second is mounted within the block 420, and the third is mounted on the second circuit board 520. Thus, the circuit modules that make up device 200 may be mounted in a variety of locations to keep all or a majority of the apparatus structure within the physical confines of the USB connector shield case.

MTI-1005, 8:54-62.

187. Based on my knowledge and experience in this field and my review of Tomio and Sukegawa, a POSITA would have found it obvious to implement, in

Tomio-Sukegawa's USB flash drive, the memory control unit (memory controller [chip]), the SDRAM (volatile memory), and the flash memory (non-volatile memory) as one, two, or three modules that are mounted within the housing formed by the USB connector shield case 120, overmold boot, and end cap 110 to provide a very small, inexpensive, portable and removable storage media. *Id*. Based on my knowledge and experience in this field, a POSITA would have been capable of employing ordinary creativity to carry out an implementation of the USB flash drive with the memory control unit (memory controller [chip]), the SDRAM (volatile memory), and the flash memory (non-volatile memory) mounted within the housing in a manner necessary to achieve the advantages taught by Sukegawa by, for example, varying the size and shape of the housing to accommodate the electronic components, as corroborated by other publications illustrating USB flash drives in varying shapes and sizes. *Id*.; *see, e.g.,* MTI-1013; MTI-1017; MTI-1018; MTI-1019; MTI-1020. An example of an implementation of the USB flash drive with the memory control unit (memory controller [chip]), the SDRAM (volatile memory), and the flash memory (non-volatile memory) as three different modules mounted within the housing is shown below.

portable memory apparatus

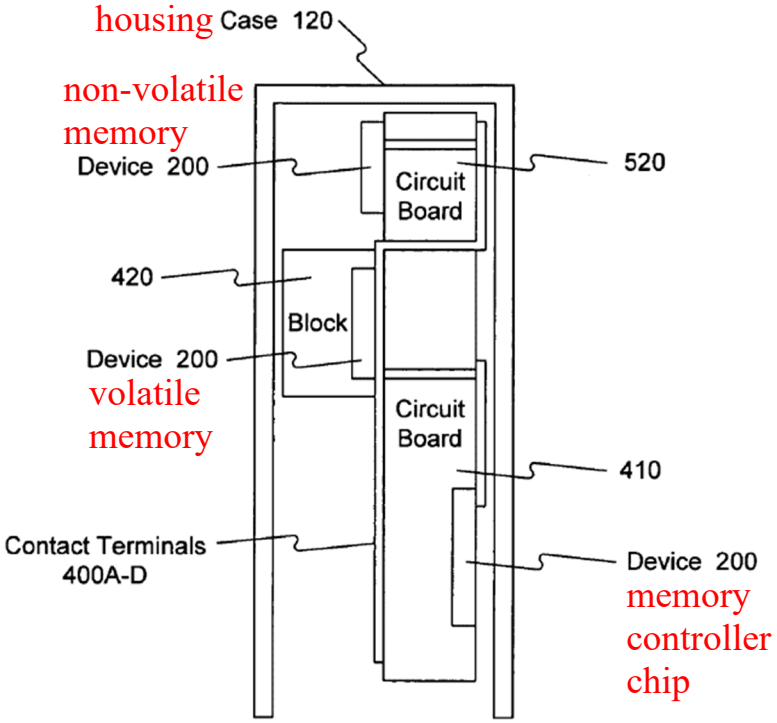


FIG. 5G

MTI-1005, FIG. 5G

(d) Element 1[e]

188. Claim element 1[e] recites "a connector positioned on the housing, wherein said connector couples said portable memory apparatus to a computer system when said connector is plugged into said computer system." The combination of Tomio and Sukegawa provides claim element 1[e]. For example, Sukegawa discloses a USB connector in the USB connector shield case:

In general, the USB flash drive is a small memory storage apparatus that **interfaces with a host system through a USB connector**.

MTI-1005, 1:38-40.

A **set of contact terminals** (shown in more detail in FIG. 4A-C) is disposed within the connector shield case 120 is **in a known configuration to line up with a mating USB connector**.

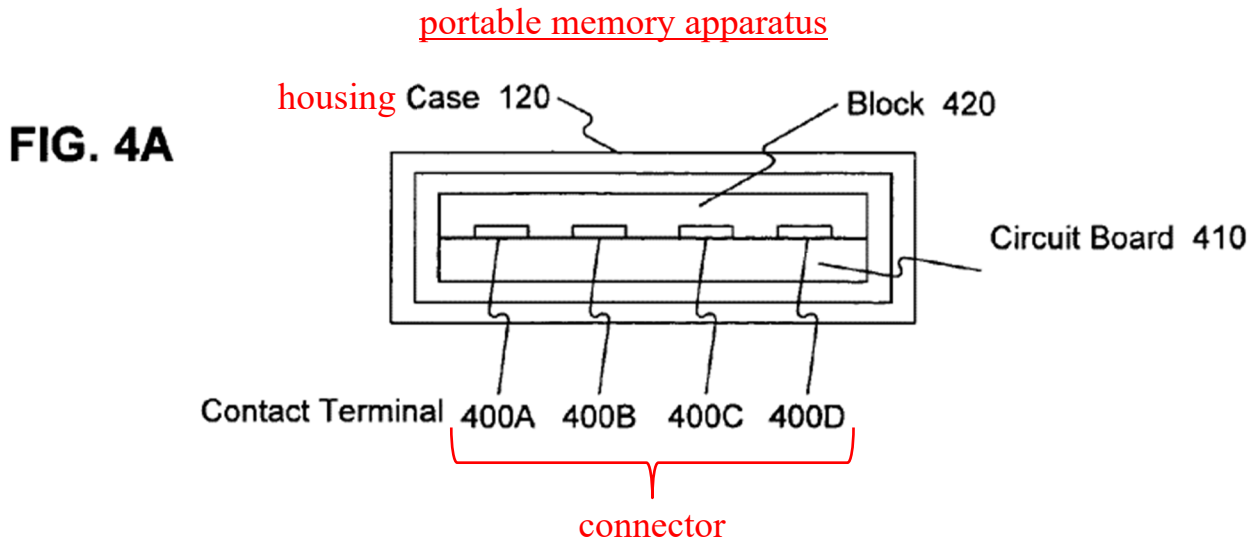
MTI-1005, 4:54-57.

In this embodiment, **the USB connector is a Series A Plug connector for use in connecting to host systems** on the upstream. As indicated in the USB 2.0 Specification, the Series A Plug includes **a Plug Housing (more generally referred to as a USB connector shield case 120)** that extends from an overmold boot (not shown) on an end of the connector opposite the contact terminals 400A-D. The overmold boot is typically an injection molded thermoplastic insulator material with a minimum UL94-VO rating.

....

A set of **contact terminals 400A-D** is shown disposed on a portion of the top side of a first circuit board 410 **within the USB connector shield case 120**. As shown in FIG. 4B, **the set of contact terminals 400A–D are arranged in a standard USB configuration to line up with a mating USB interface or connector**. In this manner, terminal 400A is deemed to be ground, terminal 400B is deemed to be +D, terminal 400C is deemed to be -D, and terminal 400D is deemed to be $+V_{BUS}$ according to the USB standard.

MTI-1005, 7:26-52. Sukegawa's disclosure of a connector "positioned on the housing" is commensurate in scope with the '527 patent's description of this limitation. MTI-1001, 1:42-45 ("The portable RAM drive may comprise a housing... and a connector to connect the portable RAM drive to the computer system."), 2:36-37 ("The portable RAM drive 103 may include a housing 104 and a connector 105."), 2:44-54, 2:57-61 ("the housing 104 of the portable RAM drive 103 may comprise a USB connection 401"), 3:48-52 ("a connector on the portable RAM drive").



MTI-1005, FIG. 4A

189. Based on my knowledge and experience in this field and my review of Tomio and Sukegawa, Tomio-Sukegawa's USB flash drive "interfaces with a host system through a USB connector." MTI-1005, 1:38-40, 7:26-52 ("USB connector is a Series A Plug connector for use in connecting to host systems."). The USB connector includes a "set of contact terminals (shown in more detail in FIG. 4A-C)...

disposed within the connector shield case 120... in a known configuration to line up with a mating USB connector." MTI-1005, 4:54-57. Accordingly, Tomio-Sukegawa's USB flash drive (portable memory apparatus) has a USB connector that is positioned on the connector shield case 120 (forming the housing) and that couples the USB flash drive to a host, which is a personal computer as discussed in the analysis of claim element 1[e] with respect to Tomio and further confirmed by Pua (U.S. Application Publication No. 2002/0147882), when the USB connector is plugged into the host. MTI-1013, [0090] ("USB host 300 such as Windows ME and Windows 2000").

(e) Element 1[f]

190. Claim element 1[f] recites "wherein, when said connector couples said portable memory apparatus to said computer system, said memory controller chip copies data from said non-volatile memory to said volatile memory, and said computer system accesses said data in said volatile memory through said connector." The combination of Tomio and Sukegawa provides claim element 1[f]. As discussed in the analysis of claim element 1[e] with respect to the combination of Tomio and Sukegawa, Tomio-Sukegawa's USB flash drive connects to the host (computer system) via the USB connector. Also as discussed in the analysis of claim element 1[f] with respect to Tomio, when the terminals (connector) couples the memory module (portable memory apparatus) to the personal computer (computer system),

the transfer control circuit (memory controller chip) copies data from the flash memory (non-volatile memory) to the DRAM (volatile memory), and the personal computer accesses the data in the DRAM through the terminals. MTI-1006, [0019], [0022]-[0026], [0032], [0038]. Based on my knowledge and experience in this field and my review of Tomio and Sukegawa, when Tomio-Sukegawa's USB flash drive is connected to the personal computer (computer system) via the USB connector (as discussed in the analysis of claim element 1[e] with respect to the combination of Tomio and Sukegawa), the transfer control circuit (memory controller chip) copies data from the flash memory (non-volatile memory) to the DRAM (volatile memory), and the personal computer accesses the data in the DRAM through the USB connector in a similar manner and for similar reasons as discussed in the analysis of claim element 1[f] with respect to Tomio.

3. Claims 2, 4, and 5

191. Claim 2 recites:

> The portable memory apparatus of claim 1, further comprising an internal power source coupled to said portable memory apparatus.

Claim 4 recites:

> The portable memory apparatus of claim 2, wherein said internal power source is rechargeable through said connector.

Claim 5 recites:

> The portable memory apparatus of claim 4, wherein said internal

power source comprises a battery or a capacitor.

For similar reasons discussed in the analysis of claims 2, 4, and 5 with respect to the combination of Tsunoda, alone or with Sukegawa, and Tomio, Tomio-Sukegawa's USB flash drive includes a rechargeable battery (internal power source) that is rechargeable through the USB connector and that continues to supply power long enough to copy data from volatile memory to nonvolatile memory in the event that the external power to the memory apparatus is abruptly stopped.

4. Claim 3

192. Claim 3 recites:

> The portable memory apparatus of claim 2, wherein said internal power source powers said portable memory apparatus when said portable memory apparatus is unplugged from said computer system, said portable memory apparatus copies data from said volatile memory to said non-volatile memory when said portable memory apparatus is unplugged from said computer system.

For similar reasons discussed in the analysis of claim 3 with respect to the combination of Tsunoda, alone or with Sukegawa, and Tomio, Tomio-Sukegawa's rechargeable battery (internal power source) powers the module 51 and the module 51 copies data from the DRAM (volatile memory) to the flash memory (non-volatile memory) when the module 51 is unplugged from the personal computer (computer system).

5. Claim 6

193. Claim 6 recites:

> The portable memory apparatus of claim 1, wherein said memory controller chip transfers said non-volatile memory with data written to said volatile memory from said computer system while said portable memory apparatus is coupled to said computer system.

The language "said memory controller chip transfers said non-volatile memory with data written to said volatile memory from said computer system" is subject to the following possible constructions: (1) the memory controller chip "transfers *to* said non-volatile memory data written to said volatile memory from said computer system" (*i.e.*, the italicized "to" should be inserted and "with" should be deleted), (2) the memory controller chip "transfers *from* said non-volatile memory data written to said volatile memory from said computer system," or (3) the memory controller chip "transfers data *from* the non-volatile memory *to* the volatile memory so that it can be accessed by the host computer." Tomio provides claim 6 under any of these possible constructions.

194. If "said memory controller chip transfers said non-volatile memory with data written to said volatile memory from said computer system" were construed to mean the memory controller chip "transfers *to* said non-volatile memory data written to said volatile memory from said computer system," the

combination of Tomio and Sukegawa renders this obvious for the reasons discussed in the analysis of claim 3 with respect to Tomio.

195. If "said memory controller chip transfers said non-volatile memory with data written to said volatile memory from said computer system" were construed to mean "transfers *from* said non-volatile memory data written to said volatile memory from said computer system" or "transfers data *from* the non-volatile memory *to* the volatile memory so that it can be accessed by the host computer," the combination of Tomio and Sukegawa renders this obvious for the reasons discussed in the analysis of claim element 1[f] with respect to Tomio.

6. Claim 7

196. Claim 7 recites:

> The portable memory apparatus of claim 6, further comprising an indicator coupled to said portable memory apparatus, wherein said indicator indicates when data stored in said volatile memory is being transferred to said non-volatile memory.

The combination of Tomio and Sukegawa provides claim 7. For example, Sukegawa discloses lights that indicate when the flash memory is being accessed:

> Additionally, end cap 110 may have an opening to expose one or more **lights that indicate connection to the host system, access to the apparatus memory or both**.

MTI-1005, 4:67-5:2.

> In a further alternative embodiment, end cap 110 may be made of a

> visually opaque material capable of reflecting **light** in many directions **when the apparatus is being accessed** or simply when the apparatus has been properly inserted within the host system.

MTI-1005, 5:16-20.

> Additionally, one or more **lights** (not shown) may also be connected to the controller 210 within device 200 to **provide an indication that the device 200 is properly connected to USB host 205 and if NAND flash memory 215 is being accessed**. In one embodiment, the light may be an LED incorporated into the end cap 110 and wired to the controller 210. In other embodiments, the light may be implemented as one or more display devices (e.g., one or more discrete LEDs, an integrated group of LEDs, a small LCD display on the end of the USB connector shield case, etc.) that provides the desired indications to the user.

MTI-1005, 6:21-31. Based on my knowledge and experience in this field and my review of Tomio and Sukegawa, Tomio-Sukegawa's USB flash drive includes "one or more lights that indicate connection to the host system, access to the apparatus memory or both." MTI-1005, 4:67-5:2, 5:16-20, 6:21-31. In Tomio-Sukegawa's USB flash drive, the lights would indicate when the flash memory is being or has been accessed, for example, when data stored in the DRAM (volatile memory) is being or has been transferred to the flash memory (non-volatile memory), as this is a typical usage of indicator lights on a USB flash drive. MTI-1013, [0016] ("The flash memory storage device... comprises an indicator, for

example an LED indicator, which indicates the status of the memory storage device such as whether it is busy or in standby."), [0072].

7. Claim 9

197. Claim 9 recites:

> The portable memory apparatus of claim 1, wherein said volatile memory is selected from a group consisting of FPM DRAM, EDO DRAM, SDRAM, RDRAM, and SRAM.

For the reasons discussed in the analysis of claim element 1[c] with respect to Tomio, the combination of Tomio and Sukegawa provides claim 9.

8. Claim 10

198. Claim 10 recites:

> The portable memory apparatus of claim 1, wherein said connection is selected from a group consisting of USB connector, firewire connector, and ATA serial connector.

For the reasons discussed in the analysis of claim element 1[e] with respect to the combination of Tomio and Sukegawa, the combination of Tomio and Sukegawa provides claim 10.

9. Claims 11 and 14

199. Claim 11 recites:

> The portable memory apparatus of claim 1, further comprising an outer impact resistant shell.

Additionally, claim 14 recites:

The portable memory apparatus of claim 1, wherein said housing comprises a material selected from ABS plastic and polycarbonate.

The combination of Tomio and Sukegawa provides claims 11 and 14. As discussed in the analysis of claim element 1[a] with respect to the combination of Tomio and Sukegawa, a POSITA would have found it obvious that Tomio-Sukegawa's USB flash drive has a housing in the form of the USB connector shield case 120, overmold boot, and end cap 110. Sukegawa further discloses that:

> **Attached to the USB connector shield case 120 is an end cap 110**. End cap 110 can be used as a handle to pull the apparatus out from the host system's USB connection or interface. In the embodiment illustrated in FIG. 1, ridged side surfaces 130 of end cap 110 provide a gripping surface so that a user can grab hold of the apparatus 110 when inserting or removing it from the host system. In this embodiment, **end cap 110 is made of a molded plastic** typically with a logo on an exterior surface.

MTI-1005, 4:58-66.

> In this embodiment, the USB connector is a Series A Plug connector for use in connecting to host systems on the upstream. As indicated in the USB 2.0 Specification, the Series A Plug includes a **Plug Housing (more generally referred to as a USB connector shield case 120) that extends from an overmold boot (not shown)** on an end of the connector opposite the contact terminals 400A-D. **The overmold boot is typically an injection molded thermoplastic insulator material with a minimum UL 94-VO**

rating.

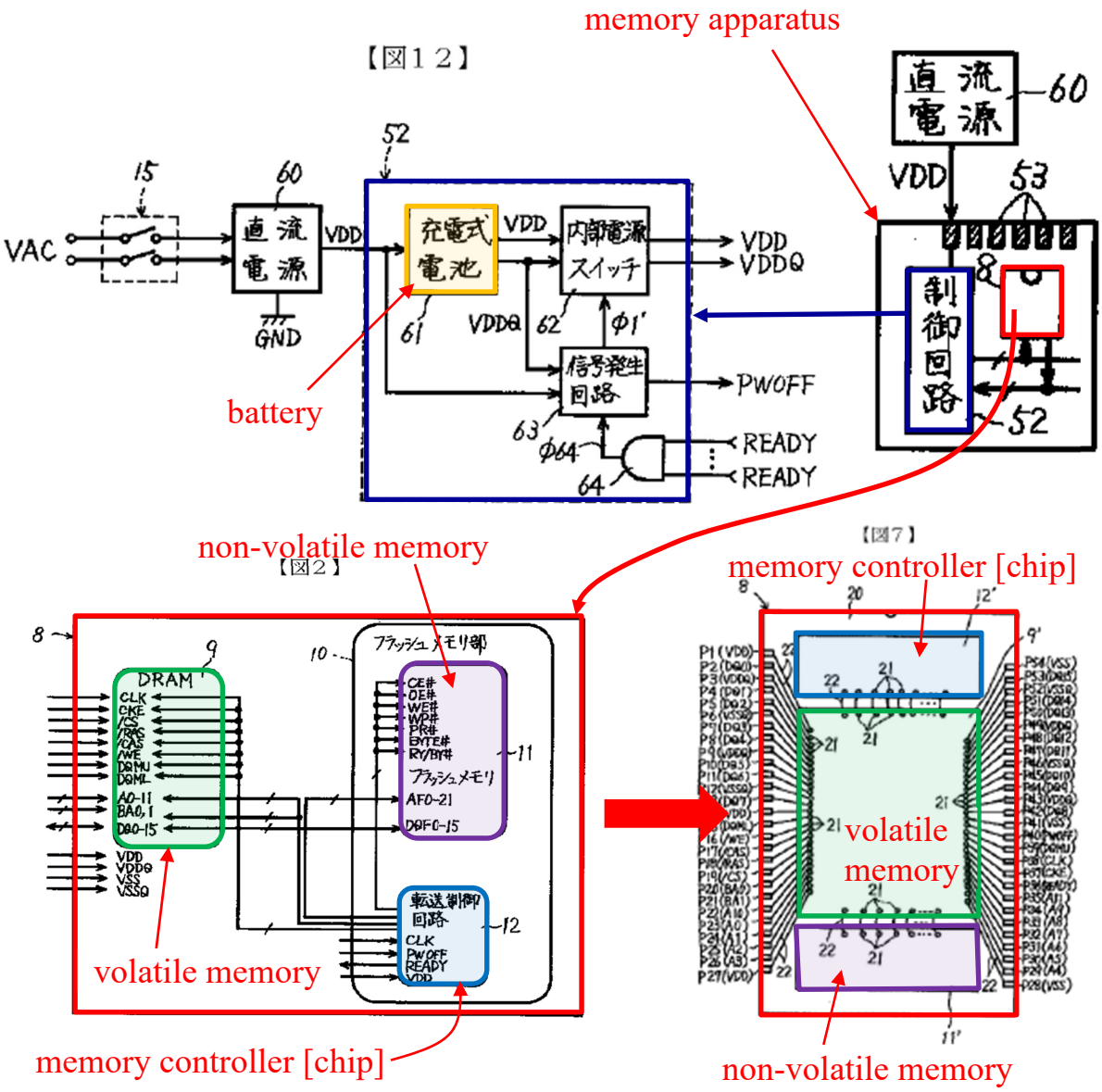
MTI-1005, 7:26-37. Based on my knowledge and experience in this field, it would have been well within the general knowledge of a POSITA that the "injection molded thermoplastic insulator material with a minimum UL 94-VO rating" includes materials such as ABS, which possesses outstanding impact strength, to form a rigid impact resistant plastic housing. For example, one publication discloses that "Plastic Products for UL-94 Flame Class" include "ABS." MTI-1014, 4. Another publication titled "UL 94 Classification and Flame-Retardant Thermoplastics" discloses that "stocked materials with UL 94 V-O or greater" include "ABS." MTI-1015, 2. One publication describes that "ABS possesses outstanding impact strength" and is "impact resistant." MTI-1011. Another publication describes the "Major Application Characteristics" of "Acrylonitrile-Butadiene-Styrene (ABS)" as including "Outstanding strength and toughness." MTI-1023, 10. Based on my knowledge and experience in this field and my review of Tomio and Sukegawa, a POSITA would have found it an obvious design choice to use ABS to form at least a portion of the housing (e.g., the overmold boot and end cap) of Tomio-Sukegawa's USB flash drive to beneficially provide an outer shell that has outstanding impact strength, toughness, and resistance to protect the components of the flash drive from damage due to mishandling, moisture, dust and debris, and electrostatic discharge.

10. Claim 12

200. Claim 12 recites:

> The portable memory apparatus of claim 1, wherein said portable memory apparatus does not have any moving parts.

The combination of Tomio and Sukegawa provides claim 12. As discussed in the analysis of the combination of Tomio and Sukegawa (Section VIII.E.1), a POSITA would have found it obvious, from Tomio's explicit teachings, to implement a memory apparatus with one semiconductor memory and a control circuit mounted on a substrate, as shown below. MTI-1006, [0018]-[0024], [0025]-[0026], [0028], [0030]-[0032], [0034]-[0035], [0043]-[0044], [0048], FIGS. 2, 7-9, claims 1-6 (claiming the elements of one semiconductor memory and a control circuit), [0045]-[0050] (describing the same). As discussed in the analysis of claim 12 with respect to Tomio, FIG. 7 shows a possible configuration of a semiconductor memory 8 with input/output pins P1-P54, a DRAM chip 9', a flash memory chip 11', and a transfer control circuit chip 12' connected via pads 21 and bonding wires 22 provided in a package 20. As discussed in the analysis of claim elements 1[b]-1[d] with respect to Tomio, the semiconductor memory includes a DRAM 9/9′ (volatile memory) (green) couple to a transfer control circuit 12/12′ (blue) and a flash memory 11/11′ (non-volatile memory) (purple) couple to the transfer control circuit 12/12′ (blue), as shown below. MTI-1006, [0018], [0030]-[0031], [0034]-[0035], [0043].



MTI-1006, FIGS. 2, 7, 11, 12
(modified to show one semiconductor memory 8 and collated)

201. Based on my knowledge and experience in this field and my review of Tomio and Sukegawa, Tomio-Sukegawa's USB flash drive includes a DRAM chip 9′, a flash memory chip 11′, and a transfer control circuit chip 12′ connected via pads 21 and bonding wires 22. MTI-1006, [0030]-[0031]; MTI-1005, 4:48-50, 6:42-7:18, 8:6-9:16, FIGS. 3, 5A-5H. A POSITA would have found it obvious that Tomio-

Sukegawa's USB flash drive, which includes DRAM, flash memory, and transfer control circuit on different silicon chips housed in a USB connector shield case 120 that "extends from an overmold boot" "on an end of the connector opposite the contact terminals" and an end cap 110, as shown below, does not have any moving parts. MTI-1004, [0124]; MTI-1005, 4:58-59, 7:26-32, FIG. 1. Cheng (U.S. Patent Application Publication No. 2002/0010827) confirms that "a portable data storage device comprising a coupling device with an interface device, memory control device and a non-volatile solid-state memory device ... does not include moving parts..." so as "to be more compact than conventional portable data storage devices." MTI-1012, [0005], [0031].

portable memory apparatus

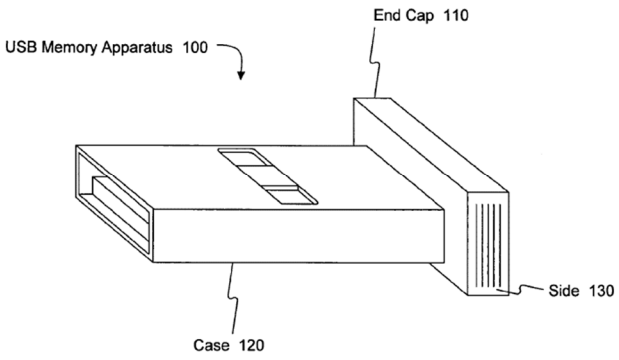


FIG. 1

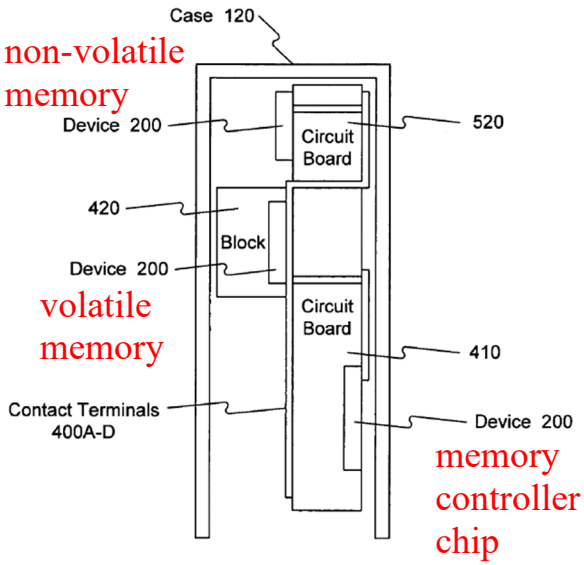


FIG. 5G

11. Claim 15

(a) Element 15[p]

202. The preamble of claim 15 recites "[a] method." The combination of Tomio and Sukegawa provides a method as recited in the preamble of claim 15 as set forth below in the analysis of claim elements 15[a]-15[e] with respect to the combination of Tomio and Sukegawa.

(b) Element 15[a]

203. Claim element 15[a] recites "coupling a portable memory apparatus to a computer system." For the reasons discussed in the analysis of claim elements 1[p] and 1[e] with respect to the combination of Tomio and Sukegawa, the combination of Tomio and Sukegawa provides claim element 15[a].

(c) Element 15[b]

204. Claim element 15[b] recites "wherein said portable memory apparatus comprises a memory controller chip, a non-volatile memory, and a volatile memory." For the reasons discussed in the analysis of claim elements 1[b], 1[c], 1[d] with respect to the combination of Tomio and Sukegawa, the combination of Tomio and Sukegawa provides claim element 15[b].

(d) Element 15[c]

205. Claim element 15[c] recites "copying data from said non-volatile memory to said volatile memory using said memory controller chip." For the reasons discussed in the analysis of claim element 1[f] with respect to the combination of Tomio and Sukegawa, the combination of Tomio and Sukegawa provides claim element 15[c].

(e) Element 15[d]

206. Claim element 15[d] recites "accessing said data in said volatile memory using said computer system through a connector coupled to said portable memory apparatus and said memory controller chip." For the reasons discussed in the analysis of claim element 1[f] with respect to the combination of Tomio and Sukegawa, the combination of Tomio and Sukegawa provides claim element 15[d].

(f) Element 15[e]

207. Claim element 15[e] recites "updating said non-volatile memory with data from said volatile memory." For the reasons discussed in the analysis of claim 6 with respect to the combination of Tomio and Sukegawa, the combination of Tomio and Sukegawa provides claim element 15[e].

12. Claim 16

208. Claim 16 recites:

> The method of claim 15, further comprising: powering said portable memory apparatus with an internal power source coupled to said

portable memory apparatus, when said portable memory apparatus is unplugged from said computer system, to transfer said non-volatile memory with data from said volatile memory.

For the reasons discussed in the analysis of claims 2 and 3 with respect to Tomio, the combination of Tomio and Sukegawa provides claim 16.

13. Claim 17

209. Claim 17 recites:

> The method of claim 15, further comprising: recharging an internal power source coupled to said portable memory apparatus.

For the reasons discussed in the analysis of claim 4 with respect to Tomio, the combination of Tomio and Sukegawa provides claim 17.

14. Claim 18

210. Claim 18 recites:

> The method of claim 15, further comprising: indicating when data stored in said volatile memory has been transferred to said non-volatile memory.

For the reasons discussed in the analysis of claim 7 with respect to the combination of Tomio and Sukegawa, the combination of Tomio and Sukegawa provides claim 18.

F. Analysis of Tsunoda, alone or with Sukegawa, Tomio, in view of Shigeo with respect to Claims 13 and 20 and Analysis of Tomio,

alone or with Sukegawa, in view of Shigeo with respect to Claims 13 and 20

211. For the reasons articulated in detail below, and based on my review of the '527 patent and the Tsunoda, Sukegawa, Tomio and Shigeo references, I am confident that a POSITA would have readily understood that Tsunoda, alone or with Sukegawa, Tomio, in view of Shigeo renders obvious all elements of claims 13 and 20 and that Tomio, alone or with Sukegawa, in view of Shigeo renders obvious all elements of claims 13 and 20.

1. Overview of Shigeo

212. Shigeo relates to preventing the loss of data stored in volatile memory when remaining battery power is low. MTI-1007, [0009]-[0012]. Shigeo recognized that "information such as the current state of the computer, an address book, and documents" is stored in "nonvolatile memory such as flash memory" "when the power is turned off." MTI-1007, [0005]. "Memory that does not lose its content when the power is turned off often has very slow read and write access speeds." *Id.* In order to avoid the slow access speed of nonvolatile memory, the data is read from nonvolatile memory and "stored in RAM, which is a volatile memory but with a high access speed." MTI-1007, [0006].

213. Shigeo explains that information stored in volatile memory "becomes corrupted" when the battery does not have enough power to power the volatile memory, and "is lost if enough power is not supplied" to the volatile memory "due

to a decrease in the power supply capacity of the battery" and "the battery dies." MTI-1007, [0009]-[0010], [0061]. In Shigeo, when information is stored in volatile RAM, the capacity of the battery becomes low, and the contents of the volatile RAM may become corrupted, the contents are automatically written and saved in flash memory, and data is directly written to flash memory without using the volatile RAM "to minimize data loss even if the battery runs out during a writing operation." MTI-1007, [0071], [0082], [0089]. When data is to be read, if the data is in volatile RAM, it is read from volatile RAM, but if the data is not in volatile RAM, it is read from flash memory. MTI-1007, [0084]-[0085]. When the battery power has been restored by charging, the information saved in flash memory is read to the volatile RAM and restored, and normal read/write processing is performed. MTI-1007, [0072], [0083].

214. Shigeo thus provides a storage medium that prevents the loss of information "when the power supply capacity decreases by detecting that the power supply capacity is decreasing, automatically saving (writing) the... information in the RAM to a predetermined save region in the flash ROM when the power supply capacity falls below a predetermined threshold value, and restoring (copying) the saved... information to the RAM the power supply capacity is once again sufficient due to charging." MTI-1007, [0011], [0094], [0096]. Shigeo also aims to "reduce

the amount of data loss if the battery dies during a writing operation." MTI-1007, [0012].

2. Combination of Tsunoda, alone or with Sukegawa, Tomio, and Shigeo and Combination of Tomio, alone or with Sukegawa, and Shigeo

215. As discussed in the analysis of element 1[f] with respect to Tsunoda and Tomio, Tsunoda and Tomio both describe transferring data stored in flash memory to volatile RAM when the memory apparatus first receives power from the computer system. MTI-1004, [0042]-[0043], [0048]-[0049], [0062], [0068], [0078], [0080]-[0084], [0093], [0096], [0099], [0131], [0139]-[0140], FIGS. 18, 23, FIG. 24 (4061-4062), FIG. 25 (4101-4105), FIG. 26 (4206); MTI-1006, [0022]-[0024], [0032]. Tomio also discloses that all data in the flash memory is erased after completing the data transfer "because all data in the memory cells has to be erased in order to write data to flash memory." MTI-1006, [0026]. In both Tsunoda and Tomio, data in volatile RAM is stored in flash memory when the external power supply is stopped or turned off. MTI-1004, [0042]-[0043], [0046]-[0047], [0062], [0068], [0078], [0085]-[0088], [0093], [0098]-[0099], [0104], [0112], [0133]-[0138], FIGS. 20-22, 24 (4063-4065), 25 (4107, 4109-4113), 26 (4206); MTI-1006, [0032]. In the event that the external power supply is abruptly stopped, Tomio's module includes a "rechargeable battery 61" that "continues to output direct current power supply potentials VDD and VDDQ for a predetermined period of time even

when supply of the direct current power supply potential VDD from the direct current power supply 60 has been stopped." MTI-1006, [0039], [0027].

216. Shigeo explains that information stored in volatile RAM "becomes corrupted" when the battery does not have enough power to power the volatile RAM, and "is lost if enough power is not supplied" to the volatile RAM "due to a decrease in the power supply capacity of the battery" and "the battery dies." MTI-1007, [0009]-[0010], [0061]. Shigeo thus provides techniques for preventing the loss of data stored in volatile RAM when remaining battery power is low and reducing the amount of data loss if the battery dies during a writing operation. MTI-1007, [0009]-[0012]. A POSITA would have been motivated to apply the teachings of Shigeo to Tsunoda-Tomio's and Tomio's (each with or without Sukegawa) memory apparatus to prevent loss of the data stored in volatile RAM and reduce data loss during a writing operation in the event that the external power supply is abruptly stopped and the battery does not have enough power to power the volatile RAM and the flash memory for the writing of data to the flash memory. MTI-1006, [0032], [0039], [0027]; MTI-1007, [0009]-[0012], [0061].

217. Tsunoda and Tomio expressly contemplate transferring data stored in the flash memory to volatile RAM for faster access and transferring data stored in volatile RAM to flash memory before power is turned off. MTI-1004, [0042]-[0043], [0046]-[0049], [0062], [0068], [0078], [0080]-[0088], [0093], [0096]-

[0099], [0104], [0112], [0131], [0133]-[0140], FIGS. 18, 20-23, 24 (4061-4065), 25 (4101-4105, 4107, 4109-4113), FIG. 26 (4206); MTI-1006, [0004]-[0005],[0022]-[0024], [0028], [0032]. A POSITA implementing Tsunoda-Tomio's and Tomio's memory apparatus (each with or without Sukegawa) would have turned to examples of similar memory apparatus to identify suitable techniques for operating the memory module to prevent data loss. *Id.* Shigeo provides suitable techniques for operating a memory apparatus to prevent data loss. MTI-1007, [0009]-[0012], [0061]. Shigeo's teachings enable implementation of a memory apparatus, such as that provided by Tsunoda-Tomio and Tomio (each with or without Sukegawa), so as to prevent loss of the data stored in volatile RAM and reduce data loss during a writing operation in the event that the external power supply is abruptly stopped and the battery does not have enough power to power the volatile RAM and the flash memory for the writing of data to the flash memory. MTI-1006, [0032], [0039], [0027]; MTI-1007, [0009]-[0010], [0061], [0009]-[0012]. A POSITA would have been motivated to apply the teachings of Shigeo to Tsunoda-Tomio's and Tomio's memory apparatus (each with or without Sukegawa) to achieve these benefits. *Id.*

218. A POSITA would have viewed the implementation of Tsunoda-Tomio's and Tomio's memory apparatus (each with or without Sukegawa) in a manner that applied Shigeo's suggested techniques for operating the memory module to prevent data loss as merely the predictable result of combining known

prior art elements according to known methods. *Id.* A POSITA would have had a reasonable expectation of success in doing so as such an implementation was well-known as demonstrated by Shigeo and commonly utilized in similar memory apparatus. *Id.* A POSITA would have recognized that the above described modifications would have yielded predictable results, would have been within the ordinary level of skill of a POSITA, and would not have required undue experimentation. *Id.*

3. Claims 13 and 20

219. Claim 13 recites:

> The portable memory apparatus of claim 1, wherein said memory controller chip copies data from said non-volatile memory to said volatile memory after an internal power source has been recharged through said connection, that said internal power source has sufficient power to transfer data from said volatile memory to said non-volatile memory if said portable memory apparatus is unplugged from said computer system before said volatile memory is transferred to said non-volatile memory, wherein, until said internal power source recharges to said sufficient power, said computer system accesses said data on said non-volatile memory through said connector.

Similarly, claim 20 recites:

> The method of claim 15, further comprising: copying said data from said non-volatile memory to said volatile memory after an internal

> power source has been recharged through said connection, such that said internal power source has sufficient power to transfer data from said volatile memory to said non-volatile memory if said portable memory apparatus is unplugged from said computer system before said volatile memory is transferred to said non-volatile memory, wherein, until said internal power source recharges to said sufficient power, said computer system accesses said data on said non-volatile memory through said connector.

Each of the combination of Tsunoda, alone or with Sukegawa, Tomio, and Shigeo and the combination of Tomio, alone or with Sukegawa, and Shigeo provides claims 13 and 20.

220. As discussed in the analysis of element 1[f] with respect to each of Tsunoda and Tomio, Tsunoda and Tomio both describe transferring data stored in flash memory to volatile RAM when the memory apparatus first receives power from a host computer system. MTI-1004, [0042]-[0043], [0048]-[0049], [0062], [0068], [0078], [0080]-[0084], [0093], [0096], [0099], [0131], [0139]-[0140], FIGS. 18, 23, FIG. 24 (4061-4062), FIG. 25 (4101-4105), FIG. 26 (4206); MTI-1006, [0022]-[0024], [0032]. Also discussed in the analysis of claim 4 with respect to Tomio, Tomio describes a memory module that includes a rechargeable battery:

> In the modified example shown in Fig. 11, the module 51 is composed of a plurality of semiconductor memories 8 and a control circuit 52. The **control circuit 52 receives direct current power supply potential VDD from a direct current power supply 60**

outside of the module 51 via an input terminal 53, and supplies direct current power supply potentials VDD and VDDQ to each semiconductor memory 8 in the module 51.

...

The control circuit 52 includes **a rechargeable battery 61**, an internal power supply switch 62, a signal generating circuit 63, and an AND gate 64. **The rechargeable battery 61 is charged with the direct current power supply potential VDD from the direct current power supply 60** and outputs direct current power supply potentials VDD and VDDQ. The rechargeable battery 61 continues to output direct current power supply potentials VDD and VDDQ for a predetermined period of time even when supply of the direct current power supply potential VDD from the direct current power supply 60 has been stopped.

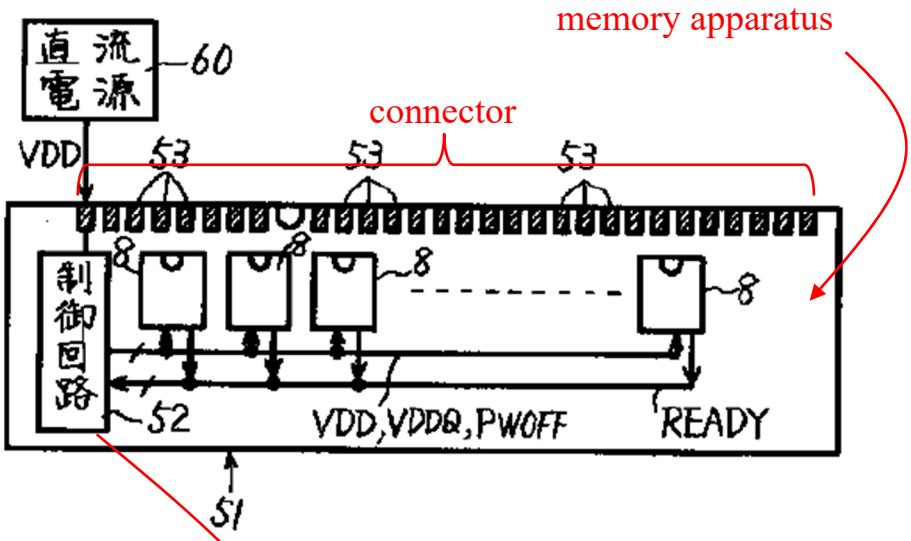
MTI-1006, [0038]-[0039].

When the external power supply switch 15 is turned off in ③ (time t3), the signal φ1 reaches the "L" level and the supply of the alternating current power supply voltage VAC for the direct current power supply 6 is stopped. Because the direct current power supply 6 includes **rechargeable batteries** as described above, it continues to output power supply voltages VCC, VDD, and VDDQ even when the supply of the alternating current power supply voltage VAC is stopped.

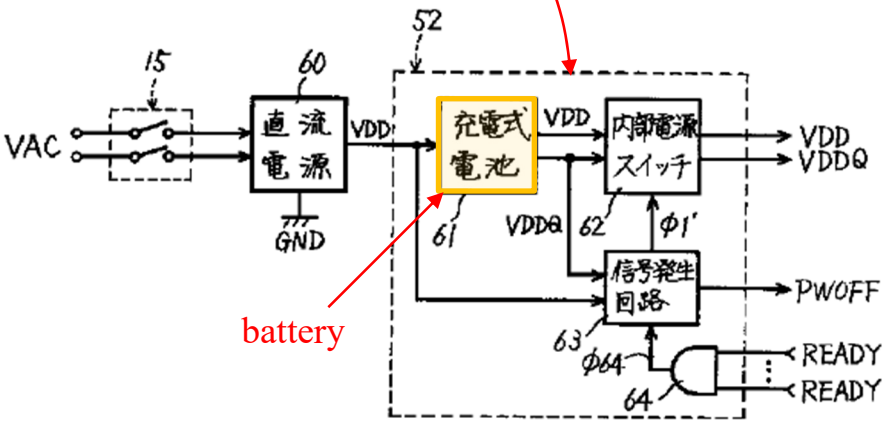
MTI-1006, [0027]. As shown in Tomio's FIGS. 11 and 12 (below), "control circuit 52 receives direct current power supply potential VDD from a direct current

power supply 60 outside of the module 51 via an input terminal 53" (of the connector). MTI-1006, [0038].

【図１１】



【図１２】



MTI-1006, FIGS. 11, 12 (collated, annotated)

221. Based on my knowledge and experience in the field and my review of Tomio, a POSITA would have found it obvious that if the external power supply is abruptly stopped and the battery is not sufficiently charged and does not have enough

power to power the volatile RAM and the flash memory for the writing of data to the flash memory, the data stored in the volatile RAM would be lost. For example, Tsunoda discloses that "[s]ince the SDRAM 4010 is a volatile memory, data written in the SDRRAM 4010 is lost when the power supply to the memory apparatus 4000 is stopped." MTI-1004, [0075]. Similarly, Tomio discloses that "DRAMs currently used in a wide variety of applications can be accessed at high speed, but are volatile memories that lose stored information when the power is turned off." MTI-1006, [0002], [0032], [0039], [0027]. Additionally, Shigeo discloses that "data stored in the volatile RAM is also lost when the remaining battery power is low and the battery dies." MTI-1007, [0009]-[0012], [0061].

222. To address such a problem, Shigeo discloses that:

> In the present embodiment, when the flash disk management information 8 is placed in the RAM 4, **the capacity of the battery or dry cell becomes low**, and the contents of the flash disk management information may become corrupted, **the contents are automatically written and saved in a predetermined save region of the flash ROM** if necessary.

MTI-1007, [0071], [0082].

> In the present embodiment, the user can write data to the mobile information device faster, and **data is written directly to** the nonvolatile RAM 103 [such as **flash ROM** which stores data even when no power supply voltage is supplied but whose access speed

is slower than that of volatile memory] **when the battery capacity of the mobile information device is low to minimize data loss even if the battery runs out during a writing operation**.

MTI-1007, [0089], [0074].

A situation will now be described in which **the user retrieves data** such as an address in an address book in the mobile information device. Fig. 12 is a flow chart showing the data read processing steps. This processing program, like the data writing processing program, is stored in the ROM 106 and executed by the CPU 104. First, the process determines whether or not the data requested by the user is in the temporary storage area for the nonvolatile RAM 103 allocated to the RAM 107 (step S801). This can be determined by checking and following the link in the table 401 in Fig. 9.

If the data to be read is in the RAM 107, it is read from the RAM 107 (see arrow a in Fig. 7; step S802). However, **if the data to be read is not in the RAM 107, it is read from the nonvolatile RAM 103** (see arrow c in Fig. 8; step S803). The process is then ended.

MTI-1007, [0084]-[0085]. While one of Shigeo's embodiments relates to preventing the loss of "flash disk management information" stored in volatile RAM, a POSITA would have found it obvious to apply Shigeo's teachings to prevent the loss of any data stored in volatile RAM that needs to be retained when the power is turned off.

223. Based on Shigeo's disclosures above, Shigeo teaches that when information is stored in volatile RAM, the capacity of the battery becomes low, and

the contents of the volatile RAM may become corrupted, the contents are automatically written and saved in the non-volatile memory, and data is directly written to the non-volatile memory without using the volatile RAM "to minimize data loss even if the battery runs out during a writing operation." MTI-1007, [0071], [0082], [0089], [0074]. When data is to be read, if the data is in volatile RAM, it is read from volatile RAM, but if the data is not in volatile RAM (which occurs in the case where data is directly written to the non-volatile memory without using the volatile RAM), it is read from non-volatile memory. MTI-1007, [0084]-[0085]. Accordingly, in the Tsunoda-Tomio-Shigeo and Tomio-Shigeo (each with or without Sukegawa) memory apparatus, when the battery is not sufficiently charged and the host (computer system) accesses the memory apparatus, the host reads/writes data from/to the flash memory (non-volatile memory) through the terminals (of the connector), until the battery (internal power source) recharges to sufficient power to transfer data from volatile RAM to the flash memory if the memory apparatus is unplugged from the host before data in the volatile RAM is transferred to the flash memory. MTI-1007, [0036], [0059], [0066], [0071], [0082], [0084]-[0085], [0089].

224. Shigeo also teaches that when the battery power has been restored by charging, the information saved in flash memory is read to the volatile RAM and restored, and normal read/write to volatile RAM is performed:

> Then, **when the power has been restored by charging** or

> replacing the battery and the reset process has been started, the saved flash disk management **information is read to a predetermined region of the RAM 4 and restored**. As a result, an information processing device can be provided that has a pseudo disk device **using flash ROM** whose content is not corrupted by a power drop even when flash disk management information is placed in a RAM that can be read from and written to at high speed.

MTI-1007, [0072], [0083]. As such, each of Tsunoda-Tomio-Shigeo and Tomio-Shigeo (each with or without Sukegawa) renders obvious that the memory controller chip copies data from the flash memory (non-volatile memory) to volatile RAM (volatile memory) after the battery (internal power source) has been recharged through the terminal (of the connector) to where the battery has sufficient power to transfer data from volatile RAM to said flash memory if the memory module is unplugged from the computer system before data in the volatile RAM is transferred to the flash memory.

IX. ADDITIONAL REMARKS

I currently hold the opinions set expressed in this declaration. But my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code.

Dated: May 04, 2023 By: 

David Kuan-Yu Liu, Ph.D.

APPENDIX A

DAVID KUAN-YU LIU, Ph.D.

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PROFESSIONAL PROFILE

- Technical expert with over 20 years of industrial experience in the development of advanced CMOS devices and process technology, with special emphasis on non-volatile semiconductor memory devices and process technology, and high-voltage semiconductor devices, with additional 12 years of experience serving as expert consultant.
    - Named inventor on 99 US patents.
- Consultant and expert witness for past 15 years in semiconductor intellectual property evaluation and patent litigation, with deposition experience and successful ITC trial testifying experience.
- Successful track record in transitioning products from development phase to high-volume manufacturing phase, both as an individual contributor and as manager/director.
- Co-founder of an LLC in the development and licensing of intellectual property with emphasis on embedded flash memory technology.
- Co-founder of a semiconductor memory start-up company (Progressant Technologies, Inc.); participated in its successful sale to Synopsys, Inc.
- Fluent in Mandarin Chinese (native language) and English; over 10 years experience as real-time translator of church sermons and proficient in written translation.

EDUCATION

Stanford University, Palo Alto, California

Ph.D., Electrical Engineering (1989)

Thesis: Physics and Technology of Novel Conductivity-Modulated Power MOSFET's

M.S., Electrical Engineering (1985)

Coursework in integrated-circuit technology, semiconductor device physics, computer modeling of semiconductor devices and fabrication processes, and solid-state physics

University of California, Berkeley, California

B.S., Electrical Engineering (1983)

Certificate of Distinction (awarded annually to the top EECS graduate)

KEY EXPERT WORK EXPERIENCE:

Case:	**Element Capital. vs*. Beijing BOE Display Technology Co., Ltd.***
Jurisdiction:	Civil Action No. 2:22-cv-00118-JRG Eastern District of Texas
Work Product:	Expert consulting work relating to OLED technology. Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration on 3 patents.
Nature of Case:	Civil action.
Counsel:	Retained by Fish & Richardson (Contact: Linhong Zhang)
Date:	4/23 – Current

Case:	**Daedalus Prime LLC vs. *Samsung Electronics Co.,***
Jurisdiction:	Civil Action E.D. TX, Marshall Div., No. 2:22-cv-353 Eastern District of Texas, Marshall Div., and Investigation No. 337-TA-1336
Work Product:	Expert consulting work relating to FINFET process technology. Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration on 2 patents. Source code database viewing (GDS layout and process flow documents) for supporting of non-infringement position.
Nature of Case:	Civil action and ITC Investigation on Certain Semiconductor Devices, Mobile Devices Containing the Same and Components Thereof..
Counsel:	Retained by Fish & Richardson (Contact: Kevin Su)
Date:	10/22 – 4/23

Case:	**Netlist, Inc. vs*. Samsung Electronics Co. Ltd. et al.,***
Jurisdiction:	Civil Action No. 2:21-cv-00463 Eastern District of Texas
Work Product:	Expert consulting work relating to memory modules.
Nature of Case:	Civil action.
Counsel:	Retained by Fish & Richardson (Contact: Tony Nguyen)
Date:	8/22 – Current

Case:	**Vervain, LLC vs. *Micron Technology &* related IPR Petition**
Jurisdiction:	Action No. 6:21-cv-00487-ADA Western District of Texas
Work Product:	Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration on 4 patents, all 4 petitions instituted, and deposed on both initial declaration and reply declaration.
Counsel:	Retained by Orrick, Herrington & Sutcliffe LLP (Contact: Jared Bobrow)
Date:	8/21 – 2/23

Case:	**Monterey Research vs. *Qualcomm* PTAB Matter**
Work Product:	Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel:	Retained by Jones Day (Contact: David Cochran)
Date:	12/21 – Current

Case:	***Semiconductor Energy Laboratory Co.,* OLED Patent Matters**
Jurisdiction:	Action No. 8:21-cv-00554-JAK-ADS Central District of California
Work Product:	Expert for infringement on 3 patents relating to OLED driver circuit and layout, responsibilities include source code viewing, GDS layers viewing, and claim charts review.
Nature of Case:	Civil action.
Counsel:	Retained by Fish & Richardson (Contact: Bryan Basso)
Date:	9/21 – 4/22
Case:	***Apple Inc. IPR Petition for U.S. Patents 6,622,108 & 6,807,505***
Work Product:	Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel:	Retained by Erise IP (Contact: Paul Hart)
Date:	8/21 – 9/21

Case:	***Texas Instruments IPR Petition***
Work Product:	Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel:	Retained by Fish & Richardson (Contact: Josh Griswold)
Date:	9/20 – 4/21

Case:	***Micron Technology* vs. UMC/JinHua**
Jurisdiction:	Case No. 4:17-CV-06932-MMC United States District Court for the Northern District of California
Work Product:	Testifying expert, trade secret documents review, and declaration submission.
Nature of Case:	Trade secret contention of Micron confidential documents.
Counsel:	Retained by Jones Day (Contact: Randy Kay)
Date:	3/17 – Current

Case:	***SK Hynix* vs. BitMicro**
Jurisdiction:	Investigation No. 337-TA-1097 United States International Trade Commission
Work Product:	Testifying expert for non-infringement on 2 patents, issued expert rebuttal report, deposition taken, issued witness statement.
Nature of Case:	ITC infringement case concerning module stacking of SDRAM.
Counsel:	Retained by Fish Richardson (Contact: Joseph Colaianni)
Date:	11/18 – 4/19

Case:	***Rohm Company IPR Petition***
Work Product:	Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel:	Retained by Fish & Richardson (Contact: Matt Colvin)
Date:	4/18 – 8/18

Case:	***Apple Inc.,* vs. Qualcomm Incorporated**
Jurisdiction:	Case No. 3:17-CV-02402 United States District Court for the Southern District of California
Work Product:	Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration, 2 depositions taken.
Counsel:	Fish & Richardson (Contact: Tony Nguyen)
Date:	1/18 – 5/19

Case:	***Macronix* vs. Toshiba**
Jurisdiction:	Investigation No. 337-TA-1046 United States International Trade Commission
Work Product:	Testifying expert for infringement and non-invalidity on 2 patents, claim construction analysis, technical tutorial, database viewing for evidence gathering, issuing expert report and expert rebuttal report, deposition taken for 2 patents, issued witness statement and rebuttal witness statement, testified in ITC court on both infringement and invalidity.
Nature of Case:	ITC infringement case concerning advanced NAND Flash memory.
Counsel:	Retained by Fish Richardson (Contact: David Barken)
Date:	4/17 – 10/18

Case:	***Novatek Microelecronics Corp. IPR Petition***
Work Product:	Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel:	Retained by Kroub, Silbersher & Kolmykov PLLC (Contact: Sergey Kolmykov)
Date:	2/17 – 4/17

Case:	***Taiwan Semiconductor Manufacturing Company IPR Petition***
Work Product:	Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel:	Retained by Fish & Richardson (Contact: John Goetz)
Date:	7/15 – 4/17

Case:	**Triune Systems, LLC vs. *Wayne Chen, et al.,***
Jurisdiction:	Case No. 296-03209-2013, District Court of Collin County, TX
Work Product:	Testifying expert, database viewing, expert report, video-taped testimony
Nature of Case:	Defending against trade secret contention.
Counsel:	Retained by Gordon & Rees LLP (Contact: Robert Bragalone)
Date:	5/15 – 9/15

Case:	***Macronix* vs. Spansion**
Jurisdiction:	Investigation No. 337-TA-922 United States International Trade Commission
Work Product:	Testifying expert, claim construction analysis, technical tutorial, database viewing for evidence gathering, expert report, expert rebuttal report.
Nature of Case:	ITC infringement case concerning Flash memory cell
Counsel:	Retained by Fish Richardson (Contact: David Barken)
Date:	9/14 – 1/15

Case:	***Macronix* vs. Spansion**
Jurisdiction:	Investigation No. 337-TA-909 United States International Trade Commission
Work Product:	Database viewing for evidence gathering, support technical content of expert report, support technical content against rebuttal report.
Nature of Case:	ITC infringement case concerning Flash memory cell
Counsel:	Retained by Winston & Strawn (Contact Michael Murray)
Date:	5/14 – 1/15

Case:	***Keranos, LLC* v. Analog Devices et. al.**
Jurisdiction:	Civil Case No. 2:10-CV-00207 United States District Court for the Eastern District of Texas
Work Product:	Claim Chart Generation and Claim Construction
Nature of Case:	Patent infringement case concerning split gate Flash memory cell
Counsel:	Retained by Agility IP (Contact Michelle Breit)
Date:	2/09 – 2/14

Case:	**Silicon Storage Technology, Inc. v. *Xicor, LLC***
Jurisdiction:	Civil Case No. CV 10-01515 United States District Court for the Northern District of California
Work Product:	Expert report and declarations
Nature of Case:	Matter concerning United States Reissue Patent RE38,370 on the process of flash memory cell.
Counsel:	Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date:	6/11 – 10/11

Case:	***Fast Memory Erase, LLC* v. Spansion et.al.**
Jurisdiction:	Civil Case No. 3:10CV-481 United States District Court for the Northern District of Texas
Work Product:	Declarations
Nature of Case:	Defending Motion for Attorney Fees.
Counsel:	Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date:	2/10 – 6/10

Case:	***Fast Memory Erase, LLC* v. Spansion et.al.**
Jurisdiction:	Civil Case No. 3-08cv0977M United States District Court for the Northern District of Texas
Work Product:	Testifying expert: issuing expert report, declarations, and deposition taken.
Nature of Case:	Patent infringement case concerning minimizing source current during erase of Flash memory cell.
Counsel:	Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date:	2/09 – 5/10

EXPERIENCE:

10/07 to present: **Technical Consultant/Expert Witness**

Serving as a technical consultant and advisor in the area of semiconductor device and process technologies. Expert witness in ITC cases and district court cases, with successful testifying experience in trial hearing. Depositions taken at least 6 times for both litigation cases and IPR petitions. Experienced in source code viewings of circuit schematics and GDS layouts; seasoned in reverse engineering of integrated circuits, as well as techniques for de-processing and analyzing semiconductor chips. Responsibilities including gathering and reviewing of evidence, issuing declaration on claim construction, giving technical tutorial, issuing expert report and expert rebuttal report. Technical consultant for evaluating numerous flash memory and CMOS image sensor patent portfolios for licensing and acquisition consideration. Assessed qualitative merits of each patent portfolio and identified potential infringers and potential licensees. Generated numerous claim charts against potential infringers based on published patents, technical papers and datasheets, and reverse engineering reports.

10/07 to 4/11: **Jonker, LLC**

Inventor and Partner. Developed an intellectual property (IP) portfolio (7 U.S. patents granted and 3 U.S. patent applications pending) on zero-cost CMOS-logic-compatible embedded flash memory. Successfully negotiated the acquisition of this IP portfolio by a major semiconductor company.

8/04 to 10/07: **Maxim Integrated Products, San Jose, California**

Senior Scientist. Responsible for developing embedded non-volatile memory process technology for battery management products. Duties included supervising the development of integrated process flows at the 0.35μm and 0.18μm CMOS technology nodes. Analyzed and solved process-related reliability issues.

5/00 to 8/04: **Xilinx, Incorporated, San Jose, California**
Senior Manager. Responsible for developing non-volatile memory process technology for flash and CPLD products, as well as advanced CMOS process technology (75nm node). Duties included supervising the development of integrated non-volatile memory process flows at multiple CMOS technology nodes to meet product application requirements. Analyzed and solved process-related reliability issues.

2/00 to 5/00 **Progressant Technologies, Fremont, California**
Co-Founder. Facilitated IP development and sale of the company to Synopsys, Inc.

9/98 to 2/00 **Programmable Silicon Solutions, Sunnyvale, California**
Director of Process Engineering. Responsible for developing a fully logic compatible embedded flash memory technology for WSMC (a semiconductor foundry). Developed a new integrated process flow to implement a proprietary flash cell in a high-performance logic process, supervised testchip and product tapeout, process optimization, device optimization, and product yield enhancement. Applied interpersonal skills to align the goals of the foundry technology development group to that of PSS. Participated in the strategic planning of a technology roadmap and foundry strategy for the company.

9/97 to 9/98 **AMIC Technology, Santa Clara, California**
Director of Flash Technology. Responsible for developing 0.35µm ETOX-based flash memory technology. Prepared the business plan and technology roadmap. Developed a new integrated process flow, supervised testchip and product tapeout, process optimization, device optimization, and product yield enhancement.

5/96 to 9/97 **Altera Corp., San Jose, California**
Device Engineering Manager. Responsible for technology development, process integration, and foundry interface for 0.35µm generation of logic and EEPROM programmable logic device technology. Duties included project schedule planning, supervision of testchip and product tapeout, process optimization, and product yield enhancement.

7/95 to 5/96 **Information Storage Devices, San Jose, California**
Technology Development Manager/Program Manager. Led a project team of 10 in technology development, process integration, and first product introduction, with a new foundry. Duties included project schedule planning, supervision of testchip and product tapeout, process optimization, resolution of sorting issues and yield enhancement.

5/92 to 7/95 **Advanced Micro Devices, Sunnyvale, California**

Member of Technical Staff. Led the development of low-energy/DINOR-type flash EPROM technology. Key individual contributor in optimizing the process and design of flash cell and periphery devices in AMD's 0.5μm and 0.35μm flash EPROM technologies. Duties included process integration, device modeling, and development of triple-well technology and high-voltage transistors for negative gate erase operation.

1/89 to 4/92 **Texas Instruments, Dallas, Texas**

Member of Technical Staff. Research and development of 16Mb generation of flash EPROM technology, as well as a new generation of antifuse-based FPGAs. Duties included process integration, device modeling, high-voltage CMOS process integration, and investigation of a novel source-side injection mechanism for EPROM channel hot-electron programming.

AWARDS/HONORS

U.C. Berkeley Certificate of Distinction Award, 1983
AEA Faculty Development Fellowship, 1983-1985
AMD Spotlight Award, 1995

PATENTS

1. U.S. Patent 5,106,773, "Programmable Gate Array and Methods for Its Fabrication" (with K-L. Chen and H. Tigelaar), issued April 21, 1992.

2. U.S. Patent 5,166,557, "Gate Array with Built-in Programmable Circuitry" (with K.-L. Chen), issued November 24, 1992.

3. U.S. Patent 5,202,576, "Asymmetrical Non-Volatile Memory Cell, Arrays, and Methods for Fabricating the Same" (with M. Wong), issued April 13, 1993.

4. U.S. Patent 5,219,782, "Sublithographic Antifuse and method for Manufacturing" (with K.-L. Chen), issued June 15, 1993.

5. U.S. Patent 5,250,464, "Method of Making a Low Capacitance, Low Resistance Sidewall Antifuse Structure" (with M. Wong), issued October 5, 1993.

6. U.S. Patent 5,264,384, "Method of Making a Non-Volatile Memory Cell" (with C. Kaya), issued November 23, 1993.

7. U.S. Patent 5,300,803, "Source Side Injection Non-volatile Memory Cell," issued April 5, 1994.

8. U.S. Patent 5,365,105, "Sidewall Antifuse Structure and Method for Making," issued November 15, 1994.

9. U.S. Patent 5,371,402, "Low Capacitance, Low Resistance Sidewall Antifuse Structure and Process" (with M. Wong), issued December, 1994

10. U.S. Patent 5,395,797, "Antifuse Structure and Method of Fabrication," issued March 7, 1995.

11. U.S. Patent 5,470,773, "Method of Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch" (with Y. Sun and C. Chang), issued November 28, 1995.

12. U.S. Patent 5,482,880, "Non-Volatile Memory and Fabrication Method," (with C. Kaya), issued January 9 1996.

13. U.S. Patent 5,517,443, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch in a Semiconductor Device," issued May 14, 1996.

14. U.S. Patent 5,521,867, "Adjustable Threshold Voltage Conversion Circuit" (with Jian Chen), issued May 28, 1996.

15. U.S. Patent 5,534,455, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch in a Semiconductor Device," issued July 9, 1996.

16. U.S. Patent 5,541,875, "High Energy Buried Layer Implant To Provide A Low Resistance P-Well in A Flash EPROM Array" (with Jian Chen), issued May 28, 1996.

17. U.S. Patent 5,590,076, "Channel Hot-Carrier Page Write," issued December 31, 1996.

18. U.S. Patent 5,596,531, "Method for Decreasing the Discharge Time of A Flash Memory Cell," issued January 21, 1997.

19. U.S. Patent 5,612,914, "Asymmetrical Non-volatile Memory Cell, Arrays and Methods for Fabricating Same" (with Man Wong), issued May 18, 1997.

20. U.S. Patent 5,624,859, "Method for Providing Device Isolation and Off-State Leakage Current for a Semiconductor Device," issued April 29, 1997.

21. U.S. Patent 5,625,220, "Sublithographic Antifuse," (with K.L. Chen), issued April 29, 1997.

22. U.S. Patent 5,646,430, "Non-volatile Memory Cell Having Lightly-Doped Source Region" (with C. Kaya), Issued July 8, 1997.

23. U.S. Patent 5,650,964, "Method of Inhibiting Degradation of Ultra Short Channel Charge-carrying Devices during Discharge," (with Jian Chen), Issued July 22, 1997.

24. U.S. Patent 5,652,155, "Method for Making Semiconductor circuit Including Non-ESD Transistors with Reduced Degradation Due to an Impurity Implant," Issued July 27, 1997.

25. U.S. Patent 5,656,509, "Method and Test Structure for Determining Gouging in a Flash EPROM Cell During SAS Etch," Issued July 29, 1997

26. U.S. Patent 5,661,059, "Boron Penetration to Suppress Short Channel Effect in P-channel Device," Issued August 26, 1997.

27. U.S. Patent 5,674,764, "Method of Making Asymmetrical Non-volatile Memory Cell," Issued October 7, 1997.

28. U.S. Patent 5,693,972, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self-Aligned Source (SAS) Etch in a Semiconductor Device," Issued December 2, 1997.

29. U.S. Patent 5,751,631, "Flash memory cell and a new method for sensing the content of the new memory cell," Issued May 12, 1998

30. U.S. Patent 5,789,295, "Method of Eliminating or Reducing Poly1 Oxidation at Stacked Gate Edge in Flash EPROM Process," Issued August 4, 1998.

31. U.S. Patent 5,814,854, "Highly scalable FLASH EEPROM cell," Issued September 29, 1998.

32. U.S. Patent 5,814,864, "Semiconductor Circuit Including Non-ESD Transistors with Reduced Degradation Due to an Impurity Implant," Issued September 29, 1998.

33. U.S. Patent 5,912,836, "Circuit for Detecting Both Charge Gain and Charge Loss Properties in a Non-Volatile Memory Array," Issued June 15, 1999.

34. U.S. Patent 5,930,174, "Circuit and Method for Erasing Flash Memory Array," Issued July 27, 1999.

35. U.S. Patent 5,981,994, "Method and Semiconductor circuit for Maintaining Integrity of Field Threshold Voltage Requirements," Issued November 9, 1999.

36. U.S. Patent 5,995,418, “Circuit and Method for Erasing Flash Memory Array,” Issued November 30, 1999.

37. U.S. Patent 6,026,017, “Compact nonvolatile memory,” Issued February 15, 2000.

38. U.S. Patent 6,027,974, “Nonvolatile memory,” Issued February 22, 2000.

39. U.S. Patent 6,088,263, “Non-volatile memory using substrate electrons,” Issued July 11, 2000.

40. U.S. Patent 6,091,636, “Flash memory cell and a new method for sensing the content of the new memory cell,” Issued July 18, 2000.

41. U.S. Patent 6,127,225, “Memory cell having implanted region formed between select and sense transistors,” Issued October 3, 2000.

42. U.S. Patent 6,159,800, “Method of forming memory cell,” Issued December 12, 2000.

43. U.S. Patent 6,188,604, “Flash memory cell & array with improved pre-program and erase characteristics,” Issued February 13, 2001.

44. U.S. Patent 6,185,133, “Flash EPROM using junction hot hole injection for erase,” Issued February 6, 2001.

45. U.S. Patent 6,252,799, “Device with embedded Flash and EERPOM memories,” Issued June 26, 2001.

46. U.S. Patent 6,326,265, “Device with Embedded Flash and EPROM Memories,” Issued December 4, 2001.

47. U.S. Patent 6,417,550, “High voltage MOS devices with high gated-diode breakdown voltage and punch-through voltage,” Issued July 9, 2002.

48. U.S. Patent 6,479,862, “Charge trapping device and method for implementing a transistor having a negative differential resistance mode,” Issued November 12, 2002.

49. U.S. Patent 6,512,274, “CMOS-process compatible, tunable NDR (negative differential resistance) device and method of operating same,” Issued January 28, 2003.

50. U.S. Patent 6,596,617, “CMOS compatible process for making a tunable negative differential resistance (NDR) device,” Issued July 22, 2003.

51. U.S. Patent 6,624,026, “Nonvolatile Memory,” Issued September 23, 2003.

52. U.S. Patent 6,680,245, “Method for making both a negative differential resistance (NDR) device and a non-NDR device using a common MOS process,” Issued January 20, 2004.

53. U.S. Patent 6,686,631, “Negative differential resistance (NDR) device and method of operating same,” Issued February 3, 2004.

54. U.S. Patent 6,693,027, “Method for configuring a device to include a negative differential resistance (NDR) characteristic,” Issued February 17, 2004.

55. U.S. Patent 6,700,155, “Charge trapping device and method for implementing a transistor having a configurable threshold,” Issued March 2, 2004.

56. U.S. Patent 6,711,063, "EEPROM memory cell array architecture for substantially eliminating leakage," Issued March 23, 2004.

57. U.S. Patent 6,835,979, "Nonvolatile Memory," Issued December 28, 2004.

58. U.S. Patent 6,969,894, "Variable threshold semiconductor device and method of operating same," Issued November 29, 2005.

59. U.S. Patent 6,972,234, "High Voltage MOS Devices with High Gated-Diode Breakdown Voltage and Punch-through Voltage," Issued December 6, 2005.

60. U.S. Patent 6,972,465, "CMOS process compatible, tunable negative differential resistance (NDR) device and method of operating same," Issued December 6, 2005.

61. U.S. Patent 7,067,873, "Charge Trapping Device," Issued June 27, 2006.

62. U.S. Patent 7,091,077, "Method of directionally trimming polysilicon width," Issued August 15, 2006.

63. U.S. Patent 7,109,078, "CMOS compatible process for making a charge trapping device," Issued September 19, 2006.

64. U.S. Patent 7,301,194, "Shrinkable and highly coupled double poly EEPROM with Inverter," Issued November 27, 2007.

65. U.S. Patent 7,436,710, "EEPROM memory device with cell having NMOS in a P pocket as a control gate, PMOS program/erase transistor, and PMOS access transistor in a common well," Issued October 14, 2008.

66. U.S. Patent 7,535,758, "One or Multiple-Times Programming Device," Issued May 19, 2009.

67. U.S. Patent 7,782,668, "Integrated circuit embedded with Non-volatile One-Time-Programmable and Multiple-Time Programmable memory," Issued August 24, 2010.

68. U.S. Patent 7,787,295, "Integrated circuit embedded with Non-volatile Multiple-Time Programmable memory having variable coupling," Issued August 31, 2010.

69. U.S. Patent 7,787,304, "Method of making integrated circuit embedded with Non-volatile One-Time-Programmable and Multiple-Time Programmable memory," Issued August 31, 2010

70. U.S. Patent 7,787,309, "Method of operating integrated circuit embedded with Non-volatile One-Time Programmable and Multiple-Time Programmable memory," Issued August 31, 2010.

71. U.S. Patent 7,791,955, "Method of erasing a block of memory cells," Issued September 7, 2010.

72. U.S. Patent 7,835,184, "EEPROM memory cell with first-dopant-type control gate transistor, and second-dopant type program/erase and access transistors formed in common well," Issued November 16, 2010

73. U.S. Patent 7,835,186, "Method of programming a selected memory cell," Issued November 16, 2010.

74. U.S. Patent 7,852,672, "Integrated Circuit embedded with Non-Volatile programmable memory having variable coupling," Issued December 14, 2010

75. U.S. Patent 7,876,615, "Method of operating integrated circuit embedded with Non-Volatile programmable memory having variable coupling related application data," Issued January 25, 2011

76. U.S. Patent 7,920,426, "Non-volatile memory programmable through areal capacitive coupling," Issued April 5, 2011

77. U.S. Patent 7,944,750, "Multi-programmable Non-Volatile Memory Cell," Issued May 17, 2011

78. U.S. Patent 8,203,861, "Non-Volatile One-Time Programmable and Multiple-Time Programmable Device," Issued June 19, 2012

79. U.S. Patent 8,208,299, "Integrated Circuit Embedded with Non-Volatile Programmable Memory Having Variable Coupling and Separate Read/Write Paths," Issued June 26, 2012

80. U.S. Patent 8,300,470, "Two Terminal Programmable Hot Channel Electron Non-Volatile Memory," Issued October 30, 2012

81. U.S. Patent 8,305,805, "Common Drain Non-Volatile Multiple-Time Programmable Memory," Issued November 6, 2012

82. U.S. Patent 8,325,519, "Method of Operating Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling Ratio," Issued December 4, 2012.

83. U.S. Patent 8,580,622, "Method of Making Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling," Issued November 12, 2013.

84. U.S. Patent 8,582,342, "Non-Volatile One-Time-Programmable and Multiple-Time Programmable Memory Configuration Circuit," Issued November 12, 2013.

85. U.S. Patent 8,599,612, "Method of Operating Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling Related Application data," Issued December 3, 2013.

86. U.S. Patent 8,705,263, "Non-Volatile One-Time-Programmable and Multiple-Time Programmable Memory Configuration Circuit," Issued April 22, 2014.

87. U.S. Patent 8,988,103, "Capacitively Coupled Logic Gate," Issued March 24, 2015.

88. U.S. Patent 9,064,192, "Automatic Valid Vote Count Storage using Secure Embedded Non-Volatile Memory," Issued June 23, 2015.

89. U.S. Patent 9,224,739, "Method of Making Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling," Issued December 29, 2015.

90. U.S. Patent 9,305,931, "Zero Cost NVM Cell Using High Voltage Devices in Analog Process," Issued April 5, 2016.

91. U.S. Patent 9,324,438, "Method of Operating Incrementally Programmable Non-Volatile Memory," Issued April 26, 2016.

92. U.S. Patent 9,558,813, "Method of Operating Incrementally Programmable Non-Volatile Memory," Issued January 31, 2017.

93. U.S. Patent 9,570,161, "Method of Operating Incrementally Programmable Non-Volatile Memory," Issued February 14, 2017.

94. U.S. Patent 9,570,175, "Incrementally Programmable Non-Volatile Memory," Issued February 14, 2017.

95. U.S. Patent 10,061,738, "Ephemeral Peripheral Device," Issued August 28, 2018.

96. U.S. Patent 10,115,467, "One time Accessible (OTA) Non-Volatile Memory," Issued October 30, 2018.

97. U.S. Patent 10,198,889, "Automatic Valid Vote Count Storage Using Secure Embedded Non-Volatile Memory," Issued February 5, 2019

98. U.S. Patent 10,559,700, "Zero Cost ANVM Cell Using High Voltage Devices in Analog Process," Issued February 11, 2020.

99. U.S. Patent 10,629,607, "Semiconductor CMOS Non-Volatile Memory Device," Issued April 21, 2020

(additional patent applications pending)

PUBLICATIONS

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2. D. K. Y. Liu and J. D. Plummer, "A novel trench-injector power device with low ON-resistance and high switching speed," *IEEE Electron Device Letters*, Vol. 9, No. 7, pp. 321-323, 1988.
3. D. M. Boisvert, D. K. Y. Liu and J. D. Plummer, "Circuit approaches to increasing IGBT switching speed," *IEEE Journal of Solid-State Circuits*, Vol. 23, No. 5, pp. 1276-1279, 1988.
4. D. K. Y. Liu and J. D. Plummer, "Device physics and optimization of conductivity-modulated power MOSFET's," *IEEE Transactions on Electron Devices*, Vol. 35, No. 12, pp. 2457-2458, 1988.
5. D. K. Y. Liu, K.-L. Chen, H. Tigelaar, J. Paterson and S. O. Chen, "Scaled dielectric antifuse structure for field-programmable gate array applications," *IEEE Electron Device Letters*, Vol. 12, No. 4, pp. 151-153, 1991.
6. M. Wong, D. K. Y. Liu, M. M. Moslehi and D. W. Reed, "Preoxidation treatment using HCl/HF vapor," *IEEE Electron Device Letters*, Vol. 12, No. 8, pp. 425-426, 1991.
7. D. K. Y. Liu, C. Kaya, M. Wong, J. Paterson and P. Shah, "Optimization of a source-side injection FAMOS cell for flash EPROM applications," *International Electron Devices Meeting Technical Digest*, pp. 315-318, 1991.
8. K.-L. Chen, D. K. Y. Liu, G. Misium, W. M. Gosney, S.-J. Wang, J. Camp and H. Tigelaar, "A sublithographic antifuse structure for field-programmable gate array applications," *IEEE Electron Device Letters*, Vol. 13, No. 1, pp. 53-55, 1992.
9. K. T. San, C. Kaya, D. K. Y. Liu, T. P. Ma, and P. Shah, "A new technique for determining capacitive coupling coefficients in flash EPROMs," *IEEE Electron Device Letters*, Vol. 13, No. 6, pp. 328-331, 1992.
10. C. Kaya, D. K. Y. Liu, J. Paterson and P. Shah, "Buried source-side injection (BSSI) for flash EPROM programming," *IEEE Electron Device Letters*, Vol. 13, No. 9, pp. 465-467, 1992.
11. M. Wong, D. K. Y. Liu and S. S.-W. Huang, "Analysis of the subthreshold slope and the linear transconductance techniques for the extraction of the capacitance coupling coefficients of floating-gate devices," *IEEE Electron Device Letters*, Vol. 13, No. 11, pp. 566-568, 1992.
12. D. K. Y. Liu and J. D. Plummer, "Design and analysis of a new conductivity-modulated power MOSFET," *IEEE Transactions on Electron Devices*, Vol. 40, No. 2, pp. 428-438, 1993.
13. J. Z. Peng, S. Haddad, H. Fang, C. Chang, S. Longcor, B. Ho, Y. Sun, D. Liu, Y. Tang, J. Hsu, S. Luan, J. Lien, "Flash EPROM endurance simulation using physics-based models," In *International Electron Devices Meeting Technical Digest*, pp. 295-298, 1994.
14. J. Chen, J. Hsu, S. Luan, Y. Tang, D. Liu, S. Haddad, C. Chang, S. Longcor, J. Lien, "Short Channel enhanced degradation during discharge of Flash EEPROM memory Cell," *International Electron Devices Meeting Technical Digest*, pp. 331-334, 1995.

15. V. H. Chan and D. Liu, “An Enhanced Erase Mechanism During Channel Fowler-Nordheim Tunneling in Flash EPROM Memory Devices,” *IEEE Electron Devices Letters,* Vol. 20, No. 3, pp. 140-142, 1999.