

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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**PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT
NO. 6,920,527 PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42**

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EXHIBITS

- MTI-1001 U.S. Patent No. 6,920,527 to Cloutier et al. (“the ’527 patent”)
- MTI-1002 Excerpts from the Prosecution History of the ’527 patent
- MTI-1003 Declaration of David Kuan-Yu Liu, Ph.D.
- MTI-1004 U.S. Patent Application Publication No. 2003/0028733 to Tsunoda et al. (“Tsunoda”)
- MTI-1005 U.S. Patent No. 7,069,370 to Sukegawa et al. (“Sukegawa”)
- MTI-1006 Certified translation and original document of Japanese Published Patent Application No. 2001-005723 to Tomio Suzuki (“Tomio”)
- MTI-1007 Certified translation and original document of Japanese Published Patent Application No. 2000-112836 to Shigeo Suzuki (“Shigeo”)
- MTI-1008 U.S. Patent No. 6,353,870 to Mills et al.
- MTI-1009 U.S. Patent No. 6,539,623 to Chen
- MTI-1010 U.S. Patent No. 6,376,283 to Chen
- MTI-1011 Acrylonitrile Butadiene Styrene (ABS), Dynalabcorp.com, https://web.archive.org/web/20031118100126/http://dynalabcorp.com/technical_info_abs.asp
- MTI-1012 U.S. Patent Publication No. 2002/0010827 to Cheng
- MTI-1013 U.S. Patent Publication No. 2002/0147882 to Pua et al.
- MTI-1014 Plastic Products for UL-94 Flame Class, Polymershapes.com, <https://www.polymershapes.com/regulatory/ul-94-flame-class/>
- MTI-1015 UL 94 Classification and Flame-Retardant Thermoplastics, Protolabs.com, <https://www.protolabs.com/resources/blog/flame-retardant-thermoplastics-and-ul-classifications/>

- MTI-1016 Common DIMM Memory Form Factors, Simmtester.com,
<https://www.simmtester.com/News/PublicationArticle/168>
- MTI-1017 U.S. Patent No. 6,567,273 to Liu et al.
- MTI-1018 U.S. Patent Application Publication No. 2004/0017634 to Chin-Lung
et al.
- MTI-1019 U.S. Patent No. 6,490,163 to Pua et al.
- MTI-1020 U.S. Patent Application Publication No. 2004/0017637 to Chang et al.
- MTI-1021 Complaint For Patent Infringement Against Micron Technology, Inc.
in *Sonrai Memory Ltd. v. Micron Technology, Inc.*, Case No. 6:22-cv-
00855 (W.D. Tex. Aug. 2022)
- MTI-1022 U.S. Patent No. 5,887,145 to Harari et al.
- MTI-1023 Excerpt of Callister, “Materials Science and Engineering, An
Introduction,” Fifth Edition, John Wiley & Sons, Inc. (2000)
- MTI-1024 M.2 SSD, TechTarget.com,
<https://www.techtarget.com/searchstorage/definition/M2-SSD>
- MTI-1025 Interim Procedure for Discretionary Denials in AIA Post-Grant
Proceedings with Parallel District Court Litigation, Katherin K. Vidal
(USPTO June 21, 2022)
- MTI-1026 Stipulation

LISTING OF CHALLENGED CLAIMS

Claim 1	
1[p]	A portable memory apparatus, comprising:
1[a]	a housing;
1[b]	a memory controller comprised in the housing;
1[c]	a volatile memory coupled to said memory controller comprised in the housing;
1[d]	a non-volatile memory coupled to said memory controller comprised in the housing;
1[e]	a connector positioned on the housing, wherein said connector couples said portable memory apparatus to a computer system when said connector is plugged into said computer system; and
1[f]	wherein, when said connector couples said portable memory apparatus to said computer system, said memory controller chip copies data from said non-volatile memory to said volatile memory, and said computer system accesses said data in said volatile memory through said connector.
Claim 2	
2	The portable memory apparatus of claim 1, further comprising an internal power source coupled to said portable memory apparatus.
Claim 3	
3	The portable memory apparatus of claim 2, wherein said internal power source powers said portable memory apparatus when said portable memory apparatus is unplugged from said computer system, said portable memory apparatus copies data from said volatile memory to said non-volatile memory when said portable memory apparatus is unplugged from said computer system.

Claim 4	
4	The portable memory apparatus of claim 2, wherein said internal power source is rechargeable through said connector.
Claim 5	
5	The portable memory apparatus of claim 4, wherein said internal power source comprises a battery or a capacitor.
Claim 6	
6	The portable memory apparatus of claim 1, wherein said memory controller chip transfers said non-volatile memory with data written to said volatile memory from said computer system while said portable memory apparatus is coupled to said computer system.
Claim 7	
7	The portable memory apparatus of claim 6, further comprising an indicator coupled to said portable memory apparatus, wherein said indicator indicates when data stored in said volatile memory is being transferred to said non-volatile memory.
Claim 9	
9	The portable memory apparatus of claim 1, wherein said volatile memory is selected from a group consisting of FPM DRAM, EDO DRAM, SDRAM, RDRAM, and SRAM.
Claim 10	
10	The portable memory apparatus of claim 1, wherein said connection is selected from a group consisting of USB connector, firewire connector, and ATA serial connector.
Claim 11	
11	The portable memory apparatus of claim 1, further comprising an outer impact resistant shell.

Claim 12	
12	The portable memory apparatus of claim 1, wherein said portable memory apparatus does not have any moving parts.
Claim 13	
13	The portable memory apparatus of claim 1, wherein said memory controller chip copies data from said non-volatile memory to said volatile memory after an internal power source has been recharged through said connection, that said internal power source has sufficient power to transfer data from said volatile memory to said non-volatile memory if said portable memory apparatus is unplugged from said computer system before said volatile memory is transferred to said non-volatile memory, wherein, until said internal power source recharges to said sufficient power, said computer system accesses said data on said non-volatile memory through said connector.
Claim 14	
14	The portable memory apparatus of claim 1, wherein said housing comprises a material selected from ABS plastic and polycarbonate.
Claim 15	
15[p]	A method, comprising:
15[a]	coupling a portable memory apparatus to a computer system,
15[b]	wherein said portable memory apparatus comprises a memory controller chip, a non-volatile memory, and a volatile memory;
15[c]	copying data from said non-volatile memory to said volatile memory using said memory controller chip;
15[d]	accessing said data in said volatile memory using said computer system through a connector coupled to said portable memory apparatus and said memory controller chip; and
15[e]	updating said non-volatile memory with data from said volatile memory.

Claim 16	
16	The method of claim 15, further comprising: powering said portable memory apparatus with an internal power source coupled to said portable memory apparatus, when said portable memory apparatus is unplugged from said computer system, to transfer said non-volatile memory with data from said volatile memory.
Claim 17	
17	The method of claim 15, further comprising: recharging an internal power source coupled to said portable memory apparatus.
Claim 18	
18	The method of claim 15, further comprising: indicating when data stored in said volatile memory has been transferred to said non-volatile memory.
Claim 20	
20	The method of claim 15, further comprising: copying said data from said non-volatile memory to said volatile memory after an internal power source has been recharged through said connection, such that said internal power source has sufficient power to transfer data from said volatile memory to said non-volatile memory if said portable memory apparatus is unplugged from said computer system before said volatile memory is transferred to said non-volatile memory, wherein, until said internal power source recharges to said sufficient power, said computer system accesses said data on said non-volatile memory through said connector.

Micron Technology, Inc. (“Petitioner”) petitions for *Inter Partes* Review (“IPR”) of claims 1-7, 9-18, and 20 (“Challenged Claims”) of U.S. Patent No. 6,920,527 (“the ’527 patent”).

I. REQUIREMENTS FOR IPR

A. Grounds for Standing

Petitioner certifies that the ’527 patent is available for IPR. Petitioner is not barred or estopped from requesting this review of the Challenged Claims.

B. Challenge and Relief Requested

Petitioner requests IPR of the Challenged Claims on the grounds below. Dr. Liu provides supporting explanations in his Declaration (MTI-1003) cited throughout this petition.

Ground	Claims	Basis	References
1A	1, 6, 9, 11-12, 14-15	§103	Tsunoda
1B	2-5, 16-17	§103	Tsunoda and Tomio
1C	13, 20	§103	Tsunoda, Tomio, and Shigeo
2A	1, 6-7, 9-12, 14-15, 18	§103	Tsunoda and Sukegawa
2B	2-5, 16-17	§103	Tsunoda, Sukegawa, Tomio
2C	13, 20	§103	Tsunoda, Sukegawa, Tomio, and Shigeo
3A	1-6, 9, 12, 15-17	§103	Tomio
3B	13, 20	§103	Tomio and Shigeo
4A	1-7, 9-12, 14-18	§103	Tomio and Sukegawa
4B	13, 20	§103	Tomio, Sukegawa, and Shigeo

Each reference pre-dates the '527 patent's earliest possible priority date (February 11, 2003; "Critical Date") and qualifies as prior art.

Reference	Date	Prior Art Under
Tsunoda	2/6/2003 (published)	§102(a)
Sukegawa	1/31/2003 (filed)	§102(e)
Tomio	1/12/2001 (published)	§102(b)
Shigeo	4/21/2000 (published)	§102(b)

II. THE '527 PATENT

A. Brief Description

The '527 patent discloses a portable RAM drive in which data is stored on a non-volatile memory and transferrable to a volatile memory when the portable RAM drive is coupled to a computer system for faster access by the computer system. MTI-1001, Abstract; MTI-1003, ¶¶32-33. The portable RAM drive comprises "a housing, a memory controller, a volatile memory, a nonvolatile memory, and a connector to connect the portable RAM drive to the computer system." MTI-1001, 1:42-45. The non-volatile memory stores data when the portable RAM drive is not connected to a computer system, and the data is transferred to the volatile memory when the portable RAM drive is plugged into the computer system for faster access. MTI-1001, 1:45-54. If the portable RAM drive is unplugged from the computer system, an internal power source powers the portable RAM drive long enough to transfer data from the volatile memory (i.e.,

RAM) to the non-volatile memory. MTI-1001, 1:54-58.

B. Summary of the Prosecution History

The claims of the '527 patent were allowed as originally filed. MTI-1002, 46-47; MTI-1003, ¶¶34-35.

C. Level of Ordinary Skill in the Art

A person of ordinary skill in the art (“POSITA”) would have had at least a bachelor of science in electrical engineering, computer engineering, computer science, or a related discipline, with at least two years of relevant experience in a field related to data storage and electronic memory devices. MTI-1003, ¶27. A greater amount of education, e.g., a doctorate in electrical engineering, computer engineering, computer science, or a related discipline, would also qualify for the hypothetical POSITA in lieu of fewer years of work experience. *Id.* Additional education or industry experience may compensate for a deficit in one of the other aspects of the requirements stated above. *Id.*

D. Claim Construction

Claim terms generally should be given their ordinary and customary meaning according to the *Phillips* standard. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R. § 42.100. For purposes of this proceeding only, Petitioner submits that no claim terms require a formal construction for purposes of addressing the Grounds in this Petition. *Wellman, Inc. v. Eastman Chem. Co.*, 642

F.3d 1355, 1361 (Fed. Cir. 2011). Petitioner reserves the right to respond to any constructions offered/adopted by Patent Owner/Board. Furthermore, Petitioner does not concede that each challenged claim satisfies all statutory requirements and does not waive any arguments concerning grounds that can only be raised in district court.

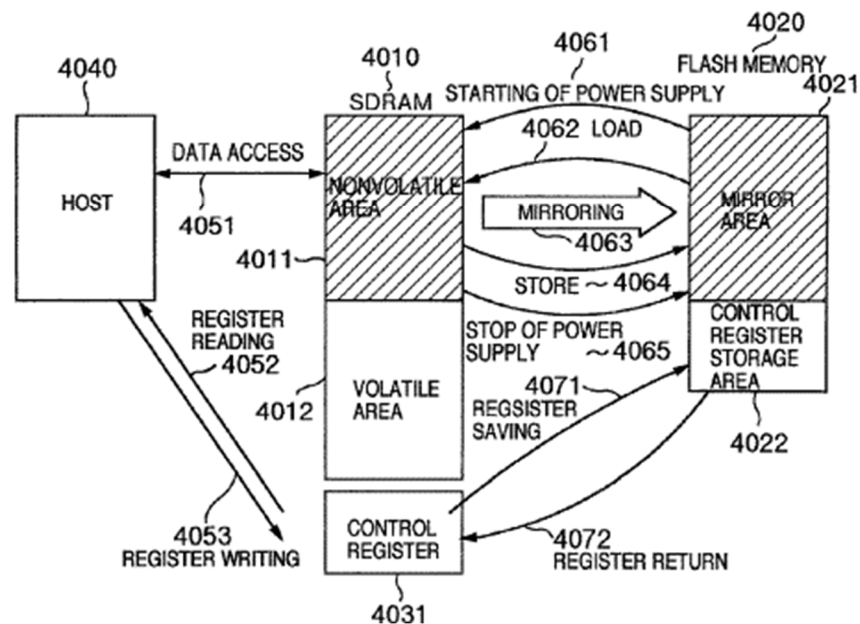
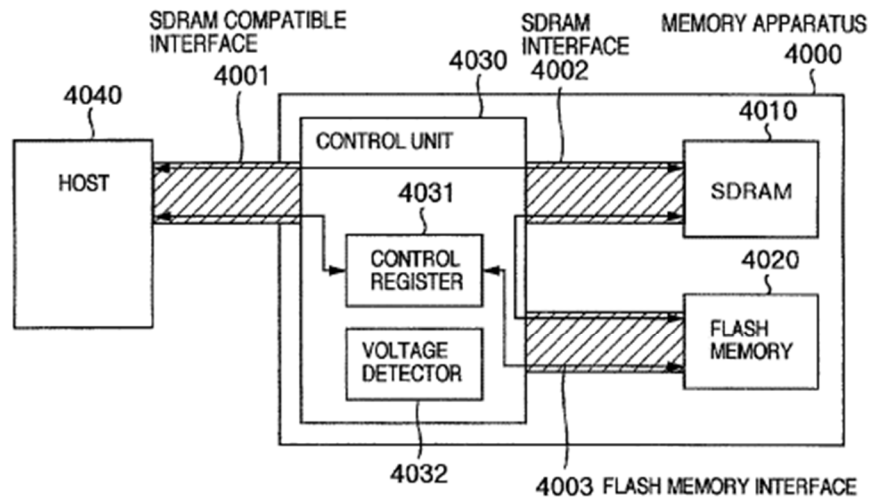
III. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. GROUND 1A—Claims 1, 6, 9, 11-12, and 14-15 are obvious over Tsunoda

1. Overview of Tsunoda

Tsunoda relates to “a memory apparatus, which uses a volatile memory and a nonvolatile memory.” MTI-1004, [0001]; MTI-1003, ¶¶40-49. Tsunoda describes “a configuration example of the memory apparatus” in conjunction with FIG. 24. MTI-1004, [0035]. The memory apparatus 4000 includes “an SDRAM 4010 to be accessed randomly, a flash memory 4020 as a nonvolatile memory, [and] SDRAM compatible interface 4001 for enabling the host 4040 to access the memory apparatus 4000.” MTI-1004, [0042], [0060]-[0061], [0077], [0090]. Tsunoda’s FIG. 24 is an “example of using the SDRAM compatible interface as the interface for interconnecting the memory apparatus 4000 and the host 4040,” but Tsunoda discloses that “other interfaces...can be used.” MTI-1004, [0094].

FIG.24

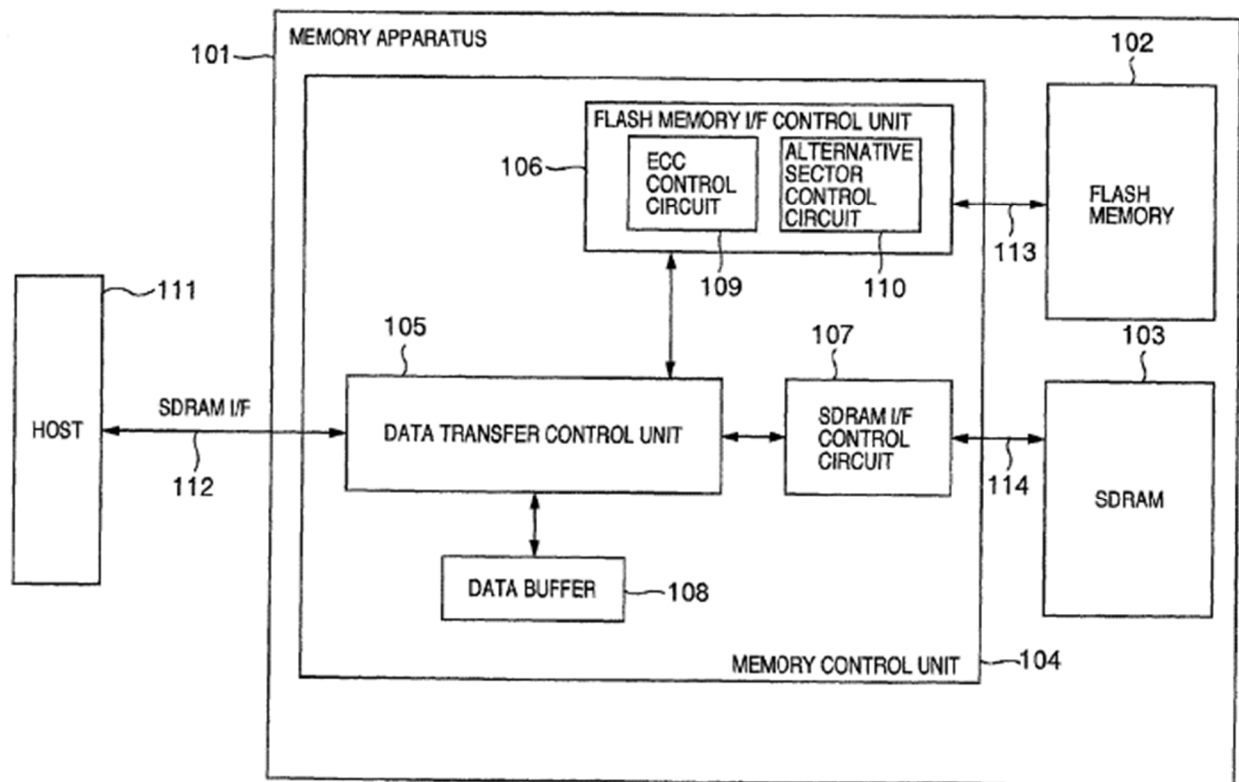


MTI-1004, FIG. 24

In “a more specific embodiment of the memory apparatus 4000” shown in FIG. 1, the “memory apparatus 101 includes a flash memory 102 as a nonvolatile memory, an SDRAM (synchronous SDRAM) 103 as a volatile memory, and a memory control unit 104 for controlling the memories.” MTI-1004, [0096]. “The

memory control unit 104 controls data transfer or the like between a host 111 and the memory apparatus 101, and between the flash memory 102 and the SDRAM 103 in response to a request from the host 111.” *Id.*

FIG.1

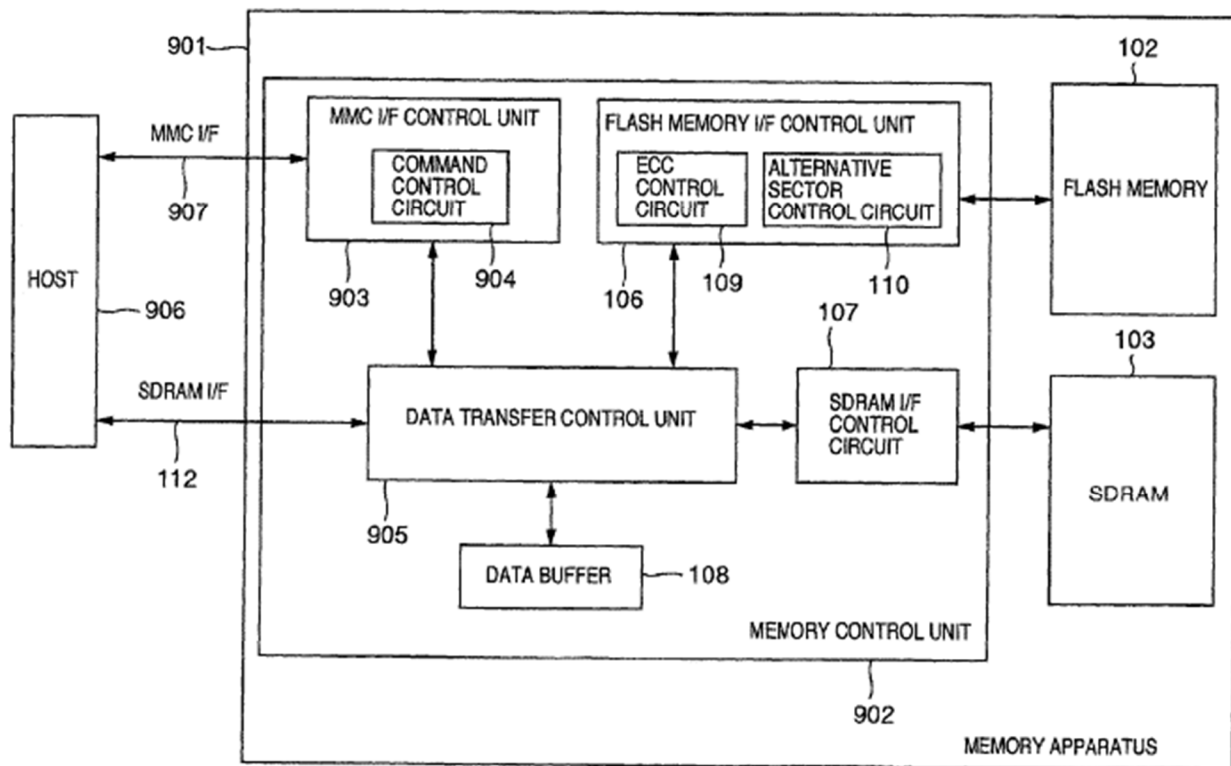


MTI-1004, FIG. 1

In a second embodiment shown in FIG. 9, a “memory apparatus 901 includes a MultiMediaCard (...“MMC”...) interface 907” “as an interface for connection with a host 906, in addition to the SDRAM interface 112 shown in FIG. 1.” MTI-1004, [0113]. “The MMC is a memory card using the flash memory 102 as a storage medium,” and “the memory apparatus 901 includes a function as an MMC in addition to the foregoing data transfer between the memories.” *Id.* In

FIG. 9, “the host 906 including the MMC interface 907 and the SDRAM interface 112 can use the memory apparatus 901 not only as the high-speed volatile and nonvolatile memory but also as the MMC.” MTI-1004, [0120]. Tsunoda’s “invention is not limited to the foregoing MMC interface 907, but it can be applied to various interfaces” such as “interfaces of an SD card (small memory card having a width of 24 mm, a length of 32 mm, and a thickness of 2.1 mm, nine external terminals, and flash memory loaded), and a memory stick.” MTI-1004, [0117].

FIG.9

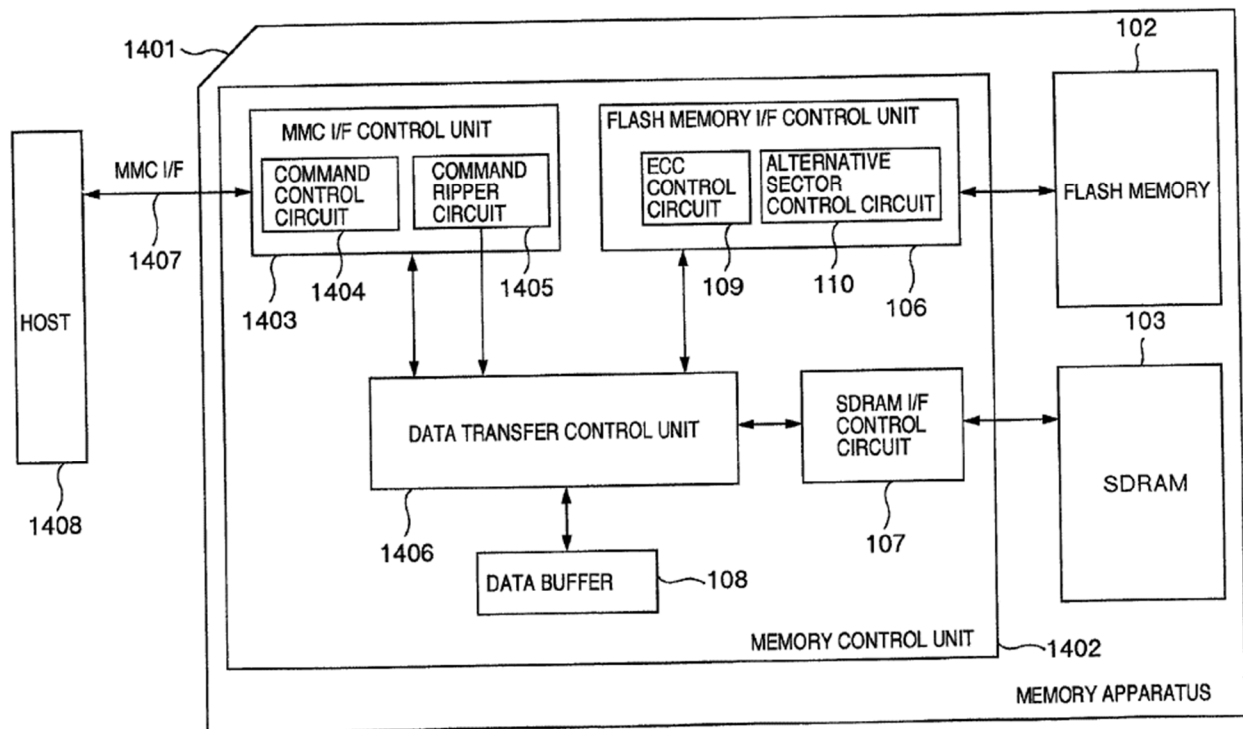


MTI-1004, FIG. 9

In a third embodiment shown in FIG. 14, a “memory apparatus 1401 includes an MMC interface 1407 as an interface with a host 1408” and “is card-

shaped.” MTI-1004, [0121]. As in the FIG. 9 embodiment, the memory apparatus 1401 “can be used not only as the MMC function but also as a high-speed volatile or nonvolatile memory.” MTI-1004, [0120], [0123].

FIG.14



MTI-1004, FIG. 14

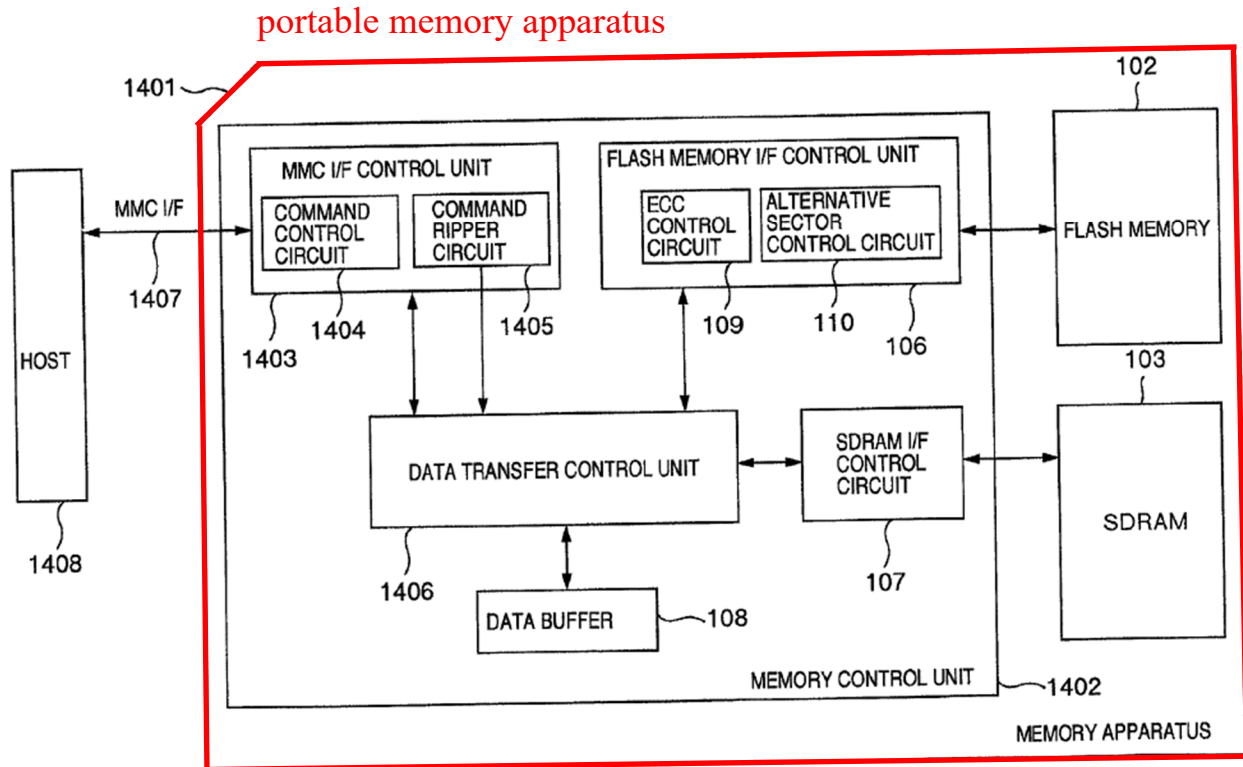
2. Claim 1

(a) Element 1[p]

Tsunoda’s memory apparatus 101 (FIG. 1) and 1401 (FIG. 14) “can be applied to any shapes,” such as “a LSI, in which memory chips and a control chip are sealed in one package,” and the “components may be housed in a memory card shape such as an MMC.” MTI-1004, [0124]. Tsunoda FIG. 14 shows such “a

memory apparatus 1401” “in a memory card shape such as an MMC.” MTI-1004, [0121], [0124]. “The MMC is a memory card using the flash memory 102 as a storage medium.” MTI-1004, [0113]. A POSITA would have found it obvious that Tsunoda’s MMC 1401 is a portable memory apparatus having a form factor that can be mounted on a portable information terminal and beneficially allows the contents of the MMC to be transferred easily between computer systems. MTI-1003, ¶¶50-52; MTI-1004, [0038], [0096], [0117]; MTI-1008, 2:1-20, FIGS. 2A, 3A, 6A (below), 6B (below); MTI-1013, [0004], [0006].

FIG.14



MTI-1004, FIG. 14¹

¹ Annotations and color added unless otherwise noted.

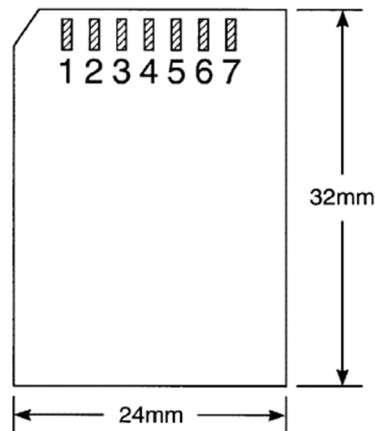


FIG. 6A

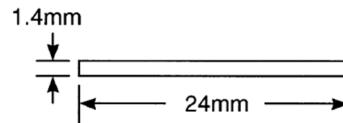


FIG. 6B

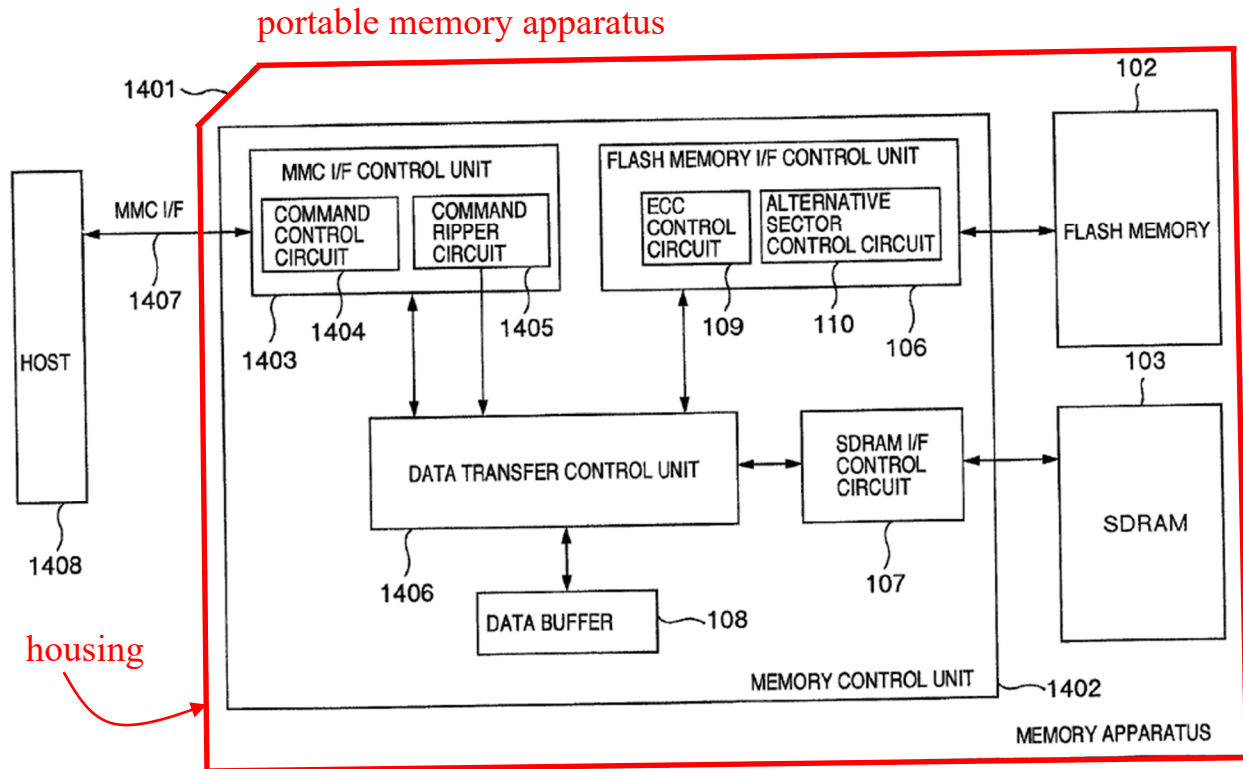
MTI-1008, FIGS. 6A (partial), 6B (partial)

(b) Element 1[a]

Tsunoda illustrates and describes “an internal configuration” for each memory apparatus of FIGS. 1, 9 and 14. MTI-1004, [0096], [0012], [0020], [0025], [0115], [0121]. Specifically, Tsunoda’s FIG. 14 shows “an internal configuration” of the MMC 1401. MTI-1004, [0025], [0121]. In Tsunoda, MMC 1401 “may be a LSI, in which memory chips and a control chip are sealed in one package” and “may be housed in a memory card shape such as an MMC.” MTI-1004, [0124], [0056] (LSI package form where SDRAM, flash memory, and control unit are “on different silicon chips... providing a multichip package, in which the components are sealed in one package.”). A POSITA would have found it obvious that Tsunoda’s MMC 1401 has a housing in the form of a shell that encapsulates and protects the memory chips and control chip of the MMC to allow

the MMC 1401 to be portable. MTI-1003, ¶¶53-56; MTI-1008, 2:1-20, FIGS. 2A, 3A (showing the “MultiMediaCard form factor” and “internal architecture”); MTI-1009, 1:24-27 (“shell”); MTI-1010, 1:22-24 (“card body”).

FIG.14



MTI-1004, FIG. 14

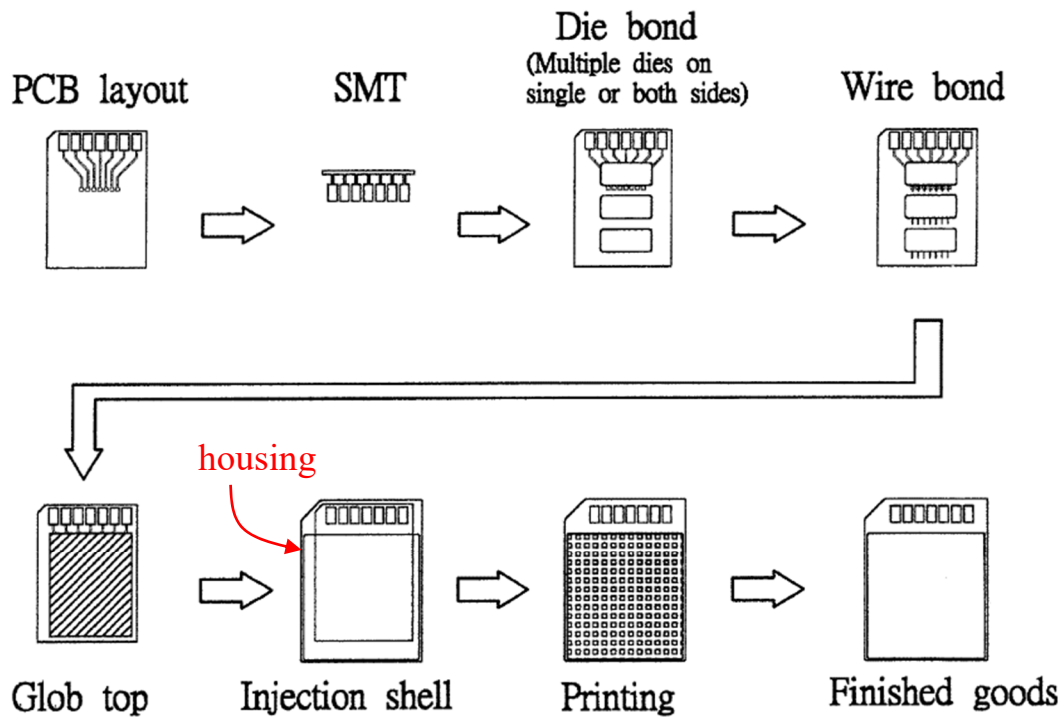
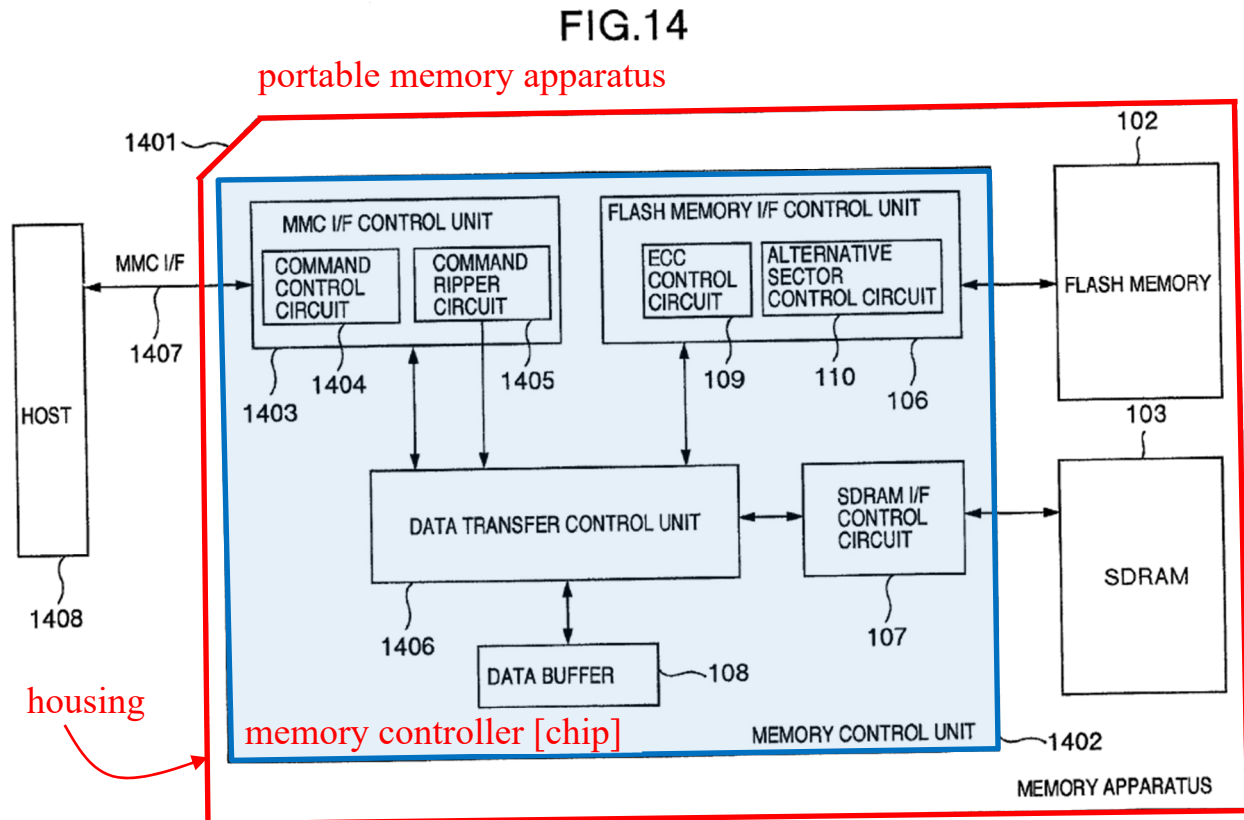


FIG.2
MTI-1009, FIG. 2

(c) Element 1[b]

Tsunoda's MMC 1401 internal configuration within the housing includes "a memory control unit 1402" for controlling the memories and data transfers. MTI-1004, [0121]-[0122] ("as in the case of previous embodiments"), [0054], [0062], [0068], [0096]-[0099], [0104]-[0105], [0115], [0131], [0133]-[0140], FIGS. 1, 9, 14, 18, 20-24. Tsunoda discloses that MMC 1401 "may be a LSI, in which memory chips and a control chip are sealed in one package" and "may be housed in a memory card shape such as an MMC." MTI-1004, [0124], [0056] (LSI package form where SDRAM, flash memory, and control unit are "on different

silicon chips... providing a multichip package, in which the components are sealed in one package.”). Tsunoda’s FIG. 14 shows the memory control unit 1402 (memory controller [chip]) (blue) in the housing (outlined red) of the MMC 1401. MTI-1003, ¶¶57-60.



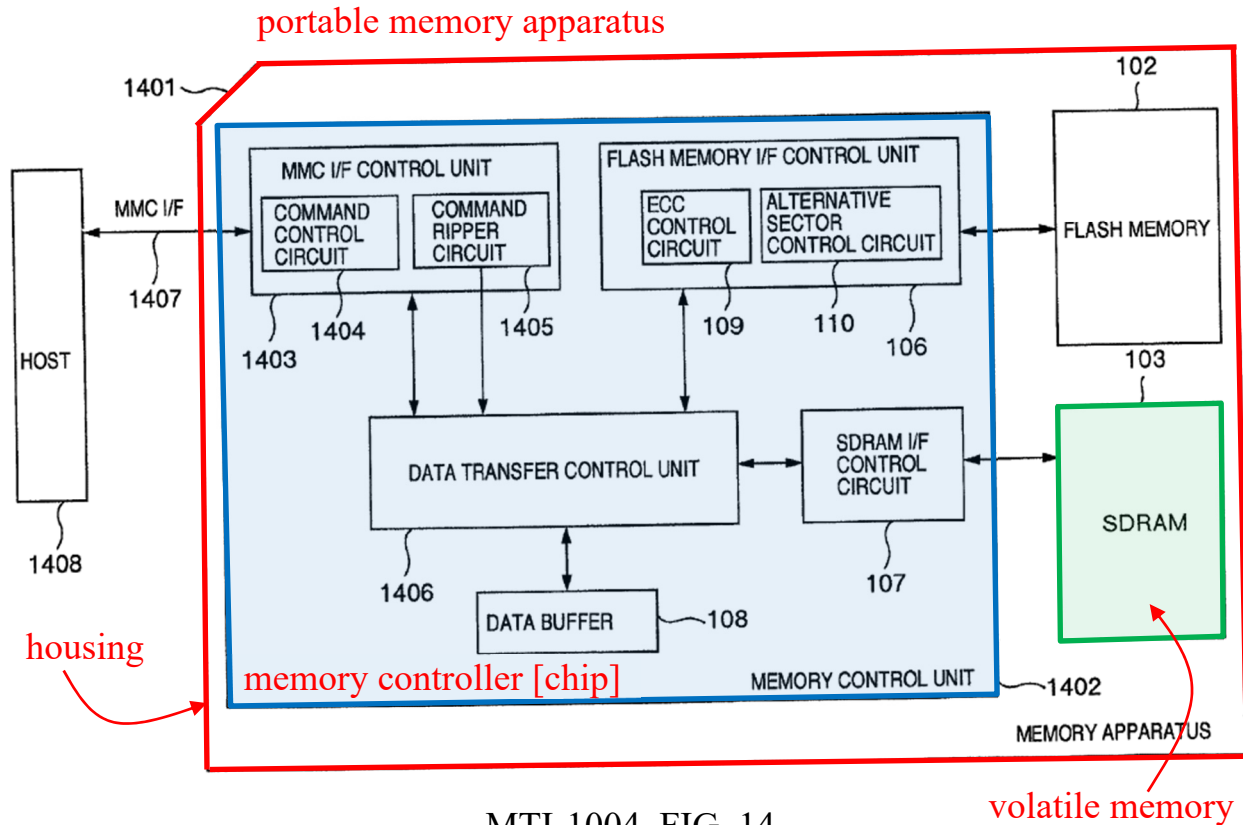
MTI-1004, FIG. 14

(d) Element 1[c]

The Tsunoda MMC 1401 internal configuration within the housing includes “a volatile memory,” e.g., “SDRAM 103,” that “can be accessed from the memory control unit 1402.” MTI-1004, [0122], [0096] (“an SDRAM (synchronous SDRAM) 103 as a volatile memory”), [0097]-[0099], [0001], [0035], [0042],

[0054] (“SDRAM 4010 and the control unit 4030 are connected to each other”), [0060], [0062], [0068], [0075], [0094], [0104]-[0105], [0124], [0131], [0133]-[0140], FIGS. 1, 9, 14, 18, 20-24. Tsunoda teaches that MMC 1401 “may be a LSI” that includes SDRAM, flash memory, and a control unit “on different silicon chips, and interconnects terminals of the silicon chips by, for example wire bonding, thereby providing a multichip package, in which the components are sealed in one package.” MTI-1004, [0056], [0124]. Tsunoda’s FIG. 14 shows the SDRAM 103 (volatile memory) (green) coupled to the memory control unit 1402 (memory controller) (blue) in the housing (outlined red) of the MMC 1401. MTI-1003, ¶¶61-64.

FIG.14

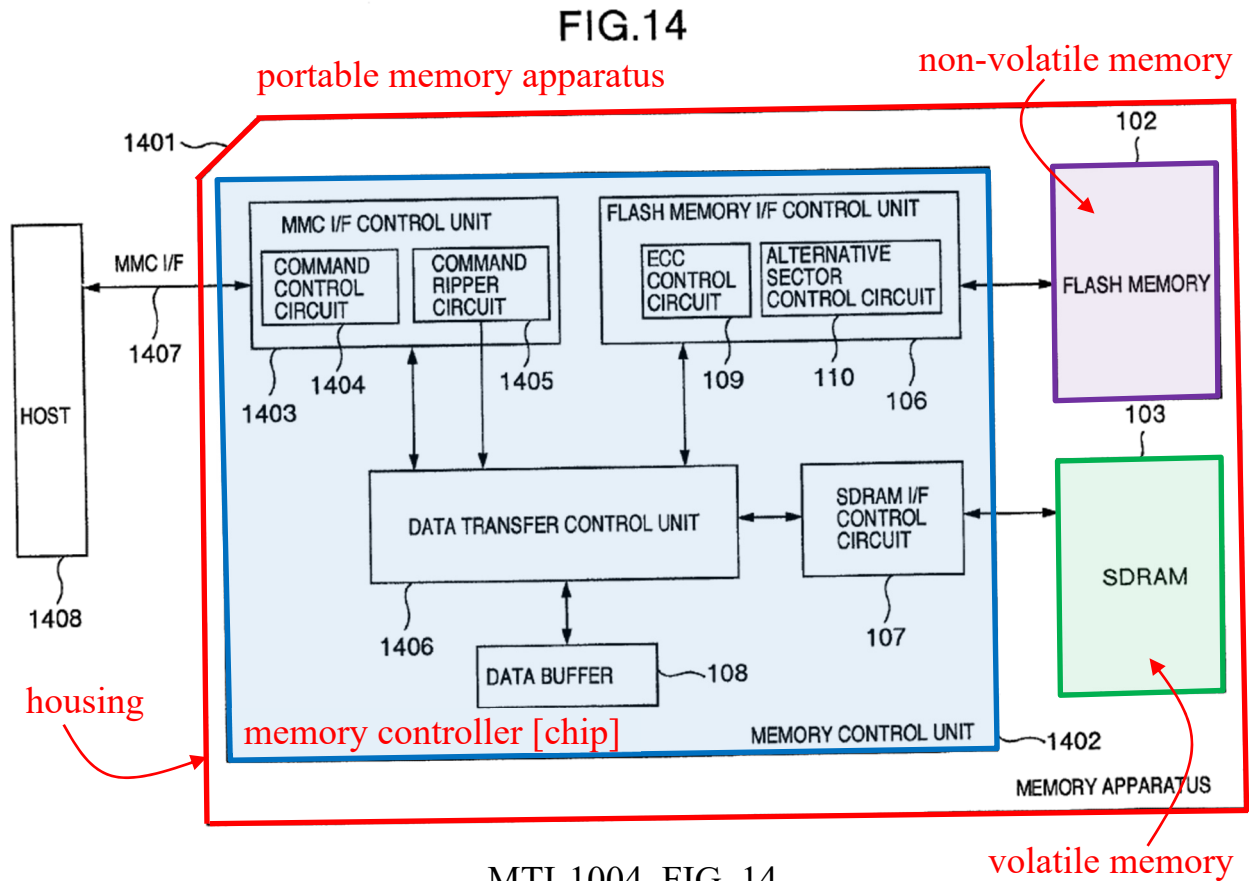


MTI-1004, FIG. 14

(e) Element 1[d]

The Tsunoda MMC 1401 internal configuration within the housing includes “a nonvolatile memory,” e.g., “flash memory 102,” that is controlled by memory control unit 1402. MTI-1004, [0122], [0096] (“a flash memory 102 as a nonvolatile memory”), [0097]-[0099], [0001], [0035], [0042], [0054]-[0055] (“control unit 4030 and the flash memory 4020 are connected to each other”), [0061]-[0062], [0068], [0094], [0104]-[0105], [0124], [0131]-[0140], FIGS. 1, 9, 14, 18, 20-24. Tsunoda teaches that MMC 1401 “may be a LSI” that includes SDRAM, flash memory, and a control unit “on different silicon chips, and

interconnects terminals of the silicon chips by, for example wire bonding, thereby providing a multichip package, in which the components are sealed in one package.” MTI-1004, [0056], [0124]. Tsunoda’s FIG. 14 shows the flash memory 102 (non-volatile memory) (purple) coupled to the memory control unit 1402 (memory controller) (blue) in the housing (outlined red) of the MMC 1401. MTI-1003, ¶¶65-68.

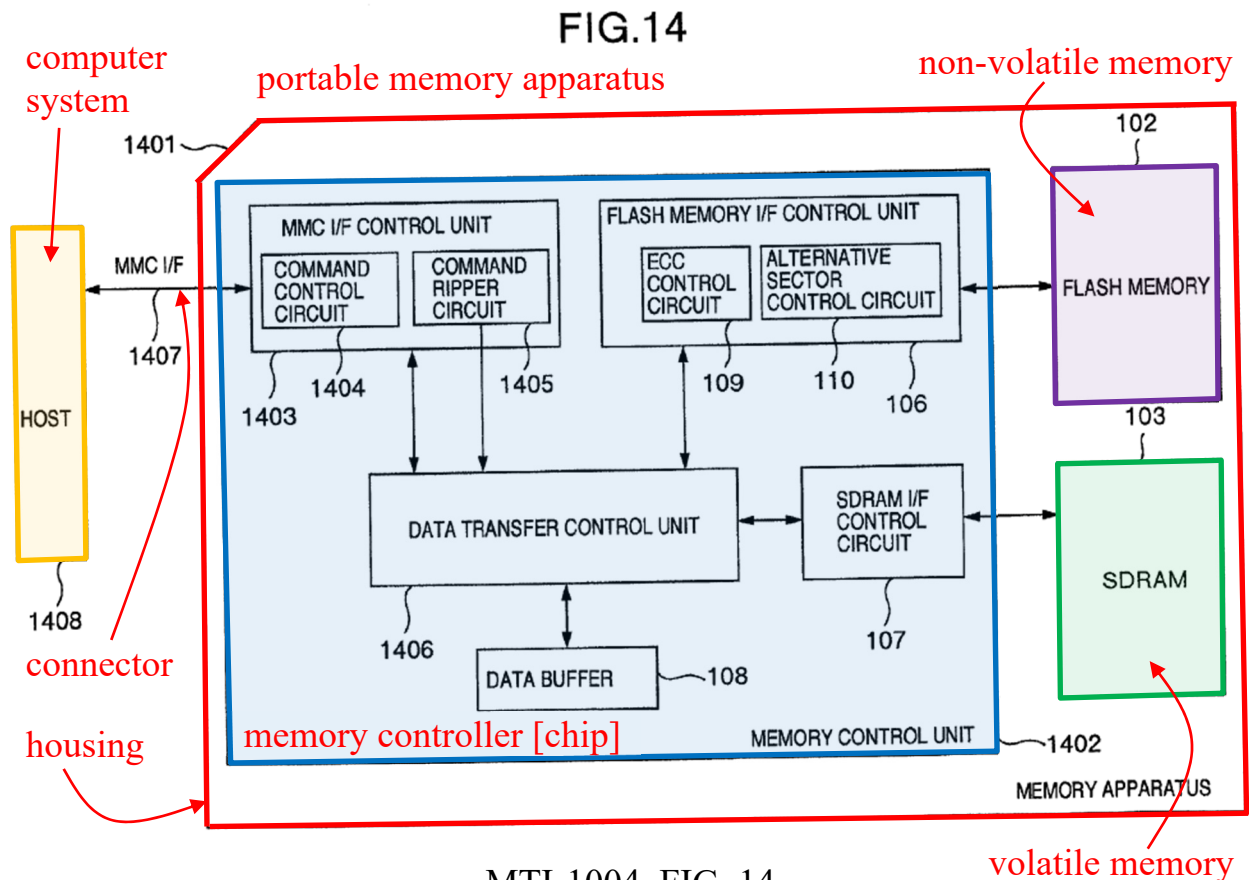


MTI-1004, FIG. 14

(f) Element 1[e]

From Tsunoda’s description of FIGS. 1 and 24, a POSITA would have found it obvious that Tsunoda’s MMC 1401 “can be mounted on an information

terminal such as a portable telephone set, personal digital assistants (PDA), a music player, a digital camera, a digital video camera, a set top box, a personal computer, or a car navigation system,” and the host “is an information processor such as a CPU or ASIC incorporated in the information terminal” that enables the information terminal to access the contents of the MMC. MTI-1004, [0038], [0035], [0040], [0096]; MTI-1003, ¶69. MMC 1401 “includes an MMC interface 1407 as an interface with a host 1408,” and “connection with the host 1408 is made... through the MMC interface 1407.” MTI-1004, [0121]-[0123], [0042]-[0043], [0054]-[0055], [0060], [0077], [0090].



MTI-1004, FIG. 14

The MMC interface 1407 includes “seven terminals,” as shown below, for connecting to and communicating with the host. MTI-1004, [0114]-[0115], [0009]; MTI-1003, ¶70; MTI-1008, 2:1-20, 4:3-17 (describing a host interface device with “an internal connector for accepting a MultiMediaCard”); FIGS. 2A, 2B, 3A. A POSITA would have found it obvious that the seven terminals of the MMC interface 1407 are positioned on the housing², as shown below, and are,

² The prior art’s disclosure of a connector “positioned on the housing” is

individually or collectively, a connector that couples the MMC 1401 (portable memory apparatus) to the host (computer system) to enable the host to access the contents of the MMC when the MMC 1401, and thus the connector, is plugged into the host. *Id.*

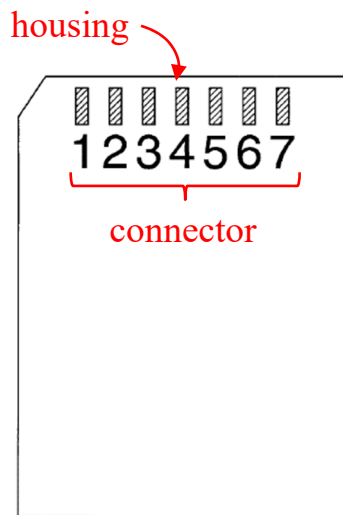


FIG. 2A

MTI-1008, FIG. 2A (partial)

(g) Element 1[f]

While Tsunoda describes various features in the context of FIGS. 1 and 24, a POSITA would have found it obvious to apply any of Tsunoda's features to the FIGS. 9, 10, and 14 embodiments. MTI-1004, [0035]; MTI-1003, ¶¶71-73. For example, a POSITA would have found it obvious that the MMC 1401 of FIG. 14

commensurate in scope with the '527 patent's description of this limitation. MTI-1001, 1:42-45, 2:36-37, 2:44-54, 2:57-61, 3:48-52.

also stores “various data such as a text, an image, a voice, a moving image and the like, or operation parameters/setting files of the programs” or “[o]ther data.” MTI-1004, [0041], MTI-1003, ¶73. The MMC interface 1407 of the MMC 1401 includes “a command terminal (CMD) 1002” used by the host “to transmit a memory card command” and “a power supply terminal (VCC 1) 1004 from the host,” as described with respect to FIG. 10. MTI-1004, [0114]. Additionally, a POSITA would have found it obvious for the memory control unit 1402 (memory controller chip) to copy the data held in the flash memory 102 (non-volatile memory) to the SDRAM 103 (volatile memory), when the MMC interface 1407 (connector) couples the MMC 1401 (portable memory apparatus) and the host 1408 (computer system), and the host 1408 starts supplying power to the MMC 1401 through the power supply terminal 1004 of the MMC interface 1407 or when the host 1408 issues a request to copy data from the flash memory 102 to the SDRAM 103 through the command terminal 1002 of the MMC interface 1407. MTI-1004, [0042]-[0043], [0048]-[0049], [0062], [0068], [0078], [0080]-[0084], [0093], [0096], [0099], [0104], [0131], [0139]-[0140], FIGS. 18, 23, FIG. 24 (4061-4062), FIG. 25 (4101-4105), FIG. 26 (4206); MTI-1003, ¶73. A POSITA would have been motivated to do so for several reasons, including to beneficially allow the host 1408 to control data transfer between the flash memory 102 and the SDRAM 103 (MTI-1004, [0004]-[0005]), use the MMC 1401 as a nonvolatile

SDRAM compatible memory (MTI-1004, [0042]), and access data on the MMC 1401 via SDRAM 103 at a high speed (MTI-1004, [0112]). MTI-1003, ¶73.

For Tsunoda's MMC 1401, "connection with the host 1408 is made not through the SDRAM interface 112, but only through the MMC interface 1407," and "access to the SDRAM 103 from the host[]" is "carried out through the MMC interface 1407." MTI-1004, [0121]-[0123], [0009], [0039], [0042], [0060], [0062], [0075], [0077], [0090]-[0092], [0094], [0099], [0133]-[0134], FIGS. 20 (2001-2003), 24 (4051), 26 (4201). The MMC interface 1407 includes a "data (DAT) 1007" terminal, which "is an input-output terminal used by the host [1408] to transmit[] input data of a form compliant with memory card interface specifications to the memory apparatus [1401], or receive output data of a form compliant with the same specifications from the memory apparatus [1401]," through which "the host [1408] transmits/receives... host data." MTI-1004, [0114]. Because Tsunoda's MMC 1401 connects with the host 1408 only through the MMC interface 1407 (and not through an SDRAM interface), when the MMC interface 1407 (connector) couples the MMC 1401 (portable memory apparatus) to the host (computer system), the host accesses the data in the SDRAM 103 (volatile memory) through the data terminal 1007 of the MMC interface 1407. *Id.*; MTI-1003, ¶74.

3. Claim 6³

If the Board construes “transfers said non-volatile memory with data written to said volatile memory from said computer system” to mean “transfers *to* said non-volatile memory data written to said volatile memory from said computer system” (*i.e.*, the italicized “to” should be inserted and “with” should be deleted), Tsunoda renders this obvious. MTI-1003, ¶¶75-76.

³ Petitioner does not concede that this claim is not indefinite and reserves the right to argue indefiniteness in other proceedings where such arguments are permitted. Because Petitioner is unable to raise indefiniteness here, Petitioner applies prior art to the possible constructions of the claim language. *Samsung Electronics Co. LTD., et al. v. Seven Networks, LLC*, IPR2018-01124, Paper 29, 17 (PTAB Jan. 2019) (“Petitioner’s argument about indefiniteness in the related district court case does not warrant denying the Petition because Petitioner cannot raise indefiniteness in this case.”). Notably, when determining validity, “claim terms need only be construed to the extent necessary to resolve the controversy.” *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011). Here, the prior art discloses these features consistent with embodiments described in the ’527 patent, and validity can be resolved. Petitioner will promptly inform the Board of any district court developments related to definiteness of the claims.

While Tsunoda describes various features in the context of FIGS. 1 and 24, a POSITA would have found it obvious to apply any of Tsunoda's features to the FIGS. 9, 10, and 14 embodiments. MTI-1003, ¶¶76-78. For example, a POSITA would have found it obvious for the memory control unit 1402 (memory controller chip) to transfer to the flash memory 102 (non-volatile memory) data written to the SDRAM 103 (volatile memory) from the host 1408 (computer system) while the host 1408 is coupled to the MMC 1401. MTI-1004, [0035], [0042]-[0043], [0046]-[0047], [0062], [0068], [0078], [0085]-[0088], [0093], [0098]-[0099], [0104], [0112], [0133]-[0138], FIGS. 20-22, 24 (4063-4065), 25 (4107, 4109-4113), 26 (4206); MTI-1003, ¶78. A POSITA would have been motivated to do so for several reasons, including to update any changes or additions to user data to the flash memory, to prevent a data loss of the SDRAM 103 caused by a stop of the power supply, and to hold the data even after the power is turned off. MTI-1004, [0042], [0112]; MTI-1003, ¶78.

If the Board construes "transfers said non-volatile memory with data written to said volatile memory from said computer system" to mean "transfers *from* said non-volatile memory data written to said volatile memory from said computer system" or "transfers data *from* the non-volatile memory *to* the volatile memory so that it can be accessed by the host computer," Tsunoda renders this obvious for the reasons discussed above for 1[f]. MTI-1003, ¶79.

4. Claim 9

Supra 1[c]. MTI-1003, ¶80.

5. Claims 11 and 14

As discussed in 1[a], Tsunoda's MMC 1401 has a housing in the form of a shell that encapsulates the memory chips and control chips of the MMC. MTI-1003, ¶81; MTI-1008, 2:1-20, FIGS. 2A, 3A (showing the "MultiMediaCard form factor" and "internal architecture"); *see generally* MTI-1009 and MTI-1010 (describing general MMC fabrication and known use of ABS (acrylonitrile-butadiene-styrene) for forming the encapsulating shell of MMCs). A POSITA would have found it an obvious design choice, based on a POSITA's general knowledge, to use ABS (acrylonitrile-butadiene-styrene), which is a plastic that possesses outstanding impact strength, to form an outer rigid impact resistant plastic shell housing to protect the components of Tsunoda's MMC from damage due to mishandling, moisture, dust and debris, and electrostatic discharge. MTI-1003, ¶¶81-82; MTI-1009, 1:25-27 ("the shell is separately injection-molded from... ABS (acrylonitrile-butadiene-styrene)"); MTI-1010, 1:21-24 ("ABS (acrylonitrile-butadiene-styrene) card body preparation"); MTI-1011 ("ABS possesses outstanding impact strength" and is "impact resistant"); MTI-1023, 10.

6. Claim 12

As previously discussed, Tsunoda's memory apparatus 4000 can be "an LSI

package form” and includes “the SDRAM 4010, the flash memory 4020, and the control unit 4030 on different silicon chips, and interconnects terminals of the silicon chips by, for example wire bonding, thereby providing a multichip package, in which the components are sealed in one package.” MTI-1004, [0056], [0124].

A POSITA would have found it obvious that MMC 1401, which includes the SDRAM 103, flash memory 102, and memory control unit 1402 on different silicon chips housed “in a memory card shape such as an MMC,” as shown below, does not have any moving parts so as to provide a compact portable data storage device. MTI-1004, [0124]; MTI-1003, ¶¶83-84; MTI-1008, FIGS. 6A (below), 6B (below); MTI-1009; MTI-1010; MTI-1012, [0005] (“a portable data storage device comprising a coupling device with an interface device, memory control device and a non-volatile solid-state memory device it is possible to provide a portable data storage device... which does not include moving parts....”), [0031] (“the device 10 has no moving parts” so as “to be more compact than conventional portable data storage devices.”).

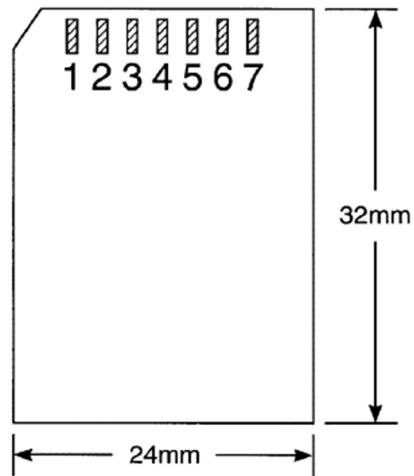


FIG. 6A

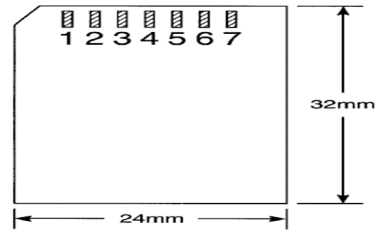


FIG. 6A

MTI-1008, FIGS. 6A (partial), 6B (partial)

7. Claim 15

(a) Element 15[p]

Tsunoda teaches a method as set forth below. MTI-1003, ¶85.

(b) Element 15[a]

Supra 1[p] and 1[e]. MTI-1003, ¶86.

(c) Element 15[b]

Supra 1[b]-1[d]. MTI-1003, ¶87.

(d) Element 15[c]

Supra 1[f]. MTI-1003, ¶88.

(e) Element 15[d]

Supra 1[f]. MTI-1003, ¶89.

(f) Element 15[e]

Supra claim 6. MTI-1003, ¶¶90.

B. GROUND 2A—Claims 1, 6-7, 9-12, 14-15, and 18 are obvious over Tsunoda and Sukegawa

1. Overview of Sukegawa

Sukegawa relates to a “USB memory storage apparatus that uses an integrated semiconductor device incorporated within a USB connector shield case.” MTI-1005, 1:8-11; MTI-1003, ¶¶92-94. Sukegawa’s FIG. 1 shows a “USB memory apparatus 100.” MTI-1005, 4:44-48.

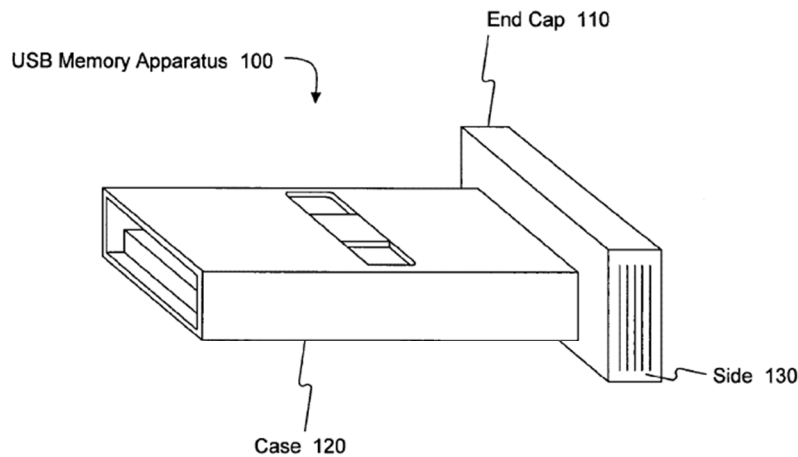


FIG. 1

MTI-1005, FIG. 1

In Sukegawa, “[t]he circuit components of the flash drive apparatus can be mounted within case 120 in various configurations.” MTI-1005, 4:48-50, 8:6-9:16,

FIGS. 5A-5H. “A set of contact terminals (shown in more detail in FIG. 4A-C) is disposed within the connector shield case 120 is in a known configuration to line up with a mating USB connector.” MTI-1005, 4:54-57, 7:26-52. “Attached to the USB connector shield case 120 is an end cap 110” that “may have an opening to expose one or more lights that indicate connection to the host system, access to the apparatus memory or both.” MTI-1005, 4:58-59, 4:67-5:2, 5:16-20, 6:21-31.

2. Tsunoda-Sukegawa Combination

As discussed above, Tsunoda’s memory apparatus 101, 901, and 1401 “can be applied to any shapes,” such as “a LSI, in which memory chips and a control chip are sealed in one package,” and the “components may be housed in a memory card shape such as an MMC.” MTI-1004, [0124], [0056]. Regarding the memory card shape described in Tsunoda, others in the field have recognized that “when moving the flash memory card between devices, an additional host or adapter is required in order for the host to communicate with the flash card” and thus “there is a need for a flash memory device that can be directly connected to a host device without the need for special cables or adapters.” MTI-1013, [0006]-[0008]. This is achieved by “a flash memory storage device that is connectable to a host via a universal serial bus” (USB). MTI-1013, [0009]. Those in the field have recognized that a USB flash storage device has advantages over a conventional flash memory card in that it offers “a standard serial interface which allows data to

be stored in and read from an external memory device at high speed” and “permits the host and flash memory device to connect and interact with ease.”

MTI-1013, [0009]-[0010]; MTI-1005, 1:13-44; MTI-1017, 1:7-17, 1:39-2:10. A POSITA would have been motivated to apply the teachings of Sukegawa to Tsunoda’s memory apparatus to provide a memory apparatus that connects to a host via a USB connector to achieve these advantages. MTI-1005, 1:19-24; MTI-1013, [0006]-[0010]; MTI-1003, ¶95.

Tsunoda expressly contemplates that its memory apparatus can use interfaces other than a SDRAM compatible interface or a MMC interface for connecting the memory apparatus and the host, and “can be applied to any shapes” other than “a memory card shape.” MTI-1004, [0094], [0117], [0124], [0056]. A POSITA implementing Tsunoda’s memory apparatus would have turned to examples of similar memory apparatus to identify suitable interfaces and shapes. MTI-1003, ¶96.

Sukegawa provides a suitable interface and shape for a flash memory apparatus. MTI-1003, ¶97. Sukegawa discloses that a flash memory device, such as Tsunoda’s memory apparatus, can be implemented as a “USB flash drive apparatus” that “interfaces with a host system through a USB connector.” MTI-1005, 1:38-40, 4:35-38. Sukegawa’s teachings enable implementation of a memory apparatus, such as that described in Tsunoda, as a USB flash drive apparatus.

MTI-1003, ¶97; MTI-1005, 4:48-50, 8:6-9:16, FIGS. 5A-5H. A POSITA would have been motivated to apply the teachings of Sukegawa to Tsunoda's memory apparatus to beneficially provide a USB flash drive apparatus having "additional bandwidth for multimedia and storage applications" and offering "Plug-and-Play capability" between different devices or computers without the need for special cables or adapters. MTI-1003, ¶97; MTI-1005, 1:27-30; MTI-1013, [0006]-[0008]; MTI-1017, 1:7-17, 1:39-2:10.

Sukegawa also provides that the USB flash drive apparatus includes "one or more lights that indicate connection to the host system, access to the apparatus memory or both." MTI-1005, 4:67-5:2, 5:16-20, 6:21-31. These additional teachings of Sukegawa would further motivate a POSITA to implement a flash memory device, such as Tsunoda's memory apparatus, as a USB flash drive apparatus with indicator lights. MTI-1003, ¶98. A POSITA would have found it obvious that removing a memory apparatus during data transfers is not desirable and would have been motivated to add an indicator light to advantageously provide the user with a visual indication that the USB flash drive apparatus is transferring data to at least discourage removal of the memory card from a host system during a memory transfer. *Id.*; MTI-1005, 4:67-5:2, 5:16-20, 6:21-31; MTI-1013, [0016], [0072]; MTI-1018, [0005], [0030]; MTI-1019, 3:1-3.

Accordingly, a POSITA would have found it obvious and would have been

motivated to implement Tsunoda's memory apparatus with a USB connector for connecting the memory apparatus and the host, and with indicator lights to provide a visual indication of the status of the memory apparatus. MTI-1003, ¶99; MTI-1005, 1:19-24, 4:67-5:2, 5:16-20, 6:21-31; MTI-1013, [0006]-[0010], [0016], [0072]. A POSITA would have viewed the implementation of Tsunoda's memory apparatus in a manner that applied Sukegawa's suggested connector configuration as merely the predictable result of combining known prior art elements according to known methods. *Id.*; *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 405 (2007); *Intel Corp. v. Pact XPP Schweiz AG*, No. 22-1037 at 10-13 (Fed. Cir. 2023). A POSITA would have had a reasonable expectation of success in doing so as such an implementation was well-known as demonstrated by Sukegawa and commonly utilized in similar memory apparatus. MTI-1003, ¶99. A POSITA would have recognized that the above described modifications would have yielded predictable results, would have been within the ordinary level of skill of a POSITA, and would not have required undue experimentation. *Id.*

3. Claim 1

(a) Element 1[p]

Tsunoda-Sukegawa provides a "USB flash drive" which "is a small memory storage apparatus." MTI-1005, 1:38-42. Sukegawa's FIG. 1 shows a "USB memory apparatus 100" "with a USB connector shield case 120" that measures "12

millimeters (mm) wide $\pm$ 0.10 mm, 4.5 mm tall $\pm$ 0.10 mm, and a minimum of 11.75 mm deep.” MTI-1005, 4:44-48, 7:26-37; 9:17-31. A POSITA would have found it obvious that Tsunoda-Sukegawa’s flash drive is a portable memory apparatus. MTI-1003, ¶¶100-101; MTI-1013, [0004].

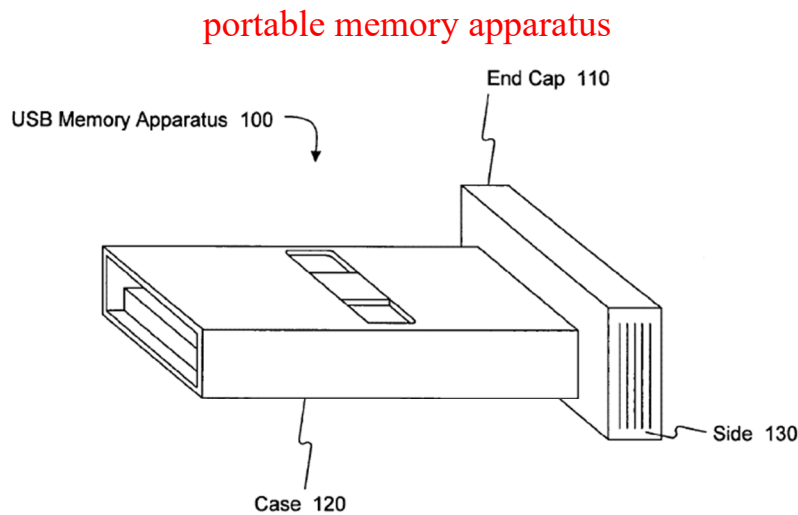


FIG. 1

MTI-1005, FIG. 1

(b) Element 1[a]

Tsunoda-Sukegawa’s USB flash drive includes “a USB connector shield case 120” that “extends from an overmold boot” and an end cap 110. MTI-1005, 4:44-48, 4:58-59, 7:26-32. “The circuit components of the flash drive apparatus can be mounted within case 120 in various configurations.” MTI-1005, 4:48-5:2, 5:16-24, 6:21-31, 8:6-9:16, FIGS. 5A-5H; MTI-1003, ¶¶102-103. A POSITA

would have found it obvious that Tsunoda-Sukegawa's USB flash drive has a housing in the form of the USB connector shield case 120, overmold boot, and end cap 110 that beneficially provides "a relatively low-profile, unobtrusive, and compact exterior for use with reduced size USB flash drive apparatus" within which the circuit components are mounted. *Id.*

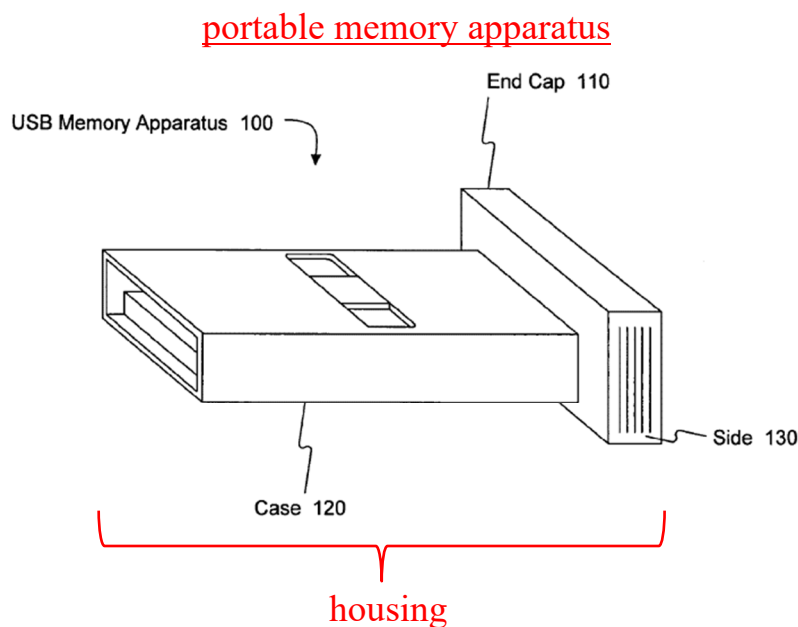


FIG. 1

MTI-1005, FIG. 1

(c) Elements 1[b]-1[d]

As discussed above (Ground 1A, 1[b]-1[d]), Tsunoda provides a memory apparatus with a memory control unit (memory controller [chip]), a SDRAM (volatile memory) coupled to the memory control unit, and a flash memory (non-volatile memory) coupled to the memory control unit. MTI-1004, [0001], [0035],

[0042], [0054]-[0056], [0060]-[0062], [0068], [0075], [0094], [0096]-[0099], [0104]-[0105], [0115], [0121]-[0122], [0124], [0131]-[0140], FIGS. 1, 9, 14, 18, 20-24. For a USB flash drive implementation, Sukegawa teaches that “[t]he circuit components of the flash drive apparatus can be mounted within case 120 in various configurations” and can be “implemented as one or more modules,” e.g., “three different modules.” MTI-1005, 4:44-66, 5:20-24, 5:29-37, 7:6-18, 7:26-37, 8:6-9:31, FIGS. 5A-5H; MTI-1003, ¶¶104-105. A POSITA would have found it obvious to implement, in Tsunoda-Sukegawa’s USB flash drive, the memory control unit (memory controller [chip]), the SDRAM (volatile memory), and the flash memory (non-volatile memory) as one, two, or three modules that are mounted within the housing formed by the USB connector shield case 120, overmold boot, and end cap 110, as shown below. *Id.*; MTI-1003, ¶106. A POSITA would have been capable of employing ordinary creativity to carry out an implementation of the USB flash drive in a manner necessary to achieve the advantages taught by Sukegawa by, for example, varying the size and shape of the housing to accommodate the electronic components. *Id.*; MTI-1013; MTI-1017; MTI-1018; MTI-1019; MTI-1020; *Facebook, Inc. v. Windy City Innovations, LLC*, 973 F.3d 1321, 1343 (Fed. Cir. 2020) (“‘a person of ordinary skill is also a person of ordinary creativity, not an automaton,’ so the fact that it would take some creativity to carry out the combination does not defeat a finding of obviousness.”).

An example of an implementation of the USB flash drive with the memory control unit (memory controller [chip]), the SDRAM (volatile memory), and the flash memory (non-volatile memory) as three different modules mounted within the housing is shown below.

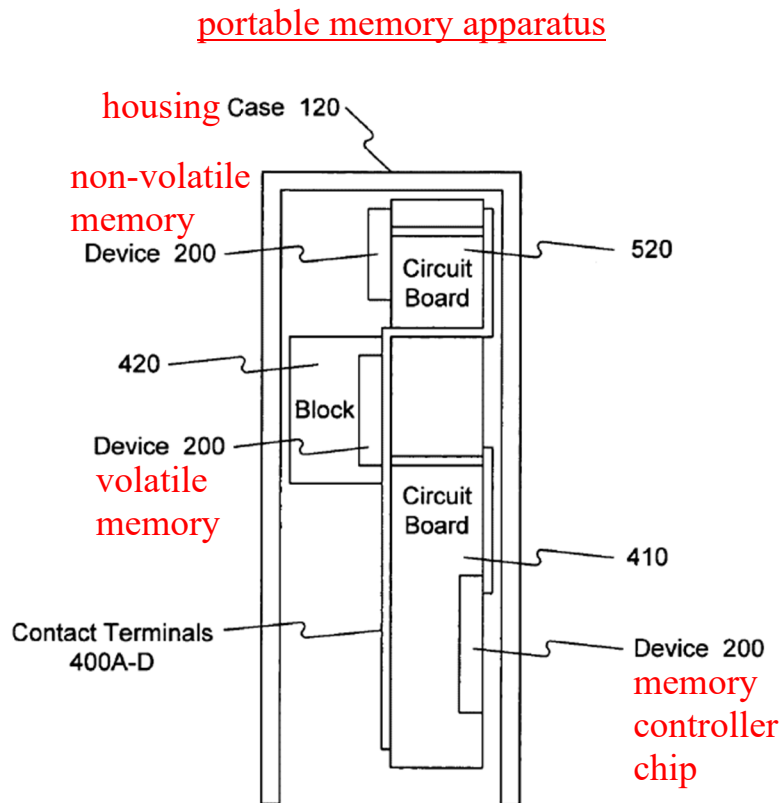


FIG. 5G

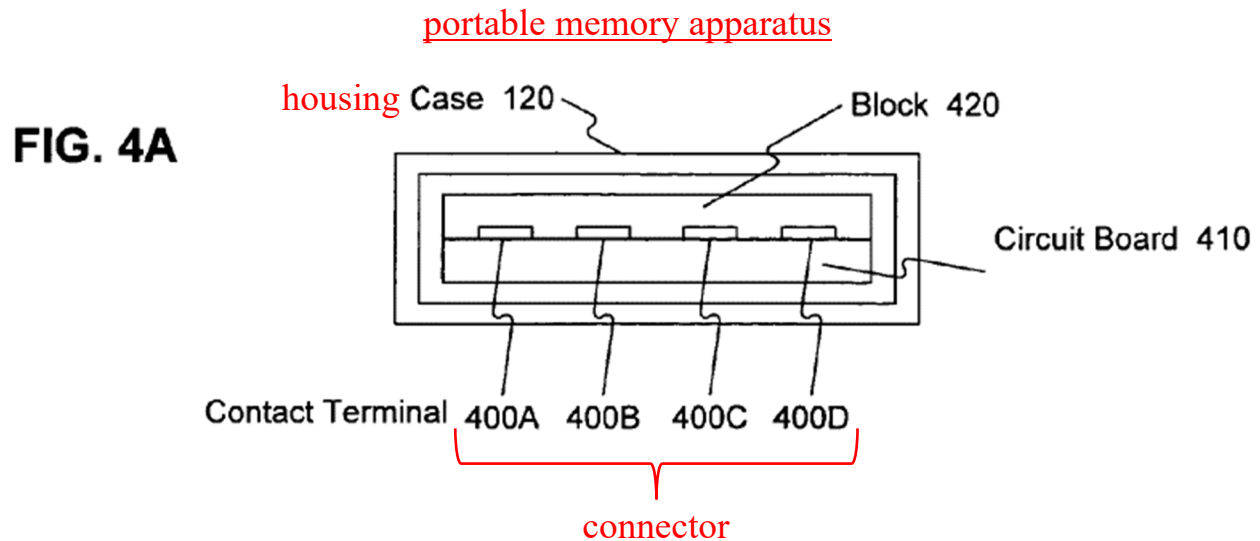
MTI-1005, FIG. 5G

(d) Element 1[e]

Tsunoda-Sukegawa's USB flash drive "interfaces with a host system

through a USB connector.” MTI-1005, 1:38-40. The USB connector includes a “set of contact terminals (shown in more detail in FIG. 4A-C)... disposed within the connector shield case 120... in a known configuration to line up with a mating USB connector” of a host system. MTI-1005, 4:54-57, 7:26-52. Accordingly, Tsunoda-Sukegawa’s USB flash drive (portable memory apparatus) has a USB connector that is positioned on the connector shield case 120 (forming the housing)⁴, as shown below, and that couples the USB flash drive to a host (computer system, *supra* Ground 1A, 1[e])) when the USB connector is plugged into the host. MTI-1003, ¶¶107-108; MTI-1013, [0090].

⁴ See footnote 1.



MTI-1005, FIG. 4A

(e) Element 1[f]

When Tsunoda-Sukegawa's USB flash drive is connected to the host (computer system) via the USB connector (*supra* Ground 2A, 1[e]), the memory control unit (memory controller chip) copies data from the flash memory (non-volatile memory) to the SDRAM (volatile memory), and the host accesses the data in the SDRAM through the USB connector in a similar manner and for similar reasons as explained in Ground 1A, 1[f]. MTI-1003, ¶109; MTI-1004, [0041]-[0043], [0048]-[0049], [0062], [0068], [0078], [0080]-[0084], [0093], [0096], [0099], [0104], [0112], [0131], [0139]-[0140], FIGS. 18, 23, 24 (4061-4062), 25 (4101-4105), 26 (4206).

4. Claim 6

Supra Ground 1A, claim 6. MTI-1003, ¶110.

5. Claim 7

Tsunoda-Sukegawa's USB flash drive includes "one or more lights that indicate connection to the host system, access to the apparatus memory or both." MTI-1005, 4:67-5:2, 5:16-20, 6:21-31. In Tsunoda-Sukegawa's USB flash drive, the lights would indicate when the flash memory is being or has been accessed, for example, when data stored in the SDRAM (volatile memory) is being or has been transferred to the flash memory (non-volatile memory). MTI-1003, ¶111; MTI-1013, [0016], [0072].

6. Claim 9

Supra Ground 1A, claim 9. MTI-1003, ¶112.

7. Claim 10

Supra Ground 2A, 1[e]; MTI-1003, ¶113.

8. Claims 11 and 14

Tsunoda-Sukegawa's USB flash drive has a USB connector shield case 120 that "extends from an overmold boot" and an end cap 110. MTI-1005, 4:58-66, 7:26-37. "The overmold boot is typically an injection molded thermoplastic insulator material with a minimum UL 94-VO rating." MTI-1005, 7:33-34. Based on a POSITA's general knowledge that "injection molded thermoplastic insulator material with a minimum UL 94-VO rating" includes materials such as ABS, which possesses outstanding impact strength, a POSITA would have found it an

obvious design choice to use ABS to form at least a portion of the housing (e.g., the overmold boot and end cap) of Tsunoda-Sukegawa's USB flash drive to beneficially provide an outer shell that has outstanding impact strength, toughness, and resistance to protect the components of the flash drive from damage due to mishandling, moisture, dust and debris, and electrostatic discharge. MTI-1003, ¶114; MTI-1014, 4; MTI-1015, 2; MTI-1011; MTI-1023, 10.

9. Claim 12

Tsunoda-Sukegawa's USB flash drive includes SDRAM, flash memory, and memory control unit on different silicon chips, and interconnects terminals of the silicon chips by, for example, wire bonding, through-holes, or solder bumps. MTI-1004, [0056], [0124]; MTI-1005, 4:48-50, 6:42-7:18, 8:6-9:16, FIGS. 3, 5A-5H. A POSITA would have found it obvious that Tsunoda-Sukegawa's USB flash drive, which includes the SDRAM, flash memory, and memory control unit on different silicon chips housed in a USB connector shield case 120 that "extends from an overmold boot" and an end cap 110, as shown below, does not have any moving parts. MTI-1004, [0124]; MTI-1005, 4:58-59, 7:26-32, FIG. 1; MTI-1003, ¶¶115-116; MTI-1012, [0005], [0031].

portable memory apparatus

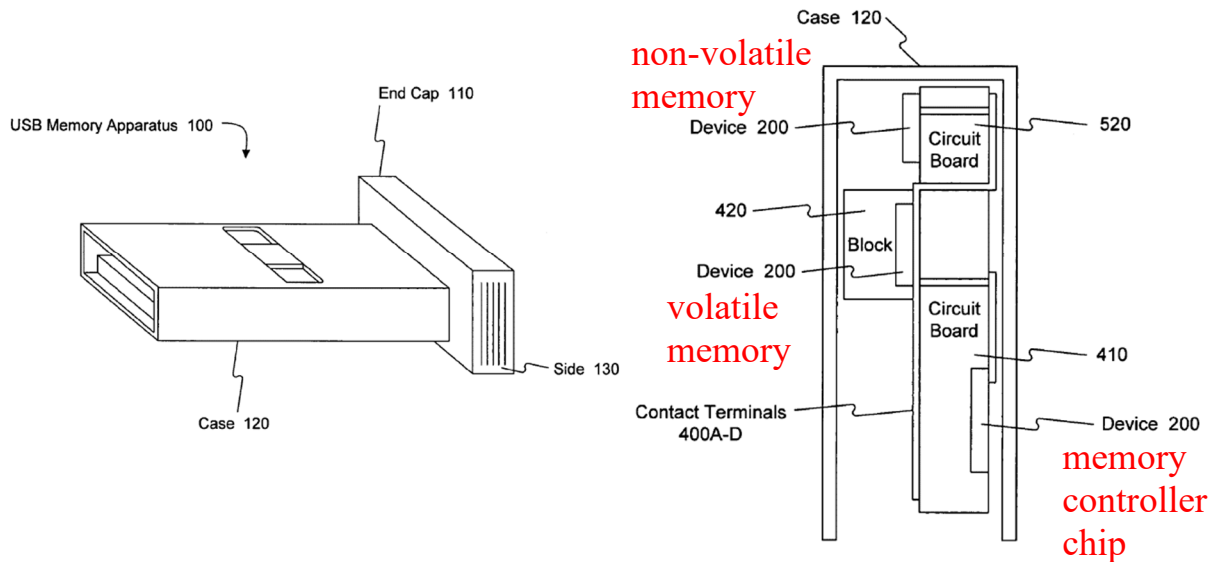


FIG. 1

FIG. 5G

MTI-1005, FIGS. 1 , 5G

10. Claim 15

(a) Element 15[p]

Tsunoda-Sukegawa teaches a method as set forth below. MTI-1003, ¶117.

(b) Element 15[a]

Supra Ground 2A, 1[p] and 1[e]. MTI-1003, ¶118.

(c) Element 15[b]

Supra Ground 2A, 1[b], 1[c], 1[d]. MTI-1003, ¶119.

(d) Element 15[c]

Supra Ground 2A, 1[f]. MTI-1003, ¶120.

(e) Element 15[d]

Supra Ground 2A, 1[f]. MTI-1003, ¶121.

(f) Element 15[e]

Supra Ground 2A, claim 6. MTI-1003, ¶122.

11. Claim 18

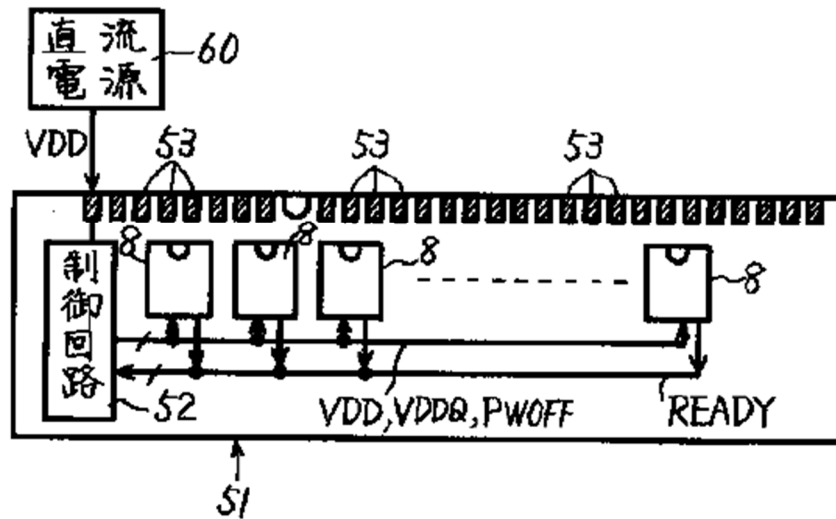
Supra Ground 2A, claim 7. MTI-1003, ¶123.

**C. GROUNDS 1B and 2B—Claims 2-5 and 16-17 are obvious over
Tsunoda, alone or with Sukegawa, and Tomio**

1. Overview of Tomio

Tomio relates to “a semiconductor memory apparatus that can be accessed quickly and that has nonvolatile data.” MTI-1006, [0001], [0005], [0045]; MTI-1003, ¶¶125-128. Tomio’s FIG. 11 shows an example of a memory module 51 that includes semiconductor memories 8 and a control circuit 52. MTI-1006, [0038].

【図 11】



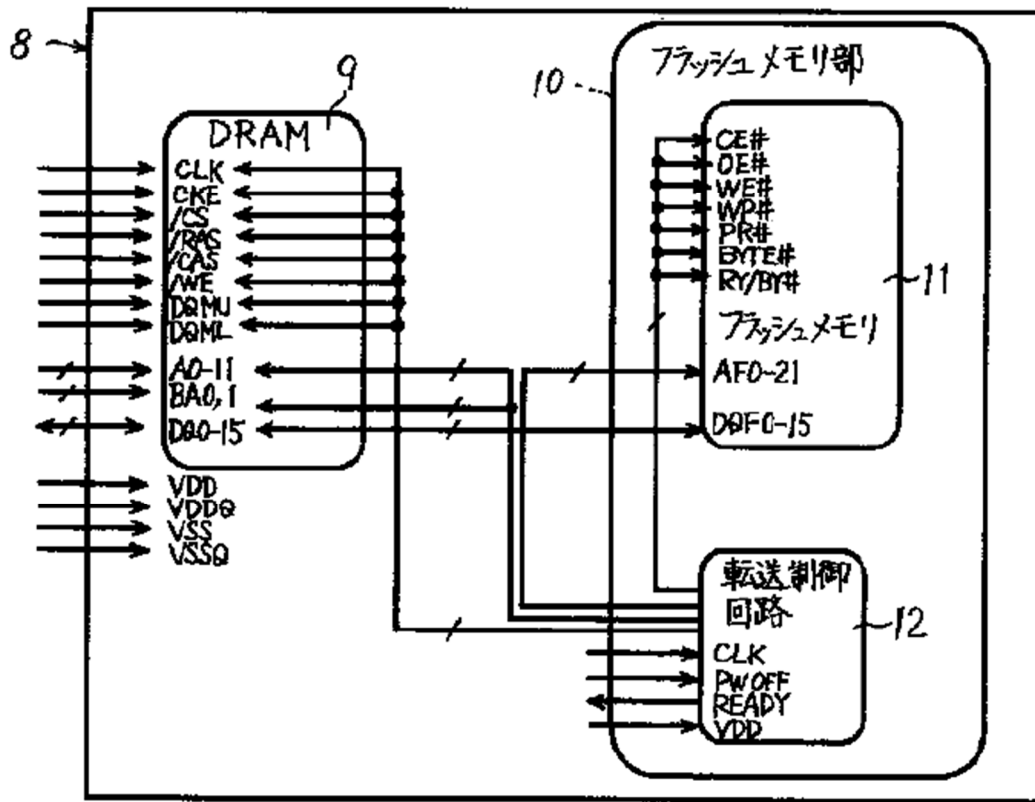
MTI-1006, FIG. 11

“The control circuit 52 includes a rechargeable battery 61” (FIG. 12) that “is charged with the direct current power supply potential VDD from the direct current power supply 60 and outputs direct current power supply potentials VDD and VDDQ.” MTI-1006, [0039]. “The rechargeable battery 61 continues to output direct current power supply potentials VDD and VDDQ for a predetermined period of time even when supply of the direct current power supply potential VDD from the direct current power supply 60 has been stopped.” MTI-1006, [0039], [0027].

Each semiconductor memory 8 includes “DRAM 9 and a flash memory unit 10, and the flash memory unit 10 includes flash memory 11 and a transfer control circuit 12,” as shown in FIG. 2. MTI-1006, [0018], [0043]. The DRAM 9 stores data supplied from a personal computer during a write operation and supplies read

data to the personal computer during a read operation. MTI-1006, [0019], [0025], [0032]. The DRAM 9 also receives signals from the transfer control circuit 12 during data fetching and data storage, stores read data in the flash memory 11 during data fetching, and supplies read data to the flash memory 11 during data storage. MTI-1006, [0020]. The flash memory 11 receives signals from the transfer control circuit 12, stores read data from the DRAM 9 during data storage, and supplies read data to the DRAM 9 during data fetching. MTI-1006, [0021]. “The transfer control circuit 12 transfers data stored in the flash memory 11 to the DRAM 9 in response to the rising edge of the power supply potential VDD.” MTI-1006, [0022]-[0024], [0032]. In addition, the transfer control circuit 12 transfers data in the DRAM 9 to the flash memory 11 in response to a PW OFF signal from the personal computer. MTI-1006, [0022], [0028], [0032].

【図2】



MTI-1006, FIG. 2

2. Tsunoda-Tomio (GROUND 1B) and Tsunoda-Sukegawa-Tomio (GROUND 2B) Combinations

Tsunoda discloses that “when power is turned OFF, a content of the volatile memory is copied in the nonvolatile memory, and a result of its processing is notified through an exclusive line to the host” and consequently, “power is safely turned OFF, and data is held even after the power is OFF.” MTI-1004, [0002]. However, Tsunoda does not account for the situation where power is abruptly turned off (by unplugging or power outage) before the transfer starts or before the

transfer completes. MTI-1003, ¶129. In this situation, data that is not copied from the volatile memory to the nonvolatile memory will be lost. *Id.*; MTI-1004, [0075]; MTI-1006, [0002], [0032], [0039], [0027]; MTI-1007, [0009]-[0012], [0061].

In the event that the external power supply is abruptly stopped, Tomio's module includes a "rechargeable battery" that "continues to output direct current power supply potentials VDD and VDDQ for a predetermined period of time even when supply of the direct current power supply potential VDD from the direct current power supply 60 has been stopped," a "control circuit" that "supplies a PW OFF signal to each semiconductor memory 8 in response to the supply of the direct current power supply potential VDD from the direct current power supply 60 being stopped," and a "transfer control circuit" that "transfers data in the DRAM 9 to the flash memory 11 in response to a PW OFF signal." MTI-1006, [0038]-[0039], [0022], [0027]-[0028], [0032]. A POSITA would have been motivated to apply the teachings of Tomio to Tsunoda's and Tsunoda-Sukegawa's memory apparatus to provide a memory apparatus with a rechargeable battery that continues to supply power long enough for the memory controller to copy data from volatile memory to nonvolatile memory in the event that the external power to the memory apparatus is abruptly stopped. MTI-1003, ¶130; MTI-1004, [0002]; MTI-1006, [0039], [0027].

Tsunoda expressly contemplates that its memory apparatus holds data even after the power is OFF using a nonvolatile memory. MTI-1004, [0002], [0039], [0075], [0098], [0112]. A POSITA implementing Tsunoda's and Tsunoda-Sukegawa's memory apparatus would have turned to examples of similar memory apparatus to identify additional suitable techniques for retaining data after the power is off. MTI-1003, ¶131. Tomio's teachings enable implementation of a memory apparatus, such as that described in Tsunoda, where the memory controller copies data from volatile memory to nonvolatile memory using power supplied by a rechargeable battery to achieve Tsunoda's goals of retaining data after the power is off. *Id.*; MTI-1004, [0002], [0039], [0075], [0098], [0112]; MTI-1006, [0039], [0027]. A POSITA would have been motivated to apply the teachings of Tomio to Tsunoda's or Tsunoda-Sukegawa's memory apparatus to beneficially provide a memory apparatus that retains data even when the external power supply is abruptly stopped. *Id.*

Accordingly, a POSITA would have found it obvious and would have been motivated to implement Tsunoda's and Tsunoda-Sukegawa's memory apparatus with a rechargeable battery that supplies power and functionality in the memory controller for transferring data from volatile memory to nonvolatile memory after the external power supply has been stopped or turned off based on Tomio's teachings. *Id.*; MTI-1003, ¶132. A POSITA would have viewed the

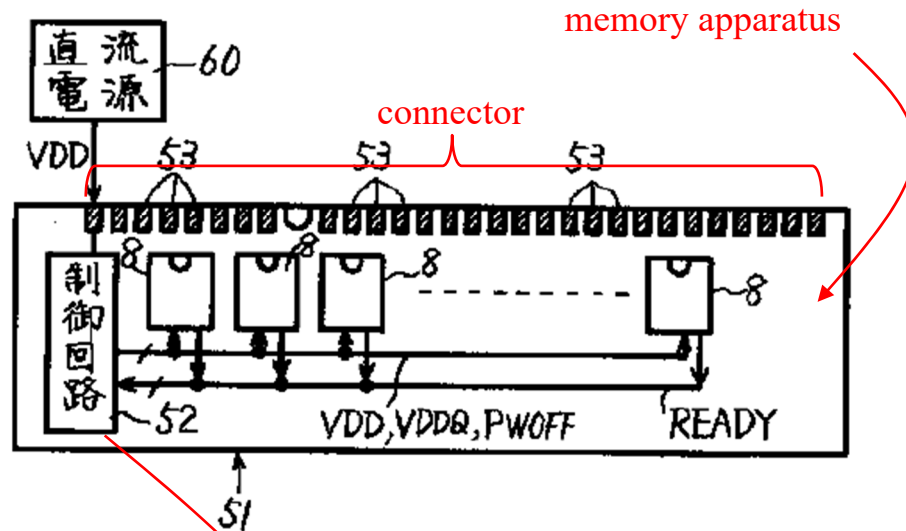
implementation of Tsunoda's and Tsunoda-Sukegawa's memory apparatus in a manner that applied Tomio's suggestion regarding a rechargeable battery and corresponding functionality of its memory controller as merely the predictable result of combining known prior art elements according to known methods. *Id.*; *KSR*, 550 U.S. at 405; *Intel*, No. 22-1037 at 10-13. A POSITA would have had a reasonable expectation of success in doing so as such an implementation was well-known as demonstrated by Tomio and commonly utilized in similar memory apparatus. *Id.* A POSITA would have recognized that the above described modifications would have yielded predictable results, would have been within the ordinary level of skill of a POSITA, and would not have required undue experimentation. *Id.* A POSITA would have been capable of employing ordinary creativity to carry out an implementation of the memory apparatus with the rechargeable battery and corresponding memory controller functionality in a manner necessary to achieve the advantages taught by Tomio by, for example, varying the size and shape of the memory apparatus and housing (as taught by Tsunoda or Sukegawa) to accommodate the electronic components and rechargeable battery. *Id.*; MTI-1013; MTI-1017; MTI-1018; MTI-1019; MTI-1020; *Facebook*, 973 F.3d at 1343.

3. Claims 2, 4, and 5

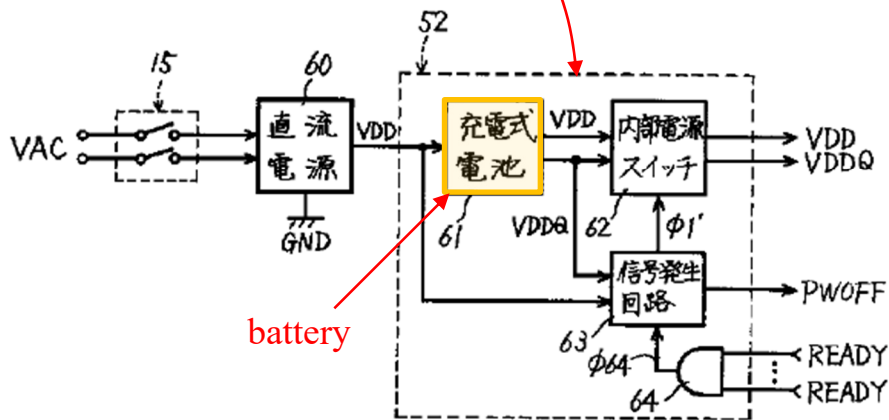
Tomio describes a memory module that includes a "rechargeable battery 61"

(yellow in FIG. 12 below) that “is charged with the direct current power supply potential VDD from the direct current power supply 60 and outputs direct current power supply potentials VDD and VDDQ.” MTI-1006, [0039]. “The rechargeable battery 61 continues to output direct current power supply potentials VDD and VDDQ for a predetermined period of time even when supply of the direct current power supply potential VDD from the direct current power supply 60 has been stopped.” MTI-1006, [0039], [0027]. As shown in Tomio’s FIGS. 11 and 12, “control circuit 52 receives direct current power supply potential VDD from a direct current power supply 60 outside of the module 51 via an input terminal 53” (of the connector). MTI-1006, [0038].

【図11】



【図12】



MTI-1006, FIGS. 11, 12 (collated)

From Tomio's teachings, a POSITA would have found it obvious to include a rechargeable battery (internal power source) in Tsunoda-Tomio's and Tsunoda-Sukegawa-Tomio's memory apparatus (portable memory apparatus) that is rechargeable through its respective connectors (MTI-1004, [0114]; MTI-1005,

7:26-52) to supply power long enough to copy data from volatile memory to nonvolatile memory in the event that the external power to the memory apparatus is abruptly stopped. MTI-1003, ¶¶133-135.

4. Claim 3

In Tomio's memory module, "rechargeable battery 61 continues to output direct current power supply potentials VDD and VDDQ for a predetermined period of time even when supply of the direct current power supply potential VDD from the direct current power supply 60 has been stopped." MTI-1006, [0039], [0027]. A POSITA would have found it obvious that "supply of the direct current power supply potential VDD from the direct current power supply 60 has been stopped" when the module 51 is unplugged from the personal computer or when the personal computer powers off. MTI-1003, ¶136.

Tomio further teaches that during normal operations, "the semiconductor memory 8 operates as a DRAM 9" from the perspective of the personal computer. MTI-1006, [0025]. The DRAM 9 is in an idle state or access standby when not accessed by the personal computer, and reads and writes data when accessed by the personal computer. *Id.* The DRAM 9 stores data supplied from a personal computer during a write operation and supplies read data to the personal computer during a read operation. MTI-1006, [0019], [0025], [0032]. In response to the external power supply being stopped or turned off, "data in the DRAM 9 is stored

in the flash memory 11.” MTI-1006, [0032], [0022]. “In this way, a semiconductor memory 8 can be realized that enables high-speed access like a DRAM but has data nonvolatility like a flash memory.” *Id.* From Tomio’s teachings, a POSITA would have found it obvious to include the rechargeable battery to supply power for Tsunoda-Tomio’s and Tsunoda-Sukegawa-Tomio’s memory apparatus to copy data from the SDRAM (volatile memory) to the flash memory (non-volatile memory) when the memory apparatus is unplugged from the host (computer system) to beneficially provide a memory apparatus that enables high-speed access like a DRAM but has data nonvolatility like a flash memory. MTI-1003, ¶137.

5. Claim 16⁵

Supra Grounds 1B/2B, claims 2 and 3. MTI-1003, ¶138.

6. Claim 17

Supra Grounds 1B/2B, claim 4. MTI-1003, ¶139.

D. GROUND 3A—Claims 1-6, 9, 12, and 15-17 are obvious over Tomio

In its complaint for infringement, Patent Owner appears to advance a scope for the terms “portable” and “housing” with which Petitioner disagrees. Specifically, Patent Owner identifies Petitioner’s memory devices having a M.2

⁵ See footnote 2.

form factor (a specification for internally mounted computer cards) as allegedly infringing claims of the '527 patent. MTI-1021, 3 (listing accused products as including, e.g., 3400 SSD with NVMe, Crucial P5 Plus with NVMe, Crucial P3 with NVMe, among other M.2 form factor memory devices). This ground addresses the claims under the scope of these claim terms advanced by Patent Owner in its complaint for infringement.⁶

1. Claim 1

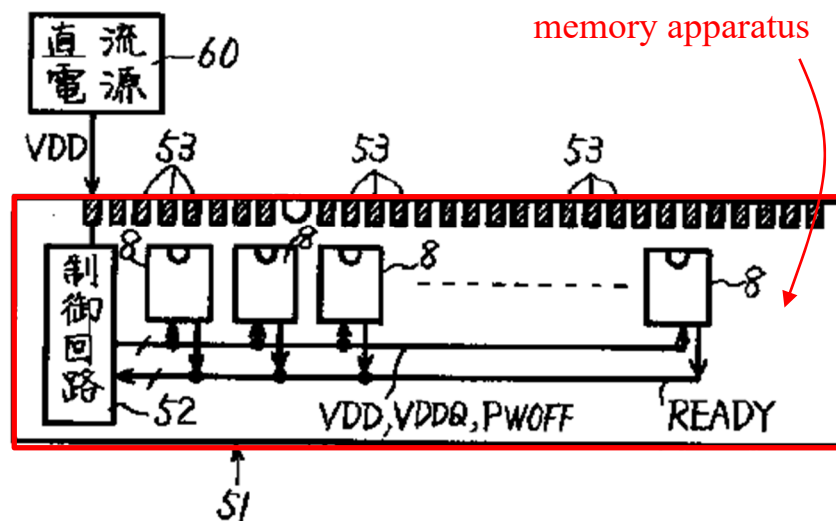
(a) Element 1[p]

Tomio's FIG. 11 shows an example of a memory module 51 that includes semiconductor memories 8. MTI-1006, [0038]. The module 51 "operates as a single memory unit" with semiconductor memories 8 mounted on a substrate such as "a Mitsubishi Electric 256 MB 168 pin unbuffered dual inline module." MTI-1006, [0037]. "This 256 MB module can also be used as the main memory in a personal computer by pre-storing data that is usually stored in ROM in the flash memory 11 of the semiconductor memory 8." MTI-1006, [0037]. In accordance with the scope of the term "portable" advanced by Patent Owner in its complaint

⁶ Petitioner reserves the right to challenge Patent Owner's allegation that a M.2 or similar form factor memory device satisfies the "portable" and "housing" limitations required by the claims of the '527 patent.

for infringement, Tomio's memory module 51 is labeled as a "portable memory apparatus" in the figure below (although Petitioner disagrees), as Tomio's 168 pin unbuffered dual inline module is a form factor that is similar to the M.2 form factor that Patent Owner alleges satisfies this claim element. MTI-1021, 3; MTI-1003, ¶141; MTI-1016; MTI-1024.

【図 11】



MTI-1006, FIG. 11

(b) Element 1[a]

Tomio's memory module 51 includes semiconductor memories 8 and a control circuit 52 mounted on a substrate such as "a Mitsubishi Electric 256 MB 168 pin unbuffered dual inline module," as shown in FIG. 11 (above). MTI-1006, [0037]-[0038]. Each semiconductor memory 8 includes "DRAM, flash memory, and transfer control circuit... sealed in a single package." MTI-1006, [0043],

[0030]-[0031], [0034]-[0035], FIGS. 7-9. In accordance with the scope of the term “housing” advanced by Patent Owner in its complaint for infringement, Tomio’s memory module 51 includes packages in which the semiconductor memories 8 are provided and a substrate on which the semiconductor memories 8 and the control circuit 52 are mounted similar to the M.2 form factor memory devices that Patent Owner alleges satisfies this claim element.⁷ MTI-1021, 3; MTI-1003, ¶142; MTI-1024.

(c) Element 1[b]

On Tomio’s memory module 51, each semiconductor memory 8 includes “a transfer control circuit 12” that controls the transfer of data between the memories, as shown in FIG. 2. MTI-1006, [0018], [0020]-[0024], [0028], [0032], [0043]. The “DRAM, flash memory, and transfer control circuit are sealed in a single package.” MTI-1006, [0043], [0018], [0030]-[0031], [0034]-[0035], FIGS. 7-9.

Tomio’s FIGS. 2 and 7 show the transfer control circuit 12/12’ (memory controller [chip]) (blue) in the package (outlined red) of the semiconductor memory 8. In accordance with the scope of the term “housing” advanced by Patent Owner in its complaint for infringement, Tomio’s memory module 51 includes a package in which the transfer control circuit is provided and a substrate on which

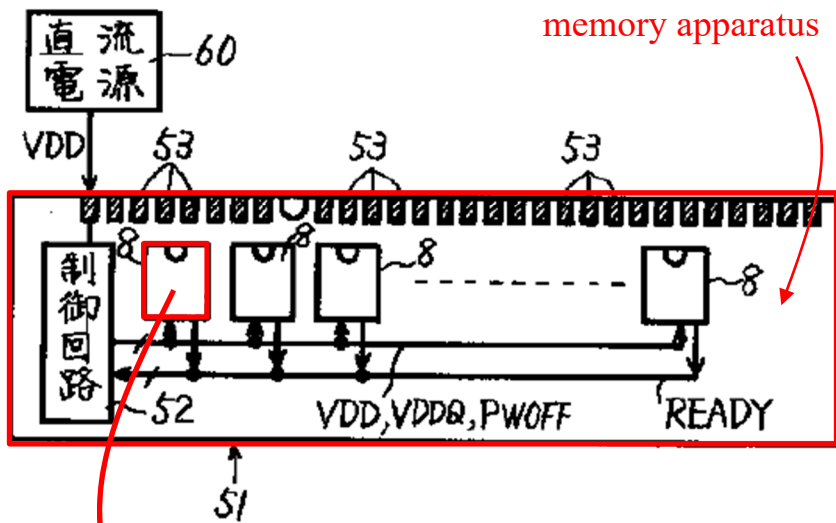
⁷ See footnote 5.

the package is mounted similar to the M.2 form factor memory devices that Patent Owner alleges satisfies this claim element. MTI-1003, ¶¶143-145; MTI-1021, 3; MTI-1024.

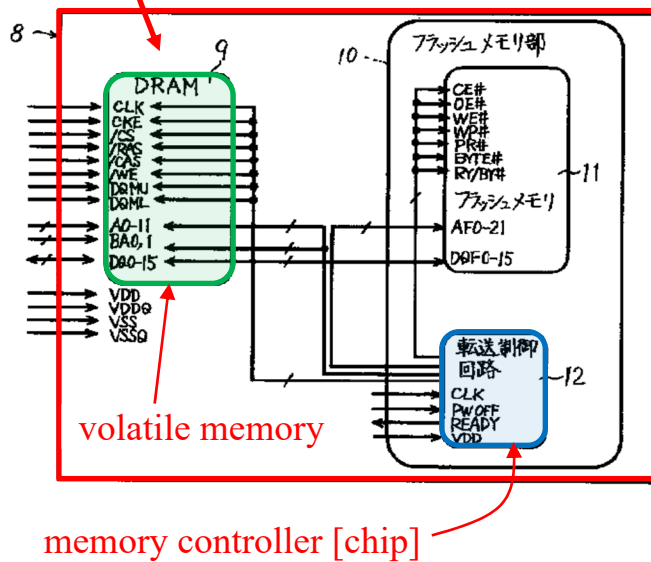
(“DRAMs... are volatile memories”), [0018], [0020]-[0024], [0028], [0032], [0043]. The “DRAM, flash memory, and transfer control circuit are sealed in a single package.” MTI-1006, [0048], [0018], [0030]-[0031], [0034]-[0035], FIGS. 7-9. Tomio’s FIGS. 2 and 7 show the DRAM 9/9’ (volatile memory) (green) coupled to the transfer control circuit 12/12’ (memory controller [chip]) (blue) in the package (outlined red) of the semiconductor memory 8. In accordance with the scope of the term “housing” advanced by Patent Owner in its complaint for infringement, Tomio’s memory module 51 includes a package in which the DRAM is provided and a substrate on which the package is mounted similar to the M.2 form factor memory devices that Patent Owner alleges satisfies this claim element.⁸ MTI-1003, ¶¶146-149; MTI-1021, 3; MTI-1024.

⁸ See footnote 5.

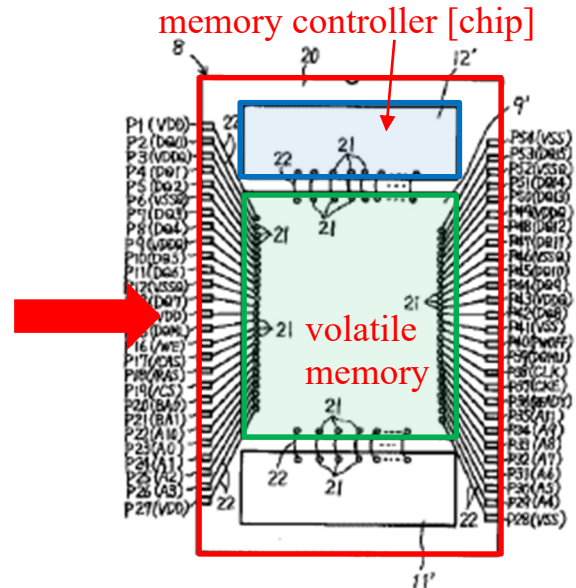
【図 1 1】



【図 2】



【図 7】



MTI-1006, FIGS. 11, 2, 7 (collated)

(e) Element 1[d]

On Tomio's memory module 51, each semiconductor memory 8 includes a nonvolatile memory, e.g., "a flash memory unit 10" as shown in FIG. 2. MTI-

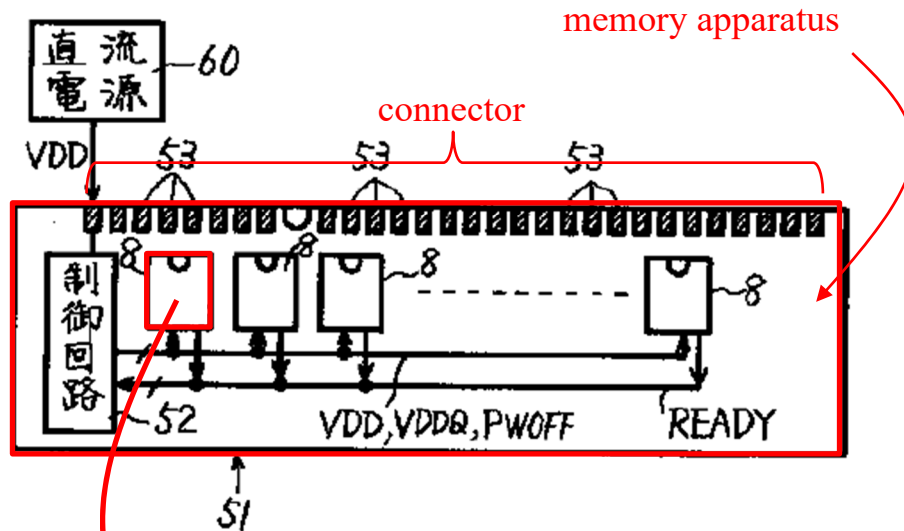
1006, [0002] (“a nonvolatile storage medium such as... a flash memory card”), [0018], [0020]-[0024], [0028], [0032], [0043]. The “flash memory, and transfer control circuit are sealed in a single package.” MTI-1006, [0043], [0018], [0030]-[0031], [0034]-[0035], FIGS. 7-9. Tomio’s FIGS. 2 and 7 show the DRAM 9/9’ (volatile memory) (green) and the flash memory 11/11’ (non-volatile memory) (purple) coupled to the transfer control circuit 12/12’ (memory controller [chip]) (blue) in the package (outlined red) of the semiconductor memory 8. In accordance with the scope of the term “housing” advanced by Patent Owner in its complaint for infringement, Tomio’s memory module 51 includes a package in which the DRAM, the flash memory, and the transfer control circuit are provided and a substrate on which the package is mounted similar to the M.2 form factor memory devices that Patent Owner alleges satisfies this claim element.⁹ MTI-1003, ¶¶150-153; MTI-1021, 3; MTI-1024.

⁹ See footnote 5.

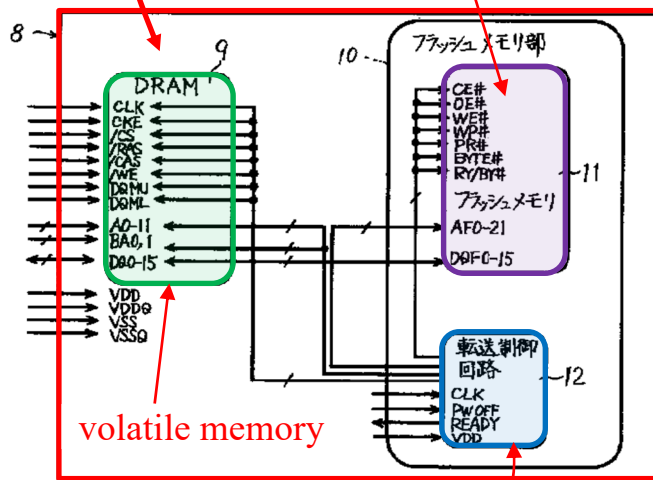
(connector) positioned on the substrate (outlined red) of the memory module 51 similar to the M.2 form factor memory devices that Patent Owner alleges satisfies this claim element.¹⁰ MTI-1006, [0037]-[0038], FIG. 11; MTI-1021, 3; MTI-1024; MTI-1003, ¶154. A POSITA would have found it obvious that the terminals 53 couple the memory module 51 to a personal computer (computer system) when the terminals 53 are plugged into the personal computer to enable the memory module 51 to communicate with the personal computer. *Id.*

¹⁰ See footnote 5.

【図 1 1】



non-volatile memory
【図 2】

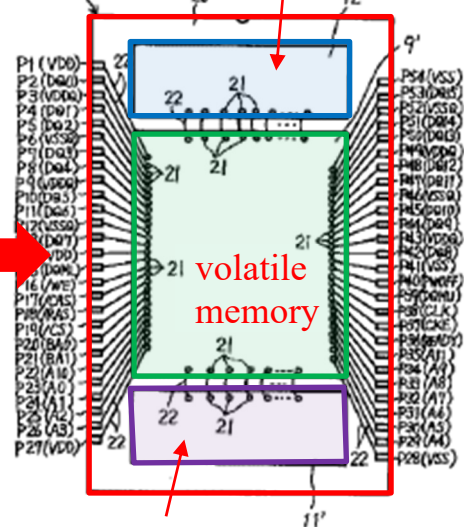


volatile memory

memory controller [chip]

【図 7】

memory controller [chip]



non-volatile memory

MTI-1006, FIGS. 11, 2, 7 (collated)

(g) Element 1[f]

When the terminals 53 of Tomio's memory module 51 couples the module 51 to a personal computer, "control circuit 52 receives direct current power supply

potential VDD from a direct current power supply 60 outside of the module 51 via an input terminal 53, and supplies direct current power supply potentials VDD and VDDQ to each semiconductor memory 8 in the module 51.” MTI-1006, [0038].

“The transfer control circuit 12 transfers data stored in the flash memory 11 to the DRAM 9 in response to the rising edge of the power supply potential VDD.” MTI-1006, [0022]-[0026], [0032].

After the data has been copied from the flash memory 11 to the DRAM 9, normal operations are performed where “the semiconductor memory 8 operates as a DRAM 9” from the perspective of the personal computer. MTI-1006, [0025].

The DRAM 9 is in an idle state or access standby when not accessed by the personal computer, and reads and writes data when accessed by the personal computer. *Id.* The DRAM 9 stores data supplied from a personal computer during a write operation and supplies read data to the personal computer during a read operation. MTI-1006, [0019], [0032]. Accordingly, when the terminals 53 (connector) couples the module 51 to the personal computer (computer system), the transfer control circuit (memory controller chip) copies data from the flash memory (non-volatile memory) to the DRAM (volatile memory), and the personal computer accesses the data in the DRAM through the terminals 53. MTI-1003, ¶¶155-157.

2. Claims 2, 4, and 5

For similar reasons discussed above (Grounds 1B/2B, claims 2, 4, and 5), Tomio’s memory module 51 includes a rechargeable battery (internal power source) that is rechargeable through the terminal 53 (of the connector) and that continues to supply power long enough to copy data from volatile memory to nonvolatile memory in the event that the external power to the memory apparatus is abruptly stopped. MTI-1003, ¶158.

3. Claim 3

For similar reasons discussed above (Grounds 1B/2B, claim 3), the rechargeable battery (internal power source) powers the module 51 and the module 51 copies data from the DRAM (volatile memory) to the flash memory (non-volatile memory) when the module 51 is unplugged from the personal computer (computer system). MTI-1003, ¶159.

4. Claim 6¹¹

If the Board construes “transfers said non-volatile memory with data written to said volatile memory from said computer system” to mean “transfers *to* said non-volatile memory data written to said volatile memory from said computer system” (*i.e.*, the italicized “to” should be inserted and “with” should be deleted),

¹¹ See footnote 2.

Tomio renders this obvious for the reasons discussed above for Ground 3A, claim 3. MTI-1003, ¶¶160-161.

If the Board construes “transfers said non-volatile memory with data written to said volatile memory from said computer system” to mean “transfers *from* said non-volatile memory data written to said volatile memory from said computer system” or “transfers data *from* the non-volatile memory *to* the volatile memory so that it can be accessed by the host computer,” Tomio renders this obvious for the reasons discussed above for Ground 3A, 1[f]. MTI-1003, ¶162.

5. Claim 9

Supra Ground 3A, 1[c]. MTI-1003, ¶163.

6. Claim 12

As previously discussed, Tomio’s memory module 51 includes semiconductor memories 8 and a control circuit 52 mounted on a substrate such as “a Mitsubishi Electric 256 MB 168 pin unbuffered dual inline module,” as shown in FIG. 11 (above). MTI-1006, [0037]-[0038]. Each semiconductor memory 8 includes “DRAM, flash memory, and transfer control circuit... sealed in a single package.” MTI-1006, [0048], [0030]-[0031], [0034]-[0035], [0043], FIGS. 7-9. A POSITA would have understood or at least found it obvious that the memory module 51, which includes packaged semiconductor memories 8 and a control circuit 52 mounted on a substrate, does not have any moving parts. MTI-1003,

¶164.

7. Claim 15

(a) Element 15[p]

Under the scope of the term “portable” advanced by Patent Owner in its complaint for infringement,¹² Tomio teaches a method as set forth below. MTI-1003, ¶165.

(b) Element 15[a]

Supra Ground 3A, 1[p] and 1[e]. MTI-1003, ¶166.

(c) Element 15[b]

Supra Ground 3A, 1[b], 1[c], 1[d]. MTI-1003, ¶167.

(d) Element 15[c]

Supra Ground 3A, 1[f]. MTI-1003, ¶168.

(e) Element 15[d]

Supra Ground 3A, 1[f]. MTI-1003, ¶169.

(f) Element 15[e]

Supra Ground 3A, claim 6. MTI-1003, ¶170.

8. Claim 16¹³

Supra Ground 3A, claims 2 and 3. MTI-1003, ¶171.

¹² See footnote 5.

¹³ See footnote 2.

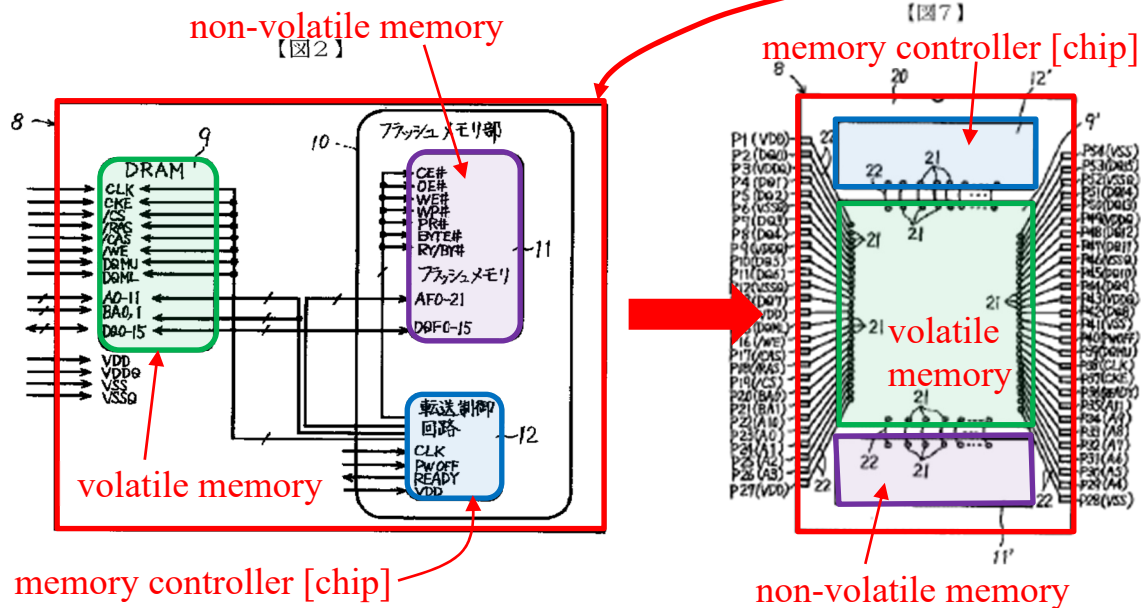
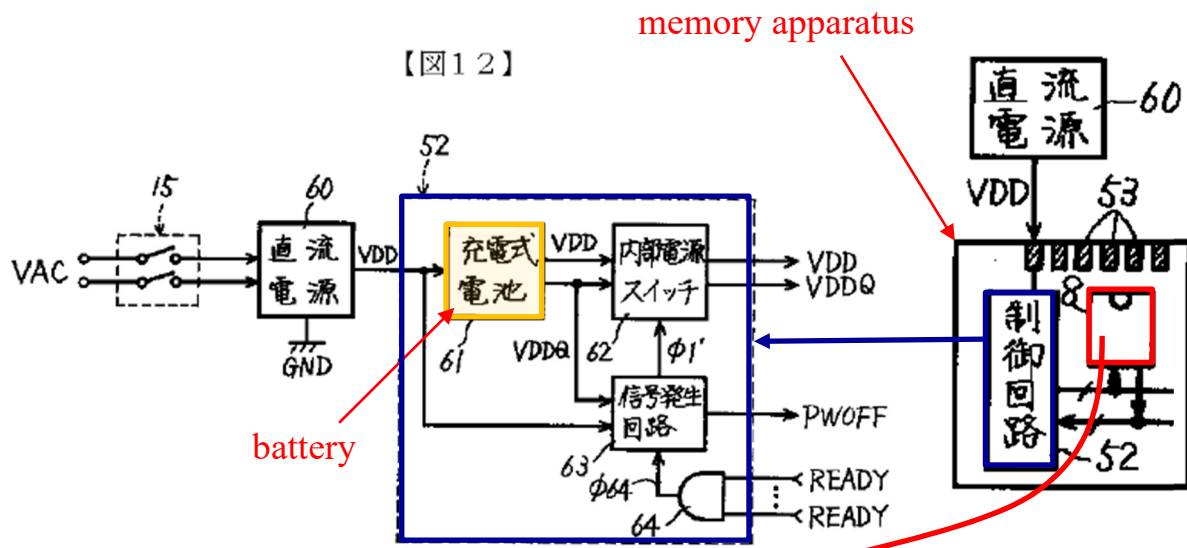
9. Claim 17

Supra Ground 3A, claim 4. MTI-1003, ¶172.

E. GROUND 4A—Claims 1-7, 9-12, and 14-18 are obvious over Tomio and Sukegawa

1. Tomio-Sukegawa Combination

Although the above description of Tomio relates to a memory module with multiple semiconductor memories and a control circuit mounted on a substrate (MTI-1006, [0037]-[0038], FIG. 11), a POSITA would have found it obvious, from Tomio's explicit teachings, to implement a memory apparatus with one semiconductor memory and a control circuit mounted on a substrate, as shown below. MTI-1006, [0018]-[0024], [0025]-[0026], [0028], [0030]-[0032], [0034]-[0035], [0043]-[0044], [0048], FIGS. 2, 7-9, claims 1-6 (claiming the elements of one semiconductor memory and a control circuit), [0045]-[0050] (describing the same); MTI-1003, ¶174.



MTI-1006, FIGS. 2, 7, 11, 12

(modified to show one semiconductor memory 8 and collated)

A POSITA implementing such a memory apparatus would have turned to examples of similar memory apparatus to identify suitable housings for the electrical components and interfaces for connecting to a computer system. MTI-1003, ¶175. Sukegawa provides a suitable housing and interface for such a

memory apparatus. *Id.*; MTI-1005, 1:13-24. Those in the field have recognized that a USB interface has advantages over other interfaces in that it offers “the advantages of high safety, high data transmission speed (12 mb/sec.), hot swapping, convenient operation, no need of any computer assembling experience or any computer changing device, and of being able to support systems such as Windows 98 and Mac OS 8.6 etc.” and “can be quickly connected to communicate with computers having USB plugs, and can easily have data directly transmitted to and from other types of consumer electronic and communication devices.” MTI-1017, 1:53-67; MTI-1005, 1:13-44; MTI-1013, [0010]. A POSITA would have been motivated to apply the teachings of Sukegawa to Tomio’s suggested memory apparatus to provide a memory apparatus that connects to a host via a USB connector to achieve the above-stated benefits of a USB flash memory device. *Id.*; MTI-1003, ¶175.

Sukegawa discloses that a flash memory device, such as Tomio’s suggested memory apparatus, can be implemented as a “USB flash drive apparatus” that “interfaces with a host system through a USB connector.” MTI-1005, 1:38-40, 4:35-38. Sukegawa’s teachings enable implementation of a memory apparatus, such as that suggested in Tomio, as a USB flash drive apparatus. MTI-1003, ¶¶176-177; MTI-1005, 4:48-50, 8:6-9:16, FIGS. 5A-5H. A POSITA would have been motivated to apply the teachings of Sukegawa to Tomio’s suggested memory

apparatus to beneficially provide a USB flash drive apparatus having “an expandable, hot-pluggable serial interface that ensures a standard, low-cost connection for peripheral devices” and “provides additional bandwidth for multimedia and storage applications and also offers Plug-and-Play capability.”

MTI-1005, 1:13-30; MTI-1017, 1:53-67; MTI-1003, ¶177.

Sukegawa also provides that the USB flash drive apparatus includes “one or more lights that indicate connection to the host system, access to the apparatus memory or both.” MTI-1005, 4:67-5:2, 5:16-20, 6:21-31. These additional teachings of Sukegawa would further motivate a POSITA to implement a flash memory device, such as Tomio’s suggested memory apparatus, as a USB flash drive apparatus with indicator lights. *Id.*; MTI-1003, ¶178. A POSITA would have found it obvious that removing a USB flash drive apparatus during data transfers is not desirable and would have been motivated to add an indicator light to advantageously provide the user with a visual indication that the USB flash drive apparatus is transferring data to at least discourage removal of the memory card from a host system during a memory transfer. *Id.*; MTI-1005, 4:67-5:2, 5:16-20, 6:21-31; MTI-1013, [0016], [0072]; MTI-1018, [0005], [0030]; MTI-1019, 3:1-3.

Accordingly, a POSITA would have found it obvious and would have been motivated to implement Tomio’s suggested memory apparatus with a USB connector for connecting the memory apparatus and the host, and with indicator

lights to provide a visual indication of the status of the memory apparatus. MTI-1003, ¶179; MTI-1005, 1:13-30, 4:67-5:2, 5:16-20, 6:21-31; MTI-1013, [0006]-[0010], [0016], [0072]; MTI-1017, 1:53-67; MTI-1018, [0005], [0030]; MTI-1019, 3:1-3. A POSITA would have viewed the implementation of Tomio's memory apparatus in a manner that applied Sukegawa's suggested connector configuration as merely the predictable result of combining known prior art elements according to known methods. *Id.*; *KSR*, 550 U.S. at 405 (2007); *Intel*, No. 22-1037 at 10-13. A POSITA would have had a reasonable expectation of success in doing so as such an implementation was well-known as demonstrated by Sukegawa and commonly utilized in similar memory apparatus. *Id.* A POSITA would have recognized that the above described modifications would have yielded predictable results, would have been within the ordinary level of skill of a POSITA, and would not have required undue experimentation. *Id.*

2. Claim 1

(a) Element 1[p]

Tomio-Sukegawa provides a "USB flash drive" which "is a small memory storage apparatus." MTI-1005, 1:38-42. Sukegawa's FIG. 1 shows a "USB memory apparatus 100," which is "an integrated flash drive apparatus shown with a USB connector shield case 120" that measures "12 millimeters (mm) wide±0.10 mm, 4.5 mm tall±0.10 mm, and a minimum of 11.75 mm deep." MTI-1005, 4:44-

48, 7:26-37. A POSITA would have found it obvious that Tomio-Sukegawa's flash drive is a portable memory apparatus. MTI-1003, ¶¶180-181; MTI-1013, [0004]; MTI-1012, [0004]-[0005].

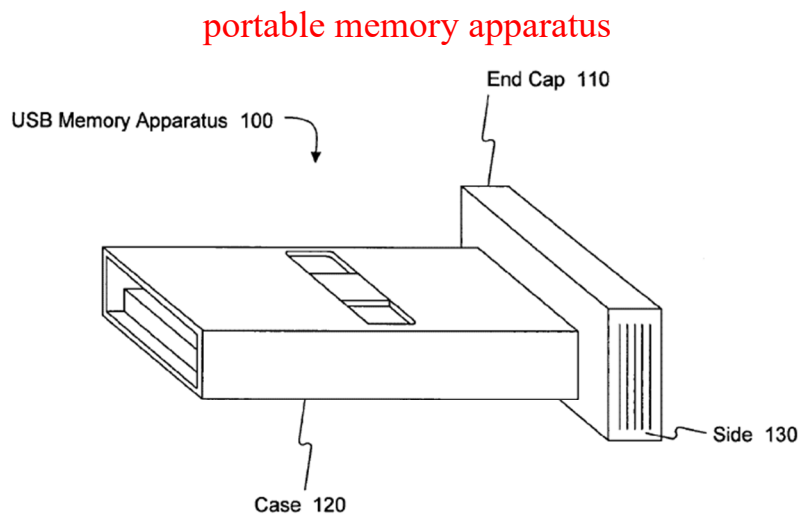


FIG. 1

MTI-1005, FIG. 1

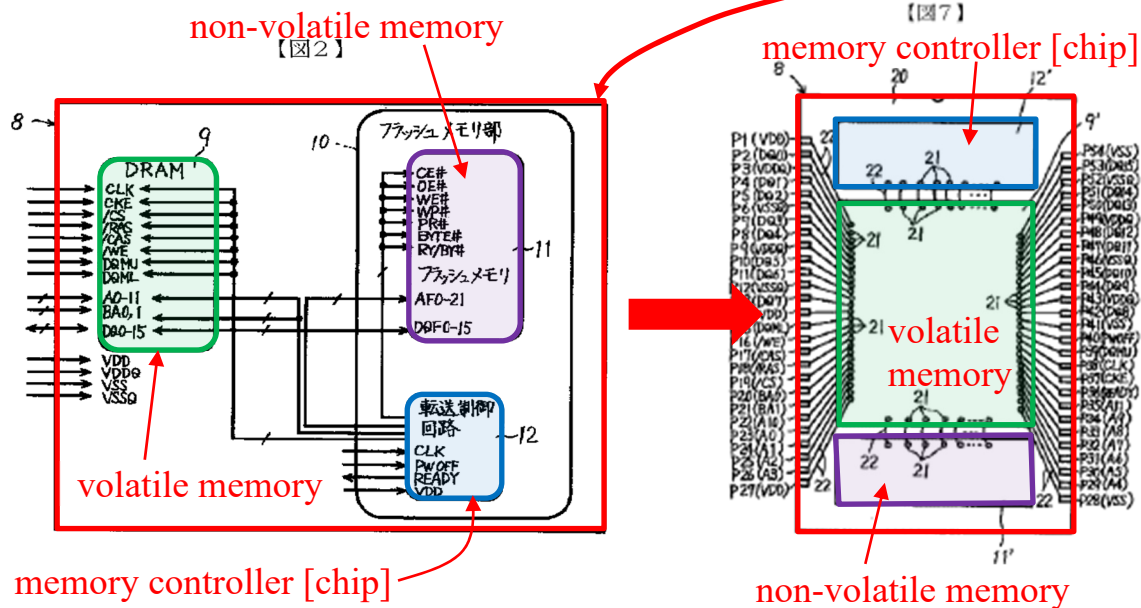
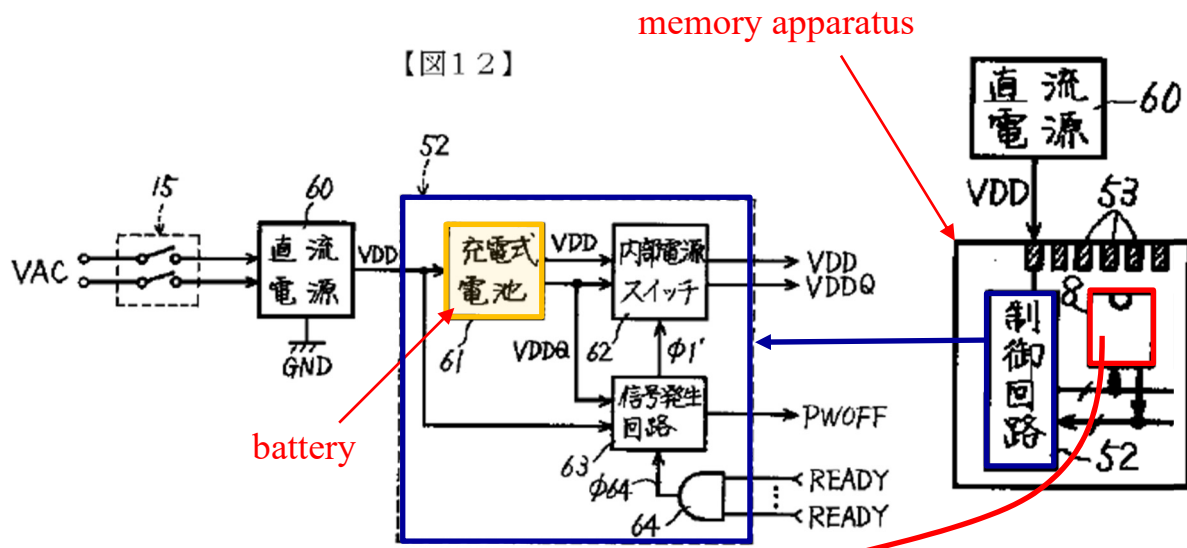
(b) Element 1[a]

Tomio-Sukegawa's USB flash drive includes "a USB connector shield case 120" that "extends from an overmold boot" and an end cap 110. MTI-1005, 4:44-66, 7:26-37. "The circuit components of the flash drive apparatus can be mounted within case 120 in various configurations." MTI-1005, 4:44-66, 5:20-24, 7:26-37, 8:6-9:31, FIGS. 5A-5H; MTI-1003, ¶¶182-183. A POSITA would have found it obvious that Tomio-Sukegawa's USB flash drive has a housing in the form of the

USB connector shield case 120, overmold boot, and end cap 110 that beneficially provides “a relatively low-profile, unobtrusive, and compact exterior for use with reduced size USB flash drive apparatus” within which the circuit components are mounted. *Id.*

(c) Elements 1[b]-1[d]

As discussed above (Section III.E.1), a POSITA would have found it obvious, from Tomio’s explicit teachings, to implement a memory apparatus with one semiconductor memory and a control circuit mounted on a substrate, as shown below. MTI-1006, [0018]-[0024], [0025]-[0026], [0028], [0030]-[0032], [0034]-[0035], [0043]-[0044], [0048], FIGS. 2, 7-9, claims 1-6 (claiming the elements of one semiconductor memory and a control circuit), [0045]-[0050] (describing the same). As discussed above (Ground 3A, 1[b]-1[d]), the semiconductor memory includes a DRAM 9/9’ (volatile memory) (green) coupled to a transfer control circuit 12/12’ (blue) and a flash memory 11/11’ (non-volatile memory) (purple) coupled to the transfer control circuit 12/12’ (blue), as shown below. MTI-1006, [0018], [0030]-[0031], [0034]-[0035], [0043].



MTI-1006, FIGS. 2, 7, 11, 12

(modified to show one semiconductor memory 8 and collated)

For a USB flash drive implementation, Sukegawa teaches that “[t]he circuit components of the flash drive apparatus can be mounted within case 120 in various configurations” and can be “implemented as one or more modules,” e.g., “three different modules.” MTI-1005, 4:44-66, 5:20-24, 5:29-37, 7:6-18, 7:26-37, 8:6-

9:31, FIGS. 5A-5H. A POSITA would have found it obvious to implement, in Tomio-Sukegawa's USB flash drive, the transfer control circuit (memory controller [chip]), the DRAM (volatile memory), and the flash memory (non-volatile memory) as one, two, or three modules that are mounted within the housing formed by the USB connector shield case 120, overmold boot, and end cap 110, as shown below, to provide a very small, inexpensive, portable and removable storage media. *Id.*; MTI-1003, ¶¶184-187. A POSITA would have been capable of employing ordinary creativity to carry out an implementation of the USB flash drive with the transfer control circuit (memory controller [chip]), the DRAM (volatile memory), and the flash memory (non-volatile memory) mounted within the housing in a manner necessary to achieve the advantages taught by Sukegawa by, for example, varying the size and shape of the housing to accommodate the electronic components. *Id.*; MTI-1013; MTI-1017; MTI-1018; MTI-1019; MTI-1020; *Facebook, LLC*, 973 F.3d at 1343. An example of an implementation of the USB flash drive with the memory control unit (memory controller [chip]), the SDRAM (volatile memory), and the flash memory (non-volatile memory) as three different modules mounted within the housing is shown below.

portable memory apparatus

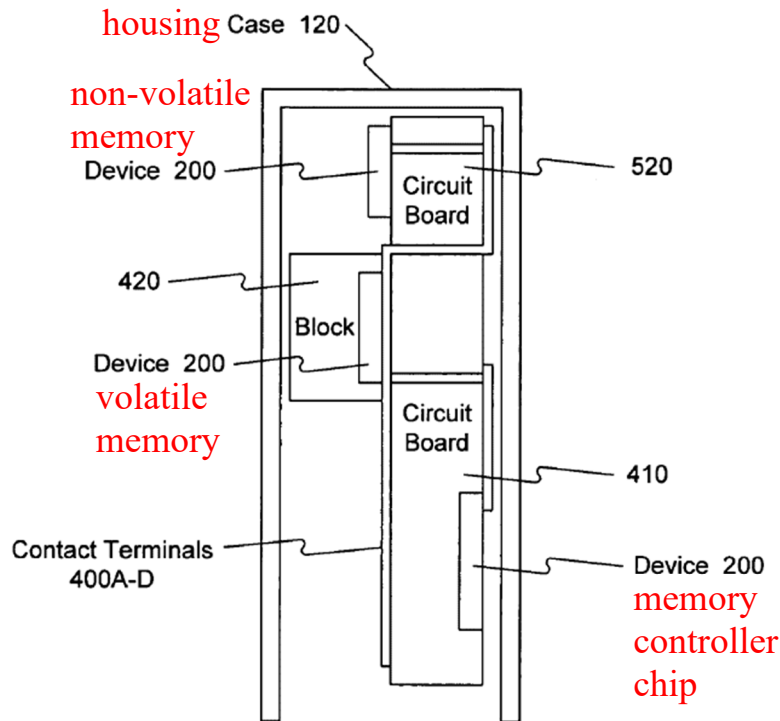
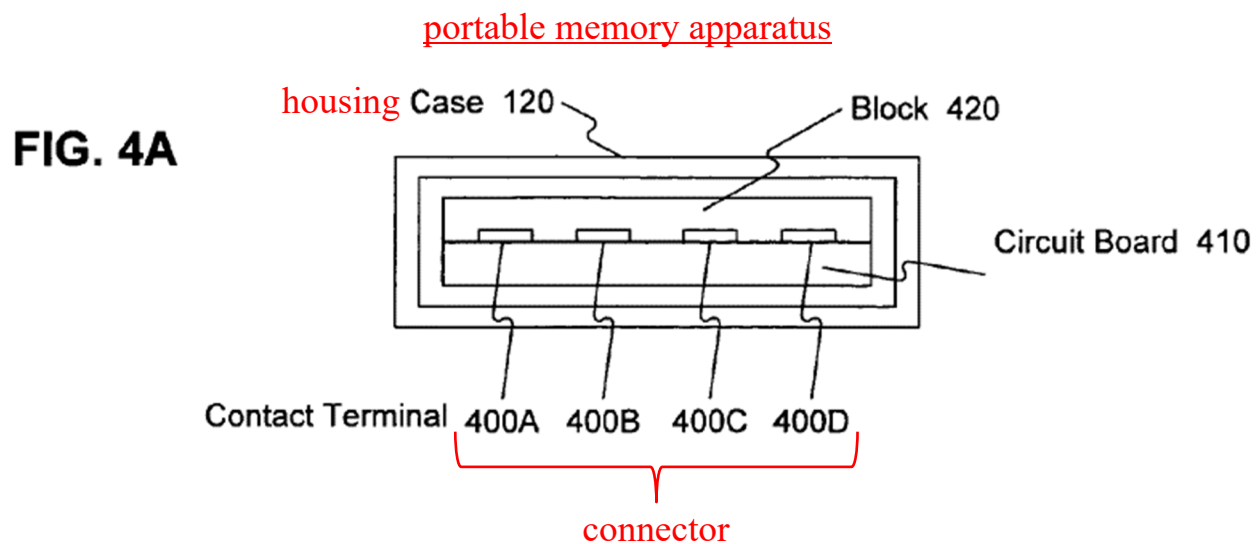


FIG. 5G
MTI-1005, FIG. 5G

(d) Element 1[e]

Tomio-Sukegawa's USB flash drive "interfaces with a host system through a USB connector." MTI-1005, 1:38-40. The USB connector includes a "set of contact terminals (shown in more detail in FIG. 4A-C)... disposed within the connector shield case 120... in a known configuration to line up with a mating USB connector" of a host system. MTI-1005, 4:54-57, 7:26-52. Accordingly, Tomio-

Sukegawa's USB flash drive (portable memory apparatus) has a USB connector that is position on the connector shield case 120 (forming the housing)¹⁴, as shown below, and that couples the USB flash drive to a host (computer system, *supra* Ground 3A, 1[e])) when the USB connector is plugged into the host. MTI-1003, ¶¶188-189; MTI-1013, [0090].



MTI-1005, FIG. 4A

(e) Element 1[f]

When Tomio-Sukegawa's USB flash drive is connected to the personal computer (computer system) via the USB connector (*supra* Ground 4A, 1[e]), the transfer control circuit (memory controller chip) copies data from the flash memory (non-volatile memory) to the DRAM (volatile memory), and the personal

¹⁴ See footnote 1.

computer accesses the data in the DRAM through the USB connector in a similar manner and for similar reasons as explained in Ground 3A, 1[f]. MTI-1003, ¶190; MTI-1006, [0019], [0022]-[0026], [0032], [0038].

3. Claims 2, 4, and 5

Supra Ground 3A, claims 2, 4, and 5. MTI-1003, ¶191.

4. Claim 3

Supra Ground 3A, claim 3. MTI-1003, ¶192.

5. Claim 6

Supra Ground 3A, claim 6. MTI-1003, ¶¶193-195.

6. Claim 7

Tomio-Sukegawa's USB flash drive includes "one or more lights that indicate connection to the host system, access to the apparatus memory or both." MTI-1005, 4:67-5:2, 5:16-20, 6:21-31. In Tomio-Sukegawa's USB flash drive, the lights would indicate when the flash memory is being or has been accessed, for example, when data stored in the DRAM (volatile memory) is being or has been transferred to the flash memory (non-volatile memory). MTI-1003, ¶196; MTI-1013, [0016], [0072].

7. Claim 9

Supra Ground 3A, 1[c]. MTI-1003, ¶197.

8. Claim 10

Supra Ground 4A, 1[e]; MTI-1003, ¶198.

9. Claims 11 and 14

Tomio-Sukegawa's USB flash drive has a USB connector shield case 120 that "extends from an overmold boot" and an end cap 110. MTI-1005, 4:58-66, 7:26-37. "The overmold boot is typically an injection molded thermoplastic insulator material with a minimum UL 94-VO rating." MTI-1005, 7:33-34. Based on a POSITA's general knowledge that the "injection molded thermoplastic insulator material with a minimum UL 94-VO rating" includes materials such as ABS, which possesses outstanding impact strength, a POSITA would have found it an obvious design choice to use ABS to form at least a portion of the housing (e.g., the overmold boot and end cap) of Tomio-Sukegawa's USB flash drive to beneficially provide an outer shell that has outstanding impact strength, toughness, and resistance to protect the components of the flash drive from damage due to mishandling, moisture, dust and debris, and electrostatic discharge. MTI-1003, ¶199; MTI-1014, 4; MTI-1015, 2; MTI-1011; MTI-1023, 10.

10. Claim 12

Tomio-Sukegawa's USB flash drive includes a DRAM chip 9', a flash memory chip 11', and a transfer control circuit chip 12' connected via pads 21 and bonding wires 22. MTI-1006, [0030]-[0031]; MTI-1005, 4:48-50, 6:42-7:18, 8:6-9:16, FIGS. 3, 5A-5H; *supra* Ground 3A, claim 12; MTI-1003, ¶¶200-201. A POSITA would have found it obvious that Tomio-Sukegawa's USB flash drive,

which includes DRAM, flash memory, and transfer control circuit on different silicon chips housed in a USB connector shield case 120 that “extends from an overmold boot” and an end cap 110, as shown below, does not have any moving parts. *Id.*; MTI-1004, [0124]; MTI-1005, 4:58-59, 7:26-32, FIG. 1; MTI-1012, [0005], [0031].

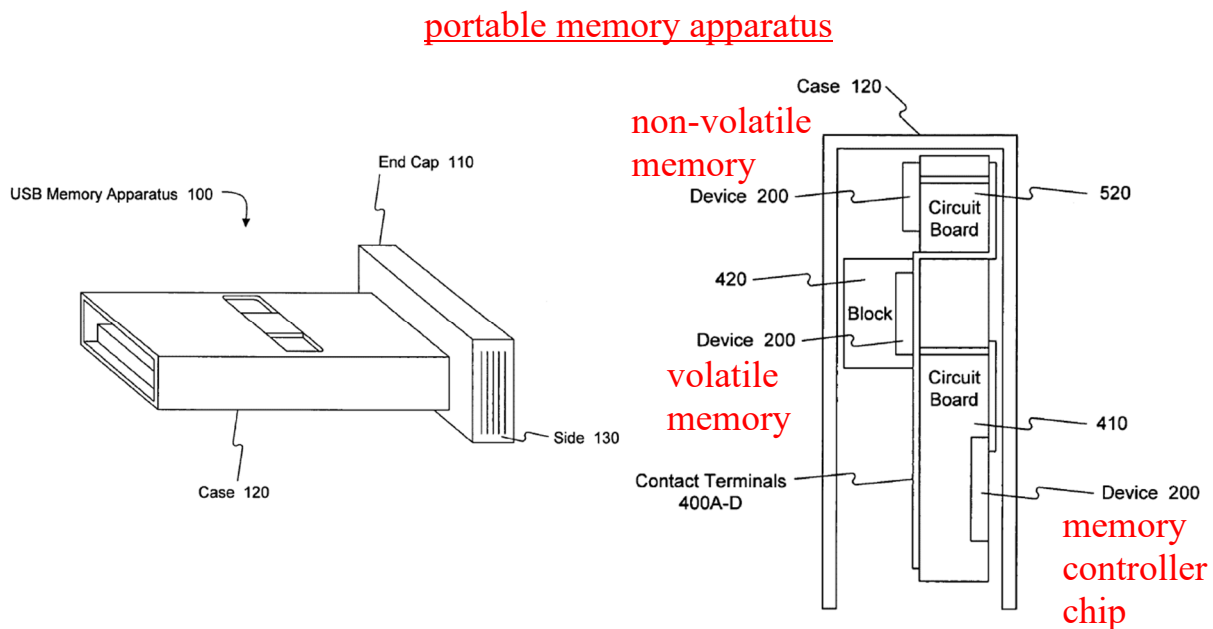


FIG. 1

FIG. 5G

MTI-1005, FIGS. 1, 5G

11. Claim 15

(a) Element 15[p]

Tomio-Sukegawa teaches a method as set forth below. MTI-1003, ¶202.

(b) Element 15[a]

Supra Ground 4A, 1[p] and 1[e]. MTI-1003, ¶203.

(c) Element 15[b]

Supra Ground 4A, 1[b], 1[c], 1[d]. MTI-1003, ¶204.

(d) Element 15[c]

Supra Ground 4A, 1[f]. MTI-1003, ¶205.

(e) Element 15[d]

Supra Ground 4A, 1[f]. MTI-1003, ¶206.

(f) Element 15[e]

Supra Ground 4A, claim 6. MTI-1003, ¶207.

12. Claim 16

Supra Ground 3A, claims 2 and 3. MTI-1003, ¶208.

13. Claim 17

Supra Ground 3A, claim 4. MTI-1003, ¶209.

14. Claim 18

Supra Ground 4A, claim 7. MTI-1003, ¶210.

F. GROUNDS 1C, 2C, 3B, and 4B—Claims 13 and 20 are obvious over Tsunoda, alone or with Sukegawa, Tomio, and Shigeo (GROUNDS 1C and 2C) and are obvious over Tomio, alone or with Sukegawa, and Shigeo (GROUNDS 3B and 4B)

1. Overview of Shigeo

Shigeo relates to preventing the loss of data stored in volatile memory when remaining battery power is low. MTI-1007, [0009]-[0012]; MTI-1003, ¶¶212-214.

In Shigeo, when information is stored in RAM, the capacity of the battery becomes low, and the contents of the RAM may become corrupted, the contents are automatically written and saved in flash memory, and data is directly written to flash memory without using the RAM “to minimize data loss even if the battery runs out during a writing operation.” MTI-1007, [0071], [0082], [0089]. When data is to be read, if the data is in RAM, it is read from RAM, but if the data is not in RAM, it is read from flash memory. MTI-1007, [0084]-[0085]. When the battery power has been restored by charging, the information saved in flash memory is read to the RAM and restored, and normal read/write processing is performed. MTI-1007, [0072], [0083].

2. Tsunoda-Tomio-Shigeo (GROUND 1C), Tsunoda-Sukegawa-Tomio-Shigeo (GROUND 2C), Tomio-Shigeo (GROUND 3B) and Tomio-Sukegawa-Shigeo (GROUND 4B) Combinations

As discussed above (Grounds 1A/3A, 1[f]), Tsunoda and Tomio both describe transferring data stored in flash memory to RAM when the memory apparatus first receives power from the computer system. MTI-1004, [0042]-[0043], [0048]-[0049], [0062], [0068], [0078], [0080]-[0084], [0093], [0096], [0099], [0131], [0139]-[0140], FIGS. 18, 23, FIG. 24 (4061-4062), FIG. 25 (4101-4105), FIG. 26 (4206); MTI-1006, [0022]-[0026], [0032]. In both Tsunoda and Tomio, data in RAM is stored in flash memory when the external power supply is

stopped or turned off. MTI-1004, [0042]-[0043], [0046]-[0047], [0062], [0068], [0078], [0085]-[0088], [0093], [0098]-[0099], [0104], [0112], [0133]-[0138], FIGS. 20-22, 24 (4063-4065), 25 (4107, 4109-4113), 26 (4206); MTI-1006, [0032]. In the event that the external power supply is abruptly stopped, Tomio's module includes a "rechargeable battery 61" that "continues to output direct current power supply potentials VDD and VDDQ for a predetermined period of time even when supply of the direct current power supply potential VDD from the direct current power supply 60 has been stopped." MTI-1006, [0039], [0027].

Shigeo explains that information stored in RAM "becomes corrupted" when the battery does not have enough power to power the RAM, and "is lost if enough power is not supplied" to the RAM "due to a decrease in the power supply capacity of the battery" and "the battery dies." MTI-1007, [0009]-[0010], [0061]. Shigeo thus provides techniques for preventing the loss of data stored in RAM when remaining battery power is low and reducing the amount of data loss if the battery dies during a writing operation. MTI-1007, [0009]-[0012]. A POSITA would have been motivated to apply the teachings of Shigeo to Tsunoda-Tomio's and Tomio's (each with or without Sukegawa) memory apparatus to prevent loss of the data stored in RAM and reduce data loss during a writing operation in the event that the external power supply is abruptly stopped and the battery does not have enough power to power the RAM and the flash memory for the writing of data to

the flash memory. MTI-1003, ¶¶215-216; MTI-1006, [0032], [0039], [0027]; MTI-1007, [0009]-[0012], [0061].

Tsunoda and Tomio expressly contemplate transferring data stored in the flash memory to RAM for faster access and transferring data stored in RAM to flash memory before power is turned off. MTI-1004, [0042]-[0043], [0046]-[0049], [0062], [0068], [0078], [0080]-[0088], [0093], [0096]-[0099], [0104], [0112], [0131], [0133]-[0140], FIGS. 18, 20-23, 24 (4061-4065), 25 (4101-4105, 4107, 4109-4113), FIG. 26 (4206); MTI-1006, [0004]-[0005],[0022]-[0024], [0028], [0032]. A POSITA implementing Tsunoda-Tomio's and Tomio's memory apparatus (each with or without Sukegawa) would have turned to examples of similar memory apparatus to identify suitable techniques for operating the memory module to prevent data loss. *Id.*; MTI-1003, ¶217. Shigeo provides suitable techniques for operating a memory apparatus to prevent data loss. MTI-1007, [0009]-[0012], [0061]. Shigeo's teachings enable implementation of a memory apparatus, such as that provided by Tsunoda-Tomio and Tomio (each with or without Sukegawa), so as to prevent loss of the data stored in RAM and reduce data loss during a writing operation in the event that the external power supply is abruptly stopped and the battery does not have enough power to power the RAM and the flash memory for the writing of data to the flash memory. MTI-1003, ¶217; MTI-1006, [0032], [0039], [0027]; MTI-1007, [0009]-[0010], [0061],

[0009]-[0012]. A POSITA would have been motivated to apply the teachings of Shigeo to Tsunoda-Tomio's and Tomio's memory apparatus (each with or without Sukegawa) to achieve these benefits. *Id.*

A POSITA would have viewed the implementation of Tsunoda-Tomio's and Tomio's memory apparatus (each with or without Sukegawa) in a manner that applied Shigeo's suggested techniques for operating the memory module to prevent data loss as merely the predictable result of combining known prior art elements according to known methods. *KSR*, 550 U.S. at 405 (2007); *Intel*, No. 22-1037 at 10-13; MTI-1003, ¶218. A POSITA would have had a reasonable expectation of success in doing so as such an implementation was well-known as demonstrated by Shigeo and commonly utilized in similar memory apparatus. *Id.* A POSITA would have recognized that the above described modifications would have yielded predictable results, would have been within the ordinary level of skill of a POSITA, and would not have required undue experimentation. *Id.*

3. Claims 13 and 20

As discussed above (Grounds 1A/3A, 1[f]), Tsunoda and Tomio both describe transferring data stored in flash memory to RAM when the memory apparatus first receives power from a host computer system. MTI-1004, [0042]-[0043], [0048]-[0049], [0062], [0068], [0078], [0080]-[0084], [0093], [0096], [0099], [0131], [0139]-[0140], FIGS. 18, 23, FIG. 24 (4061-4062), FIG. 25 (4101-

4105), FIG. 26 (4206); MTI-1006, [0022]-[0024], [0032]. Also discussed above (Grounds 1B/2B/3A, claim 4), Tomio describes that “control circuit 52 includes a rechargeable battery 61” that “is charged with the direct current power supply potential VDD from the direct current power supply 60 and outputs direct current power supply potentials VDD and VDDQ.” MTI-1006, [0039]. As shown in Tomio’s FIGS. 11 and 12, “control circuit 52 receives direct current power supply potential VDD from a direct current power supply 60 outside of the module 51 via an input terminal 53” (of the connector). MTI-1006, [0038], [0027].

A POSITA would have found it obvious that if the external power supply is abruptly stopped and the battery is not sufficiently charged and does not have enough power to power the RAM and the flash memory for the writing of data to the flash memory, the data stored in the RAM would be lost. MTI-1003, ¶¶219-221; MTI-1004, [0075]; MTI-1006, [0002], [0032], [0039], [0027]; MTI-1007, [0009]-[0012], [0061], [0009]. To address such a problem, Shigeo teaches that when information is stored in RAM, the capacity of the battery becomes low, and the contents of the RAM may become corrupted, the contents are automatically written and saved in the non-volatile memory, and data is directly written to the non-volatile memory without using the RAM “to minimize data loss even if the battery runs out during a writing operation.” MTI-1007, [0071], [0082], [0089], [0074]. When data is to be read, if the data is in RAM, it is read from RAM, but if

the data is not in RAM, it is read from non-volatile memory. MTI-1007, [0084]-[0085]. Accordingly, in the Tsunoda-Tomio-Shigeo and Tomio-Shigeo (each with or without Sukegawa) memory apparatus, when the battery is not sufficiently charged and the host (computer system) accesses the memory apparatus, the host reads/writes data from/to the flash memory (non-volatile memory) through the terminals (of the connector), until the battery (internal power source) recharges to sufficient power to transfer data from RAM to the flash memory if the memory apparatus is unplugged from the host before data in the RAM is transferred to the flash memory. MTI-1007, [0036], [0059], [0066], [0071], [0082], [0084]-[0085], [0089]; MTI-1003, ¶¶222-223.

Shigeo also discloses that when the battery power has been restored by charging, the information saved in flash memory is read to the RAM and restored, and normal read/write to RAM is performed. MTI-1007, [0072], [0083]. As such, each of Tsunoda-Tomio-Shigeo and Tomio-Shigeo (each with or without Sukegawa) renders obvious that the memory controller chip copies data from the flash memory (non-volatile memory) to RAM (volatile memory) after the battery (internal power source) has been recharged through the terminal (of the connector) to where the battery has sufficient power to transfer data from RAM to said flash memory if the memory module is unplugged from the computer system before data in the RAM is transferred to the flash memory. MTI-1003, ¶224.

IV. THE BOARD SHOULD CONSIDER THE PETITION ON THE MERITS AND NOT EXERCISE ITS DISCRETION TO DENY INSTITUTION

A. The *General Plastic* Factors Weigh Against Exercising Discretion To Deny Institution

The '527 patent was the subject of IPR2022-00255 (filed 12/6/2021, instituted 6/8/2022, terminated 10/5/2022), IPR2022-00437 (filed 1/14/2022, instituted 7/29/2022, terminated 1/3/2023), IPR2022-00762 (filed 3/25/2022, terminated 10/5/2022), and IPR2022-00765 (filed 3/25/2022, terminated 10/5/2022) involving different petitioners, separately and independent of Micron. These proceedings were terminated due to settlement and are no longer pending. The present Petition relies on references not asserted in the previous petitions.

In *General Plastic Industrial Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357—01361, Paper 19 at 9-10 (Sept. 6, 2017) (PTAB Precedential), the Board identified seven factors that inform application of discretionary institution denials under 35 U.S.C. §314(a). Evaluation of these factors weighs against using the Board's discretion to deny this petition without consideration on the merits, especially where the present petitioner is different from the petitioner in the earlier-filed IPR. See, e.g., *Acronis, Inc. v. Realtime Data LLC*, IPR2018-00706, Paper 11, 15-16 (Oct. 1, 2018) (citing *Alcatel-Lucent USA Inc. v. Oyster Optics, LLC*, IPR2017-02146, Paper 12, 12 (Feb. 28, 2018) ("Once resolution of

factor 1 indicates that Petitioner had not previously filed a petition against the same patent, factors 2–5 bear little relevance unless there is evidence in the record of extenuating circumstances.”).

1. Factor 1: Micron and the previous petitioners are separate and distinct parties

The first factor weighs heavily in favor of considering this Petition on the merits because Micron, the Petitioner here, has not previously filed any petition challenging the ’527 patent. As the Board has explained, concerns of strategically staging petitions “have less persuasive value when the second petition is filed by a different petitioner.” *Toshiba America Information Systems v. Wallex Microelectronics LTD.*, IPR2018-01538, Paper 11, 20 (March 5, 2019); *Acronis*, Paper 11, 15-16. Not only is there no control or cooperation in the IPRs between Petitioner and the earlier petitioners, but they remain “distinct parties, with ultimately distinct interests, and distinct litigation strategies,” and are “often competitors in the marketplace.” *Id.* at 22. Deciding this petition on the merits would not be unfair to Patent Owner, but exercising discretion to deny consideration of the only petition Petitioner advanced would be unfair to Petitioner, especially considering that the prior cases brought by other petitioners have been terminated before a final written decision.

2. Factors 2, 4, and 5: Micron filed this Petition promptly after searching revealed new prior art

Factors 2, 4, and 5 do not weigh against consideration of this Petition.

Petitioner learned of Tsunoda, Sukegawa, Tomio, and Shigeo through prior art searching conducted in November and December of 2022. Upon discovering these references, Petitioner worked diligently to prepare and file the present Petition.

3. Factor 3: This Petition does not implicate road-mapping concerns

The third factor does not weigh against consideration of this Petition because Petitioner did not delay filing this petition for the purpose of using an earlier proceeding as a roadmap. Because the present Petition relies on references not asserted in the previous petitions, Petitioner derived no benefit from the earlier petitions.

4. Factors 6 and 7: Institution would efficiently promote patent quality

The sixth and seventh factors weigh in favor of considering this petition when considering the limited resources of the Board, balanced against the usefulness of invalidating patents in view of the relevant prior art cited here. Indeed, the previous IPR terminated due to settlement after the Board instituted review but before it analyzed on the merits in a final written decision, so the present Petition is now the only IPR before the Board, thus providing for efficient resolution of the unpatentability of the '527 patent within one year after institution.

This is especially the case where there is no evidence of prejudicial “road-mapping” or other gamesmanship by Petitioner that would warrant the punitive measure of denial without consideration on the merits, where there is no other IPR pending against the ’527 patent.

The public interest also weighs in favor of considering this Petition on the merits in comparison to the highly pertinent prior art combinations of references that were never previously considered by the Office. There is no prejudice to Patent Owner here because this petition and the earlier-filed petitions against the ’527 patent are “a directed result of [Patent Owner’s] own litigation activity.” *Samsung Electronics America, Inc. et al v. Uniloc 2017 LLC*, IPR2017-01797, Paper 8, 33 (February 6, 2018).

Because Petitioner filed a single petition against the ’527 patent and has a meaningful due process interest to be heard in this forum on the merits in light of the termination of the earlier IPR proceedings against the ’527 patent, the *General Plastic* factors weigh in favor of instituting IPR.

Additionally, while concurrent district court litigation involving the ’527 patent is ongoing, it remains at an early phase, with the complaint having only been filed in August 2022. Petitioner has worked diligently to identify and apply prior art discussed herein to file the Petition well before its statutory deadline. Additionally, Dr. Liu is the expert for Petitioner in the present IPR proceeding, and

provides significant evidence not of record in the district court or the prior IPRs.

B. The *Fintiv* Factors Weigh Against Exercising Discretion To Deny Institution

The PTAB considers a set of non-exclusive factors (the *Fintiv* factors) in determining whether to institute an IPR proceeding where there is parallel district court litigation. *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (designated precedential May 5, 2020). On June 21, 2022, Director Vidal issued “binding agency guidance” entitled “Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation.” MTI-1025 (hereinafter the “Interim Guidance”). This Interim Guidance presents “several clarifications... to the PTAB’s... application of *Fintiv* to discretionary institution where there is parallel litigation.” *Id.*, 2.

One clarification provided by the Interim Guidance specifies the effect of particular types of stipulations presented by petitioners on the Board’s application of the *Fintiv* framework. *Id.*, 3, 7-8. In particular, the Interim Guidance unequivocally states that “***the PTAB will not discretionarily deny institution*** of an IPR or PGR in view of parallel district court litigation where a petitioner stipulates not to pursue in a parallel district court proceeding the same grounds as in the petition or any grounds that could have reasonably been raised in the petition.” *Id.*, 7 (emphasis added) (citing *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019,

Paper 12 (PTAB Dec. 1, 2020)). In the present case, Petitioner presents a stipulation not to pursue in the parallel district court proceeding the same grounds as in the present Petition or any grounds that could have reasonably been raised in the present Petition. *See* MTI-1026. Accordingly, based on the Interim Guidance, institution of the present Petition ***should not*** be discretionarily denied in view of the parallel district court proceeding. *See* MTI-1025, 7.

C. The *Becton, Dickinson* Factors Weigh Against Exercising Discretion To Deny Institution

Although petitions based on different prior art references were previously filed in IPR2022-00255, IPR2022-00437, IPR2022-00762, and IPR2022-00765 and instituted in IPR2022-00255 and IPR2022-00437, they were terminated due to settlement. The Board has already determined that institution of a petition challenging validity of the '527 patent was warranted; Patent Owner evaded final decisions on unpatentability through settlement. Petitioner's filing of the present Petition after those earlier petitions is simply the product of Patent Owner's delay in suing Petitioner such that any prejudice to Patent Owner is a consequence of its litigation choices.

V. CONCLUSION

As demonstrated herein, the Challenged Claims are unpatentable. Accordingly, Petitioner respectfully requests that the Board institute IPR.

VI. PAYMENT OF FEES

Petitioner authorizes charge of fees to Deposit Account 06-1050.

VII. MANDATORY NOTICES UNDER 37 C.F.R § 42.8(a)(1)

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)

Micron Technology, Inc. is the real party-in-interest. No other parties had access to or control over the present Petition, and no other parties funded the present Petition.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

Sonrai Memory Limited (“Sonrai”)—the alleged Patent Owner—filed a complaint on August 16, 2022 in the U.S. District Court for the Western District of Texas (Case No. 6:22-cv-00855) against Micron asserting the ’527 patent. The complaint was served on August 17, 2022.

Sonrai also filed complaints alleging infringement of the ’527 patent by other parties: Kingston Technology Company, Inc. et al. (W.D. Tex. 6:21-cv-01284 transferred from C.D. Cal. 8:21-cv-01039); Western Digital Technologies, Inc. (W.D. Tex. 6:21-cv-01168; C.D. Cal. 8:21-cv-01040); KIOXIA Corporation (W. D. Tex. 6:21-cv-00400); and Dell Technologies, Inc. (W.D. Tex. 6:21-cv-00361; W.D. Tex. 6:21-cv-00487; W.D. Tex. 6:22-cv-00188). Micron is not a real party-in-interest to any of these above-listed district court proceedings. Also, none of the parties in these district court proceedings is a real party-in-interest in the

proceedings involving Micron or in privity with Micron. *Taylor v. Sturgell*, 553 US, 890 (2008).

Other petitioners have filed IPR proceedings challenging claims of the '527 patent including: Samsung Electronics Co., Ltd. (IPR2022-00762, IPR2022-00765); Kingston Technology Company, Inc., and Kingston Technology Corporation (IPR2022-00437); and Kioxia Corporation, Kioxia America, Inc., Western Digital Technologies, Inc., and Dell Technologies, Inc. (IPR2022-00255). These IPR proceedings have been terminated. Micron was not a real party-in-interest to these above-listed IPR proceedings. Also, none of the parties in the earlier IPR proceedings is a real party-in-interest in this proceeding or in privity with Micron.

C. Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel.

Lead Counsel	Backup counsel
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D. Service Information

Please address all correspondence and service to the address listed above.

Petitioner consents to electronic service by email at IPR36144-0035IP1@fr.com.

Respectfully submitted,

Dated: May 8, 2023

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CERTIFICATION UNDER 37 CFR § 42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter partes* Review totals 13,996 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated: May 8, 2023

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on May 8, 2023, a complete and entire copy of this Petition for *Inter partes* Review and all supporting exhibits were provided via USPS, to the Patent Owner by serving the correspondence address of record as follows:

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