

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.
Petitioner,

v.

SONRAI MEMORY LIMITED,
Patent Owner

IPR2021-01561
Patent No. 6,724,241

**DECLARATION OF DR. MICHAEL C. BROGIOLI IN SUPPORT OF
PATENT OWNER'S RESPONSE**

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I, Michael C. Brogioli, PhD, hereby declare as follows:

I. INTRODUCTION

1. I am over the age of eighteen (18) years and otherwise competent to make this declaration.

2. I have been retained as an expert witness on behalf of Sonrai Memory Limited (“Sonrai”) for the above-captioned *inter partes* review (“IPR”). I understand that the petition for *inter partes* review involves U.S. Patent No. 6,920,527 (“the ’527 Patent”).

3. I make this declaration based on my personal knowledge, educational background and training, consideration of the materials I discuss herein, and my expert opinions.

4. I am being compensated at a rate of \$700 per hour for my time in this matter. My compensation does not depend on the outcome of this proceeding, and I have no financial interest in its outcome.

5. In preparing this Declaration, I have reviewed and considered the ’527 Patent, the ’527 Patent’s prosecution history, the Petition, Dr. Liu’s declaration submitted in this proceeding, and each document cited in my declaration.

II. BACKGROUND AND QUALIFICATIONS

6. My qualifications for forming the opinions given in this declaration are summarized here and are addressed more fully in my curriculum vitae, which is submitted as Exhibit 2013. That exhibit also includes a list of my publications.

7. I am currently an Adjunct Professor of Electrical and Computer Engineering at Rice University in Houston, TX, teaching Ph.D. candidate level courses in wireless telecommunications, embedded computing software, embedded computing hardware, and software/hardware design. I have held this position since July 2009. I am also currently the Managing Director of Polymathic Consulting in Austin, TX, a company that advises a variety of clients on engineering, research and development, intellectual property, and other technical leadership matters, and I have held this position since October 2011.

8. I am a named inventor on multiple issued and pending patent applications. The subject matter of these applications includes, but is not limited to, embedded processing, edge computing, and various aspects of distributed systems including computation, interconnectivity and hardware/software design and implementation.

9. From November 2009 to October 2011, I was Chief Architect, Senior Member Technical Staff at Freescale Semiconductor in Austin, TX (formerly Motorola), responsible for management of technology, engineering roadmaps,

design lead on compiler infrastructure and optimizations for mobile and embedded computing solutions including the technologies involved in this matter. From 2008 to 2009, I was Senior Engineer working with high performance compiler design and next generation baseband compiler design and next generation baseband microprocessor and microcontroller architecture at Freescale Semiconductor in Austin, Texas.

10. From June 2006 to August 2007, I worked as the Technical Co-Founder of Method Seven LLC, in Boston, MA, working with high performance software and hardware systems architecture. I am currently the co-founder, co-inventor, and Chief Technology Officer of Network Native, an Internet of Things hardware and software company. I have also served on multiple advisory boards for technology companies over the past 10 years.

11. While at Rice University, I developed various computer architecture designs. For example, from 2002 to 2004, I developed Spinach, a simulator design toolset for modeling programmable network interface architectures, which models system components common to all programmable computing environments as well as components specific to embedded. From 2004 to 2009, I developed Spinach DSP-FPGA, a modular and composable simulator design infrastructure for programmable and reconfigurable embedded SOC architectures specifically targeting mobile, embedded and portable computing devices. From 2005 to 2009, I

developed and published a retargetable compiler infrastructure for software and systems related to mobile and embedded computing technologies. Many of these tools have been used at U.S. universities in the area of electrical and computer engineering research.

12. I am recognized as an expert in the field of computer architecture, computer hardware and computer software systems as they relate to the subject matter at hand. I am a member of the Institute of Electrical and Electronics Engineers (IEEE). I am currently the Program Chair of Design Automation Conference in the areas of Embedded and Wireless Solutions. I have been a Program Committee member for the IEEE and ACM Design Automation Conference from 2011 to the present, as well as other IEEE and ACM conferences. I have published, co-published and contributed to numerous works on wireless and mobile computing, sensor technologies, GPU Architecture, software optimizations, signal processing systems, digital signal processing and related architectures, and low power computing, among other topics.

13. I have previously served as an engineering consultant and testifying witness on matters related to, and including power circuits, voltage regulators, and power management in computer system hardware and software. This experience is encompassed in my work in academia and as a faculty member, my time in

industry as a system designer and architect, as well as my work as an engineering consultant and expert witness over the past 15 years.

14. Over the past 15+ years, I have authored numerous peer reviewed publications in the area of embedded and high performance computing, interconnect technologies, memory system technologies and optimization at the hardware and software design level. I have also been a committee member, and chair of Design Automation Conference in areas of technology related to the '680 Patent, often reviewing and vetting submissions from major industry players in the design and architectural issues related to various technologies at issue in this matter.

15. During my tenure at Freescale Semiconductor, I was in charge of system developer tools for baseband processor design, both in the hardware and software spaces. This work included hardware and software design issues of next generation wireless networking equipment, including system level programming models, interconnect technology, heterogeneous computing, various hardware acceleration technologies and related components.

16. My current curriculum vitae, provided in Exhibit 2002, contains more information on my background and experience, as well as the cases in which I have served as an expert witness the past four years.

17. No part of my compensation is contingent upon the outcome of this proceeding. I have no other interests in this proceeding or with any of the parties.

III. LEGAL PRINCIPLES

A. Claim construction

18. I understand that the first step in performing a validity analysis of the patent claims is to interpret the meaning and scope of the claims by construing the terms and phrases found in those claims. I understand that the appropriate construction of a claim term is its ordinary and accustomed meaning as understood by one of ordinary skill in the art at the time of the invention in the context of the entire patent.

19. I understand that standard for claim construction in an *inter partes* review is the same standard as is applied in district court proceedings.

20. I understand that a determination of the meaning and scope of the claims is a matter of law. I have been informed that to determine the meaning of the claims, one should consider the intrinsic evidence, which includes the patent's claims, written description, and prosecution history.

B. Burden of Proof

21. I understand that in an *inter partes* review, the petitioner has the burden of proving unpatentability by a preponderance of the evidence.

C. Anticipation

22. I have been instructed by counsel and understand that a reference is anticipated if a single prior art reference discloses each and every claim element,

either explicitly or inherently, as arranged in the same way as in the claim. I understand that where even one claim element is not disclosed in a reference, a contention of anticipation fails.

23. I further understand that when a reference fails to explicitly disclose a claim element, that reference inherently discloses that element only if the reference must *necessarily* include the undisclosed claim element.

D. Obviousness

24. I have been instructed by counsel and understand that a combination of prior art references may render a claim obvious if, at the time of the invention, a person of ordinary skill in the art would have selected and combined those prior-art elements in the normal course of research and development to yield the claimed invention.

25. I understand that in an obviousness analysis, one should consider the *Graham* factors: the scope and content of the prior art; the differences between the claimed inventions and the prior art; the level of ordinary skill in the art; and certain secondary considerations, identified below. I further understand the obviousness analysis is to be performed on a claim-by-claim basis. I understand that a person of ordinary skill in the art is a person of ordinary creativity, not an automaton.

26. I have been instructed by counsel and understand that obviousness requires more than a mere showing that the prior art includes separate references covering each separate limitation in a claim under examination. I understand obviousness requires the additional showing that a person of ordinary skill at the time of the invention would have been *motivated* to combine those references in a manner that would include all limitations of the challenged claim, and, in making that combination, a person of ordinary skill in the art would have had a *reasonable expectation of success*.

27. I also understand that an obviousness analysis must be conducted with awareness of the distortion caused by hindsight bias and with caution of arguments reliant upon *ex post* reasoning. For instance, I understand that when considering obviousness, I should put myself in the position of a person of ordinary skill in the field at the time of the invention, rather than considering new information that is known today but was not known before the priority date of the challenged patent.

28. In particular, I understand that it is improper to use the challenged patent's disclosure or invention as a roadmap to find its prior-art components, because such an approach discounts the value of combining various existing features or principles in a new way to achieve a new result.

IV. PERSON OF ORDINARY SKILL IN THE ART

29. Dr. Liu states that “a person of ordinary skill in the art (‘POSITA’) at the time of the earliest possible priority date of the ’527 patent would have had a Bachelor of Science in electrical engineering, computer engineering, computer science, or a related discipline, with at least 2 years of experience in a field related to data storage and electronic memory devices.” Ex. 1003 ¶ 27.

30. In my opinion, a POSITA would have had at least a Bachelor of Science in electrical engineering, computer engineering, computer science, or a related discipline, with at least two years of relevant experience in a field related to data storage and electronic memory devices. A person with more education, such as a doctorate in electrical engineering, computer engineering, computer science, or a related discipline, would also qualify as a hypothetical POSITA in lieu of fewer years of work experience.

V. CLAIM CONSTRUCTION

31. Dr. Liu does not offer any opinion as to the claim construction of any term in the challenged claims of the ’527 patent. However, Dr. Liu does acknowledge that the scope of the terms “portable” and “housing” are disputed between the parties. Dr. Liu says that “Patent Owner identifies Petitioner’s memory devices have a M.2 form factor (a specification for internally mounted computer cards) as allegedly infringing claims of the ’527 patent” and that he

“address[es] claims 1-6, 9, 12, and 15-17 under the scope of these claims terms advanced by Patent Owner in its complaint for infringement.” Ex. 1003 ¶140. Dr. Liu does not explain his interpretation of “the scope of these claim terms advanced by Patent Owner in its complaint for infringement.”

32. The word “portable” appears only three times in Patent Owner’s complaint for infringement. *See* Ex. 1021 at 3. The first instance is a recitation of the title of the ’527 patent (“Portable RAM drive”), and the other two instances are used in a list of products that includes “Crucial X8 Portable SSD” and “Crucial X6 Portable SSD.” *See id.* The word “housing” does not appear in Patent Owner’s complaint for patent infringement. Accordingly, I disagree with Dr. Liu that Patent Owner’s complaint for infringement advances any position as to the scope of the terms “portable” or “housing.” Because Dr. Liu offers no explanation as to the scope of the terms “portable” or “housing” that he applies, I am not able to opine on whether or not the meaning he applies to these two terms is consistent with how these terms would be understood to a POSITA in light of the ’527 specification and file history.

33. A POSITA would not consider a memory module like the one disclosed in Tomio to be a portable memory device in the context of the specification and claims the ’527 Patent. The memory module in Tomio is not designed to be plugged and unplugged.

VI. TSUNODA DOES NOT RENDER OBVIOUS ANY OF CLAIMS 1, 6, 9, 11-12 OR 14-15 OF THE '527 PATENT.

34. The Tsunoda reference does not render independent claims 1 and 15 obvious. Tsunoda's first embodiment is an internal memory apparatus communicating with a CPU or ASIC in an information terminal through a synchronous DRAM interface. Ex. 1004 ¶¶ [0038]-[0039]. Tsunoda's first embodiment does not disclose a portable memory apparatus that would function correctly if unexpectedly disconnected or uncoupled from a host. A POSITA would understand that features of this embodiment, such as Tsunoda's processing from a start of power supply to a stop of power supply, would have to be reimplemented for a portable memory apparatus. *See, e.g.*, Ex. 1004 ¶¶ [0080], [0093], Fig. 25.

35. Tsunoda's second embodiment includes both a MultiMediaCard (MMC) interface and a Synchronous DRAM interface. Ex. 1004, [0113], Fig. 9. Tsunoda's second embodiment is also not a portable MultiMediaCard but is instead a modification of Tsunoda's first embodiment that adds a MMC interface and a MMC interface control unit. *Compare* Ex.1004, Fig. 1 *and* Fig. 9. *See also Id.*, Fig. 10. A POSITA would not have understood that Tsunoda's second embodiment with an SDRAM interface was a portable memory apparatus.

36. The variations within the second embodiment disclosed by Tsunoda of adding either an SD card interface (Ex. 1004, Fig. 11) or a memory stick (*Id.*, Fig. 12), instead of MMC interface 907, along with an SDRAM interface, would still include an SDRAM interface. A POSITA would not have understood that any of the disclosed alternatives to Tsunoda's second embodiment that retained an SDRAM interface were a portable memory apparatus.

37. A POSITA would not have combined the teachings of Tsunoda and Sukegawa. A POSITA would have known that Tsunoda's teachings of additional components were incompatible with Sukegawa's teachings of a minimally sized flash drive that should be small enough to fit in a USB connector shield.

38. Tsunoda's Fig. 13 embodiment is not compatible with a portable memory device because it teaches using an SDRAM interface to connect to the host, and a POSITA would understand that an SDRAM interface is not a portable memory apparatus interface.

39. Tsunoda's third embodiment utilizes a MultiMediaCard without an SDRAM interface (Ex. 1004, Fig. 14), but it does not disclose or suggest copying data from the flash memory to the SDRAM when the MultiMediaCard is coupled to the host system. Tsunoda's description of copying data from the non-volatile memory to the volatile memory as part of a power up sequence that only applies

when there is an SDRAM compatible interface. *See, e.g.*, Ex. 1004 ¶¶ [0080], [0093], Fig. 25.

40. In Tsunoda, the triggering event for when data is copied from the non-volatile memory to the volatile memory is powering up, which is detected using voltage detector 4032 in a control unit 4030. Ex. 1004 ¶¶ [0067]-[0068]. A POSITA would understand from Tsunoda's description of the third embodiment that Tsunoda's it does not include a Control Unit with a Control Register and a Voltage Detector intended for use with a SDRAM compatible interface. *See* Ex. 1004 ¶¶ [0054]-[0068], Fig. 14, Fig. 24 (Control Unit 4030 including Control Register 4031 and Voltage Detector 4032).

41. A POSITA would not have found it obvious to expand or augment the circuitry of an SDRAM compatible interface control unit to any of the embodiments within Tsunoda that did not already include an SDRAM interface. SDRAM memory devices, and memory modules which are comprised of multiple memory devices, are design to talk to host side memory controller. Such a memory controller and SDRAM interface require complex and costly circuitry that is tailed to support the highly parallel signaling interfaces and protocols of SDRAM memory technology, and the robust control, data rates, and operation of SDRAM. These protocols are different than those of solid-state memory such as that of

Tsunoda, for which the MMC controller in Tsunoda is tailored for their respective operation.

42. Tsunoda discloses that “[p]referably the SDRAM compatible interface 4001 for interconnecting the host 4040 and the control unit 4030 has compatibility not only between the SDRAM terminal group of, for example JEIDA standard and electric characteristics, but also between the SDRAM terminal group and a package size of the memory apparatus 4000, a terminal group size of for example a pin or a solder ball disposed on the package of the memory apparatus 4000, terminal group disposition or the like.” Ex. 1004 ¶ [0058]. A POSITA would have understood that an MMC interface would not be capable of providing the required SDRAM compatible interface utilized in Tsunoda. Thus, I disagree with Dr. Liu’s assertion that a POSITA would have found it obvious to apply “any” of Tsunoda’s features to Tsunoda’s third embodiment. Ex. 1003 ¶¶ 71-73. Moreover, a POSITA would not have found it obvious to add the additional circuitry of the SDRAM compatible interface control unit to any embodiments in Tsunoda that did not include an SDRAM interface such as, for example, the MMC embodiment of Figure 14.

43. For these reasons, Tsunoda does not disclose, teach or suggest the limitations of claim 1 of “a portable memory apparatus” ... “wherein, when said connector couples said portable memory apparatus to said computer system, said

memory controller chip copies data from said non-volatile memory to said volatile memory.”

VII. TSUNODA IN VIEW OF TOMIO DOES NOT RENDER OBVIOUS ANY OF CLAIMS 2-5 OR 16-17.

44. In support of Petitioner’s Ground 1B, based on Tsunoda in view of Tomio, and Ground 2B, based on Tsunoda-Sukegawa in view of Tomio, Dr. Liu opines that “[a] POSITA would have been motivated to apply the teachings of Tomio to Tsunoda’s and Tsunoda-Sukegawa’s memory apparatus to provide a memory apparatus with a rechargeable battery that continues to supply power long enough for the memory controller to copy data from volatile memory to nonvolatile memory in the event that the external power to the memory apparatus is abruptly stopped.” Ex. 1003 ¶ 129. Dr. Liu also says “a POSITA would have found it obvious and would have been motivated to implement Tsunoda’s and Tsunoda-Sukegawa’s memory apparatus with a rechargeable battery that supplies power and functionality in the memory controller for transferring data from volatile memory to nonvolatile memory after the external power supply has been stopped or turned off based on Tomio’s teachings.” ¶ 132. I disagree, as explained below.

45. Tsunoda discloses issuing a busy signal that prevents the host from stopping supply of power to the memory apparatus until the busy signal is released

by the memory apparatus. *Id.* [0085]-[0087]. Because Tsunoda discloses a method to ensure data transfer is completed before power is shut off, an internal power source to ensure that the memory apparatus can transfer the data from the volatile memory to the non-volatile memory would unnecessarily add components and complexity to the memory apparatus. A POSITA would not have been motivated to add an internal power supply to the memory apparatus of Tsunoda. To begin, Tsunoda already provides a mechanism for ensuring that the power from the host is not stopped until the appropriate time, such as after the busy signal is released by the memory apparatus. As Tsunoda states, “hereinafter, writing of a part of all of the content held in the control register 4031 of the control unit 4030 in the storage area of the control register 4031 of the flash memory 4020 is referred to as register saving 4071. After the end of the register saving, the busy signal of the control register 4031 is released (4112). The host stops supplying of power to the memory apparatus 4000 when it detects the releasing of the busy signal, by palling [sic] of the control register 4031.” Ex. 1004 ¶ [0087]. A POSITA would thus understand that the well-defined and coordinated logic of the host and memory device of Tsunoda ensures proper operating, and ordered power down of the memory device to ensure proper functioning and storage of required data and control register information to non-volatile memory. Accordingly, a POSITA

would not be motivated to add an internal power source to Tsunoda's memory apparatus.

46. Dr. Liu additionally opines that “a POSITA would have viewed the implementation of Tsunoda's and Tsunoda-Sukegawa's memory apparatus in a manner that applied Tomio's suggestion regarding a rechargeable battery and corresponding memory controller functionality as merely the predictable result of combining known prior art elements according to known methods.” I disagree, as explained below.

47. Dr. Liu states “[a] POSITA would have been capable of employing ordinary creativity to carry out an implementation of the memory apparatus with the rechargeable battery and corresponding memory controller functionality in a manner necessary to achieve the advantages taught by Tomio by, for example, varying the size and shape of the memory apparatus and housing (as taught by Tsunoda or Sukegawa) to accommodate the electronic components and rechargeable battery, as corroborated by other publications illustrating USB flash drives in varying shapes and sizes.” I disagree for the reasons provided below.

48. First, as Dr. Liu appears to acknowledge (*see, e.g.*, Ex. 1003 ¶ 132) the size and shape of the Tsunda embodiment that Petitioner relies on—i.e., the MMC embodiment illustrated in Figure 14 of Tsunoda—would not accommodate a rechargeable battery. MMC was designed to be a relatively small form factor

device that uses a limited set of pins for communication with the host system. As discussed in various literature regarding MMC, and as would have been known to a POSITA, MMC was designed to be approximately the size of a postage stamp, with devices being approximately 32mm x 24mm x 1.4mm. *See* Ex. 1008 at 2:16-20, 4:35-36, Fig. 6B. A POSITA at the time the '527 patent was filed would have been aware of the packaging restrictions of MMC and would have recognized that a rechargeable battery, such as the one described in Tomio, would be entirely incompatible with those restrictions. Dr. Liu has presented no evidence of any rechargeable battery technology that would fit within the very limited form factors for which MMC was specifically designed.

49. Second, a POSITA would recognize that the MMC interface includes a very limited pin count and a low power electrical interface that would not—without significant, costly, and impractical re-engineering and modifications—have the ability to recharge a battery, such as the rechargeable battery in Tomio on which Dr. Liu relies. Indeed, Dr. Liu has not provided any evidence of the ability to charge said battery via the limited pin count, lower power electrical interface that MMC is designed to use. As a POSITA would understand, incorporating a battery or other power supply device into a small form factor electronic device would require supporting power circuitry, as well as the need to account for electrical interference, noise, and other factors for integration into such as device,

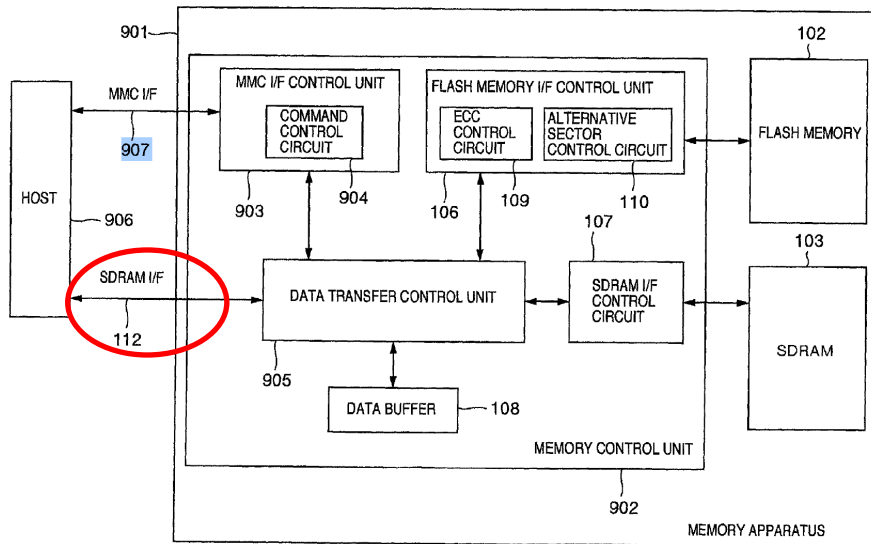
all of which would make such a modification exceedingly impractical in a portable memory device with a form factor such as an MMC.

50. Third, Dr. Liu's citation to several other references relating to "USB flash drives," *see* Ex. 1003 ¶ 132 (citing Exs. 1013, 1017, 1018, 1019, 1020), is misplaced in the context of the Tsunoda and Tsunoda-Sukegawa memory apparatus. As a POSITA would have known, USB interfaces would not be compatible with the SDRAM included in Tsunoda. Neither the petition nor Dr. Liu's declaration include any instances in the prior art where a USB interface is used by a computer system to access data in volatile memory. And the petition provides no explanation of how a USB interface, which utilizes a different pin configuration than Tsunoda's MMC interface, would have been modified to allow a computer system to access Tsunoda's SDRAM. SDRAM uses a highly parallel interface, with dedicated command and data signals for SDRAM operation. USB 2.0, in contrast, is a packetized communication protocol using serial communication. USB 2.0 supports limited data transfer rates of up to 400 Mb/s or 53MB/s via serial packetized communication, a factor of 60x slower than PC-3200 SDRAM. The form factor of USB interfaces, being low pin count, serial and intended for peripheral devices are also incompatible with the 100s of signals required for a 64/72-bit SDRAM memory module interface to a host computer. Accordingly, at the time of the invention of the '527 patent, a POSITA would not

view a USB interface as desirable, practical, or compatible with a memory device that includes SDRAM. And, not only is the proposed combination of Tsunoda and Tomio impractical, it also fails to meet the limitations of claims 1 and 15 because there is no showing how this combination would be able to access data in volatile memory using the computer system through a USB connector.

51. I also disagree with any suggestion by Dr. Liu that Tsunoda describes—“expressly” or otherwise—an embodiment in which a computer system accesses volatile memory over a serial interface such as a USB interface. Ex. 1003 ¶ 96 (citing Tsunoda ¶¶ [0094], [0117], [0124], [0056]). Paragraph [0094] of Tsunoda says “other interfaces, such as a DDR-SDRAM interface, can be used.” As a POSITA would readily understand, DDR-SDRAM (double data rate SDRAM) is a parallel interface that is *faster* than a standard SDRAM interface and would not consider Tsunoda’s disclosure of using “other interfaces, such as a DDR-SDRAM interface” as a suggestion that a drastically slower interface, such as a USB interface would be an appropriate replacement for the disclosed SDRAM interface. Paragraph [0117] describes using “interfaces of an SD card” or “a memory stick” instead of MMC interface 907. MMC interface 907 is shown in Figures 9 and 13 of Tsunoda, both of which explicitly utilize an SDRAM interface *in addition* to MMC interface 907.

FIG.9



Thus, neither the “SD card” interface nor the “memory stick” are described as a replacement for the dedicated SDRAM interface included in this embodiment, and a POSITA would not find such a replacement obvious due to the significant performance disadvantages of a USB interface compared with an SDRAM interface. Indeed, as Dr. Liu acknowledges, both Tsunoda and Tomio recognize that volatile RAM is used for “faster access” compared to flash memory. Ex. 103 ¶ 217. A POSITA would recognize that a (slower) USB interface would defeat the “faster access” advantages of volatile RAM, and a POSITA would therefore not be motivated to use such an interface. In addition, Tsunoda does not disclose, suggest, or contemplate replacing MMC interface 1407, which is described in Tsunoda’s third embodiment as using a “newly defined MMC command” (Ex. 1004 ¶ 122). Neither of paragraphs [0124] or [0056] of Tsunoda, which Dr. Liu also cites,

describe or suggest a different memory interface, let alone an interface with slower performance than an SDRAM interface.

52. A POSITA would not consider the memory module disclosed in Tomio to be a portable memory device in the context of the specification and claims the '527 Patent. The memory module in Tomio is not designed to be plugged and unplugged.

53. Dr. Liu relies on Tomio's disclosure of memory module 51. Ex. 1003 ¶¶ 125-126, 141. Tomio teaches using a 168-pin dual inline module. Ex. 1006, [0037]-[0038]. *See also Id.*, Fig. 7 (showing 54 connections to a single semiconductor memory). A POSITA would not look to Tomio for a portable memory apparatus, at least in part because of the problems that would be encountered plugging and unplugging a portable memory apparatus comprised of the many signals that Tomio discloses.

54. A POSITA would have known that unplugging Tomio's memory apparatus would likely corrupt the volatile memory. Accordingly, a POSITA have been dissuade from copying data from the volatile memory to the non-volatile memory when Tomio's memory apparatus (or one of Tsunoda's SDRAM interface embodiments) was unplugged from the computer.

55. The combination of Tsunoda in view of Tomio does not render dependent claims 2-5 and 16-17 obvious because a POSITA would not be

motivated to combine the teachings of Tsunoda and Tomio to add an internal power supply to the memory apparatus of Tsunoda and would not expect the proposed combination to be successful.

VIII. TSUNODA IN VIEW OF TOMIO AND SHIGEO DOES NOT RENDER OBVIOUS ANY OF CLAIMS 1, 6-7, 9-12, 14-15, OR 18 OF THE '527 PATENT.

56. Ground 1C (claims 13 and 20) relies on Tsunoda, Tomio, and Shigeo. The combination of Tsunoda in view of Tomio and Shigeo does not render dependent claims 13 and 20 unpatentable for the same reasons the combination of Tsunoda and Tomio would not have rendered dependent claims 2-5 and 16-17 unpatentable as obvious. A POSITA would not have added an internal power supply to the memory apparatus of Tsunoda and, in the absence of an internal power supply, would not have looked to Shigeo's teachings regarding an information processing device running low on battery power.

57. Shigeo discloses an information processing device, such as a mobile information terminal, that is driven by a battery or dry cell (e.g., flashlight battery). Ex. 1007 ¶ [0001]. Shigeo's information processing device is not a memory apparatus, let alone a portable memory apparatus with a connector. Shigeo's information processing device includes a CPU and a power supply detecting device that periodically checks the power supply voltage and, depending on the power supply voltage detected, can interrupt the CPU or set a CPU-readable register

value. Ex. 1007 ¶ [0059]. A POSITA would have recognized that Shigeo's teachings regarding an information processing device are neither analogous nor applicable to a portable memory apparatus.

IX. TSUNODA IN VIEW OF SUKEGAWA DOES NOT RENDER OBVIOUS ANY OF CLAIMS 1, 6-7, 9-12, 14-15, OR 18 OF THE '527 PATENT.

58. Ground 2A (claims 1, 6-7, 9-12, 14-15, 18) relies on Tsunoda and Sukegawa. I disagree with Dr. Liu's assertion that a POSITA would have been motivated to combine Tsunoda with Sukegawa.

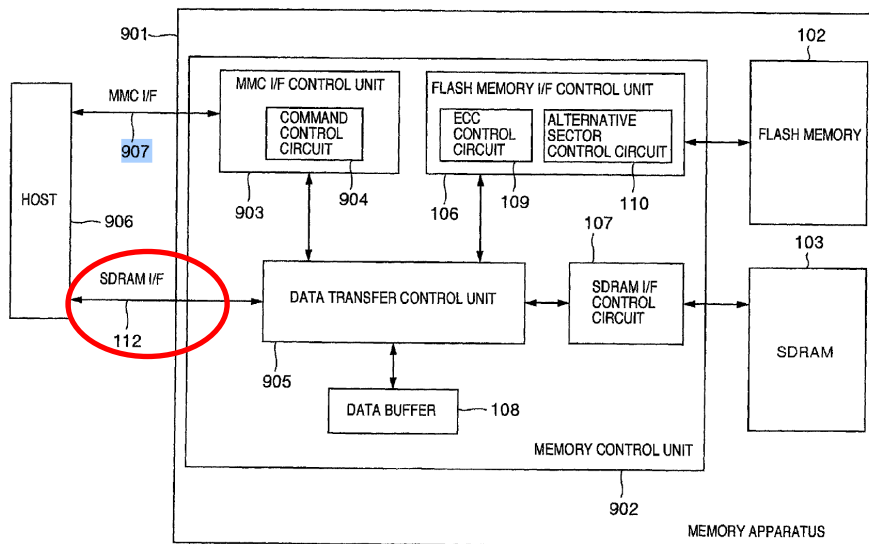
59. First, a POSITA would have known that Tsunoda's teachings of additional components were incompatible with Sukegawa's teachings of a minimally sized flash drive that should be small enough to fit in a USB connector shield. Sukegawa disclose that the flash drive should be small enough to be "mounted within the USB connector shield case." *Id.*, 4:35-36. Sukegawa teaches that a USB connector shield case is "a Plug Housing (more generally referred to as a USB connector shield case 120) that extends from an overmold boot (not shown) on an end of the connector opposite the contact terminals 400A-D." *Id.*, 7:29-32. "The USB connector shield case 120 for the Series A Plug measure 12 millimeters (mm) wide $\pm$ 0.10 mm, 4.5 mm tall $\pm$ 0.10 mm, and a minimum of 11.75 mm deep." *Id.*, 7:35-37.

60. Second, as a POSITA would have known, USB interfaces would not be compatible with the SDRAM included in Tsunoda. Neither the petition nor Dr. Liu's declaration include any instances in the prior art where a USB interface is used by a computer system to access data in volatile memory. And the petition provides no explanation of how a USB interface, which utilizes a different pin configuration than Tsunoda's MMC interface, would have been modified to allow a computer system to access Tsunoda's SDRAM. SDRAM uses a highly parallel interface, with dedicated command and data signals for SDRAM operation. USB 2.0, in contrast, is a packetized communication protocol using serial communication. USB 2.0 supports limited data transfer rates of up to 400 Mb/s or 53MB/s via serial packetized communication, a factor of 60x slower than PC-3200 SDRAM. The form factor of USB interfaces, being low pin count, serial and intended for peripheral devices are also incompatible with the 100s of pins required for a 64/72-bit SDRAM channel interface to a host computer. Accordingly, at the time of the invention of the '527 patent, a POSITA would not view a USB interface as desirable, practical, or compatible with a memory device that includes SDRAM.

61. There is no embodiment in Tsunoda in which a computer system accesses volatile memory over a serial interface such as USB. Paragraph [0094] of Tsunoda says "other interfaces, such as a DDR-SDRAM interface, can be used."

As a POSITA would readily understand, DDR-SDRAM (double data rate SDRAM) is a parallel interface that is *faster* than a standard SDRAM interface and would not consider Tsunoda's disclosure of using "other interfaces, such as a DDR-SDRAM interface" as a suggestion that a drastically slower interface, such as a USB interface, would be an appropriate replacement for the disclosed SDRAM interface. Paragraph [0117] describes using "interfaces of an SD card" or "a memory stick" instead of MMC interface 907. MMC interface 907 is shown in Figures 9 and 13 of Tsunoda, both of which explicitly utilize an SDRAM interface *in addition* to MMC interface 907.

FIG.9



62. Thus, neither the "SD card" interface nor the "memory stick" are described as a replacement for the dedicated SDRAM interface included in this embodiment, and a POSITA would not find such a replacement obvious due to the

significant performance disadvantages of a USB interface compared with an SDRAM interface. Indeed, as Dr. Liu acknowledges, both Tsunoda and Tomio recognize that volatile RAM is used for “faster access” compared to flash memory. Ex. 103 ¶ 217. A POSITA would recognize that a (slower) USB interface would defeat the “faster access” advantages of volatile RAM, and a POSITA would therefore not be motivated to use such an interface. In addition, Tsunoda does not disclose, suggest, or contemplate replacing MMC interface 1407, which is described in Tsunoda’s third embodiment as using a “newly defined MMC command” (Ex. 1004 ¶ 122). And modifying Tsunoda’s memory apparatus with a USB interface would not have been within the level of a POSITA without undue experimentation.

63. A POSITA would have known that a USB interface is not an SDRAM interface. A POSITA would have known that a USB interface is not an MMC interface. A POSITA would have further understood that a USB interface is not an SDRAM-compatible interface.

X. TSUNODA IN VIEW OF SUKEGAWA AND TOMIO DOES NOT RENDER OBVIOUS ANY OF CLAIMS 2-5 OR 16-17 OF THE ’527 PATENT.

64. Ground 2B (claims 2-5, 16-17) relies on Tsunoda, Tomio and Sukegawa. The combination of Tsunoda in view of Sukegawa and Tomio does not render dependent claims 2-5 and 16-17 obvious, because, in addition to all the

reasons provided above for Grounds 1B and 2A, a POSITA would not have been motivated to combine Tsunoda and Tomio to add an internal power supply to the memory apparatus of Tsunoda. Sukegawa's teaching of a USB memory device without volatile memory would not have altered this analysis. To the contrary, Sukegawa's recognition of "an urgent need for an improved USB flash drive that is reduced in size, [and] is less expensive, ..." would have dissuaded a POSITA from additional expense and complexity. Ex. 1005 ¶ 2:27-28; *see also* Ex. 1005 at 4:39-40 ("In this way, the number of parts within the USB flash drive is reduced and the physical size of the drive can be drastically reduced ...").

65. Claim 3 recites in part "wherein said internal power source powers said portable memory apparatus when said portable memory apparatus is unplugged from said computer system, said portable memory apparatus copies data from said volatile memory to said non-volatile memory when said portable memory is unplugged from said computer system." A POSITA would not have found this limitation, or the similar limitation in claim 16, obvious in light of Tsunoda, Sukegawa and Tomio for the additional reasons provided below.

66. There is no disclosure in either Tsunoda, Tomio, or Sukegawa related to a memory device being unplugged. Indeed, if the memory device in Tsunoda were removed from the host by the user, without a priori knowledge by the host, it would create multiple unacceptable and potentially catastrophic problems. To

begin, allowing a device to be removed from the host at a point in time that is random from the host's perspective, precludes the host from being able to perform an orderly set of commands to ensure data and control integrity of the device. Commands and signals cannot be sent back and forth in an orderly manner to ensure proper command signaling protocol and data integrity, but abruptly removing the device presents an issues whereby the electrical signals at the device interface can be in seemingly random states upon removal. This would have undesirable and potentially electrically damaging effects on the system.

67. In addition, because the device may be in a state of processing a given transaction such as a read or write operation to non-volatile memory when the power is removed, the data integrity of file content in the non-volatile memory cannot be ensured. A simple example of this, which a POSITA would immediately appreciate, is the saving of a file such as media, Microsoft Word files, or other work that does not completely get stored in the non-volatile memory. This would result in non-recoverable data corruption and loss of information for the host computer and user. Dr. Liu's opinion that claims 3 and 16 are rendered obvious by the combination of Tsunoda, Sukegawa and Tomio does not consider or address these problems, and I disagree with his analysis for these additional reasons.

68. The problems inherent in unplugging a memory apparatus with numerous connectors such as Tomio's memory apparatus (or one of Tsunoda's

SDRAM interface embodiments) including, e.g., floating electrical signal values, necessary modification of logic and command structure, etc., would have meant that combining Tomio's and Tsunoda's teachings would have required more than combining known prior art elements according to known methods and would not have yielded predictable results.

XI. TSUNODA IN VIEW OF SUKEGAWA, TOMIO, AND SHIGEO DOES NOT RENDER OBVIOUS ANY OF CLAIMS 13 OR 20 OF THE '527 PATENT.

69. The combination of Tsunoda in view of Sukegawa, Tomio and Shigeo does not render dependent claims 13 and 20 unpatentable for the same reasons the combination of Tsunoda and Tomio would not have rendered dependent claims 2-5 and 16-17 unpatentable as obvious. A POSITA would not have added an internal power supply to the memory apparatus of Tsunoda and, in the absence of an internal power supply, would not have looked to Shigeo's teachings regarding an information processing device running low on battery power.

XII. TOMIO DOES NOT RENDER OBVIOUS ANY OF CLAIMS 1-6, 9, 12, OR 15-17 OF THE '527 PATENT.

70. Ground 3A (claims 1-6, 9, 12, and 15-17) relies on Tomio. A POSITA would not consider the memory module disclosed in Tomio and relied upon by Petitioner to be a portable memory device in the context of the specification and claims the '527 Patent. The memory module in Tomio is not designed to be plugged and unplugged. In contrast, the '527 describes memory modules that are

intended to be plugged and unplugged. *See, e.g.*, Ex. 1001, 1:51-57 (describing plugging and unplugging the portable RAM drive). *See also, Id.*, 3:48-52 (“The portable RAM drive may be coupled to the computer system through a connector on the portable RAM drive and a connector, such as, but not limited to, a USB connector, a firewire connector, and an ATA serial connector.”); 4:16-21, 39-48 (describing plugging and unplugging the portable RAM drive).

71. A POSITA would not understand that Tomio’s teachings are directed to a portable memory apparatus. Tomio is instead directed to an internal memory that could shorten the startup time for a personal computer. Ex. 1006 ¶ [0004] (“Because the transfer of data from the ROM to the DRAM is slow, a considerable amount of time is required after turning on power to the personal computer before the user can actually start working on the personal computer, and this time cannot be shortened.”). Tomio essentially discloses a boot loader that is on the motherboard of personal computer. *Id.*, [0012] (“Fig. 1 is a block diagram showing essential components on the motherboard 1 of a personal computer in an embodiment of the invention.”). *See also, Id.*, [0033] (“The cost of the motherboard 1 can also be reduced because a ROM separately mounted on the motherboard 1 becomes unnecessary and a data transfer circuit from the ROM to the main memory becomes unnecessary. Because there is no need to transfer data from the ROM to the main memory, the time from turning on the power to the

personal computer becoming ready for use is shortened.”). Accordingly, Tomio is directed to a non-portable memory that is on the motherboard when a computer is turned on. A POSITA would not have understood Tomio’s disclosure of an internal memory module as teaching a portable memory apparatus.

XIII. TOMIO IN VIEW OF SHIGEO DOES NOT RENDER OBVIOUS CLAIMS 13 OR 20 OF THE ’527 PATENT.

72. Ground 3B (claims 13 and 20) relies on Tomio and Shigeo and is flawed for the same reasons as Ground 1A.

XIV. TOMIO IN VIEW OF SUKEGAWA DOES NOT RENDER OBVIOUS ANY OF CLAIMS 1-7, 9-12, OR 14-18 OF THE ’527 PATENT

73. Ground 4A (claims 1-7, 9-12, 14-18) relies on Tomio and Sukegawa, and is flawed for the same reasons as Ground 3A. A POSITA would not understand that Tomio’s teachings are directed to a portable memory apparatus. Tomio is instead directed to an internal memory that could shorten the startup time for a personal computer. Ex. 1006, [0004] (“ Because the transfer of data from the ROM to the DRAM is slow, a considerable amount of time is required after turning on power to the personal computer before the user can actually start working on the personal computer, and this time cannot be shortened.”). Tomio essentially discloses a boot loader that is on the motherboard of personal computer. *Id.*, [0012] (“Fig. 1 is a block diagram showing essential components on the motherboard 1 of a personal computer in an embodiment of the invention.”). *See*

also, Id., [0033] (“The cost of the motherboard 1 can also be reduced because a ROM separately mounted on the motherboard 1 becomes unnecessary and a data transfer circuit from the ROM to the main memory becomes unnecessary. Because there is no need to transfer data from the ROM to the main memory, the time from turning on the power to the personal computer becoming ready for use is shortened.”). Accordingly, Tomio is directed to a non-portable memory that is on the motherboard when a computer is turned on.

74. A POSITA would not look to Tomio for a portable memory apparatus because of the problems that would be encountered plugging and unplugging a portable memory apparatus. As discussed in Ex. 1007, even low power can corrupt a memory connection. *See* Ex. 1007 ¶ [0061]. *See also* Paper 2, Pet., at 84 (“Shigeo explains that information stored in RAM ‘becomes corrupted’ when the battery does not have enough power to power the RAM, ...”). A POSITA would have known that unplugging Tomio’s memory would likely corrupt the volatile memory. A POSITA would have known that unplugging memory without previous notification to the host device would create significant problems and could be catastrophic. There would be a loss of data integrity and possible damage to the host or the portable memory apparatus. A POSITA would have recognized that the data corruption could result in an unacceptable data loss to the user. Accordingly, a POSITA would have understood that “hot swapping” would not be

an available benefit using Tomio's memory. For these reasons, one of the purported benefits of a USB interface, so-called "hot swapping," would have been detrimental to a portable memory apparatus combining the teachings of Tomio and Sukegawa.

75. Furthermore, the shortened data transfer time Tomio teaches for volatile versus non-volatile memory would be nullified by a USB interface. Even with the "high data transmission speed (12 mb/sec)" identified by Petitioner, Paper 2, Pet. at 70, the USB transmission rate would be slower than the flash memory access rate. A POSITA would not be motivated to add the complexity of a DRAM, including DRAM controller functionality, to a USB flash drive.

76. A POSITA would not have found it obvious to use Tomio's combination memory with a USB connector in a portable memory apparatus. None of the prior art identified by Petitioner discloses DRAM with a USB connector and implementing it would not have been the predictable result of combining known prior art elements according to known methods for the reasons discussed above. Resolving the data corruption and loss issues would not have been within the level of skill of a POSITA, even with undue experimentation.

77. A POSITA would have known that unplugging memory without previous notification to the host device would create significant problems and could be catastrophic. There would be a loss of data integrity and possible damage

to the host or the portable memory apparatus. A POSITA would have recognized that the data corruption could result in an unacceptable data loss to the user. Accordingly, dependent claims 3 and 16 would have been non-obvious to a POSITA for these reasons as well.

XV. TOMIO IN VIEW OF SUKEGAWA AND SHIGEO DOES NOT RENDER OBVIOUS CLAIMS 13 OR 20 OF THE '527 PATENT

78. Ground 4B (claims 13 and 20) relies on Tomio, Sukegawa and Shigeo and is flawed for the same reasons Grounds 3A and 4A. The combination of Tomio in view of Sukegawa and Shigeo does not render dependent claims 13 and 20 unpatentable for the same reasons the combination of Tomio and Shigeo would not have rendered dependent claims 13 and 20 unpatentable as obvious. A POSITA would not have would not have looked to Tomio's teachings regarding an internal memory module or Shigeo's teachings regarding an information processing device running low on battery power in the context of a portable memory apparatus.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true.

March 11, 2024



Michael C. Brogioli, Ph.D.