

VLSI

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DESIGN TECHNIQUES

Phillip E. Allen

FOR ANALOG AND

Noel R. Strader

DIGITAL CIRCUITS

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McGraw-Hill Publishing Company

New York St. Louis San Francisco Auckland Bogotá Caracas
Hamburg Lisbon London Madrid Mexico Milan
Montreal New Delhi Oklahoma City Paris San Juan
São Paulo Singapore Sydney Tokyo Toronto

This book was set in Times Roman by Publication Services, Inc.
 The editors were Alar E. Elken and John M. Morriss;
 the production supervisor was Janelle S. Travers.
 The cover was designed by Robin Hessel.
 Project supervision was done by Publication Services, Inc.
 Arcata Graphics/Halliday was printer and binder.

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34567890 HDHD 99876543

ISBN 0-07-023253-9

Library of Congress Cataloging-in-Publication Data

Geiger, Randall L.
 VLSI design techniques for analog and
 digital circuits.
 (McGraw-Hill series in electrical engineering)
 Includes index.
 1. Integrated circuits--Very large scale
 integration--Design and construction. I. Allen, P. E.
 (Phillip E.) II. Strader, Noel R. III. Title.
 IV. Series.
 TK7874.G43 1990 621.381'73 88-37737
 ISBN 0-07-023253-9

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3.4.2 Monolithic Resistors

Considerably more options exist for monolithic resistors. Some monolithic resistors are passive devices and others contain active devices. Major tradeoffs must be made between linearity, area, biasing complexity, and temperature characteristics in monolithic resistors. Table 3.4-2 lists the characteristics of some of the structures that are used for resistors.

In standard MOS processes, the most ideal resistors are merely strips of polysilicon. Diffusion strips are also used for resistors but exhibit an undesirable nonlinear relationship between voltage and current. Ion implants offer some advantages over depositions for the introduction of impurities to control absolute resistance values in diffused resistors. Thin film resistors with excellent characteristics are added in some specialized processes. For each of these types of resistors, a serpentine pattern is often used to improve packing density. The major limitations of these resistors are the low resistance densities, which limit the total resistance to quite small values; the high deviations in resistance due to process variations; and large temperature coefficients.

In bipolar processes epitaxial strips or diffusion strips are commonly used for resistors. These devices are quite linear. The base diffusion is often used because of its reasonably high sheet resistance. A base-diffused resistor is shown in Fig. 3.4-1a. To prevent forward biasing of the "base-collector" junction, a contact is needed to the epitaxial layer. This will be typically connected to the most positive power supply voltage used for the circuit.

It can be argued that the resistance of the base-diffused resistor could be increased if the depth of the p-base diffusion could be decreased. The depth of this diffusion, however, is generally determined to optimize performance of the BJTs themselves. An alternative is to place an n^+ emitter diffusion in the p base region. This masking step already exists and will result in a significant increase of the sheet resistance of the underlying p diffusion. Such a device, which is termed a *pinch* resistor, is shown in Fig. 3.4-1b. Contact must be made to both the n^+ emitter diffusion and the n^- epitaxial region. These regions are typically both connected to the most positive power supply voltage used for the circuit. Although the resistance increases significantly due to this pinching, the variance in emitter and base diffusion depths due to process variations makes the tolerances of pinch resistors quite wide. They also exhibit an increased voltage dependent nonlinearity and are limited in voltage range to circumvent breakdown of the reverse-biased base-emitter junction. Other types of pinch resistors (e.g., epitaxial pinch) can also be made.

Several *active resistors* are shown in Fig. 3.4-2. These active resistors often offer considerable reductions in area requirements compared to passive resistors at the expense of increased nonlinearity and/or reduced signal swing and/or complicated biasing requirements. A more detailed discussion of the active resistor structures appears in Chapter 5.

The circuit of Fig 3.4-2a is merely a MOSFET biased to operate in the ohmic region. From (3) of Table 3.1-1, the relationship between I_D and V_{GS} is

$$I_D = \frac{K'W}{L} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \quad (3.4-1)$$

TABLE 3.4-2
Characteristics of MOS Resistors

Device	Characterizing equation	Ideal resistance†
Poly Strip	$V = IR \square \frac{L}{W}$	$R = R \square \frac{L}{W}$
Diffusion	$V = IR \square \frac{L}{W}$	$R = R \square \frac{L}{W}$
MOSFET (Ohmic region, Fig. 3.4-2a)	$I = \frac{K'W}{L} [(V_{GS} - V_T) - \frac{V}{2}]V$	$R = \frac{L}{K'W (V_{GS} - V_T)}$
MOSFET (Saturated region, Fig. 3.4-2b)	$I = \frac{K'W}{2L} (V_{GS} - V_T)^2 (1 + \lambda V)$	$R_{SS} = \frac{2L}{\lambda K'W (V_{GS} - V_T)^2}$
MOS depletion (Fig. 3.4-2c)	$I = \begin{cases} \frac{K'W}{L} (-V_T)V & V < -V_T \\ \frac{K'W}{2L} V_T^2 (1 + \lambda V) & V > V_T \end{cases}$	$R = \frac{L}{K'W V_T }$ $R_{SS} = \frac{2L}{K'W V_T^2 \lambda}$
MOS Enhancement (Fig. 3.4-2d)	$I = \frac{K'W}{2L} (V - V_T)^2 (1 + \lambda V)$	$R_{SS} = \frac{L}{K'W (V_Q - V_T)}$
Linearity Compensated ¹⁸ (Fig. 3.4-2e)	$I = \begin{cases} \frac{2K'W}{L} (-V_T)V & V < -V_T \\ \frac{K'W}{L} V_T^2 (1 + \lambda V) & V > -V_T \end{cases}$	$R = \frac{L}{2K'W V_T }$ $R_{SS} = \frac{L}{K'W V_T^2 \lambda}$
Bootstrapped Budak ¹⁷ (Fig. 3.4-2f)	$I = \frac{K'W}{L} (V_C - V_T - V \frac{[\theta + 1]}{2}) (1 - \theta) V$ $V < V_C - V_T$	$R = \frac{L}{K'W (1 - \theta)}$

If $V_{DS} \ll (V_{GS} - V_T)$, then, as seen in Eq. 3.4-1, the relationship between I_D and V_{DS} is linear (assuming V_{GS} is independent of V_{DS}), resulting in an equivalent resistance of

$$R_{eq} \approx \frac{L}{K'W (V_{GS} - V_T)} \quad (3.4-2)$$

This approximation is quite good for $V_{DS} < 0.5(V_{GS} - V_T)$. A model that includes the nonlinearity is

$$R_{eq} \approx \frac{L}{K'W [(V_{GS} - V_T) - V_{DS}/2]} \quad (3.4-3)$$

The resistance density (resistance per unit area) of the MOS resistor will now be calculated. Assume d_1 is the minimum moat width, d_2 the minimum

Resistance density‡	Temperature characteristic	Absolute accuracy	Relative accuracy	Comments
$\frac{R_{\square}}{d_4(d_3 + d_4)}$	1500 ppm/°C	±30%	±2%	Linear, low resistance density
$\frac{R_{\square}}{d_3(d_3 + d_4)}$	1500 ppm/°C	±35%	±2%	Somewhat voltage dependent
$\frac{1}{K'(V_{GS} - V_T)d_1(d_1 + 2d_2 + d_3)}$				To minimize distortion, $V < (V_{GS} - V_T)/2$
$\frac{1}{\lambda \frac{K'}{2}(V_{GS} - V_T)^2 d_1(d_1 + 2d_2 + d_3)}$				Small signal impedance only, high impedance values
$\frac{1}{K' V_T d_1(d_1 + 2d_2 + d_3)}$				Popular load device
$\frac{1}{\lambda \frac{K'}{2}V_T^2 d_1(d_1 + 2d_2 + d_3)}$				Quite nonlinear
$\frac{1}{K'(V_Q - V_T)d_1(d_1 + 2d_2 + d_3)}$				Quite nonlinear, good resistance density
$\frac{1}{2K' V_T d_1(d_1 + 2d_2 + d_3)}$				Major improvement in density
$\frac{1}{\lambda K'V_T^2 d_1(d_1 + 2d_2 + d_3)}$				
Depends upon how θV is realized				Good linearity potential

†R denotes large signal impedance; R_{SS} denotes small signal impedance only.

‡Assuming a minimum size layout, see Fig. 3.4-3 d_1 , d_2 , d_3 , and d_4 as defined in Sec. 3.4.2.

required overlap of poly over moat, and d_3 the minimum poly-poly spacing as defined by the design rules of the process. If a large serpentine MOS device is constructed with minimum moat width and with separate polysilicon strips for each diffusion strip in the serpentine and if the incremental area required by the corners is neglected, then the diagram of Fig. 3.4-3 can be used to calculate the resistance density of this device. The section of length h has a resistance of

$$R = \frac{h}{K'd_1(V_{GS} - V_T)} \quad (3.4-4)$$

and an area of

$$A = h(d_3 + d_1 + 2d_2) \quad (3.4-5)$$

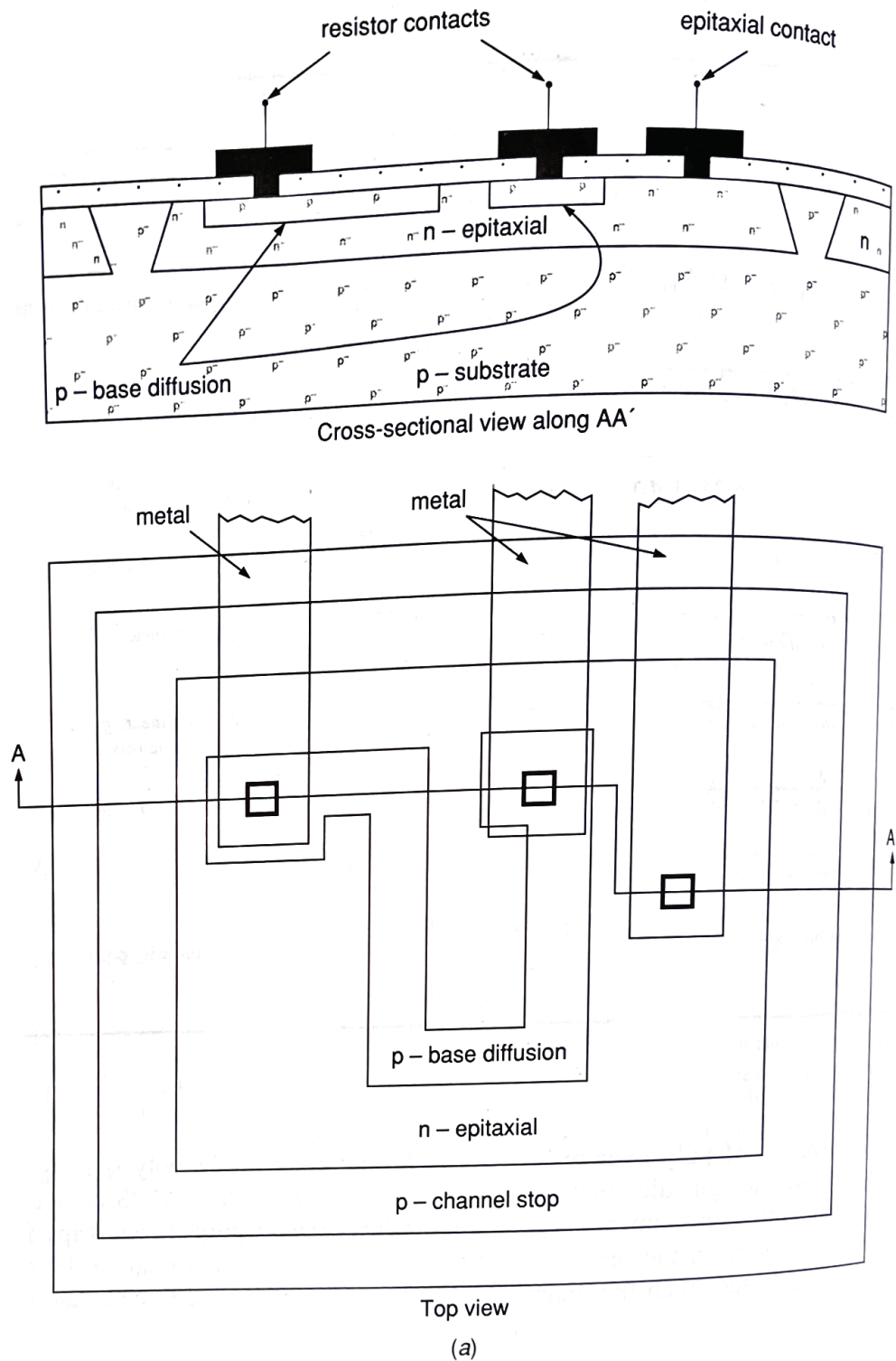


FIGURE 3.4-1
Monolithic resistors: (a) Base diffused, (b) Base-pinch.

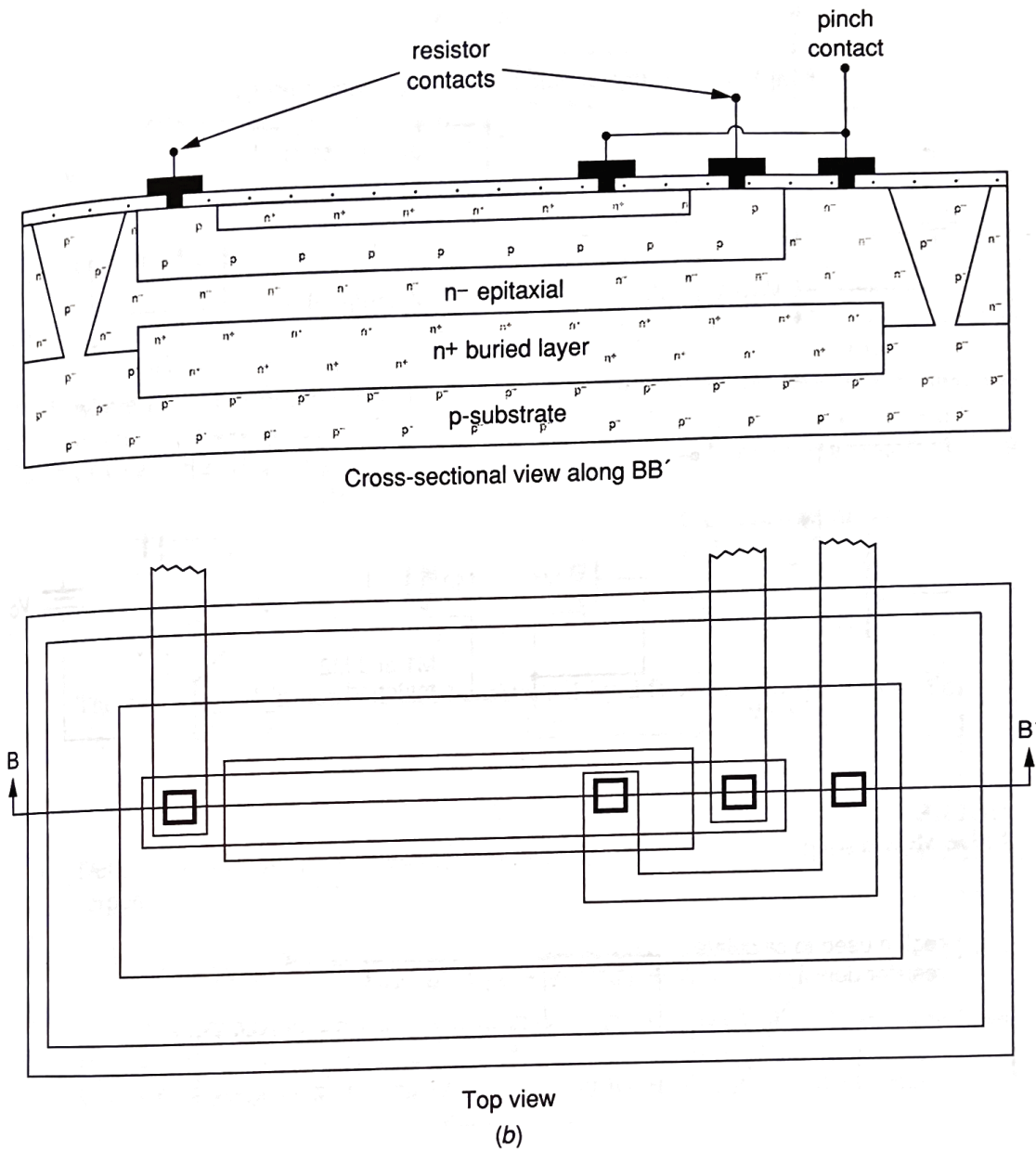


FIGURE 3.4-1
(continued)

so a resistance density of

$$R_d = \frac{1}{K'(V_{GS} - V_T)(d_1 + 2d_2 + d_3)d_1} \quad (3.4-6)$$

Although making V_{GS} close to V_T can make R_d very high, it is generally impractical due to process variations to directly make $V_{GS} - V_T < 1$ V. Some improvements in resistance density can be realized if the polysilicon strips are merged into one large rectangular region. In this case, the minimum diffusion spacings will determine how close the serpentine strips can be placed. If the MOSFET is a depletion device, it is particularly convenient to make $V_{GS} = 0$ as shown in Fig. 3.4-2c, thus eliminating the need for a voltage source.

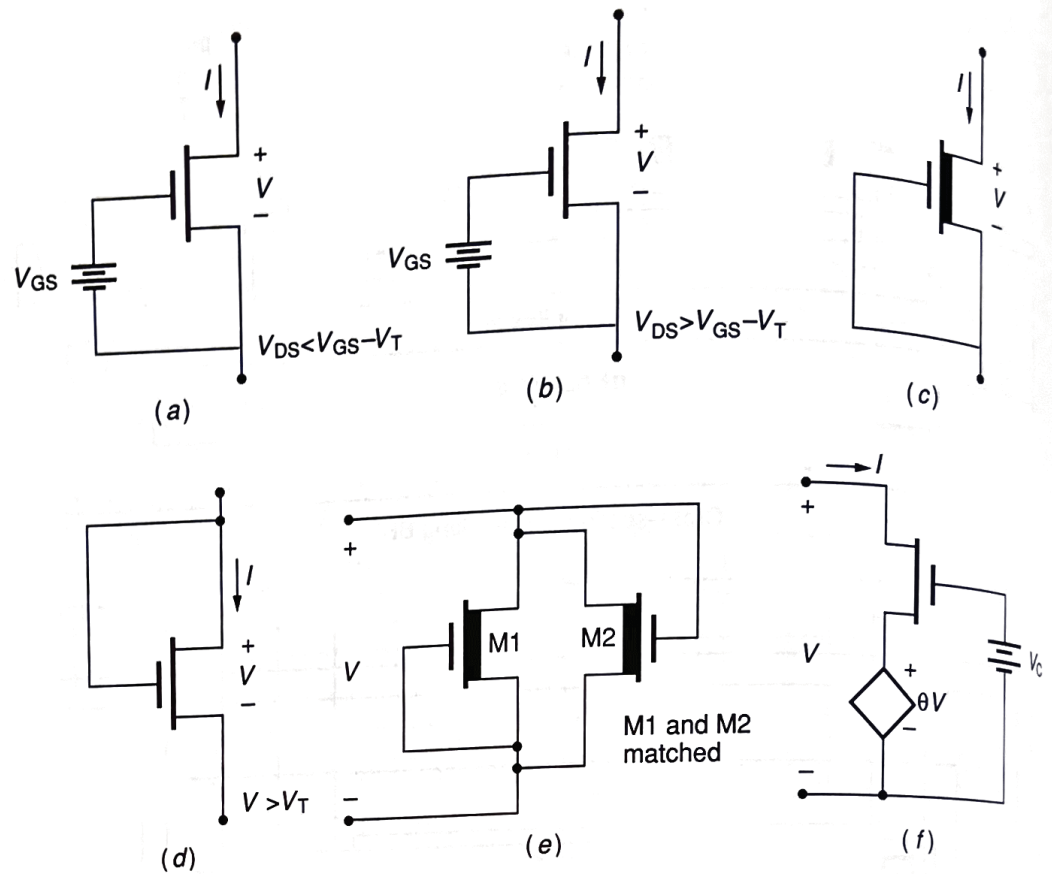


FIGURE 3.4-2
Active MOS resistors.

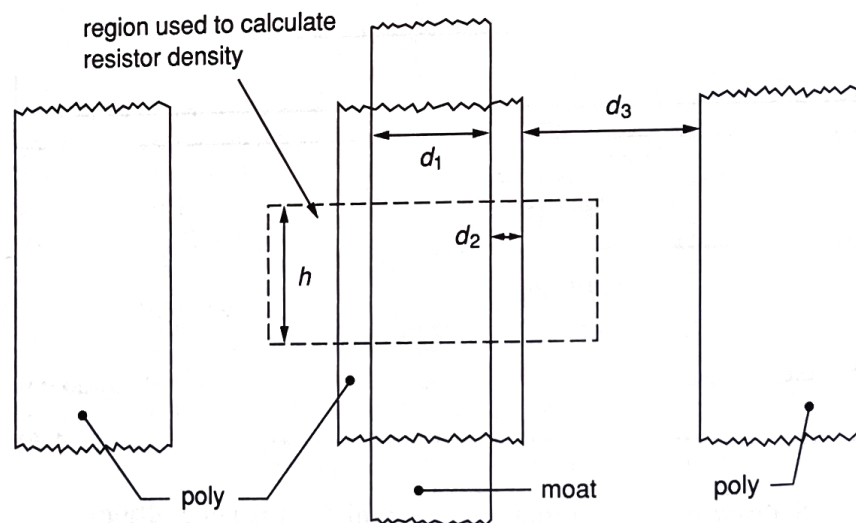


FIGURE 3.4-3
Calculation of resistance density of MOS resistor in ohmic region.

Example 3.4-1. Compare the area required to make a 1 M Ω resistor using a minimum size POLY I string with that using a MOS depletion resistor operating in the saturation region with $V_{GS} = 0$. Use the design rules and process parameters of the NMOS process discussed in Appendix 2A of Chapter 2. Assume the POLY I is uncovered and the feature size of the process is 3 μ (i.e., $\lambda = 1.5 \mu$).

Solution. The resistance density of the POLY I string can be readily obtained (see Problem 3.55) and is given by

$$R_{dp} = \frac{R_{\square}}{d_4(d_3 + d_4)} \quad (3.4-7)$$

where d_3 is the minimum poly spacing, d_4 is the minimum poly width, and $R_{\square}$ is the sheet resistance of POLY I. From Tables 2A.2 and 2A.4 of Appendix A of Chapter 2, $d_3 = 3 \mu$, $d_4 = 3 \mu$, and $R_{\square} = 25 \Omega/\square$. Substituting into (3.4-7), it follows that $R_{dp} = 1.39 \Omega/\mu^2$.

If the MOSFET shown in Fig. 3.4-2c is biased to operate in the saturation region, then, from (4) of Table 3.1-1, the drain current is given by

$$I_D = \frac{K'W}{2L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

The small signal impedance can be obtained by differentiation (assuming V_{GS} and V_{BS} constant) with respect to V_{DS} to obtain

$$R_{ss} = \frac{2L}{[\lambda K'W(V_{GS} - V_T)^2]} \quad (3.4-8)$$

Defining d_1 – d_3 as in Fig. 3.4-3, it follows that the resistance density for a large serpentine structure is

$$R_{ds} = \frac{2}{[\lambda K'd_1(V_{GS} - V_T)^2(d_1 + 2d_2 + d_3)]} \quad (3.4-9)$$

From Tables 2A.2 and 2A.4 of Chapter 2, $\lambda = 0.01 \text{ V}^{-1}$, $K' = 25 \mu\text{A}/\text{V}^2$, $V_T = -3 \text{ V}$, $d_1 = 3 \mu$, $d_2 = 3 \mu$, and $d_3 = 3 \mu$. Substituting into (3.4-9) and setting $V_{GS} = 0$, we obtain $R_{ds} = 74 \text{ k}\Omega/\mu^2$. It follows that the area ratio is the ratio of the resistance densities; that is, the ratio of R_{dp} to R_{ds} , which is about 67,000 to 1. The area required to make the 1 M Ω poly resistor is about $9 \times 10^5 \mu^2$, whereas the active resistor requires an area of around $13 \mu^2$.

Note that for reasonable values of $V_{GS} - V_T$, the λ in the denominator of (3.4-9) makes the resistance density of the MOS resistor in the saturation region considerably higher than the resistance density of the same device biased to operate in the ohmic region. Small signal resistances in the 1 M Ω range become practical with the MOS resistor biased to operate in the saturation region.

Several other MOS active resistors are shown in Fig. 3.4-2. Those of Fig. 3.4-2c and d have proven the most popular in NMOS applications due to their simplicity. The structures of Fig. 3.4-2e and f offer improvements in linearity at the expense of increased area and/or complexity. The characteristics of these active loads are summarized in Table 3.4-2.

A popular bipolar active resistor is shown in Fig. 3.4-4. The equivalent resistance and resistance density will now be calculated.

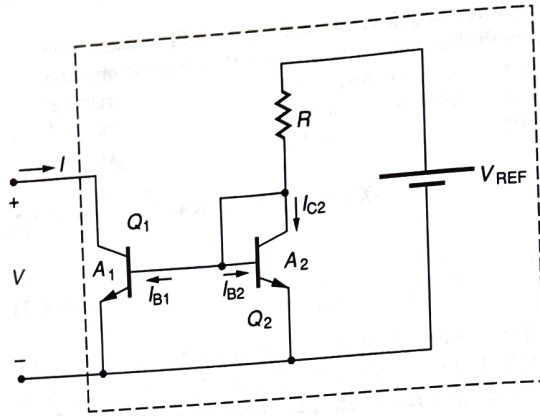


FIGURE 3.4-4
Active bipolar resistor.

Assuming Q_2 is operating in the active region and that β_F is large enough so that $(I_{B1} + I_{B2}) \ll I_{C2}$, it follows from (2) of Table 3.3-3 that

$$I_{C2} \approx (V_{REF} - 0.6 \text{ V})/R \quad (3.4-10)$$

and from (1) of Table 3.3-2 (neglecting V_{AF} , which is justifiable since $V_{CE2} \approx 0.6 \text{ V} \ll V_{AF}$),

$$I_{C2} \approx J_S A_2 \exp\left(\frac{V_{BE2}}{V_t}\right) \quad (3.4-11)$$

Equating the two expressions for I_{C2} , it follows that

$$\exp\left(\frac{V_{BE2}}{V_t}\right) \approx \frac{V_{REF} - 0.6 \text{ V}}{R J_S A_2} \quad (3.4-12)$$

Again, from (1) of Table 3.3-2, it follows that

$$I = J_S A_1 \left(1 + \frac{V}{V_{AF}}\right) \exp\left(\frac{V_{BE1}}{V_t}\right) \quad (3.4-13)$$

Since $V_{BE1} = V_{BE2}$ it follows from (3.4-12) and (3.4-13) that

$$I = \frac{A_1 \left(1 + \frac{V}{V_{AF}}\right) (V_{REF} - 0.6 \text{ V})}{A_2 R} \quad (3.4-14)$$

The small signal impedance follows from differentiation with respect to V and is given by

$$R_{eq} = \frac{V_{AF} A_2 R}{A_1 (V_{REF} - 0.6 \text{ V})} \quad (3.4-15)$$

It can be shown that for large R , the area of R dominates that of Q_1 and Q_2 ; hence the resistance density is approximately m times that of R where

$$m = \left(\frac{V_{AF}}{V_{REF}}\right) \left(\frac{A_2}{A_1}\right) \quad (3.4-16)$$

It can be seen that this active resistor requires 10 to 1000 times the area of the circuit of Fig. 3.4-4 will be required in Chapter 5.

Both active and passive resistors for passive resistors becomes a resistor alternative but must be nonlinear and often require special

3.5 SUMMARY

In this chapter, models for MOSFETs have been developed. Included are low-frequency and high-frequency models of MOSFETs. Models were obtained by differentiating the processes in which the device allows the user to select the most notable difference law contrasted to exponential impedances, characterized by a small input will be used for analysis and for use in computer simulation.

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with two gates, one of which is isolated from the circuit. If this floating gate somehow acquires charge to represent a stored data value, the charge remains there for a long period of time because the gate is insulated from its surroundings by silicon dioxide. The leakage paths for this circuit are of such high resistance that the time constant for the discharge path of the EPROM memory cell is tens of years. The presence or absence of stored charge is the mechanism by which the cell stores a data value, but how is the data value changed once it has been stored?

The mechanism for programming new data comes from the second part of the FAMOS name, *avalanche injection*. If a relatively high voltage (about 25 V—less for newer parts) is applied to the floating gate–substrate region, avalanche injection of electrons onto the gate takes place. This phenomenon serves to program memory by placing charge on the gate. Memory is erased by removing undesired charge from a gate as follows. If the floating gate is exposed to strong light of the proper wavelength (UV–2537 Å) for a period of time, enough energy is imparted to the stored charge to remove it from the floating gate. A quartz window is incorporated into the memory chip package; thus, all memory cells are exposed and erased simultaneously. Typical erase times for EPROMs are in the range of 20 to 30 minutes.

EPROMs are widely used in electronic systems where product volume is insufficient to justify the high initial cost of ROM parts. They are also used in prototyping microprocessor systems where reprogrammable but nonvolatile memory is required. A disadvantage of EPROM memory is the usual need to remove the memory part from the system if it becomes necessary to erase and reprogram the EPROM. The next section describes an improvement to the EPROM that was designed to overcome this undesirable characteristic.

9.9.2 Electrically Erasable Programmable Read-Only Memory

As useful as EPROM memories are, there are many applications requiring nonvolatile memory that can be reprogrammed quickly without removing the memory part from the system. For example, it is often desirable to program a standard CRT terminal with serial interface characteristics that will not be lost when power is disconnected. Yet, these characteristics must be changeable if the terminal is connected to a computer using a different serial data format. Applications such as this created a need for an EPROM whose contents could be changed electrically. Several manufacturers now offer memory parts called EAPROMs (electrically alterable) or EEPROMs (electrically erasable) that fulfill this need.

Interestingly, the EEPROMs solve the programming and erasure problems with two simple techniques. First, programming has been simplified by on-chip generation of the programming voltage. Instead of requiring an external connection to 25 V, a circuit called a *charge pump* is used to generate the necessary programming voltage from the standard 5 V supply. Second, instead of using ultraviolet light to erase the data, an internal connection is provided to reverse the electron injection phenomenon, allowing charge to be removed from the floating gate of the EEPROM.