

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Micron Technology, Inc.,
Petitioner

v.

Sonrai Memory Limited,
Patent Owner

Case IPR2023-00909
Patent No. 6,724,241

Declaration of James C. Dickens, Ph.D., P.E.

I, James C. Dickens, Ph.D., P.E., declare that:

I. Introduction

1. My name is James Claude Dickens, and I have been retained by counsel for Petitioner Micron Technology, Inc. (“Micron” or “Petitioner”) as an expert witness to provide assistance regarding U.S. Patent No. 6,724,241 (“the ’241 Patent”). Specifically, I have been asked to consider the validity of claims 1-25 of the ’241 Patent (the “Challenged Claims”) in view of prior art, anticipation and obviousness considerations, and understanding of a person of ordinary skill in the art at the time of the alleged invention (“POSITA”) as it relates to the ’241 Patent. I have personal knowledge of the facts and opinions set forth in this declaration and believe them to be true. If called upon to do so, I would testify competently thereto.

2. I am being compensated for my time at my standard consulting rate. I am also being reimbursed for expenses that I incur during the course of this work. My compensation is not contingent upon the results of my study, the substance of my opinions, or the outcome of any proceeding involving the challenged claims. I have no financial interest in the outcome of this matter or on the pending litigation between Petitioner and Patent Owner.

3. My analysis here is based on my years of education, research and experience, as well as my investigation and study of relevant materials, including

those cited herein.

4. I may rely upon these materials, my knowledge and experience, and/or additional materials to rebut arguments raised by the Patent Owner. Further, I may also consider additional documents and information in forming any necessary opinions, including documents that may not yet have been provided to me.

5. My analysis of the materials produced in this proceeding is ongoing and I will continue to review any new material as it is provided. This declaration represents only those opinions I have formed to date. I reserve the right to revise, supplement, and/or amend my opinions stated herein based on new information and on my continuing analysis of the materials already provided.

II. Background and Qualifications

6. My qualifications are set forth in my curriculum vitae, a copy of which is attached as exhibit EX-1004 to this Petition. As set forth therein, I am a tenured Professor in the Electrical and Computer Engineering Department of Texas Tech University in Lubbock, Texas, and a Licensed Professional Engineer in the State of Texas. I hold the C. B. Thornton Chair for Electronics in Electrical Engineering, and currently serve as Co-Director of the Center for Pulsed Power and Power Electronics at Texas Tech University.

7. I earned a Bachelor of Science (B.S.), a Master of Science (M.S.), and

a Doctorate (Ph.D.) degree in Electrical Engineering from Texas Tech University in 1991, 1993, and 1995, respectively. I have over 25 years of design and research experience in the areas of microelectronics and Very Large Scale Integration (VLSI) design, power electronics, radio frequency (RF) and microwaves, high speed pulse data acquisition systems, Si, GaN, GaAs and SiC fabrication processes and device design, and energetic materials and systems.

8. I have published over one-hundred articles in peer-reviewed journals and spoken at more than 100 conferences throughout the world, many of which involve circuits and systems. I regularly teach the terminal Advanced Electronics course at Texas Tech University in which I cover many aspects of electronic circuits discussed in the '241 Patent.

9. Based on my experience of over 3 decades in communications technologies as described above, and the acceptance of my publications and professional recognition by societies in my field, I believe that I am qualified to be an expert in electronic circuits and systems, including electronic circuits used in memory devices.

10. Based on my experiences described above, and as indicated in my curriculum vitae, I am qualified to provide the following opinions with respect to the '241 Patent in this case. Additionally, I was at least a person having ordinary skill in the art as of the Critical Date (which I discuss below) of the '241 Patent.

III. Level of Ordinary Skill in the Art

11. In rendering the opinions set forth in this declaration, I have been asked to consider the patent claims and the prior art through the eyes of a person of ordinary skill in the art (“POSITA”) at the time of the alleged invention, which I understand to be October 25, 2002 (“Critical Date”)—the filing date of the foreign priority application. I understand that the factors considered in determining the ordinary level of skill in a field of art include the level of education and experience of persons working in the field; the types of problems encountered in the field; the teachings of the prior art, and the sophistication of the technology at the time of the alleged invention. I understand that a person of ordinary skill in the art is not a specific real individual, but rather is a hypothetical individual having the qualities reflected by the factors above. I understand that a person of ordinary skill in the art would also have knowledge from the teachings of the prior art, including the art cited below.

12. Taking these factors into consideration, on or before October 25, 2002, a person of ordinary skill in the art (POSITA) relating to the technology of the '241 Patent would have had a Bachelor's degree in electrical engineering or a related field, and 2-3 years of experience in the design or development of electronic circuits or systems, or the equivalent. Additional graduate education could substitute for professional experience, or significant experience in the field

could substitute for formal education.

13. Before October 25, 2002, my level of skill in the art was at least that of a POSITA. I am qualified to provide opinions concerning what one of ordinary skill would have known and understood at that time, and my analysis and conclusions herein are from the perspective of one of ordinary skill as of that date.

IV. Materials Considered and Relied Upon

14. In reaching the conclusions described in this declaration, I have relied on the documents and materials cited herein as well as those identified in this declaration, including the '241 Patent, the prosecution history of the '241 Patent, and prior art references cited herein. These materials comprise patents, related documents, and printed publications. Each of these materials is a type of document that experts in my field would have reasonably relied upon when forming their opinions.

15. I have also relied on my education, training, research, knowledge, and personal and professional experience in the relevant technologies and systems that were already in use prior to, and within the timeframe of the Critical Date.

- EX-1001: U.S. Patent No. 6,724,241 to Lorenzo Bedarida, et al. (“the '241 Patent”)
- EX-1002: Prosecution History of the '241 Patent (“Prosecution History”)
- EX-1005: U.S. Patent No. 5,872,733 to Buti et al. (“Buti”)
- EX-1006: U.S. Patent No. 4,769,784 to Doluca et al. (“Dolucas”)

- EX-1007: U.S. Patent No. 6,404,274 to Hosono et al. (“Hosono”)
- EX-1008: U.S. Patent No. 6,424,570 to Le et al. (“Le”)
- EX-1009: Japanese Patent Application No. S61-024094 to Ujiie et al. (“Ujiie”)
- EX-1010: U.S. Patent No. 6,091,613 to Yang et al. (“Yang”)
- EX-1011: U.S. Patent No. 6,373,325 to Kuriyama et al. (“Kuriyama”)
- EX-1012: U.S. Patent No. 4,506,350 to Asano et al. (“Asano”)
- EX-1014: Webster’s Unabridged Dictionary, 2d ed. 2001 (excerpts)
- EX-1015: McGraw-Hill Electronics Dictionary, 6th ed. 1997 (excerpts)
- EX-1017: Geiger *et al.*, VLSI Design Techniques for Analog And Digital Circuits (1990), ISBN 0070232539 (excerpts)
- EX-1019: Texas Instruments, *SNx4LS24x, SNx4S24x Octal Buffers and Line Drivers With 3-State Outputs* (Apr. 1985, rev. Oct. 2016)

V. Legal Standards

16. I am not a lawyer and do not provide any legal opinions, but I have been advised that certain legal standards are to be applied by technical experts in forming opinions regarding meaning and validity of patent claims. I have applied the legal standards described below, which were provided to me by counsel for the Petitioner.

17. It is my understanding that assessing the validity of a U.S. patent based on a prior art analysis requires two steps. First, one must construe the terms of the patent claims to understand what meaning one of ordinary skill in the art would have given the terms. Second, after the claim terms have been construed,

one may then assess validity by comparing a patent claim to the “prior art.” I understand that the teaching of the prior art is viewed through the eyes of a POSITA at the time the invention was made. My analysis as to what constitutes a relevant POSITA is set forth above.

A. Legal Standards for Prior Art

18. I understand that a patent or other publication must first qualify as prior art before it can be used to invalidate a patent claim.

19. As I noted earlier, the Critical Date of the '241 Patent is October 25, 2002. In this case, I understand that a U.S. or foreign patent qualifies as prior art if the date of issuance of the U.S. or foreign patent is prior to the Critical Date. I further understand that a printed publication, such as an article published in a magazine or trade publication, qualifies as prior art if the date of publication, or the date the printed publication was otherwise made available to the public, is prior to the Critical Date.

20. I understand that, regardless of the Critical Date, a U.S. or foreign patent qualifies as prior art if the date of issuance of the U.S. or foreign patent is more than one year before the Critical Date. I further understand that a printed publication, such as an article published in a magazine or trade publication, constitutes prior art if the publication, or public availability otherwise, occurs more than one year before the Critical Date.

21. I understand that a U.S. patent or published U.S. application that names another inventor qualifies as prior art if the application for that patent was effectively filed in the United States before the Critical Date.

22. I understand that to qualify as prior art, a reference must contain an enabling disclosure that allows one of ordinary skill to practice the claims without undue experimentation.

23. I understand that documents and materials that qualify as prior art can be used to invalidate a patent claim as anticipated or as obvious.

B. Legal Standard for Priority Date

24. I understand that the “priority date” or “earliest effective filing date” of a patent is the date on which it is filed, or the date on which an earlier-filed U.S. or international patent application was filed if the patentee claims the benefit of priority to that earlier-filed U.S. or international patent application. I further understand that although a foreign priority document may be used to try to overcome certain prior art references, the effective filing date is not the filing date of a foreign priority document.

C. Legal Standard for Anticipation/Obviousness

25. I have been informed by counsel that a patent claim is invalid as “anticipated” under 35 U.S.C. § 102 if each and every element of a claim, as properly construed, is found either explicitly or inherently in a single prior art reference.

Under the principles of inherency, if the prior art necessarily functions in accordance with, or includes the claimed limitations, it anticipates.

26. I have been informed by counsel that a claim is invalid under 35 U.S.C. § 102(a)(1) if the claimed invention was patented, described in a printed publication, or in public use, on sale, or otherwise available to the public before the effective filing date of the claimed invention. I further have been informed that a claim is invalid under 35 U.S.C. § 102(a)(2) if the claimed invention was described in a patent issued under section 151, or in an application for patent published or deemed published under section 122(b), in which the patent or application, as the case may be, names another inventor and was effectively filed before the effective filing date of the claimed invention.

27. I have been informed by counsel that a patent claim is invalid as “obvious” under 35 U.S.C. § 103 in light of one or more prior art references if it would have been obvious to a POSITA, taking into account (1) the scope and content of the prior art, (2) the differences between the prior art and the claims, (3) the level of ordinary skill in the art, and (4) any so called “secondary considerations” of non-obviousness, which include: (i) “long felt need” for the claimed invention, (ii) commercial success attributable to the claimed invention, (iii) unexpected results of the claimed invention, and (iv) “copying” of the claimed invention by others.

28. I have been informed by counsel that a claim can be obvious in light of

a single prior art reference or multiple prior art references. To be obvious in light of a single prior art reference or multiple prior art references, there must be a reason to modify the single prior art reference, or combine two or more references, in order to achieve the claimed invention. This reason may come from a teaching, suggestion, or motivation to combine, or may come from the reference or references themselves, the knowledge or “common sense” of one skilled in the art, or from the nature of the problem to be solved, and may be explicit or implicit from the prior art as a whole. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand it is improper to rely on hindsight in making the obviousness determination.

29. I have been instructed by counsel that if any of these secondary considerations are relied upon to reach a conclusion of obviousness, the law requires that the analysis of such a consideration must be made explicit. I understand that the decision-maker must be careful not to determine obviousness using the benefit of hindsight and that many true inventions might seem obvious after the fact. I understand that the decision-maker should consider obviousness from the position of one of ordinary skill at the time the claimed invention was made and that the decision-maker should not consider what is known today or what is learned from the teaching of the patent.

30. I understand that in order to determine whether a patent claim is obvious, one must make certain factual findings regarding the claimed invention and the prior art. As mentioned above, I understand that the following factors must be evaluated to determine whether a claim is obvious: the scope and content of the prior art; the difference or differences, if any, between the claim of the patent and the prior art; the level of ordinary skill in the art at the time the claimed invention was made; and, if available, the objective indicia of non-obviousness, also known as “secondary considerations.”

31. I understand that the secondary considerations include: commercial success of a product due to the merits of the claimed invention; a long felt need for the solution provided by the claimed invention; unsuccessful attempts by others to find the solution provided by the claimed invention; copying of the claimed invention by others; unexpected and superior results from the claimed invention; acceptance by others of the claimed invention as shown by praise from others in the field or from the licensing of the claimed invention; teaching away from the conventional wisdom in the art at the time of the invention; independent invention of the claimed invention by others before or at about the same time as the named inventor thought of it; and other evidence tending to show obviousness.

32. I understand that, to establish a secondary consideration, the evidence must demonstrate a nexus between that secondary consideration and the claimed

invention.

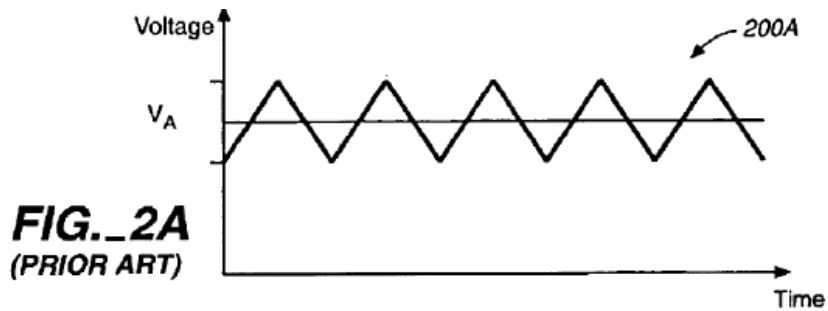
VI. Overview of the '241 Patent

A. Subject Matter Overview

33. The technology in the '241 Patent at issue generally relates to charge pump circuits, which have been used for decades for generating voltages higher than the voltage of the available power source. For example, when a power source supplies a voltage of 5V to a circuit while certain functions of the circuit require a higher voltage of 10V or 15V, a charge pump can be used to provide the higher voltage from the supplied voltage of 5V.

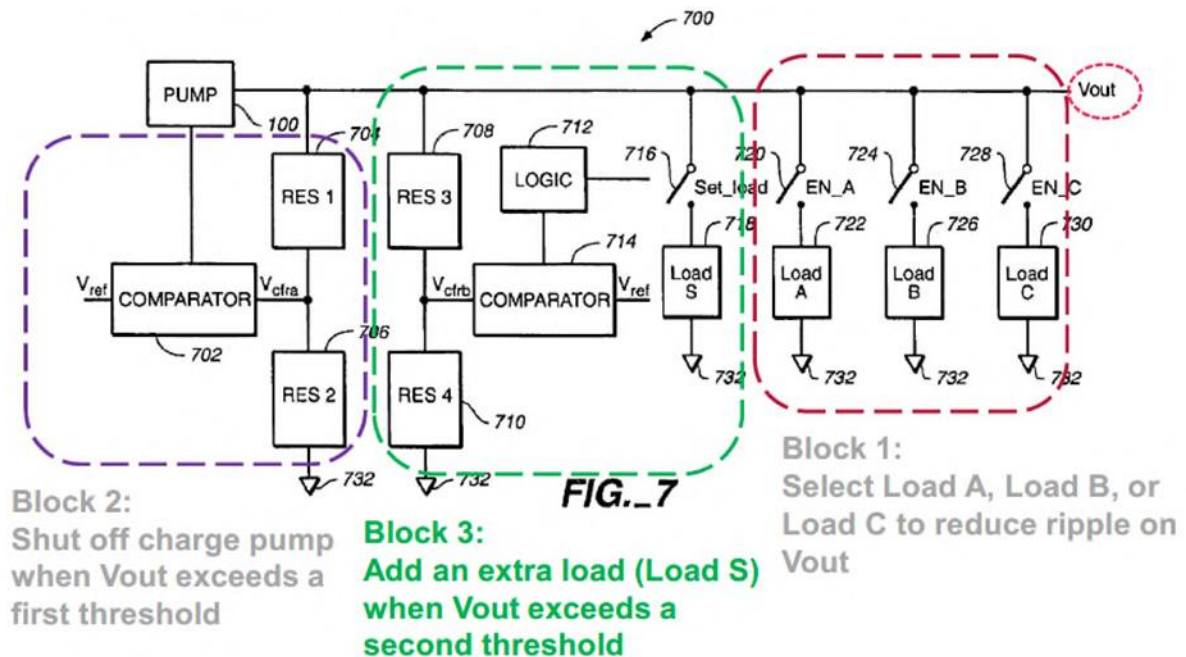
34. Due to this feature, charge pumps have been commonly used in memory devices for program and erase operations, which sometimes require higher voltages than the supply voltage to the memory device. This is also the context of the '241 Patent.

35. The '241 Patent attempts to address a known problem that charge pumps sometimes generate an output voltage containing a voltage ripple due to differences in the capacitances of the charge pump and the load (e.g., a memory device) driven by the charge pump. An example of voltage ripple, which had been known prior to the Critical Date, was described in FIG. 2A of the '241 Patent as prior art. EX-1001, FIG. 2A (reproduced below).



EX-1001, FIG. 2A.

36. To reduce the voltage ripple, the '241 Patent allows the charge pump to turn on and off, and provides paths for current to flow from the charge pump output to the ground, both depending on the output voltage. The '241 Patent describes these techniques with reference to FIG. 7, which, as annotated below, primarily includes three blocks: Block 1, Block 2 and Block 3.



EX-1001, FIG. 7 (annotated)

37. Block 1 shows loads A, B, and C coupled to switches EN_A, EN_B,

and EN_C, respectively, whereas each of loads A, B, and C corresponds to a specific output voltage. When a switch is turned on, a corresponding load is coupled to Vout to form a path from Vout to the ground 732. EX-1001, FIGS. 5A, 5B, 7, 4:33-5:21.

38. Block 2 shows the circuit that shuts down the charge pump when comparator 702 determines that voltage V_{cfra} , which is sampled by resistors RES 1 and RES 2 from charge pump output Vout, exceeds reference voltage V_{ref} . *Id.*, 6:9-17.

39. Block 3 shows the circuit that adds a load when Vout becomes higher than an acceptable level. *Id.*, 6:4-16. The claims of the '241 Patent are directed to either Block 1 alone, Blocks 1-2, or Blocks 1-3.

40. Prior to the priority date of the '241 Patent, there existed numerous products, publications, and patents that implemented or described the functionality claimed in the '241 Patent. As I discuss further below, the methodology of the '241 Patent was well-known in the prior art. Indeed, to the extent there was any problem to be solved in the '241 Patent, it had already been solved in the prior art systems before the priority date of the '241 Patent.

B. File History of the '241 Patent

41. As part of my preparation of this declaration, I reviewed the file history of the '241 Patent (EX-1002). I understand that the '241 Patent was filed

on March 27, 2003 as U.S. Patent Application No. 10/352,733 (the '733 Application), which claimed priority to Italian Patent Application No. MI 2002A 002268, filed on October 25, 2002. EX-1002, at 43. The '733 Application was filed with claims 1-25, which were the same as claims 1-25 of the '241 Patent. *Id.*, at 19-29; EX-1001, Claims 1-25.

42. On April 16, 2003, the applicant of the '733 Application filed an Information Disclosure Statement (IDS), citing nine U.S. patents and two published U.S. patent applications, including Le (EX-1008), which I will discuss below. *Id.*, at 99-100.

43. On December 19, 2003, Examiner Zweizig at the United States Patent and Trademark Office (USPTO) issued a Notice of Allowance (NOA) to the '733 Application, which subsequently issued as the '241 Patent. *Id.*, at 103-107, 111-113; EX-1001, cover page. The Examiner made a brief comment in the NOA: "The Prior Art of record does not appear to disclose a charge pump with a selectable voltage output and a selectable load wherein a load is selected so as to minimize output ripple for a given output voltage." *Id.*, at 107. Along with the NOA, Examiner Zweizig indicated consideration of the references cited in the IDS, as well as consideration of three U.S. patents that the Examiner cited from their own search. *Id.*, at 108-110. With the sole exception of Le, none of the references cited by the Petitioner in this IPR were among those cited and considered by the

Examiner. *Id.*

As I will discuss in detail below, it is my opinion that all claims of the '241 Patent would have been rendered obvious by the prior art references cited in the IPR petition, most of which apparently never considered by the Examiner.

C. Interpretation of the '241 Patent Claims at Issue

44. For purposes of my analysis in this IPR proceeding, I understand that the terms that appear in the claims of the '241 Patent should be interpreted according to their plain and ordinary meaning under the *Phillips* standard. In determining the ordinary and customary meaning, I understand that the words of a claim are first given their plain meaning that those words would have had to one of ordinary skill at the time of the alleged invention. I also understand that the structure of the claims, the specification and file history also may be used to better construe a claim insofar as the plain meaning of the claims cannot be understood. Moreover, I understand that even treatises and dictionaries may be used, albeit under limited circumstances, to determine the meaning attributed by one of ordinary skill to a claim term at the time of filing. I have followed this approach in my analysis. In my opinion, the following claim constructions should be applied by the Board in this proceeding. For all other claim terms considered in this declaration, I have applied the plain and ordinary meaning of those terms.

1. “load” (claims 1, 13)

45. A POSITA would have understood that the term “load” has two possible constructions as used in the ’241 Patent. My opinion that the claims are unpatentable is equally applicable to both constructions.

46. Broadly construed, a “load” is a device that receives electrical power. For example, the specification states that a load can be a “capacitor” or a “current sinker,” which are known electrical circuit components that receive electrical power. EX-1001, 4:34-35. This construction is supported by dictionaries. *See, e.g.*, EX-1014 (Webster’s Unabridged Dictionary) (2d ed. 2001) (“*Elect.* . . . “a device that receives power”); EX-1015 (McGraw-Hill Electronics Dictionary) (6th ed. 1997) (“A device that consumes electric power”).

47. Under a narrower construction, a “load” is a device that absorbs surplus charge to reduce voltage ripple when compared to a case without the device. The specification explains that a load can be a “capacitor” or a “current sinker,” which is a device that absorbs surplus charge to produce a minimum voltage ripple. *See, e.g.*, EX-1001 at Abstract (describing that the pump circuit “uses a plurality of selectable loads to minimize the voltage ripples of the pumped output by selecting the appropriate load for a preselected pump voltage”); *see also* 4:5-8, 4:64-65, 9:20-24 (claim 8), 9:34-38 (claim 10).

2. “a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit” (claim 1)

48. I understand that this phrase is a means-plus-function limitation,

whose interpretation is subject to pre-AIA 35 U.S.C. 112, sixth paragraph.

49. The function of this limitation is “selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit.” In my opinion, the function should be construed as: choosing a load based on the target pump voltage, such that the load is coupled to the output of the pumping circuit when the target pump voltage is selected.

50. The '241 Patent explains that each load (e.g., Load A, B, or C) is “associated” with a specific pump voltage and that the load is attached to the output when that specific pump voltage is selected. EX-1001, 4:33-51. The attachment of the load is triggered by the pump voltage selection, not a later event. *Id.*, 4:33- 51, 7:7-16, 7:31-42. The '241 Patent also discloses that a different load (e.g., Load S) can be added if needed based on a measurement of the output voltage; that different load is not described as being “associated” with the particular output voltage because it is not added at the time of the target pump voltage selection. *Id.*, 6:8-17, 7:7-16, 7:31-42.

51. To perform the function of this limitation, the '241 Patent discloses switches 320, 324, and 328 and their respective control signals EN_A, EN_B, and EN_C. For example, the specification of the '241 Patent states that the “three switches 320, 324, and 328 together with their respective control signals EN_A, EN_B and EN_C form a load selector means that reduce voltage ripple at the

charge pump output to a minimum.” EX-1001, 4:47-50; *see also id.*, FIG. 3, 4:2-8, 4:52-5:15. The ’241 Patent further describes structural embodiments for switches 320, 324, and 328 and indicates that the switches can be structurally implemented with transistors. *Id.*, FIGS. 5A-5B.

52. The ’241 Patent further discloses a “controller” as part of the structure that generates control signals EN_A, EN_B and EN_C for controlling switches 320, 324, and 328. EX-1001, 4:51-61. If the controller is considered part of the structure that performs the recited function, then the structure would include switches 320, 324, and 328 and their control signals EN_A, EN_B, and EN_C and the controller. My opinion that the claims are unpatentable is applicable regardless whether the controller is considered part of the structure to perform the recited function.

3. “target output pump selector for shutting down the variable charge pump circuit when the target output pump voltage (Vcfra) is greater than or equal to a reference voltage (Vref)” (claim 2) and “a target output pump selector sampling the output of the pump circuit for shutting down the variable charge pump circuit whenever the sampled output voltage (vcfra) is greater than or equal to a reference voltage (Vref)” (claim 13)

53. I understand that these limitations are means-plus-function limitations, as evidenced by claims 3, 12 and 13 referring to these limitations as the “target output selector means.” EX-1001, claims 3, 12 and 13.

54. The functions of these limitations are “shutting down the variable charge pump circuit when the target output pump voltage (Vcfra) is greater than or

equal to a reference voltage (V_{ref})” for claim 2 and “sampling the output of the pump circuit for shutting down the variable charge pump circuit whenever the sampled output voltage (V_{cfra}) is greater than or equal to a reference voltage (V_{ref})” for claim 13.

55. For both of the recited functions, the specification of the '241 Patent discloses comparator 702 as the corresponding structure.

4. “a load selector means coupled to the output pump for selecting a load that satisfies a specific pump voltage” (claim 13)

56. I understand that this limitation is a means-plus-function limitation.

57. The function is “selecting a load that satisfies a specific pump voltage.” EX-1001, claim 13.

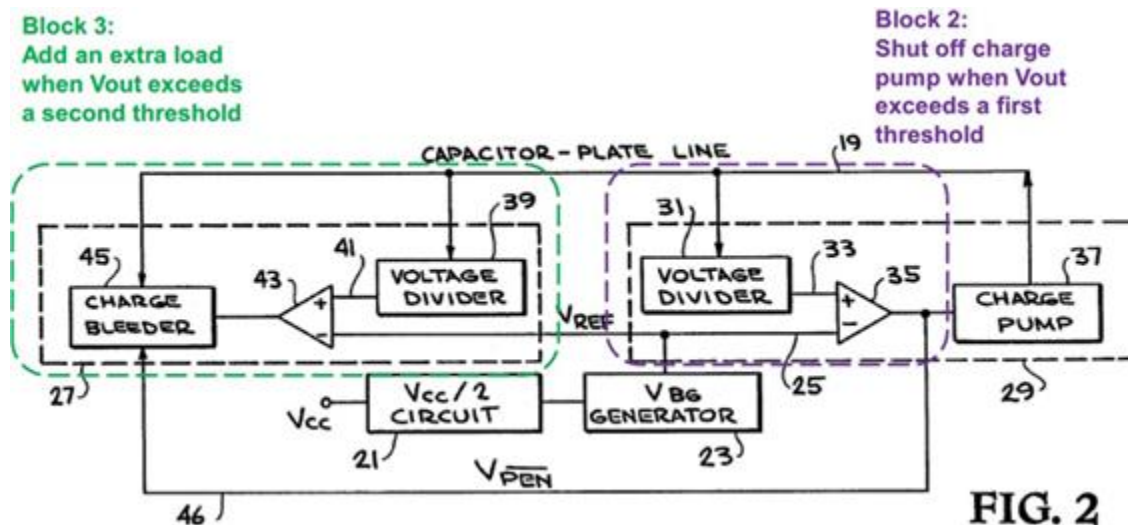
58. To the extent that this function, in particular “satisfies a specific pump voltage,” means “selectively coupling a load associated with a specific pump voltage” or similar, as recited in claim 1, the structure of the “load selector means” of claim 13 is the substantially the same as the structure of the “load selector means” of claim 1.

VII. GROUND 1A: Claims 1-3, 24, and 25 are rendered obvious by Doluca and Buti

A. Overview of Doluca

59. I have fully reviewed Doluca. In my understanding, Doluca’s disclosure includes the following aspects.

60. Doluca is directed to a “capacitor-plate bias generator” used in memory devices. See EX-1006, Title, Abstract. The capacitor-plate bias generator circuit (which I also refer to as “bias circuit”) includes a charge pump for supplying voltage to memory devices. EX-1006, 1:1-12, 1:64-2:39. To generate a desired output voltage, the bias circuit has an enabling/disabling control circuit (“Block 2” in Doluca’s FIG. 2 below) and a charge bleeder circuit (“Block 3” in Doluca’s FIG. 2) to regulate the charge pump output voltage. *Id.*, Abstract, 1:64-2:39.



EX-1006, FIG. 2 (annotated)

61. In FIG. 2 of Doluca, the enabling/disabling control circuit has a voltage divider 31 that receives a feedback signal, via capacitor-plate line 19, from the output of charge pump 37. *Id.*, 3:54-5:20, FIG. 2. The feedback signal is the same as the charge pump output V_{CP} . *Id.* Voltage divider 31 obtains a fraction of

V_{CP} and provides the fraction as an input to comparator 35, which compares fraction with a reference voltage, V_{REF} . *Id.* Depending on the comparison result, the output of comparator 35 generates an enable signal $\overline{VPEN}$ that controls charge pump 37 and charge bleeder 45 to turn on or off. *Id.*

62. In FIG. 2 of Doluca, the charge bleeder circuit removes charge from the output storage capacitor of the charge pump to reduce the output voltage as commanded. The charge bleeder circuit is a dynamic load that is selectively coupled to the output when the output voltage is above a reference threshold that works to lower the output voltage to the commanded reference level. A POSITA would have understood that this is a form of a shunt regulator.

B. Buti (EX-1005)

63. I have fully reviewed Buti. In my understanding, Buti's disclosure includes the following aspects.

64. Buti is directed to controlling the ramp-up rate of output voltage V_{out} of a charge pump circuit, i.e., controlling the speed at which V_{out} increases while the charge pump circuit is used provide voltages to memory devices. EX-1005, Title, Abstract; 1:5-4:15, 4:61-5:26, FIG. 1A. It is my understanding and within Buti's disclosure that controlling the V_{out} ramp-up rate is a form of regulating the charge pump output to prevent V_{out} from increasing too fast. *Id.*; *see also id.*, 5:27-9:28; FIGs. 1B-6. As shown in FIG. 6 of Buti below, V_{out} increases at lower

speeds for circuits corresponding to curves B and C (which implement Buti's ramp-rate control circuits) than for the circuit corresponding to curve A (which does not implement Buti's ramp-rate control circuits). *Id.*, FIG. 6, 9:8-28. For example, comparing curves A and B, it takes longer ramp-up time for curve B to reach 12.95V than curve A; at any given time before curve B reaches 12.95V, the circuit corresponding to curve B generates less voltage at V_{out} than does the circuit corresponding to curve A.

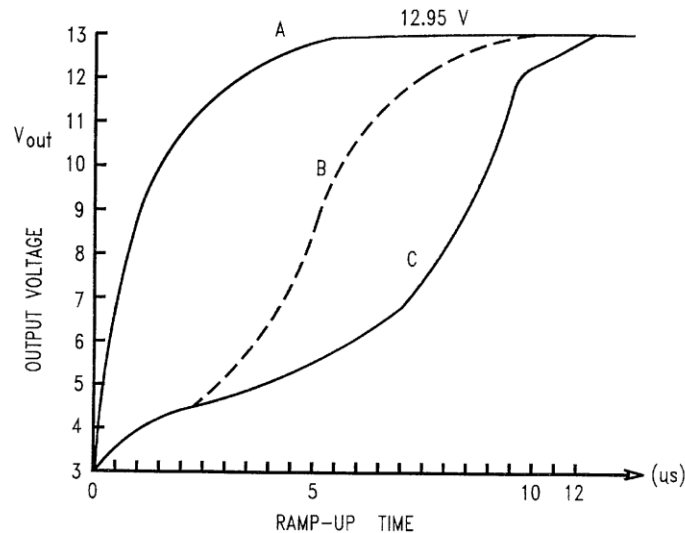
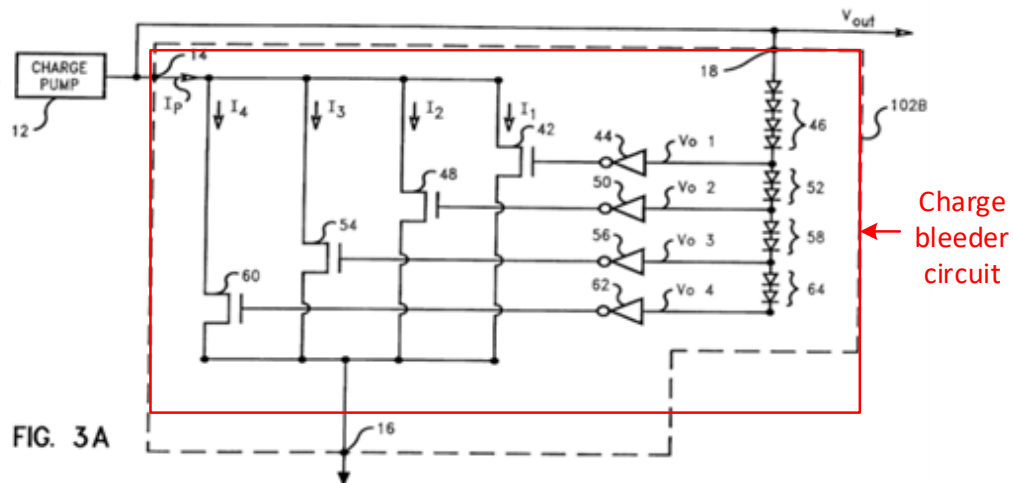


FIG. 6

EX-1005, FIG. 6.

65. Buti reduces V_{out} ramp-up rate using a charge bleeding circuit coupled to the charge pump output to regulate the current flow between the pump output and the ground potential based on the magnitude of V_{out} . *Id.* As an example, Buti describes bleeding circuit 102B in FIG. 3A, which is coupled between the output

of charge pump 12 and the ground potential (connected to node 16). *Id.*, FIG. 3A. Bleeding circuit 102B has four bleeding paths, illustrated in FIG. 3A as arrows next to labels I_1 to I_4 . *Id.* Each bleeding path is controlled using a chain of diodes coupled with an inverter and an n-channel field-effect transistor (FET), and is associated with a threshold voltage for turning the path on/off. Taking the path corresponding to I_1 as an example, the path is controlled by the chain of diodes (also known as “series diodes” or “diode stack”) 46, inverter 44, and FET 42.



EX-1005, FIG. 3A (annotated)

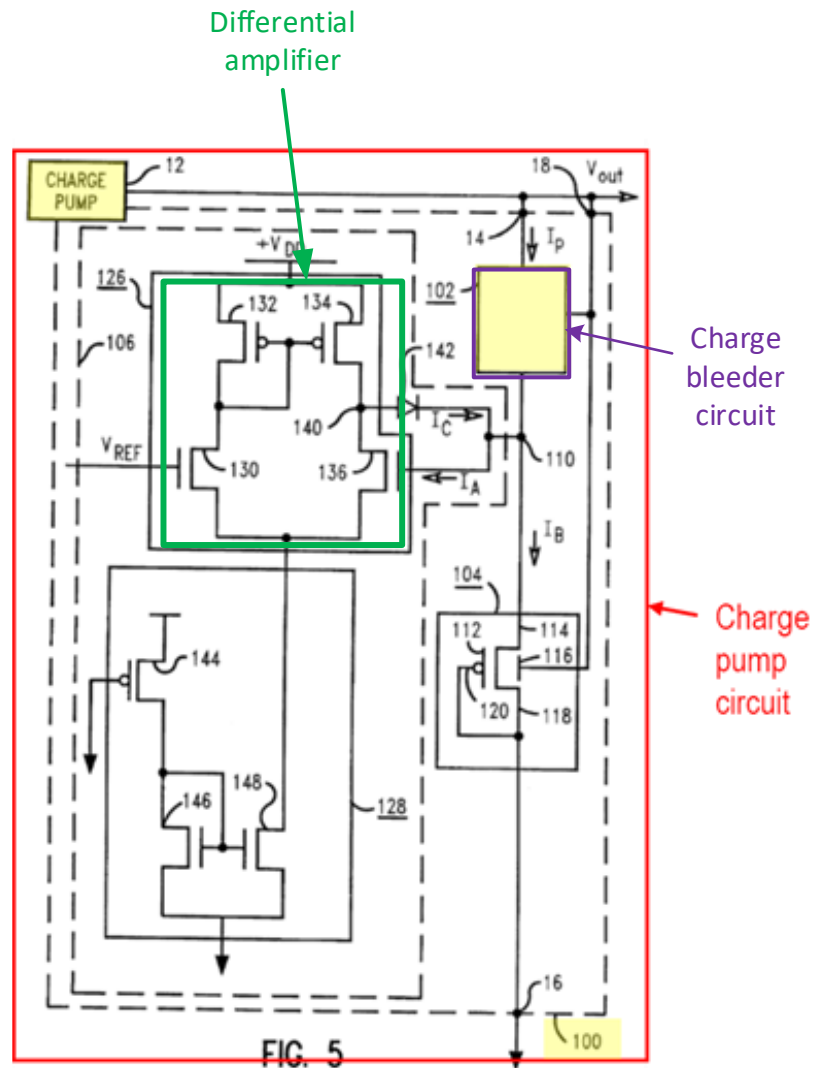
66. Diode stack 46 corresponds to a threshold voltage (5.78V, see EX-1005, 7:12-23), which is determined based on the physical properties of the diodes in the stack. When V_{out} exceeds the threshold voltage of diode stack 46, diode stack 46 is forward-biased (or “activated”), allowing current from the charge pump output to flow through diode stack 46. The current produces a logic “1” at the

input of inverter 44, which outputs a logic “0.” The logic “0” output by the inverter 44 is propagated to the gate terminal of FET 42. Because FET 42 is an n-channel FET (specifically, an N-type metal–oxide–semiconductor [NMOS] transistor), a logic “0” at the gate turns FET 42 off, so no bleeding current flows through it. FET 42 is thus deactivated. Conversely, when V_{out} is below the threshold voltage of diode stack 46, diode stack 46 is reverse-biased (or “deactivated”), thereby producing a logic “0” at the input of inverter 44. Inverter 44 thus outputs a logic “1,” which is propagated to the gate terminal of FET 42 and turns FET 42 on, allowing bleeding current I_1 to flow through it to the ground potential via node 16. FET 42 is thus activated.

67. The bleeding paths corresponding to I_2 to I_4 can be controlled following mechanisms similar to that described above with respect to the bleeding path corresponding to I_1 . The threshold voltages corresponding to diode stacks to activate/deactivate FETs 48, 54, and 60, are about 7.6V, 9.5V, and 11.43V, respectively. *See id.*, 7:24-58.

68. Buti’s charge bleeder circuit 102B can be implemented along with other circuit components of a charge pump circuit to supply voltage to a memory device. Buti shows an example of a charge pump circuit in FIG. 5, which includes a charge bleeder circuit 102 that can be implemented as charge bleeder circuit 102B of FIG. 3. EX-1005, 8:1-32, FIG. 5. The circuit in FIG. 5 also has voltage

setting circuit 106, which includes a differential amplifier (“diff amp”) 126. Diff amp 126 functions as a comparator.



EX-1005, FIG. 5 (annotated)

C. Combination of Doluca with Buti

69. I believe that a POSITA would have understood that Doluca and Buti describe related technologies, and that their teachings can be combined to address various technical needs. Doluca discloses a charge pump circuit to supply voltages

to memory devices. See ¶ 60. Buti discloses its charge pump circuit in the context of supplying voltage to memory devices, similar and analogous to the disclosure of Doluca. See ¶¶ 60, 68. Both Doluca and Buti contemplate using a charge bleeder circuit to regulate the output voltage of the charge pump. See ¶¶ 60-62, 64-68. Moreover, similar to the structure of Buti's diff amp 126, which operates in conjunction with Buti's charge bleeder circuit, see ¶ 68, Doluca's comparator 43, which controls Doluca's charge bleeder 45, is also structured as a diff amp. EX-1006, FIG. 5 (reproduced below).

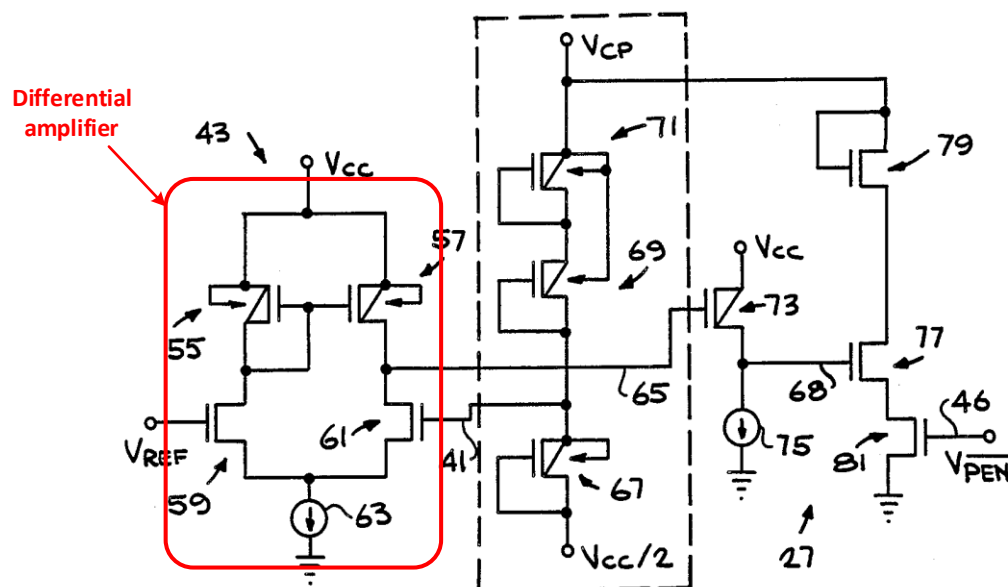


FIG. 5

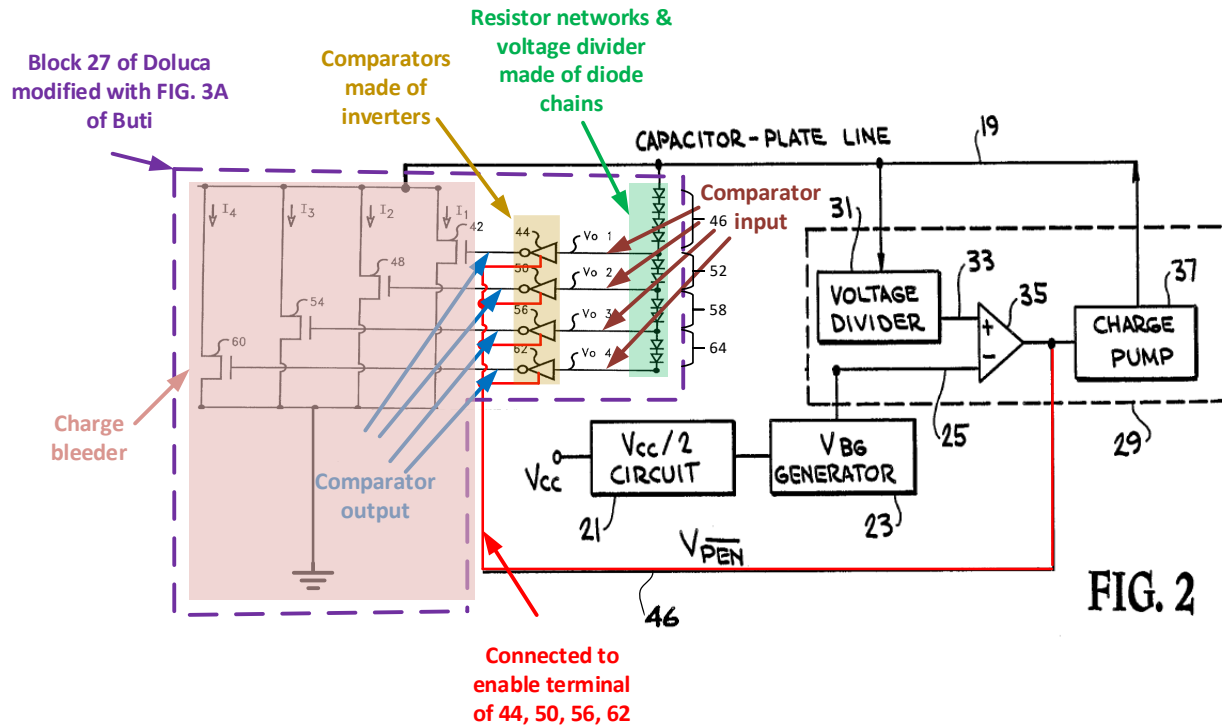
EX-1006, FIG. 5 (annotated).

70. While disclosing that bleeder control circuit 27 controls charge bleeder 45 to regulate the output voltage on capacitor line 19, Doluca illustrates charge bleeder 45 in a block without structural or operational detail. EX-1006,

FIG. 2. Doluca's silence in this regard would have motivated a POSITA to seek supplemental material about charge bleeder examples, and/or how to implement the example charge bleeders to lower the charge pump output voltage when it becomes excessive. I believe that in doing so, among other sources, a POSITA would have considered the charge bleeder disclosed by Buti.

71. Buti, like Doluca, discloses using a charge bleeder circuit to regulate the charge pump output voltage. EX-1005, Title, Abstract, 1:5-4:15, 4:61-9:28. Buti's charge pump circuit in FIG. 5 includes charge pump 12 and a charge bleeder circuit 102, with the latter including a structure as shown by circuit 102B in FIG. 3A. *Id.* Bleeder circuit 102B includes (i) FETs 42, 48, 54, and 60, each of which can be selectively coupled to output V_{out} of charge pump 12 at node 14, depending on the level of V_{out} , to regulate the pump output voltage, and (ii) diode stacks 46, 52, 58, and 64 that control activation/deactivation of the FETs depending on whether V_{out} exceeds a respective threshold voltage. See ¶¶ 65-68.

72. Accordingly, in my opinion, a POSITA would have found it obvious to combine Doluca and Buti and make routine and obvious modifications. An example circuit as a result of the combination and modifications is provided below with annotations showing some relevant features. In this circuit, Doluca's bleeder control circuit 27 of FIG. 2 is implemented based on Buti's charge bleeder circuit 102B of FIG. 3B.



EX-1006, FIG. 2 (modified in view of EX-1005, FIG. 3, annotated)

73. In the above circuit obtained by combining and modifying Doluca's circuit with Buti's charge bleeder circuit, FETs 42, 48, 54, and 60 and the bleeding paths corresponding to I_1 to I_4 operate as Doluca's charge bleeder 45, according to a principle similar to that described above. See ¶¶ 65-68.

74. It is well-known that diodes, when forward-biased, have a forward voltage drop whose value depends upon the diode type. It is also well-known that each diode has intrinsic resistance and has properties similar to a resistor.

Accordingly, in the above circuit, each of diode stacks 46, 52, 58, and 64 can be regarded as a resistor voltage drop network, and diode stacks 46, 52, 58, and 64 together can be regarded as four resistors with associated diodes connected in

series. The diode stacks 46, 52, 58, and 64 together effectively form a voltage divider, which operates in a manner similar to voltage divider 39 in FIG. 2 of Doluca. Using the bleeding path corresponding to I_1 as an example, the voltage value V_{o1} at the input of inverter 44 equals a fraction of the capacitor-plate line 19 voltage V_{CP} (which equals the output voltage of charge pump 37), where the fraction is determined based on the voltage division between the resistance of diode stack 46 and the combined resistance of diode stacks 52, 58, and 64.

75. Also in the above circuit, each of inverters 44, 50, 56, and 62 operates as a comparator corresponding to a bleeding path, similar to comparator 43 illustrated in FIG. 2 of Doluca. The idea and practice of using inverters (or likewise, buffers) for comparison have been well-known for decades. A buffer has a structure very similar to an inverter. Contrary to an inverter whose output is the logic opposite of the input, a buffer outputs the same logic value as the input. A POSITA would have found it obvious to use buffers in lieu of inverters 44, 50, 56, and 62 in the circuit shown in ¶ 72. A resultant circuit would look like the one illustrated below:

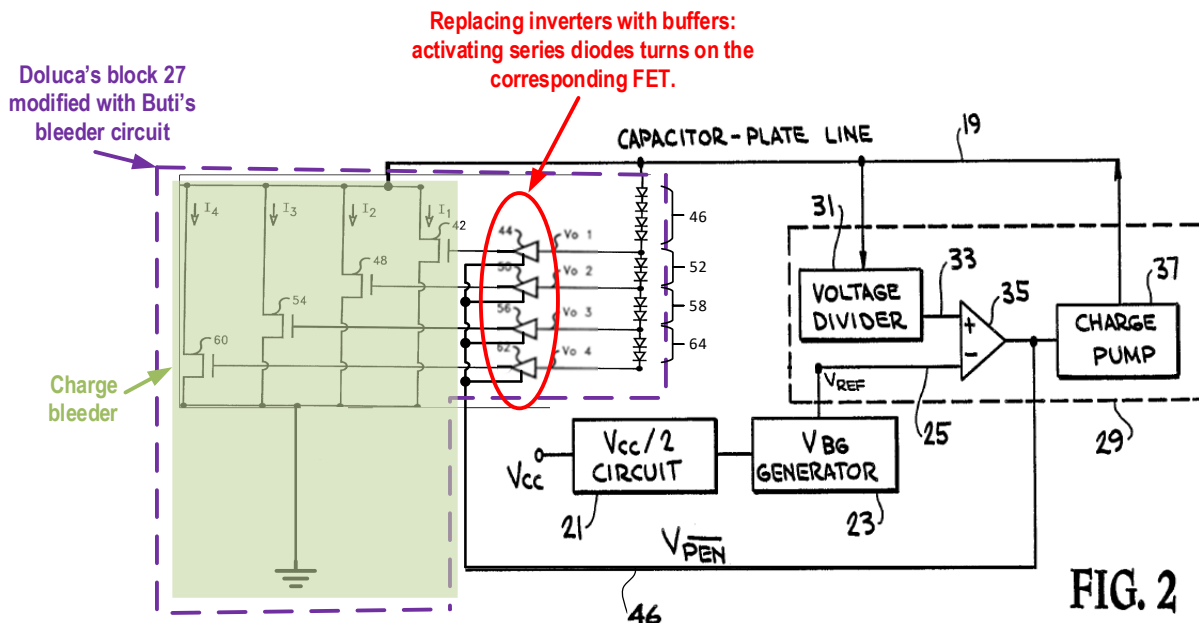


FIG. 2

76. It has been well-known for decades that a comparator can have an enable terminal in addition to multiple input terminals and an output terminal. EX-1019. A fixed level comparator is formed using an inverter or a buffer with a Schmitt trigger input. Inverters and buffers often utilize enable signals. Accordingly, consistent with Doluca's use of $\overline{VPEN}$ on line 46 to enable/disable charge bleeder 45 (see EX-1006, FIG. 2, 5:9-19), a POSITA would have found it obvious to use the same $\overline{VPEN}$ signal to enable/disable the comparators formed by inverters 44, 50, 56, and 62 in the above circuit of Doluca-Buti combination, thereby enabling/disabling the bleeding paths in the above circuit. The connection of the $\overline{VPEN}$ signal to the enable terminal of each of inverters 44, 50, 56, and 62, in my opinion, would have been readily conceived by a POSITA given the context

of the Doluca-Buti combination.

77. With the understanding that inverters 44, 50, 56, and 62 in the Doluca-Buti combination of ¶ 72 can function as comparators, a POSITA would have found it obvious to make a further design change by replacing the inverter-based, fixed-level comparators with operational amplifier (op-amp)-based or two-input comparators, such as comparator 43 of Doluca. A resultant circuit is illustrated below, showing the modified Doluca-Buti bias circuit with comparators, and also separately showing Doluca's modified block 27. In this circuit, each comparator has its “-” input terminal coupled to V_{REF} and its “+” input terminal coupled to the output of the corresponding diode stack. When a diode stack is forward biased, the corresponding comparator outputs a logic ‘1’ if the voltage at the “+” input terminal (which equals the charge pump output voltage minus the voltage drop caused by the diode stack) is greater than V_{REF} . Conversely, the corresponding comparator outputs a logic ‘0’ if the diode stack is reverse biased, or if the voltage at the “+” input terminal is less than V_{REF} .

1005, FIG. 3, annotated)

78. As I have explained above, the Doluca-Buti combination provides an example of implementing Doluca's bleeder control circuit 27 based on Buti's charge bleeder 102B. *See* ¶ 72. With the knowledge of both Doluca and Buti, a POSITA would have found the combination obvious. Besides the above-described modifications to the circuit of the Doluca-Buti combination, a POSITA would have been motivated to make other obvious modifications to change or optimize circuit operations. I explain some of these additional modifications in later sections of this Declaration.

79. As I explain below, the combination of Doluca and Buti renders obvious claims 1-3, 24, and 25.

D. Analysis

1. Claim [1pre]: A charge pump circuit for generating a charge pump voltage having minimal voltage ripples, comprising:

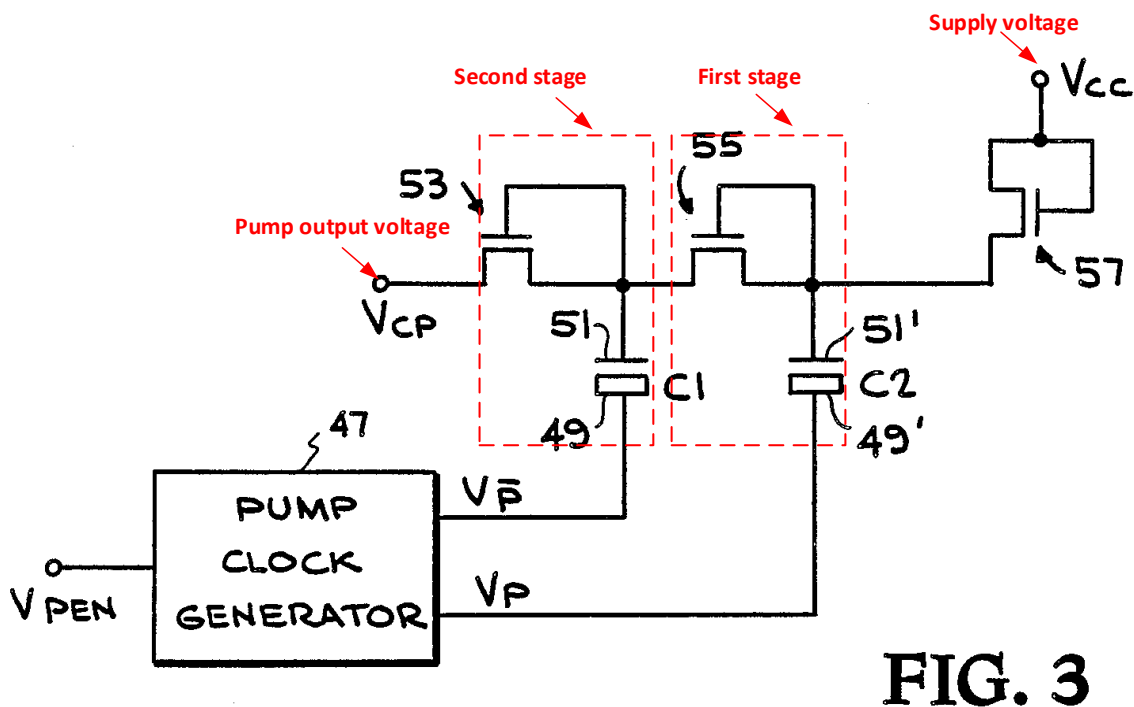
80. The "bias circuit" of Doluca is a charge pump circuit, which includes charge pump 37. *See, e.g.*, EX-1006, Abstract, 3:26-4:30, FIGS. 2-3; *see also id.* 1:64-2:39. Charge pump 37 outputs a voltage V_{CP} on capacitor-plate line 19. *Id.*, 3:26-4:17.

81. Doluca describes using its bias circuit to generate a "stable" voltage that "remain[s] within a narrow range around a design voltage." *Id.*, 2:13-39, 1:29-38. I believe that a POSITA would have understood that this description of Doluca

teaches that the bias circuit outputs a charge pump voltage that stays close to a target voltage, and accordingly, generates a charge pump voltage “having minimal voltage ripples.”

2. Claim [1a]: a) a pumping circuit comprising one or more stages operable to receive a supply voltage and generate a selected one of a plurality of pump voltages;

82. Doluca’s bias circuit of FIG. 2 includes charge pump 37, the schematic of which is shown in FIG. 3. EX-1006, FIG. 3, 2:51-55. Charge pump 37 has two stages with respective capacitors C1 and C2 and respective diode-connected NMOS transistors 53 and 55. *Id.* Charge pump 37 receives source voltage V_{CC} as the supply voltage and generates output V_{CP} . EX-1006, 5:19-54, FIG. 3 (reproduced below).



EX-1006, FIG. 3 (annotated)

83. To provide bias voltage for memory device operation, Doluca teaches that an ideal value of V_{CP} should equal $V_{CC}/2 + K$, where K is a constant having a value $K > V_{CC}/2 + V_T$. EX-1006, 2:65-3:54. The value of K can be chosen within a specified range, such as between 3.5V and 4V. *Id.*, 3:31-54. In other words, one can control charge pump 37 to generate a selected pump output voltage by selecting the value of K . This, in my opinion, is what is described by the claimed feature of [1a] and would have been readily understood by a POSITA.

84. In addition to choosing the value K , the Doluca-Buti combination given in ¶ 72 provides another obvious mechanism of selecting the pump output voltage. As I have described earlier with reference to the circuit in the Doluca-Buti combination, each bleeding path is controlled depending on the activation or deactivation of the corresponding diode stack. See ¶¶ 65-67, 71-73. Still using the bleeding path corresponding to I_1 as an example, the activation/deactivation of the corresponding diode stack (labeled as diode stack 46 in FIG. 3A of Buti) depends on whether the voltage on capacitor-plate line 19 (labeled as V_{CP} in FIG. 2 of Doluca) exceeds the threshold voltage of the diode stack. See ¶ 66. I believe that a POSITA would have understood that the threshold voltage of diode stack 46 can be selectively changed by increasing or decreasing the number of diodes in the stack: adding more diodes to the stack increases the threshold voltage, while removing some diodes from the stack decreases the threshold voltage. A POSITA would

have understood that this design selection of diode stack 46 determines when the corresponding bleeding path is activated to regulate the charge pump output voltage V_{CP} . As such, by selecting the number of diodes in diode stack 46, the POSITA can select the specific pump output voltage. In my opinion, this selection mechanism reads on the feature of [1a].

3. Claim [1b]: a plurality of loads selectively coupleable to an output of the pumping circuit, each load associated with a specific pump voltage; and

85. Doluca's FIG. 2 shows that the bias circuit includes bleeder control circuit 27 and pump control circuit 29, which operate to regulate the voltage on capacitor-plate line 19 (i.e., output voltage V_{CP} of charge pump 37). *Id.*, 3:54-5:20, FIG. 2. As I have noted previously, a POSITA would have found it obvious to implement Doluca's bleeder control circuit 27 according to Buti's bleeder circuit 102B. *See* ¶ 72. In the resultant circuit of the Doluca-Buti combination, FETs 42, 48, 54, and 60 are selectively activated or deactivated. *See* ¶ 65-67, 71-73. For example, when the gate terminal of FET 42 receives a voltage corresponding to logic "1," FET 42 is activated to allow current I_1 to flow from its drain terminal (coupled to the output of charge pump 37 via capacitor-plate line 19) to its source terminal (coupled to the ground). FETs 48, 54, and 60 manifest similar behaviors when activated by a logic "1" at their respective gate terminals. This behavior of FETs 42, 48, 54, and 60 would have been readily understood by a POSITA.

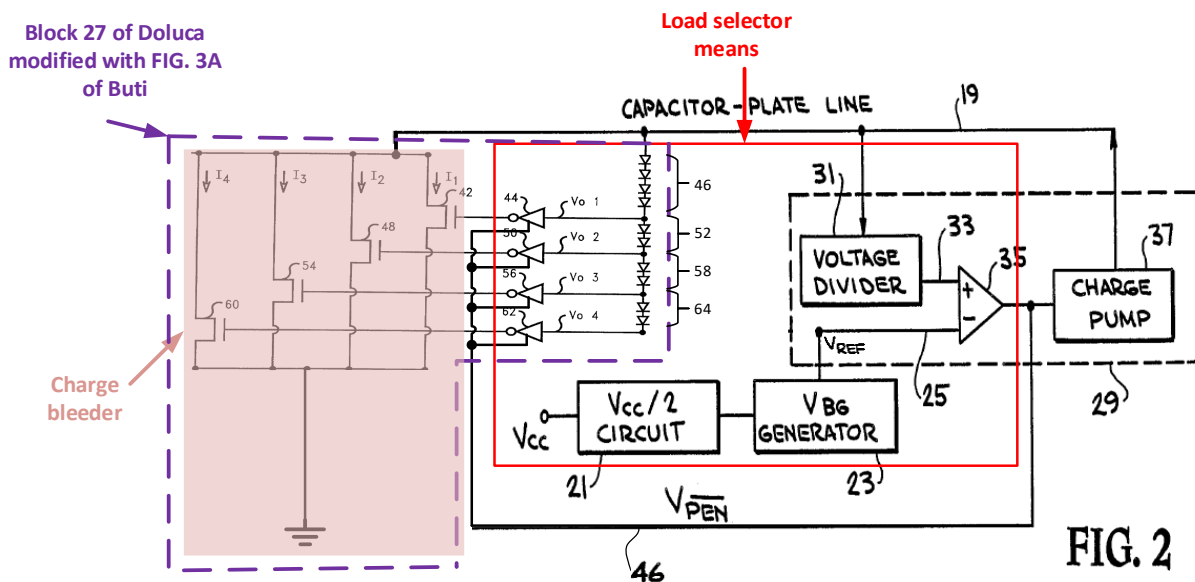
86. In the context of charge pump circuits, a "load" typically is

characterized by its ability to remove charge from the output storage capacitor of the charge pump. A large load would remove more charge per unit time than say a small load. Given the behaviors of FETs 42, 48, 54, and 60, a POSITA would have considered these FETs as “loads” of charge pump 37. Each of these FET loads 42, 48, 54, and 60 is associated with a specific pump output voltage, the value of which equals the threshold voltage of the corresponding diode stack(s). For example, FET 42 is associated with a pump voltage that corresponds to the threshold voltage of diode stack 46; FET 48 is associated with a pump voltage that corresponds to the combined threshold voltage of diode stacks 46 and 52; FET 54 is associated with a pump voltage that corresponds to the combined threshold voltage of diode stacks 46, 52 and 58; and FET 60 is associated with a pump voltage that corresponds to the combined threshold voltage of diode stacks 46, 52, 58 and 60. Example voltage ranges for the output voltage (e.g., V_{CP}) are provided in Table 1 of Buti. EX-1005, 7:47-58. Depending on the value of charge pump output V_{CP} , each of FET loads 42, 48, 54, and 60 can be selectively activated, i.e., selectively coupled to charge pump 37. Accordingly, in my opinion, the Doluca-Buti combination reads on the feature of [1b].

4. Claim [1c]: c) a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit.

87. I have explained above that FET loads 42, 48, 54, and 60 can be selectively coupled to the output of charge pump 37 of the circuit in the Doluca-

Buti combination. See ¶¶ 85-86. I believe a POSITA would have considered the circuit components involved in the above-described operations as “load selector means,” as illustrated below. These circuit components forming the load selector means include Doluca’s voltage divider 31, comparator 35, voltage divider 39 (and/or its equivalent in the Doluca-Buti combined circuit, as discussed below), comparator 43 (and/or its equivalent in the Doluca-Buti combined circuit, as discussed below), $V_{CC}/2$ circuit 21 and V_{BG} generator 23.

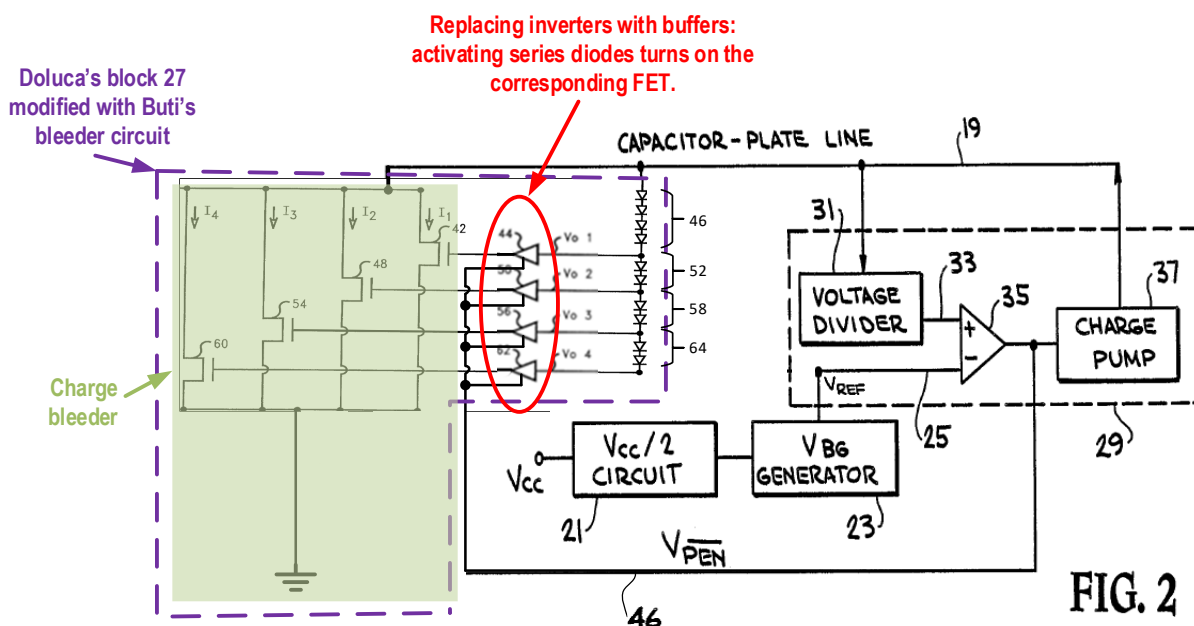


EX-1006, FIG. 2 (modified in view of EX-1005, FIG. 3, annotated)

88. In the circuit of Doluca-Buti combination provided in ¶¶ 72 and 87, when the voltage on capacitor-plate line 19 V_{CP} increases above the threshold voltage of diode stack 46, the input of inverter 44 is logic “1” and the output of inverter 44 is logic “0.” This would *deactivate* FET 42. Similarly, as V_{CP} increases, FETs 48, 54, and 60 are subsequently *deactivated*. With a simple and

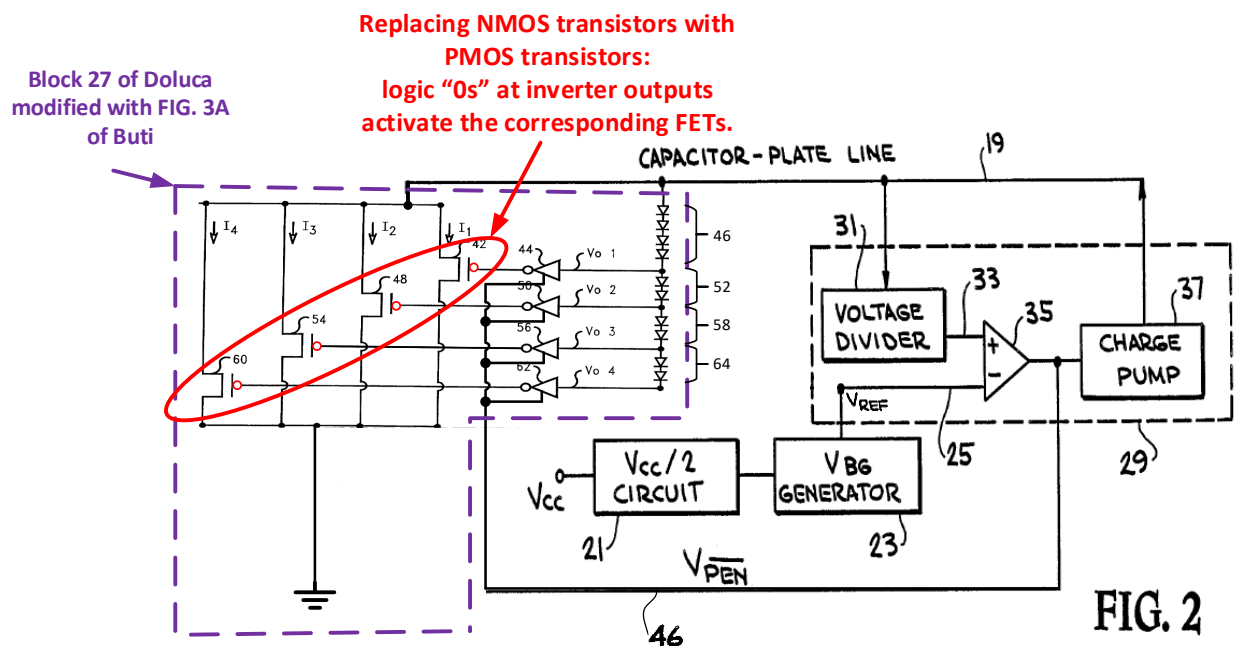
obvious design change, the increase of V_{CP} can, conversely, lead to the *activation* of the FETs 42, 48, 54, and 60.

89. One way of such design change is to replace inverters 44, 50, 56, and 62 with buffers, as illustrated below in red. A buffer has a structure very similar to an inverter. Contrary to an inverter whose output is the logic opposite of the input, a buffer outputs the same logic value as the input. With this design change, when V_{CP} increases above the threshold voltage of FET 42, the input and the output of now-buffer 44 are both logic “1.” This would activate FET 42. Similarly, as V_{CP} increases, FETs 48, 54, and 60 are subsequently *activated* now that inverters 50, 56, and 62 have been replaced with buffers.



EX-1006, FIG. 2 (modified in view of EX-1005, FIG. 3, annotated)

90. Alternative to replacing inverters 44, 50, 56, and 62 with buffers, another simple and obvious design change would be to use P-type metal–oxide–semiconductor (PMOS) transistors, instead of NMOS transistors, to form FETs 42, 48, 54, and 60, along with Buti’s inverters 44, 50, 56, and 62, as illustrated below. A PMOS transistor is activated when its gate terminal receives a logic “0.” With this change, increasing V_{CP} can also lead to the subsequent activation of FETs 42, 48, 54, and 60. Moreover, a POSITA would have readily understood that, in the various alternative obvious modifications I have described above, the inverters or buffers can further be replaced with op-amp-based comparators. See ¶ 77.



EX-1006, FIG. 2 (modified in view of EX-1005, FIG. 3, annotated)

91. I believe a POSITA would have been motivated to make either of the two changes described in ¶¶ 89 and 90. First, these changes merely involve

substituting an existing circuit component for its logic complement (e.g., substituting a buffer for an inverter or substituting a PMOS transistor for an NMOS transistor) to realize a similar outcome, which in this case is to control the output voltage of the charge pump circuit. Both the existing circuit component and the substituting circuit component are basic logic circuit components that are routinely used by a POSITA. In circuit design, it would have been a common situation where a POSITA needs to change a logic value of a signal, and it would have been a common practice for a POSITA to modify an existing circuit in a manner similar to those described in ¶¶ 89 and 90. Moreover, the modifications described in ¶¶ 89 and 90 are consistent with Doluca's objective of regulating V_{CP} , i.e., turning on charge bleeder 45 when V_{CP} exceeds certain target values. EX-1006, 2: 13-33, 4:10-65. The modifications described in ¶¶ 89 and 90 both achieve Doluca's objective: When V_{CP} becomes higher than the threshold voltage corresponding to a bleeding path, the FET load of that bleeding path is activated such that current can flow from the charge pump output to the ground, thereby reducing V_{CP} or at least slowing down the increase of V_{CP} . Because of these reasons, I believe that a POSITA would have found it obvious to combine Doluca and Buti and modify the resultant circuit such that the FET loads are selectively coupled, by a load selector means, to the charge pump output as the output voltage increases.

5. Claim 2: The charge pump circuit of claim 1, wherein the load selector means includes a target output pump selector for shutting down the variable charge pump circuit when the target

output pump voltage (V_{cp}) is greater than or equal to a reference voltage (V_{ref}).

92. Consistent with the Doluca-Buti combination shown in ¶ 87 and the modifications described in ¶¶ 89 and 90, a POSITA would have considered voltage divider 31 and comparator 35 as performing the function of the “target output pump selector.” According to Doluca, pump control circuit 29 “derive[s] a voltage which is a certain fraction of the voltage on line 19” using considered voltage divider 31, “compare[s] this voltage with the V_{REF} voltage” using comparator 35, and “turn[s] the charge pump[] on or off in response to the difference between the two voltages” based on the output V_{33} of comparator 35. EX-1006, 3:55-4:52, FIG. 2. Specifically, the charge pump is turned on when $V_{33} \leq V_{REF}$, and is turned off when $V_{33} > V_{REF}$, where V_{33} equals a fraction of pump output voltage V_{CP} and V_{REF} is a reference voltage generated by V_{BG} generator 23. *Id.*, 3:55-4:52, 6:64-7:23, FIGS. 2 and 6. I believe that a POSITA would have understood that comparing a fraction of V_{CP} with V_{REF} is mathematically equivalent to comparing the entirety of V_{CP} with a multiple of V_{REF} . In this sense, the “multiple of V_{REF} ” would read on the claimed “reference voltage (V_{ref}).” Alternatively, Doluca’s teaching would have made it obvious to directly compare V_{CP} with V_{REF} without voltage division. In either case, claim 2 would have been obvious to a POSITA in my opinion.

6. Claim 3: The charge pump circuit of claim 2, wherein the load selector means further includes a maximum ripple on the

target output selector means for adding a load, whenever a maximum ripple on the target output voltage (V_{cfrb}) greater than the reference voltage (V_{ref}) then the maximum ripple on the target output selector means adds additional loads until the V_{cfrb} voltage is less than or equal to the reference voltage (V_{ref}).

93. Doluca discloses bleeder control circuit 27 activates charge bleeder circuit 45 when the pump output exceeds an upper limit. EX-1006, 2:27-33, FIG. 2. As I have explained in ¶¶ 60-62, activating charge bleeder circuit 45 would increase the bleeding current from capacitor-plate line 19 to ground, thereby reducing the charge pump output voltage. With the combining of Doluca and Buti as shown in ¶ 87 and the modifications as described in ¶¶ 89 and 90, charge bleeder circuit 45 is implemented as FET loads 42, 48, 54, and 60, which are selectively activated (i.e., “added”) to provide bleeding paths. See ¶¶ 77-82. Following a modification pursuant to either ¶ 89 or ¶ 90, each FET load is activated to allow current to bleed whenever V_{CP} exceeds a threshold voltage corresponding to that FET. See ¶¶ 89-90. The bleeding does not stop until V_{CP} drops below that threshold voltage, causing the deactivation of that FET. This function of activating and deactivating FET loads, which I believe would have been readily understood by a POSITA, reads on “for adding a load, whenever a maximum ripple on the target output voltage (V_{cfrb}) greater than the reference voltage (V_{ref}) then the maximum ripple on the target output selector means adds additional loads until the V_{cfrb} voltage is less than or equal to the reference voltage (V_{ref}).” Correspondingly, I believe that a POSITA would have understood

that diode stacks 46, 52, 58, and 64, and inverters 44, 50, 56, and 62, which perform the function of activating and deactivating the FET loads, read on “maximum ripple on the target output selector means.”

7. Claim 24: A method for generating an output voltage with minimal ripples in a charge pump circuit, comprising: a) selecting a output pump voltage (V_{pump}); b) turning on a load associated with the selected V_{pump} ; and c) comparing a target output voltage (V_{cfra}) with a reference voltage (V_{ref}) whenever the target output voltage greater than the reference voltage, disabling the charge pump circuit; whenever the target output voltage is less or equal to the voltage reference, leaving the charge pump circuit on.

94. I believe that a POSITA would have found it obvious that the combination of Doluca and Buti teaches the method of claim 24. For example, in my analysis of claims 1 and 2, I discussed that the circuit formed by the combination of Doluca and Buti would have rendered obvious features such as “generating an output voltage with minimal ripples in a charge pump circuit” (see ¶¶ 80-81), “selecting a output pump voltage (V_{pump})” (see ¶¶ 82-84), “turning on a load associated with the selected V_{pump} ” (see ¶¶ 85-91), and “comparing a target output voltage (V_{cfra}) with a reference voltage (V_{ref}) whenever the target output voltage greater than the reference voltage, disabling the charge pump circuit” (see ¶ 92).

95. With respect to the remaining feature “whenever the target output voltage is less or equal to the voltage reference, leaving the charge pump circuit on,” this feature would have been obvious to a POSITA for reasons similar to those

discussed in ¶ 92. As I have discussed, Doluca teaches disabling the charge pump when the output voltage of the charge pump is higher than the reference voltage. EX-1006, 3:55-4:52, 6:64-7:23, FIGS. 2 and 6. Doluca also teaches turning on the charge pump (which reads on “leaving the charge pump circuit on”) when the output voltage of the charge pump is higher than the reference voltage. These teachings would have rendered the remaining feature of claim 24 obvious to a POSITA.

8. Claim [25a]: The method of claim 24, further comprises the following steps: a) comparing a maximum acceptable ripple on output voltage value (V_{cfrb}) with a reference voltage (V_{ref}) whenever the maximum acceptable ripple output voltage value is greater than the reference voltage, connecting a load until the V_{cfrb} voltage value is less than or equal to the reference voltage; b) comparing a minimum acceptable drop on output voltage value (V_{cfrc}) with the reference voltage (V_{ref})

96. As I have explained in my analysis of claim 3, the modified circuit of the Buti-Dolucas combination would have rendered obvious all features of [25a].

See ¶ 93.

9. Claim [25b]: whenever the minimum acceptable drop on output voltage value is less than the reference voltage, removing a load until the V_{cfrc} voltage value is greater than the reference voltage.

97. Following the analysis in ¶ 93, because the Dolucas-Buti combination would have made it obvious to add a load to decrease the pump output, the Dolucas-Buti combination also would have made it obvious to remove a load (opposite to adding a load) to increase the pump output (opposite to decreasing the pump output). Accordingly, when the pump output is lower than a desired level, a

POSITA would have had the motivation to remove loads until the pump output reaches the desired level.

VIII. Ground 1B: Claims 4-5, 11-15, 21-23 are obvious based on Doluca, Buti, and Hosono

A. Overview of Hosono

98. I have fully reviewed Hosono. In my understanding, Hosono's disclosure includes the following aspects.

99. Hosono discloses a charge pump circuit 70 that generates a desired output voltage V_{xx} for use in memory devices. EX-1007, 1:6-14, 5:5-8:65, FIG. 2 (reproduced below). The charge pump circuit 70 is connected to a load comprising resistor R_L , second voltage setting circuit 12, and first voltage setting circuit 11. *Id.* Hosono discloses that the charge pump output voltage can be regulated at a desired level. *Id.*, 14:51-15:5.

part of the well-known pumping operations of a typical charge pumps. A POSITIA would have known that the numbers of diode-connected NMOS transistors 81 and capacitors 82 can be different than those shown in FIG. 5B.

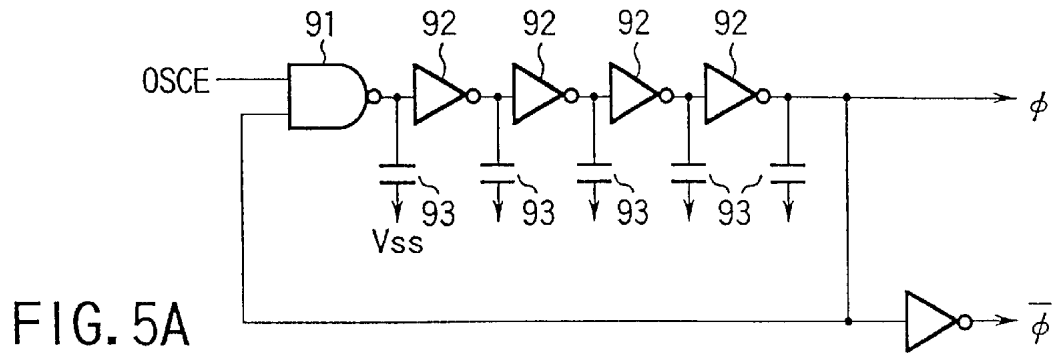


FIG. 5A

EX-1007, FIG. 5A

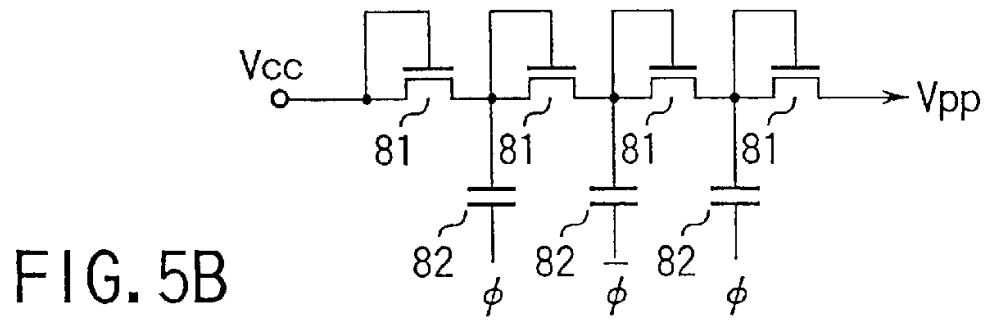


FIG. 5B

EX-1007, FIG. 5B

101. Hosono details a memory device in which the charge pump circuit can be used. EX-1007, 13:12-14:3, FIG. 4 (reproduced below). As illustrated below and readily understood by a POSITA, the memory device includes: a memory cell array 61; a substrate potential control circuit 67; an address bus comprising address buffer 64 and connections to row/column decoders; a data bus comprising a data

input/output buffer 66 and bit line control circuit 62; an address decoder comprising column decoder 63 and row decoder 65 coupled to the address bus; a read/write circuit comprising bit line control circuit 62 that is coupled to the data bus; and memory cell array 61 that is coupled to the address decoder, control circuit and read/write circuit. The memory device further includes voltage generating circuits 681-683, which each use a charge pump circuit for obtaining a high voltage to support the memory read/write operations. EX-1007, 14:4-50, FIGS. 4-6.

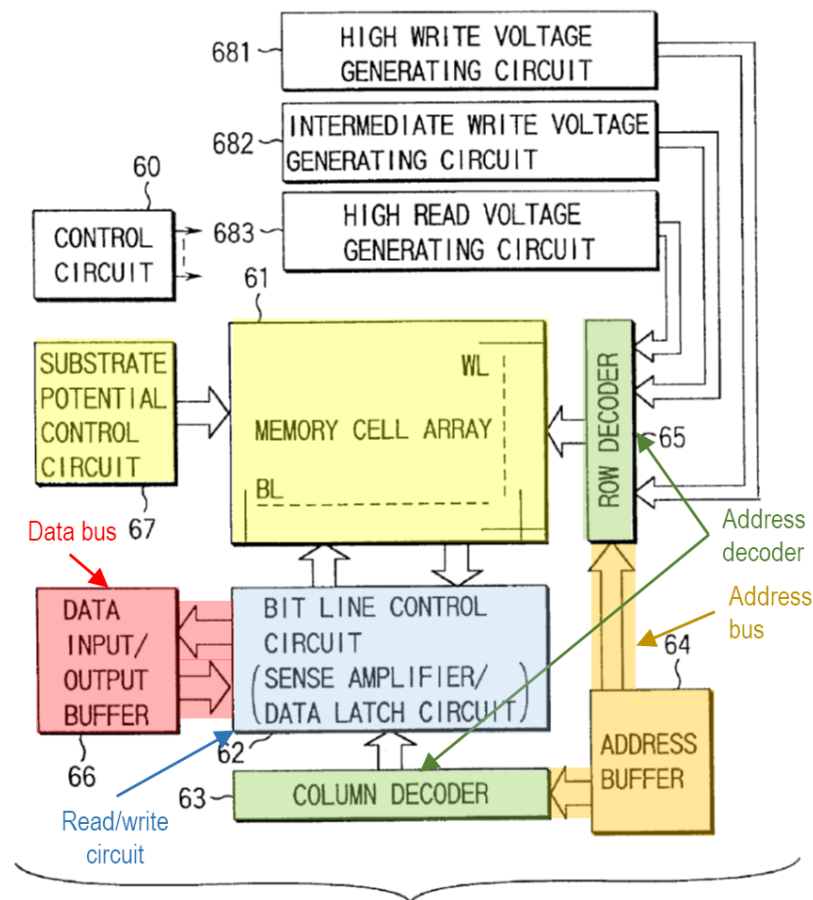


FIG. 4

B. Combination of Doluca, Buti, and Hosono

102. Hosono's disclosures about using a charge pump output circuit to supply voltage to memory devices, and to regulate the supplied voltage, are similar to the teachings of Doluca and Buti. EX-1007, 1:6-41, 2:65-3:31, 5:5-64, 14:51-15:5; *see* ¶¶ 60, 64, 69, 99. I believe that a POSITA would have been motivated to look to Hosono for teachings that would supplement or improve upon Doluca and Buti.

103. For example, Doluca discloses that its charge pump circuit 37 includes a pump clock generator 47, but does not describe the structure of the clock generator 47. EX-1006, 5:19-54, FIG. 3. A POSITA seeking to learn more about the clock generator circuit would have been motivated to look at other references for details about this circuit. In doing so, a POSITA would have noted that Hosono describes a charge pump circuit that is similar to Doluca's, and would have found that Hosono provides a detailed structure of a ring oscillator circuit for generating clock signals used in the charge pump circuit. EX-1007, 14:13-35, FIGS. 5A-5B; *see* ¶ 100. In my opinion, the POSITA would have considered implementing Doluca's clock generator 47 based on Hosono's ring oscillator circuit, and would have had a reasonable expectation of success in making the combination. The techniques for such implementation were known and the resulting circuit would

have been nothing more than a typical charge pump circuit driven by a typical clock generator circuit, the operations of both of which were well known before the Critical Date.

C. Analysis

1. Claim [4a]: The charge pump circuit of claim 1, wherein the pumping circuit comprises: a) a plurality of diodes coupled in series, each diode having an input terminal and an output terminal, the input terminal of the first diode in the series is coupled to the supply voltage, the output of the first diode being connected to the input terminal of the second diode, and the output terminal of the last diode connected to the output pump

104. Doluca teaches that its capacitor-plate bias circuit (charge pump circuit) includes pumping circuit 37, which includes several stages formed using capacitors and transistors. See ¶ 82. Doluca shows that its pumping circuit 37 includes diode-connected transistors 53, 55, and 57. EX-1006, FIG. 3. The practice of forming a diode by shorting the gate and source (or drain) of a transistor (i.e., a diode-connected transistor) have been well-known for a long time. In FIG. 3 of Doluca, each of diode-connected transistors 53, 55, and 57 can be regarded as a diode with an anode (i.e., input terminal) and a cathode (i.e., output terminal), and the three diodes are connected in series: The anode of diode 57 is coupled to the supply voltage V_{CC} ; the cathode of diode 57 is coupled to the anode of diode 55; the cathode of diode 55 is coupled to the anode of diode 53; and the cathode of diode 53 is coupled to the charge pump output V_{CP} . EX-1006, FIG. 3. I believe that, with such an arrangement, a POSITA would have interpreted transistors 57,

55, and 53 as the “first diode,” “second diode,” and “last diode,” respectively; V_{CC} as “the supply voltage;” and V_{CP} as the “output pump.”

2. Claim [4b]: b) a plurality of capacitors having a first terminal and a second terminal, wherein the first terminal of the first capacitor being coupled to the output of a first diode and the input of a second diode, the first terminal of the second capacitor being coupled to the output of the second diode and the input of a third diode, and the first terminal of the last capacitor is coupled to the input terminal of a last diode

105. FIG. 3 of Doluca shows capacitors C2 and C1, where each of capacitors C2 and C1 has an anode (the claimed “first terminal”) 51’ and 51, respectively, and a cathode 49’ and 49 (the claimed “second terminal”), respectively. EX-1006, FIG. 3. A POSITA would have interpreted capacitors C2 and C1 as the claimed “first capacitor” and “second capacitor,” respectively. Consistent with ¶ 104, the first terminal of capacitor C2 (i.e., anode 51’) is coupled to the output of diode 57 and to the input of diode 55, and the first terminal of capacitor C1 (i.e., anode 51) is coupled to the output of diode 55 and to the input of diode 53. In Doluca’s FIG. 3 and consistent with FIGS. 1 and 3 of the ’241 Patent, the second capacitor C1 is the last capacitor. EX-1001, FIGS. 1 and 3. As shown in FIG. 3 of Doluca, the first terminal of capacitor C1 (i.e., anode 51) is also coupled to the input of diode 53. EX-1006, FIG. 3. Accordingly, the arrangement of capacitors C1, C2, and diodes 57, 55, and 53 fully satisfies the feature of [4b].

106. In my opinion, a POSITA would have readily understood that the charge pump structure shown in Doluca’s FIG. 3 can be expanded to have more

stages, with each additional stage having an additional capacitor and an additional corresponding diode coupled in a manner similar to that illustrated in FIG. 3. A POSITA would certainly have had knowledge of charge pump fundamentals and known that the number of stages needed is determined by the desired output voltage compared to the input voltage. A POSITA would also have known that the individual stages are near duplicates of each other simply placed in series to achieve the desired output voltage. With the expansion of charge pump stages, e.g., with three or more stages, the second capacitor C1 will no longer be the last capacitor and the third diode 53 will no longer be the last diode. The capacitor and the diode in the third (or last stage) will be the last capacitor and the last diode, respectively. However, regardless of whether Doluca's charge pump structure is expanded, a POSITA would still have found the feature of [4b] obvious because the connection of each capacitor and the corresponding diode in each stage remains unchanged.

3. Claim [4c]: c) a plurality of inverters coupled in series to one another, each having an input terminal and an output terminal, the output of the first inverter being coupled to the second terminal of the first capacitor forming the first stage of the charge pump circuit, the second output of the second inverter coupled to the second terminal of the second capacitor forming the second stage of the charge pump circuit, and the output of the last inverter is coupled to the second terminal of the last capacitor forming the last stage of the charge pump circuit

107. In the charge pump circuit shown in Doluca's FIG. 3, cathodes 49' and 49 (i.e., second terminals of the first capacitor C2 and the second capacitor C1,

respectively, see ¶ 105), are coupled to signals V_p and $\overline{V_p}$, which are a “biphase pair” of signals output by pump clock generator 47. EX-1006, FIG. 3, 5:19-29. As I have explained previously, Doluca’s lack of detail about the internal circuitry of pump clock generator 47 would have motivated a POSITA to look at other sources for supplemental information about the clock generator circuit, e.g., Hosono, and would have found that FIGs. 5A and 5B of Hosono provide such information.

108. In FIG. 5A, Hosono shows a plurality of inverters 92 that output a clock signal ϕ , and shows an unlabeled inverter that outputs a complimentary signal $\bar{\phi}$. EX-1007, FIG. 5A, 14:13-23; see ¶ 100. Hosono’s teachings would have provided an obvious example for a POSITA to implement pump clock generator 47 of Doluca. The implementation would have involved using Hosono’s inverters ϕ and $\bar{\phi}$ to drive Doluca’s signals V_p and $\overline{V_p}$, as illustrated below.

Although the below figure only shows two inverters, it would have been obvious to include more inverters in series to output the pair of biphase signals V_p and $\overline{V_p}$.

As annotated in the below figure and would have been understood by a POSITA, the arrangement of the inverters and the capacitors Doluca’s charge pump, modified in view of Hosono’s clock generator, meets the features of [4c].

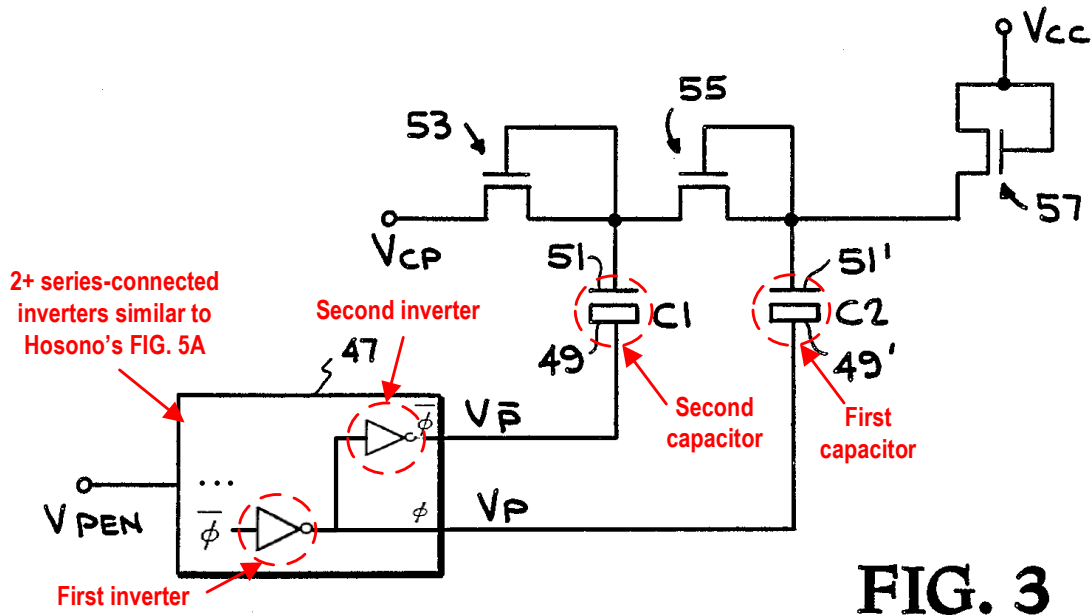


FIG. 3

EX-1006, FIG. 3 (modified and annotated based on EX-1008, FIG. 5A)

109. The above-illustrated FIG. 3 of Doluca as modified by Hosono can be further embodied as charge pump 37 in the Doluca-Buti combination, as described in ¶¶ 80-83. The techniques for doing so would have been obvious to a POSITA.

4. Claim [4d]: d) a clock signal coupled to the input terminal of the first inverter

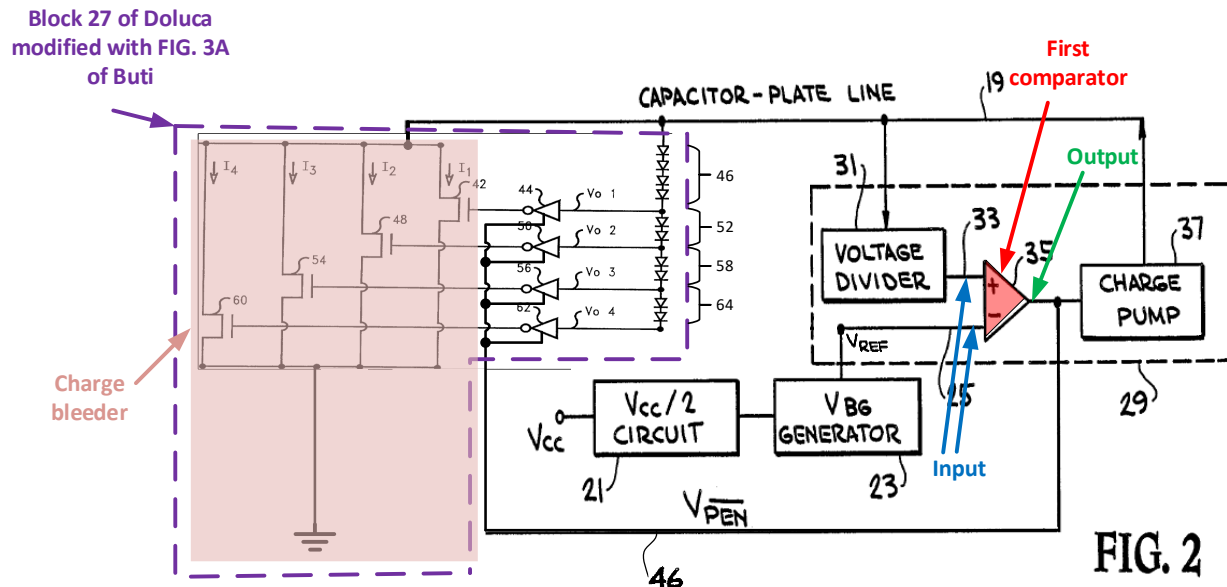
110. As illustrated in the annotated figure in ¶ 98, the input terminal of the first inverter receives $\bar{\phi}$, which Hosono discloses as a clock signal. EX-1007, FIG. 5A, 14:13-23. As a general matter, for a ring oscillator similar to that shown in Hosono's FIG. 5A, a POSITA would have understood that the input of each inverter is a clock signal with a phase of either signal ϕ or $\bar{\phi}$.

5. Claim 5: The variable charge pump circuit of claim 4, wherein each of the plurality of diodes is a diode-connected NMOS transistor, the gate of each transistor being connected to its drain forming the input terminal and its source forming the second terminal.

111. FIG. 3 of Doluca, with or without the modification based on Hosono, shows what is described in claim 5, as would have been readily understood by a POSITA. Each of transistors 57, 55, and 53 is a diode-connected NMOS transistor with the gate terminal connected to the drain terminal, together effectively forming the anode (i.e., input terminal) of a diode. The source of that NMOS transistor effectively forms the cathode (which reads on the “second terminal”) of the same diode.

6. Claim [11a]: The charge pump circuit of claim 2 wherein the target output pump selector comprises: a) a first comparator having two input terminals, an output terminal and a first enable terminal, one of the two input terminals being connected to the reference voltage (V_{ref})

112. As I have explained above, voltage divider 31 and comparator 35 in the circuit of the Doluca-Buti combination perform the function of the claimed “target output pump selector.” See ¶¶ 87, 92. As illustrated below, comparator 35 has two input terminals, one of which is connected to the reference voltage V_{REF} . See ¶ 92. Comparator 35 further has an output terminal, which provides a signal to turn charge pump 37 on or off. See ¶ 92.



EX-1005, FIG. 2 (modified, annotated)

113. With respect to the claimed “first enable terminal,” it has been well-known in circuit design that a comparator can have an enable terminal that enables or disables the functioning of the comparator.

114. In the instant case, the ’241 Patent does not appear to show a comparator having an enable terminal separate from the two input terminals and the output terminal. In all instances, the ’241 Patent consistently shows that a comparator has only three terminals: two inputs and one output. In FIG. 6, comparator 602 is shown to have its output labeled “ENAPUMP,” which appears to me to be the only relevant disclosure about the “first enable terminal” of a comparator. EX-1001, 5:45-53, FIG. 6. Assuming ENAPUMP is what the claimed “first enable terminal” refers to, a POSITA would have understood that

“the first enable terminal” and “the output terminal” refer to the same terminal, which is shown in Doluca’s illustration of comparator 35 having an output terminal that is coupled to the charge pump 37.

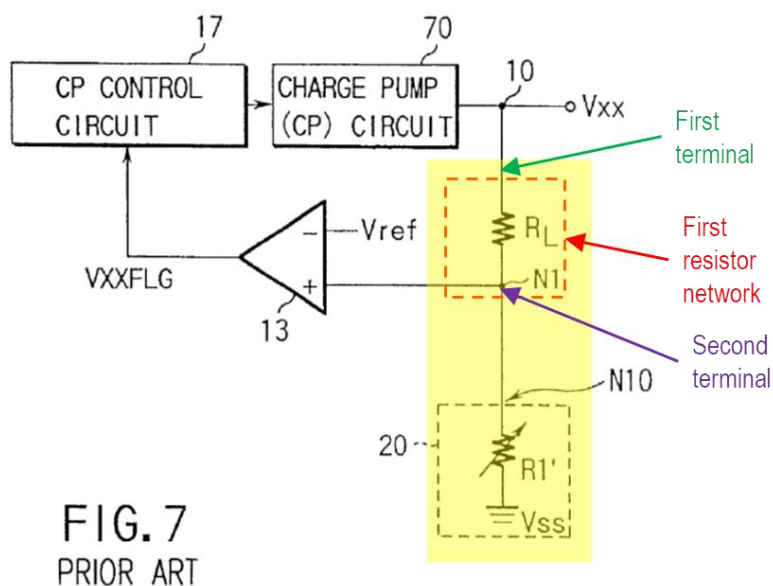
7. Claim [11b]: b) a first resistor network having two terminals, the first terminal being coupled to the output pump, the second terminal being coupled to one of the input terminals of the first comparator

115. Doluca teaches that voltage divider 31, which is part of the “target output pump selector,” has two terminals: one connected to the output of charge pump 37 via capacitor-plate line 19, and the other connected to input terminal “+” of comparator 35. EX-1006, FIG. 2, 4:31-41; see ¶ 60.

116. Doluca describes an implementation of voltage divider 31 that comprises a series of transistors. EX-1006, 6:21-44, 6:21-44, 6:64-7:14, FIGS. 5-6. As a POSITA would have known, there are alternative ways of implementing a voltage divider, such as using one or more resistor networks.

117. For example, Hosono describes a voltage generating circuit with respect to FIG. 7, having series-connected resistors R_L and $R1'$ “for setting the value of output node 10.” EX-1007, 1:38-61, FIG. 7 (reproduced below). A POSITA would have readily understood that R_L and $R1'$ together form a “potential dividing scheme,” i.e., a voltage divider circuit, with R_L and $R1'$ being the first and second resistor networks, respectively. *Id.*, 1:62-2:8, 6:35-39, FIG. 8. A first terminal of R_L is connected to output of charge pump 70 at node 10, and a second

terminal at node N1 connected to input “+” terminal of comparator 13. *Id.*, 1:38-61, FIG. 7 (reproduced below).



EX-1007, FIG. 7 (annotated)

118. I believe that a POSITA would have found it obvious that Doluca’s voltage divider 31 can be implemented using Hosono’s voltage divider circuit formed by R_L and $R1'$. The implementation does not change the input/output connections of the voltage divider circuit nor does the implementation materially effect the overall circuit operation of Doluca’s bias circuit.

8. Claim [11c]: c) a second resistor network having two terminals, the first terminal being coupled to the second terminal of the first resistor network, and the second terminal of the second resistor network being coupled to an electrical ground

119. Consistent with ¶¶ 107-108, the voltage divider circuit in FIG. 7 of Hosono includes equivalent resistor $R1'$ as the “second resistor network.” Hosono’s FIG. 7 shows that one terminal of $R1'$ is connected to the second

terminal of first resistor network R_L at node N1, and the second terminal of $R1'$ is connected to ground V_{SS} . EX-1007, FIG. 7 (reproduced below).

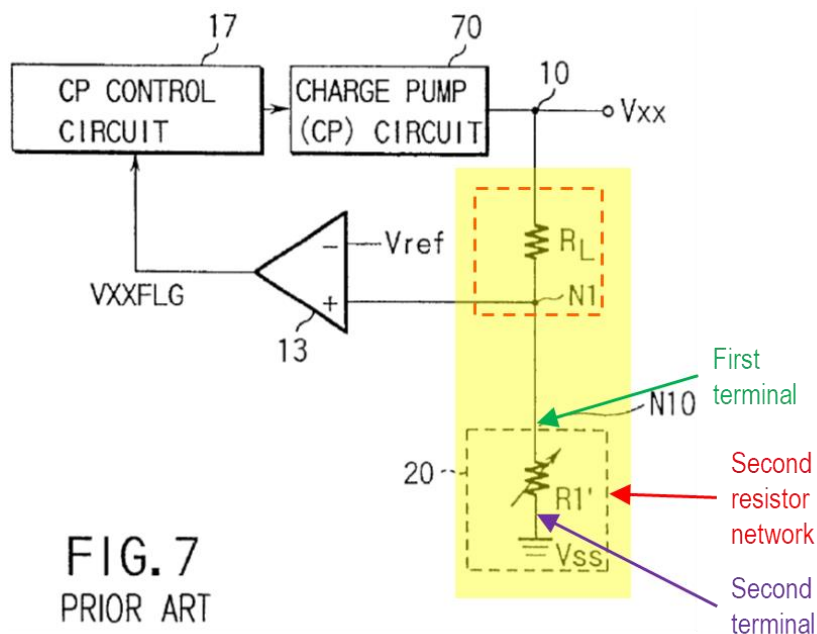


FIG. 7
PRIOR ART

EX-1007, FIG. 7 (annotated)

9. Claim [11d]: d) a reference voltage source (V_{ref}) coupled to one of the input terminals of the first comparator

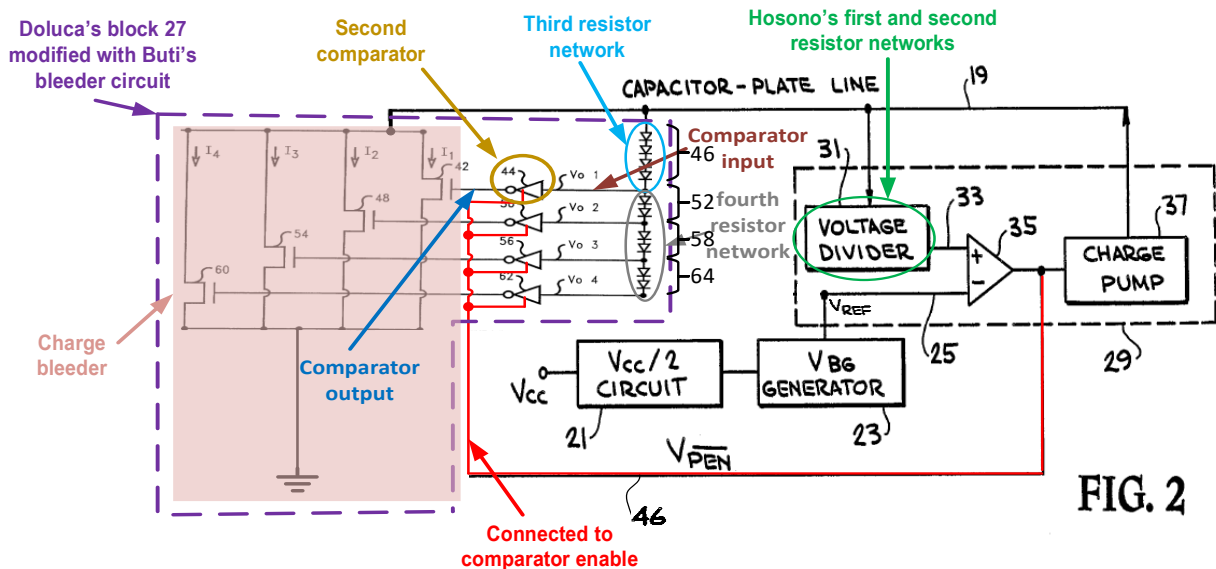
120. As a POSITA would have understood, Doluca's V_{BG} generator 23 is the source of reference voltage V_{REF} , where V_{BG} generator 23 is coupled to the "-" input terminal of comparator 35. EX-1006, FIG. 3; See ¶ 92.

10. Claim [12a]: The charge pump circuit of claim 11, wherein the maximum overshoot on target output selector means comprises: a) a third resistor network having two terminals, the first terminal is coupled to the output pump

121. As I have discussed previously, the Doluca-Buti combination teaches diode stacks 46, 52, 58, and 64, which a POSITA would have regarded as resistor networks. See ¶¶ 72, 74. As illustrated below, the upper four diodes

(corresponding to diode stack 46 in Buti's charge bleeder 102B) form a resistor network with one terminal coupled to the output of charge pump 37 via capacitor-plate line 19, while the lower six diodes (corresponding to diode stacks 52, 58, and 64 in Buti's charge bleeder 102B) form another resistor network. EX-1006, FIG.

2. A POSITA would have understood that the resistor network formed by the upper four diodes reads on the “third network.”



EX-1006, FIG. 2 (modified, annotated)

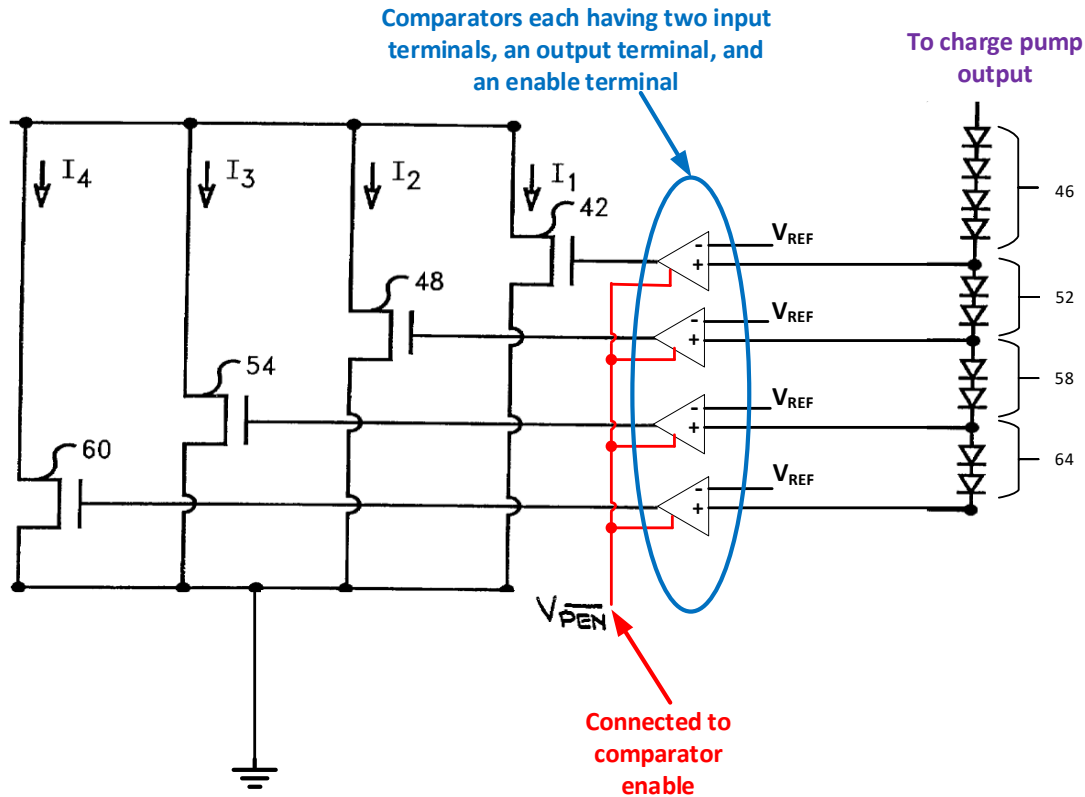
11. Claim [12b]: b) a fourth resistor network having two terminals, the first terminal is coupled to second terminal of the third resistor network, and the second terminal of the fourth resistor network being coupled to an electrical ground

122. Consistent with ¶ 121, the resistor network formed by the lower six diodes (corresponding to diode stacks 52, 58, and 64 in Buti's charge bleeder 102B) has an upper terminal coupled to the third network (formed by the upper four diodes, and has a lower terminal coupled to the electrical ground via inverter

62 and FET 60. *Id.* A POSITA would have understood that the resistor network formed by the lower six diodes reads on the “fourth network.”

12. Claim [12c]: c) a second comparator having two input terminal, an output terminal, and an enable terminal, one of the input terminals being coupled to the input terminal of the fourth resistor network and the other of the input terminals being coupled to the reference voltage V_{ref}

123. I have explained that inverters and buffers can be considered a comparator with a fixed internal reference. See ¶¶ 75-76. I have also explained that it would have been obvious to use op-amp-based, two-input comparators in lieu of inverters (or buffers) 44, 50, 56, and 62 in the circuit of the Doluca-Buti combination illustrated in ¶ 121. See ¶ 77. Each of the op-amp-based comparators in the resultant circuit, partially reproduced below, reads on [12c]. Further, since the replacement of inverter/buffer-based comparators with op-amp-based comparators does not change the rest of the circuit of the Doluca-Buti combination, the resultant circuit reads on [12a]-[12b].



EX-1006, FIG. 2 (in-part, modified in view of EX-1005, FIG. 3, annotated)

13. Claim [12d]: d) a logic circuit having two terminals, the first terminal is coupled to the output terminal of the second comparator

124. In the circuit of ¶ 123, the output terminal of each comparator is coupled to the gate terminal of a corresponding FET. A POSITA would have understood that each FET, which has a gate terminal, a drain terminal, and a source terminal, is a logic circuit.

14. Claim [12e]: e) a set load coupled to the pump output and being controlled by the logic circuit for adding an additional load to the output pump when the output pump has an overshoot greater than a maximum allowed on the output terminal

125. See As I have discussed above, each of FETs 42, 48, 54, and 60 is a logic circuit, which, when selectively activated, functions as a load to provide a

bleeding path from the charge pump output to the ground. See ¶¶ 71-77, 85-91, and 123-124. Specifically, when the pump output voltage on capacitor-plate line 19 becomes excessive (i.e., “having an overshoot greater than a maximum allowed on the output terminal”), one or more of the diode stacks will be forward-biased and, together with the corresponding comparators, control the corresponding FET(s) to turn on one or more bleeding paths. A POSITA would have understood that these operations read on the features of [12e].

15. Claim [13a]:

A memory device, comprising: an address bus; a control circuit; a data bus; an address decoder coupled to the address bus; a read/write circuit coupled to the data bus; a memory cell array coupled to the address decoder, control circuit, and read/write circuit; and

a charge pump circuit that generates a boosted output voltage with minimum ripples on an output node coupled to the address decoder, read/write circuit, and memory cell array, the charge pump circuit comprising:

126. Doluca, Buti and Hosono all disclose charge pump circuits for use in memory devices. See, e.g., EX-1006, 1:5-38; EX-1005, 1:11-2:28; EX-1007, 1:6-14. Indeed, using charge pump circuits to supply boosted voltage to memory devices was well-known as of the Critical Date. See, e.g., EX-1017, at 826.

127. As I have explained in ¶ 101, Hosono’s memory device illustrated in FIG. 4 has the following components: address buffer 64 (the claimed “address bus”); substrate potential control circuit 67 (the claimed “control circuit”); data input/output buffer 66 (the claimed “data bus”); column decoder 63 and row

decoder 65 (the claimed “address decoder”), both coupled to address buffer 64; bit line control circuit 62 (the claimed “read/write circuit”) coupled to data input/output buffer 66; and memory cell array 61 (the claimed “memory cell array”), which is coupled to column decoder 63 and row decoder 65, substrate potential control circuit 67, and bit line control circuit 62. *See* ¶ 101.

128. As I have explained in ¶ 101, Hosono’s memory device illustrated in FIG. 4 further has voltage generating circuits 681-683, which each use a charge pump circuit for obtaining a high voltage to support the memory read/write operations. EX-1007, 14:4-50, FIGS. 4-6; *see* ¶ 101. Hosono discloses that the charge pump circuit generates voltage with minimum ripples by describing a feedback mechanism to stabilize the charge pump voltage at a desired level. EX-1007, 14:61-15:5. Doluca similarly discloses this limitation with regard to generating a charge pump voltage with minimum ripples. *See* ¶ 102.

129. A POSITA would have understood that Doluca’s bias circuit can be used as the charge pump circuit in Hosono’s high voltage generating circuits 681-683 for obtaining a high voltage. *See* ¶ 102. Similar to Hosono’s charge pump circuit, Doluca’s bias circuit provides a pump output voltage with minimum ripples by generating a stable voltage within a narrow range of a target (e.g., design) voltage. Accordingly, I believe that a POSITA would have found it obvious that the combination of Hosono with Doluca (as modified by Buti) reads on [13a].

16. Claim [13b]:

- a) a pumping circuit comprising one or more stages operable to receive a supply voltage and generate one or more pump voltages;**
- b) a plurality of loads, each load associated with a specific pump voltage and selectively coupleable to an output of the pump circuit (output pump);**
- c) a load selector means coupled to the output pump for selecting a load that satisfies a specific pump voltage;**
- d) a target output pump selector sampling the output of the pump circuit for shutting down the variable charge pump circuit whenever the sampled output voltage (V_{cfra}) is greater than or equal to a reference voltage (V_{ref});**
- e) a maximum ripple on target output selector means sampling the output of the pump circuit for adding a load, whenever a maximum ripple on sampled output voltage (V_{cfrb}) is greater or equal to than the reference voltage (V_{ref}) then the output selector means adds additional loads until the V_{cfrb} voltage is less than the reference voltage (V_{ref}).**

130. The features of [13b] are either disclosed or made obvious by the Doluca-Buti combination, as I have explained above. See ¶¶ 82-93.

131. I note that [13b] uses the term “sampling the output of the pump circuit” and “the sampled output voltage.” A POSITA would have understood that the operation of “sampling” in the context of charge pump circuits simply refers to obtaining an instantaneous value of a signal, e.g., an output voltage. In the context of [13b], I believe that the sampling operation refers to obtaining a voltage value of the charge pump output, which is needed to compare the charge pump output voltage with a reference voltage. Accordingly, a POSITA would have understood that the operations recited in [13b] are substantively similar to the features recited in claims 1-3, in spite of different words having been used.

17. Claim 14: A memory system of claim 13, wherein the pumping circuit comprises:

a) a plurality of diodes coupled in series, each diode having an input terminal and an output terminal, the input terminal of the first diode in the series being coupled to the supply voltage, the output of the first diode being connected to the input terminal of the second diode, and the output terminal of the last diode connected to the output pump voltage;

b) a plurality of capacitors having a first terminal and a second terminal, wherein the first terminal of the first capacitor being coupled to the output of the first diode, the first terminal of the second capacitor being coupled to the output of the second diode, and the first terminal of the last capacitor being coupled to the input terminal of the last diode;

c) a plurality of inverter coupled in series to one another, each having an input terminal and an output terminal, the output of the first inverter being coupled to the second terminal of the first capacitor and the input of the second inverter forming the first stage of the charge pump circuit, the second output of the second inverter coupled to the second terminal of the second capacitor forming the second stage of the charge pump circuit, and the output of the last inverter being coupled to the input of the last diode;

d) a clock signal coupled to the input terminal of the first inverter.

132. As I have explained with respect to claim 4, the Doluca-Buti-Hosono combination would have rendered obvious all features of claim 14. See ¶¶ 104-110. In particular, with respect to the feature “the output of the last inverter being coupled to the input of the last diode,” Doluca’s FIG. 3 as modified shows the output of the second inverter is coupled to the anode of diode 53 via capacitor C1. See ¶ 108.

18. Claim 15: The memory system of claim 13, wherein the plurality of diodes is a NMOS transistor connected as a diode, the gate of each transistor being connected to its drain forming the input terminal and the source forming the second terminal.

133. As I have explained with respect to claim 5, the Doluca-Buti-Hosono

combination would have rendered obvious all features of claim 15. See ¶ 111.

19. Claim 21: The memory system of claim 13, wherein load selector means comprises:

a) a first comparator having two input terminal, an output terminal and a first enable terminal, one of the two input terminals connected to the reference voltage (V_{ref});

b) a first resistor network having two terminals, the first terminal being coupled to the output pump, the second terminal being coupled to the output terminal of the first comparator;

c) a second resistor network having two terminals, the first terminal is coupled to the second terminal of the first resistor network, and the second terminal of the second resistor network being coupled to an electrical ground;

d) a third resistor network having two terminals, the first terminal being coupled to the output pump;

e) a fourth resistor network having two terminals, the first terminal being coupled to the second terminal of the third resistor network, the second terminal of the fourth resistor network being coupled to ground;

f) a second comparator having two input terminals, and output terminal and an enable terminal, one of the input terminals being coupled to the input terminal of the fourth resistor network and the other of the input terminals being coupled to the reference voltage V_{ref} ; and

g) a logic circuit having two terminals, the first terminal coupled to the second comparator.

134. As I have explained with respect to claims 1-3, the Doluca-Buti-

Hosono combination would have rendered obvious all features of claim 21. See ¶¶

80-93.

20. Claim 22: The memory system of claim 21, wherein the pumping circuit comprises:

a) a plurality of capacitors or current sinkers having a first terminal and a second terminal, wherein the first terminal of the first capacitor being coupled to the output of the first diode, the first terminal of the second capacitor being coupled to the output of the second diode, and the first terminal of the last capacitor being coupled to the input terminal of the last diode;

b) a plurality of inverter coupled in series to one another, each having an input terminal and an output terminal, the output of the first inverter being coupled to the second terminal of the first capacitor and the input of the second inverter forming the first stage of the charge pump circuit, the second output of the second inverter coupled to the second terminal of the second capacitor forming the second stage of the charge pump circuit, and the output of the last inverter being coupled to the input of the last diode; and

c) a clock signal coupled to the input terminal of the first inverter.

135. As I have explained with respect to claim features [4b]-[4d], the Doluca-Buti-Hosono combination would have rendered obvious all features of claim 22. See ¶¶ 104-110. In particular, modified FIG. 3 of Doluca, see ¶ 108, shows the second inverter being coupled to diode 53 via intervening capacitor 51, which reads on “b) ... the output of the last inverter being coupled to the input of the last diode.”

21. Claim 23: The memory system of claim 13, wherein the memory cell is a flash memory cell.

136. Hosono discloses that the memory cell, such that shown in FIG. 4, may be a flash memory cell. EX-1007, 1:1-20, 3:1-31, 11:61-12:4.

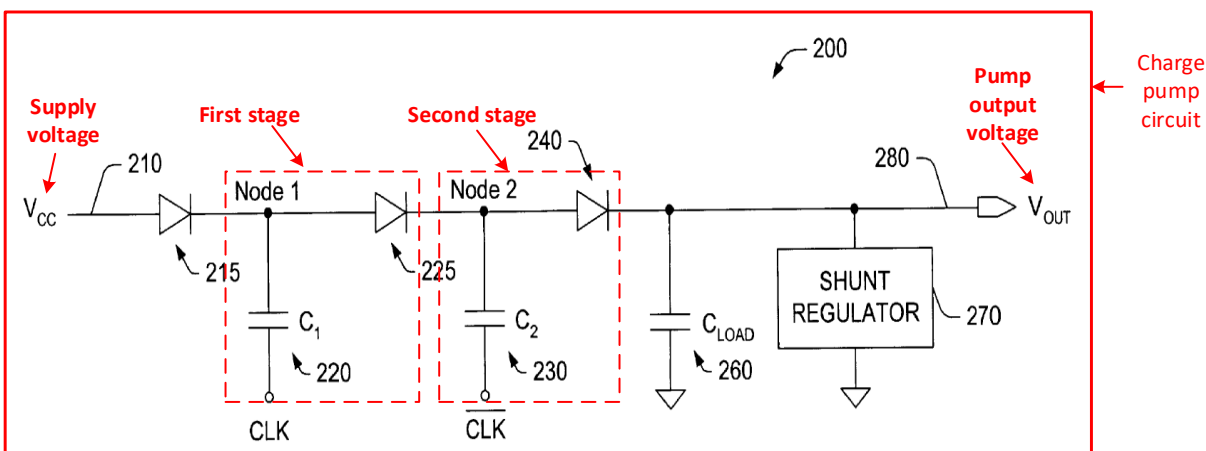
IX. GROUND 2A: Claims 1 and 6-10 are rendered obvious by Le and Ujiie

A. Overview of Le

137. I have fully reviewed Le. In my understanding, Le’s disclosure includes the following aspects.

138. Le describes a conventional multi-stage charge pump circuit, shown below, that generates an output voltage V_{out} using a supply voltage V_{CC} . EX-1008,

1:52-4:18, FIGS. 1-2. Le further discloses regulating V_{out} using shunt regulator 270. *Id.* Shunt regulators were well-known as of the Critical Date and are a type of charge bleeder. The shunt regulator works by loading the circuit to direct excess charge away from the output to ground to regulate the voltage to a desired lower level.

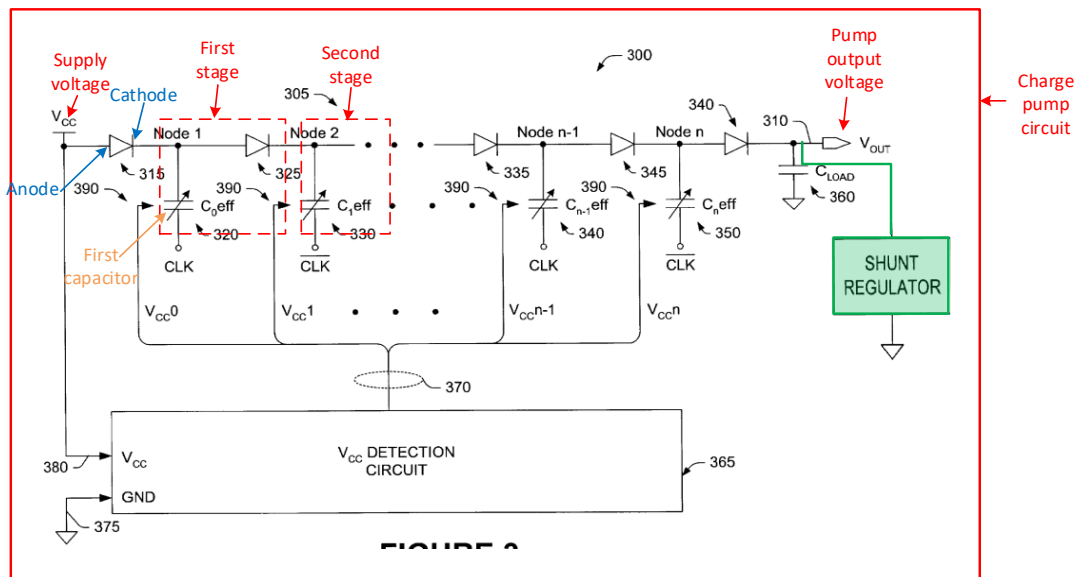


EX-1008, FIG. 2 (annotated)

139. Le modifies the conventional multi-stage charge pump circuit by using “variable bootstrap capacitance value which is varied as a function of the input supply voltage.” *Id.*, 4:30-5:32. The modified circuit which Le refers to as charge pump system 300, can use a shunt regulator to reduce ripple of the pump output voltage, which is provided for flash memory cell operations. *Id.*, 6:22-26, 7:4-25, 10:41-11:6, FIG. 3. Given that the only example of shunt regulator described in Le is shunt regulator 270, a POSITA would have found it obvious that, when Le describes using a shunt regulator in the circuit of FIG. 3, Le is

referring to using a shunt regulator that is similar to shunt regulator 270.

Accordingly, I believe that a POSITA would have understood that Le's modified circuit would look similar to the one reproduced below, with a shunt regulator coupled between V_{OUT} and the ground, serving as a load of the charge pump circuit.



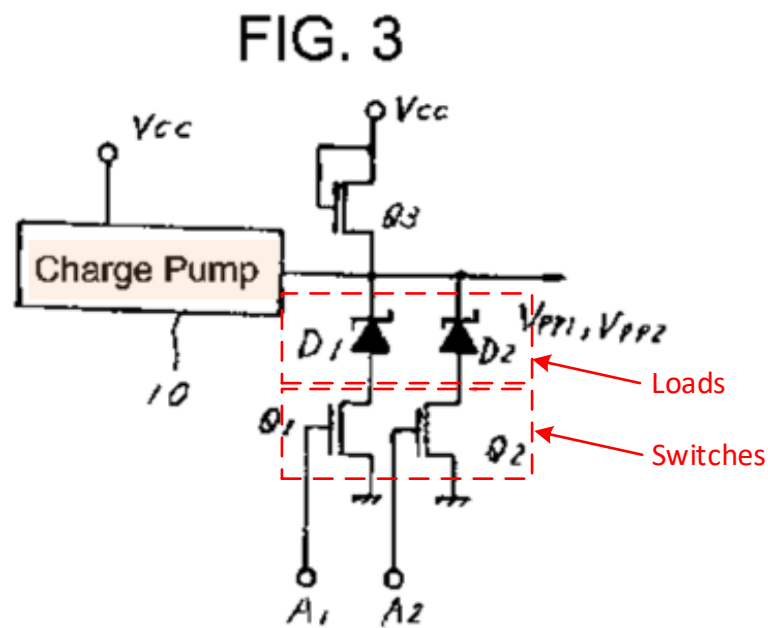
EX-1008, FIG. 3 (modified and annotated)

B. Overview of Ujiie

140. I have fully reviewed the English translation of Ujiie. In my understanding, Ujiie's disclosure includes the following aspects.

141. Ujiie describes a booster circuit that includes a charge pump to generate voltages used during write and erase operations of a memory device. EX-1009, ¶[01], ¶¶[18]-[21]. Ujiie discloses that fluctuations in the output voltage can be reduced by using a shunt circuit coupled to the charge pump output. *Id.*, ¶¶[20]-

[25], FIG. 3 (reproduced below). Ujiie's shunt circuit includes NMOS switches Q1 and Q2 that selectively couple diodes D1 and D2, respectively, as loads to the charge pump. *Id.* Despite the different phrasing by Ujiie's, I believe that a POSITA would have understood that Ujiie's disclosure of reducing voltage fluctuation is similar to reducing voltage ripple, and that Ujiie's shunt circuit is a used as a shunt regulator.



EX-1009, FIG. 3 (annotated)

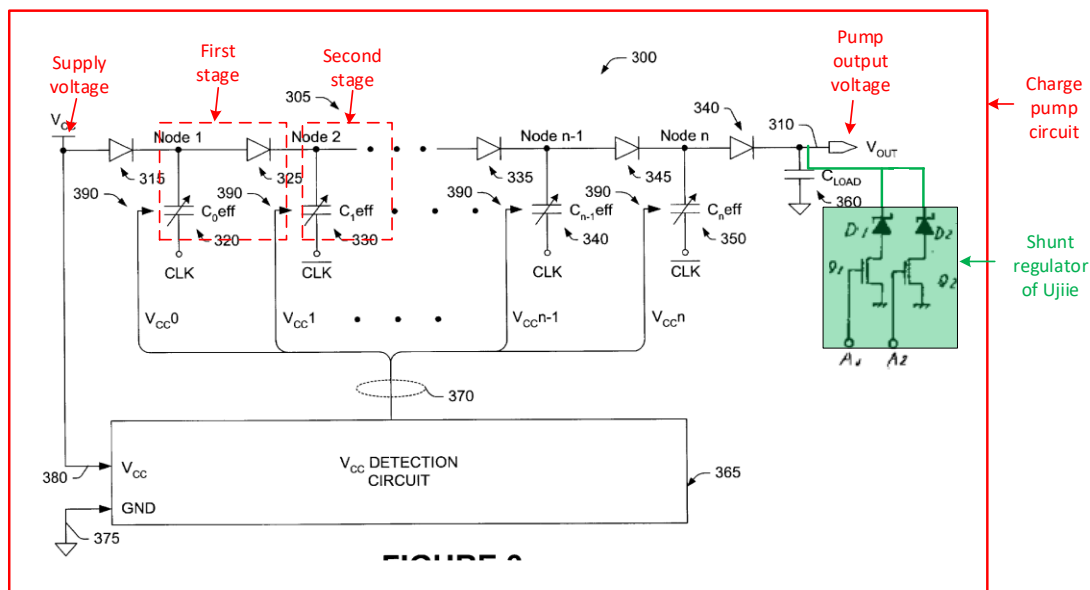
C. Combination of Le with Ujiie

142. In my opinion, a POSITA would have found it obvious to combine Le and Ujiie, for at least the following reasons. Le discloses a charge pump circuit to supply voltages to memory devices and describes using shunt regulator 270 to regulate the output voltage of the charge pump circuit. See ¶¶ 138-139. Le

however does not provide further structural or functional description of the shunt regulator. A POSITA who read the description of Le's charge pump circuit and wanted to know more about how a shunt regulator can be used to regulate the output voltage, would have looked at other sources of information about shunt regulators. In seeking such information, a POSITA would have been motivated to consider references that describe shunt regulators in the context of charge pump circuits used for memory devices.

143. I believe that a POSITA considering additional references to know about shunt regulators would have found that Ujiie is one such reference, describing use of a booster (i.e., charge pump) circuit to supply voltages to memory devices. See ¶ 141. A POSITA would have noted that Ujiie discloses the use of shunt circuit to regulate the charge pump output voltage, which is similar to the disclosure of Le. EX-1009, ¶¶[20]-[25], FIG. 3; see ¶ 141. A POSITA accordingly would have understood that Ujiie's shunt circuit can be used as a shunt regulator in Le's charge pump circuit to regulate the pump output voltage, as a matter of design choice. See ¶ 141. A POSITA would have conceived a modification to Le's charge pump circuit based on Ujiie's shunt regulator circuit, similar to the circuit shown below. A POSITA would have had a reasonable expectation of success for this modification, as the techniques involved were known and the modification would not have affected the operation of Le's charge

pump circuit that is modified.



EX-1008, FIG. 3 (modified based on EX-1009, FIG. 3, annotated)

D. Analysis

1. Claim [1pre]: A charge pump circuit for generating a charge pump voltage having minimal voltage ripples, comprising:

144. Le’s charge pump system 300 has a charge pump circuit that generates a charge pump voltage V_{OUT} . See ¶ 138. Le notes using a shunt regulator, such as shunt regulator 270 to provide “further reduction in power consumption.” EX-1008, 10:61-11:6, 3:5-52, FIG. 2. Le also discloses that the shunt regulator “advantageously provides a smaller ripple voltage at its regulation output [than prior art charge pump circuits].” *Id.*, 6:15-25, 10:41-11:6. In view of Le’s above disclosure, I believe that a POSITA would have found it obvious to include a shunt regulator in Le’s charge pump system 300, in a manner similar to that I have discussed previously in ¶ 139. Le’s disclosure accordingly reads on the

feature of [1pre].

2. Claim [1a]: a) a pumping circuit comprising one or more stages operable to receive a supply voltage and generate a selected one of a plurality of pump voltages;

145. Le teaches charge pump circuit 305 as part of charge pump system 300 and having one or more stages “to receive the supply voltage 380 and generate the charge pump output voltage V_{OUT} 310.” *Id.*, 7:4-49, 2:18-3:24, 4:31-59, FIGs. 1-3.

146. According to Le, the generated charge pump output voltage V_{OUT} 310 can have multiple values. Specifically, Le teaches that the charge pump voltage generated by its disclosed embodiment can be applied to program/erase operations of memory cells, and notes that such operations in semiconductor memory devices use different voltage levels, which are generated by the charge pump circuits. EX-1008, 1:7-18, 1:51-2:34. I believe that a POSITA would have found it obvious that Le’s disclosed pump system 300 with pumping circuit 305 can be applied to generate different (i.e., “a plurality of”) pump voltages used in memory device operations.

3. Claim [1b]: a plurality of loads selectively coupleable to an output of the pumping circuit, each load associated with a specific pump voltage; and

147. While a POSITA would have found it obvious, based on Le’s disclosure, to couple a shunt regulator to the output of a charge pump, as discussed above with respect to the figure of ¶ 139, Le does not elaborate the internal

structure of the shunt regulator, so it would have been up to a POSITA's choice of implementation.

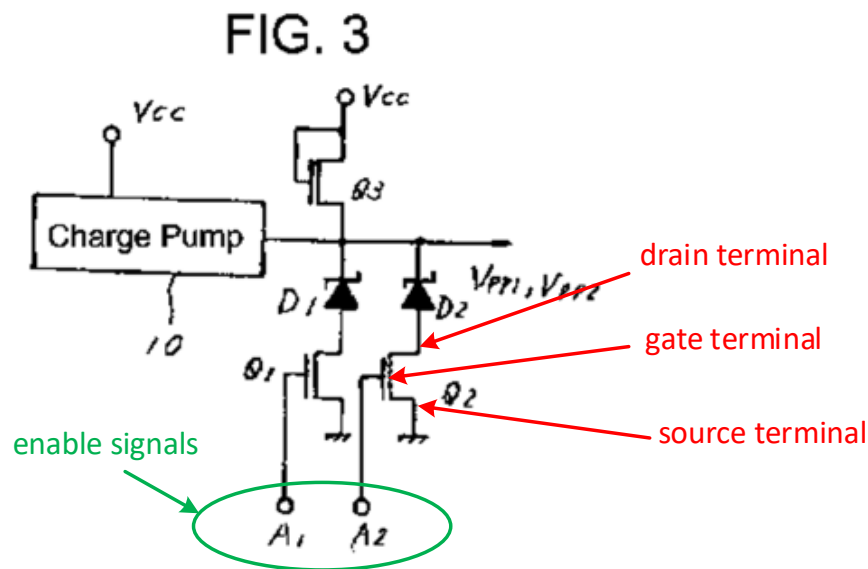
148. As I have discussed above, when looking for a shunt regulator implementation, a POSITA would have looked into Ujiie and used Ujiie's structure formed by diodes D1 and D2, and switches Q1 and Q2 as a shunt regulator in Le's circuit. See ¶ 143. Looking at the circuit shown in ¶ 143, a POSITA would have understood that diodes D1 and D2 form the loads of the combined charge pump circuit. The POSITA would also have understood that these diode loads are selectively coupleable to the charge pump output under the control of switches Q1 and Q2, which are further controlled by signals A1 and A2, respectively. EX-1009, ¶¶[18]-[25]. As a POSITA would have further understood, Ujiie teaches that diodes D1 and D2 are associated with write voltage V_{pp1} and erase voltage V_{pp2} , respectively, each of which is "a specific pump voltage." *Id.*

4. Claim [1c]: c) a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit.

149. Consistent with ¶ 139, given Ujiie's teaching about selectively coupling diodes D1 and D2 to the charge pump output, a POSITA would have understood that switches Q1 and Q2 and control signals A1 and A2 function to select loads to generate V_{pp1} and V_{pp2} . See ¶ 148. I believe that a POSITA accordingly would have understood that switches Q1 and Q2 and control signals A1 and A2 form the claimed "load selector means."

5. **Claim 6: The charge pump circuit of claim 1, wherein the load selector means is a plurality of switches, one switch for each of said loads, each switch having a first terminal, a second terminal, and an enable terminal, the switch being coupled in series with each load, the first terminal of the switch being coupled to the output pump and the second terminal of the switch is coupled to each load.**

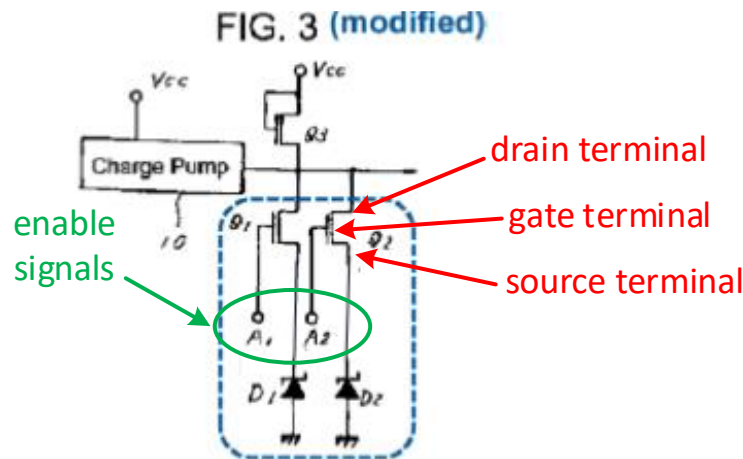
150. Ujiie's switches Q1 and Q2 are NMOS transistors, as clearly seen from the symbol used in Ujiie's FIG. 3. EX-1009, FIG. 3 (reproduced below). An NMOS transistor has a drain terminal, a gate terminal, and a source terminal, as well-known in the semiconductors industry for many decades.



151. The gate terminal of an NMOS transistor controls the activation or deactivation of the NMOS, as well-known in the semiconductors industry for many decades. Ujiie uses signals A1 and A2 to control the gate terminals of switches Q1 and Q2, respectively. *Id.*, FIG. 3. Accordingly, a POSITA would have considered signals A1 and A2 as “enable signals” and the gate terminal of each NMOS

transistor as the “enable terminal.” The POSITA would have also considered the drain and source terminals of each NMOS transistor as the respective “first” and “second” terminals.

152. In Ujiie’s original FIG. 3, each diode is connected in series with a corresponding NMOS transistor. *Id.*, FIG. 3. As a simple matter of design choice, a POSITA would have known that the positions of each diode and the corresponding NMOS transistor can be swapped, resulting in a modified version of Ujiie’s FIG. 3 as illustrated below. In the modified circuit, each of switches Q1 and Q2 has its drain (second) terminal coupled to the output of charge pump 10 and source (first) terminal coupled to its corresponding diode load. *Id.* A POSITA would have had a reasonable expectation of success for this modification, as the logic operation of the resulting circuit would have been similar. Moreover, a POSITA would have been motivated to make this modification depending upon their design choice of specific transistors, internal voltage levels and other design factors that a POSITA regularly considers in the specific design implementation.

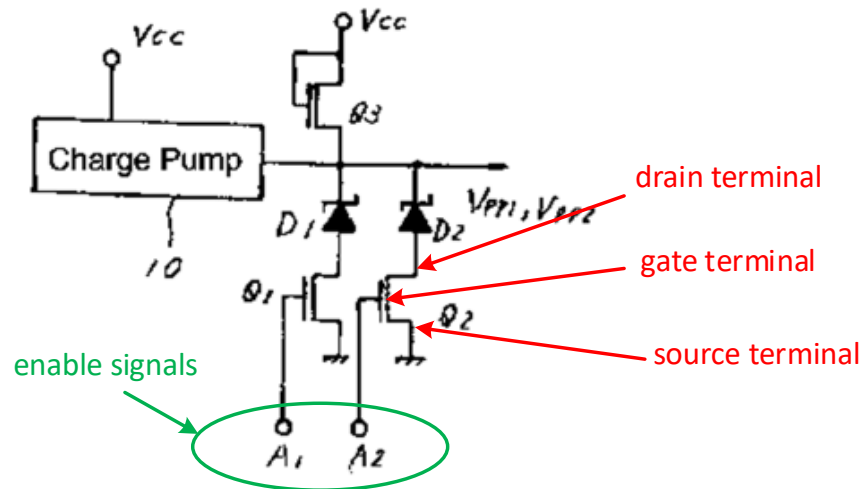


EX-1009, FIG. 3 (modified with annotation)

6. **Claim 7: The charge pump circuit of claim 1, wherein each load selector means comprises an NMOS transistor having a gate, a drain and a source, the gate of the NMOS load transistor being coupled to an enable signal, the source of the load NMOS load transistor being coupled to an electrical ground, and the drain being coupled to a load.**

153. The claim recites “NMOS transistor,” “NMOS load transistor,” and “load NMOS load transistor.” If they all refer to the same concept “NMOS transistor,” then the features of claim 7 are well covered by Ujiie’s original FIG. 3, as I have explained above. See ¶¶ 150-151. In particular, in Ujiie’s original FIG. 3 reproduced below, the gate of each NMOS transistor is coupled to a corresponding enable signal, the source to the ground, and the drain to a corresponding diode load. EX-1009, FIG. 3.

FIG. 3



EX-1009, FIG. 3 (annotated)

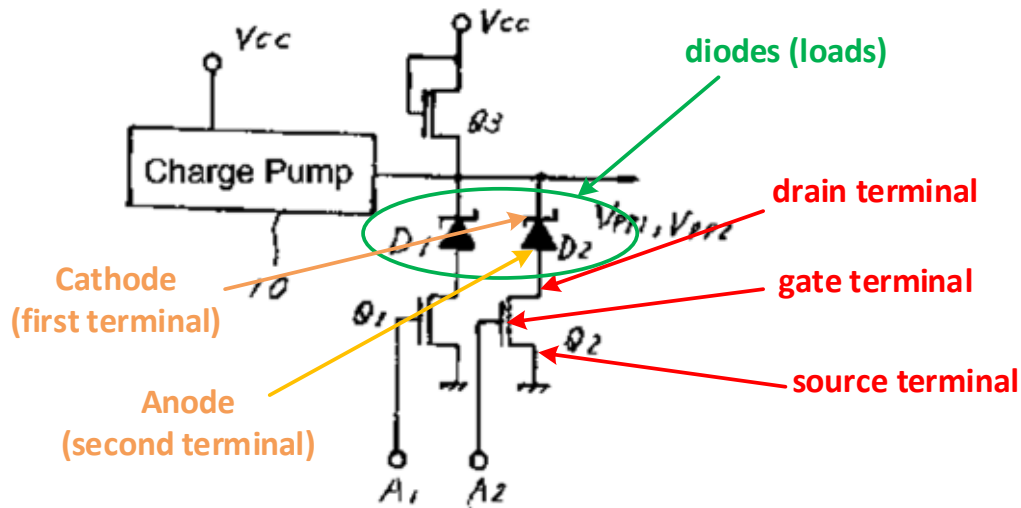
7. **Claim 8: The charge pump circuit of claim 7, wherein each load is a capacitor or a current sinker having a first terminal and a second terminal, the first terminal being coupled to the pump voltage and the second terminal being coupled to the drain of the NMOS transistor.**

154. Diodes were well-known as current sinkers as of the Critical Date.

Diodes were also well-known to have a cathode and an anode. When a diode is forward-biased, current flows through the diode from the anode to the cathode. In Ujiie's FIG. 3 as reproduced below, the cathode (first terminal) of each diode load is coupled to the output voltage of charge pump 10, and the anode (second terminal) of the same diode load is coupled to a corresponding NMOS transistor.

Id., FIG. 3.

FIG. 3



EX-1009, FIG. 3 (annotated)

8. **Claim 9: The charge pump circuit of claim 1 wherein each load selector means comprises an elevator circuit having an input terminal and an output terminal, the input terminal being coupled to an enable signal, the output terminal being coupled to a load NMOS transistor, the gate of the load NMOS transistor being connected to the output terminal of the elevator circuit, the drain of the NMOS transistor being coupled to the pump output, and the source being coupled to the load.**

155. The '241 Patent does not describe what an “elevator circuit” is. EX-1001, 5:32-43, FIG. 5B. The term “elevator circuit” also is not a term in the art in the context of charge pump circuits. In my opinion, a POSITA would have considered a level shifter, which is refers to a common type of circuit for increasing or decreasing the voltage level of a signal, as an example of the claimed “elevator circuit.” In this case, claim 9 merely recites an obvious design choice from Ujiie, as a POSITA would have readily found.

156. Specifically, a POSITA would have found it obvious to modify FIG. 3

of Ujiie by swapping positions of diodes D1 and D2 with respective NMOS switches Q1 and Q2, such that the sources of Q1 and Q2 are connected to the cathodes of D1 and D2, respectively. See ¶ 150-152. In Ujiie's original circuit of FIG. 3 as reproduced in ¶ 150, the source terminals of Q1 and Q2 are connected to the ground, so the source voltages of Q1 and Q2 are equal to the ground voltage (usually 0V). With the modification to the circuit as described in ¶ 143, the source voltages of Q1 and Q2 are higher than the ground voltage due to voltage drop on diodes D1 and D2.

157. In general, for an NMOS transistor to turn on, the gate-to-source voltage V_{GS} must be greater than a threshold voltage V_{th} ; thus the increase of the source voltages of NMOS transistors Q1 and Q2 would require an increase of the gate voltages of Q1 and Q2 in order to satisfy adequate V_{GS} for activating Q1 and Q2. To increase the gate voltages of Q1 and Q2, it would have been obvious for a POSITA to use a level shifter to boost the voltage of control signals A1 and A2 to levels higher than that those in Ujiie's original, un-modified circuit.

158. To this end, a POSITA would have found it obvious to couple control signals A1 and A2 to an input terminal of respective level shifters and couple the output terminal of respective level shifters to the gate terminal of respective NMOS transistors Q1 and Q2. Such arrangement would read on claim 9.

9. Claim 10: The charge pump circuit of claim 9, wherein each load is a capacitor or a current sinker having a first terminal and a second terminal, the first terminal being coupled to the source of

the NMOS transistor and the second terminal being coupled to an electrical ground.

159. Diodes were well-known as current sinkers as of the Critical Date.

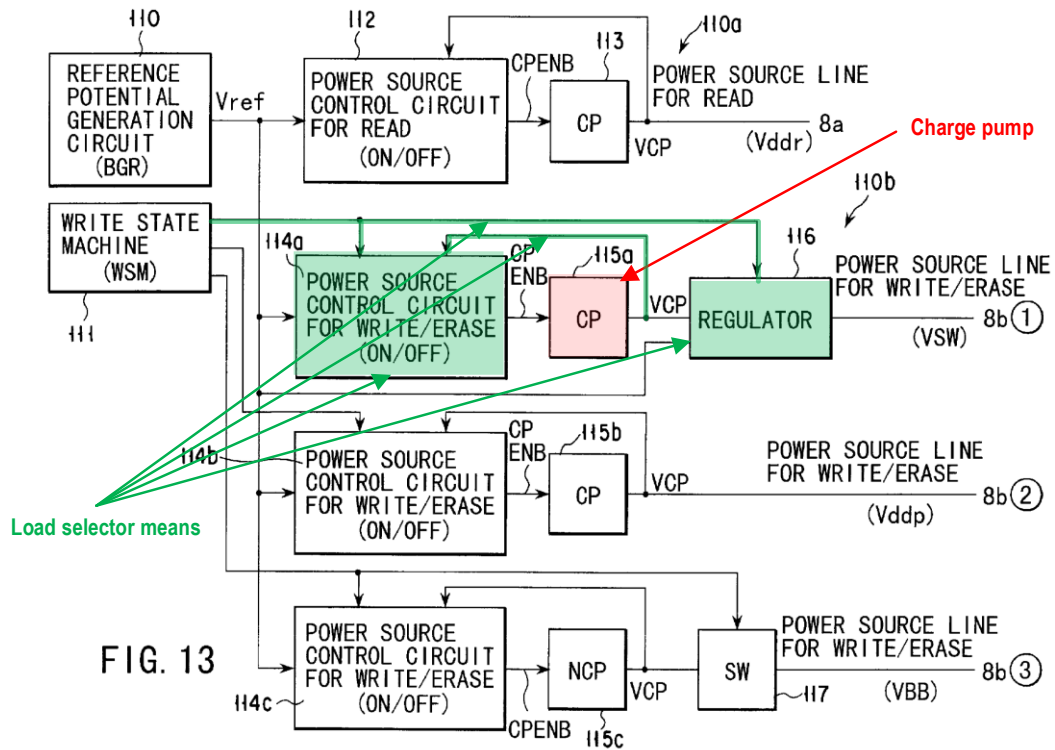
See ¶ 154. As noted previously, an obvious modification of Ujiie's FIG. 3 would have resulted in the cathodes of D1 and D2 being connected to the sources of NMOS switches Q1 and Q2, respectively, and the anodes of D1 and D2 being connected to ground. See ¶¶ 150-152. Such arrangement would read on claim 10.

X. GROUND 2B: Claims 2, 3, 11, 24, and 25 are rendered obvious by Le, Ujiie, and Kuriyama

A. Overview of Kuriyama

160. I have fully reviewed Kuriyama. In my understanding, Kuriyama's disclosure includes the following aspects.

161. Kuriyama discloses a memory device power system that uses a charge pump 115a to provide boosted voltage to memory cells. EX-1011, 4:42-5:18, 11:19-13:3, FIGS. 12-15. To generate a target output voltage, Kuriyama turns charge pump 115a on and off by comparing the output voltage with a reference voltage V_{ref} , and further regulates the output voltage using a regulator having multiple operational amplifiers (OPs). *Id.*, 11:38-12:45, FIGS. 13-15 (reproduced below).



EX-1011, FIG. 13 (annotated)

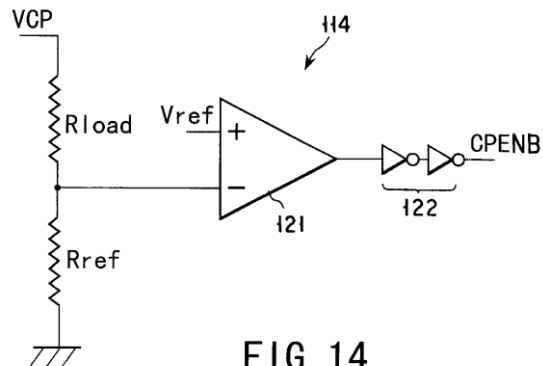


FIG. 14

EX-1011, FIG. 14

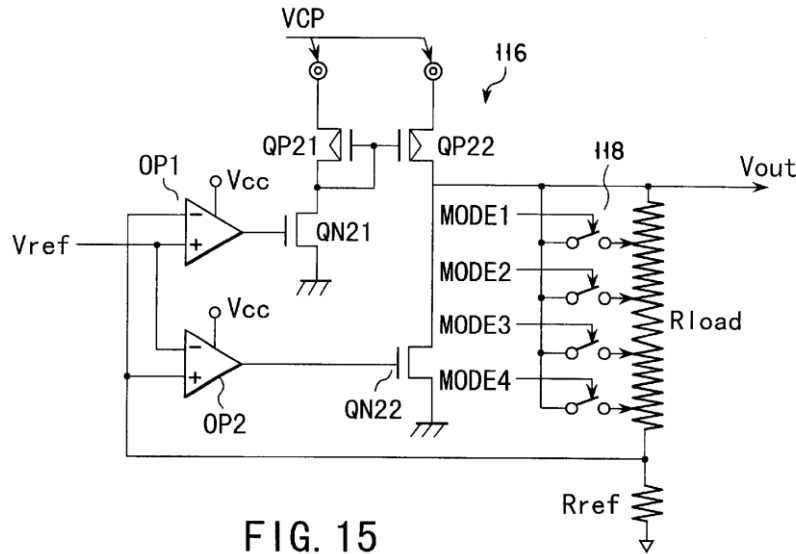


FIG. 15

EX-1011, FIG. 15

162. More specifically, power source control circuit 114a in FIG. 13 of Kuriyama receives a feedback signal from the output VCP of charge pump 115a. *Id.* Based on the voltage level of VCP, power source control circuit 114a generates an enable signal CPENB that controls charge pump 115a to turn on or off. *Id.* Consistent with a common practice in circuit design, the label “CPENB” suggests that the enable signal is active-low, meaning that the charge pump is enabled when CPENB equals logic “0” and is disabled when CPENB equals logic “1.”

163. FIG. 14 of Kuriyama provides the detailed structure of the circuit that generates enable signal CP ENB: The charge pump output voltage VCP is sampled by a voltage divider formed by resistors Rload and Rref, and the sampled voltage is compared with a reference voltage Vref at comparator 121. *Id.* According to the illustration in FIG. 14 and as would have been readily understood by a POSITA,

because V_{ref} is connected to the “+” input and the sampled voltage is connected to the “-“ input, comparator 121 outputs logic “0” when the sampled voltage is greater than V_{ref} and outputs logic “1” when the sampled voltage is less than V_{ref} . The output of comparator 121 is stabilized by buffers 122 and then becomes CPENB.

164. In addition to power source control circuit 114a, regulator 116 in FIG. 13 of Kuriyama serves as another mechanism for achieving the target output voltage level. *Id.*, 12:28-46, FIG.15. The detailed structure of regulator 116 is provided in FIG. 15 of Kuriyama. *Id.* As a POSITA would have readily understood upon reviewing Kuriyama, regulator 116 controls the output V_{out} of charge pump circuit 115a based on a comparison between V_{CP} (as divided using resistors R_{load} and R_{ref}) and V_{ref} . *Id.*

B. Combination of Le, Ujiie, and Kuriyama

165. In my opinion, a POSITA would have found it obvious to combine Kuriyama with Le and Ujiie. In the charge pump circuit of Le-Ujiie, a shunt regulator having a load selector means is used to selectively couple loads to the pump output in order to regulate the output voltage. See ¶¶ 142-149. A POSITA would have known, or would have found it obvious (or advantageous), that having an additional mechanism to shut down the charge pump in some instances would benefit the voltage regulation and/or improve power efficiency. Thus, the POSITA

would have had the motivation to include additional circuitry in the load selector means to shut down the charge pump when the output voltage exceeds the desired threshold and enables the charge pump when the voltage is below the desired threshold. This is basic feedback theory that is ubiquitous in almost every regulated voltage source.

166. Similar to Le and Ujiie, Kuriyama describes using a charge pump to provide voltages to memory devices and is concerned about regulating the charge pump output voltage using . See ¶ 161; EX-1011, 4:42-5:18, 11:19-13:3. Given the operations described in ¶¶ 162-164, a POSITA would have found it obvious that including Kuriyama's control circuit 114a in Le-Ujiie's charge pump circuit provided the capability to turn off the charge pump circuit when V_{OUT} reached a reference voltage, e.g., V_{pp1} or V_{pp2} . In view of Kuriyama's teachings about regulator 116 as part of the overall circuitry for adjusting the output voltage, the POSITA would have found it an obvious design choice to further include regulator 116 in Le-Ujiie's charge pump circuit. The POSITA would have understood that the inclusion provides flexibility to regulate the charge pump output, e.g., by enabling additional target voltage levels to be provided by the charge pump circuit beyond V_{pp1} and V_{pp2} . The POSITA would have had a reasonable expectation of success in doing so, as the operation of the resulting circuit would have been completely predictable. Accordingly, a POSITA would have had the motivation to

combine Le, Ujiie, and Kuriyama.

C. Analysis

1. Claim 2: The charge pump circuit of claim 1, wherein the load selector means includes a target output pump selector for shutting down the variable charge pump circuit when the target output pump voltage (V_{cfra}) is greater than or equal to a reference voltage (V_{ref}).

167. As noted above, I believe that a POSITA would have been motivated to include Kuriyama's control circuit 114a as part of the load selector means in Le-Ujiie's charge pump circuit to provide the capability to turn off the charge pump circuit when V_{OUT} (the claimed "target output voltage (V_{cfra})") reaches a reference voltage, e.g., V_{pp1} or V_{pp2} . See ¶¶ 161-163, 165-166. Kuriyama's control circuit 114a in the Le-Ujiie-Kuriyama combination thus performs the function of the "target output pump selector."

2. Claim 3: The charge pump circuit of claim 2, wherein the load selector means further includes a maximum ripple on the target output selector means for adding a load, whenever a maximum ripple on the target output voltage (V_{cfrb}) greater than the reference voltage (V_{ref}) then the maximum ripple on the target output selector means adds additional loads until the V_{cfrb} voltage is less than or equal to the reference voltage (V_{ref}).

168. As noted above, a POSITA, exercising an obvious design choice, would have been motivated to include Kuriyama's regulator 116 as part of the load selector means in Le-Ujiie's charge pump circuit. See ¶ 166. This provides flexibility to regulate the charge pump output, e.g., by enabling additional target voltage levels to be provided by the charge pump circuit beyond V_{pp1} or V_{pp2} voltages.

adjustment can be made by using signals MODE1-MODE4 to control switch 118 and thereby change the value of R_{load} . For example, when V_{out} is higher than a corresponding threshold voltage (the claimed “maximum ripple on the target output voltage (V_{cfrb})”), it would have been obvious to a POSITA to control switch 118 to reduce the value of R_{load} (e.g., changing from R_1 to R_4 by switching from MODE1 to MODE4). The decrease of the value of R_{load} causes an increase to the voltage at the “+” terminal of operational amplifier (op-amp) OP2 due to the voltage division between R_{load} and R_{ref} . EX-1011, 12:28-55, FIG. 15.

171. A well-known property of an op-amp is that the output voltage is substantially proportional to the voltage difference between the “+” and “-” input terminals. Thus, with the “-” terminal of OP2 coupled to V_{ref} , a voltage increase at the “+” terminal causes the OP2 output voltage to increase, which increases the bias voltage at the gate terminal of QN22.

172. A well-known property of an NMOS transistor (such as QN22) is that, when the NMOS transistor is biased at the gate terminal, an increase of the gate-to-source voltage V_{GS} causes the effective resistance R_{DS} between the drain terminal and the source terminal to decrease. EX-1017, 213-220. The decrease in R_{DS} causes the current flowing through QN22 to increase, and in turn causes V_{out} to decrease, thereby regulating V_{out} utilizing bleeder or shunt regulation.

173. With the knowledge about the mechanism described in ¶¶ 170-172, a

POSITA would have understood that the mechanism for adjusting Rload to increase the gate bias of QN22 and correspondingly the current flowing through QN22 can be likened to “adding additional loads.” Accordingly, I believe that a POSITA would have found this teaching of Kuriyama in combination with Le and Ujiie renders the features of claim 3 obvious.

3. Claim [11a]: The charge pump circuit of claim 2 wherein the target output pump selector comprises: a) a first comparator having two input terminals, an output terminal and a first enable terminal, one of the two input terminals being connected to the reference voltage (Vref)

174. A POSITA would have understood that Kuriyama’s control circuit 114a in the Le-Ujiie-Kuriyama combination performed the function of the claimed “target output pump selector.” See ¶ 167. In FIG. 14, Kuriyama shows that control circuit 114a (labeled 114 in FIG. 14) has comparator 121 (the claimed “first comparator”) with two input terminals, labeled “+” and “–,” respectively. EX-1011, FIG. 14, 12:19-27. Kuriyama shows that comparator 121 has an output terminal (the claimed “output terminal”), which provides enable signal CPENB to control charge pump 115a to turn on or off. *Id.*; see ¶ 162. As of the Critical Date, it was well-known in circuit design that a comparator can have an enable terminal that enables or disables the functioning of the comparator. See ¶ 113. Accordingly, whether the claimed “first enable terminal” refers to the comparator output that enables the charge pump or the comparator input that enables the comparator itself, the features in [11a] would have been obvious in view of

Kuriyama.

4. Claim [11b]: b) a first resistor network having two terminals, the first terminal being coupled to the output pump, the second terminal being coupled to one of the input terminals of the first comparator

175. With comparator 121 in Kuriyama's FIG. 14 reading on "the first comparator," FIG. 14 of Kuriyama further shows resistor Rload with its upper terminal coupled to VCP ("output pump") and with its lower terminal coupled to the "-" input of comparator 121. EX-1011, FIG. 14. Rload thus reads on the claimed "first resistor network."

5. Claim [11c]: c) a second resistor network having two terminals, the first terminal being coupled to the second terminal of the first resistor network, and the second terminal of the second resistor network being coupled to an electrical ground

176. Consistent with ¶¶ 174-175, FIG. 14 of Kuriyama further shows resistor Rref. The upper terminal of Rref is coupled to the lower terminal of Rload (which reads on the "first resistor network", see ¶ 175) and the lower terminal of Rref is coupled to the ground. EX-1011, FIG. 14. Rref thus reads on the claimed "second resistor network."

6. Claim [11d]: d) a reference voltage source (Vref) coupled to one of the input terminals of the first comparator

177. FIG. 14 of Kuriyama shows signal V_{ref} coupled to the "+" input terminal of comparator 121. *Id.* Signal V_{ref} thus reads on the claimed "reference voltage source (Vref)."

7. Claim 24: A method for generating an output voltage with minimal ripples in a charge pump circuit, comprising: a) selecting a output pump voltage (V_{pump}); b) turning on a load associated

with the selected V_{pump} ; c) comparing a target output voltage (V_{cfra}) with a reference voltage (V_{ref}) whenever the target output voltage greater than the reference voltage, disabling the charge pump circuit; whenever the target output voltage is less or equal to the voltage reference, leaving the charge pump circuit on.

178. I have explained that Le, Ujiie, and Kuriyama teach all features of claim 24, see ¶¶ 144-149, 161-163, 167, 174, except “whenever the target output voltage is less or equal to the voltage reference, leaving the charge pump circuit on.”

179. Disclosing the operations of comparator 121 in FIG. 14, Kuriyama, in combination with Le and Ujiie, would have made it obvious to a POSITA to disable the charge pump circuit when $V_{\text{cfra}} > V_{\text{ref}}$. See ¶¶ 162-162, 174. I believe that this further would have made it obvious to a POSITA to leave the charge pump circuit on when $V_{\text{cfra}} \leq V_{\text{ref}}$. EX-1011, 11:61-65.

180. Accordingly, a POSITA would have found all features of claim 24 obvious in view of the combination of Le, Ujiie, and Kuriyama.

8. Claim 25: The method of claim 24, further comprises the following steps: a) comparing a maximum acceptable ripple on output voltage value (V_{cfrb}) with a reference voltage (V_{ref}) whenever the maximum acceptable ripple output voltage value is greater than the reference voltage, connecting a load until the V_{cfrb} voltage value is less than or equal to the reference voltage; b) comparing a minimum acceptable drop on output voltage value (V_{cfrc}) with the reference voltage (V_{ref}), whenever the minimum acceptable drop on output voltage value is less than the reference voltage, removing a load until the V_{cfrc} voltage value is greater than the reference voltage.

181. I have explained that Le, Ujiie, and Kuriyama teach feature a) of claim 25: “a) comparing a maximum acceptable ripple on output voltage value

(Vcfrb) with a reference voltage (Vref) whenever the maximum acceptable ripple output voltage value is greater than the reference voltage, connecting a load until the Vcfrb voltage value is less than or equal to the reference voltage.” See ¶¶ 164, 168-173.

182. Kuriyama also renders obvious the remaining feature b) of claim 25: “b) comparing a minimum acceptable drop on output voltage value (Vcfrc) with the reference voltage(Vref), whenever the minimum acceptable drop on output voltage value is less than the reference voltage, removing a load until the Vcfrc voltage value is greater than the reference voltage.” Specifically, because Kuriyama would have made it obvious that adding loads can reduce the pump output voltage, see ¶¶ 168-173, a POSITA would have readily understood that removing loads can conversely increase the pump output voltage.

183. Accordingly, a POSITA would have found all features of claim 25 obvious in view of the combination of Le, Ujiie, and Kuriyama.

XI. GROUND 2C: Claims 4 and 5 are rendered obvious by Le, Ujiie, and Hosono

A. Combination of Le, Ujiie, and Hosono

184. Hosono’s disclosures about using a charge pump output circuit to supply voltage to memory devices, and to regulate the supplied voltage are similar to the teachings of Le and Ujiie. EX-1007, 1:6-41, 2:65-3:31, 5:5-64, 14:51-15:5; see ¶¶ 99-101, 138-139, 141-143. Thus, a POSITA would have been motivated to

look to Hosono for teachings that would supplement or improve upon Le and Ujiie.

185. For example, Le discloses that its charge pump system 300 includes clock signal pairs CLK and $\overline{\text{CLK}}$, which “oscillate from 0 to V_{cc} .” EX-1008, FIG. 3, 3:25-30. Le does not specify the circuit structure behind the generation of CLK and $\overline{\text{CLK}}$, so a POSITA would have looked into other references for supplemental teachings. The POSITA would have found Hosono, which discloses in FIG. 5A a ring oscillator for generating biphas clock signals ϕ and $\bar{\phi}$, and discloses in FIG. 5B coupling clock signals ϕ and $\bar{\phi}$ to a multi-stage charge pump. EX-1007, FIGs. 5A-5B, 14:13-35. Accordingly, I believe that a POSITA would have been motivated to combine Hosono with Le-Ujiie to implement a multi-stage charge pump circuit with biphas clock signals. A POSITA would have had a reasonable expectation of success in making this combination, as these techniques were known and the operation of the resulting circuit would have been predictable.

B. Analysis

1. Claim [4a]: The charge pump circuit of claim 1, wherein the pumping circuit comprises: a) a plurality of diodes coupled in series, each diode having an input terminal and an output terminal, the input terminal of the first diode in the series is coupled to the supply voltage, the output of the first diode being connected to the input terminal of the second diode, and the output terminal of the last diode connected to the output pump

186. In Le’s charge pump system 300 shown in FIG. 3, charge pump circuit 305 receives supply voltage V_{cc} and provides output voltage V_{OUT} . EX-1008, FIG. 3. Charge pump circuit 305 is shown to have a number of diodes

connected in series, including diode 315 (“first diode”), 325 (“second diode”), and 340 (“last diode”). Each diode has an anode (“input terminal”) and a cathode (“output terminal”), as would have been well-known to a POSITA. The anode and cathode of 315 are respectively coupled to V_{cc} (“supply voltage”) and the anode of 325, while the cathode of 340 is coupled to V_{OUT} (“output pump”). *Id.* These arrangements read on [4a].

2. Claim [4b]: b) a plurality of capacitors having a first terminal and a second terminal, wherein the first terminal of the first capacitor being coupled to the output of a first diode and the input of a second diode, the first terminal of the second capacitor being coupled to the output of the second diode and the input of a third diode, and the first terminal of the last capacitor is coupled to the input terminal of a last diode

187. Le’s charge pump circuit 305 in FIG. 3 is shown to have a number of capacitors, including C_{0eff} (“first capacitor”), C_{1eff} (“second capacitor”) and C_{neff} (“last capacitor”). *Id.* Each capacitor has two plates, each of which has a terminal, as would have been understood by a POSITA. For each of capacitors C_{0eff} , C_{1eff} , and C_{neff} , the plate illustrated in the figure with an upper position (i.e., the terminal illustrated as coupled to a respective node of Nodes 1, 2, and n) reads on the “first terminal”), and the plate illustrated in the figure with a lower position (i.e., the terminal illustrated in the figure as coupled to CLK or $\overline{CLK}$) reads on the “second terminal.” *Id.* Specifically, the upper plate of C_{0eff} is shown to be coupled to the cathode of first diode 315 and to the anode of second diode 325 at Node 1. *Id.* The upper plate of C_{1eff} is shown to be coupled to the cathode of second diode 325

and to the anode of next diode in the series (“third diode”) at Node 2. *Id.* The upper plate of C_{neff} is shown to be coupled to the anode of diode 340 (“last diode”) at Node n. *Id.* These arrangements read on [4b].

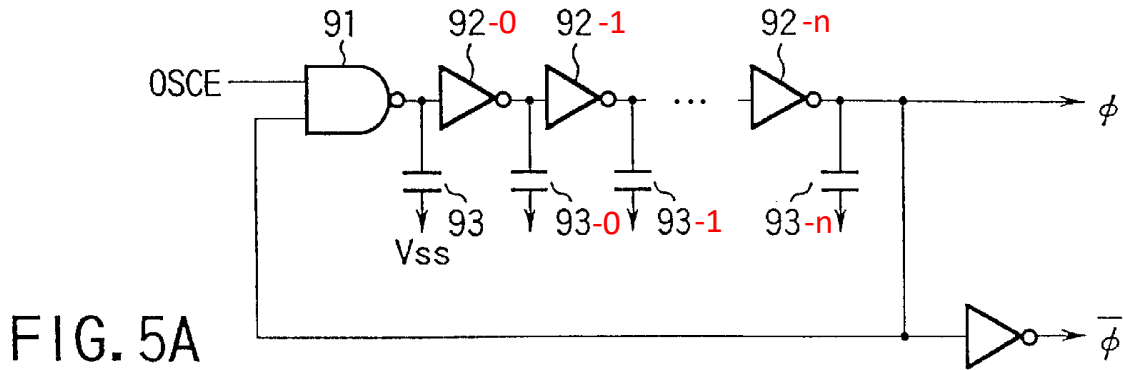
3. Claim [4c]: c) a plurality of inverters coupled in series to one another, each having an input terminal and an output terminal, the output of the first inverter being coupled to the second terminal of the first capacitor forming the first stage of the charge pump circuit, the second output of the second inverter coupled to the second terminal of the second capacitor forming the second stage of the charge pump circuit, and the output of the last inverter is coupled to the second terminal of the last capacitor forming the last stage of the charge pump circuit

188. Le teaches clock signals CLK and $\overline{CLK}$ provided to the lower plates of capacitors C_{0eff} to C_{neff} , and Ujiie similarly teaches clock signals ϕ and $\bar{\phi}$ provided to the lower plates of capacitors C_1 - C_m . EX-1008, FIG. 3; EX-1009, FIG.

4. However, neither Le nor Ujiie explicitly describes the circuit that generates the clock signals, so a POSITA would have been motivated to look at Hosono, which not only discloses the generation of biphase clock signals ϕ and $\bar{\phi}$ in FIG. 5A, but also discloses the coupling of clock signals ϕ and $\bar{\phi}$ to capacitors of a multi-stage charge pump in FIG. 5B. See ¶ 185.

189. FIG. 5A of Hosono shows a ring oscillator with four inverters labeled 92. EX-1007, FIG. 5A. A POSITA would have readily understood that the output of each of inverter 92 is either ϕ or $\bar{\phi}$, and that the outputs of two consecutive inverters are opposite to each other. The POSITA would have found it obvious to make a generalized ring oscillator structure with more or less than four inverters,

such as the one illustrated below that has with $(n+1)$ inverters labeled 92-0, 92-1, ... 92-n. Correspondingly, the output of each of inverters 92-0, 92-1, ... 92-n is coupled to a capacitor labeled 93-0, 93-1, ... 93-n, respectively.



EX-1007, FIG. 5A (modified, relabeled with colored text)

190. Hosono further teaches that clock signals ϕ and $\bar{\phi}$ output by inverters 92 of the ring oscillator can be used in the charge pump circuit shown in FIG. 5B. *Id.*, 14:13-26. Accordingly, it would have been obvious to a POSITA that the ring oscillator having $(n+1)$ inverters, as expanded from Hosono's FIG. 5A, can be used in Le's charge pump circuit having $(n+1)$ corresponding capacitors. In the combined circuit, capacitors 93-0, 93-1, ... 93-n would be in the positions of $C_{0\text{eff}}$, $C_{0\text{eff}}$, ... $C_{n\text{eff}}$, respectively. Each of the capacitors would be driven by a clock signal output by a corresponding inverter in the series that outputs either ϕ or $\bar{\phi}$. Each capacitor forms a stage, totaling $(n+1)$ stages in the charge pump circuit. See ¶ 139.

191. In my opinion, the above-described expansion of Hosono's FIG. 5A

and combination of Hosono with Le would have been obvious to a POSITA. The resultant circuit would read on the features of [4c].

4. Claim [4d]: d) a clock signal coupled to the input terminal of the first inverter

192. A POSITA would have readily understood that the input to the first inverter 92-0 in the expanded ring oscillator illustrated in ¶ 189 is a clock signal. This would read on [4d].

5. Claim 5: The variable charge pump circuit of claim 4, wherein each of the plurality of diodes is a diode-connected NMOS transistor, the gate of each transistor being connected to its drain forming the input terminal and its source forming the second terminal.

193. Le describes diode connected NMOS transistors 515-518 being used instead of regular diodes in charge pump systems. EX-1008, 9:27-10:7, FIG. 5. This is consistent with the knowledge that a POSITA would have had that diode-connected NMOS transistors are often interchangeable with diodes. Le's FIG. 5 shows that each of NMOS transistors 515-518 has the gate terminal connected to the drain terminal, together effectively forming the anode (i.e., input terminal) of a diode. A POSITA would also have understood that the source terminal of each of NMOS transistors 515-518 effectively forms the cathode (i.e., output terminal) of the same diode.

XII. GROUND 3A: Claims 13-17, 19, and 21-23 are rendered obvious by Asano, Le, Ujiie, and Kuriyama

A. Overview of Asano

194. I have fully reviewed Asano. In my understanding, Asano's disclosure includes the following aspects.

195. Asano describes a memory system that provides boosted voltages to memory cells, such as Erasable Programmable Read Only Memory (EPROM) cells. EX-1012, 1:6-2:5, 4:40-5:4, 7:50-8:59, FIGS. 3-15. FIG. 3 of Asano provides the architecture of a memory cell array 10 along with peripheral circuitry. *Id.*

B. Combination of Asano, Le, Ujiie, and Kuriyama

196. Asano's disclosure about the memory system is in a context similar to those of Le, Ujiie, and Kuriyama, as all of these references are concerned about providing memory devices with boosted voltages that are generated from charge pump circuits. See ¶¶ 138-139, 141, 161-164, 195.

197. I believe that a POSITA would have been motivated to combine Asano with Le (possibly with further obvious modifications based on Ujiie and Kuriyama). Le discloses that its charge pump circuit can be used to provide boosted voltage for memory devices without providing structural details of a memory device, leaving it to a POSITA's choice of implementation to use Le's

charge pump circuit in various memory devices. EX-1008, 1:7-5:26. A POSITA would have noted that Asano teaches a memory device that uses a voltage boosting circuit to provide a boosted voltage to the memory cells. EX-1012, 1:6-5:4. A POSITA accordingly would have found it obvious to use Le's charge pump circuit as a design alternative to Asano's own voltage boosting circuit. A POSITA would have had a reasonable expectation of success, as such change to Asano's memory device would have been a combination of known techniques yielding predictable results.

C. Analysis

1. Claim [13a]:

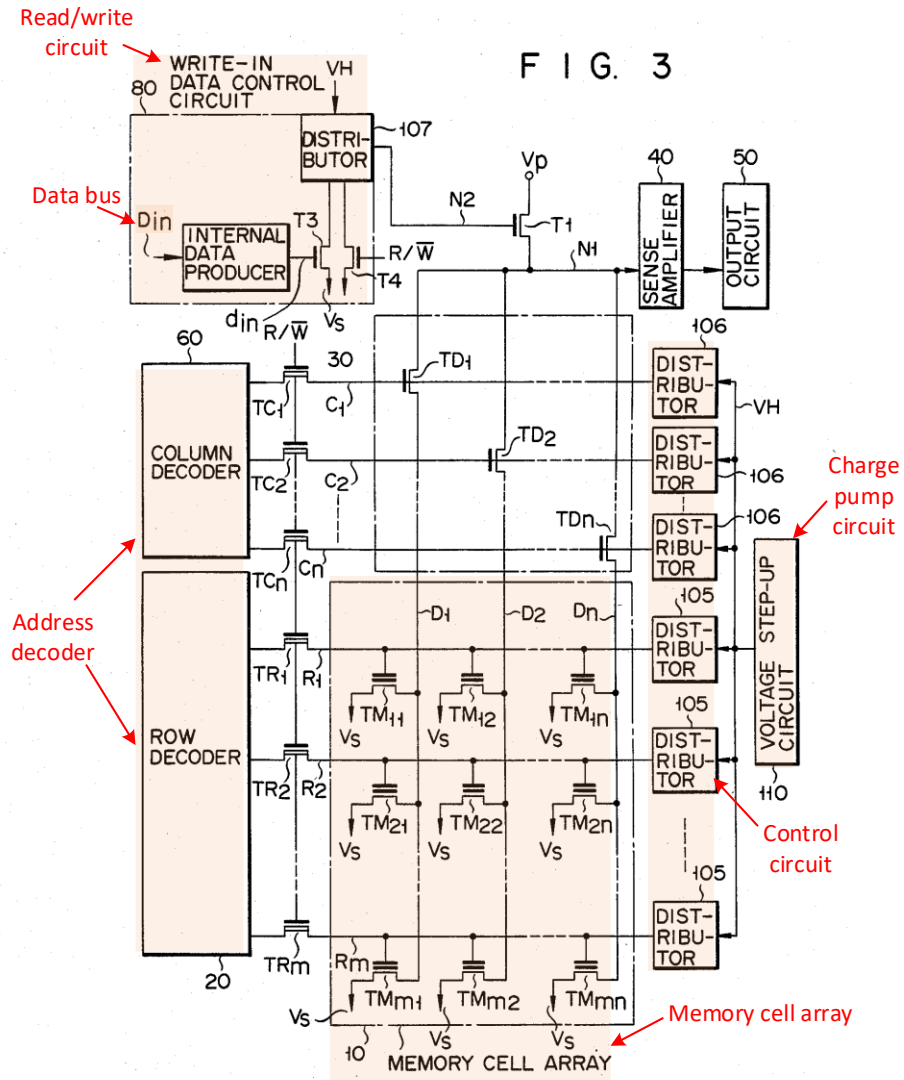
A memory device, comprising: an address bus; a control circuit; a data bus; an address decoder coupled to the address bus; a read/write circuit coupled to the data bus; a memory cell array coupled to the address decoder, control circuit, and read/write circuit; and

a charge pump circuit that generates a boosted output voltage with minimum ripples on an output node coupled to the address decoder, read/write circuit, and memory cell array, the charge pump circuit comprising:

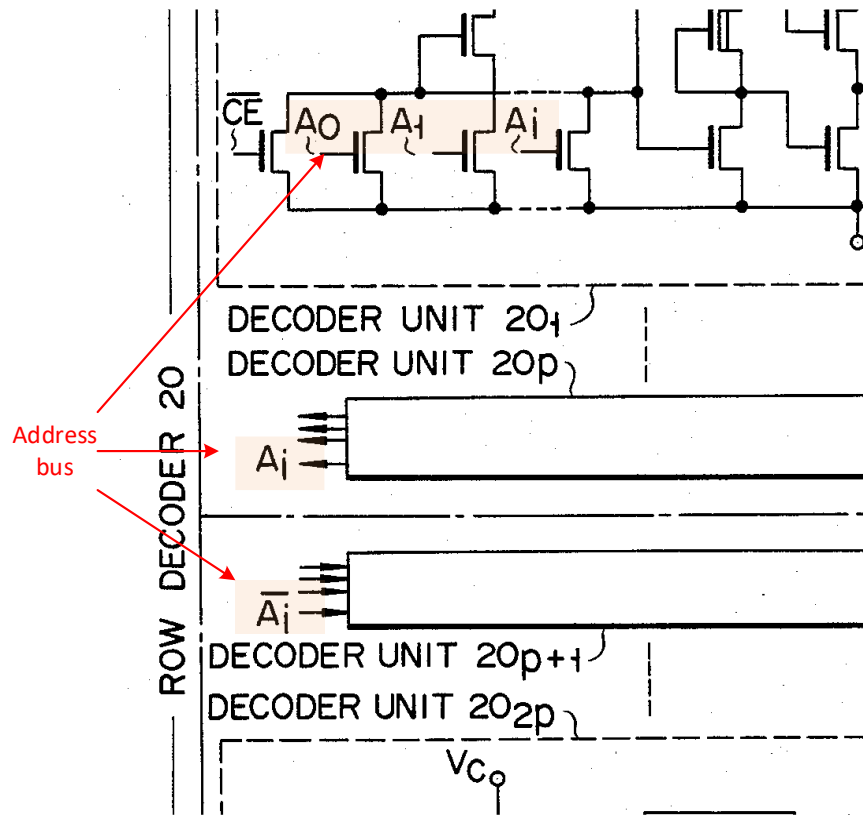
198. Le, Ujiie and Kuriyama all disclose that their charge pump circuits are for use in memory devices. See ¶¶ 138-139, 142, 161-164. Indeed, it was well-known as of the Critical Date to use charge pump circuits to provide memory devices with boosted voltage. See, e.g., EX-1017, at 826. It was also well-known as of the Critical Date that a memory device in general can have an address bus, a control circuit, a data bus, an address decoder coupled to the address bus, a

read/write circuit coupled to the data bus, and a memory cell array coupled to the address decoder, control circuit, and read/write circuit.

199. Asano provides an example of such a well-known memory device architecture described in ¶ 198. EX-1012, 2:22-3:10; 6:4-8:59, FIGs. 3, 6, 10, 17A-17B. As illustrated in Asano's FIG. 3, memory cell array 10 is coupled, via transistors TC_1 to TC_n and TR_1 to TR_n , to column decoder 60 and row decoder 20 (which read on the "address decoder"). *Id.*, FIG. 3. Memory cell array 10 is shown as being coupled to distributors 105 and 106 (which read on the "control circuit") that distribute boosted voltage under the control of a control signal. *Id.*, FIG. 3, 6:4-64. Memory cell array 10 is shown as also being coupled, via transistors TC_1 to TC_n and TR_1 to TR_n , to the output port $R/\bar{W}$ of write-in data control circuit 80 (which reads on the "read/write circuit"). *Id.*, FIG. 3. FIG. 3 shows external input data D_{in} (which reads on the "data bus") as an input to write-in data control circuit 80. *Id.* Furthermore, FIG. 10 of Asano shows that row decoder 20 is coupled to signals $A_0, A_1, \dots A_i$, which read on the "address bus." EX-1012, 2:22-46, 16:54-17:31, FIGs. 10 (reproduced below), 17A-17B.



EX-1012, FIG. 3 (annotated)



EX-1012, FIG. 10 (partial, annotated)

200. FIG. 3 of Asano also shows voltage set-up circuit 110 (referred to in the specification as “boosting circuit 110” for providing a “boosted voltage,” which reads on the “charge pump circuit that generates a boosted output voltage”). *Id.*, FIG. 3, 6:4-8:59. Boosting circuit 110 generates output voltage V_H , which is applied to the memory cell array according to a selection by row decoder 20. *Id.*, FIG. 3, 10:65-11:16. According to FIG. 3, the output of boosting 110 is coupled to distributors 105 and further coupled, via distributors 105, to row decoder 20, write-in data control circuit 80, and memory cell array 10. *Id.*, FIG. 3.

201. Accordingly, Asano discloses all the components of [13a], as well as

the arrangement of these components as described in [13a]. Combining Asano with Le, Ujiie and Kuriyama, a POSITA would have found it obvious to control the resultant charge pump circuit to minimize voltage ripples, e.g., by using a shunt regulator.

2. Claim [13b]:

- a) a pumping circuit comprising one or more stages operable to receive a supply voltage and generate one or more pump voltages;**
- b) a plurality of loads, each load associated with a specific pump voltage and selectively coupleable to an output of the pump circuit (output pump);**
- c) a load selector means coupled to the output pump for selecting a load that satisfies a specific pump voltage;**
- d) a target output pump selector sampling the output of the pump circuit for shutting down the variable charge pump circuit whenever the sampled output voltage (V_{cfra}) is greater than or equal to a reference voltage (V_{ref});**
- e) a maximum ripple on target output selector means sampling the output of the pump circuit for adding a load, whenever a maximum ripple on sampled output voltage (V_{cfrb}) is greater or equal to than the reference voltage (V_{ref}) then the output selector means adds additional loads until the V_{cfrb} voltage is less than the reference voltage (V_{ref}).**

202. As I have explained in my analysis of claims 1-3 in Grounds 2A and 2B, the Le-Ujiie-Kuriyama combination teaches all features of [13b]. See ¶¶ 144-149, 167-173.

3. Claim 14: A memory system of claim 13, wherein the pumping circuit comprises:

- a) a plurality of diodes coupled in series, each diode having an input terminal and an output terminal, the input terminal of the first diode in the series being coupled to the supply voltage, the output of the first diode being connected to the input terminal of the second diode, and the output terminal of the last diode connected to the output pump voltage;**

b) a plurality of capacitors having a first terminal and a second terminal, wherein the first terminal of the first capacitor being coupled to the output of the first diode, the first terminal of the second capacitor being coupled to the output of the second diode, and the first terminal of the last capacitor being coupled to the input terminal of the last diode;

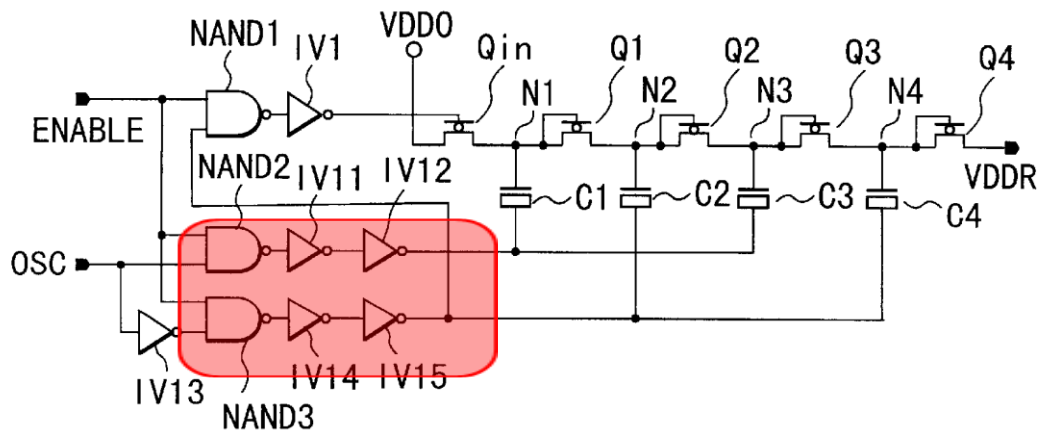
c) a plurality of inverter coupled in series to one another, each having an input terminal and an output terminal, the output of the first inverter being coupled to the second terminal of the first capacitor and the input of the second inverter forming the first stage of the charge pump circuit, the second output of the second inverter coupled to the second terminal of the second capacitor forming the second stage of the charge pump circuit, and the output of the last inverter being coupled to the input of the last diode;

d) a clock signal coupled to the input terminal of the first inverter.

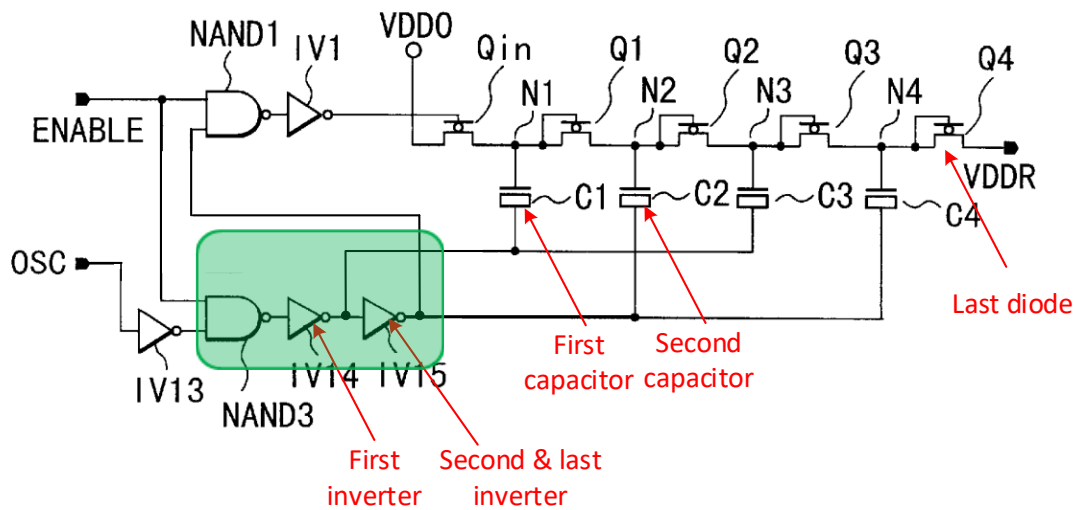
203. As I have explained in my analysis of claim 4 in Ground 2C above, Le teaches features a) and b) recited by claim 14. See ¶¶ 186-187, 192.

204. With regards to feature c), Asano, Le, and Ujiie do not explicitly describe the circuit structure that generates clock signals in their respective charge pumps, so a POSITA would have been motivated to look at other references for description of a clock generator for charge pump circuits used in memory devices. A POSITA would have found Kuriyama, in particular, FIG. 8 of Kuriyama, shows oscillation signal OSC passing through logic gates NAND2 and NAND3 and inverters IV11-IV14. I believe that a POSITA would have further understood that the circuit in FIG. 8 is logically equivalent to a modified version. Both original FIG. 8 and the modified version are reproduced below, with the original and modified portions highlighted in red and green, respectively. The modification would have been obvious given the simplicity of changes and the logic equivalence

between before and after the changes.



EX-1011, FIG. 8 (annotated)



EX-1011, FIG. 8 (modified, annotated)

205. Modified FIG. 8 of Kuriyama reads on the features of c). As illustrated in ¶ 204, two inverters IV14 and IV15 are coupled in series, with the output of first inverter IV14 coupled to the input of second inverter IV15. See ¶ 204. The output of first inverter IV14 is coupled to the anodes (i.e., “second

terminals” of capacitors in the context of claim 14) of capacitors C1 (“first capacitor,” which forms the first stage) and C3, while the output of second inverter IV15 is coupled to the anode of capacitors C2 (“second capacitor,” which forms the second stage). See ¶ 204. Additionally, the output of IV15, which is also the last inverter in the series, is coupled to the anode of diode Q4 (“last diode”) via capacitor C4.

206. With regards to feature d), a POSITA would have understood that the output of NAND3, which is the input of first inverter IV14, can be considered a “clock signal.”

207. Accordingly, a POSITA would have found it obvious to combine Kuriyama with Asano, Le, and Ujiie and would have been motivated to modify Kuriyama as described in ¶ 204. The resultant circuit reads on all features of claim 14.

4. Claim 15: The memory system of claim 13, wherein the plurality of diodes is a NMOS transistor connected as a diode, the gate of each transistor being connected to its drain forming the input terminal and the source forming the second terminal.

208. As I have explained in my analysis of claim 5 in Ground 2C, Le teaches the features recited by claim 15. See ¶ 203.

5. Claim 16: The memory system of claim 13, wherein the load selector means is a switch having a first and a second terminal coupled in series with each load, the first terminal of the switch being coupled to the output pump and the second terminal of the switch is coupled to the load.

209. As I have explained in my analysis of claim 6 in Ground 2A, Le and

Ujiie would have rendered obvious the features recited by claim 16. See ¶¶ 150-152.

6. Claim 17: The memory system of claim 13, wherein each load selector means comprises an NMOS transistor having a gain a drain and a source, the gate of the NMOS load transistor being coupled to an enable signal, the source of the load NMOS load transistor being coupled to an electrical ground, and the drain being coupled to a load.

210. As I have explained in my analysis of claim 7 in Ground 2A, Le and Ujiie would have rendered obvious the features recited by claim 17. See ¶ 153.

7. Claim 19: The memory system of claim 13 wherein each load selector means comprises an elevator circuit having an input terminal and an output terminal, the input terminal being coupled to an enable signal, the output terminal being coupled to a load NMOS transistor, the gate of the load NMOS transistor being connected to the output terminal of the elevator circuit, the drain of the NMOS transistor being coupled to the pump output.

211. As I have explained in my analysis of claim 9 in Ground 2A, Le and Ujiie would have rendered obvious the features recited by claim 19. See ¶¶ 155-158.

8. Claim [21a]:

The memory system of claim 13, wherein load selector means comprises:

a) a first comparator having two input terminal, an output terminal and a first enable terminal, one of the two input terminals connected to the reference voltage (V_{ref});

b) a first resistor network having two terminals, the first terminal being coupled to the output pump, the second terminal being coupled to the output terminal of the first comparator;

c) a second resistor network having two terminals, the first terminal is coupled to the second terminal of the first resistor network, and the second electrical terminal of the second resistor network being coupled to an electrical ground;

212. Feature b) in [21a] recites “second terminal being coupled to the

output terminal of the first comparator.” If the phrase were to instead read “second terminal being coupled to an input ~~the output~~ terminal of the first comparator,” which I believe to be the correct interpretation, then Kuriyama discloses all features of [21a], as I have discussed in the analysis of claim 11 in Ground 2B. See ¶¶ 174-176.

9. Claim [21b]:

- d) a third resistor network having two terminals, the first terminal being coupled to the output pump;**
- e) a fourth resistor network having two terminals, the first terminal being coupled to the second terminal of the third resistor network, the second terminal of the fourth resistor network being coupled to ground;**
- f) a second comparator having two input terminals, and output terminal and an enable terminal, one of the input terminals being coupled to the input terminal of the fourth resistor network and the other of the input terminals being coupled to the reference voltage V_{ref} ;**
- g) a logic circuit having two terminals, the first terminal coupled to the second comparator.**

213. As I have discussed previously, it would have been obvious to include Kuriyama’s control circuit 114a as part of the load selector means in the charge pump circuit of Le-Ujiiie. See ¶ 166. As such, R_{load} , which has a first terminal coupled to VCP (i.e., “output pump”) would read on the claimed “third resistor network” of feature d), and R_{ref} , which has one terminal coupled to R_{load} and another terminal coupled to the ground, would read on the claimed “fourth resistor network” of feature e). EX-1011, FIG. 14.

214. Furthermore, comparator 121 is shown to have two input terminals

“+” and “-,” and an output terminal connected to buffer 122. *Id.* The “-” input terminal is coupled to Rref and the “+” input terminal is coupled to Vref. *Id.* Given that the output of comparator 121 is “acquired as a charge-pumping enable signal CPENB via []buffer 122,” *id.*, 12:19-27, a POSITA would have found it obvious that the output terminal of comparator 121 also serves as the “enable terminal.” Accordingly, comparator 121 would read on the claimed “second comparator” of feature f). In addition, buffer 122 receives an input from comparator 121 and outputs CPENB. *Id.*, FIG. 14. Accordingly, buffer 122 would read on the claimed “logic circuit” of feature g).

215. As I have explained above in ¶¶ 213-214, all features of [21b] are disclosed by Kuriyama.

10. Claim 22:

The memory system of claim 21, wherein the pumping circuit comprises: a) a plurality of capacitors or current sinkers having a first terminal and a second terminal, wherein the first terminal of the first capacitor being coupled to the output of the first diode, the first terminal of the second capacitor being coupled to the output of the second diode, and the first terminal of the last capacitor being coupled to the input terminal of the last diode;

b) a plurality of inverter coupled in series to one another, each having an input terminal and an output terminal, the output of the first inverter being coupled to the second terminal of the first capacitor and the input of the second inverter forming the first stage of the charge pump circuit, the second output of the second inverter coupled to the second terminal of the second capacitor forming the second stage of the charge pump circuit, and the output of the last inverter being coupled to the input of the last diode; and

c) a clock signal coupled to the input terminal of the first inverter.

216. In my analysis of claim 14 in Ground 3A, I have explained that the

features of claim 22 would have been obvious in view of the Asano-Le-Ujiie-Kuriyama combination. See ¶¶ 203-207.

11. Claim 23: The memory system of claim 13, wherein the memory cell is a flash memory cell.

217. Le discloses that its charge pump circuit provides pump voltage for memory cells in flash memory array systems. EX-1008, 1:7-318, 4:31-5:33. This would read on claim 23.

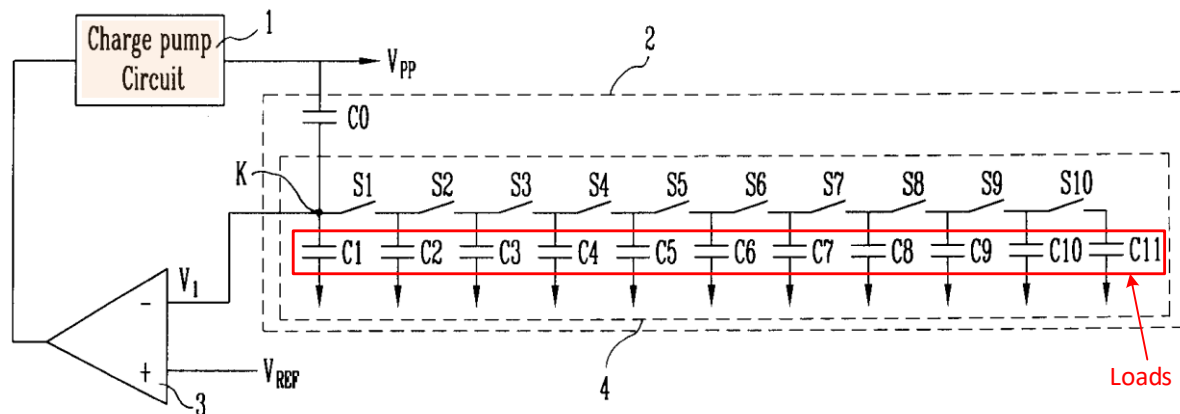
XIII. GROUND 3B: Claims 18 and 20 are rendered obvious by Asano, Le, Ujiie, Kuriyama, and Yang

A. Overview of Yang

218. I have fully reviewed Yang. In my understanding, Yang's disclosure includes the following aspects.

219. Yang discloses using a charge pump to generate voltages for a memory device. EX-1010, 1:7-59, 2:46-65, 4:39-51, FIG. 2 (reproduced below). Similar to some other references I have discussed above, Yang is concerned with reducing voltage ripple at the charge pump output. *Id.* As illustrated in FIG. 2 of Yang, the charge pump output is coupled to a voltage divider circuit 2 comprising a capacitor block 4 with multiple capacitors, which a POSITA would have understood are loads of the charge pump circuit. *Id.*, FIG. 2. These capacitor loads can be selectively coupled to the pump output via C0. For example, as would have been readily understood by a POSITA, closing switch S1 would couple

capacitor C2, closing switches S1 and S2 would couple capacitor C3, and closing switches S1-S10 would couple capacitor C11, to the pump output. *Id.*



EX-1010, FIG. 2 (annotated)

B. Combination of Asano, Le, Ujiie, Kuriyama, and Yang

220. I believe that a POSITA would have found it obvious to combine Yang with Asano, Le, Ujiie and Kuriyama. Similar to Asano, Le, Ujiie, and Kuriyama, Yang discloses using charge pumps to generate voltages for memory devices, and is similarly concerned about regulating charge pump output voltages to reduce voltage ripple. *Id.*, 1:7-59. 4:39-51. A POSITA would have understood that Yang's voltage divider circuit can be used to realize Le's shunt regulator, or used to modify Ujiie's shunt circuit with additional capacitor stages. Such modifications has the potential of providing a finer-grained control in regulating the output voltage, e.g., by enabling generation of multi-step pulses for use with multi-level memory cells. Accordingly, a POSITA would have been motivated to

combine Asano, Le, Ujiie, Kuriyama, and Yang.

C. Analysis

1. Claim 18: The memory system of claim 17, wherein the load is a capacitor having a first terminal and a second terminal, the first terminal being coupled to the pump voltage and the second terminal being coupled to the drain of the NMOS transistor.

221. As discussed in my analysis of Ground 2A, Ujiie provides an example implementation of a shunt regulator to be used in Le's charge pump circuit. See ¶¶ 142-143. As also discussed in my analysis of Ground 3A, it would have been obvious to use Le's charge pump circuit to provide boosted voltages to Asano's memory devices. See ¶ 197. In the resultant circuit, each of Ujiie's diodes D1 and D2 would serve as a load of the charge pump circuit, with one terminal coupled to the output of the charge pump and the other terminal coupled to the drain of respective NMOS transistor Q1 and Q2. See ¶ 143.

222. In a similar context of regulating charge pump output voltage, Yang discloses a circuit with capacitors-loads C1-C11 coupled between the output of charge pump circuit 1 and the ground. See ¶ 219. I believe that, in view of Yang's teaching, a POSITA would have found it obvious that Ujiie's shunt regulator can be modified to use capacitors in lieu of diodes as loads. A POSITA thus would have been motivated to make the modification to the Asano-Le-Ujiie-Kuriyama combination, thereby rendering claim 18 obvious.

2. Claim 20: The memory system of claim 19, wherein each load is a capacitor having a first terminal and a second terminal, the first terminal being coupled to the source of the NMOS

transistor and the second terminal being coupled to an electrical ground.

223. I have previously discussed an obvious modification to Ujiie's shunt regulator, i.e., swapping the positions of each of diodes-loads D1 and D2 with respective NMOS switch Q1 and Q2. See ¶ 152. In the modified shunt regulator, the cathode (i.e., "first terminal" in the context of claim 20) of each diode-load is coupled to the source of the corresponding NMOS transistor and the anode of that diode-load is coupled to the ground. See ¶ 152.

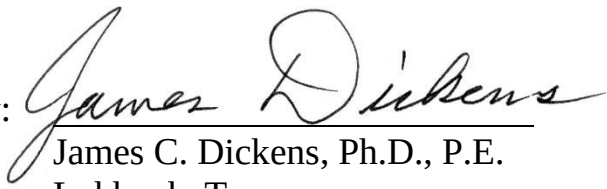
224. With the supplement of Yang, which teaches in a similar context using capacitors as loads, it would have been an obvious design choice to use Yang's capacitors-loads in lieu of Ujiie's diodes-loads D1 and D2 in the modified shunt regulator. A POSITA would have had a reasonable expectation of success for this modification, as the operation of the resulting circuit would have been predictable. The resultant circuit would read on claim 20.

XIV. Additional Remarks

225. I currently hold the opinions expressed in this declaration. But my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

226. I hereby declare that all statements made are of my own knowledge, are true and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this proceeding.

Dated: May 8, 2023

By: 
James C. Dickens, Ph.D., P.E.
Lubbock, Texas