

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Lorenzo Bedarida et al.
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Title: VARIABLE CHARGE PUMP CIRCUIT WITH DYNAMIC
LOAD

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**PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT
NO. 6,724,241 PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42**

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EXHIBITS

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EX-1002	Excerpts from the Prosecution History of the ’241 Patent
EX-1003	Declaration of Dr. James Dickens
EX-1004	Curriculum vitae of Dr. James Dickens
EX-1005	U.S. Patent No. 5,872,733 to Buti et al. (“Buti”)
EX-1006	U.S. Patent No. 4,769,784 to Doluca et al. (“Doluca”)
EX-1007	U.S. Patent No. 6,404,274 to Hosono et al. (“Hosono”)
EX-1008	U.S. Patent No. 6,424,570 to Le et al. (“Le”)
EX-1009	Japanese Patent Application No. S61-024094 to Ujiie et al. (“Ujiie”)
EX-1010	U.S. Patent No. 6,091,613 to Yang et al. (“Yang”)
EX-1011	U.S. Patent No. 6,373,325 to Kuriyama et al. (“Kuriyama”)
EX-1012	U.S. Patent No. 4,506,350 to Asano et al. (“Asano”)
EX-1013	District Court’s Claim Construction Order in <i>Sonrai Memory Limited v. Kioxia et al.</i> , Dkt. 55, W.D. Tex. 6:21-cv-00400-ADA
EX-1014	Webster’s Unabridged Dictionary, 2d ed. 2001 (excerpts)
EX-1015	McGraw-Hill Electronics Dictionary, 6th ed. 1997 (excerpts)
EX-1016	U.S. District Courts–Combined Civil and Criminal Federal Court Management Statistics (September 30, 2022), available at: https://www.uscourts.gov/sites/default/files/data_tables/cms_na_distprofile0930.2022.pdf
EX-1017	Geiger <i>et al.</i> , VLSI Design Techniques for Analog And Digital Circuits (1990), ISBN 0070232539 (excerpts)

- EX-1018 Plaintiff's Sur-Reply Claim Construction Brief in *Sonrai Memory Limited v. Apple Inc.*, Dkt. 48, W.D. Tex. 6:22-cv-00787-ADA
- EX-1019 Texas Instruments, *SNx4LS24x, SNx4S24x Octal Buffers and Line Drivers With 3-State Outputs* (Apr. 1985, rev. Oct. 2016)
- EX-1020 District Court's Claim Construction Order in *Sonrai Memory Limited v. Apple Inc.*, Dkt. 53, W.D. Tex. 6:22-cv-00787-ADA
- EX-1021 Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, Katherin K. Vidal (USPTO June 21, 2022) ("Interim Guidance")
- EX-1022 Stipulation

LISTING OF CHALLENGED CLAIMS

Claim 1	
[1pre]	A charge pump circuit for generating a charge pump voltage having minimal voltage ripples, comprising:
[1a]	a) a pumping circuit comprising one or more stages operable to receive a supply voltage and generate a selected one of a plurality of pump voltages;
[1b]	c) a plurality of loads selectively coupleable to an output of the pumping circuit, each load associated with a specific pump voltage; and
[1c]	c) a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit.
Claim 2	
[2]	The charge pump circuit of claim 1, wherein the load selector means includes a target output pump selector for shutting down the variable charge pump circuit when the target output pump voltage (V_{cfra}) is greater than or equal to a reference voltage (V_{ref}).
Claim 3	
[3]	The charge pump circuit of claim 2, wherein the load selector means further includes a maximum ripple on the target output selector means for adding a load, whenever a maximum ripple on the target output voltage (V_{cfrb}) greater than the reference voltage (V_{ref}) then the maximum ripple on the target output selector means adds additional loads until the V_{cfrb} voltage is less than or equal to the reference voltage (V_{ref}).
Claim 4	
[4a]	a) The charge pump circuit of claim 1, wherein the pumping circuit comprises: a) a plurality of diodes coupled in series, each diode having an input terminal and an output terminal, the input terminal of the first diode in the series is coupled to the supply voltage, the output of the first diode being connected to the input terminal of the second diode, and the output terminal of the last diode connected to the output pump;
[4b]	b) a plurality of capacitors having a first terminal and a second terminal, wherein the first terminal of the first capacitor being coupled to the output of a first diode and the input of a second diode, the first terminal of the second capacitor being coupled to the output of the second diode and the input of a third diode, and the first terminal of the last capacitor is coupled to the input terminal of a last diode;

[4c]	c) a plurality of inverters coupled in series to one another, each having an input terminal and an output terminal, the output of the first inverter being coupled to the second terminal of the first capacitor forming the first stage of the charge pump circuit, the second output of the second inverter coupled to the second terminal of the second capacitor forming the second stage of the charge pump circuit, and the output of the last inverter is coupled to the second terminal of the last capacitor forming the last stage of the charge pump circuit;
[4d]	d) a clock signal coupled to the input terminal of the first inverter.
Claim 5	
[5]	The variable charge pump circuit of claim 4, wherein each of the plurality of diodes is a diode-connected NMOS transistor, the gate of each transistor being connected to its drain forming the input terminal and its source forming the second terminal.
Claim 6	
[6]	The charge pump circuit of claim 1, wherein the load selector means is a plurality of switches, one switch for each of said loads, each switch having a first terminal, a second terminal, and an enable terminal, the switch being coupled in series with each load, the first terminal of the switch being coupled to the output pump and the second terminal of the switch is coupled to each load.
Claim 7	
[7]	The charge pump circuit of claim 1, wherein each load selector means comprises an NMOS transistor having a gate, a drain and a source, the gate of the NMOS load transistor being coupled to an enable signal, the source of the load NMOS load transistor being coupled to an electrical ground, and the drain being coupled to a load.
Claim 8	
[8]	The charge pump circuit of claim 7, wherein each load is a capacitor or a current sinker having a first terminal and a second terminal, the first terminal being coupled to the pump voltage and the second terminal being coupled to the drain of the NMOS transistor.
Claim 9	
[9]	The charge pump circuit of claim 1 wherein each load selector means comprises an elevator circuit having an input terminal and an output terminal, the input terminal being coupled to an enable signal, the output terminal being coupled to a load NMOS transistor, the gate of the load NMOS transistor being connected to the output terminal of

	the elevator circuit, the drain of the NMOS transistor being coupled to the pump output, and the source being coupled to the load.
Claim 10	
[10]	The charge pump circuit of claim 9, wherein each load is a capacitor or a current sinker having a first terminal and a second terminal, the first terminal being coupled to the source of the NMOS transistor and the second terminal being coupled to an electrical ground.
Claim 11	
[11a]	The charge pump circuit of claim 2 wherein the target output pump selector comprises: a) a first comparator having two input terminals, an output terminal and a first enable terminal, one of the two input terminals being connected to the reference voltage (Vref);
[11b]	b) a first resistor network having two terminals, the first terminal being coupled to the output pump, the second terminal being coupled to one of the input terminals of the first comparator;
[11c]	c) a second resistor network having two terminals, the first terminal being coupled to the second terminal of the first resistor network, and the second terminal of the second resistor network being coupled to an electrical ground
[11d]	d) a reference voltage source (Vref) coupled to one of the input terminals of the first comparator.
Claim 12	
[12a]	The charge pump circuit of claim 11, wherein the maximum overshoot on target output selector means comprises: a) a third resistor network having two terminals, the first terminal is coupled to the output pump;
[12b]	b) a fourth resistor network having two terminals, the first terminal is coupled to second terminal of the third resistor network, and the second terminal of the fourth resistor network being coupled to an electrical ground;
[12c]	c) a second comparator having two input terminal, an output terminal, and an enable terminal, one of the input terminals being coupled to the input terminal of the fourth resistor network and the other of the input terminals being coupled to the reference voltage Vref;
[12d]	d) a logic circuit having two terminals, the first terminal is coupled to the output terminal of the second comparator;
[12e]	e) a set load coupled to the pump output and being controlled by the logic circuit for adding an additional load to the output pump when the output pump has an overshoot greater than a maximum allowed on the output terminal.

Claim 13	
[13a]	A memory device, comprising: an address bus; a control circuit; a data bus; an address decoder coupled to the address bus; a read/write circuit coupled to the data bus; a memory cell array coupled to the address decoder, control circuit, and read/write circuit; and a charge pump circuit that generates a boosted output voltage with minimum ripples on an output node coupled to the address decoder, read/write circuit, and memory cell array, the charge pump circuit comprising:
[13b]	a) a pumping circuit comprising one or more stages operable to receive a supply voltage and generate one or more pump voltages;
[13c]	b) a plurality of loads, each load associated with a specific pump voltage and selectively coupleable to an output of the pump circuit (output pump);
[13d]	c) a load selector means coupled to the output pump for selecting a load that satisfies a specific pump voltage;
[13e]	d) a target output pump selector sampling the output of the pump circuit for shutting down the variable charge pump circuit whenever the sampled output voltage (vcfra) is greater than or equal to a reference voltage (Vref);
[13f]	e) a maximum ripple on target output selector means sampling the output of the pump circuit for adding a load, whenever a maximum ripple on sampled output voltage (Vcfrb) is greater or equal to than the reference voltage (Vref) then the output selector means adds additional loads until the Vcfrb voltage is less than the reference voltage (Vref).
Claim 14	
[14a]	A memory system of claim 13, wherein the pumping circuit comprises: a) a plurality of diodes coupled in series, each diode having an input terminal and an output terminal, the input terminal of the first diode in the series being coupled to the supply voltage, the output of the first diode being connected to the input terminal of the second diode, and the output terminal of the last diode connected to the output pump voltage;
[14b]	b) a plurality of capacitors having a first terminal and a second terminal, wherein the first terminal of the first capacitor being coupled to the output of the first diode, the first terminal of the second capacitor being coupled to the output of the second diode, and the first terminal of the last capacitor being coupled to the input terminal of the last diode;

[14c]	c) a plurality of inverter coupled in series to one another, each having an input terminal and an output terminal, the output of the first inverter being coupled to the second terminal of the first capacitor and the input of the second inverter forming the first stage of the charge pump circuit, the second output of the second inverter coupled to the second terminal of the second capacitor forming the second stage of the charge pump circuit, and the output of the last inverter being coupled to the input of the last diode;
[14d]	d) a clock signal coupled to the input terminal of the first inverter.
Claim 15	
[15]	The memory system of claim 13, wherein the plurality of diodes is a NMOS transistor connected as a diode, the gate of each transistor being connected to its drain forming the input terminal and the source forming the second terminal.
Claim 16	
[16]	The memory system of claim 13, wherein the load selector means is a switch having a first and a second terminal coupled in series with each load, the first terminal of the switch being coupled to the output pump and the second terminal of the switch is coupled to the load.
Claim 17	
[17]	The memory system of claim 13, wherein each load selector means comprises an NMOS transistor having a gate, a drain and a source, the gate of the NMOS load transistor being coupled to an enable signal, the source of the load NMOS load transistor being coupled to an electrical ground, and the drain being coupled to a load.
Claim 18	
[18]	The memory system of claim 17, wherein the load is a capacitor having a first terminal and a second terminal, the first terminal being coupled to the pump voltage and the second terminal being coupled to the drain of the NMOS transistor.
Claim 19	
[19]	The memory system of claim 13 wherein each load selector means comprises an elevator circuit having an input terminal and an output terminal, the input terminal being coupled to an enable signal, the output terminal being coupled to a load NMOS transistor, the gate of the load NMOS transistor being connected to the output terminal of the elevator circuit, the drain of the NMOS transistor being coupled to the pump output.
Claim 20	

[20]	The memory system of claim 19, wherein each load is a capacitor having a first terminal and a second terminal, the first terminal being coupled to the source of the NMOS transistor and the second terminal being coupled to an electrical ground.
Claim 21	
[21a]	The memory system of claim 13, wherein load selector means comprises: a) a first comparator having two input terminal, an output terminal and a first enable terminal, one of the two input terminals connected to the reference voltage (V_{ref});
[21b]	b) a first resistor network having two terminals, the first terminal being coupled to the output pump, the second terminal being coupled to the output terminal of the first comparator;
[21c]	c) a second resistor network having two terminals, the first terminal is coupled to the second terminal of the first resistor network, and the second terminal of the second resistor network being coupled to an electrical ground;
[21d]	d) a third resistor network having two terminals, the first terminal being coupled to the output pump;
[21e]	e) a fourth resistor network having two terminals, the first terminal being coupled to the second terminal of the third resistor network, the second terminal of the fourth resistor network being coupled to ground;
[21f]	f) a second comparator having two input terminals, and output terminal and an enable terminal, one of the input terminals being coupled to the input terminal of the fourth resistor network and the other of the input terminals being coupled to the reference voltage V_{ref} ;
[21g]	g) a logic circuit having two terminals, the first terminal coupled to the second comparator.
Claim 22	
[22a]	The memory system of claim 21, wherein the pumping circuit comprises: a) a plurality of capacitors or current sinkers having a first terminal and a second terminal, wherein the first terminal of the first capacitor being coupled to the output of the first diode, the first terminal of the second capacitor being coupled to the output of the second diode, and the first terminal of the last capacitor being coupled to the input terminal of the last diode;
[22b]	b) a plurality of inverter coupled in series to one another, each having an input terminal and an output terminal, the output of the first inverter

	being coupled to the second terminal of the first capacitor and the input of the second inverter forming the first stage of the charge pump circuit, the second output of the second inverter coupled to the second terminal of the second capacitor forming the second stage of the charge pump circuit, and the output of the last inverter being coupled to the input of the last diode; and
[22c]	c) a clock signal coupled to the input terminal of the first inverter.
Claim 23	
[23]	The memory system of claim 13, wherein the memory cell is a flash memory cell.
Claim 24	
[24pre]	A method for generating an output voltage with minimal ripples in a charge pump circuit, comprising:
[24a]	a) selecting a output pump voltage (V_{pump});
[24b]	b) turning on a load associated with the selected V_{pump} ; and
[24c]	c) comparing a target output voltage (V_{cfra}) with a reference voltage (V_{ref}) whenever the target output voltage greater than the reference voltage, disabling the charge pump circuit; whenever the target output voltage is less or equal to the voltage reference, leaving the charge pump circuit on.
Claim 25	
[25a]	The method of claim 24, further comprises the following steps: a) comparing a maximum acceptable ripple on output voltage value (V_{cfra}) with a reference voltage (V_{ref}) whenever the maximum acceptable ripple output voltage value is greater than the reference voltage, connecting a load until the V_{cfra} voltage value is less than or equal to the reference voltage;
[25b]	b) comparing a minimum acceptable drop on output voltage value (V_{cfrc}) with the reference voltage (V_{ref}), whenever the minimum acceptable drop on output voltage value is less than the reference voltage, removing a load until the V_{cfrc} voltage value is greater than the reference voltage.

Micron Technology, Inc. (“Petitioner” or “Micron”) petitions for *Inter Partes* Review (“IPR”) under 35 U.S.C. §§311–319 and 37 C.F.R. §42 of claims 1-25 (“the Challenged Claims”) of U.S. Patent 6,724,241 (“the ’241 Patent”). Petitioner respectfully requests institution of IPR and cancellation of the Challenged Claims as unpatentable.

I. REQUIREMENTS FOR IPR

A. Grounds for Standing

Petitioner certifies that the ’241 Patent is available for IPR and Petitioner is not barred from requesting review.

B. Challenge and Relief Requested

Petitioner requests IPR of the Challenged Claims on the grounds below and for the reasons set forth herein. Additional explanation and support are set forth in the accompanying Declaration of Dr. James Dickens. EX-1003, ¶¶1-226.

Ground	Claims	Pre-AIA §103 Basis
1A	1-3, 24, 25	Doluca (EX-1006) in view of Buti (EX-1005)
1B	4-5, 11-15, 21-23	Doluca, Buti and Hosono (EX-1007)
2A	1, 6-10	Le (EX-1008) in view of Ujiie (EX-1009)
2B	2, 3, 11, 24, 25	Le, Ujiie, and Kuriyama (EX-1011)
2C	4, 5	Le, Ujiie, and Hosono
3A	13-17, 19, 21-23	Asano (EX-1012) in view of Le, Ujiie, and Kuriyama
3B	18, 20	Asano, Le, Ujiie, Kuriyama, and Yang (EX-1010)

Each reference pre-dates October 25, 2002 (“Critical Date”), which is the date of filing of the priority foreign application of the ’241 Patent.¹

Reference	Date	Prior Art Under
Buti	February 16, 1999 (issued)	Pre-AIA § 102(b)
Doluca	September 6, 1988 (issued)	Pre-AIA § 102(b)
Hosono	June 11, 2002 (issued)	Pre-AIA § 102(a)
Le	July 23, 2002 (issued)	Pre-AIA § 102(a)
Ujiie	February 1, 1986 (published)	Pre-AIA § 102(b)
Yang	July 18, 2000 (issued)	Pre-AIA § 102(b)
Kuriyama	April 16, 2002 (issued)	Pre-AIA § 102(a)
Asano	March 19, 1985 (issued)	Pre-AIA § 102(b)

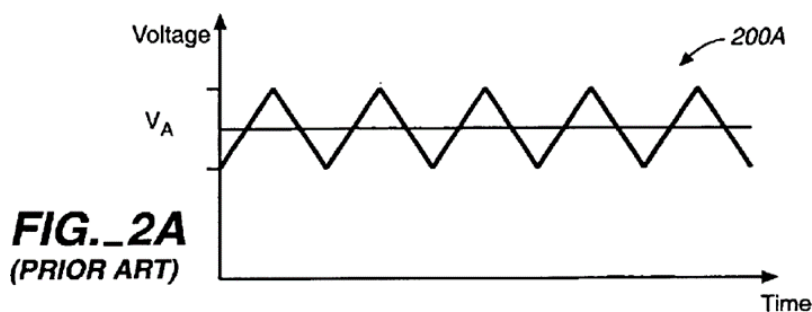
¹ Petitioner does not concede the ’241 Patent is entitled to claim priority to the Critical Date.

II. THE '241 PATENT

A. Brief Description

The '241 Patent relates to charge pumps. EX-1001, Title and Abstract; EX-1003, ¶33. Charge pumps were well-known in the prior art to generate voltages higher than the voltage of the available power source. EX-1001, 1:15-17. For example, a charge pump might generate output voltages of 10V or 15V using a voltage supply of 5V. Such voltages were used to perform program and erase operations in non-volatile memory devices. EX-1001, 1:12-15; EX-1003, ¶34.

The '241 Patent notes that it was a known problem that charge pumps sometimes generate output voltage containing a voltage ripple (e.g., as depicted in FIG. 2A) due to differences in the capacitances of the charge pump and the load (e.g., memory device) being driven by the charge pump. EX-1001, 2:3-15; EX-1003, ¶35.



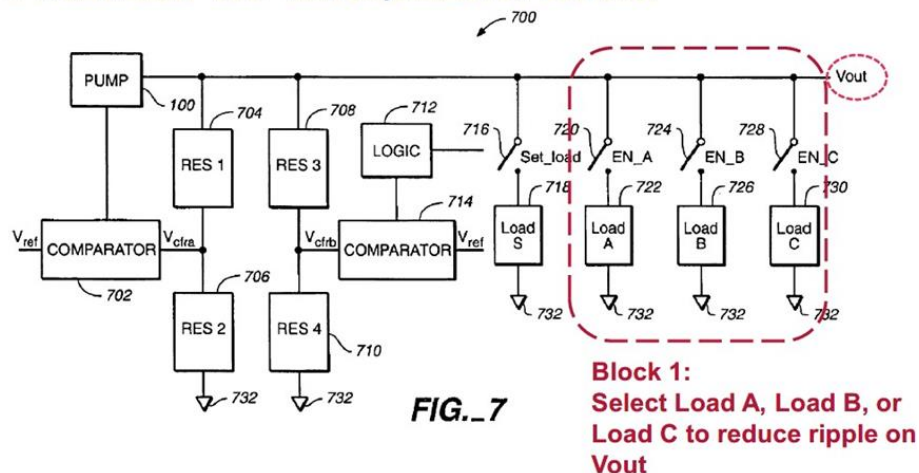
EX-1001, FIG. 2A

As the '241 Patent admits, there were known techniques for minimizing the

voltage ripple. EX-1001, 2:46-67. The patent discloses a particular technique for minimizing the voltage ripple. EX-1001, Abstract.

The disclosed technique comprises three circuit blocks shown in FIG. 7 (reproduced below) that are attached to the output, V_{out} , of a charge pump to minimize the voltage ripple. EX-1001, 5:54-6:17. The first block (annotated “Block 1”) contains selectable loads, each of which is associated with a voltage level and is attached to V_{out} when that voltage level is desired. EX-1001, 4:33-5:21; EX-1003, ¶¶36-37.

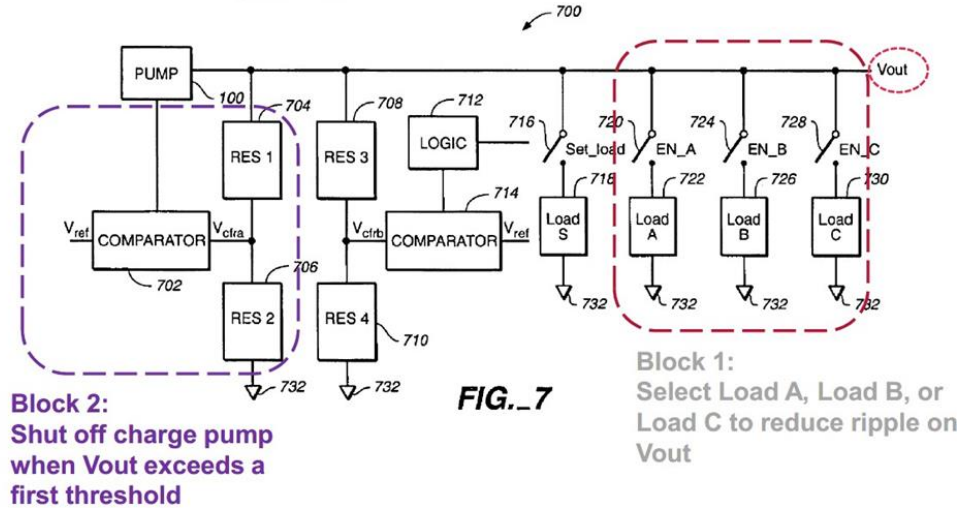
Block 1: Add an extra “load” that is optimized for V_{out} level



EX-1001, FIG. 7 (annotated)

The second block (“Block 2”) shuts off the charge pump if the output exceeds a certain level. EX-1001, 6:9-17; EX-1003, ¶38.

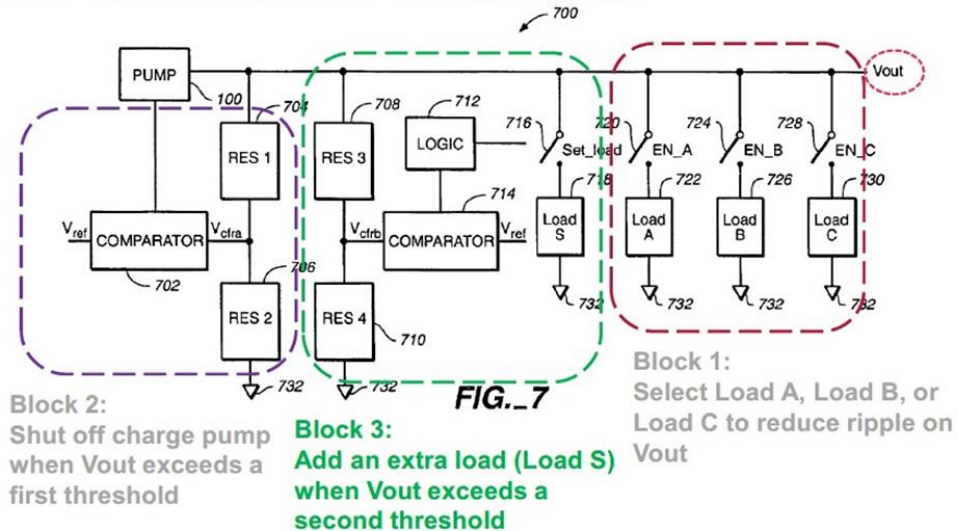
Block 2: Turn off charge pump when Vout exceeds certain level



EX-1001, FIG. 7 (annotated)

The third block (“Block 3”) adds an extra or additional load if the output reaches a maximum acceptable voltage level. EX-1001, 6:4-8; EX-1003, ¶39.

Block 3: Add an additional “load” if Vout gets too high



EX-1001, FIG. 7 (annotated)

The Challenged Claims are directed to either Block 1 alone, Blocks 1-2, or

Blocks 1-3. As demonstrated below, the disclosed technique, including the three blocks, were known in the prior art, and all Challenged Claims are obvious. EX-1003, ¶¶39-40.

B. Summary of the Prosecution History

U.S. Application 10/352,733, which resulted in the '241 Patent, was filed on January 27, 2003, with a foreign application priority date of October 25, 2002. EX-1002, 1-3, 43-45, 113. There were no rejections of the claims and the application was allowed in a first action on December 19, 2003. *Id.*, 1-3, 103-113. EX-1003, ¶¶41-43.

C. Level of Ordinary Skill in the Art

A POSITA as of the Critical Date would have had a Bachelor's degree in electrical engineering or a related field and 2-3 years of experience working with electronic circuits or systems, or equivalent. EX-1003, ¶11-13.

D. Claim Construction

Petitioner proposes the following constructions.

1. “load” (claims 1, 13)

A POSITA would have understood that the term “load” has two possible constructions as used in the '241 Patent. EX-1003, ¶45.

Under a broader construction, a “load” is “a device that receives electrical

power.” For example, the specification states that a load “can” be a capacitor or a “current sinker,” which are known electrical circuit components that receive electrical power. EX-1001, 4:34-35; EX-1003, ¶46. This construction is supported by dictionaries. *See, e.g.*, EX-1014 (Webster’s Unabridged Dictionary) (2d ed. 2001) (“*Elect.* . . . “a device that receives power”); EX-1015 (McGraw-Hill Electronics Dictionary) (6th ed. 1997) (“A device that consumes electric power”). EX-1003, ¶46.

Under a narrower construction, a “load” is “a device that absorbs surplus charge to reduce voltage ripple when compared to a case without the device.” *Id.*, ¶47. The specification explains that a load “can” be a capacitor or a “current sinker,” which is a device that absorbs surplus charge to produce a minimum voltage ripple. *See, e.g.*, EX-1001 at Abstract (describing that the pump circuit “uses a plurality of selectable loads to minimize the voltage ripples of the pumped output by selecting the appropriate load for a preselected pump voltage”); *see also* 4:5-8, 4:64-65, 9:20-24 (claim 8), 9:34-38 (claim 10); and EX-1003, ¶47.

The claims are unpatentable under either construction.

2. “a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit” (claim 1)

This is a means-plus-function limitation. The **function** is “selectively

coupling a load associated with a specific pump voltage to the output of said pumping circuit,” which should be construed as “choosing a load based on the target pump voltage, such that the load is coupled to the output of the pumping circuit when the target pump voltage is selected.” EX-1003, ¶49.

The '241 Patent explains that each load (e.g., Load A, B, or C) is “associated” with a specific pump voltage and that the load is attached to the output when that specific pump voltage is selected. EX-1001, 4:33-51. The attachment of the load is triggered by the pump voltage selection, not a later event. EX-1001, 4:33- 51, 7:7-16, 7:31-42. In contrast, a different load (e.g., Load S) can be added if needed based on a measurement of the output voltage; that load is not described as being “associated” with the particular output voltage because it is not added at the time of the target pump voltage selection. EX-1001, 6:8-17, 7:7-16, 7:31-42; EX-1003, ¶50.

The **structure** disclosed for performing this function is: switches 320, 324, and 328 and their control signals EN_A, EN_B, and EN_C. For example, the specification states that the “three switches 320, 324, and 328 together with their respective control signals EN_A, EN_B and EN_C form a load selector means that reduce voltage ripple at the charge pump output to a minimum.” EX-1001,

4:47-50; *see also id.*, FIG. 3, 4:2-8, 4:52-5:15; EX-1003, ¶51.² Additionally, Fig. 5A and Fig. 5B of the '241 Patent illustrate structural embodiments for switches 320, 324, and 328 and indicate that the switches can be transistors. EX-1003, ¶51. Accordingly, transistors can also be appropriate structure for this limitation. *Id.*

The Board also might determine that the corresponding structure further includes structure that generates these control signals. That structure includes a “controller” that generates control signals EN_A, EN_B, and EN_C. EX-1001, 4:51-61. Under this construction, the **structure** would be: switches 320, 324, and 328 and their control signals EN_A, EN_B, and EN_C and a controller for generating those control signals. EX-1003, ¶52.

The prior art satisfies this limitation as to all of these possible structures.³

² Petitioner reserves the right to challenge this limitation, and others, in district court under §§101 and 112, including with respect to the inclusion of signals as structural limitations and regarding claims containing both apparatus and method limitations.

³ If Patent Owner (“PO”) argues, and the Board agrees, that the functions recited in claims 2 and 3 must be performed by the “load selector means” of claim 1, then the

3. “target output pump selector for shutting down the variable charge pump circuit when the target output pump voltage (V_{cfra}) is greater than or equal to a reference voltage (V_{ref})” (claim 2) and “a target output pump selector sampling the output of the pump circuit for shutting down the variable charge pump circuit whenever the sampled output voltage (v_{cfra}) is greater than or equal to a reference voltage (V_{ref})” (claim 13)

These limitations are means-plus-function limitations, as evidenced by claims 3, 12 and 13 referring to these limitations as the “target output selector means.” EX-1001, claims 3, 12 and 13. The recited **function** of each is “shutting down the variable charge pump circuit when the target output pump voltage (V_{cfra}) is greater than or equal to a reference voltage (V_{ref})” (claim 2) and “sampling the output of the pump circuit for shutting down the variable charge pump circuit whenever the sampled output voltage (v_{cfra}) is greater than or equal to a reference voltage (V_{ref})” (claim 13). The disclosed **structure** for both

load selector means would further include as structure resistor 704, resistor 706, and comparator 702 for the function of claim 2 and resistor 708, resistor 710, comparator 714, and logic 712 for the function of claim 3. Under this construction, claim 1 would be obvious for the reasons expressed for claims 2 and 3 in Grounds 1A and 2A-2B. EX-1003, ¶52.

functions is: comparator 702. EX-1001, 5:54-6:8; EX-1003, ¶¶53-55.

4. “a load selector means coupled to the output pump for selecting a load that satisfies a specific pump voltage” (claim 13)

This is a means-plus-function limitation. The **function** is “selecting a load that satisfies a specific pump voltage.” EX-1001, claim 13; EX-1003, ¶¶56-57. To the extent that this function is found to mean “selectively coupling a load associated with a specific pump voltage” or similar as recited in claim 1, the **structure** identified above for claim 1 is the structure for the “load selector means” of claim 13.⁴ EX-1003, ¶58.

III. THE CHALLENGED CLAIMS ARE UNPATENTABLE

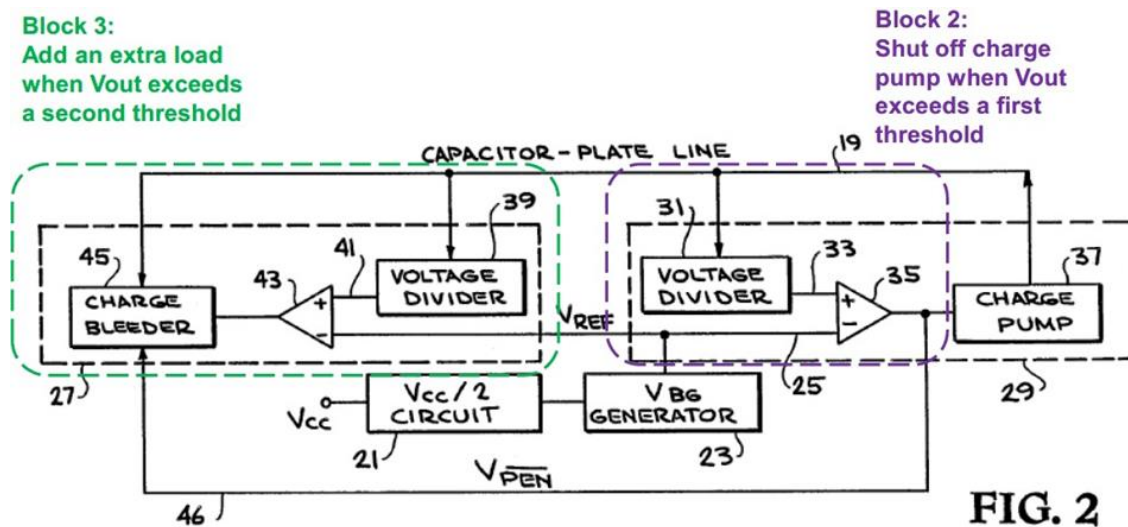
A. GROUND 1A: Claims 1-3, 24, and 25 are rendered obvious by Doluca and Buti

1. Overview of Doluca

Dolucas discloses a capacitor-plate bias circuit with a charge pump for supplying voltage to memory devices. EX-1006, 1:1-12, 1:64-2:39. The bias circuit generates a desired output voltage that is regulated using a charge bleeder. *Id.*, Abstract. The charge pump can be disabled by a control circuit (“Block 2” in

⁴ Petitioner reserves the right to challenge this limitation and others as noted throughout this Petition, as indefinite in district court litigation.

Doluca’s FIG. 2, reproduced below) if the output voltage exceeds a threshold voltage. *Id.*, 4:18-53, FIG. 2. The bias circuit includes a charge bleeder circuit (“Block 3” in FIG. 2) that can adjust the pump output voltage. *Id.*, 4:54-5:8; EX-1003, ¶¶60-62.



EX-1006, FIG. 2 (annotated)

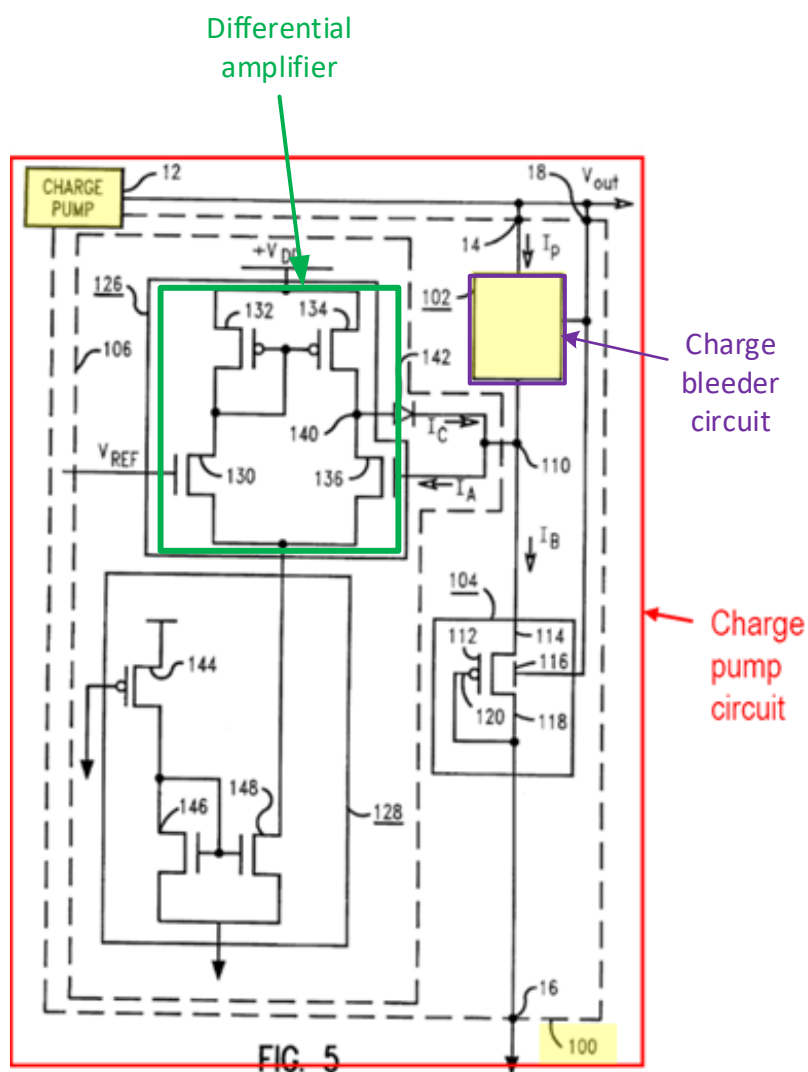
2. Overview of Buti

Buti discloses a charge pump circuit having a ramp-up rate control circuit to control the ramp-up rate of a charge pump output voltage V_{out} applied to memory devices. EX-1005, Title, Abstract; 1:5-4:15, 4:61-5:26, FIG. 1A. Recognizing a problem with high ramp-up rate, Buti prevents V_{out} from ramping up too rapidly by using a current bleeder circuit coupled to the pump output to regulate current flow between the pump output and the ground potential based on the magnitude of V_{out} .

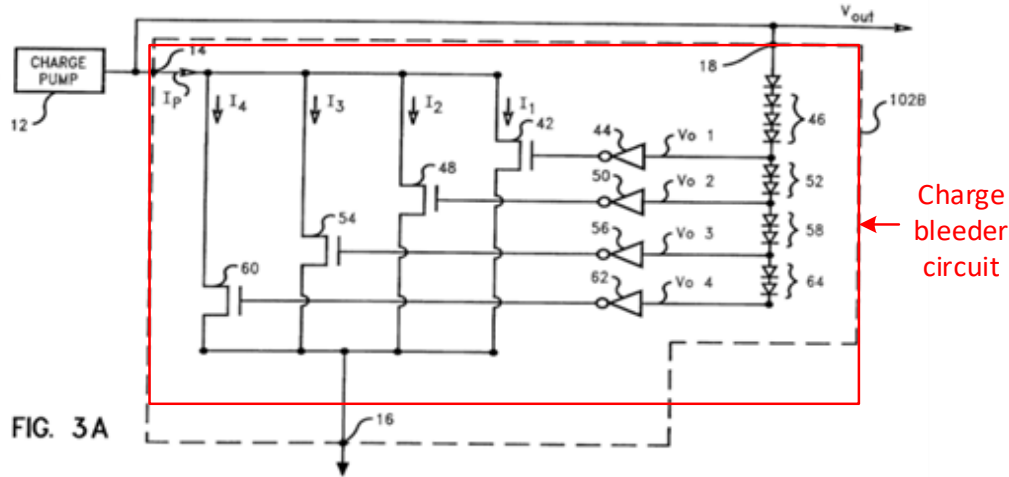
Id.; see also *id.*, 5:27-9:28; FIGs. 1B-6. Buti teaches using multiple bleeding paths to “effect accurate control of bleeding current ... for varying magnitudes of $[V_{out}]$.” *Id.*, 6:59-66; FIG. 3A. Each bleeding path is controlled using a chain of diodes coupled with an inverter and an n-channel field-effect transistor (FET), and is associated with a threshold voltage for turning the path on/off. *Id.*, 6:56-7:58; FIG. 3A. See also EX-1003, ¶¶64-68.

A POSITA would have found it obvious to combine Buti and Doluca, for at least the following reasons. Doluca discloses a charge pump circuit to supply voltages to memory devices. See *supra* §III.A.1. Doluca explains that, if the voltage output by its charge pump circuit exceeds a target threshold value, the output voltage is lowered by bleeding the charge using a bleeder control circuit 27. EX-1006, 4:10-30, 4:53-5:8. While disclosing that the bleeder control circuit 27 lowers the output voltage using charge bleeder 45, Doluca does not provide further structural or functional description of the charge bleeder. *Id.* A POSITA who, upon reviewing Doluca’s disclosure, wanted to know more about the bleeder 45 circuitry, and/or how it functions to lower the output voltage, would have looked at other sources for relevant information. EX-1003, ¶¶69-70. In doing so, a POSITA would have been motivated to consider references that describe bleeder circuits in the context of memory device charge pumps. *Id.* Buti is one such reference that

provides an example of a bleeder structure and operational details by describing use of a charge pump circuit to supply voltages to memory devices and, like Doluca, discloses the use of a bleeder circuit to regulate the charge pump output voltage. EX-1005, Title, Abstract, 1:5-4:15, 4:61-9:28, FIGS. 3A, 5 (reproduced below). Buti's charge pump circuit (in FIG. 5) includes charge pump 12 and charge bleeder circuit 102, with the latter having a structure shown by circuit 102B in FIG. 3A. *Id.* Bleeder circuit 102B includes (i) FETs 42, 48, 54, and 60, which each can be selectively coupled to output V_{out} of charge pump 12 at node 14, depending on V_{out} level to regulate the pump output voltage, and (ii) series diodes ("diode stacks") 46, 52, 58, and 64 that control activation/deactivation of the FETs depending on whether V_{out} exceeds a respective threshold voltage. EX-1005, 6:56-7:58, FIG. 3A. EX-1003, ¶¶68, 71.



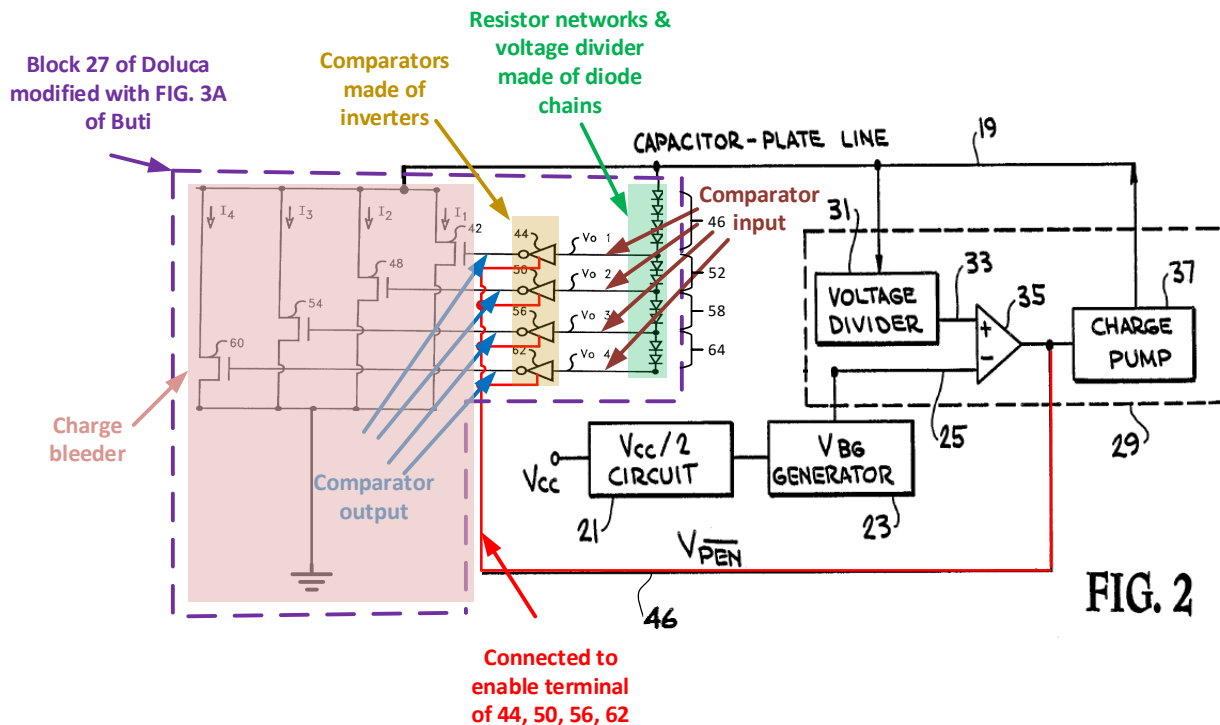
EX-1005, FIG. 5 (annotated)



EX-1005, FIG. 3A (annotated)

A POSITA would have understood that Buti's bleeder circuit can be used as the charge bleeder 45 in Doluca's bleeder control circuit 27 to regulate Doluca's pump output voltage as a matter of design choice. EX-1003, ¶¶72-73; *see also* §III.A.3.(c), *infra*. A version of Doluca's bias generator circuit, modified in view of Buti's bleeder circuit 102/102B as would have been understood by a POSITA, is shown below. EX-1003, ¶72. As illustrated, in the modified circuit, Buti's transistors 42, 48, 54, 60 form the charge bleeder 45; diode stacks 46, 52, 58, 64 perform the operations of voltage divider 39; and inverters 44, 50, 56, 62 perform the operations of comparator 43. *Id.*, ¶¶72-76. A POSITA would have also found it obvious to alternatively replace the inverters with operational amplifier (op-amp)-based, two-input comparators. *Id.*, ¶77. A POSITA would have had a

reasonable expectation of success for these modifications, as these techniques were known and the operation of the resulting circuit would have been predictable. *Id.* Accordingly, a POSITA would have been motivated to combine Doluca and Buti. *Id.*, ¶¶72-78; see also *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373 (Fed. Cir. 2023) (finding that “[i]t’s enough” for petitioner to show that there was a known problem addressed by the references and that “combining the teachings of [the prior art] wasn’t beyond the skill of an ordinary artisan.”) (citing *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 127 S. Ct. 1727, 167 L. Ed. 2d 705 (2007))).



EX-1006, FIG. 2 (modified in view of EX-1005, FIG. 3, annotated)

3. Claim 1

a) [1pre]

To the extent the preamble is limiting,⁵ Doluca discloses a charge pump circuit by describing a bias circuit that includes charge pump 37. *See, e.g.*, EX-1006, Abstract, 3:26-4:30, FIGS. 2-3; *see also id.* 1:64-2:39. Charge pump 37 generates voltage V_{CP} on capacitor-plate line 19. *Id.*; EX-1003, ¶80.

To generate a “stable” V_{CP} , Doluca describes using its bias circuit to generate a voltage that “remain[s] within a narrow range around a design voltage.” EX-1006, 2:13-39, 1:29-38. A POSITA would have understood that Doluca’s teaching of generating a “stable” voltage within a “narrow range” of a target (design) voltage reads on “generating a charge pump voltage having minimal voltage ripples.” EX-1003, ¶81.

b) [1a]

Doluca’s bias circuit of FIG. 2 includes charge pump 37, which generates

⁵ Petitioner reserves the right to argue in counterpart litigation that the preamble is not limiting. Indeed, in a related litigation, PO argued, and the court accepted, that “for generating a charge pump voltage having minimal voltage ripples” is not limiting. EX-1013, 3; *see also* EX-1018, 1-2.

output pump voltage V_{CP} . *Supra* §§III.A.1, III.A.3.(a). Charge pump 37 has two stages with respective capacitors C1 and C2, which receive source voltage V_{CC} as the supply voltage and generate V_{CP} . EX-1006, 5:19-54, FIG. 3 (reproduced below); EX-1003, ¶82.

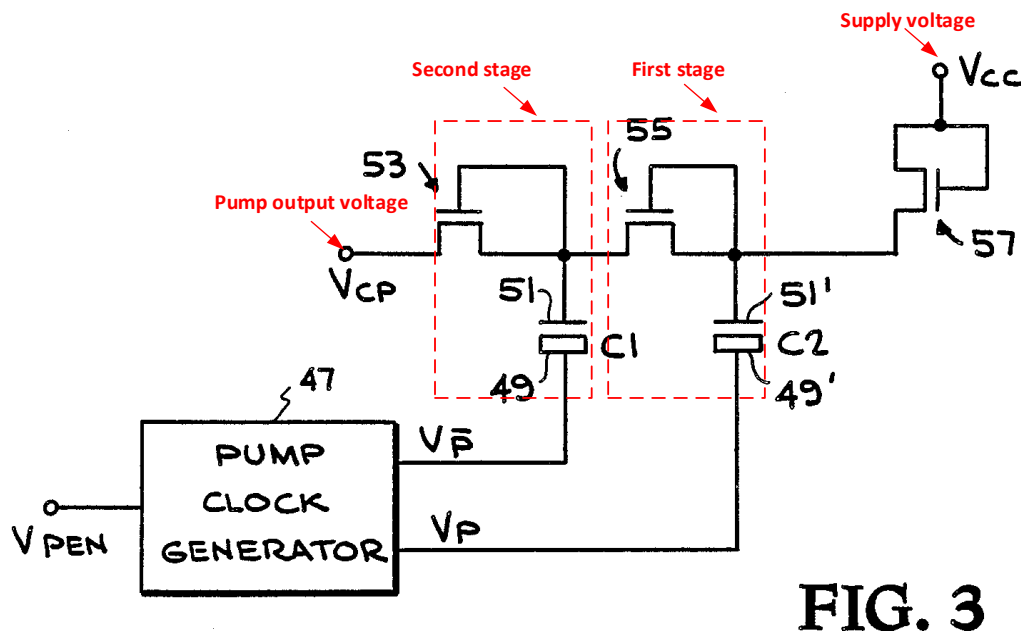


FIG. 3

EX-1006, FIG. 3 (annotated)

Doluca discloses that charge pump 37 is operated to provide V_{CP} within a range depending on the value of K, which can be “chosen” to be within a specified range. EX-1006, 3:31-54. This selection of K enables “the use of V_{CC} volts as the logic 1 voltage and 0 volts as the logic 0 voltage,” with charge pump 37 and a charge bleeder together regulating V_{CP} between upper and lower limits. *Id.*, 2:21-39, 4:10-5:18. A POSITA would have found it obvious that, by choosing the value

of K and accordingly that of V_{CP} , Doluca's charge pump can "generate a selected one of a plurality of pump voltages." EX-1003, ¶83.

Additionally, in Doluca's FIG. 2 circuit as modified by Buti's FIG. 3 (*supra* §III.A.2), the pump voltage on line 19 is regulated according to the threshold voltages of the series diodes (marked in green), which Buti teaches can be modified according to "desired operating characteristics." EX-1005, 6:55-7:11. A POSITA accordingly would have found it obvious that the desired pump voltage can be selected by modifying the numbers of diodes in each diode stack. EX-1003, 84.

c) [1b]

As shown in FIG. 2, *supra* §III.A.1, Doluca's bias circuit includes bleeder control circuit 27 and pump control circuit 29 to control the voltage on line 19 (i.e., output voltage V_{CP} of charge pump 37) by a) comparing a fraction of V_{CP} with V_{REF} and b) turning on/off charge bleeder 45 or charge pump 37 in response to the comparison. EX-1006, 3:54-5:20. Doluca describes charge bleeder 45 is activated to adjust V_{CP} when a threshold value is reached. *Id.*, 3:54-5:20, 2:21-39, FIG. 2; EX-1003, ¶85.

Although describing the use of charge bleeder 45 to regulate V_{CP} , Doluca does not detail the specific structure of charge bleeder 45 or specific techniques

used to adjust V_{CP} . As noted previously, a POSITA would have found it obvious to use Buti's bleeder circuit in Doluca's bias circuit. *See supra* §III.A.2. A POSITA would have readily understood that FETs 42, 48, 54, and 60 in Buti's bleeder circuit, and in Doluca's modified bias circuit, are analogous to loads and that these FETs may be turned on/off to regulate V_{out}/V_{CP} , depending on the output voltage range. EX-1005, 6:56-7:58, FIG. 3A; EX-1003, ¶86. Describing the operation of the bleeder circuit as disclosed in Buti with FET 42 as an example, a POSITA would have understood that, when V_{out} exceeds the threshold voltage (e.g., 5.78 volts) of the diode stack 46, these diodes are forward biased such that the input of inverter 44 is logic "1," causing the gate of FET 42 to have a voltage with logic "0," which turns off FET 42 and prevents flow of current I_1 , i.e., the FET is deselected. EX-1005, 7:12-24; *see also id.*, 8:3-23. The other FETs are similarly associated with respective threshold values of V_{out} and can be selected/deselected depending on the value of V_{out} compared to the threshold voltage. *Id.*, 7:25-58, Table 1. EX-1003, ¶86.

d) [1c]

Dolucas discloses bleeder control circuit 27 and pump control circuit 29 that turn on/off charge bleeder 45 or charge pump 37, respectively, to control output voltage V_{CP} . *See supra* §III.A.3.(c). A POSITA would have understood that

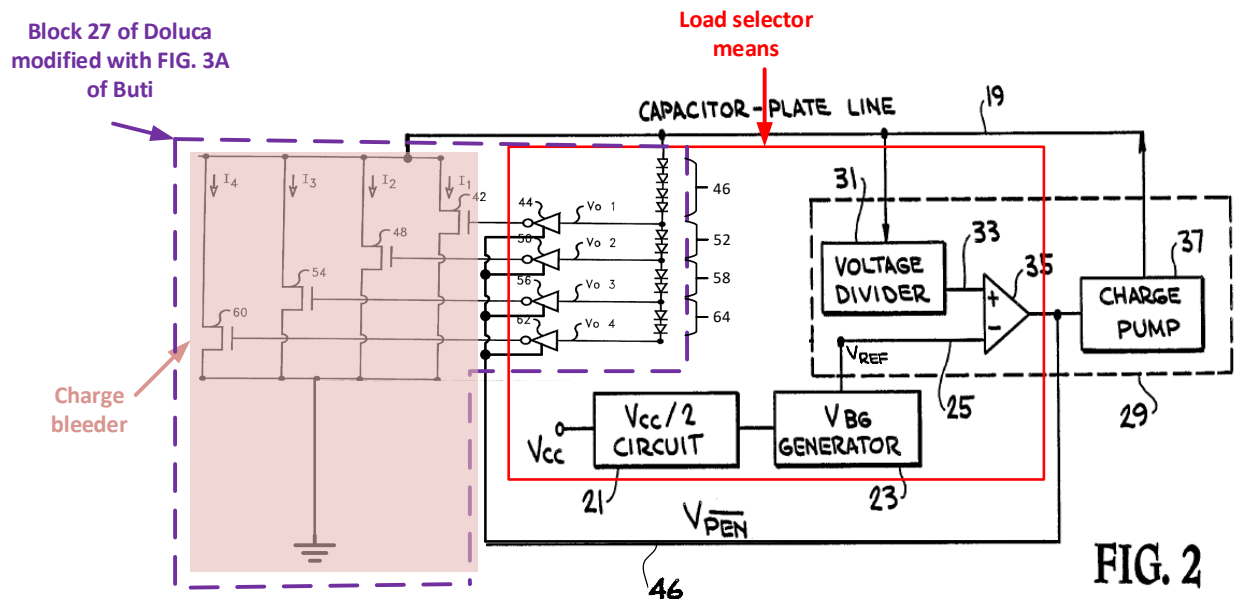
bleeder control circuit 27 and pump control circuit 29 are both part of a “load selector means” for Doluca’s charge pump circuit.⁶ EX-1003, ¶87.

Buti provides the structure and operational details of a bleeder control circuit that can be used as Doluca’s bleeder control circuit 27. *See supra* §III.A.3.(c). For example, Buti discloses that bleeder circuit 102B uses series diodes 46, 52, 58, and 64, along with inverters 44, 50, 56, and 62, to control (i.e., select/deselect) different subsets of FETs 42, 48, 54, and 60 (“loads” in Buti’s bleeder circuit) depending on the range of V_{out} . EX-1005, 6:56-7:11, FIG. 3A (reproduced below); *supra* §III.A.3.(c); EX-1003, ¶¶85-86. A POSITA would have understood that series diodes 46, 52, 58, and 64, and inverters 44, 50, 56, and 62, together form a “load selector means” for FETs 42, 48, 54, and 60, and are a part of the load selector means that comprises bleeder control circuit 27 and pump control circuit 29 in Doluca’s charge pump circuit, modified to include Buti’s bleeder circuit 102/102B. EX-1003, ¶87; *supra* §III.A.2.

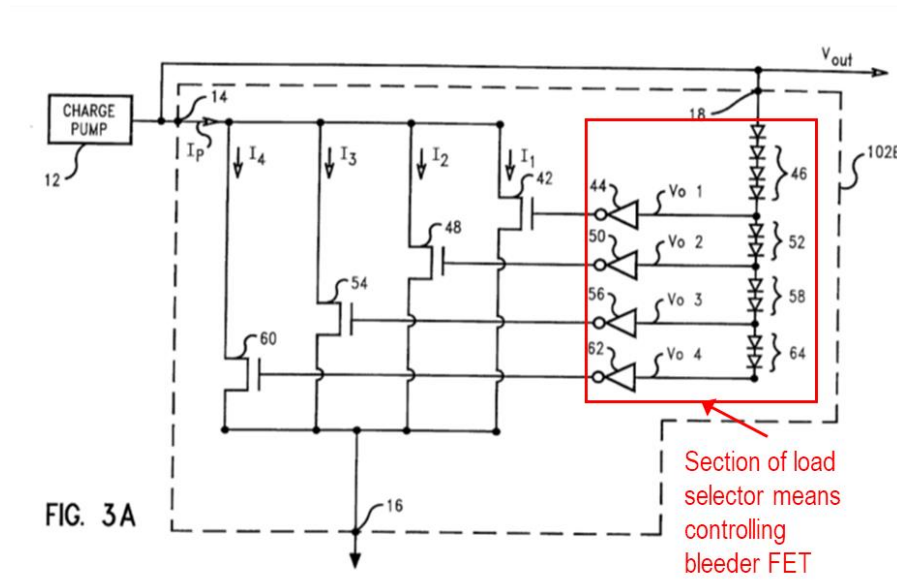
The combination of Doluca and Buti discloses performing the recited

⁶ This is consistent with the interpretation in a related litigation, in which the court interpreted “load selector means” as covering both comparators 702 and 714 in ’241 Patent FIG. 7. EX-1020, 3-4.

function of [1c]. Specifically, when V_{out} exceeds a particular threshold voltage (e.g., $5.78 \text{ volts} < V_{out} < 7.60 \text{ volts}$), series diodes 46 and inverter 44 together control the voltage supplied to the gate of FET 42, turning off current flow through the FET 42, while enabling current flow through FETs 48, 54 and 60. *See supra* §III.A.3.(c). A POSITA would have understood that, in doing so, series diodes 46, 52, 58, and 64, and inverters 44, 50, 56, and 62 selectively couple/decouple the FETs to the charge pump output. EX-1003, ¶87. In a similar manner, series diodes 46 and 52 and inverter 50 selectively couple FET 48 to the charge pump output depending on a specific threshold voltage range. EX-1005, 7:25-31. FETs 54 and 60 are similarly selectively coupled using series diodes 46-64 and inverters 56 and 62. *Id.*, 7:32-46. EX-1003, ¶87.



EX-1006, FIG. 2 (modified in view of EX-1005, FIG. 3, annotated)

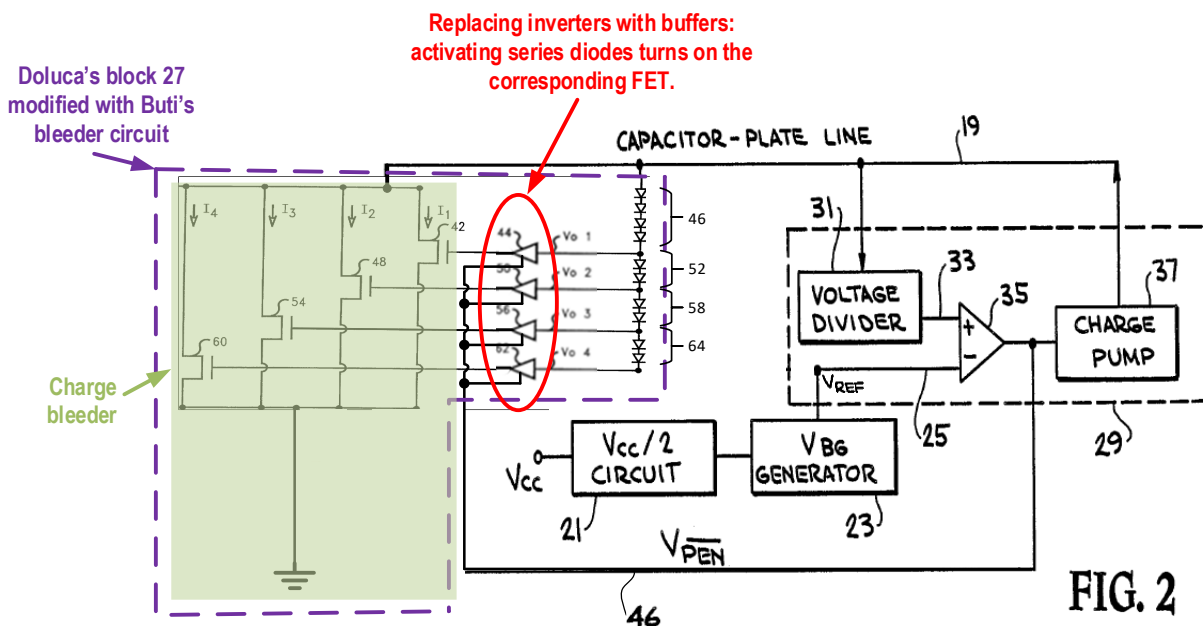


EX-1005, FIG. 3A (annotated)

To the extent the Board requires that “selectively coupling a load” requires enabling current to flow through the load, the Doluca-Buti circuit renders obvious the recited function of claim 1. Consistent with Doluca’s teaching of regulating pump voltages, a POSITA would have found it obvious to modify Buti’s bleeder circuit by replacing the Buti’s inverters with buffers, e.g., as illustrated below, such that increasing the pump output voltage (V_{CP}) from one voltage range to the next range triggers the series diodes to selectively turn on the FETs to enable bleeding current flow, resulting in a reduction of the output voltage. EX-1003, ¶¶88-91. A POSITA would have had a reasonable expectation of success, as such modification

would have been a combination of known techniques yielding predictable results.

Id. A POSITA would have readily understood that various alternative obvious modifications can be made to Buti's bleeder circuit—for example, replace inverters (or buffers) with op-amp-based comparators, or replace the NMOS FETs with PMOS FETs—to arrive at the same result. *Id.*



EX-1006, FIG. 2 (modified in view of EX-1005, FIG. 3, annotated)

4. Claim 2⁷

The “load selector means” in Doluca-Buti's charge pump circuit includes

⁷ See n.4.

voltage divider 31 and comparator 35 of pump control circuit 29. *See supra* §III.A.3.(d); EX-1003, ¶¶87-92.

Pump control circuit 29 “derive[s] a voltage which is a certain fraction of the voltage on line 19,” “compare[s] this voltage with the V_{REF} voltage” and “turn[s] the charge pump[] on or off in response to the difference between the two voltages.” EX-1006, 3:55-4:52, FIG. 2. Specifically, based on comparator 35 output, the charge pump is turned on when $V_{33} \leq V_{REF}$, where V_{33} equals a fraction of output voltage V_{CP} and V_{REF} is the reference voltage. *Id.*, 3:55-4:52, 6:64-7:23, FIG. 6; EX-1003, ¶92. Based on this teaching of Doluca, a POSITA would have readily understood that the charge pump is turned off or shut down when $V_{33} > V_{REF}$, which renders claim 2 obvious. EX-1003, ¶92.

5. Claim 3

The “load selector means” in Doluca-Buti’s charge pump circuit includes voltage divider 39 (formed by Buti’s diode stacks) and comparator 43 (formed by Buti’s inverters, or buffers in lieu thereof) of bleeder control circuit 27. *See supra* §III.A.3.(d); EX-1003, ¶¶87-93.

Dolucas discloses bleeder control circuit 27 activates charge bleeder circuit 45 to reduce the pump output voltage V_{CP} on capacitor-plate line 19 when V_{CP} exceeds an upper limit. EX-1006, 2:27-33, FIG. 2; EX-1003, ¶93. A POSITA

would have understood that activating charge bleeder circuit 45 would increase the bleeding current from capacitor-plate line 19 to ground, thereby reducing V_{CP} .

EX-1003, ¶93.

Buti provides greater detail how the pump output voltage can be reduced by controlling loads when a threshold is crossed. For example, Buti teaches that one or more of FETs 42, 48, 54, and 60 can be selectively turned off to control the current flowing through bleeder paths I_1 - I_4 when V_{CP} (V_{out}) increases from a lower to a higher voltage range. *See supra* §III.A.3.(d).

A POSITA also would have found it obvious to modify Buti's bleeder circuit in the Doluca-Buti combination, replacing the inverters with buffers, such that increasing V_{CP} causes FETs to turn on (adding "loads") selectively, causing a reduction of the output voltage. *See supra* §III.A.3.(d); EX-1003, ¶93.

6. Claim 24

a) [24pre]

To the extent the preamble is limiting,⁸ Doluca teaches a method that uses a charge pump to generate a stable output voltage within a narrow range around a design voltage (i.e., "with minimal ripples"). *See supra* §III.A.3.(a); EX-1003,

⁸ *See* n.5.

¶94.

b) [24a]

Doluca's charge pump generates voltage V_{CP} to equal $V_{CC}/2 + K$, where K is a constant chosen to have a value greater than $V_{CC}/2 + V_T$. EX-1006, 3:31-54; EX-1003, ¶83. For each chosen value of K , there is a resultant value of V_{CP} . EX-1006, 3:47-51. To maintain V_{CP} at or near $V_{CC}/2 + K$, Doluca compares a fraction of V_{CP} with reference voltage V_{REF} and controls bleeder control circuit 27 and pump control circuit 29 based on the comparison. *See supra* §III.A.3.(c). A POSITA would have understood that selecting a particular value of K corresponds to selecting a particular output pump voltage (V_{CP}). EX-1003, ¶94. A POSITA would have found it obvious to compare V_{CP} (rather than V_{33}) with reference voltage V_{REF} to determine whether to disable the charge pump or leave it on. *Id.*, ¶¶92, 94.

c) [24b]

With the understanding that “turning on a load” means coupling a load to the pump output, the Doluca-Buti combination teaches this limitation. *See supra*. §III.A.3.(d); EX-1003, ¶94.

d) [24c]

The Doluca-Buti combination renders this limitation obvious. *See supra*

§III.A.4; EX-1003, ¶¶94-95.

7. Claim 25

a) [25a]⁹

The Doluca-Buti combination renders this limitation obvious. *See supra* §III.A.5; EX-1003, ¶96.

b) [25b]

Because a POSITA reading Doluca and Buti would have found it obvious to add a load to decrease the pump output, *see supra* §III.A.5, a POSITA would also have found it obvious to remove a load (opposite to adding a load) to increase the pump output. Thus, when the pump output is lower than a desired level, a POSITA would have had the motivation to remove loads until the pump output reaches the desired level. EX-1003, ¶97.

B. Ground 1B: Claims 4-5, 11-15, 21-23 are obvious based on Doluca, Buti, and Hosono

1. Overview of Hosono

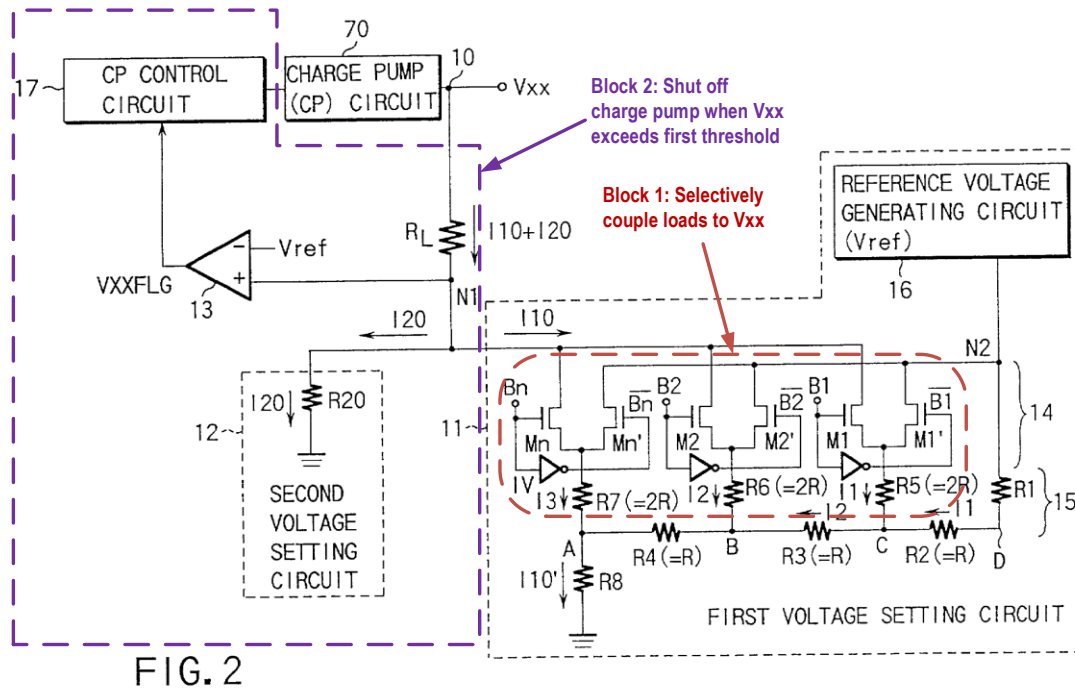
Hosono discloses charge pump circuit 70 that generates a desired output voltage V_{xx} for use in memory devices. EX-1007, 1:6-14, 5:5-8:65, FIG. 2 (reproduced below). Charge pump circuit 70 is connected to a load comprising

⁹ See n.4.

resistor R_L , second voltage setting circuit 12, and first voltage setting circuit 11. *Id.*

The charge pump output voltage can be regulated at a desired level. *Id.*, 14:51-

15:5.

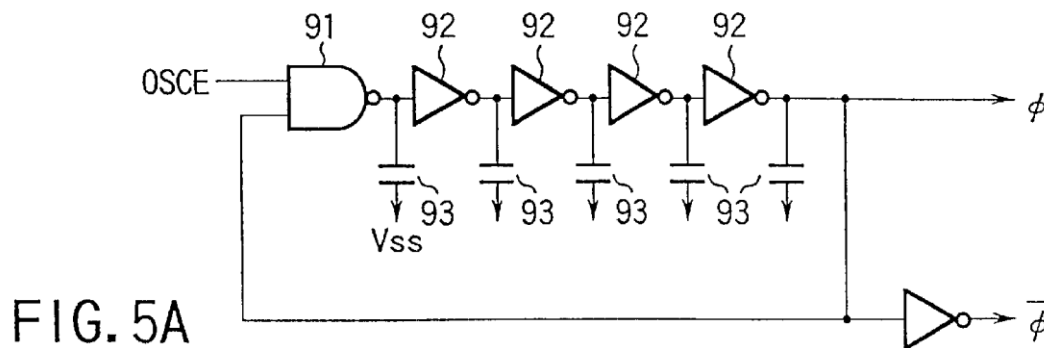


EX-1007, FIG. 2 (annotated)

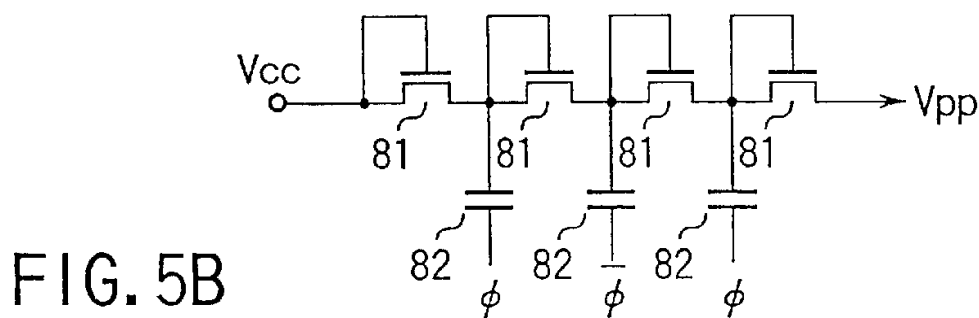
A POSITA would have noted that Hosono's disclosure about using a charge pump output circuit to supply regulated voltage to memory devices is similar to the teachings of Doluca and Buti. EX-1007, 1:6-41, 2:65-3:31, 5:5-64, 14:51-15:5; *supra* §§III.A.1-2; EX-1003, ¶¶99-102. A POSITA would have been motivated to look to Hosono for teachings that would supplement or improve upon Doluca and Buti. EX-1003, ¶102. For example, Doluca discloses that charge pump circuit 37

includes a pump clock generator 47, but does not describe the clock generator's structure. EX-1006, 5:19-54, FIG. 3. A POSITA would have been motivated to look at other references for details about the clock generator circuit. EX-1003.

¶103. In doing so, a POSITA would have noted that Hosono describes a charge pump circuit that is similar to Doluca's, and provides a detailed structure of a ring oscillator circuit for generating clock signals used in the charge pump circuit. EX-1007, 14:13-35, FIGS. 5A-5B (reproduced below). A POSITA would have understood that Hosono's ring oscillator circuit can be used in Doluca's clock generator 47, and would have been motivated to combine Hosono's teaching with Doluca's, with a reasonable expectation of success for this modification, as these techniques were known and the operation of the resulting circuit would have been predictable. EX-1003, ¶103; *see also* §III.B.2.(c), *infra*.



EX-1007, FIG. 5A



EX-1007, FIG. 5B

2. Claim 4

a) [4a]

Doluca teaches that its charge pump (bias) circuit includes pumping circuit 37, which includes multiple stages formed using capacitors and transistors. *See supra* §III.A.3.(b). Pumping circuit 37 includes diode-connected transistors 53, 55, and 57, which a POSITA would have interpreted as the claimed “plurality of diodes coupled in series.”¹⁰ *Id.*; EX-1003, ¶104. Transistors 57, 55, and 53 read on the “first diode,” “second diode,” and “last diode,” respectively, V_{cc} reads on “the supply voltage,” and V_{CP} reads on the “output pump.” EX-1003, ¶104.

¹⁰ Such interpretation is consistent with the ’241 Patent, which refers to diode-connected transistors as “diodes.” *See* ’241 Patent, 4:9-16, claim 5.

b) [4b]

Capacitors C2 and C1 in Doluca's FIG. 3 read on the "first capacitor" and "second capacitor," respectively. EX-1006, FIG. 3, 5:19-29. Each of C2 and C1 has an anode (the claimed "first terminal") 51' and 51, respectively, and a cathode 49' and 49 (the claimed "second terminal"), respectively. *Id.*; EX-1003, ¶¶105-106.

c) [4c]

Dolucas teaches that cathodes 49' and 49 (i.e., second terminals of the first and second capacitors C2 and C1, respectively, *supra* §III.B.2.(b)), are coupled to signals V_p and $\overline{V_p}$, which are a "biphase pair" of signals output by pump clock generator 47. EX-1006, FIG. 3, 5:19-29. A POSITA would have looked to FIGs. 5A and 5B of Hosono for disclosure about the circuitry of pump clock generator 47. *See supra* §III.B.1; EX-1003, ¶¶107-109.

In FIG. 5A, Hosono shows a plurality of inverters 92 that output clock signal ϕ , and shows an inverter that outputs complimentary signal $\bar{\phi}$. EX-1007, FIG. 5A, 14:13-23; EX-1003, ¶¶107-109. As a matter of design choice, a POSITA would have found it obvious to implement Dolucas's pump clock generator 47 according to Hosono's FIG. 5A to use clock signals ϕ and $\bar{\phi}$ as sources of $\overline{V_p}$

and V_p . EX-1003, ¶¶107-109. The resultant circuit is shown below. *Id.*

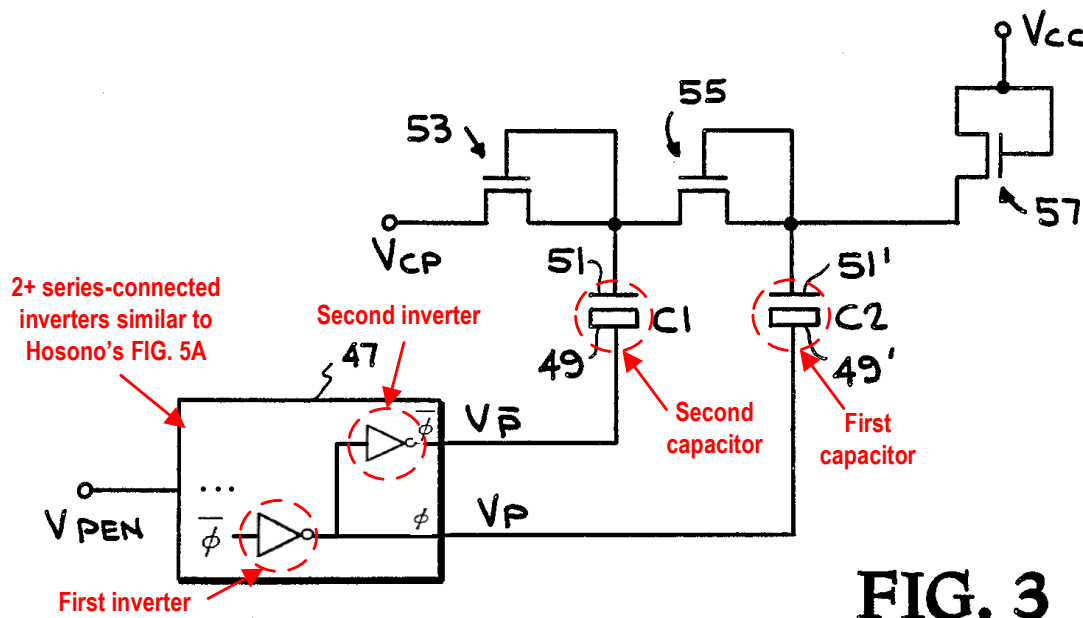


FIG. 3

EX-1006, FIG. 3 (modified and annotated based on EX-1007, FIG. 5A)

d) [4d]

Hosono discloses that its ring oscillator generates two-phase clock signals ϕ and $\bar{\phi}$. EX-1007, 14:4-35, FIG. 5A. A POSITA would have readily understood that the input of each inverter is a clock signal with a phase of either signal ϕ or $\bar{\phi}$. EX-1003, ¶110.

3. Claim 5

Doluca shows a plurality of diode-connected NMOS transistors 53, 55, and 57. *See supra* §III.B.2.(a). Each of transistors 53, 55, and 57 has its drain connected to the gate, forming a terminal that reads on the claimed “input

terminal.” EX-1003, ¶111. The source of each transistor reads on the claimed “second terminal.” *Id.*

4. Claim 11¹¹

a) [11a]

Doluca-Buti’s load selector means includes a target output pump selector comprising comparator 35 (claimed “first comparator”). EX-1006, FIG. 2 (reproduced below); *see also supra* §III.A.4. Comparator 35 has two input terminals (“+” and “-”), and an output terminal connected to charge pump 37 and line 46. EX-1006, FIG. 2, 4:31-45, 5:10-18. Comparator 35’s input terminal “-” is connected to V_{REF} , which a POSITA would have understood as being reference voltage V_{ref} . *Id.*; EX-1003, ¶112.

¹¹ In a related litigation, the court interpreted the term “coupled ... to” and “coupling ... to” in claims 6, 9, 10, and 11 to mean “connected without intervening resistors or other components that substantially change the voltage.” EX-1020, 2. Petitioner’s mappings are consistent with that interpretation.

terminal” is interpreted as separate from the “output terminal,”¹² a POSITA would have known that a comparator in some implementations has an enable terminal to receive an enable signal. *Id.*

b) [11b]

Doluca teaches that the target output pump selector includes voltage divider 31 having two terminals—one of which is connected to charge pump 37 output via capacitor-plate line 19, while the second terminal is connected to input terminal “+” of comparator 35. EX-1006, FIG. 2, 4:31-41; EX-1003, ¶¶115.

Doluca describes an implementation of voltage divider 31 that comprises a series of transistors. EX-1006, 6:21-44, 6:64-7:14, FIGS. 5-6. A POSITA would have found it obvious that voltage divider 31 can be implemented in the alternative using one or more resistor networks. EX-1003, ¶¶116-118. For example, Hosono describes a voltage generating circuit with respect to FIG. 7, having series-connected resistors R_L and R_1 ’ “for setting the value of output node 10.” EX-1007, 1:38-61, FIG. 7 (reproduced below). A POSITA would have readily understood that R_L and R_1 ’ together form a voltage divider circuit, with R_L and

¹² Under this interpretation, Petitioner reserves the right to challenge this limitation as indefinite in litigation.

R1' being equivalent to first and second resistor networks, respectively. EX-1007, 6:35-39; EX-1003, ¶¶117-118; *see also* EX-1007, 1:62-2:8, FIG. 8. A first terminal of R_L is connected to output of charge pump 70 at node 10, and a second terminal at node N1 connected to input “+” terminal of comparator 13. EX-1007, 1:38-61, FIG. 7; EX-1003, ¶¶117-118. A POSITA would have found it obvious that Doluca's voltage divider 31 can be implemented using Hosono's voltage divider circuit formed by R_L and R1', without changing the input/output connections of the divider circuit. EX-1003, ¶118.

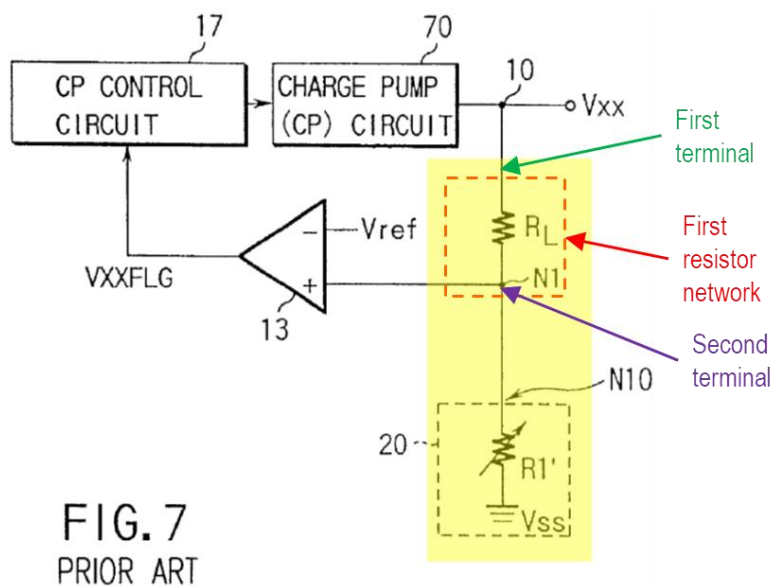


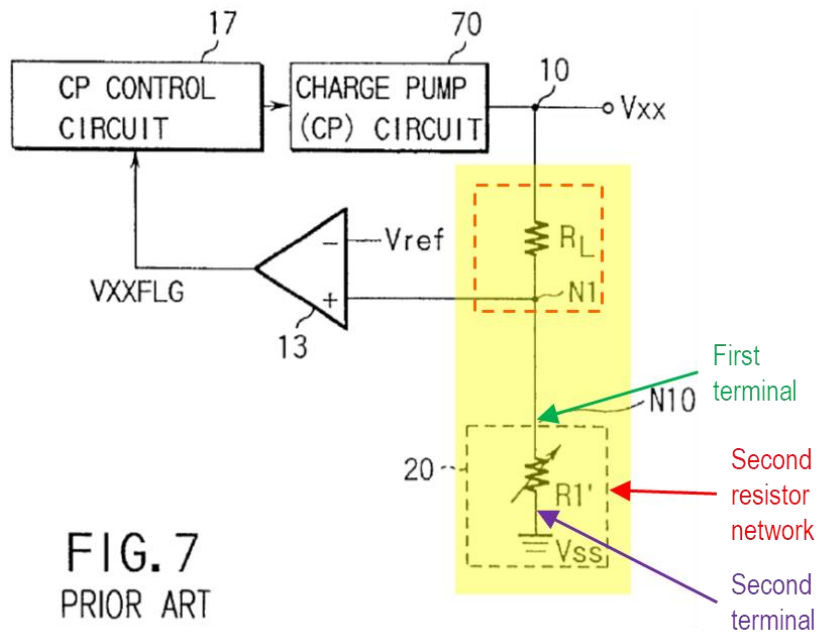
FIG. 7
PRIOR ART

EX-1007, FIG. 7 (annotated)

c) [11c]

Hosono's FIG. 7 voltage divider circuit includes equivalent resistor R1' as the “second resistor network.” *See supra* §III.B.4.(b). One terminal of R1' is

connected to the second terminal of first resistor network R_L at node $N1$, and the second terminal of $R1'$ is connected to ground V_{SS} . EX-1007, FIG. 7 (reproduced below); EX-1003, ¶119.



EX-1007, FIG. 7 (annotated)

d) [11d]

FIG. 2 of Doluca shows V_{BG} Generator 23 (“reference voltage source”) that generates V_{REF} , which is coupled to one of the two inputs of comparator 35. See *supra* §III.B.4.(a); EX-1003, ¶120.

5. Claim 12

a) [12a]¹³

The target output pump selector taught by Doluca in view of Buti includes a chain of diodes. *See supra* §III.A.2. A POSITA would have understood that each diode has intrinsic resistance and properties similar to a resistor. EX-1003, ¶¶74, 121. In the modified Doluca-Buti circuit (reproduced below), the upper four diodes form the “third resistor network” with two terminals, one of which is coupled to line 19 (output of charge pump). *Id.*

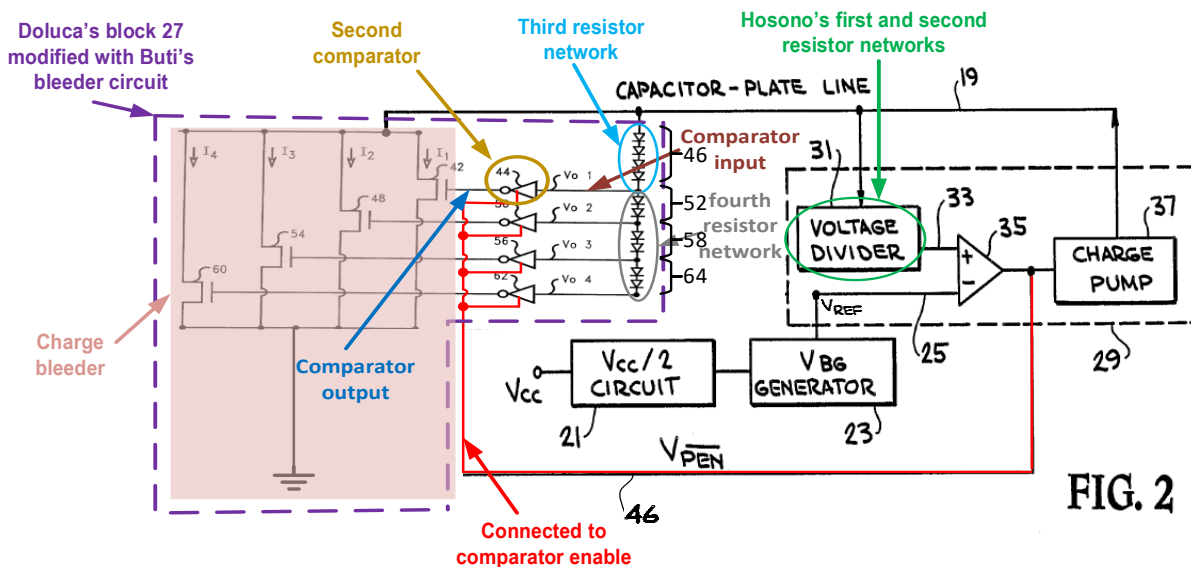


FIG. 2

¹³ See n.4.

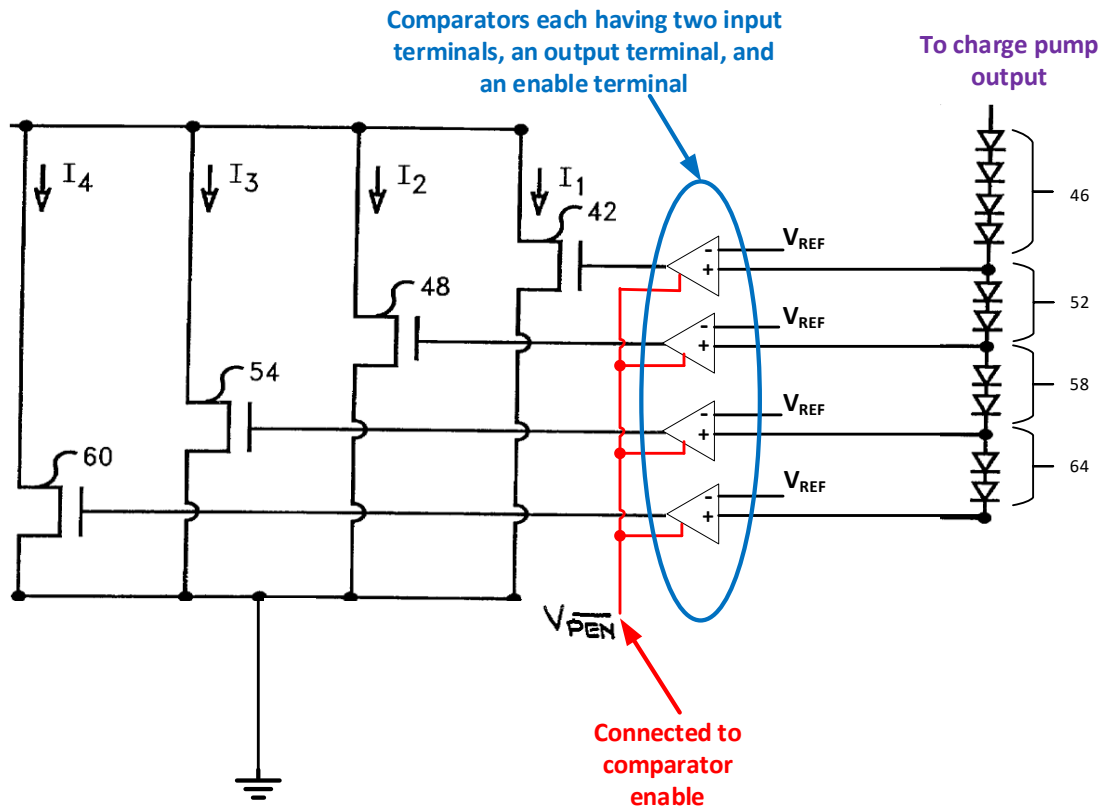
EX-1006, FIG. 2 (modified, annotated)

b) [12b]

A POSITA would have understood that, in Doluca-Buti's modified circuit, the lower six diodes form the "fourth resistor network," with the upper terminal coupled to the third resistor network (formed by the upper four diodes) and the lower terminal coupled to ground via inverter 62 and FET 60. *See supra* §III.B.5.(a); EX-1003, ¶122.

c) [12c]

Doluca-Buti's modified circuit includes inverter (or buffer) 44 with an input terminal coupled to the upper terminal of the fourth resistor network (formed by the lower six diodes) and an output terminal coupled to gate of FET 42. *See supra* §§III.B.5.(a)-III.B.5.(b). A POSITA would have understood that inverter/buffer 44, functioning as a fixed-level comparator, can be replaced with an op-amp-based comparator ("second comparator"), which has two input terminals, an output terminal, and an enable terminal, as arranged in [12c]. EX-1003, ¶¶77, 123. The resultant circuit, as partially illustrated below, reads on [12c] without negating the obviousness of [12a]-[12b]. *Id.*



EX-1006, FIG. 2 (in-part, modified in view of EX-1005, FIG. 3, annotated)

d) [12d]

Doluca-Buti's modified circuit shows the output terminal of inverter 44 ("second comparator") is coupled to the gate terminal of FET 42. *See supra* §§III.B.5.(a)-(c). A POSITA would have understood that FET 42 (and similarly, each of FETs 48, 54, 60) is a logic circuit having a gate terminal, a drain terminal, and a source terminal. EX-1003, ¶124.

e) [12e]

Consistent with [12a]-[12d], FETs 42, 48, 54, and 60 are each a logic circuit,

which, when selectively activated, functions as a load of the charge pump circuit.

Supra §§III.B.5.(a)-(d); EX-1003, ¶125. When voltage V_{CP} on capacitor-plate line 19 is higher than a maximum allowed level, one or more of the diode stacks will be forward-biased and, together with the corresponding comparators, control the corresponding FET(s) to turn on one or more bleeding paths. EX-1003, ¶125. A POSITA would have understood that these operations read on [12e]. *Id.*

6. Claim 13

a) [13a]

Doluca, Buti and Hosono all disclose charge pump circuits for use in memory devices. *See, e.g.*, EX-1006, 1:5-38; EX-1005, 1:11-2:28; EX-1007, 1:6-14. Hosono describes, with respect to FIG. 4, one such memory device that includes: an address bus comprising address buffer 64 and connections to row/column decoders; control circuit 67; a data bus comprising a data input/output buffer 66 and bit line control circuit 62; an address decoder comprising column decoder 63 and row decoder 65 coupled to the address bus; a read/write circuit comprising bit line control circuit 62 that is coupled to the data bus; and memory cell array 61 that is coupled to the address decoder, control circuit and read/write

circuit. EX-1007, 13:12-14:3, FIG. 4 (reproduced below); EX-1003, ¶¶126-127.¹⁴

Hosono's memory device of FIG. 4 further includes, coupled to the components above, high voltage generating circuits 681-683, which each use a charge pump circuit for obtaining a high voltage. EX-1007, 14:4-50, FIGS. 4-6; EX-1003, ¶128. To the extent "with minimum ripples" is limiting,¹⁵ Hosono discloses that its charge pump circuit generates voltage with minimum ripples by describing a feedback mechanism to stabilize the charge pump voltage at a desired level. *See* EX-1007, 14:61-15:5; EX-1003, ¶128. Doluca similarly discloses this limitation. *See supra* §III.A.3.(a); EX-1003, ¶128.

¹⁴ *See* n.11. While that construction was proposed in the context of different claims and Petitioner believes the Board does not need to construe this limitation for purposes of the IPR, should the Board adopt such a construction for claim [13a], then Hosono as mapped above still reads on this limitation.

¹⁵ *See* n.5.

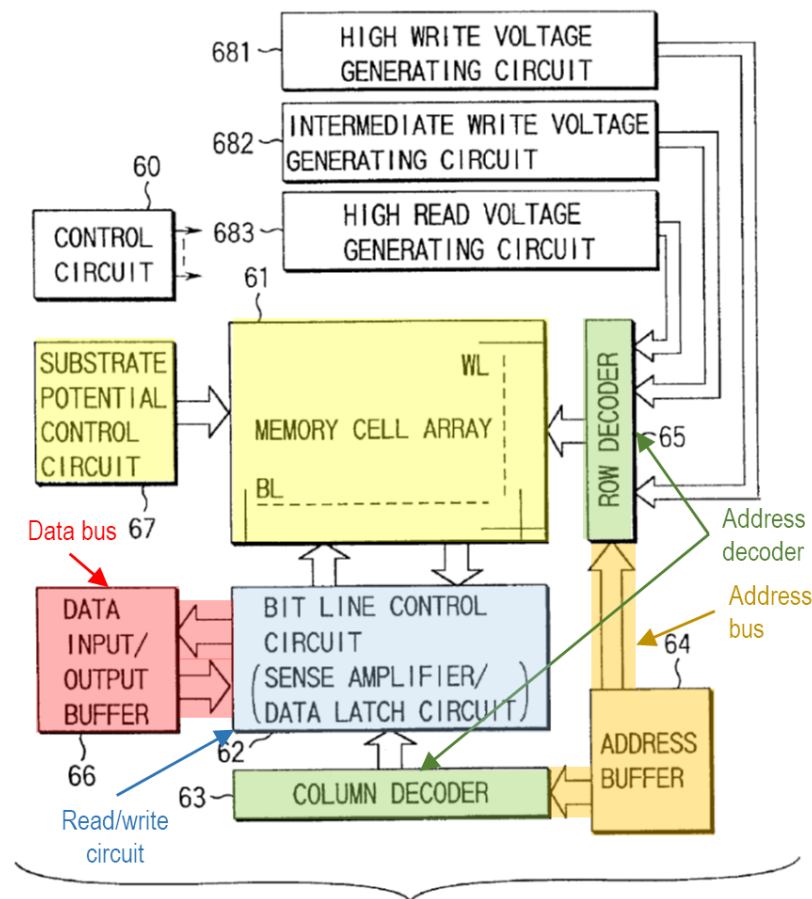


FIG. 4

EX-1007, FIG. 4 (annotated)

A POSITA would have understood that Doluca's bias circuit can be used as the charge pump circuit in Hosono's high voltage generating circuits 681-683 for obtaining a high voltage. *See supra* §III.A.3.(a); EX-1003, ¶129. Similar to Hosono's charge pump circuit, Doluca's bias circuit provides a pump voltage with minimum ripples by generating a stable voltage within a narrow range of a target (design) voltage. *See supra* §III.A.3.(a); EX-1003, ¶129.

b) [13b]-[13f]

The Doluca-Buti combination discloses [13b]-[13f]. *See supra* §§III.A.3.(b)-(d), III.A.4-III.A.5; EX-1003, ¶¶130-131.

7. Claim 14

Doluca-Buti-Hosono discloses claim 14. *See supra* §§III.B.2.(a)-(d). With respect to “the output of the last inverter being coupled to the input of the last diode,” Doluca’s FIG. 3 as modified in view of Hosono shows the output of the second inverter is coupled to the anode of diode 53 via capacitor C1. *Supra* §§III.B.2.(c); EX-1003, ¶132.

8. Claim 15

Doluca-Buti-Hosono discloses claim 15. *See supra* §§III.B.3; EX-1003, ¶133.

9. Claim 21¹⁶¹⁷

Doluca-Buti-Hosono discloses claim 21. *See supra* §§III.B.4.(a)-(d); EX-1003, ¶134.

10. Claim 22

To the extent the term “coupled to” is interpreted to allow intervening capacitors,¹⁸ Doluca-Buti-Hosono discloses claim 22. *See supra* §§III.B.2.(b)-(d). Modified FIG. 3 of Doluca, *supra* §III.B.2.(c), shows the second inverter being coupled to diode 53 via intervening capacitor 51, which reads on “b) ... the output of the last inverter being coupled to the input of the last diode.” EX-1003, ¶135.

¹⁶ Petitioner reserves the right to challenge, in litigation, [21b] as indefinite and without written description. With the understanding this limitation should read “b) ... the second terminal being coupled to ~~the output~~ an input terminal of the first comparator,” Doluca teaches the limitation. *See supra* §III.B.4.(b).

¹⁷ *See* n.4.

¹⁸ To the extent the term “coupled to” is interpreted differently, Petitioner reserves the right to challenge this claim in litigation as indefinite and lacking written description.

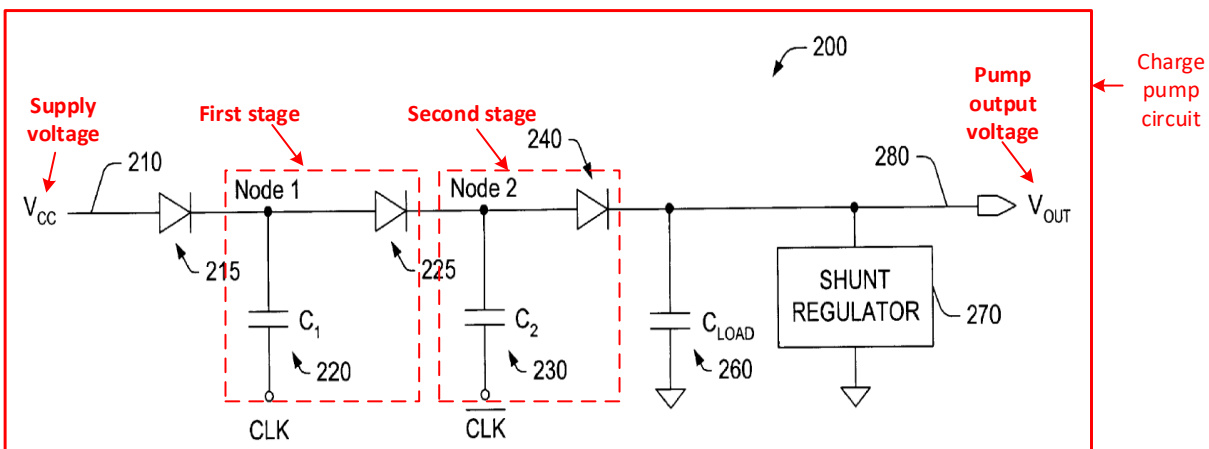
11. Claim 23

Hosono discloses claim 23. EX-1007, 1:1-20, 3:1-31, 11:61-12:4; EX-1003, ¶136.

C. GROUND 2A: Claims 1 and 6-10 are rendered obvious by Le and Ujiie

1. Overview of Le

Le describes a conventional multi-stage charge pump circuit, shown below, that generates an output voltage V_{out} using a supply voltage V_{CC} . EX-1008, 1:52-4:18, FIGS. 1-2. Le further discloses regulating V_{out} using shunt regulator 270. *Id.*; EX-1003, ¶138.



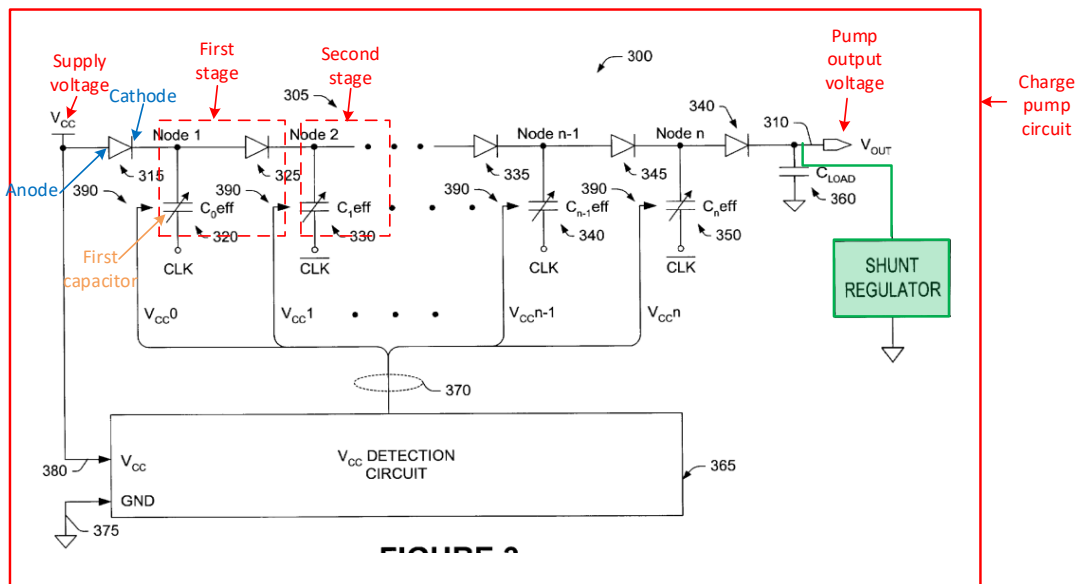
EX-1008, FIG. 2 (annotated)

Le modifies the conventional charge pump circuit by using “variable bootstrap capacitance value which is varied as a function of the input supply

voltage.” *Id.*, 4:30-5:32. The modified circuit, referred to as charge pump system 300, can use a shunt regulator to reduce ripple at the pump output voltage, which is provided for flash memory cell operations. *Id.*, 6:22-26, 7:4-25, 10:41-11:6, FIG.

3. The only example of shunt regulator described in Le is shunt regulator 270, and a POSITA would have understood that Le’s disclosure of using a shunt regulator with respect to the FIG. 3 circuit refers to using shunt regulator 270. EX-1003,

¶139. A resultant circuit would look similar to the one reproduced below. *Id.*

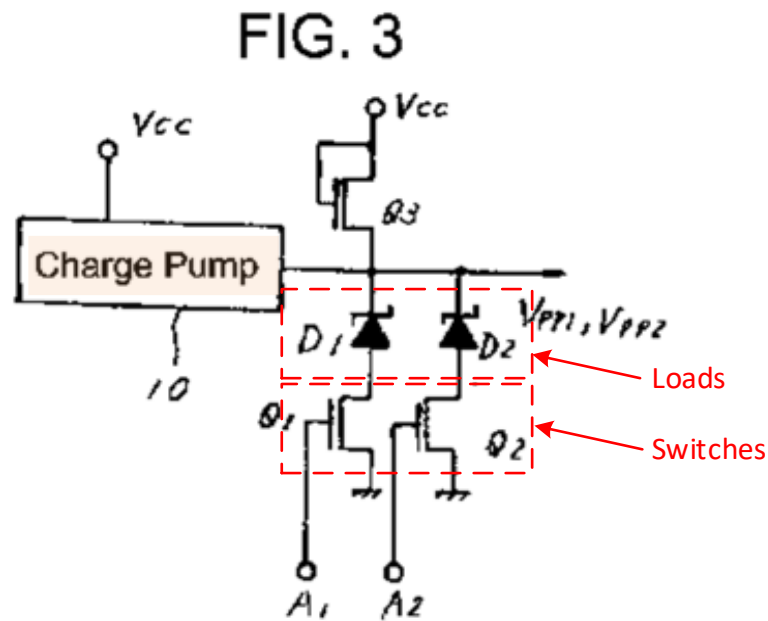


EX-1008, FIG. 3 (modified and annotated)

2. Overview of Ujiie

Ujiie discloses a booster circuit comprising a charge pump to generate voltages used during write and erase operations of a memory device. EX-1009, ¶[01], ¶¶[18]-[21]. Ujiie discloses solutions to reduce output voltage fluctuation

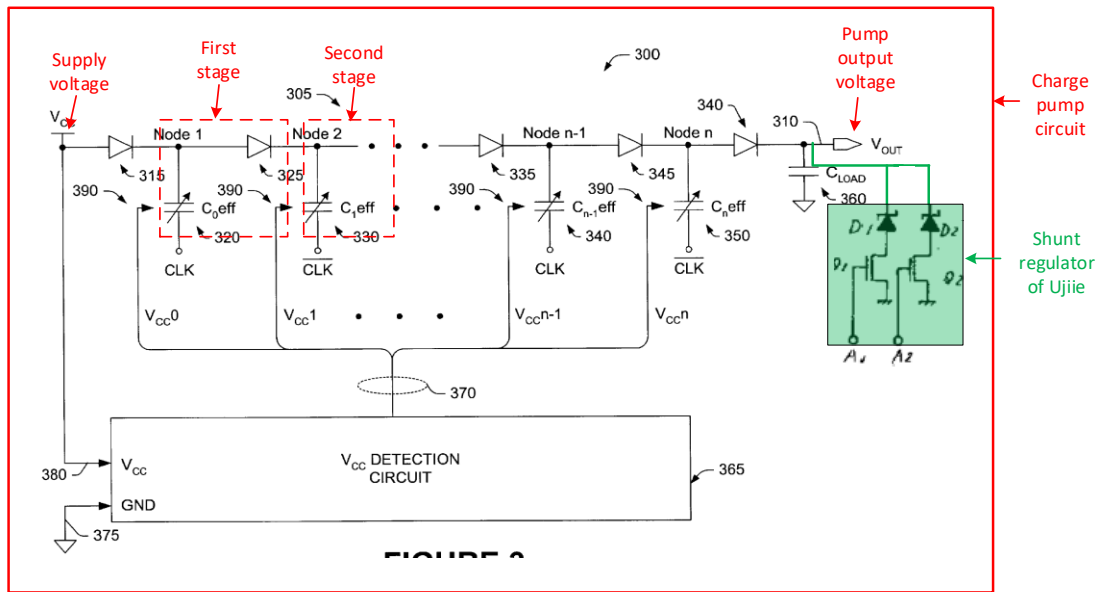
by using a shunt circuit coupled to the charge pump output. *Id.*, ¶¶[20]-[25], FIG. 3 (reproduced below). Ujiie's shunt circuit includes switches Q1 and Q2 that selectively couple diodes D1 and D2, respectively, as loads to the charge pump. *Id.*; EX-1003, ¶141.



EX-1009, FIG. 3 (annotated)

A POSITA would have found it obvious to combine Le and Ujiie, for at least the following reasons. Le discloses a charge pump circuit to supply voltages to memory devices. *See supra* §III.C.1. Le describes that the charge pump output voltage can be regulated using a shunt regulator (e.g., shunt regulator 270), but does not provide further structural or functional description of the shunt regulator. *Id.* A POSITA who, upon reviewing Le's charge pump circuit, wanted to know

more about how a shunt regulator can be used to regulate the output voltage, would have looked at other sources of information about shunt regulators. EX-1003, ¶142. In doing so, a POSITA would have been motivated to consider references that describe such regulators in the context of charge pump circuits used for memory devices. *Id.* Ujiie is one such reference describing use of a booster (i.e., charge pump) circuit to supply voltages to memory devices and, like Le, discloses the use of shunt circuit to regulate the charge pump output voltage. EX-1009, ¶¶[20]-[25], FIG. 3. A POSITA would have understood that Ujiie's shunt circuit can be used as a shunt regulator in Le's charge pump circuit to regulate the pump output voltage, as a matter of design choice. EX-1003, ¶143. A version of Le's charge pump circuit with a shunt regulator as taught by Ujiie as would have been understood by a POSITA, is shown below. *Id.* A POSITA would have had a reasonable expectation of success for this modification, as these techniques were known and the operation of the resulting circuit would have been predictable. *Id.* Accordingly, a POSITA would have been motivated to combine Le and Ujiie. *Id.*



EX-1008, FIG. 3 (modified based on EX-1009, FIG. 3, annotated)

3. Claim 1

a) [1pre]¹⁹

Le discloses embodiments of charge pump circuits that generate a charge pump voltage V_{OUT} , e.g., charge pump system 300. *See supra* §III.C.1. Le notes that the disclosed charge pump provides “further reduction in power consumption” by using a shunt regulator, an embodiment of which is shown as shunt regulator 270 with respect to prior art charge pump 200. EX-1008, 10:61-11:6, 3:5-52, FIG. 2; EX-1003, ¶144. A POSITA would have known that such a shunt regulator is commonly used for reducing voltage ripples, as noted by Le, which discloses that

¹⁹ *See* n.5.

the shunt regulator “advantageously provides a smaller ripple voltage at its regulation output [than prior art charge pump circuits].” EX-1008, 10:41-11:6; *see also id.*, 6:15-25; EX-1003, ¶144.

b) [1a]

Le teaches the claimed pumping circuit by describing that the charge pump system 300 includes a charge pump circuit 305 that has one or more stages “to receive the supply voltage 380 and generate the charge pump output voltage V_{OUT} 310.” *Supra* §III.C.1; EX-1008, 2:18-3:24, 4:31-59, 7:4-49, FIGs. 1-3; EX-1003, ¶145.

Le teaches that the charge pump voltage generated by its disclosed embodiment can be applied to program/erase operations of memory cells, and notes that such operations in semiconductor memory devices use different voltage levels, which are generated by the charge pump circuits. EX-1008, 1:7-18, 1:51-2:34. A POSITA would have found it obvious that Le’s disclosed pump system 300 with pumping circuit 305 can be applied to generate a plurality of pump voltages used in memory device operations. EX-1003, ¶146.

c) [1b]

While Le teaches that a shunt regulator can be coupled to the output of a charge pump, Ujiie discloses the structure of an example shunt regulator, which

includes diodes D1 and D2, and switches Q1 and Q2. *See supra* §III.C.2. A POSITA would have understood that diodes D1 and D2 in Ujiie's shunt regulator form the loads. EX-1003, ¶¶147-148. Ujiie further teaches that diodes D1 and D2 are associated with write voltage V_{pp1} and erase voltage V_{pp2} , respectively, and that signals A1 and A2 control switches Q1 and Q2, respectively, to selectively couple diodes D1 and D2 to the output of charge pump 10. EX-1009, ¶¶[18]-[25]; EX-1003, ¶148.

d) [1c]

Ujiie teaches that its charge pump circuit includes the claimed "load selector means" including switches Q1 and Q2 and control signals A1 and A2, which are used to selectively couple diodes D1 and D2 to the charge pump output to generate V_{pp1} and V_{pp2} . *See supra* §III.C.3.(c); EX-1003, ¶149.

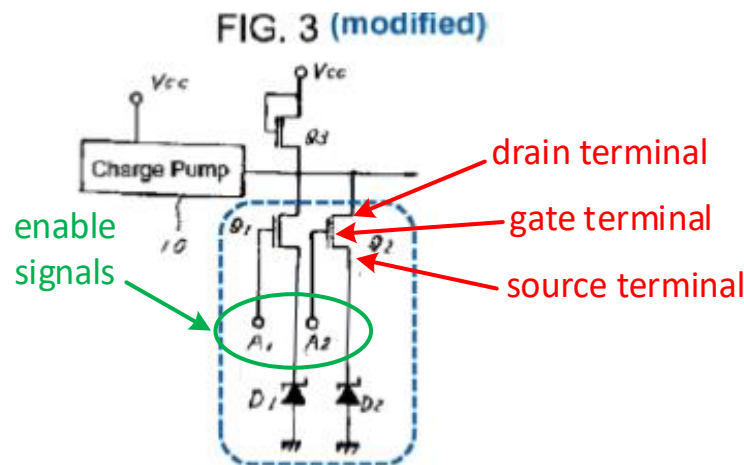
4. Claim 6²⁰

Ujiie discloses that switches Q1 and Q2 in the load selector means are NMOS switches, each coupled with one of diodes D1 and D2 ("loads") in series. EX-1009, ¶[20], FIG. 3. The gate terminal of each switch Q1 and Q2 is the "enable terminal," to which control signals A1 and A2 are respectively applied to

²⁰ See n.11.

enable the switches. *Id.*, ¶[23]. The drain and source terminals of each switch form respective “first” and “second” terminals. EX-1003, ¶¶150-151.

Because each load and its corresponding switch are connected in series, it would have been an obvious design choice to swap the positions of the load and its corresponding switch, as shown in modified FIG. 3 of Ujiie below. *Id.*, ¶152. In the modified circuit, each of switches Q1 and Q2 has its drain (second) terminal coupled to the output of charge pump 10 and source (first) terminal coupled to its corresponding load. *Id.* A POSITA would have had a reasonable expectation of success for this modification, as the operation of the resulting circuit would have been predictable. *Id.*

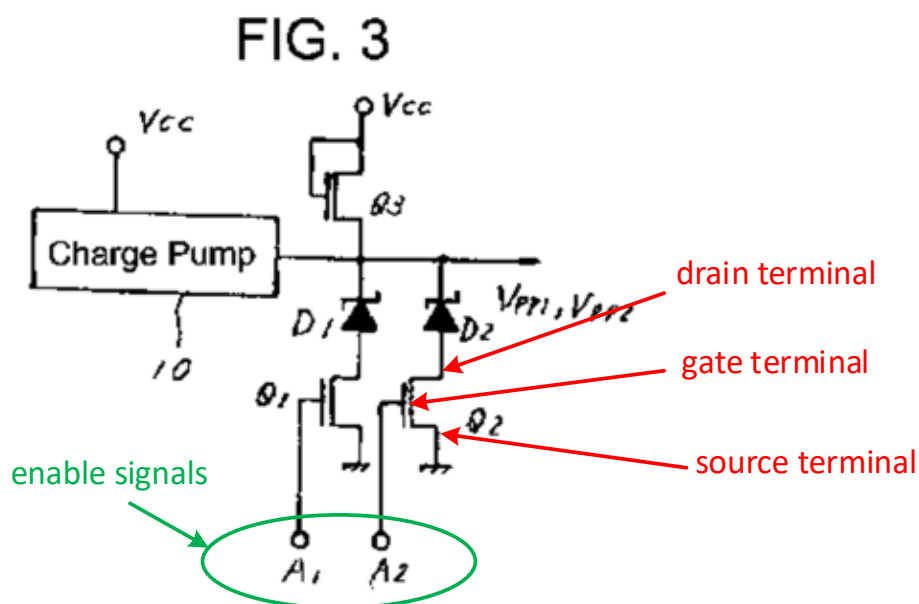


EX-1009, FIG. 3 (modified with annotation)

5. Claim 7

With the understanding that “NMOS load transistor” means NMOS

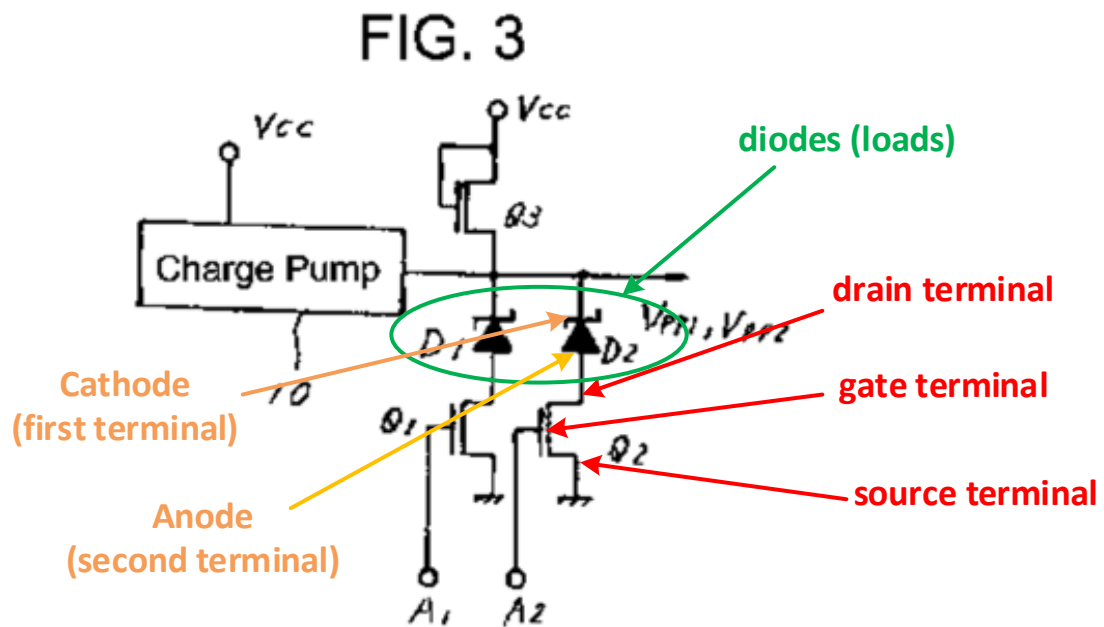
transistor controlling a load, Ujiie teaches this limitation.²¹ Switches Q1 and Q2 in Ujiie's load selector means are NMOS switches, each with a gate, a drain, and a source, which are enabled using signals A1 and A2 respectively. *See supra* §III.C.2. A POSITA would have readily understood that the gate terminals of Q1 and Q2 are connected to A1 and A2, respectively, the source terminals of Q1 and Q2 are connected to ground, and the drain terminals of Q1 and Q2 are connected to D1 and D2 ("load"), respectively. EX-1009, FIG. 3 (reproduced below); EX-1003, ¶153.



²¹ See n.4.

6. Claim 8

A POSITA would have known that diodes D1 and D2 of Ujiie are current sinkers. EX-1003, ¶154. Looking at FIG. 3 of Ujiie, a POSITA would also have understood that diodes D1 and D2 have their respective cathodes (the “first terminal”) connected to the charge pump output and their respective anodes (the “second terminal”) connected to the corresponding NMOS switch Q1 and Q2, respectively. EX-1009, FIG. 3; EX-1003, ¶154.



EX-1009, FIG. 3 (annotated)

7. Claim 9²²

With the understanding that “a load NMOS transistor” means an NMOS transistor controlling a load, Ujiie renders this limitation obvious.²³ The ’241 Patent does not describe what an “elevator circuit” is. EX-1001, 5:32-43, FIG. 5B. However, a POSITA would have known a level shifter is an example of an elevator circuit, and would have found that claim 9 merely recites an obvious design choice from Ujiie. EX-1003, ¶155. As noted previously, a POSITA would have found it obvious to modify FIG. 3 of Ujiie by swapping positions of diodes D1 and D2 with respective NMOS switches Q1 and Q2, such that the sources of Q1 and Q2 are connected to the cathodes of D1 and D2, respectively. *See supra* §III.C.4. Compared to Ujiie’s original circuit where the sources of Q1 and Q2 are connected to ground, the modification would have increased the source voltages of Q1 and Q2 when the two NMOS switches are activated. EX-1003, ¶156. For an NMOS switch to turn on, the gate-to-source voltage V_{GS} must be greater than a threshold voltage V_{th} ; thus the increase of the source voltages of Q1 and Q2 would require an increase of the gate voltages of Q1 and Q2 to maintain adequate V_{GS} for activating

²² See n.11.

²³ See n.4.

Q1 and Q2. *Id.*, ¶157. Accordingly, it would have been obvious for a POSITA to use a level shifter to boost the voltage of control signals A1 and A2 such that the voltage levels at the gates of Q1 and Q2 are higher than the voltage levels in Ujiie's original circuit. *Id.*, ¶158.

8. Claim 10²⁴

A POSITA would have known that each diode D1 and D2 in Ujiie is a current sinker. EX-1003, ¶159. As noted previously, an obvious modification of Ujiie's FIG. 3 would have resulted in the cathodes of D1 and D2 being connected to the sources of NMOS switches Q1 and Q2, respectively, and the anodes of D1 and D2 being connected to ground. *See supra* §III.C.4; EX-1003, ¶159.

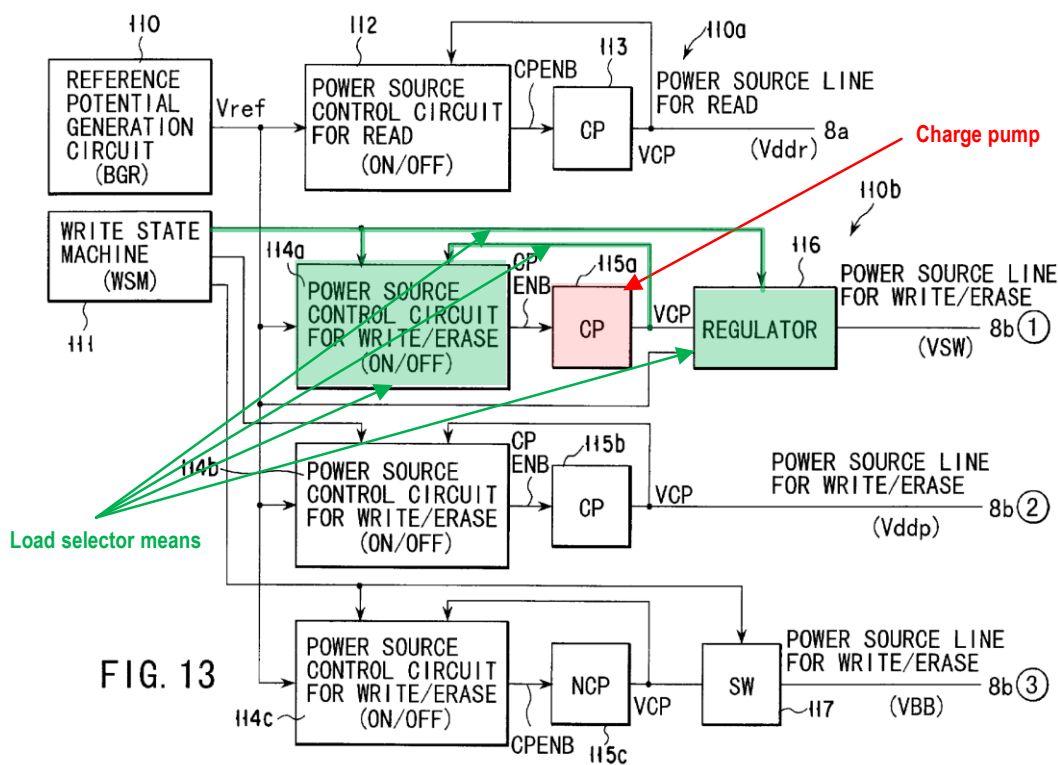
D. GROUND 2B: Claims 2, 3, 11, 24, and 25 are rendered obvious by Le, Ujiie, and Kuriyama

1. Overview of Kuriyama

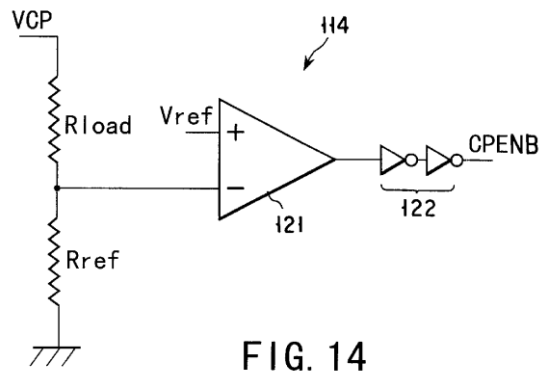
Kuriyama discloses a memory device power system comprising a charge pump for providing boosted voltage to memory cells. EX-1011, 4:42-5:18, 11:19-13:3, FIGS. 12-15. To generate a target output voltage, Kuriyama turns the charge pump 115a On/Off by comparing the output voltage with a reference voltage V_{ref} , and further regulates the output voltage using a regulator having multiple

²⁴ See n.11.

operational amplifiers (OPs). *See id.*, 11:38-12:45, FIGS. 13-15 (reproduced below). FIG. 13 illustrates the control circuit 114a (having a structure as shown in FIG. 14) for turning On/Off the charge pump, while regulator 116 (having a structure as shown in FIG. 15) is used to regulate the charge pump output V_{CP} . *Id.*; EX-1003, ¶¶161-164.



EX-1011, FIG. 13 (annotated)



EX-1011, FIG. 14

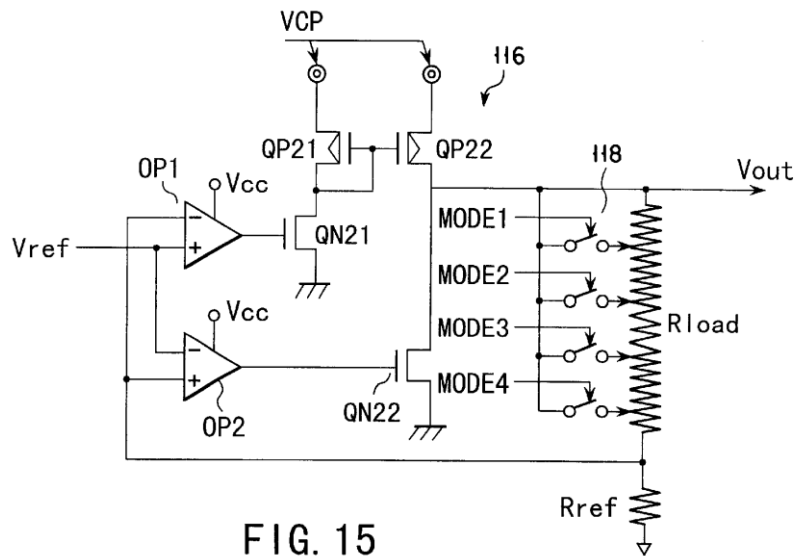


FIG. 15

EX-1011, FIG. 15

A POSITA would have found it obvious to combine Kuriyama with Le and Ujiie, for at least the following reasons. Le and Ujiie teach a charge pump circuit with a shunt regulator having a load selector means to selectively couple loads to the pump output to regulate the output voltage. *See supra* §§III.C.3.(a)-(d). A

POSITA would have known, or would have found it obvious (or advantageous), that in some charge pump circuits the load selector means includes additional circuitry to shut down the charge pump for reasons such as power efficiency.²⁵

EX-1003, ¶165. Similar to Le and Ujiie, Kuriyama describes using a charge pump to provide voltages to memory devices and is concerned about regulating the charge pump output voltage. EX-1011, 4:42-5:18, 11:19-13:3; *supra* §§III.C.1-2; EX-1003, ¶166. A POSITA would have noted that Kuriyama discloses that a control circuit 114a is used to turn off charge pump 115a when charge pump output V_{CP} reaches reference voltage V_{ref} . EX-1011, 11:38-12:45; EX-1003, ¶166.

A POSITA would have found that including Kuriyama's control circuit 114a in Le-Ujiie's charge pump circuit provided the capability to turn off the charge pump circuit when V_{OUT} reached a reference voltage, e.g., V_{pp1} or V_{pp2} . EX-1003, ¶166.

A POSITA would have been motivated to make this modification as a matter of design choice, and would have had a reasonable expectation of success in doing so, as the operation of the resulting circuit would have been completely predictable.

Id. Accordingly, a POSITA would have had the motivation to combine Le, Ujiie, and Kuriyama. *Id.*

²⁵ See n.6.

2. Claim 2

Le and Ujiie teach a charge pump circuit with a shunt regulator having a load selector means to selectively coupled loads to the pump output to regulate the output voltage. *See supra* §§III.C.3.(a)-(d). As noted above, a POSITA would have been motivated to include Kuriyama's control circuit 114a as part of the load selector means in Le-Ujiie's charge pump circuit to provide the capability to turn off the charge pump circuit when V_{OUT} reaches a reference voltage, e.g., V_{pp1} or V_{pp2} . *See supra* §III.D.1; EX-1003, ¶167.

3. Claim 3²⁶

Kuriyama discloses that a regulator 116 is used to control charge pump circuit 115a output V_{out} , based on comparing V_{CP} , divided using resistors R_{load} and R_{ref} , to V_{ref} . EX-1011, 12:28-46, FIG. 15; *see also supra* §III.D.1. A POSITA would have found it obvious that using regulator 116 of Kuriyama as part the load selector means of the Le-Ujiie combination (e.g., in conjunction with Ujiie's disclosed shunt circuit) provides flexibility to regulate the charge pump output, e.g., by enabling additional target voltage levels to be provided by the charge pump circuit beyond the V_{pp1} , V_{pp2} . EX-1003, ¶168.

²⁶ *See* n.4.

Kuriyama's voltage regulator 116 includes resistors R_{load} and R_{ref} forming a voltage divider between V_{out} and ground. EX-1011, 12:28-55, FIG. 15. Also between V_{out} and ground is an NMOS transistor QN22. *Id.* A POSITA would have found it obvious that the circuit including R_{load} , R_{ref} , and QN22 forms a load. EX-1003 ¶169. A POSITA would also have found it obvious to adjust the current flowing through the load to regulate the voltage V_{out} . *Id.*, ¶170. For example, when V_{out} is higher than a corresponding threshold, it would have been obvious to a POSITA to control switch 118 to reduce the value of R_{load} (e.g., changing from R1 to R4 by switching from MODE1 to MODE4), thereby increasing the voltage at the "+" terminal of OP2. *Id.* With the "-" terminal of OP2 coupled to V_{ref} , a voltage increase at the "+" terminal increases the OP2 output voltage, which increases the bias voltage at the gate terminal of QN22, and in turn increases the current flowing through QN22 ("adding additional loads"), causing a decrease in V_{out} . *Id.*, ¶¶171-173.

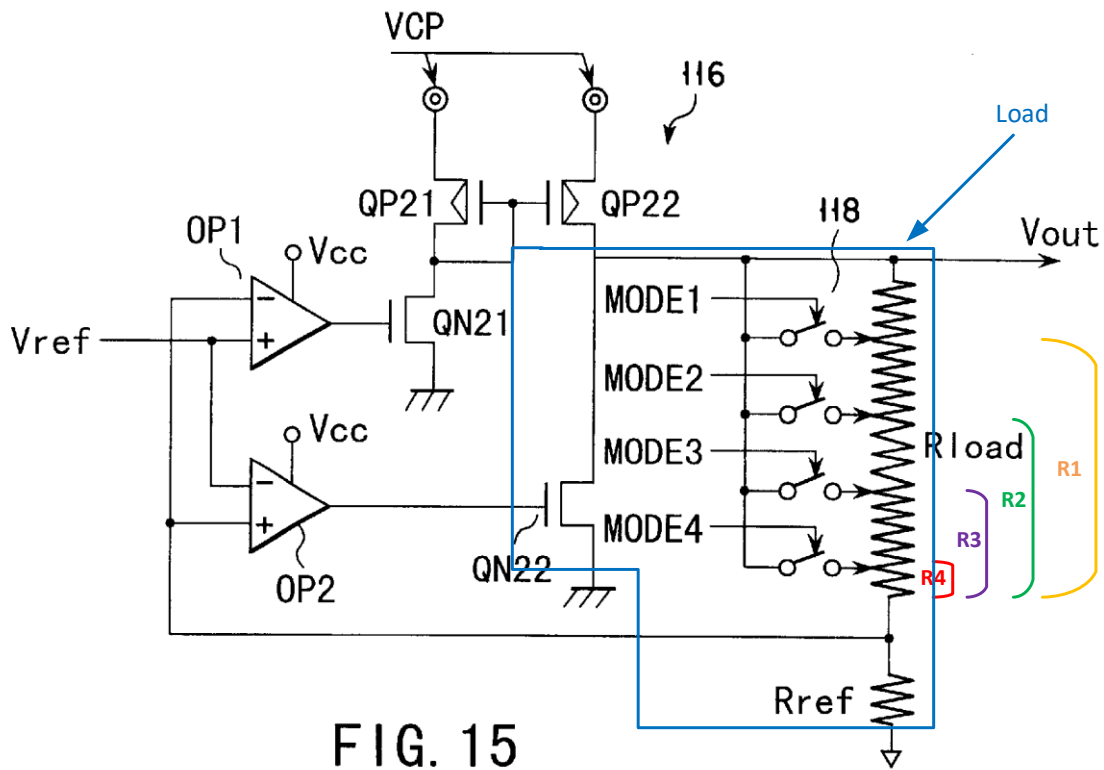


FIG. 15

EX-1011, FIG. 15 (annotated)

4. Claim 11²⁷

a) [11a]

The load selector means in the charge pump circuit of Le-Ujiiie includes Kuriyama's control circuit 114a, which performs the functions of the claimed "target output pump selector." See *supra* §III.D.2. Control circuit 114a (labeled 114 in Kuriyama's FIG. 14) includes comparator 121 ("first comparator"), which

²⁷ See n.11.

has two input terminals, labeled “+” and “-,” respectively. *See supra* §III.D.1.

The “+” input of comparator 121 is connected to Vref. EX-1011, FIG. 14; EX-1003, ¶174.

Comparator 121 has an output terminal, which controls On/Off of charge pump 115a. EX-1011, FIGS. 14-15; EX-1003, ¶174. A POSITA would have understood the output terminal of comparator 121 reads on both the “output terminal” and the “first enable terminal.” EX-1003, ¶174. Alternatively, to the extent the “first enable terminal” is interpreted as separate from the “output terminal,”²⁸ a POSITA would have found it obvious that comparator 121 has an enabled terminal (“first enable terminal”). *Id.*

b) [11b]

A POSITA would have understood that R_{load} in Kuriyama’s control circuit 114 reads on the “first resistor network.” EX-1011, FIG. 14; EX-1003, ¶175. The upper terminal of R_{load} is coupled to VCP (“output pump”), while the lower terminal of R_{load} is connected to the “-” input terminal of comparator 121. EX-1011, FIG. 14; EX-1003, ¶175.

²⁸ *See* n.4.

c) [11c]

A POSITA would have found that R_{ref} in Kuriyama's comparator 121 reads on the "second resistor network." EX-1011, FIG. 14; EX-1003, ¶176. The upper terminal of R_{ref} is connected to the lower terminal of R_{load} , and the lower terminal of R_{ref} is connected to ground. EX-1011, FIG. 14; EX-1003, ¶176.

d) [11d]

Kuriyama shows V_{ref} coupled to the "+" input terminal of comparator 121. EX-1011, FIG. 14; EX-1003, ¶177.

5. Claim 24²⁹

Le in view of Ujiie teaches [24pre]-[24b]. *See supra* §§III.C.3.(a)-(d); EX-1003, ¶178.

Kuriyama, in combination with Le and Ujiie, renders obvious disabling the charge pump circuit when $V_{\text{cfra}} > V_{\text{ref}}$. *See supra* §III.D.2; EX-1003, ¶178. A POSITA would have found it obvious that the charge pump circuit is left on when $V_{\text{cfra}} \leq V_{\text{ref}}$. EX-1003, ¶¶179-180; *see also* EX-1011, 11:61-65. This would have made [24c] also obvious.

²⁹ *See* n.5.

6. Claim 25³⁰

Kuriyama teaches [25a]. *See supra* §III.D.3; EX-1003, ¶181. In view of Kuriyama's teaching that adding loads can reduce pump output voltage, a POSITA would have readily understood that removing loads can increase the pump output voltage. EX-1003, ¶¶182-183.

E. GROUND 2C: Claims 4 and 5 are rendered obvious by Le, Ujiie, and Hosono

1. Claim 4

a) [4a]

The charge pump circuit disclosed with respect to Le's FIG. 3 includes diodes 315 ("first diode"), 325 ("second diode"), and 340 ("last diode"), connected in series, each having an anode ("input terminal") and a cathode ("output terminal"). *See supra* §III.C.1. The anode and cathode of 315 are respectively coupled to V_{cc} ("supply voltage") and the anode of 325, while the cathode of 340 is coupled to V_{OUT} ("output pump"). *Supra* §III.C.1; EX-1003, ¶186.

b) [4b]

The charge pump circuit of Le's FIG. 3 includes capacitors C_{0eff} ("first capacitor"), C_{1eff} ("second capacitor") and C_{neff} ("last capacitor"), each having an

³⁰ *See* n.4.

upper plate (“first terminal”) and a lower plate (“second terminal”). *See supra* §III.C.1. The upper plate of C_{0eff} is coupled to the cathode of first diode 315 and to the anode of second diode 325 at Node 1. The upper plate of C_{1eff} is coupled to the cathode of diode 325 and to the anode of next diode in the series (“third diode”) at Node 2. The upper plate of C_{neff} is coupled to the anode of diode 340 (“last diode”) at Node n. *Id.*; EX-1003, ¶187.

c) [4c]

Le teaches clock signals CLK and $\overline{CLK}$ provided to the lower plates of capacitors C_{0eff} to C_{neff} , and Ujiie similarly teaches clock signals ϕ and $\bar{\phi}$ provided to the lower plates of capacitors C_1 - C_m . EX-1008, FIG. 3; EX-1009, FIG. 4.

Le and Ujiie do not explicitly describe the circuit that generates the clock signals. However, a POSITA would have found that Hosono describes a compatible clock generator and can be combined with Le and Ujiie to teach this limitation. *See supra* §III.B.2.(c); EX-1003, ¶¶184-185, 188-191.

Hosono discloses its clock generator for use in a charge pump circuit to provide voltages to memory devices, and a POSITA would have found it obvious that Hosono’s clock generator can be used in Le-Ujiie’s charge pump circuit to generate CLK and $\overline{CLK}$ signals using a series of inverters. *See supra* §III.B.1; EX-

1003, ¶¶188-191. A POSITA would have been motivated to combine Hosono's teaching with Le and Ujiie with a reasonable expectation of success, as these techniques were known and the operation of the resulting circuit would have been predictable. EX-1003, ¶¶188-191.

d) [4d]

Hosono teaches this limitation. *See supra* §III.B.2.(d); EX-1003, ¶192.

2. Claim 5

Le teaches this limitation by describing diode connected transistors 515-518 being used instead of regular diodes in one aspect of the disclosed charge pump systems, suggesting that transistors 515-518 are interchangeable with diodes. EX-1008, 9:27-10:7, FIG. 5; EX-1003, ¶193. Le further references diode connected transistors while describing the operation of the charge pump system 300. EX-1008, 7:61-8:3; EX-1003, ¶193.

F. GROUND 3A: Claims 13-17, 19, and 21-23 are rendered obvious by Asano, Le, Ujiie, and Kuriyama

1. Overview of Asano

Asano describes a memory system that can provide boosted voltages to memory cells. EX-1012, 1:6-2:5, 4:40-5:4, 7:50-8:59, FIGS. 3-15; EX-1003, ¶195. In similar contexts, Le, Ujiie, and Kuriyama relate to regulating the output voltage of charge pumps (i.e., boosted voltage) that is provided to memory devices. *See*

supra §§III.C.1-2, III.D.1.

A POSITA would have been motivated to combine Asano with Le for the following reasons. Le discloses that its charge pump circuit can be used to provide boosted voltage for memory devices. EX-1008, 1:7-5:26. While Le does not describe any structural details of a memory device, a POSITA would have understood that Le's charge pump circuit can be applied to various memory devices, and would have noted that Asano teaches a memory device that uses a voltage boosting circuit to provide a boosted voltage to the memory cells. EX-1012, 1:6-5:4; EX-1003, ¶¶196-197. A POSITA accordingly would have found it obvious to use Le's charge pump circuit in Asano's memory device as a design alternative to Asano's disclosed voltage boosting circuit, and would have had a reasonable expectation of success, as such modification would have been a combination of known techniques yielding predictable results. EX-1003, ¶¶196-197.

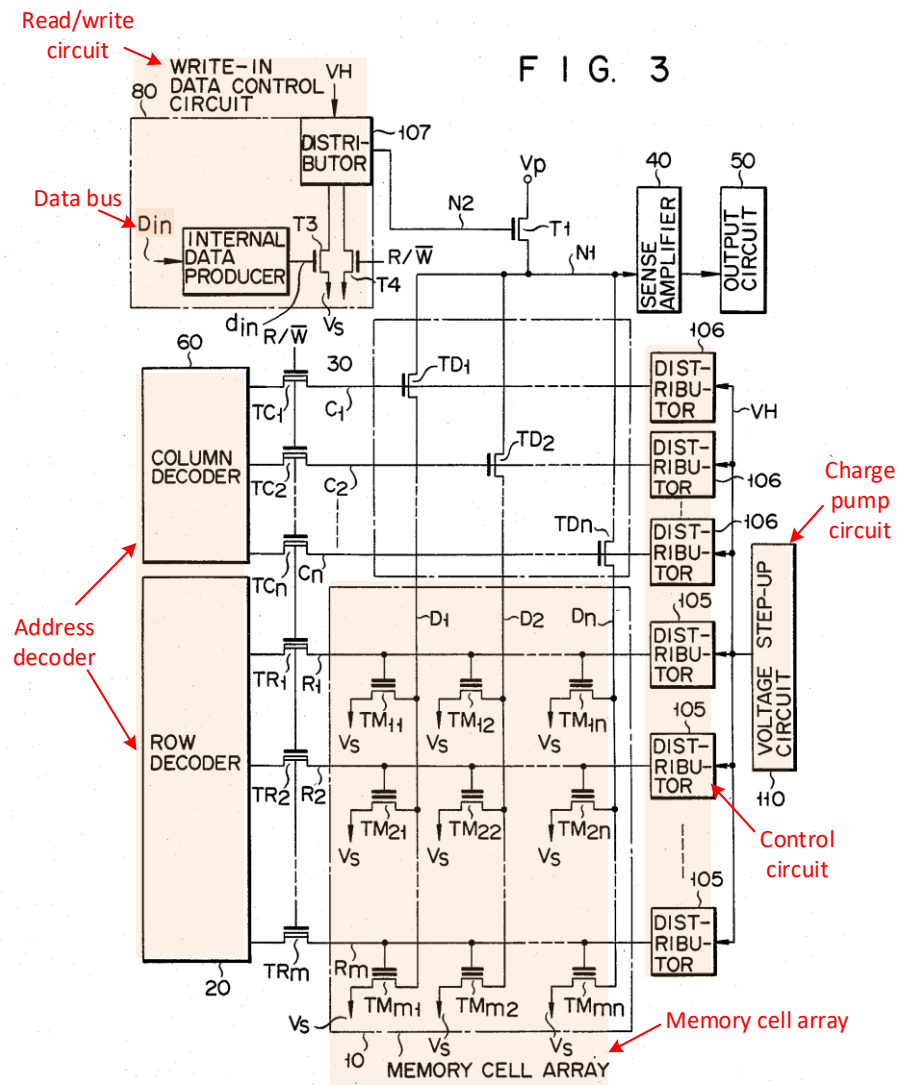
2. Claim 13

a) [13a]

Le, Ujiie and Kuriyama all disclose that their charge pump circuits are for use in memory devices. *See supra* §§III.C.1-2, III.D.1. A POSITA would have readily known that a memory device includes components recited in claim [13a].

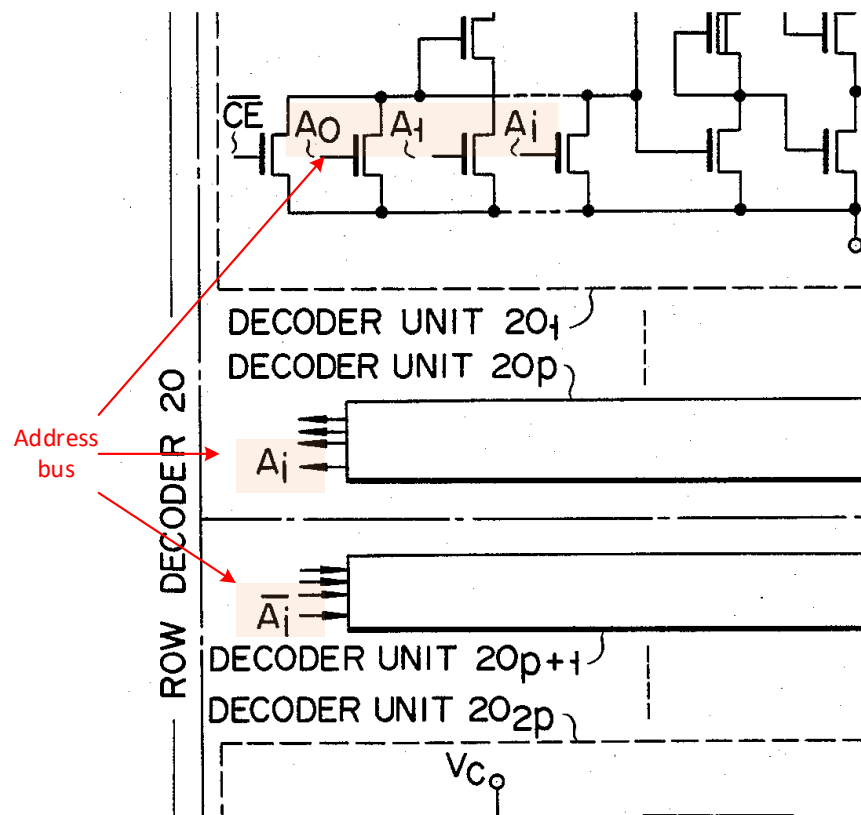
EX-1003, ¶198. For example, Asano discloses, with respect to FIG. 3, a memory system (“memory device”), which includes distributors 105, 106 (“control circuit”) that distribute the boosted voltage under control of a control signal. EX-1012, 6:4-64, FIG. 3 (reproduced below). The memory system also includes external input data Din (“data bus”); column decoder 60 and row decoder 20 (“address decoder”); write-in data control circuit 80 (“read/write circuit”), which receives external input data Din (“coupled to the data bus”); a memory cell array that is coupled to (i) column decoder 60 and row decoder 20 via transistors TC₁ to TC_n and TR₁ to TR_n (“coupled to the address decoder”), (ii) distributors 105 and 106 (“[coupled to] control circuit”), and (iii) the output port R/ $\bar{W}$ of write-in data control circuit 80 via transistors TC₁ to TC_n and TR₁ to TR_n (“[coupled to] read/write circuit”); and voltage set-up circuit 110 (“charge pump circuit”), which is coupled to (i) decoder 60 and row decoder 20 via distributors 105 and 106, transistors TC₁ to TC_n and TR₁ to TR_n (“coupled to the address decoder”), (ii) the output port R/ $\bar{W}$ of write-in data control circuit 80 via distributors 105 and 106 and transistors TC₁ to TC_n and TR₁ to TR_n (“[coupled to] read/write circuit”), and (iii) memory cell array via distributors 105 and 106 (“[coupled to] memory cell array”). *Id.*, 2:22-3:10; 6:4-8:59, FIGs. 3, 6, 10, 17A-17B. In FIG. 10, Asano shows that row decoder 20 is coupled to signals A₀, A₁, ... A_i, which read on the “address bus.” EX-1012, 2:22-

46, 16:54-17:31, FIGs. 10 (reproduced below), 17A-17B.³¹ See also EX-1003,
¶¶199-201.



EX-1012, FIG. 3 (annotated)

³¹ See n.14.



EX-1012, FIG. 10 (partial, annotated)

b) [13b]

Le discloses [13b]. *See supra* §III.C.3.(b); EX-1003, ¶202.

c) [13c]

Ujiie discloses [13c]. *See supra* §III.C.3.(c); EX-1003, ¶202.

d) [13d]

Ujiie discloses “a load selector means ... for selecting a load that satisfies a specific pump voltage”. *See supra* §III.C.3.(d). FIG. 3 of Ujiie also shows that switches Q1 and Q2 of the load selector means are coupled to the output of charge

pump 10 via diodes D1 and D2, respectively. EX-1009, FIG. 3. As an obvious modification of FIG. 3 of Ujiie, switches Q1 and Q2 may be coupled to the output of charge pump 10 without intervening diodes D1 and D2. *See supra* §III.C.3.(e); EX-1003, ¶202.

e) [13e]

Kuriyama discloses [13e]. *See supra* §III.D.2; EX-1003, ¶202.

f) [13f]

Kuriyama discloses [13f]. *See supra* §III.D.3; EX-1003, ¶202.

3. Claim 14

a) [14a]-[14b]

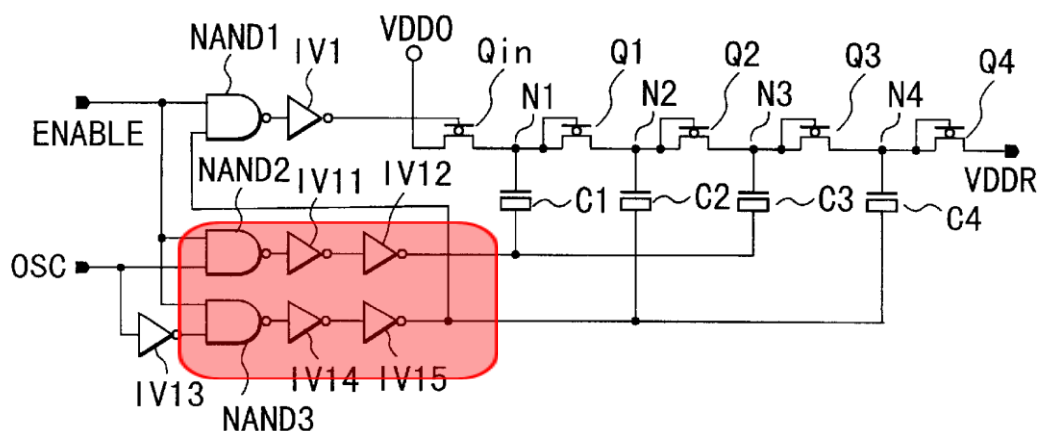
Le discloses [14a]-[14b]. *See supra* §§III.E.1.(a)-(b); EX-1003, ¶203.

b) [14c]

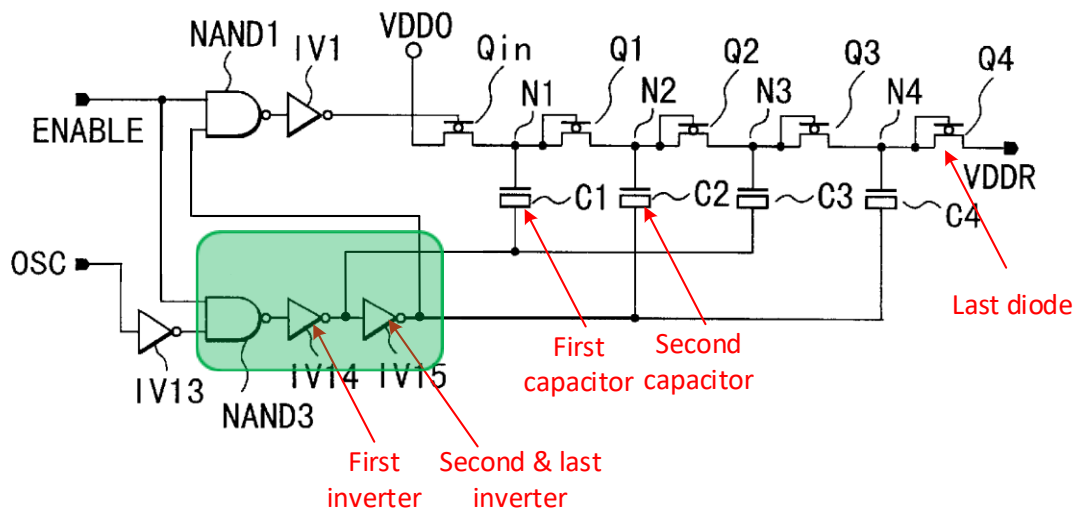
Le and Ujiie do not explicitly describe the circuit structure that generates clock signals in their respective charge pumps. *See supra* §III.E.1.(c). A POSITA would have been motivated to look at other references for description of a clock generator for charge pump circuits used in memory devices, and in doing so would have found the teaching in Kuriyama. *See supra* §III.D.1; EX-1003, ¶204.

A POSITA would have understood that this limitation is taught by a simple modification of FIG. 8 of Kuriyama, and would have found the modification

obvious because the circuits before and after the modification are logically equivalent. EX-1011, FIG. 8 (reproduced below); EX-1003, ¶204.



EX-1011, FIG. 8 (annotated)



EX-1011, FIG. 8 (modified, annotated)

In the modified circuit, the output terminal of inverter IV14 is coupled to the lower plate of capacitor C1 and to the input terminal of inverter IV15, forming a

first stage. EX-1003, ¶205. The output terminal of inverter IV15 is coupled to the lower plate of capacitor C2, forming a second stage. *Id.* The output terminal of inverter IV15 is also coupled to the last diode Q4 via capacitor C4. *Id.*

c) [14d]

Le discloses using an oscillator to generate a clock signal CLK and its inversion $\overline{\text{CLK}}$ as inputs to the capacitors (e.g., C_{0eff}, C_{1eff}, etc.) of charge pump circuit 300. EX-1008, FIGs. 3-4, 7:50-8:21. Kuriyama similarly discloses an oscillator that outputs signal OSC, which, after logic operations, becomes input signals to capacitors C1-C4. EX-1011, 7:63-8:6; *supra* §III.F.3.(b). In view of these teachings, a POSITA would have found it obvious to use a clock signal as the input to inverter IV14 of modified FIG. 8 of Kuriyama as a matter of design choice. EX-1003, ¶¶206-207. A POSITA would have had a reasonable expectation of success for this modification, as the operation of the resulting circuit would have been completely predictable. *Id.*

4. Claim 15

Le discloses claim 15. *See supra* §§III.C.1, III.E.2; EX-1003, ¶208.

5. Claim 16

Le-Ujiie discloses claim 16. *See supra* §III.C.4; EX-1003, ¶209.

6. Claim 17

Le-Ujiie discloses claim 17. *See supra* §III.C.5; EX-1003, ¶210.

7. Claim 19

Le-Ujiie discloses claim 19. *See supra* §III.C.7; EX-1003, ¶211.

8. Claim 21

a) [21a]-[21c]

Kuriyama discloses [21a]-[21c]. *See supra* §§III.D.4.(a)-(c); EX-1003, ¶212.

b) [21d]

A POSITA would have found it obvious that the load selector means in the charge pump circuit of Le-Ujiie includes Kuriyama's control circuit 114a. *See* §III.D.2. Kuriyama shows that the control circuit 114a includes R_{load} ("third resistor network"), which has the upper terminal coupled to the charge pump circuit 115a output. EX-1011, FIG. 14; EX-1003, ¶213.

c) [21e]

Kuriyama's control circuit 114a includes R_{ref} ("fourth resistor network"), which has the upper terminal coupled to the lower terminal of R_{load} ("the second terminal of the third resistor network"). EX-1011, FIG. 14. The lower terminal of R_{ref} is connected to ground. *Id.*; EX-1003, ¶213.

d) [21f]

Kuriyama's control circuit 114a includes comparator 121 ("second comparator") with two input terminals "+" and "-", and an output terminal connected to buffer 122. EX-1011, FIG. 14. Kuriyama discloses that the output of comparator 121 is "acquired as a charge-pumping enable signal CPENB via []buffer 122." *Id.*, 12:19-27. A POSITA accordingly would have found it obvious that the output terminal of comparator 121 reads on both the "output terminal" and the "enable terminal." EX-1003, ¶214.

With the understanding that "input terminal of the fourth resistor network" is one of the two terminals of the fourth resistor network,"³² Kuriyama shows that the "-" input of comparator 121 is connected to the upper terminal of R_{ref} while the "+" input of comparator 121 is connected to V_{ref} . EX-1011, FIG. 14; EX-1003, ¶214.

e) [21g]

Kuriyama's control circuit 114a includes buffer 122, which a POSITA would have readily understood as being a logic circuit. EX-1011, FIG. 14; EX-1003, ¶214. Buffer 122 has two terminals, one of which is coupled to comparator

³² See n.4.

121 (“second comparator”). EX-1003, ¶214.

9. Claim 22

a) [22a]

Le discloses [22a]. *See supra* §§III.E.1.(a)-(b); EX-1003, ¶216.

b) [22b]

Kuriyama renders [22b] obvious. *See supra* §III.F.3.(b); EX-1003, ¶216.

c) [22c]

Le-Kuriyama renders [22c] obvious. *See supra* §III.F.3.(c); EX-1003, ¶216.

10. Claim 23

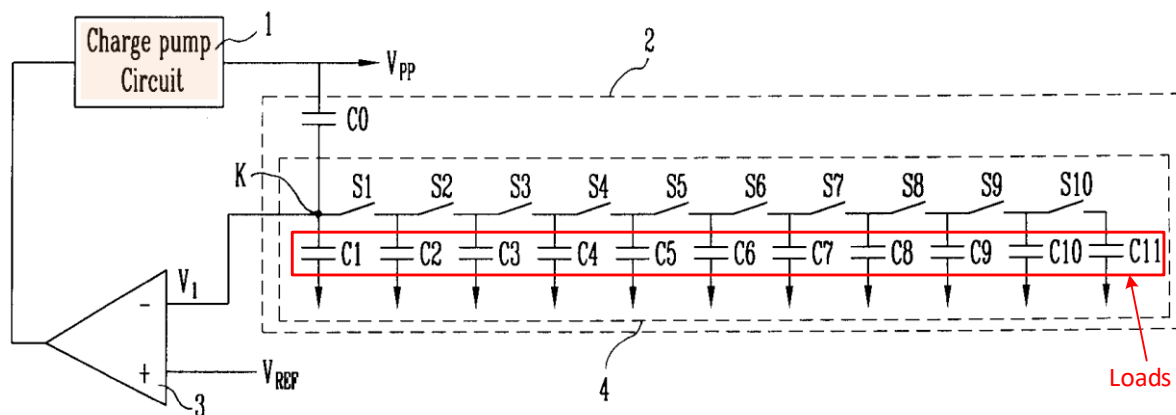
Le discloses that its charge pump circuit provides pump voltage for memory cells in flash memory array systems. EX-1008, 1:7-318, 4:31-5:33; EX-1003, ¶217.

G. GROUND 3B: Claims 18 and 20 are rendered obvious by Asano, Le, Ujiie, Kuriyama, and Yang

1. Overview of Yang

Yang discloses using a charge pump to generate voltages for memory devices with reduced voltage ripple. EX-1010, 1:7-59, 2:46-65, 4:39-51, FIG. 2 (reproduced below). The charge pump output is coupled to voltage divider circuit 2 comprising a capacitor block 4 with multiple capacitors, which a POSITA would have understood are loads in Yang’s charge pump circuit. *Id.*, FIG. 2; EX-1003,

¶219. These loads can be selectively coupled to the charge pump output by turning on one or more switches S1-S10. EX-1003, ¶219.



EX-1010, FIG. 2 (annotated)

Similar to Asano, Le, Ujiie, and Kuriyama, Yang discloses using charge pumps to provide regulated voltages for memory devices. EX-1010, 1:7-59. 4:39-51. A POSITA would have understood that Yang's voltage divider circuit can be used to realize Le's shunt regulator, or used to modify Ujiie's shunt circuit with additional capacitor stages, and accordingly would have been motivated to combine Asano, Le, Ujiie, Kuriyama, and Yang. EX-1003, ¶220.

2. Claim 18

Ujiie discloses that diodes D1 and D2, serving as loads of the charge pump, each has one terminal coupled to charge pump 10 output and the other terminal coupled to the drain of respective NMOS transistor Q1 and Q2. *See supra*

§§III.C.3.(c), III.C.6; EX-1003, ¶221.

In a similar context of regulating charge pump output voltage, Yang discloses a circuit with capacitors C1-C11 coupled between the output of charge pump circuit 1 and ground. EX-1010, FIG. 2. A POSITA would have understood that capacitors C1-C11 serve as “loads” to regulate the output of charge pump circuit 1. EX-1003, ¶222. In view of this teaching of Yang, a POSITA would have found it obvious that a shunt regulator can use capacitors in lieu of diodes as loads, and would have been motivated to modify the shunt regulator of Ujiie to use capacitors as loads, thereby rendering claim 18 obvious. *Id.* A POSITA would have had a reasonable expectation of success for this modification, as the operation of the resulting circuit would have been predictable. *Id.*

3. Claim 20

A POSITA would have found it obvious to modify Ujiie’s shunt regulator such that diodes D1 and D2 (“load”) each has one terminal coupled to the source of respective switch Q1 and Q2, and the other terminal coupled to ground. *See supra* §III.C.4; EX-1003, ¶223.

A POSITA would also have known that capacitors can be loads, and would have found it an obvious design choice to use capacitors in lieu of diodes as loads of the shunt regulator, such as loads in the modified shunt regulator circuit of Ujiie

as noted above, thereby rendering claim 20 obvious. *See supra* §III.G.2; EX-1003, ¶224.

IV. INSTITUTION IS APPROPRIATE HERE

A. 35 U.S.C. §325(d) – *Advanced Bionics*

Advanced Bionics and the *Becton* factors strongly favor institution. *Advanced Bionics LLC v. MED-EL Elektromedizinische Gerate GmbH*, IPR2019-01469, Paper 6 (PTAB Feb. 13, 2020) (“*Advanced Bionics*”) (precedential); *Becton, Dickinson and Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (PTAB Dec. 15 2017) (“*Becton*”) (precedential).

The examiner never issued a rejection during the ’241 Patent’s prosecution. *See, generally*, EX-1002. Of the references applied in this Petition, Le was cited by the Applicant to the Office, but there is no indication that the examiner substantively considered Le. *Id.*, 106-110. None of the other references in this Petition were cited during prosecution. *Id.* Because the prosecution did not involve negotiation between the Applicant and the examiner regarding the prior art teachings applied in the Petition, the Petition’s art and arguments cannot be said to be the same as, or substantially similar to, art and arguments previously presented to the Office in connection with the ’241 Patent. *Id.* Accordingly, neither condition of the first prong of the *Advanced Bionics* framework is met, and there is

no need to reach the second prong to resolve against discretionary denial under Section 325(d). *See, e.g., Oticon Medical AB et. al. v. Cochlear Ltd.*, IPR2019-00975, Paper 15 at 20 (PTAB Oct. 16, 2019) (precedential) (no discretionary denial under §325(d) because of “new, noncumulative prior art asserted in the Petition”).

Moreover, the Challenged Claims were allowed based on the Examiner’s mistaken view that the prior art failed to “disclose a charge pump with a selectable voltage output and a selectable load wherein a load is selected so as to minimize output ripple for a given output voltage.” EX-1002, 107. As demonstrated in this Petition with reference to Dr. Dickens’ testimony, the examiner’s failure to consider obviousness of the Challenged Claims over the uncited Doluca, Buti, Hosono, Kuriyama, Asano and Yang references constitutes material error. For at least this additional reason, Petitioner respectfully submits that discretionary denial is unwarranted, and that the Board should instead institute IPR based on the instant Petition’s grounds.

B. The General Plastic Factors Weigh Against Exercising Discretion To Deny Institution

The ’241 Patent was the subject of IPR2021-01561 (filed 9/22/2021, instituted 3/23/2022, terminated 1/4/2023) involving different petitioners,

separately and independent of Petitioner. IPR2021-01561 was terminated due to settlement. The present Petition relies on combinations of references not previously asserted.

In *General Plastic Industrial Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357—01361, Paper 19 at 9-10 (PTAB Sept. 6, 2017) (precedential), the Board identified seven factors that inform application of discretionary institution denials under 35 U.S.C. §314(a). Evaluation of these factors weighs against using the Board’s discretion to deny this Petition without consideration on the merits, especially where the present Petitioner is different from the petitioners in the earlier-filed IPR. See, e.g., *Acronis, Inc., v. Realtime Data LLC*, IPR2018-00706, Paper 11, 15-16 (Oct. 1, 2018) (citing *Alcatel-Lucent USA Inc. v. Oyster Optics, LLC*, IPR2017-02146, Paper 12, 12 (Feb. 28, 2018)) (“Once resolution of factor 1 indicates that Petitioner had not previously filed a petition against the same patent, factors 2–5 bear little relevance unless there is evidence in the record of extenuating circumstances.”).

1. Factor 1

Factor 1 weighs heavily in favor of considering this Petition on the merits because Petitioner has not filed any petition challenging the ’241 Patent. Concerns of strategically staging petitions “have less persuasive value when the second

petition is filed by a different petitioner.” *Toshiba America Information Systems v. Wallex Microelectronics LTD.*, IPR2018-01538, Paper 11, 20 (March 5, 2019); *Acronis*, Paper 11, 15-16. There is no control or cooperation in the IPRs between Petitioner and the earlier petitioners; they remain “distinct parties, with ultimately distinct interests, and distinct litigation strategies,” and are “often competitors in the marketplace.” *Id.* at 22. Deciding this petition on the merits would not be unfair to Patent Owner, but discretionarily denying institution of the only petition by Petitioner would be unfair to Petitioner, especially considering that the prior IPR was terminated before a final written decision.

2. Factors 2, 4, and 5

Factors 2, 4, and 5 do not weigh against consideration of this Petition. Petitioner learned of Buti, Kuriyama, Asano and Yang through prior art searching conducted in November 2022-March 2023. Upon discovering these references, Petitioner worked diligently to file this Petition.

3. Factor 3

Factor 3 does not weigh against consideration of this Petition because Petitioner did not delay filing this petition for the purpose of using an earlier proceeding as a roadmap. Indeed, the Board previously did not identify any flaws or concerns with the arguments raised in the prior petition, hence there were no

“lessons” derived from the prior institution decision. Further, because the present Petition relies on references and combinations of references not asserted in the previous petitions, Petitioner derived no benefit.

4. Factors 6 and 7

Factors 6 and 7 weigh in favor of considering this Petition when considering the limited resources of the Board, balanced against the usefulness of invalidating patents in view of the relevant prior art cited here. Indeed, the previous IPR terminated due to settlement after the Board instituted review but before it analyzed on the merits in a final written decision, so the present Petition is now the only IPR before the Board, thus providing for efficient resolution of the unpatentability of the '241 Patent within one year after institution. This is especially the case where there is no evidence of prejudicial “road-mapping” or other gamesmanship by Petitioner that would warrant the punitive measure of denial without consideration on the merits, where there is no other IPR pending against the '241 Patent.

The public interest also favors considering this Petition on the merits in view of the highly pertinent reference combinations that were never previously considered by the Office. There is no prejudice to Patent Owner here because this petition and the earlier-filed petition against the '241 Patent are “a directed result

of [Patent Owner's] own litigation activity.” *Samsung Electronics America, Inc. et al v. Uniloc 2017 LLC*, IPR2017-01797, Paper 8, 33 (February 6, 2018).

Because Petitioner filed a single petition against the '241 Patent and has a meaningful due process interest to be heard in this forum on the merits in light of the termination of the earlier IPR proceeding against the '241 Patent, the *General Plastic* factors weigh in favor of instituting IPR.

Additionally, while concurrent district court litigation involving the '241 Patent is ongoing, it remains at an early phase, with the complaint having only been filed in August 2022. Petitioner has worked diligently to identify and apply prior art discussed herein to file the Petition. Additionally, Dr. Dickens provides significant evidence not of record in the district court.

C. The *Fintiv* Factors Weigh Against Exercising Discretion To Deny Institution

The PTAB considers a set of non-exclusive factors (the *Fintiv* factors) in determining whether to institute an IPR proceeding where there is parallel district court litigation. *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential). On June 21, 2022, Director Vidal issued “binding agency guidance” which presents “several clarifications... to the PTAB's... application of *Fintiv* to discretionary institution where there is parallel litigation.”

EX-1021, 2.

One clarification provided by this Interim Guidance specifies the effect of particular types of stipulations presented by petitioners on the Board's application of the *Fintiv* framework. *Id.*, 3, 7-8. In particular, the Interim Guidance unequivocally states that “**the PTAB will not discretionarily deny institution** of an IPR or PGR in view of parallel district court litigation where a petitioner stipulates not to pursue in a parallel district court proceeding the same grounds as in the petition or any grounds that could have reasonably been raised in the petition.” *Id.*, 7 (emphasis added) (citing *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (PTAB Dec. 1, 2020)). In the present case, Petitioner presents a stipulation not to pursue in the parallel district court proceeding the same grounds as in the present Petition or any grounds that could have reasonably been raised in the present Petition. *See* EX-1022. Accordingly, based on the Interim Guidance, institution of the present Petition **should not** be discretionarily denied in view of the parallel district court proceeding. *See* EX-1021, 7.

V. PAYMENT OF FEES

Petitioner authorizes the Patent and Trademark Office to charge Deposit Account No. 06-1050 for the fee set in 37 C.F.R. § 42.15(a) for this Petition and further authorizes payment for any additional fees to be charged to this Deposit

Account.

VI. CONCLUSION

Petitioner respectfully requests institution of an IPR for the Challenged Claims.

VII. MANDATORY NOTICES UNDER 37 C.F.R § 42.8(a)(1)

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)

Micron Technology, Inc. is the Real Party-in-Interest in this proceeding.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

Petitioner is not aware of any disclaimers or reexamination certificates. PO has asserted the '241 Patent against Petitioner in district court in litigation *Sonrai Memory Ltd. v. Micron Technology Inc.*, Case No. 6:22-CV-00855-FB (W.D. Tex.).

PO has also asserted the '241 Patent in the following litigation matters:

- *Sonrai Memory Ltd. v. Apple Inc.*, Case No. 6:22-cv-00787 (W.D. Tex.);
- *Sonrai Memory Ltd. v. Google LLC*, 6-22-cv-00336 (W.D. Tex.);
- *Sonrai Memory Ltd. v. Amazon.Com, Inc.*, 6-22-cv-00225 (W.D. Tex.);
- *Sonrai Memory Ltd. v. Samsung Electronics Co., Ltd. et al*, 6-22-cv-00189 (W.D. Tex.);
- *Sonrai Memory Ltd. v. Dell Technologies, Inc.*, 6-22-cv-00188 (W.D. Tex.);

- *Sonrai Memory Ltd. v. Kingston Technology Company, Inc. et al*, 6-22-cv-00192 (W.D. Tex.);
- *Sonrai Memory Ltd. v. Kingston Technology Company, Inc. et al*, 6-21-cv-01284 (W.D. Tex.);
- *Sonrai Memory Ltd. v. Western Digital Technologies, Inc.*, 6-21-cv-01168 (W.D. Tex.);
- *Sonrai Memory Ltd. v. Amazon.com, Inc.*, 6-21-cv-00991 (W.D. Tex.);
- *Sonrai Memory Ltd. v. Dell Technologies, Inc.*, 1-22-cv-00487 (W.D. Tex.);
- *Sonrai Memory Ltd. v. Kioxia Corp. and Kioxia Am., Inc.*, Case No. 6:21-cv-00400-ADA (W.D. Tex.);
- *Sonrai Memory Ltd. v. Western Digital Corp.*, Case No. 8:21-cv-1040-CJC (C.D. Cal.);
- *Sonrai Memory Ltd. v. Dell Tech., Inc.*, Case No. 6:21-cv- 00361-ADA (W.D. Tex.);
- *Sonrai Memory Ltd. v. Google LLC*, Case No. 6:21-cv-00167- ADA (W.D. Tex.);
- *Sonrai Memory Ltd. v. Kingston Technology Company, Inc. and Kingston Tech. Corp.*, Case No. 8:21-cv-1039-CJC (C.D. Cal.);
- *Sonrai Memory Ltd. v. Samsung Electronics Co., and Samsung Elect. Am.*,

Inc., Case No. 6:21-cv-00169-ADA (W.D. Tex.);

- *Sonrai Memory Ltd. v. Apple Inc.*, Case No. 6:21-cv-00401- ADA (W.D. Tex.); and
- *Sonrai Memory Ltd. v. LG Elec. Inc. and LG Electronics U.S.A., Inc.*, Case No. 6:21-cv-00168-ADA (W.D. Tex.).

C. Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel.

Lead Counsel	Backup counsel
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D. Service Information

Please address all correspondence and service to the address listed above.

Petitioner consents to electronic service by email at IPR36144-0035IP2@fr.com.

Respectfully submitted,

Dated: May 8, 2023

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CERTIFICATION UNDER 37 CFR § 42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter partes* Review totals 13,987 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated: May 8, 2023

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on May 8, 2023, a complete and entire copy of this Petition for *Inter partes* Review and all supporting exhibits were provided via USPS, to the Patent Owner by serving the correspondence address of record as follows:

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