

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY INC.,

Petitioner,

v.

SONRAI MEMORY LIMITED,

Patent Owner.

Case IPR2023-00909

Patent 6,724,241

PATENT OWNER’S PRELIMINARY RESPONSE

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PATENT OWNER’S EXHIBIT LIST

Exhibit No.	Description
2001	Plaintiff’s Notice of IPR Petition, <i>Sonrai Memory Limited v. Micron Technology, Inc.</i> , No. 6:22-cv-0085-ADA, Dkt. No. 40 (W.D. Tex. May 22, 2023)
2002	Order Granting Motion for Entry of Scheduling Order, <i>Sonrai Memory Limited v. Micron Technology, Inc.</i> , No. 6:22-cv-0085-ADA, Dkt. No. 40 (W.D. Tex. May 22, 2023)
2003	Docket Sheet, <i>Sonrai Memory Limited v. Micron Technology, Inc.</i> , No. 6:22-cv-0085-ADA (W.D. Tex. Sept. 10, 2023)
2004	Law360 Article: <i>West Texas Judge Says He Can Move Faster Than PTAB</i>
2005	Order Granting Joint Motion for Extension of Time To Extend Venue Discovery and Claim Construction Deadlines, <i>Sonrai Memory Limited v. Micron Technology, Inc.</i> , No. 6:22-cv-0085-ADA, Dkt. No. 51 (W.D. Tex. Aug. 3, 2023)
2006	Text Order Denying Motion to Stay Pending IPR, <i>Solas OLED Ltd. v. Google, Inc.</i> , Case No. 6:19-cv-00515-ADA (W.D. Tex. June 23, 2020)
2007	Order Denying Motion to Stay Pending IPR, <i>Multimedia Content Management LLC v. DISH Network L.L.C.</i> , Case No. 6:18-cv-00207-ADA, Dkt. No. 73 (W.D. Tex. May 30, 2019)
2008	U.S. District Courts—Federal Court Management Statistics—Profiles—During the 12-Month Periods Ending June 30, 2018 Through 2023 available at https://www.uscourts.gov/statistics/table/na/federal-court-management-statistics/2023/06/30-1
2009	Micron Technology, Inc’s Preliminary Invalidity Contentions, <i>Sonrai Memory Limited v. Micron Technology, Inc.</i> , No. 6:22-cv-0085-ADA (W.D. Tex. June 7, 2023)

Exhibit No.	Description
2010	Amended Scheduling Order, <i>Sonrai Memory Limited v. Apple Inc.</i> , No. 6:22-cv-00787-ADA, Dkt. No. 79 (W.D. Tex. Sept. 5, 2023)
2011	Claim Construction Order, <i>Sonrai Memory Limited v. Apple Inc.</i> , No. 6:22-cv-00787-ADA, Dkt. No. 53 (W.D. Tex. Apr. 6, 2023)
2012	Apple Inc.'s First Supplemental Invalidity Contentions, <i>Sonrai Memory Limited v. Apple Inc.</i> , No. 6:22-cv-00787-ADA (W.D. Tex. June 15, 2023)

I. INTRODUCTION

Patent Owner Sonrai Memory Ltd. (“Patent Owner”) submits this preliminary response to Petitioner Micron Technology Inc.’s (“Petitioner”) Petition for *inter partes* review of U.S. Patent No. 6,724,241 (“the ’241 patent”).

First, the Board should deny institution because Petitioner fails to establish a reasonable likelihood of invalidity for any independent claim.¹ The independent claims recite either “a pumping circuit” that “generate[s] a selected one of a plurality of pump voltages” (independent claim 1) or that “generate[s] one or more pump voltages” (independent claim 13), or a method for generating an output voltage in “a charge pump circuit” that includes “selecting a output pump voltage (V_{pump})” (independent claim 24). Petitioner asserts that either *Doluca* alone, *Doluca* in combination with *Buti*, or *Le* alone discloses these claim limitations. However, neither *Doluca* alone, *Doluca* in combination with *Buti*, nor *Le* alone disclose charge pumps that generate multiple output voltages. Consequently, Petitioner cannot establish that the limitations of “generat[ing] a selected one of a

¹ The Petition asserts invalidity of the independent claims in Ground 1A (addressing independent claims 1 and 24 under the combination of *Doluca* and *Buti*), Ground 1B (addressing independent claim 13 under the combination of *Doluca*, *Buti* and *Hosono*), Ground 2A (addressing independent claim 1 under the combination of *Le* and *Ujiie*), Ground 2B (addressing independent claim 24 under the combination of *Le*, *Ujiie* and *Kuriyama*), and Ground 3A (addressing independent claim 13 under the combination of *Asano*, *Le*, *Ujiie* and *Kuriyama*). Grounds 2C and 3B only address dependent claims.

plurality of pump voltages” (independent claim 1) or that “generat[ing] one or more pump voltages” (independent claim 13), or that “selecting a output pump voltage (V_{pump})” (independent claim 24), are satisfied by the prior art and therefore cannot establish a reasonable likelihood of invalidity.

Second, the Board should also exercise its discretion to deny the petition under 35 U.S.C. § 314(a) in light of a parallel district court case involving overlapping claims and the same patent, prior art, and parties. By the time the Board reaches an institution decision in this proceeding, the parties and the district court will have already invested significant time and resources in the case which was filed on August 16, 2022 – over a year ago and more than fifteen months before the institution decision is due. Claim construction briefing is ongoing and a Markman hearing is currently scheduled for October 27, 2023. By the date of the institution decision, the parties will have nearly completed fact discovery. A Final Written Decision will not be due until three (3) months *after* trial is set to begin on September 18, 2024, and five (5) months after trial is set to begin in the parallel district court case involving Apple. The *Fintiv* factors strongly favor a discretionary denial.

Third, 35 U.S.C. § 314(a) also gives the Board discretion to deny instituting “follow on” petitions. *General Plastic Indus. Co. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 (Sept. 6, 2017) (precedential). A previous petition was

filed against the '241 patent before this one – IPR2021-01561 (filed September 22, 2021, instituted March 23, 2022). As discussed below, five *General Plastic* factors weigh against institution and two factors are neutral. Under § 314(a) and the totality of *General Plastic* factors, institution should be denied.

Accordingly, the Board should deny institution.

II. OVERVIEW OF *DOLUCA* AND *LE*

A. *Doluca*

U.S. Patent No. 4,769,784 to Doluca et al. (“*Doluca*”) generally describes a charge pump circuit “to produce a capacitor-plate bias voltage suitable for use in a CMOS DRAM using a $V_{CC}/2$ sense scheme.” Ex. 1006, 1:64-66. *Doluca* describes the capacitive memory cell with respect to Fig.1, reproduced below. “A capacitive memory element 3 has an anode electrode 5 and a cathode electrode 7. Cathode 7 is connected to a storage node 9, while anode electrode 5 is connected, in common with the anodes of the other capacitive memory elements in the matrix-array memory device (not shown) of which cell 1 is a part, to a capacitor-plate node 11.” *Id.*, 2:66-3:5.

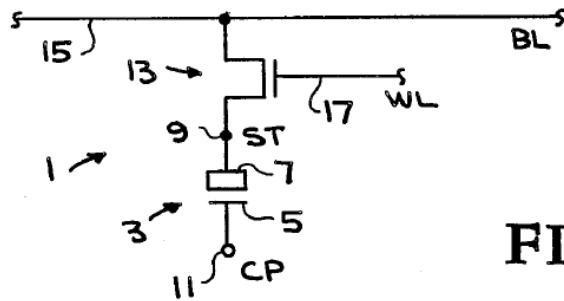


FIG. 1

Id., Fig. 1. At the storage node 9, logic level 0 is represented by 0 volts and logic level 1 is represented by V_{CC} . *Id.*, 3:11-13.

The “[c]apacitor 3 is formed with a silicon cathode, a polysilicon anode, and with a relatively thin dielectric layer of, for example, 150 Angstroms of SiO_2 separating its cathode and anode.” *Id.*, 3:17-20. The capacitive structure has a threshold voltage V_T , depending on temperature, of approximately 0.4 to 1.0 volts. *Id.*, 3:20-22. “Consequently, the capacitor-plate node 11 must always be held at a voltage which is more positive than the voltage of the storage node 9 by V_T volts or more.” *Id.*, 3:22-25. This means that the capacitor voltage must always be held at $V_{CC} + V_T$ volts. With V_{CC} at 5V and V_T at 1V, the capacitor voltage must be held at more than 6V.

With further reference to Fig. 1, *Doluca* describes the “ $V_{CC}/2$ sense scheme,” where the bit-line 15 is pre-charged to $V_{CC}/2$, the midpoint between zero volts and V_{CC} , prior to connecting to the storage node 9 through word-line 17 controlled transistor 13. *Id.*, 3:13-16. *Doluca* further discloses that the capacitor plate voltage

can defined in terms of $V_{CC}/2$. *See id.*, 3:35-38 (“[S]ince the bit-line pre-charge voltage is $V_{CC}/2$, the voltage of the capacitor-plate bias source should be function of $V_{CC}/2$ such that it follows any variations of bit-line voltage exactly.”). “Taking these requirements together, we can say that the ideal capacitor-plate bias source should produce a voltage: $V_{CP} = V_{CC}/2 + K$, where K is a constant having a value: $K > V_{CC}/2 + V_T$.” *Id.*, 3:39-45.

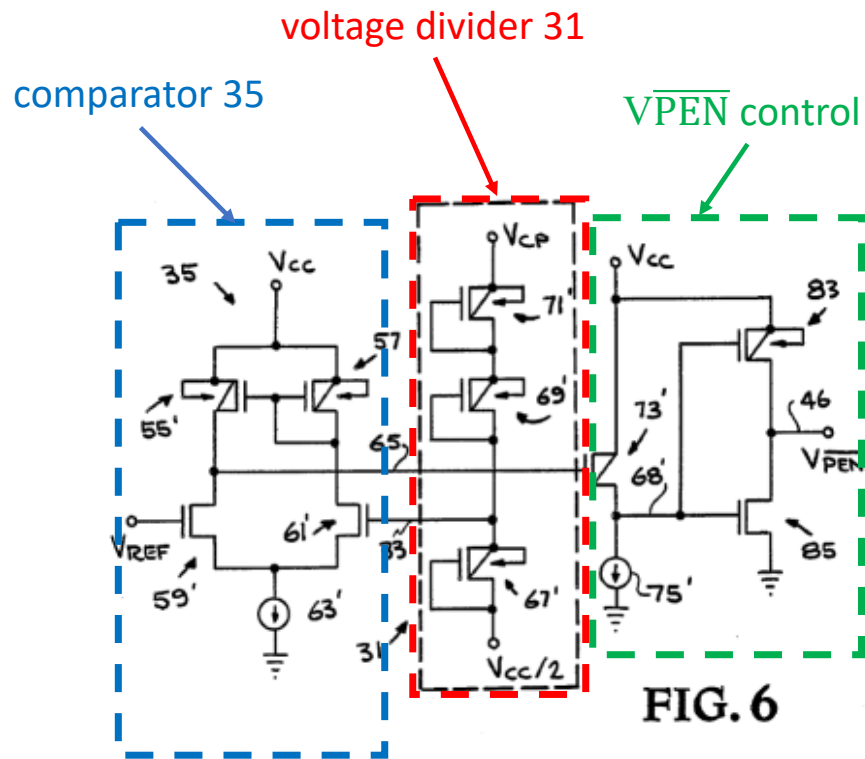
With V_{CC} at 5V and V_T at 1V, K must be greater than 3.5V. *Doluca* suggests “that K might be chosen to be 3.5 to 4, resulting in a value of V_{CP} of approximately 6 to 6.5 volts.” *Id.*, 49-50. This provides some flexibility in generating V_{CP} . Notably, *Doluca* does not describe generating K , but rather describes circuitry that achieves the minimum required capacitor plate voltage based on V_{CC} and the bandgap voltage of silicon, V_{BG} . The circuitry first consists of “[a] $V_{CC}/2$ circuit 21, which may be nothing more than a voltage divider, connects to a source of voltage V_{CC} at its input, and provides a voltage $V_{CC}/2$ to a V_{BG} generator 23 at its output. V_{BG} generator 23 generates a voltage V_{BG} which is a stable facsimile of the bandgap voltage of silicon, or about 1.2 volts.” *Id.*, 3:62-67. “The output of generator 23, consisting of the sum of $V_{CC}/2$ and V_{BG} is connected to a V_{REF} line 25, such that: $V_{REF} = V_{CC}/2 + V_{BG}$.” *Id.*, 4:4-8.

The circuitry also consists of a typical charge pump circuit, shown in Fig. 3. The charge pump is enabled by the signal $\overline{VPEN}$. Finally, the circuitry also includes

the pump control circuit 29, shown in Fig. 6, reproduced below. The pump control circuit further consists of voltage divider circuitry 31 that produces an output on line 33 of $V_{33} = (V_{CP} - V_{CC}/2)/3 + V_{CC}/2$. *See id.*, Fig. 6 (portion highlighted in red below). V_{33} is compared to V_{REF} in comparator 35 circuitry, *see id.*, Fig. 6 (portion highlighted in blue below):

The output of comparator 35 on line 65' goes low whenever V_{33} drops below V_{REF} , and this low output is coupled through a driver transistor 73' to the commonly connected gates of an inverting output pair of transistors 83 and 85. The high voltage on the common gate connection of these transistors turns transistor 83 off, and transistor 85 on. As a result, the output voltage on the line 46 drops, initiating the active low $\overline{VPEN}$ output signal on line 46.

Id., 7:15-23, Fig. 6 (portion highlighted in green below).

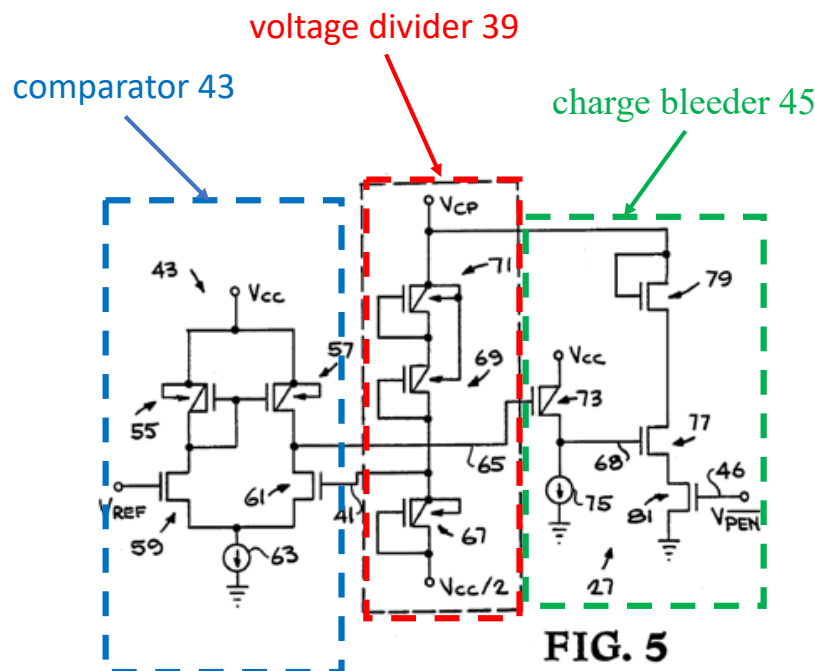


Id., Fig. 6 (annotated).

In other words, the charge pump is activated when: $(V_{CP} - V_{CC}/2)/3 + V_{CC}/2 \leq V_{CC}/2 + V_{BG}$. Simplifying further, the charge pump is activated when: $(V_{CP} - V_{CC}/2)/3 \leq V_{BG}$. Simplifying yet even further, the charge pump is activated when: $V_{CP} - V_{CC}/2 \leq 3V_{BG}$. Isolating V_{CP} , the charge pump is activated when: $V_{CP} \leq 3V_{BG} + V_{CC}/2$. *See id.*, 4:30-51. With V_{CC} at 5V and V_{BG} at 1.2V, the charge pump is activated when V_{CP} is less than or equal to 6.1V, in excess of $V_{CC} + V_T$. Because *Doluca* requires the charge pump circuitry to produce at least $V_{CP} = V_{CC}/2 + K$, and because the charge pump circuitry produces at least $V_{CP} = V_{CC}/2 + 3V_{BG}$, *Doluca* describes the “design criteria” of K as satisfied by $3V_{BG}$. That is, the design criteria is satisfied in *Doluca*’s circuitry using the fixed structures of (i) the circuitry to generate V_{BG} at 1.2V; and (ii) the voltage divider circuitry to generate $(V_{CP} - V_{CC}/2)/3 + V_{CC}/2$. *Doluca* consequently describes only generating a single V_{CP} output voltage.

Because a POSITA would recognize that the V_{CP} generated by the charge pump circuit will overshoot 6.1V due, *inter alia*, to transistor switching delays in disabling the charge pump, *Doluca* also describes a charge bleeder control circuit 27, shown in Fig. 5, reproduced below, for maintaining an approximate upper boundary to which V_{CP} will overshoot. Similar to the pump control circuit 29, the bleeder control circuit includes voltage divider 39. *See id.*, Fig. 5 (portion

highlighted in red below). However, this voltage divider differs from the voltage divider of the pump control circuit 29 in that the source of transistors 69 is connected to the substrate of transistor 71 instead of in its normal manner as with transistor 67 and 71, as well as with all of the transistors in the voltage divider 31 of pump control circuit 29. *See id.*, 6:36-41. “The effect of this asymmetry is to cause the voltage drop across transistor 69 to be increased by a small amount while the voltage drop across each of the other transistors is decreased by a small amount ... If we arbitrarily call the increase in the voltage across transistor 69 2Δ , then the decrease in drop across each of the other transistors is one half of this amount, or Δ . Consequently, the voltage output from divider 39 at line 41 is:

$$V_{41} = [(V_{CP} - V_{CC}/2)/3] + V_{CC}/2 - \Delta,” \text{ } Id., 6:41-51.$$


Id., Fig. 5 (annotated).

The output on line 41 (V_{41}) is compared to V_{REF} in comparator 43. *See id.*, Fig. 5 (portion highlighted in blue above). When V_{41} is greater than V_{REF} and $\overline{VPEN}$ is inactive (*i.e.*, logical 1 meaning the charge pump is not enabled), transistor 73 causes transistor 77 to allow current to flow through current-regulating transistor 79 and transistor 81 to ground. This bleeds charge, and consequently voltage, from V_{CP} . *See id.*, Fig. 5 (portion highlighted in green above).

In other words, the charge bleeder is activated when the charge pump is inactive and: $(V_{CP} - V_{CC}/2)/3 + V_{CC}/2 - \Delta \geq V_{CC}/2 + V_{BG}$. Simplifying further, the charge bleeder is activated when the charge pump is inactive and: $(V_{CP} - V_{CC}/2)/3 - \Delta \geq V_{BG}$. Simplifying yet even further, the charge bleeder is activated when the charge pump is inactive and: $V_{CP} - V_{CC}/2 - 3\Delta \geq 3V_{BG}$. Isolating V_{CP} , the charge bleeder is activated when the charge pump is inactive and: $V_{CP} \geq 3V_{BG} + V_{CC}/2 + 3\Delta$. *See id.*, 4:52-5:8. With V_{CC} at 5V, V_{BG} at 1.2V, and Δ a small offset voltage, the charge bleeder is activated when the charge pump is inactive and V_{CP} is greater than or equal to 6.1V plus a small offset voltage (trebled).

Doluca's circuits avoid simultaneous operation of the charge pump and the charge bleeder: “(1) the voltage V_{CP} at which the bleeder turns off is greater than the voltage V_{CP} at which the pump turns on by 3Δ ; (2) the $\overline{VPEN}$ voltage produced by comparator 35 is fed back along line 46 to bleeder control circuit 27, where it

disables charge bleeder 45 whenever charge pump 37 is in operation.” *Id.*, 5:13-19.

This allows VCP to maintain a range close to $6.1V$ to $6.1V + 3\Delta$.

B. *Le*

U.S. Patent No. 6,424,570 to Le et al. (“*Le*”) generally describes a charge pump circuit for generating a single output voltage as precisely as possible by accounting for variations in the input V_{CC} power supply by varying the capacitance values within the capacitor networks of the charge pump circuits.

Le describes the prior art charge pump circuits as having “large capacitor values to accommodate the lowest power supply level, and the addition of a shunt regulator 270 attached at the conventional point of the charge pump output 280, to reduce the output when the supply or the output voltage is higher than a target value.” Ex. 1008, 3:7-12. “The shunt regulator 280 regulates the charge pump output by partially shorting to ground that portion of the charge pump output which is greater than a desired voltage level. In this conventional method, large capacitor values may be used to compensate for the lowest power supply voltage.” *Id.*, 3:32-36. Due to higher capacitor values to accommodate for lowest supply voltage levels, “the output of the charge pump 280 and the shunt regulator 270 experience a ripple voltage signal from the charge and discharge cycles, with a period which matches the clock cycle period. The ripple voltage level on the output rises during a charge cycle, and drops again as a function of the RC discharge of the load and the load capacitance

CLOAD 260.” *Id.* 3:41-47. “The ripple voltage level rises during the charge cycle, until the shunt regulator determines that an over-voltage condition or target regulation voltage has been reached, wherein the shunt regulator shunting transistors begin to conduct and shunt the over-voltage charge to ground.” *Id.* 3:47-51. *Le* further describes “shunting transistors,” *see id.*, 3:53-54, not unlike the charge bleeder described by *Doluca*. *See* Section II.A, *supra*.

Le further describes the problems with the conventional approach, including “increased ripple magnitude (e.g., about 400 mV P-P ripple at about 9 volt output) at the output 280 when the input supply voltage 210 is high,” *id.*, 3:60-62, and the “noise spikes and valleys ... produced on the output 280 as the shunting transistors in the shunt regulator 270 discharge the over-voltage on the charge pump capacitors to ground,” *id.*, 3:63-66. *Le* consequently introduces a “novel charge pump circuit where one or more individual stages of the charge pump is characterized by having a variable bootstrap capacitance value which is varied as a function of the input supply voltage.” *Id.*, 4:31-35. “An advantage ... is the ability of the charge pump and shunt regulator system to produce a lower noise output, as compared to conventional charge pump and regulator systems without compensation.” *Id.*, 4:60-63.

Le introduces a V_{CC} input supply voltage detection circuit and a charge pump compensation circuit to modulate the capacitive loading of the charge pump:

Referring now to the figures, FIG. 3 is a simplified schematic illustration of an exemplary system 300, according to the present invention, for generating a modulated charge pump voltage VOUT 310 for flash memory cell operations, comprising **a supply voltage detection circuit 365 configured to detect a supply voltage value 380 and generate one or more output signals 370 associated therewith.** The system 300 further includes a charge pump circuit 305 comprising one or more stages operable to receive the supply voltage 380 and generate the charge pump output voltage VOUT 310 having a value greater than the supply voltage 380, and **a charge pump compensation circuit 390, operably coupled to the supply voltage detection circuit 365 and the charge pump circuit 305, and operable to receive the one or more output signals 370 from the supply voltage detection circuit 365 and modulate a capacitive loading (320, 330, 340, 350) associated with the charge pump circuit 305 based on the one or more supply voltage detection output signals 370.** Such modulation produces a low power consumption charge pump, which generates a low ripple and low noise output VOUT 310 which compensates for fluctuations of the input power supply (for example, VCC).

Id. 7:4-25 (emphasis added).

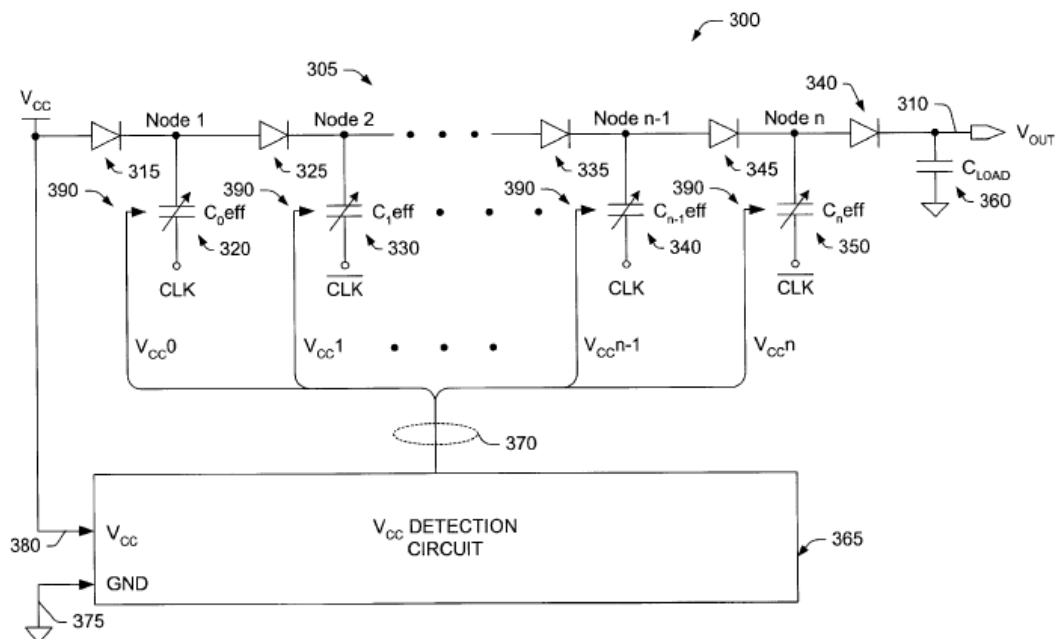
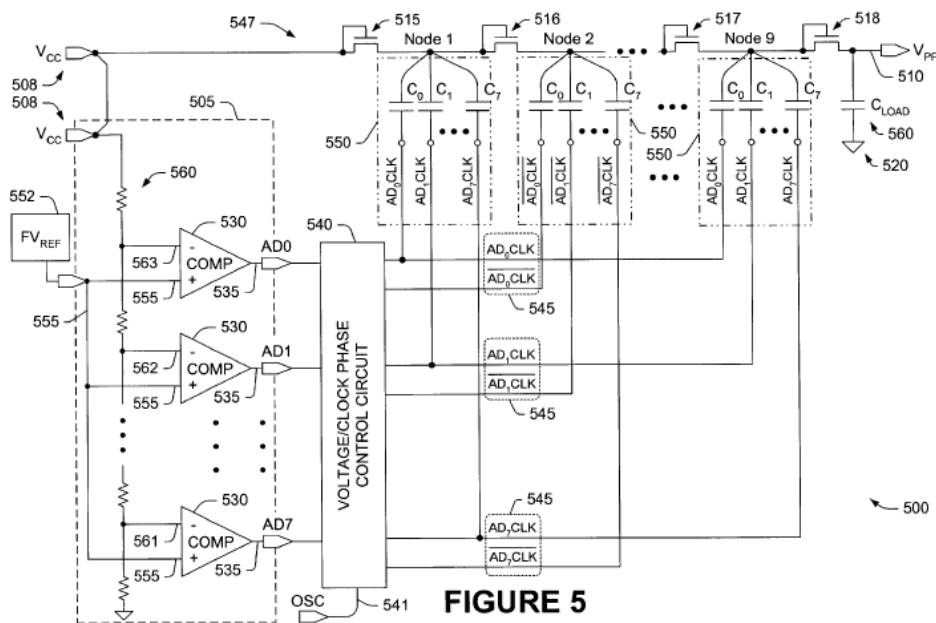


FIGURE 3

Id., Fig. 3.

With respect to Figure 5, reproduced below, *Le* more specifically describes the use of an analog-to-digital converter to measure the input supply voltage and generate a digital word that reflect the value of the input supply voltage. *Id.* 8:58-10:14. “This digital word serves as a V_{CC} level determination and each bit of the word drives its own clock circuit 542 and a capacitor selection within the capacitor networks 550. Therefore, based on the digital word, a unique combination of capacitors are electrically placed in parallel within each capacitor network 550, thereby altering the effective values associated with C_0 thru C_7 .” *Id.* 10:14-20.



Id., Fig. 5.

III. GROUNDS 1A AND 1B FAIL BECAUSE *DOLUCA* DOES NOT GENERATE A PLURALITY OF PUMP VOLTAGES

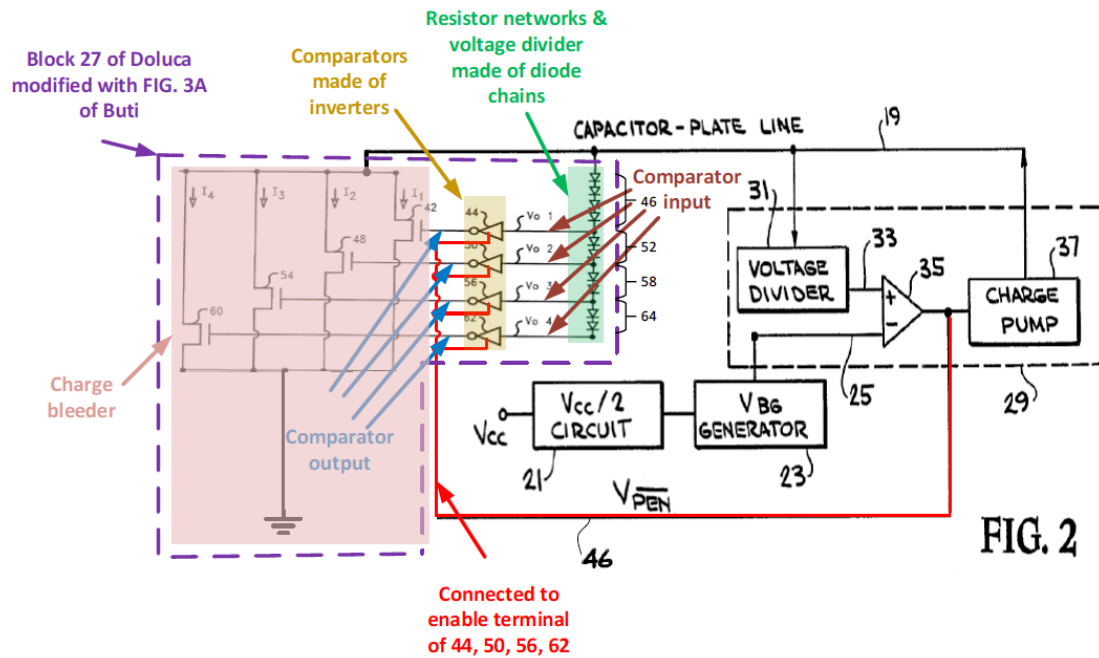
A. Claim Limitation [1a] (Ground 1A)

Claim limitation [1a] of the '241 Patent requires “a pumping circuit ... to receive a supply voltage and generate a selected one of a plurality of pump voltages.” Ex. 1001, 8:19-21. As described above in Section II.A, *Dolucas* circuitry generates only a single output voltage. Petitioner and its expert claim otherwise, asserting that *Dolucas* charge pump will “provide VCP within a range depending on the value of K, which can be ‘chosen’ to be within a specified range,” and that, consequently, using a “chosen” value of K, “*Dolucas* charge pump can ‘generate a selected one of a plurality of pump voltages.’” Petition at 19-20, citing Ex. 1003, ¶83. Petitioner and its expert are incorrect.

K is a design criteria, “a constant having a value,” Ex. 1006 at 3:42-43, and cannot be modified in the charge pump circuitry. *Dolucas* charge pump circuitry generates a minimum of $6.1V (V_{CC}/2 + 3V_{BG})$. To generate, for example, at least $8.5V (V_{CC}/2 + 5V_{BG})$, *Dolucas* charge pump circuitry would require two additional transistors in the voltage divider 31 of the pump control circuit 29. *Dolucas* does not teach or suggest such a modification, let alone a modification that can be made dynamically to allow the charge pump circuitry to generate more than one output voltage, VCP. Because *Dolucas* does not “generate a selected one of a plurality of

pump voltages,” as required by claim 1, Petitioner’s reliance on *Doluca* is misplaced.

Recognizing this problem, the Petition asserts an alternative theory—that *Doluca*’s charge pump circuit can be modified to include *Buti*’s charge bleeder circuitry, as shown below, to select from more than one pump output voltages. *See* Petition at 20, citing Ex. 1003, ¶84 (referencing ¶72 for the suggested *Doluca-Buti* combination below). The Petition ignores that the proposed combination modifies the charge bleeder circuitry of *Doluca*, but not the charge pump circuitry. The charge pump circuitry will generate a V_{CP} of more than $6.1V$ ($V_{CC}/2 + 3V_{BG}$) and then be disabled until V_{CP} falls below $6.1V$. Because *Doluca*’s charge bleeder circuitry sets an upper boundary for the overshoot of V_{CP} from the charge pump, the modified charge bleeder circuitry can only be used to modify that upper boundary. *See* Section II.A, *supra*; *see also* Ex. 1006, 5:15-19 (“the $\overline{VPEN}$ voltage [highlighted in red below] produced by comparator 35 is fed back along line 46 to bleeder control circuit 27, where it disables charge bleeder 45 whenever charge pump 37 is in operation.”). *Doluca*, as modified by the charge bleeder circuitry of *Buti* as Petitioner suggests, does not “generate a selected one of a plurality of pump voltages,” as required by claim 1. Petitioner’s reliance on the modifications to *Doluca* is again misplaced.



EX-1006, FIG. 2 (modified in view of EX-1005, FIG. 3, annotated)

Petition at 17, Ex. 1003, ¶72; *see also* Ex. 1003, ¶71 (“Buti, like Doluca, discloses using a charge bleeder circuit to regulate the charge pump output voltage.”)

B. Claim Limitation [24a] (Ground 1A)

Claim limitation [24a] of the ’241 Patent requires “selecting a output pump voltage (V_{pump}).” Ex. 1001, 12:36. As with claim limitation [1a], the Petition relies on *Dolucas* to satisfy this limitation. *See* Petition at 28 (“A POSITA would have understood that selecting a particular value of K corresponds to selecting a particular output pump voltage (V_{CP}).” (citing Ex. 1003, ¶94)). As described above in Section II.A, *Dolucas*’ circuitry generates only a single output voltage. Consequently, for the same reasons as set forth with respect to claim limitation [1a],

Doluca does not teach circuitry that provides for “selecting a output pump voltage (V_{pump}).” Petitioner’s reliance on *Doluca* for claim limitation [24a] fails.

C. Claim Limitation [13b] (Ground 1B)

Claim limitation [13b] of the ’241 Patent requires “a pumping circuit ... to receive a supply voltage and generate one or more pump voltages.” Ex. 1001, 12:26-28. Petitioner asserts that the *Doluca-Buti* combination discloses this limitation and references the discussion with respect to claim limitation [1a]. See Petition at 46. For the same reasons as set forth with respect to claim limitation [1a], *Doluca*, either alone or in the proposed combination with *Buti*, does not teach circuitry that provides for “generat[ing] one or more pump voltages.” Petitioner’s reliance on *Doluca* for claim limitation [13b] fails.

IV. GROUNDS 2A, 2B AND 3A FAIL BECAUSE *LE* DOES NOT GENERATE A PLURALITY OF PUMP VOLTAGES

A. Claim Limitation [1a] (Ground 2A)

Claim limitation [1a] requires “a pumping circuit ... to receive a supply voltage and generate a selected one of a plurality of pump voltages.” Ex. 1001, 8:19-21. As described above in Section II.B, *Le*’s charge pump generates only a single output voltage. See also Petition at 53 (“*Le* teaches ... that the charge pump system 300 includes a charge pump circuit 305 that has one or more stages ‘to receive the supply voltage 380 and *generate the charge pump output voltage* V_{OUT} 310.’”) (emphasis added)). The Petition further relies on *Le*’s teaching “that the charge pump

voltage generated by its disclosed embodiment can be applied to program/erase operations of memory cells, and notes that such operations in semiconductor memory devices use different voltage levels, which are generated by the charge pump circuits.” *Id.* (citing Ex. 1008, 1:7-18, 1:51-2:34). The Petition then concludes that a “POSITA would have found it obvious that Le’s disclosed pump system 300 with pumping circuit 305 can be applied to generate a plurality of pump voltages used in memory device operations.” Petition at 53 (citing Ex. 1003, ¶146).

Petitioner does not point to any disclosure of the charge pump of *Le* that teaches, describes or discloses the ability to generate multiple output voltages. To the contrary, *Le* is concerned with the precise generation of a single output voltage from an input voltage supply that can experience some degree of variation that would cause the output voltage of the conventional charge pump to experience “increased ripple magnitude,” as well as “noise spikes and valleys” due to the shunting regulator. Ex. 1008, 3:58-43. As explained above, in Section II.B, *Le*’s proposed solution is the inclusion of an input supply voltage detection circuit and a charge pump compensation circuit to modulate the capacitive loading of the charge pump to reduce the ripple associated with the charge pump and lessen reliance on a shunting regulator. Nowhere in *Le*’s disclosure of the charge pump circuitry is a description or disclosure that the charge pump can generate multiple output voltages.

Petitioner therefore relies on a paragraph in the Background section that

references the need to generate multiple voltage levels for various memory operations. Notably, that paragraph does not describe the multiple voltages as being generated by a single charge pump, but rather describes the use of *charge pumps*, *i.e.*, in the plural to generate the multiple voltages:

In these semiconductor applications, a charge pump sometimes is used to increase a small input, or supply voltage (for example, VCC) to a larger voltage that is passed to the word lines or bit lines of the semiconductor memory devices. For example, some dual bit memory cell architectures require about 9.5 volts to properly bias the word lines, about 6 volts for the bitline or drain of such cells, and between -6 to -8 volts for negative erase voltages, for the various memory operations discussed. *These voltages which are all higher than the applied supply voltage, are all created and fed by charge pumps to increase the supply voltage to the output voltage desired.* These voltages affect the reading and writing of data from/to the memory device. The voltage is increased by channeling the relatively small input voltage through a series of stages. The more stages a charge pump has, the greater the resulting output voltage.

Ex. 1008, 2:19-34 (emphasis added).

Because *Le* does not disclose a charge pump to generate multiple output voltages, *Le* cannot satisfy the requirement of claim limitation [1a] that “a pumping circuit ... to receive a supply voltage and generate a selected one of a plurality of pump voltages.” Petitioner’s reliance on *Le* for claim limitation [1a] therefore fails.

B. Claim Limitation [24a] (Ground 2B)

Claim limitation [24a] requires “selecting a output pump voltage (V_{pump}).”

Ex. 1001, 12:36. As with claim limitation [1a], the Petition relies on *Le* to satisfy

this limitation. *See* Petition at 67 (“*Le* in view of *Ujiie* teaches [24pre]-[24b]. *See supra* §§III.C.3.(a)-(d).”). As described above in Section II.B, *Le*’s charge pump generates only a single output voltage. Consequently, for the same reasons as set forth with respect to claim limitation [1a], *Le* does not teach circuitry that provides for “selecting a output pump voltage (V_{pump}).” Petitioner’s reliance on *Le* for claim limitation [24a] fails.

C. Claim Limitation [13b] (Ground 3A)

Claim limitation [13b] requires “a pumping circuit ... to receive a supply voltage and generate one or more pump voltages.” Ex. 1001, 12:26-28. Petitioner asserts that *Le* discloses this limitation and references the discussion with respect to claim limitation [1a]. Petition at 74 (“*Le* discloses [13b]. *See supra* §§III.C.3.(b)”). For the same reasons as set forth with respect to claim limitation [1a], *Le* does not teach circuitry that provides for “generat[ing] one or more pump voltages.” Petitioner’s reliance on *Le* for claim limitation [13b] fails.

V. THE *FINTIV* FACTORS WEIGH AGAINST INSTITUTION

35 U.S.C. § 314(a) gives the Board discretion to deny institution of the requested *inter partes* review due to the advanced state of parallel district court litigation regarding the same issues. *See NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8 (PTAB Sept. 12, 2018) (precedential, designated May 7, 2019) (“*NHK Spring*”). The Board has set forth six factors for determining whether

discretionary denial due to such parallel litigation is appropriate (the “*Fintiv* factors”):

whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;

proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision;

investment in the parallel proceeding by the court and the parties;

overlap between issues raised in the petition and in the parallel proceeding;

whether the petitioner and the defendant in the parallel proceeding are the same party; and

other circumstances that impact the Board’s exercise of discretion, including the merits.

Apple Inc. v. Fintiv, Inc., IPR2020-00019, Paper 11 at 5-6 (PTAB Mar. 20, 2020) (precedential, designated May 5, 2020) (“*Fintiv I*”); *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 15 at 7-8 (PTAB May 13, 2020) (decision denying institution of *inter partes* review) (“*Fintiv II*”). “These factors relate to whether efficiency, fairness, and the merits support the exercise of authority to deny institution in view of an earlier trial date in the parallel proceeding.” *Fintiv I* at 6. In evaluating the factors, “the Board takes a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review.” *Id.*

As set forth below, all of the *Fintiv* factors weigh against institution. To avoid duplication of efforts, wasting resources, and potentially inconsistent decisions, the Board should deny institution.

A. Factor 1: The district court has not granted a stay, nor is there any evidence that a stay will be granted.

There are presently two active district court cases involving the '241 patent pending in the Western District of Texas before Judge Albright: *Sonrai Memory Limited v. Micron Technology, Inc.*, No. 6:22-cv-00855-ADA (W.D. Tex.) (“*Micron case*”) and *Sonrai Memory Limited v. Apple Inc.*, No. 6:22-cv-00787-ADA (W.D. Tex.) (“*Apple case*”). The district court is aware of Petitioner’s pending IPR petition because Patent Owner filed a Notice of IPR Petition informing the court that defendant/Petitioner filed an IPR petition regarding claims of the '241 patent. Ex. 2001. Although defendant/Petitioner filed a motion to stay pending completion of IPR review in August, that motion has not been ruled on and the district court has not stayed the case pending IPR. Nor is there any evidence that the case will be stayed. Moreover, Apple has not filed any motion to stay the *Apple case*. Nor has Apple filed an IPR petition regarding the '241 patent.

To the contrary, the district court has entered a scheduling order and the *Micron case* is set for trial on September 18, 2024. See Ex. 2002, Order Granting Motion for Entry of Scheduling Order, *Sonrai Memory Limited v. Micron*

Technology, Inc., No. 6:22-cv-00855-ADA, Dkt. No. 29 (W.D. Tex. Apr. 26, 2023).

The district court case is not at an early stage. The case against Micron was filed more than one year ago on August 16, 2022 – well more than a year before now, and well more than fifteen (15) months before the institution decision is due. *See* Ex. 2003, Civil Docket for Case No. 6:22-cv-00855-ADA at 1. This has been an actively litigated matter with 58 docket entries to date. *See* Ex. 2003, Docket Sheet at 5. A Final Written Decision will not be due until three (3) months *after* trial is scheduled to begin with jury selection on September 18, 2024. *See* Ex. 2002, Scheduling Order at 3. Moreover, the *Apple* case is set for trial even before that on July 8, 2024. *See* Ex. 2010.

Although Petitioner has filed a motion to stay, it is unlikely to prevail because Judge Albright does not favor stays pending IPR proceedings. *See* Ex. 2004 (Law360 Article: *West Texas Judge Says He Can Move Faster Than PTAB*) (Judge Albright: “It’s my job to give people the opportunity to have their cases tried in a federal court . . . and I probably can get a patent trial resolved more quickly than the PTAB can.”); *see also Samsung Elecs. Co. Ltd. v. Evolved Wireless LLC*, IPR2021-00950, Paper 10 at 10–11 (PTAB Nov. 29, 2021) (“*Evolved*”) (finding this factor weighed in favor of denial and denying institution where patent owner showed a stay was unlikely based on the advanced stage of the case and the court’s past decisions denying stays).

Regardless, by the December 11, 2023 deadline for the institution decision, discovery will be well underway. *See* Ex. 2002, Scheduling Order at 2. Claim construction has been completed in the *Apple* case and will have been completed in the *Micron* case. *See* Exs. 2011, 2005. Thus, it is highly unlikely that Judge Albright would grant a stay at that late juncture in the case. *See, e.g.*, Ex. 2006 (Order denying motion to stay pending IPR where plaintiff had served its preliminary infringement contentions and where claim construction was scheduled to begin before the IPR institution deadline); Ex. 2007 at 5 (Order denying stay pending IPR even though discovery had not yet begun, as the district court had already “invested significant resources and time in construing all the contested claim terms”).

As explained by the Board, a stay of the district court litigation pending resolution of the PTAB proceedings “allays concerns about inefficiency and duplication of efforts.” *Fintiv I* at 6; *Fintiv II* at 12. But here, the district court has not stayed the pending litigation, nor is there any evidence that a stay will be granted. Allowing this IPR to proceed simultaneously with the district court litigation would be wasteful and inefficient. This factor weighs against institution.

B. Factor 2: The proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision.

The statutory deadline for a final written decision in this proceeding is December 11, 2024, which can be extended to June 11, 2025, for good cause or in

the case of joinder. 37 C.F.R. § 42.100. Jury selection in the *Micron* case remains scheduled for September 18, 2024. *See* Ex. 2002. And jury selection in the *Apple* case remains scheduled for July 8, 2024. *See* Ex. 2010.

Even if the Board disregards the scheduled trial date, an analysis of the current median time-to-trial statistics still weighs against institution. *See* Ex. 2008, U.S. District Courts—Federal Court Management Statistics—Profiles—During the 12-Month Periods Ending June 31, 2018 Through 2023. The most recent statistics, for a 12-month period ending June 31, 2023, show a median time-to-trial in the Western District of Texas of 26.4 months. *Id.* at 37. Accordingly, the projected trial date for purposes of *Fintiv* in accordance with Director’s June 21, 2022 Memorandum on Discretionary Denials would be October 29, 2024 – within a month and a half of the scheduled trial date and well before the expected timing of a Final Written Decision if proceedings are instituted.

This factor weighs against institution.

C. Factor 3: The parties and the courts have made a substantial investment in the parallel proceeding.

This factor relates to the “amount and type of work already completed in the parallel litigation by the court and the parties *at the time of the institution decision.*” *Fintiv I* at 9 (emphasis added). For example, “if, at the time of the institution decision, the district court has issued substantive orders related to the patent at issue

in the petition,” this factor favors denial. *Id.* at 9-10. Claim construction orders entered by the district court likewise “indicate that the court and parties have invested sufficient time in the parallel proceeding to favor denial.” *Id.* at 10.

As discussed above, this has been an actively litigated matter with 58 docket entries to date. *See* Ex. 2003. By the December 11, 2023 deadline for an institution decision, discovery will be well underway. *See* Ex. 2002. Claim construction briefing and argument has been completed in the *Apple* case and Judge Albright has issued a claim construction order. *See* Ex. 2011. Further, claim construction briefing and argument will have been completed in the *Micron* case and Judge Albright will likely have issued a claim construction order in that case as well. *See* Ex. 2005.

Thus, the parties and the district court will have invested significant time and resources in the litigation by the time the Board reaches an institution decision in this matter. This favors discretionary denial. *Fintiv I* at 10; *Fintiv II* at 13-14 (finding that “the level of investment and effort already expended on claim construction and invalidity contentions” favored denial).

D. Factor 4: There is complete overlap between this IPR and the district court proceedings.

This factor looks at “whether all or some of the claims challenged in the petition are also at issue in district court,” and whether the “petition includes the

same or substantially the same claims, grounds, arguments, and evidence” as the parallel district court case. *Fintiv I* at 12-13.

Here, Petitioner has challenged all of the asserted claims of the '241 patent. Petitioner's Invalidity Contentions in the district court case identify the same *Doluca, Buti, Hosono, Le, Ujiie, Kuriyama, Asano*, and *Yang* references asserted in the Petition as prior art that anticipates and/or renders obvious the asserted claims. *See* Ex. 2009 at 17. In fact, Petitioner explicitly incorporated by reference all positions set forth in the IPR petition in the district court invalidity contentions. *Id.* at 3. Moreover, Apple has also explicitly incorporated by reference Petitioner's IPR petition in its district court invalidity contentions. Ex. 2012 at 4. Thus, there is complete overlap with respect to Petitioner's invalidity arguments and evidence. That the district court case involves additional prior art references not asserted in this IPR is “not relevant to the question of the degree of overlap for this factor.” *Fintiv II* at 15. The fact that the Petition challenges additional claims also does not warrant institution. *See, e.g., Next Caller Inc. v. TRUSTID, Inc.*, IPR2019-00961, Paper 10 at 14 (PTAB Oct. 16, 2019) (denying institution where the district court case involved only a subset of the challenged claims).

The Petitioner's offer of a so-called *Sotera* stipulation does not resolve the question of overlap. First, since the invalidity contentions were served after the Petition, there is no indication of which references cited in its invalidity contentions

Petitioner will contend could not have been raised in the Petition and could therefore be asserted in the district court. Moreover, Petitioner’s stipulation would not apply to the *Apple* case. Second, the invalidity contentions further assert that Micron is “reserv[ing] the right to rely on prior art systems that correspond to or practice the disclosures in the above identified publications.” *See* Ex. 2009 at 17-18.

In sum, this IPR and the district court cases involve the same claims—which will be construed under the same *Phillips* standard—and substantially the same prior art (and, as discussed below, the same parties), which raises substantial “concerns of inefficiency and the possibility of conflicting decisions.” *Fintiv I* at 12. This factor thus weighs in favor of discretionary denial. *See Fintiv II* at 15; *NHK Spring* at 19–20.

E. Factor 5: Petitioner is a defendant in the district court litigation.

There is no dispute that Petitioner is the defendant in the district court litigation. “Because the petitioner and the defendant in the parallel proceeding are the same party, this factor weighs in favor of discretionary denial.” *Fintiv II* at 15.

F. Factor 6: Other circumstances that impact the Board’s exercise of discretion, including the merits.

The Board may consider other circumstances in the exercise of its discretion, including the merits of the case. *Fintiv I* at 14. However, “a full analysis of the merits is not necessary to evaluate this factor.” *Fintiv II* at 17. And, it is important

to note that the compelling merits standard is a higher standard than the standard for institution set by statute. “A challenge can only ‘plainly lead to a conclusion that one or more claims are unpatentable’ if it is highly likely that the petitioner would prevail with respect to at least one challenged claim.” *OpenSky Indus., LLC v. VLSI Tech. LLC*, IPR2021-01064, Paper 102, 49 (PTAB Oct. 4, 2022) (precedential).

Petitioner’s assertion that it will stipulate to not asserting the prior art in the district court litigation should not preclude full consideration of the *Fintiv* factors where, as here, the Petitioner waited until almost nine months after service of the district court complaint to file its petition and, even if it does file a full *Sotera* stipulation, would not address all of the *Fintiv* concerns because Petitioner is also “reserv[ing] the right to rely on prior art systems that correspond to or practice the disclosures in the above identified publications.” *See Ex. 2009* at 17-18.

Petitioner has not presented a “particularly strong” case of unpatentability because it is based solely on alleged obviousness and not anticipation. Furthermore, as set forth above, Patent Owner has presented evidence that the asserted references relied upon by Petitioner do not disclose at least one limitation of all the challenged claims.

As set forth above, the Petition does not present a reasonable likelihood of invalidity under any ground or challenged claim, let alone compelling evidence of

unpatentability, and factor 6 weighs against institution. All six *Fintiv* factors strongly favor discretionary denial, and the Petition should be denied.

VI. INSTITUTION SHOULD BE DENIED UNDER § 314(a) IN VIEW OF THE *GENERAL PLASTIC* FACTORS.

35 U.S.C. § 314(a) gives the Board discretion to deny instituting “follow on” petitions. *General Plastic Indus. Co. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 (Sept. 6, 2017) (precedential).

The Board has set forth seven factors for determining whether discretionary denial is appropriate (the “*General Plastic* factors”):

1. whether the same petitioner previously filed a petition directed to the same claims of the same patent;
2. whether at the time of filing of the first petition the petitioner knew of the prior art asserted in the second petition or should have known of it;
3. whether at the time of filing of the second petition the petitioner already received the patent owner’s preliminary response to the first petition or received the Board’s decision on whether to institute review in the first petition;
4. the length of time that elapsed between the time the petitioner learned of the prior art asserted in the second petition and the filing of the second petition;
5. whether the petitioner provides adequate explanation for the time elapsed between the filings of multiple petitions directed to the same claims of the same patent;
6. the finite resources of the Board; and

7. the requirement under 35 U.S.C. § 316(a)(11) to issue a final determination not later than 1 year after the date on which the Director notices institution of review.

General Plastic Indus. Co., IPR2016-01357, Paper 19 at 16.

Here, the *General Plastic* factors weigh against institution or are neutral.

A. Factor 1 weighs against institution.

Factor 1 relates to successive petitions filed by the same petitioner, which is not precisely at issue here because Micron is admittedly not one of the eight previous petitioners – Kioxia Corporation, Kioxia America, Inc., Western Digital Technologies, Inc., Dell Technologies Inc., Google LLC, Kingston Technology Company, Inc., Kingston Technology Corporation, and Samsung Electronics Co., Ltd. – in IPR2021-01561 (filed September 22, 2021, instituted March 23, 2022). And although Micron is a distinct party, there is no reason to assume that it has distinct interests or distinct litigation strategies from the previous petitioners. And, as the same office of the same law firm is representing Micron that represented Kingston Technology Company, Inc. and Kingston Technology Corporation in IPR2021-01561, it is reasonable to assume that Micron benefited from the prior petitions.

B. Factor 2 is neutral.

Factor 2 weighs against institution because petitioner relies upon at least three reference – *Doluca*, *Hosono*, and *Ujiie* – that were identified in IPR2021-01561. *See*

IPR2021-01561, Paper 2 at 17-20. The same office of the same law firm that represents Micron here represented Kingston in that IPR.

C. Factors 3 weighs against institution.

Factor 3 weighs against institution because petitioner was aware of and able to benefit from the Institution decision in IPR2021-01561 (instituted March 23, 2022).

D. Factor 4 weighs against institution.

Factor 4 weighs against institution because petitioner was presumably aware of at least three references relied upon by petitioner – *Doluca*, *Hosono*, and *Ujiie* – that were identified in IPR2021-01561. *See* IPR2021-01561, Paper 2 at 17-20. The same office of the same law firm that represents Micron here represented Kingston in the litigation.

E. Factor 5 weighs against institution.

Factor 5 weighs against institution because petitioner does not provide an adequate explanation for the time between filings of multiple petitions directed to the same claims of the same patent in view of petitioner’s presumed awareness of at least three reference relied upon by petitioner – *Doluca*, *Hosono*, and *Ujiie* – that were identified in IPR2021-01561. *See* IPR2021-01561, Paper 2 at 17-20. The same office of the same law firm that represents Micron here represented Kingston in the litigation.

F. Factors 6 and 7 are neutral.

Because the previous IPR was terminated before the Board issued a Final Written Decision, and notwithstanding the opportunities for prejudicial road-mapping that are provided by the Board’s previous institution decision, factors 6 and 7 are neutral.

G. Summary of Factors

<i>Factor 1</i>	Weighs against institution
<i>Factor 2</i>	Weighs against institution
<i>Factor 3</i>	Weighs against institution
<i>Factor 4</i>	Weighs against institution
<i>Factor 5</i>	Weighs against institution
<i>Factor 6</i>	Neutral
<i>Factor 7</i>	Neutral

In summary, five *General Plastic* factors weigh against institution and two factors are neutral. Under § 314(a) and the totality of *General Plastic* factors, institution should be denied.

VII. CONCLUSION

The Board should deny institution because Petitioner fails to establish a reasonable likelihood of invalidity for any independent claim. The independent claims recite either “a pumping circuit” that “generate[s] a selected one of a plurality of pump voltages” (independent claim 1) or that “generate[s] one or more pump

voltages” (independent claim 13), or a method for generating an output voltage in “a charge pump circuit” that includes “selecting a output pump voltage (V_{pump})” (independent claim 24). Neither *Doluca* alone, *Doluca* in combination with *Buti*, nor *Le* alone disclose charge pumps that generate multiple output voltages. Consequently, Petitioner cannot establish that the limitations of “generat[ing] a selected one of a plurality of pump voltages” (independent claim 1) or that “generat[ing] one or more pump voltages” (independent claim 13), or that “selecting a output pump voltage (V_{pump})” (independent claim 24), are satisfied by the prior art and therefore cannot establish a reasonable likelihood of invalidity.

In addition, all of the *Fintiv* factors and the majority of the *General Plastic* factors favor discretionary denial, and the Petition should be denied for these reasons alone.

Respectfully submitted,

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Date: September 11, 2023

CERTIFICATE OF WORD COUNT (37 C.F.R. § 42.24(d))

The undersigned hereby certifies that the word count in this Patent Owner Preliminary Response is 7,463 words, as counted by the word-processing program Microsoft Word that was used to generate this Patent Owner Preliminary Response, where such word count excludes the table of contents, table of authorities, mandatory notices, certificate of service, appendix of exhibits, claim listing, and this certificate of word count. This Patent Owner Preliminary Response is in compliance with the 14,000-word limit set forth in 37 C.F.R. § 42.24(b)(1).

Date: September 11, 2023

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CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e))

The undersigned hereby certifies that the above document was served on September 11, 2023, by filing this document, along with the accompanying exhibits, through the Patent Trial and Appeal Case Tracking System as well as delivering a copy via electronic mail upon the following attorneys of record for the Petitioner:

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