

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.
Petitioner,

v.

SONRAI MEMORY LIMITED,
Patent Owner

IPR2023-00909
Patent No. 6,724,241

**DECLARATION OF DR. MICHAEL C. BROGIOLI IN SUPPORT OF
PATENT OWNER'S RESPONSE**

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I, Michael C. Brogioli, PhD, hereby declare as follows:

I. INTRODUCTION

1. I am over the age of eighteen (18) years and otherwise competent to make this declaration.

2. I have been retained as an expert witness on behalf of Sonrai Memory Limited (“Sonrai”) for the above-captioned *inter partes* review (“IPR”). I understand that the petition for *inter partes* review involves U.S. Patent No. 6,724,241 (“the ’241 Patent”).

3. I make this declaration based on my personal knowledge, educational background and training, consideration of the materials I discuss herein, and my expert opinions.

4. I am being compensated at a rate of \$700 per hour for my time in this matter. My compensation does not depend on the outcome of this proceeding, and I have no financial interest in its outcome.

5. In preparing this Declaration, I have reviewed and considered the ’241 Patent, the ’241 Patent’s prosecution history, the Petition, Dr. James Dickens’ declaration, Ex. 1003, submitted in this proceeding, and each document cited in my declaration.

II. BACKGROUND AND QUALIFICATIONS

6. My qualifications for forming the opinions given in this declaration are summarized here and are addressed more fully in my curriculum vitae, which is submitted as Exhibit 2014. That exhibit also includes a list of my publications.

7. I am currently an Adjunct Professor of Electrical and Computer Engineering at Rice University in Houston, TX, teaching Ph.D. candidate level courses in wireless telecommunications, embedded computing software, embedded computing hardware, and software/hardware design. I have held this position since July 2009. I am also currently the Managing Director of Polymathic Consulting in Austin, TX, a company that advises a variety of clients on engineering, research and development, intellectual property, and other technical leadership matters, and I have held this position since October 2011.

8. I am a named inventor on multiple issued and pending patent applications. The subject matter of these applications includes, but is not limited to, embedded processing, edge computing, and various aspects of distributed systems including computation, interconnectivity and hardware/software design and implementation.

9. From November 2009 to October 2011, I was Chief Architect, Senior Member Technical Staff at Freescale Semiconductor in Austin, TX (formerly Motorola), responsible for management of technology, engineering roadmaps,

design lead on compiler infrastructure and optimizations for mobile and embedded computing solutions including the technologies involved in this matter. From 2008 to 2009, I was Senior Engineer working with high performance compiler design and next generation baseband compiler design and next generation baseband microprocessor and microcontroller architecture at Freescale Semiconductor in Austin, Texas.

10. From June 2006 to August 2007, I worked as the Technical Co-Founder of Method Seven LLC, in Boston, MA, working with high performance software and hardware systems architecture. I am currently the co-founder, co-inventor, and Chief Technology Officer of Network Native, an Internet of Things hardware and software company. I have also served on multiple advisory boards for technology companies over the past 10 years.

11. While at Rice University, I developed various computer architecture designs. For example, from 2002 to 2004, I developed Spinach, a simulator design toolset for modeling programmable network interface architectures, which models system components common to all programmable computing environments as well as components specific to embedded. From 2004 to 2009, I developed Spinach DSP-FPGA, a modular and composable simulator design infrastructure for programmable and reconfigurable embedded SOC architectures specifically targeting mobile, embedded and portable computing devices. From 2005 to 2009, I

developed and published a retargetable compiler infrastructure for software and systems related to mobile and embedded computing technologies. Many of these tools have been used at U.S. universities in the area of electrical and computer engineering research.

12. I am recognized as an expert in the field of computer architecture, computer hardware and computer software systems as they relate to the subject matter at hand. I am a member of the Institute of Electrical and Electronics Engineers (IEEE). I am currently the Program Chair of Design Automation Conference in the areas of Embedded and Wireless Solutions. I have been a Program Committee member for the IEEE and ACM Design Automation Conference from 2011 to the present, as well as other IEEE and ACM conferences. I have published, co-published and contributed to numerous works on wireless and mobile computing, sensor technologies, GPU Architecture, software optimizations, signal processing systems, digital signal processing and related architectures, and low power computing, among other topics.

13. I have previously served as an engineering consultant and testifying witness on matters related to, and including power circuits, voltage regulators, and power management in computer system hardware and software. This experience is encompassed in my work in academia and as a faculty member, my time in

industry as a system designer and architect, as well as my work as an engineering consultant and expert witness over the past 15 years.

14. Over the past 15+ years, I have authored numerous peer reviewed publications in the area of embedded and high performance computing, interconnect technologies, memory system technologies and optimization at the hardware and software design level. I have also been a committee member, and chair of Design Automation Conference in areas of technology related to the '680 Patent, often reviewing and vetting submissions from major industry players in the design and architectural issues related to various technologies at issue in this matter.

15. During my tenure at Freescale Semiconductor, I was in charge of system developer tools for baseband processor design, both in the hardware and software spaces. This work included hardware and software design issues of next generation wireless networking equipment, including system level programming models, interconnect technology, heterogeneous computing, various hardware acceleration technologies and related components.

16. My current curriculum vitae, provided in Exhibit 2014, contains more information on my background and experience, as well as the cases in which I have served as an expert witness the past four years.

17. No part of my compensation is contingent upon the outcome of this litigation. I have no other interests in this litigation or with any of the parties.

III. LEGAL PRINCIPLES

A. Claim construction

18. I understand that the first step in performing a validity analysis of the patent claims is to interpret the meaning and scope of the claims by construing the terms and phrases found in those claims. I understand that the appropriate construction of a claim term is its ordinary and accustomed meaning as understood by one of ordinary skill in the art at the time of the invention in the context of the entire patent.

19. I understand that standard for claim construction in an *inter partes* review is the same standard as is applied in district court proceedings.

20. I understand that a determination of the meaning and scope of the claims is a matter of law. I have been informed that to determine the meaning of the claims, one should consider the intrinsic evidence, which includes the patent's claims, written description, and prosecution history.

B. Burden of Proof

21. I understand that in an *inter partes* review, the petitioner has the burden of proving unpatentability by a preponderance of the evidence.

C. Anticipation

22. I have been instructed by counsel and understand that a reference is anticipated if a single prior art reference discloses each and every claim element,

either explicitly or inherently, as arranged in the same way as in the claim. I understand that where even one claim element is not disclosed in a reference, a contention of anticipation fails.

23. I further understand that when a reference fails to explicitly disclose a claim element, that reference inherently discloses that element only if the reference must *necessarily* include the undisclosed claim element.

D. Obviousness

24. I have been instructed by counsel and understand that a combination of prior art references may render a claim obvious if, at the time of the invention, a person of ordinary skill in the art would have selected and combined those prior-art elements in the normal course of research and development to yield the claimed invention.

25. I understand that in an obviousness analysis, one should consider the *Graham* factors: the scope and content of the prior art; the differences between the claimed inventions and the prior art; the level of ordinary skill in the art; and certain secondary considerations, identified below. I further understand the obviousness analysis is to be performed on a claim-by-claim basis. I understand that a person of ordinary skill in the art is a person of ordinary creativity, not an automaton.

26. I have been instructed by counsel and understand that obviousness requires more than a mere showing that the prior art includes separate references covering each separate limitation in a claim under examination. I understand obviousness requires the additional showing that a person of ordinary skill at the time of the invention would have been *motivated* to combine those references in a manner that would include all limitations of the challenged claim, and, in making that combination, a person of ordinary skill in the art would have had a *reasonable expectation of success*.

27. I also understand that an obviousness analysis must be conducted with awareness of the distortion caused by hindsight bias and with caution of arguments reliant upon *ex post* reasoning. For instance, I understand that when considering obviousness, I should put myself in the position of a person of ordinary skill in the field at the time of the invention, rather than considering new information that is known today but was not known before the priority date of the challenged patent.

28. In particular, I understand that it is improper to use the challenged patent's disclosure or invention as a roadmap to find its prior-art components, because such an approach discounts the value of combining various existing features or principles in a new way to achieve a new result.

IV. PERSON OF ORDINARY SKILL IN THE ART

29. Dr. Dickens states that “a person of ordinary skill in the art (POSITA) relating to the technology of the ’241 Patent would have had a Bachelor’s degree in electrical engineering or a related field, and 2-3 years of experience in the design or development of electronic circuits or systems, or the equivalent. Additional graduate education could substitute for professional experience, or significant experience in the field could substitute for formal education.” Ex. 1003, ¶ 12. For purposes of this declaration, I adopt Dr. Dickens’ proposed level of skill in the art.

V. CLAIM CONSTRUCTION

30. Dr. Dickens presents two proposed constructions for the term “load” as used in the challenged claims of the ’241 Patent: either “a device that receives electrical power” or “a device that absorbs surplus charge to significantly reduce voltage ripple compared to a case without the device.” Ex. 1003, ¶¶ 46-47. It is my understanding that Petitioner did not seek a construction for the term “load” in the corresponding district court case. Although I do not necessarily agree with either construction, I will respond to Dr. Dickens’ opinions based on his proposed constructions as appropriate.

31. Dr. Dickens also opines that the “load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit” of claim 1 of the ’241 Patent is a means-plus function limitation.

Dr. Dickens opines that the function of “selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit” should be construed to mean “choosing a load based on the target pump voltage, such that the load is coupled to the output of the pumping circuit when the target pump voltage is selected.” Ex. 1003, ¶ 49. I understand that neither Petitioner nor Patent Owner sought to construe the function in the corresponding district court case. Ex. 2015, *Joint Claim Construction Statement*. My opinions set forth below do not change if applying the plain meaning of the function or Dr. Dickens’ proposed construction of the function. As further explained below, I agree with Dr. Dickens that the ’241 Patent “explains that each load (e.g., Load A, B, or C) is ‘associated’ with a specific pump voltage and that the load is attached to the output when that specific pump voltage is selected ... [and] the attachment of the load is triggered by the pump voltage selection, not a later event.” Ex. 1003, ¶ 50 (citing Ex. 1001, 4:33-51, 7:7-16, 7:31-42).

32. With respect to the corresponding structure of the “load selector means” of claim 1 of the ’241 Patent, Dr. Dickens opines that the structure is “switches 320, 324, and 328 and their respective control signals EN_A, EN_B, and EN_C.” Ex. 1003, ¶ 51. Dr. Dickens further opines that the ’241 Patent “describes structural embodiments for switches 320, 324, and 328 and indicates that the switches can be structurally implemented with transistors.” *Id.* (citing Ex. 1001,

Figs. 5A, 5B). Dr. Dickens also suggests that the corresponding structure could further include “a ‘controller’ as part of the structure that generates control signals EN_A, EN_B and EN_C.” Ex. 1003, ¶ 52.

33. I note that, in the corresponding district court case, the Court construed the corresponding structure as “(i) a plurality of switches (320, 324, and 328) as shown in Figure 3 and associated descriptions in the specification, or shown in Figure 7 (720, 724, 728) and associated descriptions in the specification; (ii) a plurality of transistors 504A as shown in Figure 5A and associated descriptions in the specification; or (iii) a plurality of elevator circuits 502B and transistors 504B as shown in Figure 5B and associated descriptions in the specification; and equivalents thereof.” Ex. 2016, *Preliminary Claim Constructions*. My opinions set forth below do not change based on the Court’s construction or any of Dr. Dickens’ constructions.

34. Similarly, for the “load selector means coupled to the output pump for selecting a load that satisfies a specific pump voltage” means-plus-function limitation of claim 13 of the ’241 Patent, Dr. Dickens asserts that the recited function of “satisfies a specific pump voltage” means “selectively coupling a load associated with a specific pump voltage,” and the corresponding structure is the same as for the “load selector means” of claim 1. Ex. 1003, ¶¶ 56-58. My opinions

with respect to the “load selector means” of claim 13 are the same as with respect to the “load selector means” of claim 1.

35. With respect to the “target output pump selector for shutting down the variable charge pump circuit when the target output pump voltage (V_{cfra}) is greater than or equal to a reference voltage (V_{ref})” limitation of claim 2 of the ’241 Patent and the similar limitation of claim 13, I agree with Dr. Dickens that the recited functions are “shutting down the variable charge pump circuit when the target output pump voltage (V_{cfra}) is greater than or equal to a reference voltage (V_{ref})” for claim 2 and “sampling the output of the pump circuit for shutting down the variable charge pump circuit whenever the sampled output voltage (V_{cfra}) is greater than or equal to a reference voltage (V_{ref})” for claim 13. Ex. 1003, ¶ 54; *see also* Ex. 2015, *Joint Claim Construction Statement*, at 1. I also agree that the corresponding structure is comparator 702. Ex. 1003, ¶ 55; *see also* Ex. 2015, *Joint Claim Construction Statement*, at 1.

VI. GROUNDS 1A, 1B – THE COMBINATION OF DOLUCA AND BUTI DO NOT RENDER OBVIOUS THE INDEPENDENT CLAIMS OR CLAIMS DEPENDENT THEREFROM

A. Dolucas does not disclose a pumping circuit that “generate[s] a selected one of a plurality of pump voltages”

36. I understand that independent claim 1 requires a pumping circuit that “generate[s] a selected one of a plurality of pump voltages.” *See* Ex. 1001 at Claim 1, limitation 1[a]. However, in my opinion, the Petition and Dr. Dickens do not

show that Doluca discloses any charge pump to generate one of a plurality of pump voltages.

37. First, Dr. Dickens first opines that Doluca discloses a “capacitor-plate bias generator circuit ... [that] includes a charge pump for supplying voltage to memory devices.” Ex. 1003, ¶ 60. Dr. Dickens then opines that “[c]harge pump 37 receives source voltage V_{CC} as the supply voltage and generates output V_{CP} ,” *id.*, ¶ 82, and that “[t]o provide bias voltage for memory device operation, Doluca teaches that an ideal value of V_{CP} should equal $V_{CC}/2 + K$, where K is a constant having a value $K > V_{CC}/2 + V_T$.” *Id.*, ¶ 83 (citing Ex. 1006, 2:65-3:54). Because Doluca discloses that “ K might be chosen to be 3.5 to 4,” Ex. 1006, 3:49-50, Dr. Dickens concludes “one can control charge pump 37 to generate a selected pump output voltage by selecting the value of K ... [that] is described by the claimed feature of [1a].” Ex. 1003, ¶ 83. As I explain further below with respect to the disclosure of Doluca, Dr. Dickens’ conclusion is unfounded.

38. Doluca’s goal is the design of a charge pump circuit for use in generating DRAM capacitor plate voltage whose output voltage can track $V_{CC}/2$. Ex. 1006, 3:51-54. $V_{CC}/2$ is the pre-charge voltage of the bit-line in Doluca’s DRAM cell. *Id.*, 3:13-16. Pre-charging the bit-lines to $V_{CC}/2$ (half the supply voltage) reduces signal swing on the bit lines which reduces peak current and allows faster reading. In other words, pre-charging is intended to minimize

propagation delay time by ensuring that the bit-line is driven to voltage midway between 0 V (a logical “0”) and V_{CC} (a logical “1”), so that when the actual cell is read, the bit-line need only be driven from the midway voltage to either 0 V or V_{CC} . See Ex. 1006, 3:11-16. Doluca’s DRAM cell is shown in Fig. 1 and described as follows:

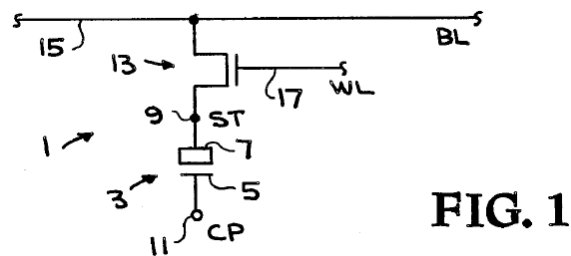


FIG. 1

In FIG. 1, a single capacitive memory cell 1 has been illustrated in a much simplified and idealized form. A capacitive memory element 3 has an anode electrode 5 and a cathode electrode 7. Cathode 7 is connected to a storage node 9, while anode electrode 5 is connected, in common with the anodes of the other capacitive memory elements in the matrix-array memory device (not shown) of which cell 1 is a part, to a capacitor-plate node 11.

A single data bit is stored in cell 1 and is represented by the voltage of storage node 9. Access to node 9 is controlled by a word-select gate transistor 13 which couples node 9 to a bit-line 15 whenever the potential on a word-line 17 goes high.

Ex. 1006, Fig. 1, 2:65-3:10.

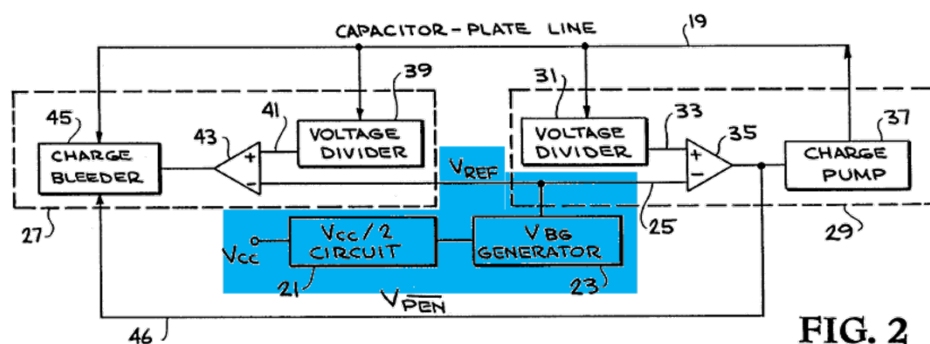
39. For reads from the DRAM cell, the word-line turns on transistor 13.

The voltage at node 9 is either expected at 0 V for logical “0” or V_{CC} for logical “1” to pull the pre-charged bit-line 15 down to 0 V or up to V_{CC} , respectively.

When the capacitor stores a logical “0,” it holds no charge and 0 V and thus node 9 will pull the bit-line voltage down to be sensed as the logical “0.” When the capacitor stores a logical “1,” it holds a charge and V_{CC} is expected at node 9 to pull the bit-line voltage up to be sensed as the logical “1.” However, because the semiconductor-based capacitor typically has a threshold voltage, V_T , of up to 1 V, the value of V_{CP} must be at least V_T above V_{CC} for node 9 to be V_{CC} to indicate the logical “1.” In other words, $V_{CP} > V_{CC} + V_T$, or $V_{CP} > 5V + 1V$ (6V). Ex. 1006, 3:17-25. Because the capacitor has an upper limit of about 10 V before experiencing dielectric breakdown, *id.*, 3:26-31, there is some allowance for V_{CP} in excess of $V_{CC} + V_T$.

40. Doluca further discloses that, because the bit-line is pre-charged to $V_{CC}/2$, “an optimum voltage source for biasing the capacitor-plate node 9 should track this bit-line voltage.” *Id.*, 3:32-35. “[S]ince the bit-line pre-charge voltage is $V_{CC}/2$, the voltage of the capacitor-plate bias source should be function of $V_{CC}/2$ such that it follows any variations of bit-line voltage exactly.” *Id.*, 3:35-38. In order to ensure that V_{CP} tracks $V_{CC}/2$, Doluca introduces the design criteria of K as the value of $V_{CC}/2 + V_T$ to satisfy that V_{CP} is at least $V_{CC} + V_T$. In the $V_{CC}=5$ V DRAM of Doluca, V_{CP} will have to be at least 6 V and K will have to be at least 3.5 V. *Id.*, 3:49-50. Doluca places the top of the range of K at 4 V, *id.*, although a POSITA would recognize that a higher top of the range could be sustained without

damaging the capacitor. In summary, Doluca uses K to define the mathematical relationship between V_{CC} and V_{CP} in terms of $V_{CC}/2$ because that's what the bit-line is charged to and Doluca seeks to maintain a relationship between $V_{CC}/2$ and V_{CP} , although the relationship of V_{CC} and V_{CP} is also applicable (at a correspondence of one-to-one).



Ex. 1006, Fig. 2 (annotated); *see also id.*, 3:55-4:8.

Comparator, 35,
active output when
 V_{REF} less than $(V_{CP} - V_{CC}/2)/3 + V_{CC}/2$.
4:40-45; 7:15-16.

Voltage divider, 33,
generates $(V_{CP} - V_{CC}/2)/3 + V_{CC}/2$. 4:30-39; 7:6-14.

$\overline{VPEN}$ driven low on
comparator active
output. 7:16-24.

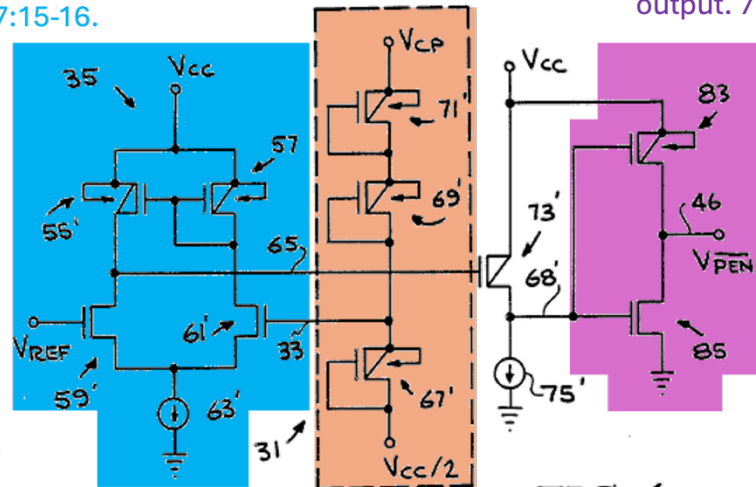
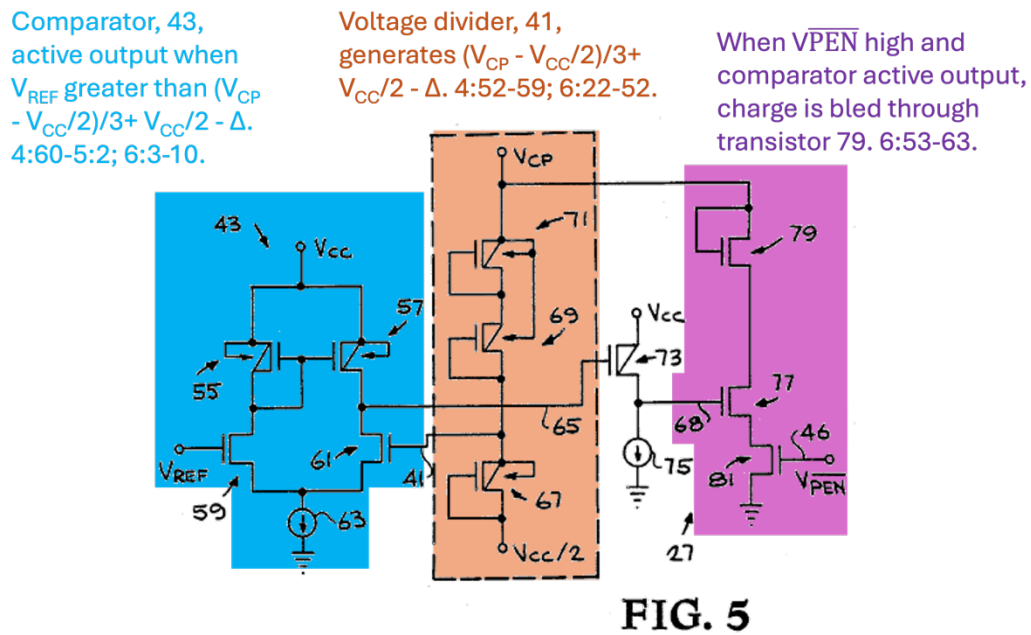


FIG. 6

Ex. 1006, Fig. 6 (annotated).

44. With respect to the charge bleeder control circuit, Fig. 5 of Doluca discloses the bleeder circuit that is active when $\overline{VPEN}$ is inactive, i.e., high (logical “1”), and when $(V_{CP} - V_{CC}/2)/3 + V_{CC}/2 - \Delta$ is greater than V_{REF} , with Δ being a small offset voltage. *Id.*, 4:53-5:8; 5:55-6:63.



Ex. 1006, Fig. 5 (annotated).

45. In the 5 V DRAM device of Doluca, the capacitor plate voltage generator circuitry is designed to generate an output voltage of between 6.1 V (where the charge pump turns on) and 6.1 V *plus* a small offset voltage . To a POSITA, this is a single output voltage. I therefore disagree with Dr. Dickens' conclusion that Doluca teaches "a pumping circuit ... to receive a supply voltage and generate a selected one of a plurality of pump voltages," as required by limitation [a] of claim 1 of the '241 Patent.

46. The '241 patent explicitly discloses that "the *same* charge pump circuit" can generate multiple different pump voltage outputs, V_A , V_B , and V_C , where $V_B = 2 \cdot V_A$ and $V_C = 4 \cdot V_A$. Ex. 1001 at 2:29-31. During prosecution, the

Examiner, when allowing the claims, stated that “[t]he Prior Art of record does not appear to disclose a charge pump with a selectable voltage output and a selectable load wherein a load is selected so as to minimize output ripple for a given output voltage.” Ex. 1002 at 107.

47. I also disagree with Dr. Dickens’ assertion that “one can control charge pump 37 to generate a selected pump output voltage by selecting the value of K.” Ex. 1003, ¶ 83. A POSITA would realize that K is not a selection mechanism to allow a charge pump circuit to generate multiple output voltages, but rather a mathematical design criteria that Doluca used to design the charge pump control circuitry, including voltage divider 33 and comparator 35, and the charge bleeder control circuitry, including voltage divider 41 and comparator 43. This mathematical design criteria allowed Doluca to design the capacitor plate voltage generation circuitry so that V_{CP} would respond to any fluctuations in $V_{CC}/2$, the bit-line pre-charge voltage. There is no K input to the Doluca capacitor plate voltage generation circuitry to allow that circuitry to generate any other voltage than that in the range of 6.1 V to 6.1 V *plus* a small offset voltage in Doluca’s 5 V V_{CC} DRAM device. Not surprisingly, Dr. Dickens provides no analysis of how K can be “selected” as anything other than a design criteria for a 5 V V_{CC} DRAM device.

48. Dr. Doluca further asserts that “the Doluca-Buti combination given in ¶ 72 provides another obvious mechanism of selecting the pump output voltage,”

Ex. 1003, ¶ 84, by selectively changing the threshold voltages in Buti's diode stack. I discuss Buti further down below and incorporate that discussion here. I disagree with Dr. Dickens that selectively changing the threshold voltages in Buti's diode stack will have any impact on the behavior of capacitor plate voltage generation circuitry. As Doluca notes, the pump and bleeder circuitry will never be simultaneously active. When $\overline{VPEN}$ is low (logical "0"), the charge pump is active, i.e., turned on, and the bleeder is inactive, i.e., turned off. When $\overline{VPEN}$ is high (logical "1"), the charge pump is inactive, i.e., turned off, and the bleeder is active, i.e., turned on. "[T]he pump and bleeder should not operate simultaneously." Ex. 1006, 5:10-11. Dr. Dickens shows the Doluca-Buti combination configured the same way. *See* Ex. 1003, ¶¶ 72, 75, 77 (showing inverters and comparators enabled when $\overline{VPEN}$ is high (logical "1")). When V_{CP} is at 6.1 V or above, $\overline{VPEN}$ will be high and the charge pump will be inactive will never be turned on. With Buti settings as in Fig. 3A (see Ex. 1005, 7:51-58 (Table 1), transistor 42 will be turned off, and transistors 48, 54 and 60 will be turned on. There will be three transistors bleeding charge and contributing to bringing V_{CP} under 6.1 V, at which point the charge pump will be activated and the bleeder will be deactivated. In other words, in the condition where V_{CP} is above 6.1 V, the charge pump is off and the bleeder is on, the voltage will be around 6.1 V, just as Doluca contemplates. Changing the diode stack thresholds can only change the

number of devices used for the charge bleeder, causing V_{CP} to fall under 6.1 V more quickly (or slowly) depending on the number of bleeder transistors active at that voltage. It does not generate a different output voltage than Doluca already does. I therefore disagree with Dr. Dickens' conclusion that "by selecting the number of diodes in diode stack 46, the POSITA can select the specific pump output voltage." Ex. 1003, ¶ 84.

49. For the reasons set forth above, I disagree that Doluca on its own, or in combination with Buti as the Petition and Dr. Dickens suggest, teach a "pumping circuit ... to receive a supply voltage and generate a selected one of a plurality of pump voltages," as required by claim 1 of the '241 Patent.

50. Because Dr. Dickens also relies on the same opinions with respect to the "pumping circuit ... to receive a supply voltage and generate one or more pump voltages," as required by claim 13 of the '241 Patent, *see* Ex. 1003, ¶ 130, I disagree that Doluca on its own, or in combination with Buti, teach this limitation of claim 13 of the '241 Patent.

51. Because Dr. Dickens also relies on the same opinions with respect to the "selecting a output pump voltage (V_{pump})," as required by claim 24 of the '241 Patent, *see* Ex. 1003, ¶ 94, I disagree that Doluca on its own, or in combination with Buti, teach this limitation of claim 24 of the '241 Patent. I further note that, in order to "select a output pump voltage," this limitation requires

that multiple output pump voltages, not just a single voltage as taught by Doluca and the proposed Doluca-Buti combination, be available to select from.

B. The combination of Doluca and Buti does not disclose a “a plurality of loads ... each load associated with a specific pump voltage”

52. The Petition and Dr. Dickens assert that “Doluca does not provide further structural or functional description of the charge bleeder.” Petition at 13; *see also* Ex. 1003, ¶ 70 (“Doluca illustrates charge bleeder 45 in a block without structural or operational detail.”). Based on this assertion, both the Petition and Dr. Dickens further assert that a POSITA would consequently be motivated to look to other sources, such as the Buti reference, to determine how the charge bleeder would be implemented. Petition at 13 (“A POSITA who, upon reviewing Doluca’s disclosure, wanted to know more about the bleeder 45 circuitry, and/or how it functions to lower the output voltage, would have looked at other sources for relevant information.”); Ex. 1003, ¶ 70 (“Doluca’s silence in this regard would have motivated a POSITA to seek supplemental material about charge bleeder examples ... among other sources, a POSITA would have considered the charge bleeder disclosed by Buti.”). I disagree with both the assessment of what Doluca discloses and the conclusion.

53. First, Dr. Dickens’ assessment that Doluca does not disclose a charge bleeder with “structural or operational detail” is contradicted by his own opinions.

For example, Dr. Dickens opines that “[t]he charge bleeder circuit is a dynamic load that is selectively coupled to the output when the output voltage is above a reference threshold that works to lower the output voltage to the commanded reference level. A POSITA would have understood that this is a form of a shunt regulator.” Ex. 1003, ¶ 62.

54. Second, and consistent with Dr. Dickens’ explanation, Doluca discloses “current-regulating transistor 79” as the charge bleeder. “Current-regulating transistor 79” is shown in Fig. 5 and is further described “as a non-linear current regulator having a generally parabolic current-voltage characteristic.” Ex. 1006, 6:54-58. Doluca also describes how the “current-regulating transistor 79” will be active when $\overline{VPEN}$ is high and $(V_{CP} - V_{CC}/2)/3 + V_{CC}/2 - \Delta$ is greater than V_{REF} , or V_{CP} is greater than 6.1 V *plus* a small offset voltage. *See* Ex. 1006, Fig. 5, 6:59-63 (“A gate transistor 81 is connected with its drain to the source of transistor 77, and with its source to ground. The gate of transistor 81 receives the $\overline{VPEN}$ voltage on the line 46 and disables the bleeder 27 whenever charge pump 37 is on.”).

55. Finally, as discussed below, I disagree with Dr. Dickens’ opinion that “[b]oth Doluca and Buti contemplate using a charge bleeder circuit to regulate the output voltage of the charge pump.” Ex. 1003, ¶ 69. A POSITA would recognize that Buti does not regulate the output voltage of a charge pump. At most, Buti’s

circuitry, that Dr. Dickens proposes substituting for Doluca charge bleeder control circuitry, regulates the rate of increase as the voltage increases from 0V to operating voltage and has no effect on the operating voltage value. I therefore disagree with Dr. Dickens's conclusion that a POSITA would be motivated to combine Doluca with Buti.

56. Even if a POSITA were motivated to combine Doluca with Buti, as I discussed above, the proposed combination yields a capacitor plate voltage generator circuit that yields the same 6.1 V V_{CP} as in Doluca alone.

57. Buti is directed at providing "a control circuit for accurately and efficiently controlling the *ramp-up rate of a charge pump* used for programming flash memory devices." Ex. 1005, 1:53-56. Buti is not directed at providing multiple different output voltages, e.g., for writing and erasing flash memory devices. The goal of Buti is further shown in Fig. 6, reproduced below, with respect to the single output voltage of 12.95 V.

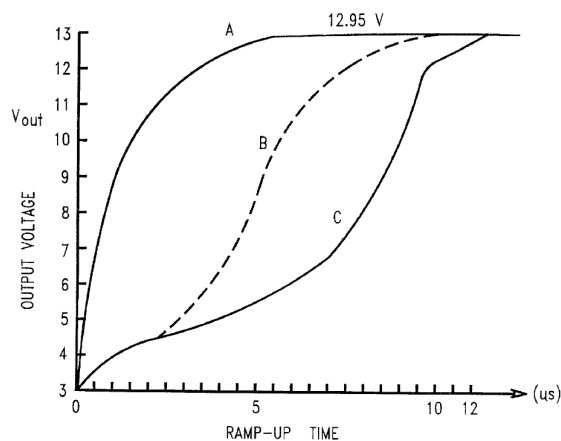
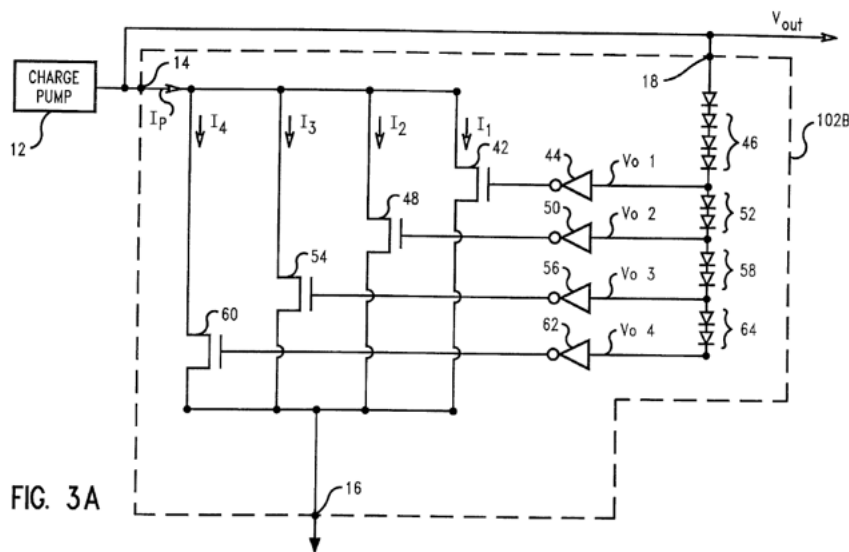


FIG. 6

Ex. 1005, Fig. 6.

58. As Buti explains, “FIG. 6 shows a comparison of the charge pump ramp-up rate with and without the ramp-up rate control circuit of the present invention.” *Id.*, 9:8-10. The figure shows: (i) a 3 μs ramp-up to 12.95 V in Curve A without any rate control, *id.*, 9:10-13; (ii) a 8 μs ramp-up to 12.95 V in Curve B using the rate control circuitry in Fig. 3A that Dr. Dickens proposes to substitute for Doluca’s charge bleeder control circuit, *id.*, 9:14-16; and (iii)) a 12 μs ramp-up to 12.95 V in Curve C using the rate control circuitry of another embodiment, *id.*, 9:16-19. Fig. 3A, the embodiment that Dr. Dickens proposes to substitute for Doluca’s charge bleeder control circuit, is reproduced below.



59. Buti explains how the bleed transistors 42, 48, 54 and 60 are all fully turned on at 2.5V and then how the diode stacks 46, 52, 48 and 64 are used to turn of those transistors, one-by-one. *See, e.g.,* Ex. 1005, 7:12-17 (“Referring to FIGS. 3A, 3B and Table 1, the first current bleed path is turned off first when charge pump output voltage V_{out} is about 5.78 volts. When V_{out} is about 5.78 volts, diodes 46 produce a series of voltage drops that produce a voltage V_{o1} which has a magnitude that constitutes a logic ‘1’ voltage. In response to this logic ‘1’ voltage, inverter 44 outputs a logic ‘0’ voltage level which turns-off FET 42 thereby substantially eliminating the flow of current I_1 through FET 42.”). Table 1, reproduced below, shows the “bleed path current contributed to current I_P for varying magnitudes of charge pump output voltage V_{out} .” *Id.*, 7:47-49.

Total Bleeding Leakage(I_P)	Output Voltage Range
$I_P = I_1 + I_2 + I_3 + I_4$	$2.5 < V_{out} < 5.78$
$I_P = I_2 + I_3 + I_4$	$5.78 < V_{out} < 7.60$
$I_P = I_3 + I_4$	$7.60 < V_{out} < 9.50$
$I_P = I_4$	$9.5 < V_{out} < 11.43$
$I_P = 0$	$11.43 < V_{out}$

Ex. 1005, 7:51-58.

60. Fig. 3B, reproduced below “is a graph of the operating characteristics of the embodiment shown in FIG. 3A.” *Id.*, 4:41-42. Fig. 3B shows how the absolute value of the current through the bleeder circuit, I_P , ramps up as the charge pump output voltage, V_{out} , ramps up from 0 V to 2.5 V. From 2.5 V until transistor 42 begins to turn off at about 5.78 V, I_P remains constant as a function of $I_1+I_2+I_3+I_4$. As transistor 42 turns off, I_P is reduced to $I_2+I_3+I_4$, etc. V_{out} continues to rise, even after the last transistor 60 turns off and I_P is reduced to zero.

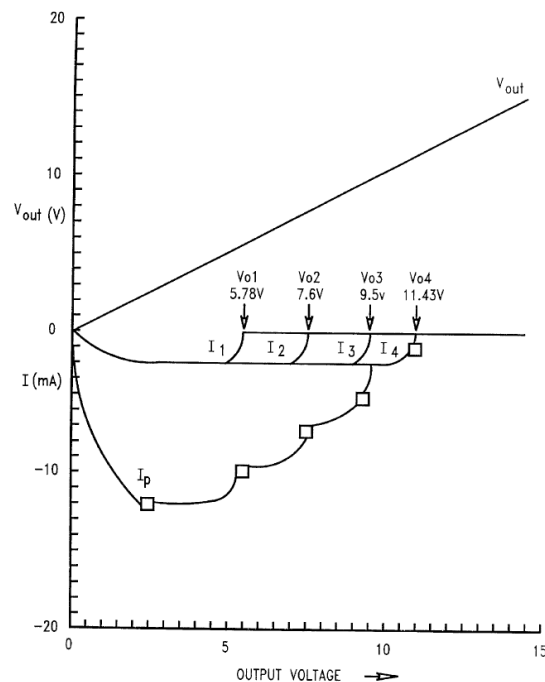


FIG. 3B

Ex. 1005, Fig. 3B.

61. As shown above in Fig. 3B, Buti's ramp rate control circuit does not regulate the value of V_{out} . As shown above, in Fig. 6, Buti's ramp rate control circuit regulates the rate of increase of V_{out} when Buti's charge pump is turned on. I therefore disagree with Dr. Dickens' opinion that "[b]oth Doluca and Buti contemplate using a charge bleeder circuit to regulate the output voltage of the charge pump." Ex. 1003, ¶ 69.

62. Limitation [b] of claim 1 recites "a plurality of loads selectively coupleable to an output of the pumping circuit, each load associated with a specific pump voltage." '241 Patent, Claim 1. Dr. Dickens asserts that the plurality of loads are met by the 42, 48, 54 and 60 of Fig. 3A of Buti. Ex. 1003, ¶ 85. More specifically, Dr. Dickens opines that "[i]n the resultant circuit of the Doluca-Buti combination, FETs 42, 48, 54, and 60 are selectively activated or deactivated." Id. I disagree that the FETs will be "selectively activated or deactivated" when $\overline{VPEN}$ goes high, i.e., when V_{CP} is above 6.1 V. Using the diode stack thresholds of Table 1 of Buti, when $\overline{VPEN}$ goes high, transistor 42 will be off and transistors 48, 54 and 60 will be on. Because the charge pump is off, transistors 48, 54 and 60 will bleed off the level of V_{CP} until it goes below 6.1 V causing $\overline{VPEN}$ to go low, turning on the charge pump and turning off the transistors. In this example, transistor 42 will never turn on. Moreover, V_{CP} will not reach 7.6 V (or higher), so

transistors 48, 54 and 60 will never turn off while $\overline{VPEN}$ is high. I therefore disagree with Dr. Dickens that “[e]ach of these FET loads 42, 48, 54, and 60 is associated with a specific pump output voltage” and “[d]epending on the value of charge pump output V_{CP} , each of FET loads 42, 48, 54, and 60 can be selectively activated, i.e., selectively coupled to charge pump 37.”

63. For the reasons set forth above, I disagree that the Doluca-Buti combination teaches “a plurality of loads selectively coupleable to an output of the pumping circuit, each load associated with a specific pump voltage,” as required by claim 1 of the ’241 Patent.

64. Because Dr. Dickens also relies on the same opinions with respect to “a plurality of loads, each load associated with a specific pump voltage and selectively coupleable to an output of the pump circuit (output pump),” as required by claim 13 of the ’241 Patent, *see* Ex. 1003, ¶ 130, I disagree that the Doluca-Buti combination teaches this limitation of claim 13 of the ’241 Patent.

65. Because Dr. Dickens also relies on the same opinions with respect to the “turning on a load associated with the selected V_{pump} ,” as required by claim 24 of the ’241 Patent, *see* Ex. 1003, ¶ 94, I disagree that the Doluca-Buti combination teaches this limitation of claim 24 of the ’241 Patent.

C. **The combination of Doluca and Buti does not disclose “load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit”**

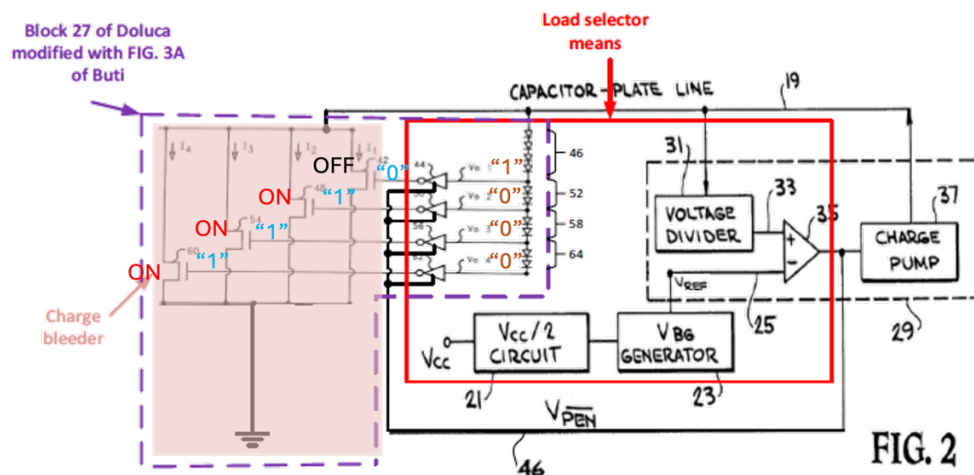
66. Limitation [c] of claim 1 recites “load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit.” ’241 Patent, Claim 1. I understand that the parties agree, and under the Court’s construction in the corresponding district court case, that this is a means-plus function limitation. Applying either Dr. Dickens’s proposed corresponding structure of “switches 320, 324, and 328 and their respective control signals EN_A, EN_B, and EN_C,” Ex. 1003, ¶ 51, or the Court’s corresponding structure of “(i) a plurality of switches (320, 324, and 328) as shown in Figure 3 and associated descriptions in the specification, or shown in Figure 7 (720, 724, 728) and associated descriptions in the specification; (ii) a plurality of transistors 504A as shown in Figure 5A and associated descriptions in the specification; or (iii) a plurality of elevator circuits 502B and transistors 504B as shown in Figure 5B and associated descriptions in the specification; and equivalents thereof,” Ex. 2016, *Preliminary Claim Constructions*, I disagree with Dr. Dickens’ opinion that the Doluca-Buti combination meets this limitation. The specification of the ’241 Patent describes that the switches 320, 323, and 328 (and the transistors of Figs. 5A and 5B that may be used as switches) are each operated exclusively. In other

words, only one switch at a time (to couple one load to the output of the pumping circuit) may be active/closed at a time.

67. More specifically, the '241 Patent recites: "Only one load can be selected at a time. For example, if voltage VA is selected, EN_A causes the first switch 320 to close, connecting the first load to the output terminal of the charge pump circuit 300. The remaining loads 326 and 330 are disconnected from the output terminal because their respective switches 324 and 328 are open." Ex. 1001, 4:56-62; *see also id.*, 5:1-6 (for selection of voltage VB, switch 324 is closed, switches 320, 328 are open), 5:12-17 (for selection of voltage VC, switch 328 is closed, switches 320, 324 are open), 5:22-32 (with respect to Fig. 5A, switches 320, 324, 328 implemented as NMOS transistor 504A), 5:33-43 (with respect to Fig. 5B, switches 320, 324, 328 implemented as NMOS transistor 504B, along with elevator circuit 502B).

68. Dr. Dickens opines that "that FET loads 42, 48, 54, and 60 can be selectively coupled to the output of charge pump 37," and that the "load selector means" is met by the circuitry he identifies in his drawing of the Doluca-Buti combination. Ex. 1003, ¶ 87 (identifying circuit components within red square). The Doluca-Buti combination does not meet the corresponding structure of "load selector means" because the inverters are not exclusively active (converting a low signal, logic "0," to a high signal, logic "1" to activate corresponding load

transistor). As I noted above, when V_{CP} rises above 6.1 V, $\overline{VPEN}$ goes from low to high. The charge pump is deactivated, and the inverters in the Buti circuit are activated. At 6.1 V, using the example voltages of Table 1 of Buti, the top-most inverter input is at a high level (logic “1”), meaning the output of the inverter is at a low level (logic “0”) and transistor 42 is turned off. Conversely, the other three inverters are at a low level (logic “0”), meaning the output of these inverter is at a high level (logic “1”) and transistors 48, 54, and 60 are turned on. I have annotated this in Dr. Dickens’ drawing below. I note that transistors 48, 54 and 60 will bleed V_{CP} until it falls below 6.1 V, at which point $\overline{VPEN}$ will transition to low, enabling the charge pump and disabling Buti’s circuit.



Ex. 1003, ¶ 87 (annotated to show logic values and transistor operation when Doluca charge pump rises above 6.1 V and $\overline{VPEN}$ enables Buti circuit).

69. Dr. Dickens confirms that, when $\overline{VPEN}$ goes high, i.e., $V_{CP} > 6.1\text{ V}$, the “voltage on capacitor-plate line 19 V_{CP} increases above the threshold voltage of diode stack 46, the input of inverter 44 is logic ‘1’ and the output of inverter 44 is logic ‘0.’” Ex. 1003, ¶ 88. FET 42 is deactivated. *Id.* Dr. Dickens then states that “as V_{CP} increases, FETs 48, 54, and 60 are subsequently deactivated.” *Id.* Dr. Dickens offers no explanation as to how V_{CP} can increase when the charge pump is enabled and the transistors 48, 54, and 60 are bleeding charge from V_{CP} . Nor can he. A POSITA would realize there is no active circuitry increasing V_{CP} when $\overline{VPEN}$ goes high, and the only subsequent deactivation of transistors 48, 54, and 60 is when $\overline{VPEN}$ goes low and transistors 48, 54, and 60 are simultaneously switched off.

70. Dr. Dickens also offers a further variation to the Buti circuit where, instead of deactivating transistor loads with increasing voltage, transistor loads are activated with increasing voltage. *See* Ex. 1003, ¶¶ 88, 89 (replacing inverters with buffers enabled by $\overline{VPEN}$), 90 (replacing NMOS transistors 42, 48, 54, 60 with PMOS transistors; replacing inverters/buffers with comparators). In the Table 1 example voltages of Buti, when $\overline{VPEN}$ goes high, i.e., $V_{CP} > 6.1\text{ V}$, only transistor 42 would be turned on. In this instance, the Doluca-Buti combination would work no differently than Doluca alone – when V_{CP} goes above 6.1 V and $\overline{VPEN}$ goes high, V_{CP} charge will be bled through a single transistor.

71. Regardless of the variations that Dr. Dickens espouses, I disagree that the corresponding structure for the “load selector means” is met. In each of Dr. Dickens’ variations, each inverter/buffer/comparator is not operated exclusively to the other inverter/buffer/comparator, meaning multiple loads can be coupled to the output of Doluca’s pump circuit at a time depending on the diode stack. This is contrary to the operation of the corresponding structure in the specification of the ’241 Patent. *See* Ex. 1001, 4:56-62, 5:1-6, 5:12-17, 5:22-32, 5:33-43. I therefore disagree that the Doluca-Buti combination meets the “load selector means” limitation of claim 1 of the ’241 Patent.

72. Because Dr. Dickens also relies on the same opinions with respect to “a load selector means coupled to the output pump for selecting a load that satisfies a specific pump voltage,” as required by claim 13 of the ’241 Patent, *see* Ex. 1003, ¶ 130, I disagree that the Doluca-Buti combination teaches this limitation of claim 13 of the ’241 Patent.

73. Because Dr. Dickens also relies on the same opinions with respect to the “turning on a load associated with the selected V_{pump} ,” as required by claim 24 of the ’241 Patent, *see* Ex. 1003, ¶ 94, I disagree that the Doluca-Buti combination teaches this limitation of claim 24 of the ’241 Patent.

VII. GROUNDS 2A, 2B, 2C, 3A, 3B – A POSITA WOULD NOT BE MOTIVATED TO COMBINE LE WITH UJIE

74. In my opinion, a POSITA would not have been motivated to arrive at the combination of Le with Ujiie that the Petition and Dr. Dickens suggest. The proposed combination of Le and Ujiie form the basis for at least the independent claims in Grounds 2A, 2B, 2C, 3A and 3B. *See* Ex. 1003, ¶¶ 147-149, 178, 202. As an initial point, I note that Le was cited during the prosecution of the '241 Patent and the claims were allowed over Le. Ex. 1002, at 100.

A. Le

75. In the Background of the Invention section, Le describes a first conventional charge pump that generates an output voltage from the V_{CC} power supply:

[T]he conventional charge pump 100 has a number of stages (stage 1 thru stage n). The charge pump 100 has at its input, a voltage, V_{CC} which is transmitted through a diode 115 to a first node (node 1) including a first bootstrap capacitor 120 having a capacitance C . A second node (node 2) is connected to the first node (node 1) via a diode 125 and also has a second bootstrap capacitor 130 having a capacitance C . The output of node 2 is then passed through a number of subsequent nodes, identical to previously described nodes 1 and 2, that also include a bootstrap capacitor having a capacitance value C that is substantially identical to the capacitance value C present at nodes 1 and 2. Finally, the conventional charge pump has an output terminal, V_{OUT} , also having a capacitor 160 having a total capacitance C_{L+P} which is defined as being the load capacitance C_L of the load connected to the output of the pump and a parasitic capacitance C_P inherent in the transmitting means of the conventional pump.

Ex. 1008, 2:52-3:3.

76. Also in the Background of the Invention section, Le describes a second conventional charge pump that builds on the first conventional charge pump by using larger capacitors to accommodate for lower voltage supply and a shunt regulator to keep the output voltage capped to a maximum:

In the prior art example of FIG. 2, a conventional two stage charge pump 200 is illustrated **with large capacitor values to accommodate the lowest power supply level, and the addition of a shunt regulator 270 attached at the conventional point of the charge pump output 280, to reduce the output when the supply or the output voltage is higher than a target value.** As in FIG. 1, the charge pump 200 of FIG. 2 includes an input 210 coupled to an input voltage such as the supply voltage V_{CC} . The input 210 is coupled to a first stage, via a diode 215, which is also coupled to a first stage node (node 1) including a capacitor 220 having a capacitance C_1 .

The first stage is further connected to a second stage, via a diode element 225, including a second and final stage node (node 2) having a bootstrap capacitor 230 having a capacitance C_2 . The final stage node (node 2) is coupled through a diode 240 to a load capacitor 260 having a capacitance value C_{LOAD} , and to the shunt regulator 270. The shunt regulator 270 produces a regulated version of the charge pump output V_{OUT} 280.

Id., 3:6-24 (emphasis added).

77. Le next identifies the general issues associated with the use of larger capacitor values and a shunt regulator including loss of pump efficiency and excess output voltage ripple:

The shunt regulator 280 regulates the charge pump output by partially shorting to ground that portion of the charge pump output which is greater than a desired voltage level. In this conventional method, large capacitor values may be used to compensate for the lowest power supply voltage. However, ***when the V_{CC} is not at its lowest level, the***

use of large capacitor values wastes power supply charge which may be simply shorted to ground through the shunt regulator, resulting in an overall loss of pump efficiency.

The output of the charge pump 280 and the shunt regulator 270 experience a ripple voltage signal from the charge and discharge cycles, with a period which matches the clock cycle period. The ripple voltage level on the output rises during a charge cycle, and drops again as a function of the RC discharge of the load and the load capacitance C_{LOAD} 260. The ripple voltage level rises during the charge cycle, until the shunt regulator determines that an over-voltage condition or target regulation voltage has been reached, wherein the shunt regulator shunting transistors begin to conduct and shunt the over-voltage charge to ground. Because of the internal regulation feedback and response time delays within the shunt regulator, the shunting transistors will not be able to react immediately to the over-voltage level, thereby causing the charge pump voltage to continue to rise beyond the target regulation voltage before the shunting transistors can respond with adequate conduction.

Id., 3:31-57 (emphasis added).

78. Le further notes that the excess output voltage ripple can be quite significant, at about 400 millivolts peak-to-peak for a 9 V output voltage. *Id.*, 3:58-62. “Additionally, noise spikes and valleys are produced on the output 280 as the shunting transistors in the shunt regulator 270 discharge the over-voltage on the charge pump capacitors to ground.” *Id.*, 3:63-66. In addition to the “noise spikes and valleys,” Le identifies the problem of “increased power consumption and reduced overall system efficiency.” *Id.*, 3:66-4:3; *see also id.*, 4:8-15 (“In addition, at high V_{CC} voltages, the charge pump circuit and shunt regulator circuit together as a system exhibit increased power consumption and reduced system efficiency.

Additionally, most device applications seek to consume a minimum of power from the supply, particularly in battery and other portable power device applications this is important.”).

79. Based on the problems that Le identifies with the prior art conventional charge pumps utilizing a shunt regulator, Le sets the goal of “a low power, low noise means of compensation for the variations in the V_{CC} supply applied to the charge pump circuit, while maintaining a simple regulator design.” *Id.*, 4:15-18. Le’s proposed solution is to “vary the capacitance of the bootstrap capacitor values within the stages ... as a function of the input supply voltage.” *Id.*, 4:31-35. More specifically:

According to an exemplary aspect of the present invention, the system incorporates a voltage detection circuit (e.g., analog to digital converter, digital thermometer), which is used to measure the V_{CC} applied to the charge pump circuit. The detected V_{CC} value is then employed in a compensation circuit to vary a manner in which the charge pump circuit output voltage is generated. By compensating for these variations in the V_{CC} supply which is applied to the charge pump circuit, the charge pump output voltage is modulated, enabling a more stable, for example, wordline or bitline voltage.

Id., 6:26-36; *see also id.*, 7:4-25.

80. The result of Le’s proposed charge pump is that “ V_{CC} variations which are typically reflected in the output of the conventional charge pump circuit are identified, and compensation for such variations are generated to thereby generate wordline or bitline voltages during various flash memory cell modes.” *Id.*,

6:17-21. The result, which Le repeats frequently, is less power consumption in Le's proposed charge pump circuit because the use of the shunt regulator is significantly reduced:

- “Consequently, a shunt regulator circuit which may operate in conjunction with such a charge pump circuit will consume less power and regulate the charge pump output with less ripple than with conventional charge pump circuits.” *Id.*, 6:21-25.
- “[T]he charge pump circuit of the present invention provides for a further reduction in power consumption when used in conjunction with a shunt regulator. Note that in prior art charge pump circuits, at high V_{CC} input voltages, the charge pump output voltage would greatly exceed the desired target output voltage, which required the shunt regulator to shunt the excess wasted charge to ground. The charge pump circuit of the present invention reduces an amount of such shunting by the regulator, thereby reducing power.” *Id.*, 10:61-11:3.

B. Ujii

81. Ujii describes a boosting circuit that produces two different voltage outputs, one of which corresponds to a write operation and one of which corresponds to an erase operation so that both write and erase operations take approximately the same amount of time.

[A] voltage boosting circuit that can generate two different voltages based on a signal that controls writing and erasing is provided, and the present invention is configured so that during data erasing, a voltage is applied to the nonvolatile memory element that is higher and in the opposite direction than when writing, therefore the charge that was injected by the write voltage is removed by an even higher voltage, and the erase time is shortened to be equivalent to the write time. Thereby achieving the above objective of shortening the time required for rewriting all of the data of the EEPROM device.

Ex. 1009 at [09]; *see also* Ex. 1009 at [06] (“An object of the present invention is to provide a write/erase method that makes the data erase time in an EEPROM device almost equal to the write time, and thereby enabling the total data rewrite time to be reduced.”).

82. To ensure that the write timing and erase timing match, Ujiie further discloses using two different voltages, V_{pp1} and V_{pp2} , separately for the write and erase operations, respectively. To produce V_{pp1} and V_{pp2} , Ujiie uses “clamp diodes D1, D2 for limiting the voltage generated by the charge pump 10 to form a constant write voltage V_{PP1} and erase voltage V_{PP2} , and switch MOSFETs Q1, Q2 connected in series with clamp diodes D1 and D2, respectively.” *Id.* at [20]. “The clamp diodes D1, D2 are formed to have breakdown voltages that are equal to write voltage V_{PP1} and the erase voltage V_{PP2} , respectively. Diodes with different breakdown voltages can be formed with a high degree of accuracy by

using, for example, Zener diodes and appropriately controlling the amount of ion implantation that occurs into the semiconductor region.” *Id.* at [22].

C. A POSITA would not be motivated to combine Le with Ujiie

83. Dr. Dickens opines that “Le discloses a charge pump circuit to supply voltages to memory devices and describes using shunt regulator 270 to regulate the output voltage of the charge pump circuit.” Ex. 1003, ¶ 142. “A POSITA who read the description of Le’s charge pump circuit and wanted to know more about how a shunt regulator can be used to regulate the output voltage, would have looked at other sources of information about shunt regulators ... a POSITA considering additional references to know about shunt regulators would have found that Ujiie is one such reference.” *Id.*, ¶¶ 142-143. Based on this, Dr. Dickens concludes that a “POSITA accordingly would have understood that Ujiie’s shunt circuit can be used as a shunt regulator in Le’s charge pump circuit to regulate the pump output voltage, as a matter of design choice” and “would have conceived a modification to Le’s charge pump circuit based on Ujiie’s shunt regulator circuit.” *Id.*, ¶ 143. I disagree with Dr. Dickens’ conclusion.

84. As noted above, Le’s design goal is to minimize the use of the shunting regulator to minimize power consumption within the memory device. Adding Ujiie’s clamp diodes would potentially maximize the use of the shunting

regulator as one or more clamp diodes would be in a constant state where current is flowing through the diode. This runs counter to Le's design goal.

85. Le's charge pump generates only a single output voltage, at a value close to, but below, the voltage where the shunt regulator would be active. In combination with Ujiie's clamp diodes, Le's charge pump circuit would have to generate the highest output voltage required by the proposed combined circuit. For example, if there are three output voltages, 5 V, 10 V and 20 V, that can be selected with Ujiie's clamp diodes, Le's charge pump would have to be designed to generate 20 V. Le's inventive, i.e., non-prior art, charge pump would therefore generate 20 V with minimal ripple, so a clamping diode with a breakdown voltage at, e.g., 20.1 V (100 millivolts above 20 V), could be used. Based on the disclosure of Le, a POSITA would expect that the 20.1 V clamping diode would be used minimally when the pump is generating 20 V using Le's proposed invention to minimize ripple.

86. However, when an output voltage less than 20 V is required, for example 10 V or 5 V as I noted above, the respective clamp diodes associated with each of those output voltages in the proposed Le-Ujiie charge pump circuit would be used maximally, i.e., constantly, while those outputs are generated. While in use, those clamp diodes would be required to sink significant amounts of current to reduce Le's charge pump's 20 V output to 10 V or 5 V. This runs counter to Le's

goal of reducing power consumption by reducing the use of a shunt regulator through fine capacitance control within the charge pump. The proposed Le-Ujiie charge pump circuit would radically increase power consumption when 10 V or 5 V outputs are required.

87. A POSITA would recognize that applying Ujiie's multiple clamp diodes to Le's inventive charge pump dissipates significantly more power when clamp diodes with breakdown voltages less than Le's charge pump's output voltage are coupled to the pump output. Watt's law (where power is equal to current multiplied by the voltage drop) tells us that the diodes, by reducing the output voltage, necessarily dissipate power in relationship to how much voltage is reduced. A POSITA would thus recognize that the usefulness of Ujiie's clamp diodes for voltage reduction is directly related to how much power they consume. The voltage reduction from 20 V to 10 V or 5 V is very significant and the Le-Ujiie charge pump circuit would be expected to sink approximately half the power generated to reduce the output voltage from to 10 V and approximately three-quarters the power generated to reduce the output voltage from to 5 V. This is directly contrary to Le's goal of providing "a low power, low noise means of compensation for the variations in the V_{CC} supply applied to the charge pump circuit, while maintaining a simple regulator design." Ex. 1008, 4:15-18. Based on

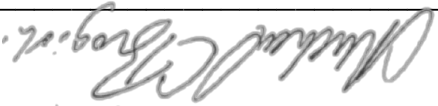
this, a POSITA would not be motivated to combine Ujiie's clamp diodes with Le's charge pump circuit.

88. Dr. Dickens opines that the power consumption of the Le-Ujiie combination could be curtailed by including the capability to turn off the charge pump when it reaches the breakdown voltage of the clamp diode (V_{pp1} , V_{pp2}), for example by including the control circuit from Kuriyama, U.S. Patent No. 6,373,325. *See* Ex. 1003, ¶ 167. I disagree that a POSITA would be motivated to make this combination. It is not a design choice as Dr. Dickens suggests. While it may reduce the power consumption across Ujiie's clamp diodes, it reintroduces other problems Le sought to resolve, namely that of excessive ripple and noise spikes and valleys as both the charge pump and shunt regulator (Ujiie's clamp diode) turn on and off. As Le noted, "[b]ecause of the internal regulation feedback and response time delays within the shunt regulator, the shunting transistors will not be able to react immediately to the over-voltage level, thereby causing the charge pump voltage to continue to rise beyond the target regulation voltage before the shunting transistors can respond with adequate conduction. Given the typical feedback-response delay of the shunt regulator 270, the conventional charge pump 200 will produce an increased ripple magnitude (e.g., about 400 mV P-P ripple at about 9 volt output) at the output 280 when the input supply voltage 210 is high." Ex. 1008, 3:52-62. In the circumstance of the charge pump turning on and off, the

feed-back response delay, now between both shunt regulator operation and charge pump operation will only lead to greater ripple in the output voltage and a higher degree of noise spikes and valleys associated with both the shunt regulator and charge pump turning on and off. Based on this, a POSITA would not be motivated to combine Ujiie's clamp diodes with Le's charge pump circuit and Kuriyama's charge pump control.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true.

March 11, 2024



Michael C. Brogioli, Ph.D.