

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY INC.,

Petitioner,

v.

SONRAI MEMORY LIMITED,

Patent Owner.

Case IPR2023-00909

Patent 6,724,241

PATENT OWNER'S RESPONSE

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PATENT OWNER’S EXHIBIT LIST

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2001	Plaintiff’s Notice of IPR Petition, <i>Sonrai Memory Limited v. Micron Technology, Inc.</i> , No. 6:22-cv-0085-ADA, Dkt. No. 40 (W.D. Tex. May 22, 2023)
2002	Order Granting Motion for Entry of Scheduling Order, <i>Sonrai Memory Limited v. Micron Technology, Inc.</i> , No. 6:22-cv-0085-ADA, Dkt. No. 40 (W.D. Tex. May 22, 2023)
2003	Docket Sheet, <i>Sonrai Memory Limited v. Micron Technology, Inc.</i> , No. 6:22-cv-0085-ADA (W.D. Tex. Sept. 10, 2023)
2004	Law360 Article: <i>West Texas Judge Says He Can Move Faster Than PTAB</i>
2005	Order Granting Joint Motion for Extension of Time To Extend Venue Discovery and Claim Construction Deadlines, <i>Sonrai Memory Limited v. Micron Technology, Inc.</i> , No. 6:22-cv-0085-ADA, Dkt. No. 51 (W.D. Tex. Aug. 3, 2023)
2006	Text Order Denying Motion to Stay Pending IPR, <i>Solas OLED Ltd. v. Google, Inc.</i> , Case No. 6:19-cv-00515-ADA (W.D. Tex. June 23, 2020)
2007	Order Denying Motion to Stay Pending IPR, <i>Multimedia Content Management LLC v. DISH Network L.L.C.</i> , Case No. 6:18-cv-00207-ADA, Dkt. No. 73 (W.D. Tex. May 30, 2019)
2008	U.S. District Courts—Federal Court Management Statistics—Profiles—During the 12-Month Periods Ending June 30, 2018 Through 2023 available at https://www.uscourts.gov/statistics/table/na/federal-court-management-statistics/2023/06/30-1
2009	Micron Technology, Inc’s Preliminary Invalidity Contentions, <i>Sonrai Memory Limited v. Micron Technology, Inc.</i> , No. 6:22-cv-0085-ADA (W.D. Tex. June 7, 2023)

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2010	Amended Scheduling Order, <i>Sonrai Memory Limited v. Apple Inc.</i> , No. 6:22-cv-00787-ADA, Dkt. No. 79 (W.D. Tex. Sept. 5, 2023)
2011	Claim Construction Order, <i>Sonrai Memory Limited v. Apple Inc.</i> , No. 6:22-cv-00787-ADA, Dkt. No. 53 (W.D. Tex. Apr. 6, 2023)
2012	Apple Inc.’s First Supplemental Invalidity Contentions, <i>Sonrai Memory Limited v. Apple Inc.</i> , No. 6:22-cv-00787-ADA (W.D. Tex. June 15, 2023)
2013	Declaration of Dr. Michael C. Brogioli
2014	Curriculum Vitae of Dr. Michael C. Brogioli
2015	Joint Claim Construction Statement, <i>Sonrai Memory Limited v. Micron Technology, Inc.</i> , No. 6:22-cv-0085-ADA, Dkt. No. 70 (W.D. Tex. October 18, 2023)
2016	Preliminary Claim Constructions, <i>Sonrai Memory Limited v. Micron Technology, Inc.</i> , No. 6:22-cv-0085-ADA (W.D. Tex. November 14, 2023)

I. INTRODUCTION

Patent Owner Sonrai Memory Ltd. (“Patent Owner”) submits this response to Petitioner Micron Technology Inc.’s (“Petitioner”) Petition for *inter partes* review of U.S. Patent No. 6,724,241 (“the ’241 Patent”).

First, the Board should find the claims of the ’241 Patent not unpatentable because Petitioner fails to show invalidity for any independent claim.¹ For Grounds 1A and 1B, Petitioner asserts that either *Doluca* alone, or *Doluca* in combination with *Buti*, disclose the limitations for independent claims 1, 13 and 24. However, neither *Doluca* alone, nor *Doluca* in combination with *Buti*, disclose charge pumps, for example, that “generate a selected one of a plurality of pump voltages,” that have “a plurality of loads, ... each load associated with a specific pump voltage,” or that have “a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit.” Consequently, Petitioner cannot establish that the limitations of the independent

¹ The Petition asserts invalidity of the independent claims in Ground 1A (addressing independent claims 1 and 24 under the combination of *Doluca* and *Buti*), Ground 1B (addressing independent claim 13 under the combination of *Doluca*, *Buti* and *Hosono*), Ground 2A (addressing independent claim 1 under the combination of *Le* and *Ujiie*), Ground 2B (addressing independent claim 24 under the combination of *Le*, *Ujiie* and *Kuriyama*), and Ground 3A (addressing independent claim 13 under the combination of *Asano*, *Le*, *Ujiie* and *Kuriyama*). Grounds 2C and 3B only address dependent claims.

claims are satisfied by the prior art and therefore cannot establish that any of the claims of the '241 Patent are unpatentable under Grounds 1A and 1B.

Second, Grounds 2A, 2B, 2C, 3A, and 3B are deficient because they rely on conclusory allegations of obviousness for the proposed combination of *Le* with *Ujiie*. Specifically, Grounds 2A, 2B, 2C, 3A, and 3B advocate for combining the charge pump circuit taught by *Le* with the clamp diode technique taught by *Ujiie* when the proposed combination would add drawbacks to *Le*'s charge pump circuit. A POSITA would understand that the proposed combination would be **detrimental** to *Le* because it contradicts *Le*'s stated goal of minimizing the power consumption in the use of a shunt regulator. Ex. 1008, 6:1-25, 10:61-11:6. The Petition fails to recognize that *Le*'s use of adjustable charge pump capacitance allows *Le*'s charge pump to meet output voltage goals with lower supply voltage while avoiding the excess output voltage ripple associated with larger capacitance, thereby avoiding the power consumption issues in a shunt regulator. A POSITA would thus **not** have been motivated to make the proposed combination. At most, the Petition establishes that a POSITA **could** have made its proposed modification to *Le* not that a POSITA **would have been motivated** to do so as required. The Petition's failure to show why a POSITA would have made the proposed combination of *Le* with *Ujiie* is the reason why Grounds 2A, 2B, 2C, 3A, and 3B of the Petition fail.

For the above reasons, and as explained in further detail below, the Petition fails to establish that any challenged claims are unpatentable.

II. BURDEN OF PROOF

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). This burden of persuasion never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (discussing the burden of proof in *inter partes* review). Furthermore, the petitioner cannot satisfy its burden of proving obviousness by employing “mere conclusory statements.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016). “The petitioner must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.” *Id.* To prevail in an *inter partes* review, Petitioner must show by a preponderance of the evidence that a patent is invalid. 35 U.S.C. § 316(e).

III. THE ‘241 PATENT

The ’241 Patent generally describes charge pump circuits in semiconductor devices for generating multiple output voltages that can maintain a low degree of

voltage ripple on each of output voltages. More specifically, the “ripple phenomenon is very critical when a charge pump circuit 100 has to provide any of several different regulated V_{out} values ... [w]hen a single charge pump circuit 100 has to furnish more than one V_{pump} value ranging from a very low to a very high value.” Ex. 1001, 2:16-20. “Usually, a charge pump output (V_{pump}) that is significantly less than the maximum output (V_{max}) experiences a ripple voltage signal caused by the sharing of charge between the capacitance of the pump circuit and that of the load circuit.” *Id.*, 2:3-7.

The '241 Patent gives an example of a charge pump that will be used to generate three output voltages, V_A , V_B (twice the value of V_A), and V_C (four times the value of V_A), and demonstrates that the ripple of the output voltage will be greater for the lower output voltages, e.g., V_A , and decrease as the output voltage approaches the charge pump maximum. *See id.*, 2:29-33, Figs. 2A, 2B, 2C. To address the circumstances where a charge pump is generating multiple output voltages, the '241 Patent proposes a charge pump with a “plurality of loads ... connectable to the charge pump output, each load associated with a specific target pump voltage” and a “load selector means [that] couples a selected load to the output according to the target pump voltage.” *Id.*, 3:10-14.

To that end, the “charge pump circuit 300 includes several different loads 322, 326, and 330, each connectable via a respective switch 320, 324, 328 to the

output 334 of the charge pump circuit. Depending on the desired pump output V_{out} , the switches select an appropriate load associated with a specific pump voltage to result in a minimum voltage ripple.” *Id.*, 4:2-8. “Loads can be capacitors or current sinkers. Each load is associated with a different pump output voltage V_{out} . The number of loads provided to the circuit may vary, depending on the number of target pump voltages that can be provided.” *Id.*, 4:35-38; see also *id.*, 6:43-48 (“When contained in a flash memory, the charge pump circuits 600 would typically receive an external supply voltage V_{cc} and generate a plurality of switchable voltage $V_P \dots$ ”).

The '241 Patent provides Fig. 3 and further elaborates:

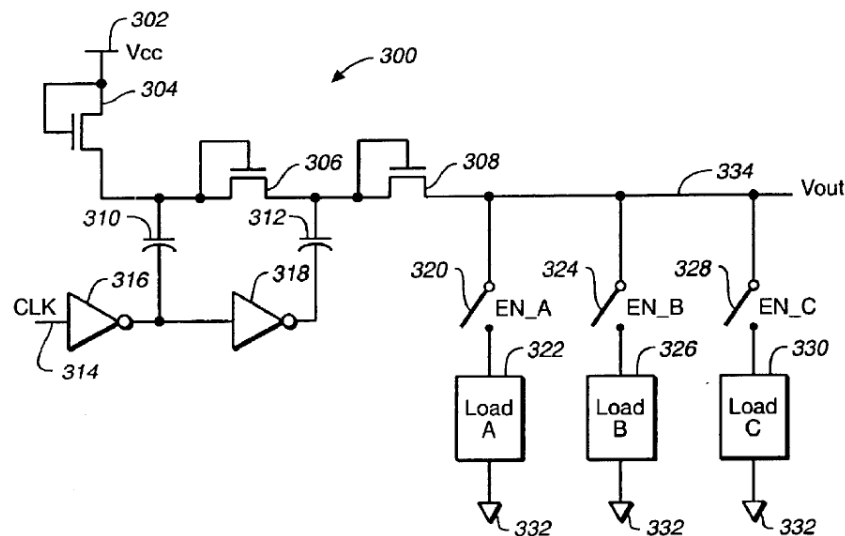


FIG._3

The first load 322 is associated with a pump output voltage V_A and is connected to a first switch 320. The first switch is enabled by a control signal EN_A. Similarly, the second load 324 is associated with a pump

output voltage VB and is connected to a second switch 324. The second switch 324 is enabled by EN_B. Finally, the third load 330 is associated with a pump output voltage VC and is connected to a switch 328. The third switch 328 is enabled by EN_C.

* * *

Only one load can be selected at a time. For example, if voltage VA is selected, EN_A causes the first switch 320 to close, connecting the first load to the output terminal of the charge pump circuit 300. The remaining loads 326 and 330 are disconnected from the output terminal because their respective switches 324 and 328 are open.

Id., Fig. 3, 4:40-62; *see also* Petition at 4.

As Dr. James Dickens, Petitioner's expert, asserts, "[t]he '241 Patent explains that each load (e.g., Load A, B, or C) is 'associated' with a specific pump voltage and that the load is attached to the output when that specific pump voltage is selected ... The attachment of the load is triggered by the pump voltage selection, not a later event." Ex. 1003, ¶ 50 (citing Ex. 1001, 4:33- 51, 7:7-16, 7:31-42); *see also* Petition at 13 (The '241 Patent describes "selectable loads, each of which is associated with a voltage level and are attached to Vout when that voltage level is desired").

A. The Claims of the '241 Patent

Independent Claim 1 of the '241 Patent recites:

[1pre] A charge pump circuit for generating a charge pump voltage having minimal voltage ripples, comprising:

[1a] a pumping circuit comprising one or more stages operable to receive a supply voltage and generate a selected one of a plurality of pump voltages;

[1b] a plurality of loads selectively coupleable to an output of the pumping circuit, each load associated with a specific pump voltage; and
[1c] a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit.

Ex. 1001, 8:16-26.

Consistent with the disclosure of the '241 Patent, Claim 1 requires “a pumping circuit ... to receive a supply voltage and generate a selected one of a plurality of pump voltages.” *Id.*, 8:18-20. Claim 1 further requires that there be a “plurality of loads ... each load associated with a specific pump voltage,” *id.*, 8:21-23, and that there be a “load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit,” *id.*, 8:24-26. Based on the totality of the claim, it requires that the loads and consequently the output voltage of the pumping circuit be dynamically selectable.

The claim expressly recites that the “pumping circuit” has to “generate a selected one of a plurality of pump voltages.” Because the claim should be interpreted “with an eye toward giving effect to all terms in the claim,” *Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 950 (Fed. Cir. 2006) (citations omitted), a reading of the claim that does not require the output voltage to be selectable, from among a group of possible output voltages, is improper because it renders the phrase “selected one of a plurality of pump voltages” superfluous and meaningless.

Moreover, the other limitations of the claim reinforce that the output voltage of the pumping circuit be dynamically selectable.

First, limitation [b] requires that there be a “plurality of loads selectively coupleable to an output of the pumping circuit, each load associated with a specific pump voltage.” Ex. 1001, 8:21-23. Because each load is “associated with a specific pump voltage,” i.e., each load is clearly tied to a particular pump voltage, this limitation reinforces that the pumping circuit must be able to generate two or more pump voltages. *See also id.*, 4:40-46 (“The first load 322 is associated with a pump output voltage VA ... the second load 324 is associated with a pump output voltage VB ...”). In an earlier *inter partes* review of the ’241 Patent, the petitioners’ expert similarly noted that “a POSITA would deduce that a load is “associated” with a voltage if the load was predetermined to be particularly suited for that voltage such that the load will be used with that voltage in all situations and not just on an as-needed basis.” IPR2021-01561, Ex. 1003 (Declaration of Vivek Subramanian, Ph.D.), ¶ 42.

Second, limitation [c] requires a “load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit.” Ex. 1001, 8:24-26. The parties agree that this is a means-plus-function limitation. *See* Ex. 2015, Joint Claim Construction Statement, at 2. The agreed recited function is “selectively coupling a load associated with a specific

pump voltage to the output of said pumping circuit.” *Id.* Petitioner’s expert, Dr. Dickens has also opined that the recited function means “choosing a load based on the target pump voltage, such that the load is coupled to the output of the pumping circuit when the target pump voltage is selected.” Ex. 1003, ¶ 49. This reinforces that the output voltage of the pumping circuit has to be dynamically selectable.

The corresponding structure for this limitation has been construed by the Court in the corresponding district court case as: “(i) a plurality of switches (320, 324, and 328) as shown in Figure 3 and associated descriptions in the specification, or shown in Figure 7 (720, 724, 728) and associated descriptions in the specification; (ii) a plurality of transistors 504A as shown in Figure 5A and associated descriptions in the specification; or (iii) a plurality of elevator circuits 502B and transistors 504B as shown in Figure 5B and associated descriptions in the specification; and equivalents thereof.” Ex. 2016, *Preliminary Claim Constructions*. The specification makes clear that the selection of a particular load, associated with a specific voltage, is to the exclusion of other loads associated with other specific voltages. Ex. 1001, 4:56-62 (“Only one load can be selected at a time. For example, if voltage VA is selected, EN_A causes the first switch 320 to close, connecting the first load to the output terminal of the charge pump circuit 300. The remaining loads 326 and 330 are disconnected from the

output terminal because their respective switches 324 and 328 are open.”), 5:4-6, 5:15-17; *see also id.*, 4:35-36 (“Each load is associated with a different pump output voltage V_{out} .”).

Claim 13 of the '241 Patent similarly recites “a pumping circuit ... to receive a supply voltage and generate one or more pump voltages,” *id.*, 10:26-28, “a plurality of loads, each load associated with a specific pump voltage and selectively coupleable to an output of the pump circuit (output pump),” *id.*, 10:29-31, and “a load selector means coupled to the output pump for selecting a load that satisfies a specific pump voltage,” *id.*, 10:32-33. Claim 24, a method claim, recites “selecting a output pump voltage (V_{pump}),” *id.*, 12:36, and “turning on a load associated with the selected V_{pump} ,” *id.*, 12:37. All of the claims of the '241 Patent require selection of an output voltage from among a group of possible voltages. In other words, to meet each of the claims, a circuit must be capable of generating multiple output voltages from which a particular output voltage may be selected.

IV. OVERVIEW OF *DOLUCA*, *BUTI*, *LE* AND *UJIE*

A. *Doluca*

U.S. Patent No. 4,769,784 to Doluca et al. (“*Doluca*”) generally describes a charge pump circuit “to produce a capacitor-plate bias voltage suitable for use in a CMOS DRAM using a $V_{CC}/2$ sense scheme.” Ex. 1006, 1:64-66. *Doluca* describes

the capacitive memory cell with respect to Fig.1, reproduced below. “A capacitive memory element 3 has an anode electrode 5 and a cathode electrode 7. Cathode 7 is connected to a storage node 9, while anode electrode 5 is connected, in common with the anodes of the other capacitive memory elements in the matrix-array memory device (not shown) of which cell 1 is a part, to a capacitor-plate node 11.” *Id.*, 2:66-3:5; *see also* Ex. 2013, Brogioli Declaration, ¶ 38.

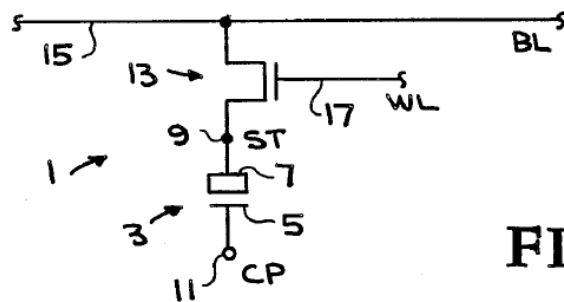


FIG. 1

Ex. 1006, Fig. 1. At the storage node 9, logic level 0 is represented by 0 volts and logic level 1 is represented by V_{CC} . *Id.*, 3:11-13; *see also* Ex. 2013, ¶ 38.

The “[c]apacitor 3 is formed with a silicon cathode, a polysilicon anode, and with a relatively thin dielectric layer of, for example, 150 Angstroms of SiO_2 separating its cathode and anode.” Ex. 1006, 3:17-20. The capacitive structure has a threshold voltage V_T , depending on temperature, of approximately 0.4 to 1.0 volts. *Id.*, 3:20-22; *see also* Ex. 2013, ¶ 39. “Consequently, the capacitor-plate node 11 must always be held at a voltage which is more positive than the voltage of the storage node 9 by V_T volts or more.” Ex. 1006, 3:22-25. This means that the

capacitor voltage must always be held at $V_{CC} + V_T$ volts. With V_{CC} at 5V and V_T at 1V, the capacitor voltage must be held at more than 6V. See Ex. 2013, ¶ 39.

With further reference to Fig. 1, *Doluca* describes the “ $V_{CC}/2$ sense scheme,” where the bit-line 15 is pre-charged to $V_{CC}/2$, the midpoint between zero volts and V_{CC} , prior to connecting to the storage node 9 through word-line 17 controlled transistor 13. Ex. 1006, 3:13-16; see also Ex. 2013, ¶ 40. *Doluca* further discloses that the capacitor plate voltage can defined in terms of $V_{CC}/2$. See Ex. 1006, 3:35-38 (“[S]ince the bit-line pre-charge voltage is $V_{CC}/2$, the voltage of the capacitor-plate bias source should be function of $V_{CC}/2$ such that it follows any variations of bit-line voltage exactly.”); see also Ex. 2013, ¶ 40. “Taking these requirements together, we can say that the ideal capacitor-plate bias source should produce a voltage: $V_{CP} = V_{CC}/2 + K$, where K is a constant having a value: $K > V_{CC}/2 + V_T$.” Ex. 1006, 3:39-45; see also Ex. 2013, ¶ 40.

With V_{CC} at 5V and V_T at 1V, K must be greater than 3.5V. See Ex. 2013, ¶ 40. *Doluca* suggests “that K might be chosen to be 3.5 to 4, resulting in a value of V_{CP} of approximately 6 to 6.5 volts.” Ex. 1006, 3:49-50. This provides some flexibility in generating V_{CP} . See Ex. 2013, ¶ 40 (“*Doluca* places the top of the range of K at 4 V ... although a POSITA would recognize that a higher top of the range could be sustained without damaging the capacitor.”). Notably, *Doluca* does not describe generating K , but rather describes circuitry that achieves the minimum

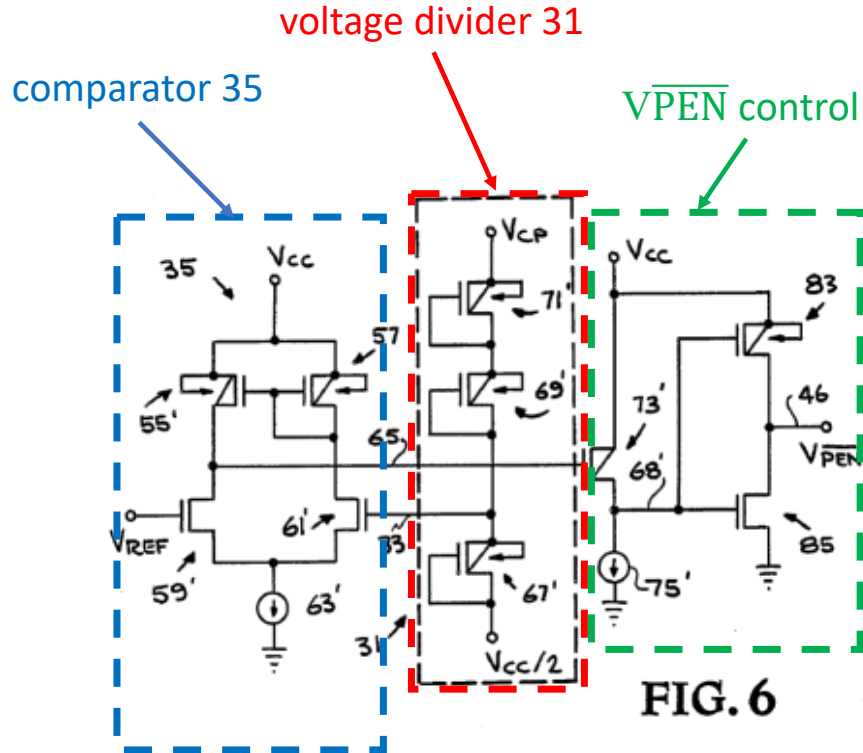
required capacitor plate voltage based on V_{CC} and the bandgap voltage of silicon, V_{BG} . *See* Ex. 2013, ¶ 41. The circuitry first consists of “[a] $V_{CC}/2$ circuit 21, which may be nothing more than a voltage divider, connects to a source of voltage V_{CC} at its input, and provides a voltage $V_{CC}/2$ to a V_{BG} generator 23 at its output. V_{BG} generator 23 generates a voltage V_{BG} which is a stable facsimile of the bandgap voltage of silicon, or about 1.2 volts.” Ex. 1006, 3:62-67; *see also* Ex. 2013, ¶ 41. “The output of generator 23, consisting of the sum of $V_{CC}/2$ and V_{BG} is connected to a V_{REF} line 25, such that: $V_{REF} = V_{CC}/2 + V_{BG}$.” Ex. 1006, 4:4-8; *see also* Ex. 2013, ¶ 41.

The circuitry also consists of a typical charge pump circuit, shown in Fig. 3. The charge pump is enabled by the signal $\overline{VPEN}$. *See* Ex. 2013, ¶ 43. Finally, the circuitry also includes the pump control circuit 29, shown in Fig. 6, reproduced below. The pump control circuit further consists of voltage divider circuitry 31 that produces an output on line 33 of $V_{33} = (V_{CP} - V_{CC}/2)/3 + V_{CC}/2$. *See* Ex. 1006, Fig. 6 (portion highlighted in red below); *see also* Ex. 2013, ¶ 43. V_{33} is compared to V_{REF} in comparator 35 circuitry, *see* Ex. 1006, Fig. 6 (portion highlighted in blue below):

The output of comparator 35 on line 65' goes low whenever V_{33} drops below V_{REF} , and this low output is coupled through a driver transistor 73' to the commonly connected gates of an inverting output pair of transistors 83 and 85. The high voltage on the common gate connection of these transistors turns transistor 83 off, and transistor 85 on. As a

result, the output voltage on the line 46 drops, initiating the active low $\overline{VPEN}$ output signal on line 46.

Id., 7:15-23, Fig. 6 (portion highlighted in green below).



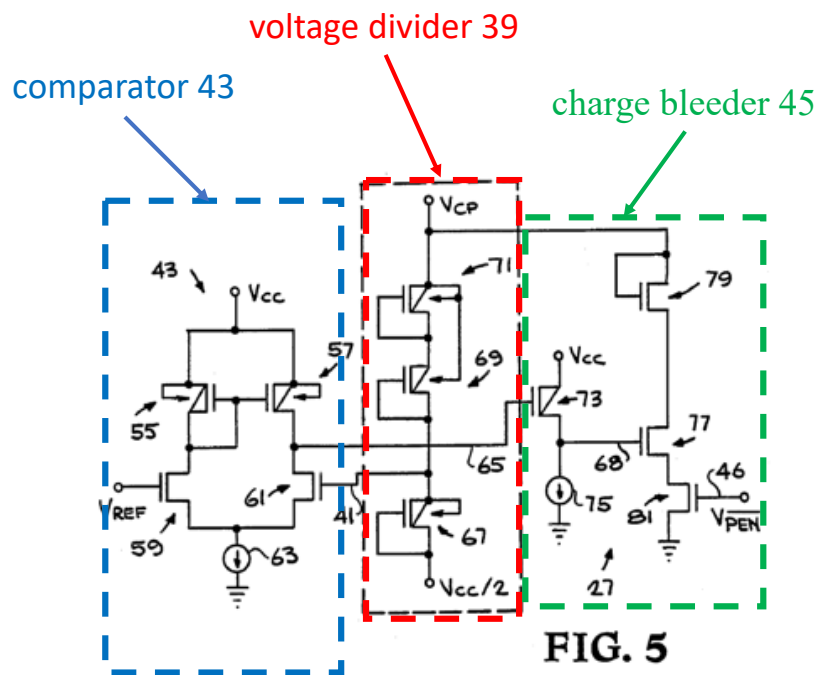
Id., Fig. 6 (annotated); *see also* Ex. 2013, ¶¶ 42, 43.

In other words, the charge pump is activated when: $(V_{CP} - V_{CC}/2)/3 + V_{CC}/2 \leq V_{CC}/2 + V_{BG}$. *See* Ex. 2013, ¶ 43. Simplifying further, the charge pump is activated when: $(V_{CP} - V_{CC}/2)/3 \leq V_{BG}$. Simplifying yet even further, the charge pump is activated when: $V_{CP} - V_{CC}/2 \leq 3V_{BG}$. Isolating V_{CP} , the charge pump is activated when: $V_{CP} \leq 3V_{BG} + V_{CC}/2$. Ex. 1006, 4:30-51; *see also* Ex. 2013, ¶ 43. With V_{CC} at 5V and V_{BG} at 1.2V, the charge pump is activated when V_{CP} is less than or equal to 6.1V, in excess of $V_{CC} + V_T$. *See id.*, ¶ 43. Because

Doluca requires the charge pump circuitry to produce at least $V_{CP} = V_{CC}/2 + K$, and because the charge pump circuitry produces at least $V_{CP} = V_{CC}/2 + 3V_{BG}$, *Doluca* describes the “design criteria” of K as satisfied by $3V_{BG}$. That is, the design criteria is satisfied in *Doluca*’s circuitry using the fixed structures of (i) the circuitry to generate V_{BG} at 1.2V; and (ii) the voltage divider circuitry to generate $V_{CP} - V_{CC}/2)/3 + V_{CC}/2$. *Doluca* consequently describes only generating a single V_{CP} output voltage.

Because a POSITA would recognize that the V_{CP} generated by the charge pump circuit will overshoot 6.1V due, *inter alia*, to transistor switching delays in disabling the charge pump, *Doluca* also describes a charge bleeder control circuit 27, shown in Fig. 5, reproduced below, for maintaining an approximate upper boundary to which V_{CP} will overshoot. Similar to the pump control circuit 29, the bleeder control circuit includes voltage divider 39. *See* Ex. 1006, Fig. 5 (portion highlighted in red below); *see also* Ex. 2013, ¶ 44. However, this voltage divider differs from the voltage divider of the pump control circuit 29 in that the source of transistors 69 is connected to the substrate of transistor 71 instead of in its normal manner as with transistor 67 and 71, as well as with all of the transistors in the voltage divider 31 of pump control circuit 29. *See* Ex. 1006, 6:36-41; *see also* Ex. 2013, ¶ 44. “The effect of this asymmetry is to cause the voltage drop across transistor 69 to be increased by a small amount while the voltage drop across each

of the other transistors is decreased by a small amount ... If we arbitrarily call the increase in the voltage across transistor 69 2Δ , then the decrease in drop across each of the other transistors is one half of this amount, or Δ . Consequently, the voltage output from divider 39 at line 41 is: $V_{41} = [(V_{CP} - V_{CC}/2)/3] + V_{CC}/2 - \Delta$,” Ex. 1006, 6:41-51; *see also* Ex. 2013, ¶ 44.



Ex. 1006, Fig. 5 (annotated)); *see also* Ex. 2013, ¶¶ 42, 44.

The output on line 41 (V_{41}) is compared to V_{REF} in comparator 43. *See id.*, Fig. 5 (portion highlighted in blue above); *see also* Ex. 2013, ¶ 44. When V_{41} is greater than V_{REF} and $\overline{VPEN}$ is inactive (*i.e.*, logical 1 meaning the charge pump is not enabled), transistor 73 causes transistor 77 to allow current to flow through current-regulating transistor 79 and transistor 81 to ground. This bleeds charge, and

consequently voltage, from V_{CP} . *See* Ex. 1006, Fig. 5 (portion highlighted in green above); *see also* Ex. 2013, ¶ 44.

In other words, the charge bleeder is activated when the charge pump is inactive and: $(V_{CP} - V_{CC}/2)/3 + V_{CC}/2 - \Delta \geq V_{CC}/2 + V_{BG}$. *See* Ex. 2013, ¶ 44. Simplifying further, the charge bleeder is activated when the charge pump is inactive and: $(V_{CP} - V_{CC}/2)/3 - \Delta \geq V_{BG}$. Simplifying yet even further, the charge bleeder is activated when the charge pump is inactive and: $V_{CP} - V_{CC}/2 - 3\Delta \geq 3V_{BG}$. Isolating V_{CP} , the charge bleeder is activated when the charge pump is inactive and: $V_{CP} \geq 3V_{BG} + V_{CC}/2 + 3\Delta$. *See* Ex. 1006, 4:52-5:8. With V_{CC} at 5V, V_{BG} at 1.2V, and Δ a small offset voltage, the charge bleeder is activated when the charge pump is inactive and V_{CP} is greater than or equal to 6.1V plus a small offset voltage. *See* Ex. 2013, ¶ 44.

Doluca's circuits avoid simultaneous operation of the charge pump and the charge bleeder: “(1) the voltage V_{CP} at which the bleeder turns off is greater than the voltage V_{CP} at which the pump turns on by 3Δ ; (2) the $\overline{VPEN}$ voltage produced by comparator 35 is fed back along line 46 to bleeder control circuit 27, where it disables charge bleeder 45 whenever charge pump 37 is in operation.” Ex. 1006, 5:13-19. This allows V_{CP} to maintain a range close to 6.1V to 6.1V plus a small offset voltage.

B. Buti

U.S. Patent No. 5,872,733 to Buti et al. (“*Buti*”) generally describes “a control circuit for accurately and efficiently controlling the ramp-up rate of a charge pump used for programming flash memory devices.” Ex. 1005, 1:53-56; *see also* Ex. 2013, ¶ 57. For example, Fig. 6 of *Buti* shows the ramp-rate for a charge pump circuit used to generate 12.95 V when no ramp-rate control is used (curve A), and when two of *Buti*’s ramp-rate control embodiments are used (curves B and C):

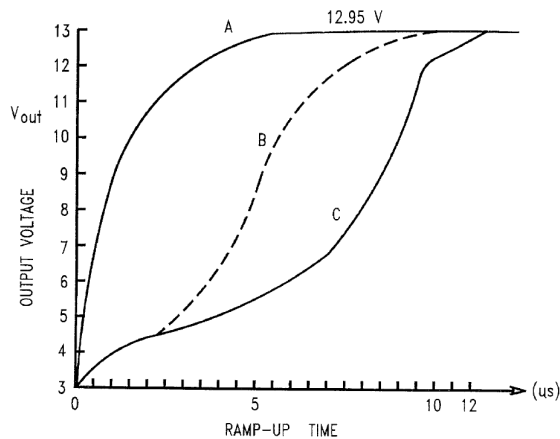


FIG. 6

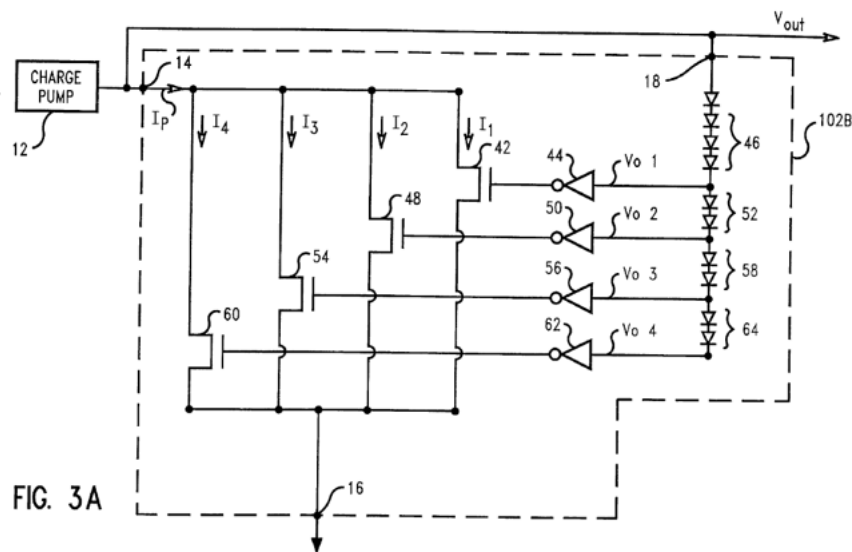
Ex. 1005, Fig. 6; *see also* Ex. 2013, ¶ 57.

FIG. 6 shows a comparison of the charge pump ramp-up rate with and without the ramp-up rate control circuit of the present invention. Referring to Curve A, the ramp-up time without the ramp-up rate control circuit of the present-invention is about 3 us (microseconds) for a maximum charge pump output voltage V_{out} of about 12.96 volts. Referring to Curve B, the ramp-up time with the circuit 102B of FIG. 3A is about 8 us (microseconds) for the same maximum charge pump output voltage. Referring to Curve C, the ramp-up time with the circuit 100 of FIG. 5 is about 12 us (microseconds) for the same maximum

charge pump output voltage. Thus, the ramp-up rate of the programming voltage pulse is significantly reduced thereby preventing the peak tunneling current from overstressing the thin tunneling oxide layer of the flash memory device.

Ex. 1005, 9:8-22; *see also* Ex. 2013, ¶ 58.

Curve B in Fig. 6 reflects the operation of the charge bleeder circuit shown in Fig. 3A, which the Petition proposes as a substitute for the *Doluca* charge bleeder circuit:



Ex. 1005, Fig. 3A; *see also* Ex. 2013, ¶ 58.

FIG. 3A shows an alternate embodiment of the ramp-up control circuit of the present invention. Circuit 102B comprises multiple-current bleed paths wherein each path is configured as the circuitry shown in FIG. 2A. As shown in FIG. 3A, four (4) current bleed paths are used. Multiple-bleeding paths effect accurate control of bleeding current to ground potential for varying magnitudes of charge pump output voltage V_{out} . The total charge pump bleed current I_P is comprised of the four branch currents I_1 , I_2 , I_3 and I_4 . Each current bleed path has a corresponding turn-off voltage (V_{OFF}) that will turn off that particular bleed path. The first current bleed path is through n-channel FET 42

which is controlled by inverter 44 and diodes 46. The second current bleed path is through n-channel FET 48 which is controlled by inverter 50 and diodes 46 and 52. The third current bleed path is through FET 54 which is controlled by inverter 56 and diodes 46, 52 and 58. Similarly, the fourth current bleed path is through FET 60 which is controlled by inverter 62 and diodes 46, 52, 58 and 64. Although four (4) current paths are shown, the embodiment shown in FIG. 3A may be modified to have more or less than four (4) current paths. It is to be understood that the quantities of diodes 46, 52, 58 and 64 shown in FIG. 3A are for purposes of discussion only. The actual required quantities of diodes depends upon the desired operating characteristics.

Ex. 1005, 6:56-7:11; *see also* Ex. 2013, ¶ 59.

Buti further explains the operation of the Fig. 3A ramp-rate control circuit:

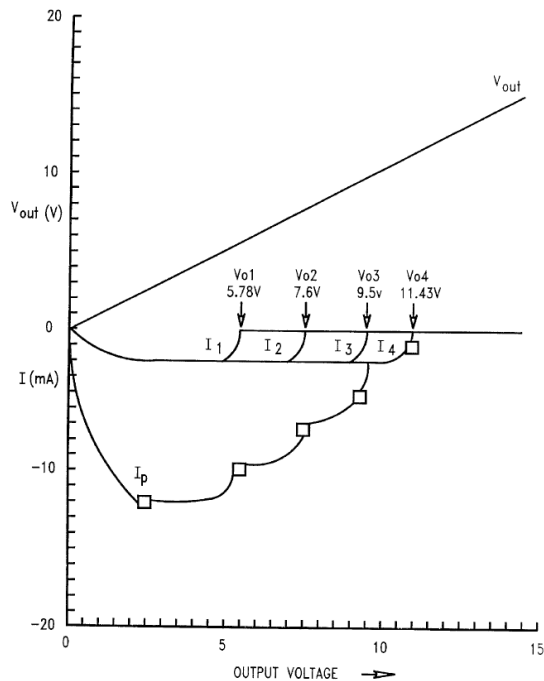


FIG. 3B

Ex. 1005, Fig. 3B; *see also* Ex. 2013, ¶ 60.

Referring to FIGS. 3A, 3B and Table 1, the first current bleed path is turned off first when charge pump output voltage V_{out} is about 5.78 volts. When V_{out} is about 5.78 volts, diodes 46 produce a series of

voltage drops that produce a voltage V_{01} which has a magnitude that constitutes a logic “1” voltage. In response to this logic “1” voltage, inverter 44 outputs a logic “0” voltage level which turns-off FET 42 thereby substantially eliminating the flow of current I_1 through FET 42. Increasing the number of diodes 46 will result in a higher charge pump output voltage being needed to turn off the first current bleed path. Similarly, fewer diodes will result in a lower charge pump output voltage being needed to turn off the first current bleed path.

The second current bleed path is turned off when charge pump output voltage V_{out} is about 7.6 volts. When V_{out} is about 7.6 volts, diodes 46 and 52 produce a series of voltage drops that produce a voltage V_{02} that has a magnitude that constitutes a logic “1” voltage. In response to this logic “1” voltage, inverter 50 outputs a logic “0” voltage level which turns-off FET 48 so as to substantially eliminate the flow of current I_2 through FET 48.

The third current bleed path is turned off when charge pump output voltage V_{out} is about 9.5 volts. When V_{out} is about 9.5 volts, diodes 46, 52 and 58 produce a series of voltage drops that produce a voltage V_{03} that has a magnitude that constitutes a logic “1” voltage. In response to this logic “1” voltage, inverter 56 outputs a logic “0” voltage level which turns-off FET 54 so as to substantially eliminate the flow of current I_3 through FET 54.

The fourth current bleed path is turned off when charge pump output voltage V_{out} about 11.43 volts. When V_{out} is about 11.43 volts, diodes 46, 52, 58 and 64 produce a series of voltage drops that produce a voltage V_{04} that has a magnitude that constitutes a logic “1” voltage. In response to this logic “1” voltage, inverter 62 outputs a logic “0” voltage level which turns-off FET 60 so as to substantially eliminate the flow of current I_4 through FET 60.

Ex. 1005, 7:12-46, 7:51-58 (Table 1); *see also* Ex. 2013, ¶ 60.

C. *Le*

U.S. Patent No. 6,424,570 to Le et al. (“*Le*”) generally describes a charge pump circuit for generating a single output voltage as precisely as possible by

accounting for variations in the input V_{CC} power supply by varying the capacitance values within the capacitor networks of the charge pump circuits.

Le describes a first prior art conventional charge pump. Ex. 1008, 2:52-3:3; *see also* Ex. 2013, ¶ 75. *Le* also describes a second prior art charge pump circuit as having “large capacitor values to accommodate the lowest power supply level, and the addition of a shunt regulator 270 attached at the conventional point of the charge pump output 280, to reduce the output when the supply or the output voltage is higher than a target value.” Ex. 1008, 3:7-12; *see also* Ex. 2013, ¶ 76. “The shunt regulator 280 regulates the charge pump output by partially shorting to ground that portion of the charge pump output which is greater than a desired voltage level. In this conventional method, large capacitor values may be used to compensate for the lowest power supply voltage.” Ex. 1008, 3:32-36; *see also* Ex. 2013, ¶ 77. Due to higher capacitor values to accommodate for lowest supply voltage levels, “the output of the charge pump 280 and the shunt regulator 270 experience a ripple voltage signal from the charge and discharge cycles, with a period which matches the clock cycle period. The ripple voltage level on the output rises during a charge cycle, and drops again as a function of the RC discharge of the load and the load capacitance C_{LOAD} 260.” Ex. 1008, 3:41-47; *see also* Ex. 2013, ¶ 77.

“The ripple voltage level rises during the charge cycle, until the shunt regulator determines that an over-voltage condition or target regulation voltage has

been reached, wherein the shunt regulator shunting transistors begin to conduct and shunt the over-voltage charge to ground.” Ex. 1008, 3:47-51; *see also* Ex. 2013, ¶ 77. *Le* further describes the problems with the conventional approach, including “increased ripple magnitude (e.g., about 400 mV P-P ripple at about 9 volt output) at the output 280 when the input supply voltage 210 is high,” Ex. 1008, 3:60-62, Ex. 2013, ¶ 78, and the “noise spikes and valleys ... produced on the output 280 as the shunting transistors in the shunt regulator 270 discharge the over-voltage on the charge pump capacitors to ground,” Ex. 1008, 3:63-66; *see also* Ex. 2013, ¶ 78. “[T]he charge pump circuit and shunt regulator circuit together as a system exhibit ***increased power consumption and reduced system efficiency.***” Ex. 1008, 4:8-11; *see also* Ex. 2013, ¶ 78. “Additionally, most device applications seek to consume a minimum of power from the supply, particularly in battery and other portable power device applications this is important.” Ex. 1008, 4:11-15; *see also* Ex. 2013, ¶ 78.

Le consequently introduces a “novel charge pump circuit where one or more individual stages of the charge pump is characterized by having a variable bootstrap capacitance value which is varied as a function of the input supply voltage.” Ex. 1008, 4:31-35; *see also* Ex. 2013, ¶ 79. “An advantage ... is the ability of the charge pump and shunt regulator system to produce a lower noise output, as compared to conventional charge pump and regulator systems without compensation.” Ex. 1008, 4:60-63; *see also* Ex. 2013, ¶ 79.

Le introduces a V_{CC} input supply voltage detection circuit and a charge pump compensation circuit to modulate the capacitive loading of the charge pump:

Referring now to the figures, FIG. 3 is a simplified schematic illustration of an exemplary system 300, according to the present invention, for generating a modulated charge pump voltage V_{OUT} 310 for flash memory cell operations, comprising ***a supply voltage detection circuit 365 configured to detect a supply voltage value 380 and generate one or more output signals 370 associated therewith.*** The system 300 further includes a charge pump circuit 305 comprising one or more stages operable to receive the supply voltage 380 and generate the charge pump output voltage V_{OUT} 310 having a value greater than the supply voltage 380, and ***a charge pump compensation circuit 390, operably coupled to the supply voltage detection circuit 365 and the charge pump circuit 305, and operable to receive the one or more output signals 370 from the supply voltage detection circuit 365 and modulate a capacitive loading (320, 330, 340, 350) associated with the charge pump circuit 305 based on the one or more supply voltage detection output signals 370.*** Such modulation produces a low power consumption charge pump, which generates a low ripple and low noise output V_{OUT} 310 which compensates for fluctuations of the input power supply (for example, V_{CC}).

Id. 7:4-25 (emphasis added); *see also id.* 8:58-10:20; *see also* Ex. 2013, ¶ 79.

“ V_{CC} variations which are typically reflected in the output of the conventional charge pump circuit are identified, and compensation for such variations are generated to thereby generate wordline or bitline voltages during various flash memory cell modes.” Ex. 1008, 6:17-21; *see also* Ex. 2013, ¶ 80. “Consequently, a shunt regulator circuit which may operate in conjunction with such a charge pump circuit will consume less power and regulate the charge pump output with less ripple than with conventional charge pump circuits.” Ex. 1008, 6:21-25; *see also* Ex. 2013,

¶ 80. “In addition, the charge pump circuit of the present invention provides for a further reduction in power consumption when used in conjunction with a shunt regulator. Note that in prior art charge pump circuits, at high VCC input voltages, the charge pump output voltage would greatly exceed the desired target output voltage, which required the shunt regulator to shunt the excess wasted charge to ground. The charge pump circuit of the present invention reduces an amount of such shunting by the regulator, thereby reducing power.” Ex. 1008, 10:61-11:3; *see also* Ex. 2013, ¶ 80.

D. *Ujiie*

Japanese Published Patent Application No. S61-024094 to Ujiie et al. (“*Ujiie*”) generally describes a charge pump circuit for generating write and erase voltages in electrically erasable programmable read-only memories (“EEPROM”) using clamp diodes with breakdown voltages formed to match the respective write voltage and erase voltage. Ex. 1009 at [22]; *see also* Ex. 2013, ¶ 81. Switch MOSFETs are connected in series with the clamp diodes and control signals applied to the MOSFETs govern the connection of the respective clamp diodes to the output of the charge pump. Ex. 1009 at [22]-[23]; *see also* Ex. 2013, ¶ 82.

V. GROUNDS 1A AND 1B FAIL BECAUSE THE *DOLUCA-BUTI* COMBINATION DOES NOT MEET THE LIMITATIONS OF THE INDEPENDENT CLAIMS

A. Claim 1 (Ground 1A)

1. *Doluca* does not “generate a selected one of a plurality of pump voltages”

Claim limitation [1a] of the '241 Patent requires “a pumping circuit ... to receive a supply voltage and generate a selected one of a plurality of pump voltages.” Ex. 1001, 8:19-21. As described above in Section II.A, *Doluca*’s circuitry generates only a single output voltage. Petitioner and its expert claim otherwise, asserting that *Doluca*’s charge pump will “provide VCP within a range depending on the value of K, which can be ‘chosen’ to be within a specified range,” and that, consequently, using a “chosen” value of K, “*Doluca*’s charge pump can ‘generate a selected one of a plurality of pump voltages.’” Petition at 19-20, citing Ex. 1003, ¶ 83. Petitioner and its expert are incorrect. As an initial matter, claim 1 of the '241 Patent requires a selectable pump voltage from a group of (“plurality of”) pump voltages. *See* Section II.A, *supra*.

K is a design criteria, “a constant having a value,” Ex. 1006 at 3:42-43, and cannot be modified in the charge pump circuitry. As Dr. Brogioli explains:

A POSITA would realize that K is not a selection mechanism to allow a charge pump circuit to generate multiple output voltages, but rather a mathematical design criteria that *Doluca* used to design the charge pump control circuitry, including voltage divider 33 and comparator 35, and the charge bleeder control circuitry, including voltage divider 41

and comparator 43. This mathematical design criteria allowed Doluca to design the capacitor plate voltage generation circuitry so that V_{CP} would respond to any fluctuations in $V_{CC}/2$, the bit-line pre-charge voltage. There is no K input to the Doluca capacitor plate voltage generation circuitry to allow that circuitry to generate any other voltage than that in the range of 6.1 V to 6.1 V *plus* a small offset voltage in Doluca's 5 V V_{CC} DRAM device. Not surprisingly, Dr. Dickens provides no analysis of how K can be "selected" as anything other than a design criteria for a 5 V V_{CC} DRAM device.

Ex. 2013, ¶ 47.

Dolucas charge pump circuitry generates a minimum of 6.1V ($V_{CC}/2 + 3V_{BG}$). Ex. 2013, ¶ 45. *Dolucas* does not teach or suggest such a modification, let alone a modification that can be made dynamically to allow the charge pump circuitry to generate more than one output voltage, V_{CP} . Because *Dolucas* does not "generate a selected one of a plurality of pump voltages," as required by claim 1, Petitioner's reliance on *Dolucas* is misplaced.

The Petition asserts an alternative theory—that *Dolucas* charge pump circuit can be modified to include *Buti's* charge bleeder circuitry, as shown below, to select from more than one pump output voltages. See Petition at 20, citing Ex. 1003, ¶84 (referencing ¶72 for the suggested *Dolucas-Buti* combination below). Petitioner and its expert, Dr. Dickens, assert that the alleged motivation to combine *Dolucas* and *Buti* is based on *Dolucas* providing no "structural or operational detail" regarding the operation of its charge bleeder. See Petition at 13, Ex. 1003, ¶ 70; see also Ex. 2013, ¶ 53. This assertion is contradicted by Dr. Dickens' own opinions elsewhere in his

declaration, *see* Ex. 2013, ¶ 54, and by *Doluca*'s own detailed disclosure. As Dr.

Brogioli explains:

Doluca discloses “current-regulating transistor 79” as the charge bleeder. “Current-regulating transistor 79” is shown in Fig. 5 and is further described “as a non-linear current regulator having a generally parabolic current-voltage characteristic.” Ex. 1006, 6:54-58. Doluca also describes how the “current-regulating transistor 79” will be active when $\overline{VPEN}$ is high and $(V_{CP} - V_{CC}/2)/3 + V_{CC}/2 - \Delta$ is greater than V_{REF} , or V_{CP} is greater than 6.1 V *plus* a small voltage. *See* Ex. 1006, Fig. 5, 6:59-63 (“A gate transistor 81 is connected with its drain to the source of transistor 77, and with its source to ground. The gate of transistor 81 receives the $\overline{VPEN}$ voltage on the line 46 and disables the bleeder 27 whenever charge pump 37 is on.”).

Ex. 2013, ¶ 54.

Furthermore, the Petition ignores that, unlike *Doluca*, *Buti* does not regulate the output voltage of its charge pump. If anything, *Buti*'s ramp-rate control circuit regulates the rate of increase of the output voltage when the charge pump is turned on. Ex. 2013, ¶¶ 55, 61. A POSITA would therefore not be motivated to combine *Doluca* with *Buti* as the Petition suggests.

Even considering the combination, a POSITA would realize that the proposed *Doluca-Buti* does not change the behavior of *Doluca*'s circuitry. Indeed, the Petition ignores that the proposed combination modifies the charge bleeder circuitry of *Doluca*, but not the charge pump circuitry. The charge pump circuitry will generate a V_{CP} of more than 6.1 V ($V_{CC}/2 + 3V_{BG}$) and then be disabled until V_{CP} falls below 6.1 V. *See* Ex. 2013, ¶¶ 43, 44; *see also* Ex. 1006, 5:15-19 (“the $\overline{VPEN}$ voltage

[highlighted in red below] produced by comparator 35 is fed back along line 46 to bleeder control circuit 27, where it disables charge bleeder 45 whenever charge pump 37 is in operation.”). *Doluca*, as modified by the charge bleeder circuitry of *Buti* as Petitioner suggests, does not “generate a selected one of a plurality of pump voltages,” as required by claim 1. Petitioner’s reliance on the modifications to *Doluca* is again misplaced.

2. The *Doluca-Buti* combination does not have “a plurality of loads ... each load associated with a specific pump voltage”

Claim limitation [1b] of the ’241 Patent requires “a plurality of loads selectively coupleable to an output of the pumping circuit, each load associated with a specific pump voltage.” Ex. 1001, 8:21-23. For this limitation, the Petition relies on the transistors 42, 48, 54, and 60 in *Buti*’s Fig. 3A bleeder circuit. *See* Petition at 20-21. The Petition, however, fails to show how the transistors are “associated with a specific pump voltage.” In the example shown in Table 1 of *Buti*, Ex. 1005, 7:51-58, transistor operation is overlapping in charge pump voltage. Transistors 42 is turned on between 2.5 V and 5.78 V; transistor 48 is turned on between 2.5 V and 7.6 V; transistor 54 is turned on between 2.5 V and 9.5 V; and transistor 60 is turned on between 2.5 V and 11.43 V. None of these particular transistor loads is “associated with a specific pump voltage.” *See* Ex. 2013, ¶¶ 61-62. The *Doluca-Buti* fails to teach “a plurality of loads selectively coupleable to an output of the

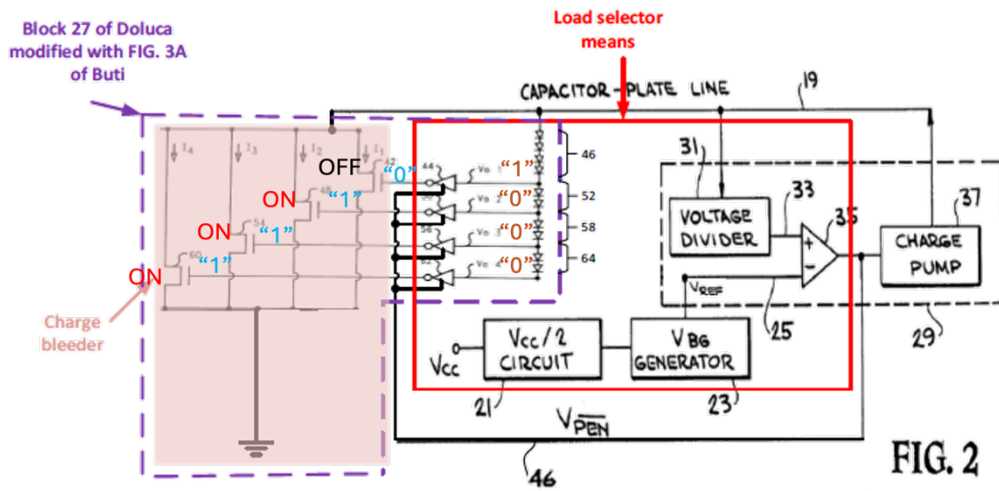
pumping circuit, each load associated with a specific pump voltage,” as required by claim 1 of the ’241 Patent. *See id.*, ¶ 63.

3. The *Doluca-Buti* combination does not have “a plurality of loads ... each load associated with a specific pump voltage”

Claim limitation [1c] of the ’241 Patent requires “a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit.” Ex. 1001, 8:24-26. As discussed, *supra*, in Section II.A, this is a means-plus-function limitation, whose corresponding structure, e.g., switches 320, 324, and 328 as shown in Fig. 3, function such that only one switch (turning on one load) can be active at any time. *See* Ex. 1001, 4:56-62 (“Only one load can be selected at a time. For example, if voltage VA is selected, EN_A causes the first switch 320 to close, connecting the first load to the output terminal of the charge pump circuit 300. *The remaining loads 326 and 330 are disconnected from the output terminal because their respective switches 324 and 328 are open.*”); *see also* Ex. 2013, ¶¶ 66-67. In the proposed *Doluca-Buti* combination, there are multiple loads in operation at the same time because the individual elements of the Petition’s proposed “load selector means” structure (inverters in Fig. 3A of *Buti*), *see* Petition 21-24, are not operated to the exclusion of the other individual elements of the proposed “load selector means” structure. As Dr. Brogioli explains:

The *Doluca-Buti* combination does not meet the corresponding structure of “load selector means” because the inverters are not

exclusively active (converting a low signal, logic “0,” to a high signal, logic “1” to activate corresponding load transistor). As I noted above, when V_{CP} rises above 6.1 V, $\overline{VPEN}$ goes from low to high. The charge pump is deactivated, and the inverters in the Buti circuit are activated. At 6.1 V, using the example voltages of Table 1 of Buti, the top-most inverter input is at a high level (logic “1”), meaning the output of the inverter is at a low level (logic “0”) and transistor 42 is turned off. Conversely, the other three inverters are at a low level (logic “0”), meaning the output of these inverter is at a high level (logic “1”) and transistors 48, 54, and 60 are turned on. I have annotated this in Dr. Dickens’ drawing below. I note that transistors 48, 54 and 60 will bleed V_{CP} until it falls below 6.1 V, at which point $\overline{VPEN}$ will transition to low, enabling the charge pump and disabling Buti’s circuit.



Ex. 1003, ¶ 87 (annotated to show logic values and transistor operation when Doluca charge pump rises above 6.1 V and $\overline{VPEN}$ enables Buti circuit).

Ex. 2013, ¶ 68; *see also id.*, ¶ 69.

Petitioner and its expert offer a variation to the *Buti* Fig. 3A circuit where the transistors 42, 48, 54, and 60 would be turned on, one at a time, with increasing V_{CP} , instead of being turned off one at a time with increasing V_{CP} . *See* Petition at 24-25;

Ex. 1003, ¶¶ 88-91. This would involve either (i) replacing the inverters with buffers enabled by $\overline{VPEN}$; (ii) replacing NMOS transistors 42, 48, 54, 60 with PMOS transistors; or (iii) replacing inverters/buffers with comparators. *See id.* This, however, does not change the fundamental operation of the *Doluca-Buti* combination. *See* Ex. 2013, ¶ 70 (“In the Table 1 example voltages of Buti, when $\overline{VPEN}$ goes high, i.e., $V_{CP} > 6.1$ V, only transistor 42 would be turned on. In this instance, the *Doluca-Buti* combination would work no differently than *Doluca* alone – when V_{CP} goes above 6.1 V and $\overline{VPEN}$ goes high, V_{CP} charge will be bled through a single transistor.”).

The combination of *Doluca* with *Buti*’s Fig. 3A circuit, regardless of any proposed modifications, does not meet the corresponding structure of the “load selector means” limitation of claim 1, which requires coupling of each load to the output of the pumping circuit to be to the exclusion of the other loads. In the Petition’s proposed *Doluca-Buti* combination, each inverter/buffer/comparator is not operated exclusively to the other inverter/buffer/comparator. *See* Ex. 1001, 4:56-62, 5:1-6, 5:12-17, 5:22-32, 5:33-43. Multiple loads can be coupled to the output of *Doluca*’s pump circuit at a time. *See* Ex. 2013, ¶ 71. The proposed combination fails to meet the “load selector means” limitation.

For the foregoing reasons, the proposed *Doluca-Buti* combination fails to satisfy the limitations of claim 1 of the ’241 Patent and claim 1, and its dependents,

are not unpatentable under Ground 1A of the Petition.

B. Claim 24 (Ground 1A)

Claim limitation [24a] of the '241 Patent requires “selecting a output pump voltage (V_{pump}).” Ex. 1001, 12:36. As with claim limitation [1a], the Petition relies on *Doluca* to satisfy this limitation. See Petition at 28 (“A POSITA would have understood that selecting a particular value of K corresponds to selecting a particular output pump voltage (V_{CP}).” (citing Ex. 1003, ¶ 94)). As described above in Section IV.A.1, *Doluca*’s circuitry generates only a single output voltage. Consequently, for the same reasons as set forth with respect to claim limitation [1a], *Doluca* does not teach circuitry that provides for “selecting a output pump voltage (V_{pump}).” See Ex. 2013, ¶ 51. Petitioner’s reliance on *Doluca* for claim limitation [24a] fails.

Claim limitation [24b] of the '241 Patent requires “turning on a load associated with the selected V_{pump} .” Ex. 1001, 12:37. As with claim limitation [1b] and claim limitation [1c], the Petition relies on the *Doluca-Buti* combination to satisfy this limitation. See Petition at 28 (“With the understanding that ‘turning on a load’ means coupling a load to the pump output, the *Doluca-Buti* combination teaches this limitation.” (citing Ex. 1003, ¶ 94)). As described above in Sections IV.A.2 and IV.A.3, the *Doluca-Buti* combination does not “turn on a load” associated with a selected pump voltage. Consequently, for the same reasons as set

forth with respect to claim limitation [1b] and claim limitation [1c], the *Doluca-Buti* combination does not teach circuitry that provides for “turning on a load associated with the selected V_{pump} .” See Ex. 2013, ¶¶ 65, 73. Petitioner’s reliance on the *Doluca-Buti* combination for claim limitation [24b] fails.

For the foregoing reasons, the proposed *Doluca-Buti* combination fails to satisfy the limitations of claim 24 of the ’241 Patent and claim 24, and its dependents, are not unpatentable under Ground 1A of the Petition.

C. Claim 13 (Ground 1B)

Claim limitation [13b] of the ’241 Patent requires “a pumping circuit ... to receive a supply voltage and generate one or more pump voltages.” Ex. 1001, 10:26-28. Petitioner asserts that the *Doluca-Buti* combination discloses this limitation and references the discussion with respect to claim limitation [1a]. See Petition at 46. As described above in Section IV.A.1, *Doluca*’s circuitry generates only a single output voltage. Consequently, for the same reasons as set forth with respect to claim limitation [1a], *Doluca* does not teach circuitry that provides for “generat[ing] one or more pump voltages.” See Ex. 2013, ¶ 50. Petitioner’s reliance on *Doluca* for claim limitation [13b] fails.

Claim limitation [13c] of the ’241 Patent requires “a plurality of loads, each load associated with a specific pump voltage and selectively coupleable to an output of the pump circuit (output pump).” Ex. 1001, 10:29-31. As with claim limitation

[1b], the Petition relies on the *Doluca-Buti* combination to satisfy this limitation. *See* Petition at 46 (citing Ex. 1003, ¶¶ 130-131). As described above in Section IV.A.2, the *Doluca-Buti* combination does not disclose that “each load” is “associated with a specific pump voltage.” *See* Ex. 2013, ¶ 62. Consequently, for the same reasons as set forth with respect to claim limitation [1b], the *Doluca-Buti* combination does not teach “a plurality of loads, each load associated with a specific pump voltage and selectively coupleable to an output of the pump circuit (output pump).” *See* Ex. 2013, ¶ 64. Petitioner’s reliance on the *Doluca-Buti* combination for claim limitation [13c] fails.

Claim limitation [13d] of the ’241 Patent requires “a load selector means coupled to the output pump for selecting a load that satisfies a specific pump voltage.” Ex. 1001, 10:32-33. As with claim limitation [1c], the Petition relies on the *Doluca-Buti* combination to satisfy this limitation. *See* Petition at 46 (citing Ex. 1003, ¶¶ 130-131). As described above in Section IV.A.3, the *Doluca-Buti* combination does not disclose the corresponding structure for the “load selector means.” *See* Ex. 2013, ¶ 71. Consequently, for the same reasons as set forth with respect to claim limitation [1c], the *Doluca-Buti* combination does not teach “a load selector means coupled to the output pump for selecting a load that satisfies a specific pump voltage.” *See* Ex. 2013, ¶ 72. Petitioner’s reliance on the *Doluca-Buti* combination for claim limitation [13d] fails.

For the foregoing reasons, the proposed *Doluca-Buti* combination fails to satisfy the limitations of claim 13 of the '241 Patent and claim 13, and its dependents, are not unpatentable under Ground 1B of the Petition.

VI. GROUNDS 2A, 2B, 2C, 3A AND 3B FAIL BECAUSE A POSITA WOULD NOT BE MOTIVATED TO COMBINE *LE* WITH *UJIE*

Grounds 2A, 2B, 2C, 3A and 3B of the Petition propose a combination of *Le* with *Ujii* to allege invalidity of the independent claims. In particular, with respect to claim 1 of the '241 Patent, the proposed combination addresses *Le*'s failure to teach limitation [1b] of "a plurality of loads selectively coupleable to an output of the pumping circuit, each load associated with a specific pump voltage," Ex. 1001, 8:21-23," and limitation [1c] of "a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit," *id.*, 8:24-26. *See* Petition at 53-54; *see also* Petition at 67 (Claim 24), 74-75 (Claim 13). As discussed below, the Petition fails to show that a POSITA would have found it obvious to use *Ujii*'s clamp diodes with *Le*'s charge pump.

Petitioner asserts that "Le describes that the charge pump output voltage can be regulated using a shunt regulator (e.g., shunt regulator 270), but does not provide further structural or functional description of the shunt regulator" and a "POSITA who, upon reviewing Le's charge pump circuit, wanted to know more about how a shunt regulator can be used to regulate the output voltage, would have looked at

other sources of information about shunt regulators.” Petition at 50-51. The Petition then asserts that a “POSITA would have understood that Ujiie’s shunt circuit can be used as a shunt regulator in Le’s charge pump circuit to regulate the pump output voltage, as a matter of design choice,” and concludes that a “POSITA would have had a reasonable expectation of success for this modification, as these techniques were known and the operation of the resulting circuit would have been predictable.” *Id.*, at 51; *see also* Ex. 2013, ¶ 83. Petitioner’s conclusion is unfounded because the motivation to combine *Le* with *Ujiie* is negated by *Le*’s teaching away from a charge pump circuit that continually uses a shunt regulator, as the proposed combination will. Because Grounds 2A, 2B, 2C, 3A, and 3B advocate for combining the charge pump taught by *Le* with the clamp diodes taught by *Ujiie* that will continually consume power when a clamp diode is connected to the output of *Le*’s charge pump, a POSITA would not be motivated to combine the references.

As noted above, in Section III.C, *Le* describes a first prior art conventional charge pump. Ex. 1008, 2:52-3:3; *see also* Ex. 2013, ¶ 75. *Le* also describes a second conventional charge pump that can accommodate low power supply voltage levels by employing “large capacitor values.” Ex. 1008, 3:7-8; *see also* Ex. 2013, ¶ 76. The second conventional charge pump also includes “a shunt regulator 270 attached at the conventional point of the charge pump output 280, to reduce the output when the supply or the output voltage is higher than a target value.” Ex. 1008,

3:9-12; *see also* Ex. 2013, ¶ 76. “The shunt regulator 280 regulates the charge pump output by partially shorting to ground that portion of the charge pump output which is greater than a desired voltage level. In this conventional method, large capacitor values may be used to compensate for the lowest power supply voltage.” Ex. 1008, 3:32-36; *see also* Ex. 2013, ¶ 77.

Le further discloses that the use of the shunt regulator is problematic because of (i) a high degree of ripple in the pump output voltage, *see* Ex. 1008, 3:41-62, Ex. 2013, ¶¶ 77-78; (ii) noise spikes and valleys, *see* Ex. 1008, 3:63-4:1, Ex. 2013, ¶ 78; and (iii) increase power consumption and reduced system efficiency, *see* Ex. 1008, 3:66-4:3, 4:8-15, Ex. 2013, ¶ 78. *Le* consequently indicates that “there is a need for a low power, low noise means of compensation for the variations in the V_{CC} supply applied to the charge pump circuit, while maintaining a simple regulator design.” Ex. 1008, 4:15-18; *see also* Ex. 2013, ¶ 79. *Le*’s solution is to “vary the capacitance of the bootstrap capacitor values within the stages ... as a function of the input supply voltage.” Ex. 1008, 4:31-35; *see also id.*, 7:4-25; *see also* Ex. 2013, ¶ 79.

The result is that “*a shunt regulator circuit which may operate in conjunction with such a charge pump circuit will consume less power and regulate the charge pump output with less ripple than with conventional charge pump circuits.*” Ex. 1008, 6:21-25 (emphasis added); *see also* Ex. 2013, ¶ 80. Contrasting with “prior art charge pump circuits,” where “at high V_{CC} input voltages, the charge

pump output voltage would greatly exceed the desired target output voltage, which required the shunt regulator to shunt the excess wasted charge to ground, Le's proposed charge pump "reduces an amount of such shunting by the regulator, thereby reducing power." Ex. 1008, 10:61-11:3; *see also* Ex. 2013, ¶ 80.

Le's design goal is to minimize the use of the shunting regulator to minimize power consumption within the memory device. Adding Ujiie's clamp diodes would only maximize the use of a shunting regulator as one or more clamp diodes would be in a constant state where current is flowing through the diode and thus maximize the consumption of power. *See* Ex. 2013, ¶ 84. This is contrary to Le's design goal and a POSITA would not be motivated to make the combination. As Dr. Brogioli explains:

Le's charge pump generates only a single output voltage, at a value close to, but below, the voltage where the shunt regulator would be active. In combination with Ujiie's clamp diodes, Le's charge pump circuit would have to generate the highest output voltage required by the proposed combined circuit. For example, if there are three output voltages, 5 V, 10 V and 20 V, that can be selected with Ujiie's clamp diodes, Le's charge pump would have to be designed to generate 20 V. Le's inventive, i.e., non-prior art, charge pump would therefore generate 20 V with minimal ripple, so a clamping diode with a breakdown voltage at, e.g., 20.1 V (100 millivolts above 20 V), could be used. Based on the disclosure of Le, a POSITA would expect that the 20.1 V clamping diode would be used minimally when the pump is generating 20 V using Le's proposed invention to minimize ripple.

However, when an output voltage less than 20 V is required, for example 10 V or 5 V as I noted above, the respective clamp diodes associated with each of those output voltages in the proposed Le-Ujiie

charge pump circuit would be used maximally, i.e., constantly, while those outputs are generated. While in use, those clamp diodes would be required to sink significant amounts of current to reduce Le's charge pump's 20 V output to 10 V or 5 V. This runs counter to Le's goal of reducing power consumption by reducing the use of a shunt regulator through fine capacitance control within the charge pump. The proposed Le-Ujiie charge pump circuit would radically increase power consumption when 10 V or 5 V outputs are required.

A POSITA would recognize that applying Ujiie's multiple clamp diodes to Le's inventive charge pump dissipates significantly more power when clamp diodes with breakdown voltages less than Le's charge pump's output voltage are coupled to the pump output. Watt's law (where power is equal to current multiplied by the voltage drop) tells us that the diodes, by reducing the output voltage, necessarily dissipate power in relationship to how much voltage is reduced. A POSITA would thus recognize that the usefulness of Ujiie's clamp diodes for voltage reduction is directly related to how much power they consume. The voltage reduction from 20 V to 10 V or 5 V is very significant and the Le-Ujiie charge pump circuit would be expected to sink approximately half the power generated to reduce the output voltage from to 10 V and approximately three-quarters the power generated to reduce the output voltage from to 5 V. This is directly contrary to Le's goal of providing "a low power, low noise means of compensation for the variations in the VCC supply applied to the charge pump circuit, while maintaining a simple regulator design." Ex. 1008, 4:15-18. Based on this, a POSITA would not be motivated to combine Ujiie's clamp diodes with Le's charge pump circuit.

Dr. Dickens opines that the power consumption of the Le-Ujiie combination could be curtailed by including the capability to turn off the charge pump when it reaches the breakdown voltage of the clamp diode (V_{pp1} , V_{pp2}), for example by including the control circuit from Kuriyama, U.S. Patent No. 6,373,325. *See* Ex. 1003, ¶ 167. I disagree that a POSITA would be motivated to make this combination. It is not a design choice as Dr. Dickens suggests. While it may reduce the power consumption across Ujiie's clamp diodes, it reintroduces other problems Le sought to resolve, namely that of excessive ripple and noise spikes and valleys as both the charge pump and shunt regulator

(Ujiie’s clamp diode) turn on and off. As Le noted, “[b]ecause of the internal regulation feedback and response time delays within the shunt regulator, the shunting transistors will not be able to react immediately to the over-voltage level, thereby causing the charge pump voltage to continue to rise beyond the target regulation voltage before the shunting transistors can respond with adequate conduction. Given the typical feedback-response delay of the shunt regulator 270, the conventional charge pump 200 will produce an increased ripple magnitude (e.g., about 400 mV P-P ripple at about 9 volt output) at the output 280 when the input supply voltage 210 is high.” Ex. 1008, 3:52-62. In the circumstance of the charge pump turning on and off, the feed-back response delay, now between both shunt regulator operation and charge pump operation will only lead to greater ripple in the output voltage and a higher degree of noise spikes and valleys associated with both the shunt regulator and charge pump turning on and off. Based on this, a POSITA would not be motivated to combine Ujiie’s clamp diodes with Le’s charge pump circuit and Kuriyama’s charge pump control.

Ex. 2013, ¶¶ 85-88.

Petitioner asserts that a POSITA, looking at the teachings of *Le*, would be motivated to undo the essential changes, minimizing the use of a shunt regulator, that *Le* advocated over the prior art. A POSITA would not be so motivated. *See Trivascular, Inc. v. Samuels*, 812 F.3d 1056, 1068 (Fed. Cir. 2016) (finding no motivation to modify the prior art where doing so “would destroy the basic objective” of the prior art); *In re Gordon*, 733 F.2d 900, 902 (Fed. Cir. 1984) (finding no reason to modify a prior art device where the modification would render the device “inoperable for its intended purpose”); *Google LLC f/k/a Google Inc. v. Singular Computing LLC*, IPR2021-00155, Paper 62, at 74 (PTAB May 23, 2022)

(“Petitioner’s asserted combination ... would ... defeat[] MacMillan’s stated objective of achieving a highly parallel SIMD computer architecture at lower system cost”) (internal quotations omitted).

The Petition’s generic allegation that the proposed combination of *Ujiie*’s clamp diodes in *Le*’s charge pump circuit would be made with a “reasonable expectation of success ... as these techniques were known and the operation of the resulting circuit would have been predictable” is inadequate to show that a POSITA would have a motivation to combine *Le* and *Ujiie*. At most, the generic allegation goes to the issue of whether a POSITA ***could have*** made the proposed combination, not to whether a POSITA ***would have been motivated*** to make that combination as required. *See Personal Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 993 (Fed. Cir. 2017) (it is not enough to show that “a skilled artisan, once presented with the two references, would have understood that they ***could*** be combined”); *Apple, Inc. v. Realtime Data LLC*, IPR2016-01737, 2018 WL 1326656, at *25 (PTAB Mar. 13, 2018) (granting motion to amend because petitioner did not adequately “articulate a *reason why* a person of ordinary skill in the art would combine the prior art references”) (citing and quoting *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (“obviousness concerns whether a skilled artisan not only ***could have made*** but ***would have been motivated to make*** the combination or modifications of prior art to arrive at the claimed invention”)) (emphases in original).

Le discourages the continual use of a shunting regulator because of the power consumption problems when used with limited energy sources. Ex. 1008, 4:11-15; *see also* Ex. 2013, ¶ 78. “Under the proper legal standard, a reference will teach away when it suggests that the developments flowing from its disclosures are unlikely to produce the objective of the applicant’s invention.” *Syntex (U.S.A.) LLC v. Apotex, Inc.*, 407 F.3d 1371, 1380 (Fed. Cir. 2005) (citing *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994)). Teaching away requires a reference to “criticize, discredit, or otherwise discourage investigation into the claimed invention.” *Meiresonne v. Google, Inc.*, 849 F.3d 1379, 1382 (Fed. Cir. 2017). A reference teaches away “when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1327 (Fed. Cir. 2009).

By discouraging the continual use of a shunting regulator for at least power consumption reasons, and disclosing a divergent embodiment that minimizes the use of a shunting regulator, *Le* teaches away from the continual use of a shunting regulator. As a result of such teaching away, the possibility of rendering a claim obvious based on the combination of *Le* with another reference that teaches continual use of a shunting regulator is negated. *See In re Mouttet*, 686 F.3d 1322, 1333 (Fed. Cir. 2012). Consequently, Petitioner’s proposed combination of *Le* with *Ujiie*

cannot render the claims of the '241 Patent obvious.

VII. CONCLUSION

As set forth above with respect to Grounds 1A and 1B, *Doluca* in combination with *Buti* does not teach multiple limitations of independent claims 1, 13, and 24 of the '241 Patent. As a result, Petitioner's Grounds 1A and 1B challenge to the independent claim, as well as its challenges to dependent claims 2-3, 4-5, 11-12, 14-15, 21-23 and 25, fail. With respect to the proposed combination of *Le* with *Ujiie* in Grounds 2A, 2B, 2C, 3A and 3B, the Petition advocates for *Le* to be modified to continually use a shunting regulator, in the form of *Ujiie*'s clamp diodes, to generate an output voltage of anything less than the design voltage for *Le*'s charge pump. This proposed modification is made in direct contravention of *Le*'s stated objective of minimizing the use of shunt regulators to avoid the power consumption issues present with such use. Ex. 1008, 6;21-25, 10:61-11:3. A POSITA would therefore understand that the proposed combination would be detrimental to *Le*. A POSITA would thus not have been motivated to make the proposed combination. For this reason, the Petition cannot show any challenged claim to be unpatentable under Grounds 2A, 2B, 2C, 3A and 3B.

For all of the reasons above, Patent Owner respectfully requests that all challenged claims be found not unpatentable.

Respectfully submitted,

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Date: March 11, 2024

CERTIFICATE OF WORD COUNT (37 C.F.R. § 42.24(d))

The undersigned hereby certifies that the word count in this Patent Owner's Response is 11,156 words, as counted by the word-processing program Microsoft Word that was used to generate this Patent Owner's Response, where such word count excludes the table of contents, table of authorities, mandatory notices, certificate of service, appendix of exhibits, claim listing, and this certificate of word count. This Patent Owner's Response is in compliance with the 14,000-word limit set forth in 37 C.F.R. § 42.24(b)(1).

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CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e))

The undersigned hereby certifies that the above document was served on March 11, 2024, by filing this document, along with the accompanying exhibits, through the Patent Trial and Appeal Case Tracking System as well as delivering a copy via electronic mail upon the following attorneys of record for the Petitioner:

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