

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

SONRAI MEMORY LIMITED,
Patent Owner

Case IPR2023-00909
Patent 6,724,241

PETITIONER'S REPLY TO PATENT OWNER RESPONSE

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	NEITHER THE '241 Patent specification NOR THE ClaimS require the PUMPING CIRCUIT be able to generate a plurality of voltages for selection during runtime	1
	A. The plain meaning of the claim language “generate a selected one of a plurality of pump voltages” does not require that the pumping circuit output is selected at runtime	2
	B. Claim limitations directed towards associating different loads with specific pump voltages do not require that the pumping circuit voltage output is selected at runtime	3
	C. The '241 Patent specification teaches that the pumping circuit output voltage is not selected at runtime.....	8
III.	THE doluca-buti combination reads on THE ClaimS even under patent owner’s interpretation that the charge pump is able to generate a plurality of voltages for selection during runtime	10
	A. Doluca’s charge pump output voltage can be adjusted in a manner similar to the '241 Patent’s charge pump output voltage	10
	B. The Doluca-Buti combination reads on the '241 Patent’s claims under Patent Owner’s interpretation	14
	C. A POSITA would have been motivated to combine Buti with Doluca..	14
	D. The Doluca-Buti combination reads on “a plurality of loads ... each load associated with a specific pump voltage”	17
	E. The Doluca-Buti combination renders obvious claims 13 and 24	20
IV.	A POSITA WOULD Have been motivated to combine le with ujii	20
V.	CONCLUSION.....	26

PETITIONER’S LIST OF EXHIBITS

- | | |
|---------|---|
| EX-1001 | U.S. Patent No. 6,724,241 to Bedarida et al. (“’241 Patent”) |
| EX-1002 | Excerpts from the Prosecution History of the ’241 Patent |
| EX-1003 | Declaration of Dr. James Dickens |
| EX-1004 | Curriculum vitae of Dr. James Dickens |
| EX-1005 | U.S. Patent No. 5,872,733 to Buti et al. (“Buti”) |
| EX-1006 | U.S. Patent No. 4,769,784 to Doluca et al. (“Doluca”) |
| EX-1007 | U.S. Patent No. 6,404,274 to Hosono et al. (“Hosono”) |
| EX-1008 | U.S. Patent No. 6,424,570 to Le et al. (“Le”) |
| EX-1009 | Japanese Patent Application No. S61-024094 to Ujiie et al. (“Ujiie”) |
| EX-1010 | U.S. Patent No. 6,091,613 to Yang et al. (“Yang”) |
| EX-1011 | U.S. Patent No. 6,373,325 to Kuriyama et al. (“Kuriyama”) |
| EX-1012 | U.S. Patent No. 4,506,350 to Asano et al. (“Asano”) |
| EX-1013 | District Court’s Claim Construction Order in <i>Sonrai Memory Limited v. Kioxia et al.</i> , Dkt. 55, W.D. Tex. 6:21-cv-00400-ADA |
| EX-1014 | Webster’s Unabridged Dictionary, 2d ed. 2001 (excerpts) |
| EX-1015 | McGraw-Hill Electronics Dictionary, 6th ed. 1997 (excerpts) |
| EX-1016 | U.S. District Courts–Combined Civil and Criminal Federal Court Management Statistics (September 30, 2022), available at:
https://www.uscourts.gov/sites/default/files/data_tables/cms_na_distprofile0930.2022.pdf |
| EX-1017 | Geiger <i>et al.</i> , VLSI Design Techniques for Analog And Digital Circuits (1990), ISBN 0070232539 (excerpts) |

- EX-1018 Plaintiff's Sur-Reply Claim Construction Brief in *Sonrai Memory Limited v. Apple Inc.*, Dkt. 48, W.D. Tex. 6:22-cv-00787-ADA
- EX-1019 Texas Instruments, *SNx4LS24x, SNx4S24x Octal Buffers and Line Drivers With 3-State Outputs* (Apr. 1985, rev. Oct. 2016)
- EX-1020 District Court's Claim Construction Order in *Sonrai Memory Limited v. Apple Inc.*, Dkt. 53, W.D. Tex. 6:22-cv-00787-ADA
- EX-1021 Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, Katherin K. Vidal (USPTO June 21, 2022) ("Interim Guidance")
- EX-1022 Stipulation
- EX-1023 Supplemental Declaration of Dr. James Dickens
- EX-1024 Deposition Transcript of Dr. Michael Brogioli

I. INTRODUCTION

Responsive to issues raised in the Patent Owner's Response (POR) and the Institution Decision, Petitioner submits the following Reply, with explanation and support as set forth in the accompanying Supplemental Declaration of Dr. James Dickens. EX-1023, ¶¶1-58. As detailed below, Patent Owner's first argument against Grounds 1A-1B (POR, §V.A.1) attempts to force a reading of claims 1, 13 and 24 that goes against the plain meaning of the claims, and also finds no support in the '241 Patent description. Patent Owner's second argument against Grounds 1A-1B (POR, §§V.A.2-V.A.3) is contradicted by the disclosure of the '241 Patent itself. Patent Owner's third and final argument—against Grounds 2A-2C and 3A 3B—are premised on a misapplication of motivation to combine case law. The Board should reject Patent Owner's arguments and find the Challenged Claims unpatentable.

II. NEITHER THE '241 PATENT SPECIFICATION NOR THE CLAIMS REQUIRE THE PUMPING CIRCUIT BE ABLE TO GENERATE A PLURALITY OF VOLTAGES FOR SELECTION DURING RUNTIME

Patent Owner asserts that the output voltage of the pumping circuit is “dynamically selectable” from multiple output voltages by arguing that: (a) a reading of the claim language “selected one of a plurality of pump voltages” requires that the output voltage of the pumping circuit be dynamically selectable;

and (b) the claimed limitations “each load associated with a specific pump voltage” and “selectively coupling a load associated with a specific pump voltage” reinforces that the pumping circuit must be able to generate two or more pump voltages. POR, 7-10. Neither argument holds up upon a reading of the ’241 Patent itself, and an understanding of a POSITA.

A. The plain meaning of the claim language “generate a selected one of a plurality of pump voltages” does not require that the pumping circuit output is selected at runtime

The claim term at issue recites that a pumping circuit is “operable to receive a supply voltage and generate a selected one of a plurality of pump voltages.” EX-1001, 8:18-20. As the Board correctly observed in the Institution Decision (DI), a plain meaning of this claim term merely requires that the pumping circuit generate a particular output voltage, which can be chosen in advance, e.g., during design. DI, 13-14. The plain meaning of this claim term *does not* require that the output voltage be selected from a group of possible output voltages dynamically during runtime. *Id.*; EX-1023, ¶¶10-14.

Patent Owner would have us believe otherwise based on an incorrect and convoluted reading of the claim language: the claim requires that “the loads and *consequently* the output voltage of the pumping circuit be dynamically selectable.”

POR, 7.¹ That is, *selection of the output voltage of the pump circuit is a function of the load selection*. EX-1023, ¶¶15-16. A POSITA would have understood that such a reading of the claim language contradicts the purported invention of the '241 Patent: a load is selected *based on* the desired pump output to minimize voltage ripple. *See, e.g.*, EX-1001, 4:5-8; EX-1023, ¶¶15-17.

B. Claim limitations directed towards associating different loads with specific pump voltages do not require that the pumping circuit voltage output is selected at runtime

Patent Owner asserts that the limitation “each load associated with a specific pump voltage” “reinforces that the pumping circuit must be able to generate *two* or more pump voltages.” POR, 8. But this assertion is plainly contradicted by the express language of the '241 Patent, which repeatedly describes that the purported invention of a pumping circuit is operable to generate *one* or more pump voltages, while having a plurality of loads connectable to the charge pump output:

The object [of the invention] is met by a charge pump circuit with variable load. The charge pump circuit comprises one or more stages operable to receive a supply voltage and **generate one or more pump voltages**. A plurality of loads are connectable to the charge pump output, each load associated with a specific target pump voltage. A load selector means couples a selected load to the output according to the

¹ Emphasis added throughout unless otherwise noted.

target pump voltage.

EX-1001, 3:7-12; *see also id.*, FIG. 3 and 8:64-4:8 (describing “charge pump circuit 300” that is operable to generate “one or more pump voltages” while including “several different loads 322, 326, and 330,” an appropriate one of which is selected depending on the desired pump output voltage); and Abstract (describing generating “one or more pump voltages”).

Patent Owner attempts to buttress this argument by asserting that the claim limitation “load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit” reinforces its position that “the output voltage of the pumping circuit has to be dynamically selectable.” POR, 8-9 (quoting EX-1001, 8:24-26). Beyond a restatement of its erroneous argument that each load is tied to a particular pump voltage, Patent Owner goes on to assert that the “specification makes clear that the *selection of a particular load*, associated with a specific voltage, *is to the exclusion of other loads* associated with other specific voltages.” *Id.* (citing EX-1001, 4:56-62).

The '241 Patent does not support such an understanding of the cited portion, which discloses:

When an instruction for either VA, VB, or VC is received by a controller (not shown), the controller (not shown) generates the enable control signal EN_A, EN_B or EN_C that selects an appropriate load for this voltage that gives the minimum voltage ripple. **Only one load**

can be selected at a time. For example, if voltage VA is selected, EN_A causes the first switch 320 to close, connecting the first load to the output terminal of the charge pump circuit 300. The remaining loads 326 and 330 are disconnected from the output terminal because their respective switches 324 and 328 are open.

EX-1001, 4:52-62. A POSITA would have understood that this description in the '241 Patent merely discloses that one load is added *at a time* by closing the corresponding switch. EX-1023, ¶¶18-19. However, this does not preclude connecting other loads to the pumping circuit output at other times by closing their respective switches. *Id.* That is, this section of the '241 Patent at most teaches adding loads one at a time to the pumping circuit output, but does not require having only one load connected to the pump output at all times. *Id.*; *see also* EX-1024 at 83:16-86:15, 165:18-21, 166:15-167:1 (Patent Owner's expert, Dr. Brogioli, agreeing that Load S can be connected to the pump output along with one of Loads A, B, C of Fig. 7 embodiment).

Indeed, the '241 Patent specification makes clear that Patent Owner's assertion is wrong—instead, making clear that more than one load can be associated with a specific voltage. Describing a method of charge pump operation, the '241 Patent discloses:

Referring to FIG. 10, the flow chart shows **a method 1000 usable especially with the circuits of FIGS. 3 and 7 for achieving minimum**

voltage ripple in the charge pump circuit 600 by **dynamically selecting the best load** that yield the desired result, **including the decision whether to set load S in addition to one of the loads A, B or C**. The method begins by choosing a desired output pump voltage (step 1004), selecting a load associated with the selected output pump voltage (step 1006), comparing (step 1008) the target output voltage (V_{cfra}) to a reference voltage (V_{ref}), comparing (step 1010) the maximum ripple target output voltage (V_{cfrb}) to the reference voltage (V_{ref}). The resistor network going V_{cfrb} is made to give $V_{cfrb} < V_{cfra}$ for a given output voltage V_{pump} . Whenever the target output voltage V_{cfra} is less than the V_{ref} , else continue the pumping process. **Whenever V_{cfrb} is greater than V_{ref} , adding a load**; otherwise, continue to next step.

...

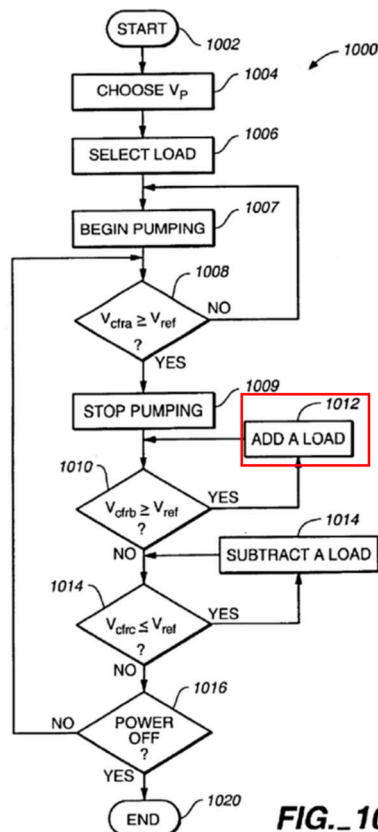
At the step 1006, the switch enables a load corresponding to the selected pump voltage by switching on the load that provides the best voltage ripple **by means of either EN_A, EN_B, or EN_C function as discussed above**. The pumping phase (step 1007) is enabled.

...

At step 1012, the circuit 600 adds a load so that voltage ripple can be reduced. This step continues until the voltage ripple is reduced and then the circuit 600 goes to the next step.

EX-1001, 7:6-8:14, and FIG. 10 (reproduced below). The '241 Patent emphasizes that this method is usable “**especially** with the circuits of FIGS. 3 and 7”—the same circuits that Patent Owner has cited to support its argument that

selection of a particular load is to the exclusion of other loads. EX-1001, 7:6-16; POR, 9. A POSITA would have found that the '241 Patent specification makes clear that more than one load can be selected and associated with a specific output voltage; Patent Owner's assertion to the contrary is plainly wrong. EX-1023, ¶¶20-23. The claim limitations that recite "each load associated with a specific pump voltage," and "selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit" do not teach that the voltage output by the pumping circuit is selected at runtime. *Id.*



EX-1001, FIG. 10 (annotated)

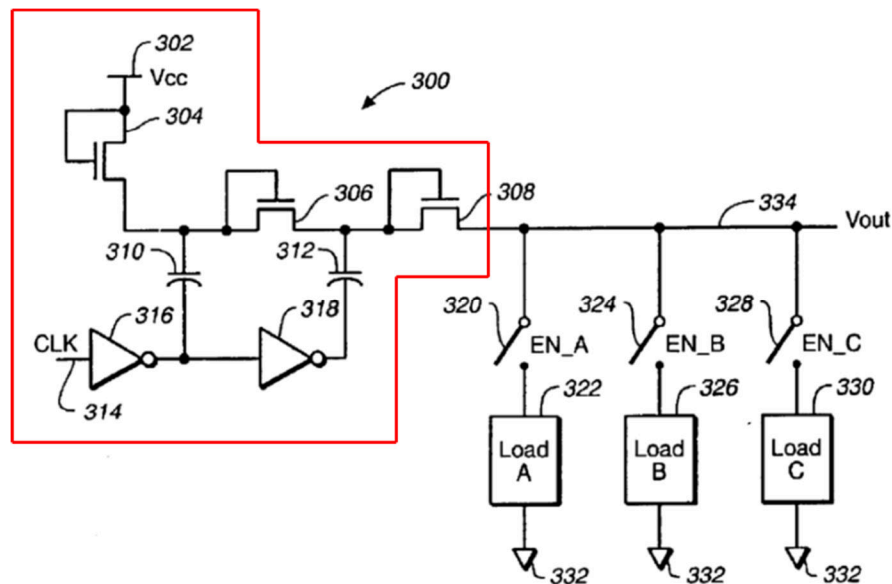
C. The '241 Patent specification teaches that the pumping circuit output voltage is not selected at runtime

A POSITA does not need to scrutinize the claim language to understand that the pumping circuit output voltage is determined in advance, and not selected during runtime—the '241 Patent itself teaches this by what its specification does or does not describe. The '241 Patent refers to dynamic selection multiple times, but *always* to describe selection of the load: “a new approach to **select dynamically the best load** for a pump as a function of the target output voltage”; and “a method 1000 usable especially with the circuits of FIGS. 3 and 7 for achieving minimum voltage ripple in the charge pump circuit 600 by **dynamically selecting the best load** that yield the desired result.” EX-1001, 3:15-18, 7:10-16; *also id.*, Title (stating “dynamic **load**”). There is no mention whatsoever of the output voltage V_p of the pumping circuit being dynamically selectable. EX-1023, ¶¶24-28.

Indeed, while the '241 Patent illustrates and describes multiple schematics for a variable charge pump circuit that enables dynamic selection of load using switch control, none of the circuits indicate that the pumping circuit itself—the circuit that generates the raw pump voltage V_p —has any dynamically selectable component, which is what Patent Owner asserts the claim requires. *Id.* To meet Patent Owner’s requirement for the claims, the “pump circuit 100” of FIGS. 3, 6

and 7 has to include components that can be adjusted during runtime to select the pump voltage V_p from among a plurality of voltages. *Id.*, ¶¶25, 28. The '241 Patent has no such disclosure or suggestion. The only dynamic control for the pump circuit 100 that is disclosed are “comparator 602” and “comparator 702”—but these are used only to disable the pump circuit, not change V_p from one target voltage to another. EX-1001, 5:44-6:9 and FIGS. 6-7; EX-1023, ¶27.

The '241 Patent provides only one schematic diagram for the internal circuitry of pump circuit 100, as shown in FIG. 3 (and also FIG. 1):²



EX-1001, FIG. 3 (annotated)

As the '241 Patent explains, this is an example of a two-stage charge pump, and

² During his deposition, Dr. Brogioli acknowledged that this is the pumping circuit recited in claim 1(a) of the '241 Patent. EX-1024, 91:8-97:12.

the output voltage is a function of the number of stages, with each stage having a capacitor (e.g., capacitors 310 and 312). EX-1001, 1:15-2:2, 3:64-4:32; EX-1023, ¶¶24-25. Different pump voltage outputs can be achieved by using charge pump circuits with different numbers of stages—a POSITA would have understood that this is feasible before manufacturing and using the charge pump, e.g., at the design phase. EX-1023, ¶25; DI, 14. Notably, the '241 Patent describes no mechanism for dynamically changing the number of stages of the charge pump during runtime, and a POSITA would not have found any suggestion of such being possible. EX-1023, ¶¶24-29.

III. THE DOLUCA-BUTI COMBINATION READS ON THE CLAIMS EVEN UNDER PATENT OWNER'S INTERPRETATION THAT THE CHARGE PUMP IS ABLE TO GENERATE A PLURALITY OF VOLTAGES FOR SELECTION DURING RUNTIME

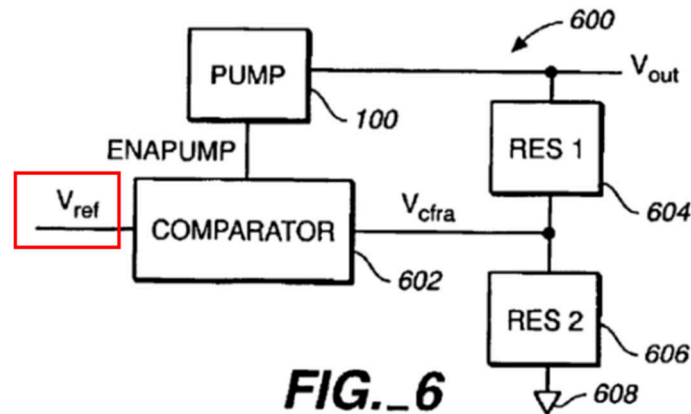
A. Doluca's charge pump output voltage can be adjusted in a manner similar to the '241 Patent's charge pump output voltage

As discussed in §II.C, the '241 Patent's charge pump can be configured to generate different output voltages by designing the charge pump with different pump stages, before deployment and use. §II.C, *supra*; EX-1023, ¶25. The Doluca-Buti combination reads on this understanding of the '241 Patent's charge pump by enabling selection of the value of K in Doluca. Pet., 18-20. Patent Owner agrees with this teaching of Doluca. POR, 26-27. A POSITA would have

understood that the Doluca-Buti combination reads on the claim limitation “generate a selected one of a plurality of pump voltages” as the limitation is interpreted in light of the ’241 Patent specification. EX-1023, ¶¶30-31.

Even otherwise—assuming *arguendo* Patent Owner’s assertion that the pumping circuit can generate a plurality of voltages at runtime³—a POSITA would have understood that such a dynamic configuration can be enabled only by external mechanism, since the circuitry of the charge pump cannot be changed when in use. In view of the ’241 Patent’s disclosure that the charge pump 100 is controlled (e.g., enabled or disabled) by the comparator 602/comparator 702 by comparing the pump output voltage to a reference voltage V_{ref} , a POSITA would have understood that an adjustment to the value of V_{ref} could cause a change in the pumping circuit output voltage. EX-1001, 5:44-6:17, FIG. 6 (reproduced below) and FIG. 7; EX-1023, ¶31.

³ To reiterate, Petitioner does not agree with this reading of the claims, as discussed throughout this Reply.



EX-1001, FIG. 6 (annotated)

As described in the Petition, Doluca's circuit controls the charge pump 37 output voltage V_{CP} in a similar manner: by comparing the pump output voltage to a reference voltage V_{REF} . Pet., 11-12, 20-21 (citing EX-1006, 3:54-5:20 and FIG. 2). A POSITA would have understood that Doluca's charge pump 37 output voltage V_{CP} can be adjusted dynamically, e.g., during runtime operation of the charge pump circuit, by adjusting the value of the reference voltage V_{REF} . EX-1023, ¶¶32-35. Doluca teaches that (i) V_{REF} is a function of $V_{CC}/2$ that is generated by voltage divider circuit 21, which a POSITA would have understood as being adjustable, and (ii) V_{REF} is variable. EX-1006, 3:62-4:9, 8:67-68 and FIG. 2; EX1023, ¶¶32-35. Indeed, Doluca explicitly mentions that its charge pump circuit output is intended to be any of a plurality of output voltages:

establishing and maintaining a voltage on said capacitor-plate node,
comprising in combination;

charge pump means for pumping electrical charge into said

capacitor-plate node, to thereby raise the potential of said node;

...

a source of reference voltage;

feedback control means for comparing the voltage of said capacitor-plate node to said reference voltage and for initiating operation of a selected one of said charge pump means and said charge bleeder means to **maintain said capacitor-plate voltage within a preselected range of voltages**

EX-1006, 7:33-8:14; EX-1023, ¶¶36. Accordingly, to the extent the '241 Patent discloses that the pumping circuit output voltage can be dynamically selected, which Petitioner does not agree with, Doluca teaches such dynamic selection. EX-1023, ¶¶34-36.⁴

⁴ As Dr. Dickens explains and as noted in the Petition, the combination of references in Grounds 2A-2C and 3A-3B similarly reads on this interpretation of the '241 Patent claim language, based at least on the disclosure of program/erase operations in Le, reference voltage comparison in Kuriyama, and V_{PP1} , V_{PP2} in Ujiie. Pet., 53, 59-62; EX 1023, ¶36. Notably, Patent Owner does not allege that Grounds 2A-2C and 3A-3B fail to teach “generate a selected one of a plurality of pump voltages.”

B. The Doluca-Buti combination reads on the '241 Patent's claims under Patent Owner's interpretation

Based on its interpretation of the claims requiring that the pumping circuit output voltage be dynamically selectable, Patent Owner alleges that the modified circuit of the Doluca-Buti combination cannot meet this requirement. POR, 27-29 (citing Petition at 20). As noted above, the '241 Patent specification does not support the interpretation that the pumping circuit output voltage is dynamically selectable. §II, *supra*. And even if Patent Owner's interpretation is considered,⁵ the modified circuit of the Doluca-Buti combination does not change Doluca's use of V_{REF} to control the charge pump output voltage V_{CP} —which renders the claims obvious even under Patent Owner's interpretation. §III.A, *supra*; EX-1023, ¶36.

C. A POSITA would have been motivated to combine Buti with Doluca

Patent Owner contends that a POSITA would not have been motivated to combine Doluca with Buti because Doluca already discloses “current-regulating transistor 79” as charge bleeder circuit, such that a POSITA would not have been motivated to look elsewhere for charge bleeder 45. POR, 27-28. This argument does not hold up.

Doluca discloses current-regulating transistor 79 as part of its bleeder

⁵ n.1, *supra*.

control circuit 27, describing that the “[t]ransistor 79 serves as a non-linear current regulator having a generally parabolic current-voltage characteristic.” EX-1006, 6:53-58, FIG. 5. A POSITA would have understood that while Doluca describes using a non-linear current source derived from transistor 79, it does not provide any information on how to design or implement such a bleeder circuit for a specific voltage-current relationship. EX-1023, ¶¶37-39. To fill the gap, a POSITA would need to look at other technical references: reading Buti, a POSITA would have understood that Buti describes, in greater detail compared to Doluca’s description of transistor 79, a bleeder circuit whose current is dependent upon the output voltage and that utilizes multiple charge bleeder paths to provide improved voltage ramp regulation. *Id.*, 40. Such additional detail and improvement in operation would have motivated a POSITA to consider Buti’s charge bleeder when implementing Doluca’s circuit. *Id.*, ¶¶40-43. *See also Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023) (finding that there is a motivation to combine if a combination is a “*suitable* option” and “[i]t’s not necessary to show that [the] combination is the *best* option”) (citing *Intel Corp. v.*

Qualcomm Inc., 21 F.4th 784, 800 (Fed. Cir. 2021)).⁶

Patent Owner advances a second argument against the motivation to combine Buti with Doluca: Buti only regulates the rate of increase of the output voltage, but does not regulate the charge pump output voltage, as intended in Doluca. POR, 27-28. But the law does not have such a requirement for combining references: courts have consistently held that the motivation to combine does not

⁶ Patent Owner appears to challenge the motivation to combine Doluca and Buti also because the combination allegedly does not read on claim 1. POR, 28-29. Such a requirement of the motivation to combine is inconsistent with the case law. *See, e.g., Alcon Research, LTD. v. Apotex Inc.*, 687 F.3d 1362, 1368 (Fed. Cir. 2012) (“We have repeatedly held that the motivation to modify a prior art reference to arrive at the claimed invention need not be the same motivation that the patentee had.”); and *Outdry Techs. Corp. v. Geox S.p.A.*, 859 F.3d 1364, 1370-71 (Fed. Cir. 2017) (“Any motivation to ... combine references, whether articulated in the references themselves or supported by evidence of the knowledge of a skilled artisan, is sufficient to combine those references to arrive at the . . . claimed process.”).

require that the references maintain their original functions in the combination.

See, e.g., In re Keller, 642 F.2d 413, 425 (C.C.P.A. 1981) (“The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art.”); *PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1366 (Fed. Cir. 2018) (rejecting argument that “relies on the presumption that one of ordinary skill would blindly incorporate [one reference’s] exact methodology into [another reference]”); and *Intel*, 61 F.4th 1381 (holding that a reference describing one solution does not negate a motivation to implement another solution, and that a Petitioner is not required to prove an actual “improvement”). As explained in the Petition and also above, a POSITA would have been motivated to combine Buti with Doluca for various reasons. Pet., 13-17. “*Nothing more is required* to show a motivation to combine under *KSR*.” *Intel*, 61 F.4th 1381 (citing *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 127 S. Ct. 1727, 167 L. Ed. 2d 705 (2007)).

D. The Doluca-Buti combination reads on “a plurality of loads ... each load associated with a specific pump voltage”

Patent Owner argues that the Doluca-Buti combination does not render

obvious “each load associated with a specific pump voltage” allegedly because there are multiple loads in operation at the same time in the combination, where Patent Owner maps each of the FETs 42, 48, 54 and 60 as distinct loads. POR, 29-30.

This argument does not withstand scrutiny. The Petition explains that “FETs 42, 48, 54, and 60 in Buti’s bleeder circuit, and in Doluca’s modified bias circuit, are analogous to loads,” where “different subsets of FETs 42, 48, 54, and 60 [are] ‘loads’ in Buti’s bleeder circuit[] depending on the range of V_{out} .” Pet., 20-22. The Petition goes on to explain how these loads, i.e., different subsets of FETs, are activated depending on the value of V_{out} . *Id.*, 22-25. Notably, the Petition does not map each of FETs 42, 48, 54, and 60 to a different load. A POSITA would have found that the activation of different subsets of FETs depending on different values of V_{out} renders obvious a plurality of loads where each load is associated with a specific pump voltage. EX-1023, ¶¶44-49.

Patent Owner advances a second argument against the Doluca-Buti combination’s mapping to “each load associated with a specific pump voltage”: alleging that multiple loads in Doluca-Buti are in operation at the same time because individual elements of the combination’s “load selector means” structure are not operated to the exclusion of the other individual elements. POR, 30-32. This argument also fails, for several reasons.

First, this argument is premised on Patent Owner's interpretation that the '241 Patent claims require that selection of a particular load is to the exclusion of other loads. POR, 32. As discussed above, such an interpretation of the claims finds no support in the Specification; on the contrary, the Specification discloses embodiments that show multiple loads being added for a target output voltage. §II.B, *supra*; EX-1023, ¶¶50-52.

Second, Patent Owner bases this argument by advancing—for the first time—the interpretation that the limitation “load selector means for selectively coupling a load associated with a specific pump voltage” means that “only one switch can be active at any time” in the '241 Patent embodiments, such that each load is coupled to the output to the exclusion of other loads. POR, 30-32 (citing EX-1001, 4:56-62 and FIG. 3). According to Patent Owner, this requires “individual elements[] (inverters in Fig. 3A of Buti)” in the load selector means structure of the Doluca-Buti combination to be “operated to the exclusion of the other individual elements,” which the combination allegedly fails to meet. POR, 30-31. Such an interpretation of the claim language is not supported by the '241 Patent specification. As discussed in §II.B, the Specification discloses that more than one load can be associated with a target output voltage, e.g., by adding an extra load to reduce voltage ripple. §II.B, *supra*; EX-1023, ¶¶50-52. A POSITA would have found it obvious that, to associate more than one load with the target

output voltage, the corresponding switches have to be in a closed state at the same time. EX-1023, ¶¶50-52. The description in the '241 Patent accordingly contradicts the interpretation advanced by Patent Owner.

E. The Doluca-Buti combination renders obvious claims 13 and 24

Patent Owner relies on the arguments it advanced with respect to claim 1 to allege that the Doluca-Buti combination fails to read on claims 24 and 13, without anything more. POR, 33-36. For reasons outlined above, Patent Owner's arguments do not withstand scrutiny and should be rejected.

IV. A POSITA WOULD HAVE BEEN MOTIVATED TO COMBINE LE WITH UJIE

Patent Owner contends that the Le-Ujie combination does not read on the Challenged Claims because a POSITA would not have been motivated to "use Ujie's clamp diodes with Le's charge pump." POR, 36-37. The crux of Patent Owner's argument, relying on Dr. Brogioli's testimony, is that Le "teache[s] away from a charge pump circuit that continually uses a shunt regulator." *Id.*, 37. These arguments are based on a fundamental misreading of Le and Ujie's teachings and a disregard of the case law.

To make their case, Dr. Brogioli and Patent Owner list a range of problems that Le mentions, and attributes these to a shunt regulator. *Id.*, 38-41 (citing EX-2013, ¶¶77-88). However, upon reading Le, a POSITA would have immediately

understood that Le describes these are problems found in a “**conventional two stage charge pump**,” and *not because of the use of a shunt regulator*, which merely serves “to reduce the output when the supply or the output voltage is higher than a target value.” EX-1008, 3:6-4:15; EX-1023, ¶¶53-55. The extent to which Le critiques a shunt regulator is to note that a typical shunt regulator cannot adequately compensate for the *deficiencies of the conventional two stage charge pump*:

In this conventional method, large capacitor values may be used to compensate for the lowest power supply voltage. However, when the V_{CC} is not at its lowest level, the use of large capacitor values wastes power supply charge which may be simply shorted to ground through the shunt regulator, resulting in an overall loss of pump efficiency.

The output of the charge pump 280 and the shunt regulator 270 experience a **ripple voltage signal from the charge and discharge cycles**, with a period which matches the clock cycle period. ... Given the typical feedback-response delay of the shunt regulator 270, **the conventional charge pump 200 will produce an increased ripple magnitude []at the output 280 when the input supply voltage 210 is high.**

Additionally, noise spikes and valleys are produced on the output 280 as the shunting transistors in the shunt regulator 270 discharge the over-voltage on the charge pump capacitors to ground. Thus, **greater supply levels result in higher charge pump output voltage peaks,**

which result in larger noise spikes and valleys at the regulator output 280, **increased power consumption and reduced overall system efficiency.**

...V_{CC} variations are typically reflected in the output of the charge pump circuit in terms of increased ripple and noise. In addition, at high V_{CC} voltages, the charge pump circuit and shunt regulator circuit together as a system exhibit increased power consumption and reduced system efficiency.

EX-1008, 3:33-4:11.

Le's solution to address these problems does not focus on constraining the types of shunt regulators that can be used; rather, it is to invent "**a novel charge pump circuit** where one or more individual stages [have] a variable bootstrap capacitance value which is varied as a function of the input supply voltage," to "compensat[e] for the variations in the V_{CC} supply[], while maintaining a simple regulator design." EX-1008, 4:15-35. "By compensating for the variations in the V_{CC} supply" using *this novel charge pump circuit*, "power consumption is reduced, and the output voltage and peak-to-peak noise variations are limited, thereby enabling a more efficient, low power voltage[.]" *Id.*, 4:36-59; *see also id.*, 10:41-60. Notably, Le places no restriction on the type of shunt regulator that can be used with the charge pump circuit of its invention, but discloses that "a shunt regulator circuit"—not just specific types of shunt regulator circuits—"which may operate in conjunction with such a charge pump circuit will consume less power

and regulate the charge pump output with less ripple than with conventional charge pump circuits.” *Id.*, 6:15-26; *see also id.*, 4:60-63 (noting that an advantage of the Le’s invention is “the ability of the charge pump **and shunt regulator system** to produce a lower noise output”); Ex-1023, ¶¶54-55. *See also* EX-1024, 143:15-144:5, 145:2-22, 148:2-18, 150:14-151:1 (Dr. Brogioli agreeing that (i) Le discloses use of shunt regulator with Le’s improved charge pump to reduce power consumption and increase power savings, and (ii) Le does not limit to any specific shunt regulator structure).

Patent Owner would have us believe that “Le’s *design goal* is to minimize the use of the shunting regulator to minimize power consumption within the memory device.” POR, 38. But a POSITA would have found that Le makes no such statement, either implicit or explicit. EX-1023, ¶54. Rather, as noted previously, Le’s design goal is “a low power, low noise means of compensation for the variations in the V_{CC} supply applied to the charge pump circuit, **while maintaining a simple regulator design**,” which Le achieves by its invention of “a novel charge pump circuit [with] one or more individual stages [each] having a variable bootstrap capacitance value.” EX-1008, 4:15-35; EX-1023, ¶¶54-55. Even the sections of Le cited by Patent Owner and Dr. Brogioli in apparent support for such a design goal makes clear that Le encourages utilizing a shunt regulator, rather than teaching away from using, or reducing the use of one: noting that while

the novel charge pump achieves low power consumption, low ripple and low noise output voltage, use of a shunt regulator—irrespective of the type—“provides for a **further** reduction in power consumption” and “a smaller ripple voltage.” EX-1008, 10:54-11:6; EX-1023, ¶¶54-55.

Patent Owner relies on its unsupportable argument about Le’s design goal and teaching away from “continual use of a shunt regulator” to disparage Ujiie’s shunt regulator for using clamp diodes, which allegedly would be used constantly at low voltages, per Dr. Brogioli’s testimony. POR, 39-41 (citing EX. 2013, ¶¶85-88). Dr. Brogioli asserts that Ujiie’s shunt regulator would consume significant power when the breakdown voltage of the clamp diodes is less than the charge pump output voltage. Ex. 2013, ¶¶85-87. However, Ujiie contemplates customizing the breakdown voltages of the clamp diodes depending on the target output voltage of the charge pump: “Diodes with different breakdown voltages can be formed with a high degree of accuracy by using, for example, Zener diodes and appropriately controlling the amount of ion implantation that occurs into the semiconductor region.” EX-1009, ¶¶21-22, ¶26; EX-1023, ¶¶56-58. A POSITA would have found it obvious to configure the breakdown voltages of the clamp diodes depending on the target output voltage to further reduce power consumption in the shunt regulator used in the Le-Ujiie combination. EX-1023, ¶¶56-58. A POSITA would also have noted that neither Le nor Ujiie discloses any voltage

range, let alone specifies different voltage ranges in which particular types of shunt regulators should be used or not. EX-1023, ¶58.

Dr. Brogioli also faults Dr. Dicken's testimony about using Kuriyama's control circuit to turn off Le-Ujiie's the charge pump circuit. Ex. 2013, ¶88 (citing EX-1003, ¶167). However, Dr. Brogioli does so by relying on problems in *conventional* charge pump systems, which are addressed by Le's novel charge pump circuit that is used in the Le-Ujiie combination. EX-1023, ¶¶59. Dr. Brogioli's position is also based on Le's disclosure about the ripple caused due to the feedback-response delay of the shunt regulator as the charge pump circuit increases the output voltage, but this does not address turning off the entire charge pump circuit when the target output voltage is reached. *Id.*

Patent Owner cites to various court and Board decisions to buttress its argument that a POSITA would not have been motivated to combine Le with Ujiie, relying on its fallacious argument about Le's teaching away from the continual use of a shunt regulator. POR, 41-44. As explained above, Patent Owner misrepresents Le's objectives and, even otherwise, ignores clear disclosures in Le and Ujiie that make the combination feasible. The Petition established a motivation to combine Le and Ujiie: Le contemplates using its novel charge pump circuit with a shunt regulator—no restrictions on the type—and Ujiie discloses one such shunt regulator that can be customized depending on the target voltage output.

Pet., 50-52; EX-1003, ¶¶142-143; EX-1023, ¶¶57-58. That is sufficient for a POSITA to combine the two references: “[A]ny need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed”

Intel, 61 F.4th,1379 (citing *KSR*, 550 U.S., 420); “[i]t’s not necessary to show that a combination is the *best* option, only that it be a *suitable* option” *Intel*, 61 F.4th, 1380 (citing *KSR*, 550 U.S., 800). As the court held in *Intel*, it is enough to show that there was a known problem of output voltage regulation in the art as contemplated by Le, that Ujiie’s shunt regulator helped address that issue, and that combining the teachings of Le and Ujiie was not beyond the skill of a POSITA. “*Nothing more is required to show a motivation to combine under KSR.*” *Intel*, F.4th, 1381.

For at least the above reasons, the Board should reject Patent Owner’s spurious arguments against the motivation to combine Le and Ujiie.

V. CONCLUSION

Petitioner has established that the Challenged Claims are unpatentable and respectfully requests that the Board find the same.

Respectfully submitted,

Dated: June 14, 2024

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CERTIFICATION UNDER 37 C.F.R. § 42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petitioner Reply to Patent Owner Response totals 5,559 words, which is less than the 5,600 allowed under 37 CFR § 42.24(c)(1).

Dated: June 14, 2024

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4) and 42.205(b), the undersigned certifies that on June 14, 2024, a complete and entire copy of this Petitioner's Reply to Patent Owner's Response and accompanying exhibits were provided by email to the Patent Owner by serving the correspondence address of record as follows:

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