

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Micron Technology, Inc.,
Petitioner

v.

Sonrai Memory Limited,
Patent Owner

Case IPR2023-00909
Patent No. 6,724,241

Supplemental Declaration of James C. Dickens, Ph.D., P.E.

I, James C. Dickens, Ph.D., P.E., declare that:

I. INTRODUCTION

1. My name is James Claude Dickens, and I have been retained by counsel for Petitioner Micron Technology, Inc. (“Micron” or “Petitioner”) as an expert witness to provide assistance in the above-captioned *inter partes* review (“IPR”) proceeding regarding U.S. Patent No. 6,724,241 (“the ’241 Patent”). I previously submitted a declaration (EX-1003) in support of the Petition for IPR of the ’241 Patent. This declaration is in support of Petitioner’s Reply to Patent Owner’s Response in the same proceeding.

2. I understand that Patent Owner submitted a Patent Owner Response (“POR”), along with a declaration from Dr. Brogioli (Ex. 2013) in support of the POR.

3. My background and qualifications were provided in my first declaration, EX-1003, and my CV was submitted as EX-1004. My statements and opinions in my first declaration regarding my review of the ’241 patent and related materials remain unchanged. In reaching my opinions in this declaration, I have reviewed the POR, Dr. Brogioli’s declaration (Ex. 2013), my first declaration (EX-1003), the materials reviewed as part of my first declaration, the exhibits listed by Micron and Patent Owner, a transcript of Dr. Brogioli’s deposition of June 5, 2024 (EX-1024), and any materials cited herein.

4. I have no financial interest in either party or in the outcome of this proceeding. I am being compensated for my work as an expert on an hourly basis, for all tasks involved. My compensation is not dependent on the outcome of these proceedings or on the content of my opinions.

II. LEVEL OF ORDINARY SKILL IN THE ART

5. I stand by my opinion on the level of ordinary skill in the art, which I understand Dr. Brogioli adopted in his declaration. EX. 2013, ¶¶29.

III. LEGAL STANDARDS

6. I incorporate by reference my understanding of the legal principles, including my discussion of claim construction, obviousness, and the level of ordinary skill in the art as set forth in my first declaration. EX-1003, ¶¶16-32.

IV. TECHNICAL DISCUSSION

7. The analysis and opinions expressed in my first declaration fully explain why each and every feature of the '241 Patent's Challenged Claims is provided in the prior art. I understand that Patent Owner and Dr. Brogioli have considered my opinions and offered their own, some of which are inconsistent with my view. I will address some of those points below. To the extent that I have not addressed all of Patent Owner's and Dr. Brogioli's opinions, this should not be interpreted as agreement with them.

8. The POR fails to address, much less rebut, positions advanced in my

previous testimony. Patent Owner relies upon Dr. Brogioli for these positions, but Dr. Brogioli provides no corroborating evidence or factual analysis in support of his conclusions.

9. As I previously explained with reference to the applied prior art and corroborating references, the Challenged Claims would have been obvious to a POSITA. Below, I provide further testimony in response to Patent Owner's arguments.

V. THE DOLUCA-BUTI COMBINATION RENDERS OBVIOUS THE LIMITATION OF A PUMPING CIRCUIT GENERATING A SELECTED ONE OF A PLURALITY OF PUMP VOLTAGES

A. Generating “a selected one of a plurality of pump voltages” does not require generating the plurality of pump voltages at runtime for selection

10. In disagreement with my earlier analysis in support of Grounds 1A and 1B of the Petition, Dr. Brogioli starts with a detailed analysis of the teachings of Doluca, with a focus on the operations of Doluca's disclosed circuit embodiments. EX. 2013, ¶¶36-45. Dr. Brogioli notes that Doluca's “capacitor plate voltage generator circuitry is designed to generate an output voltage of between 6.1 V (where the charge pump turns on) and 6.1 V plus a small offset voltage,” which a POSITA would consider “a single output voltage,” according to Dr. Brogioli. *Id.* ¶45. Dr. Brogioli then opines that Doluca's generation of this “single output voltage” does not meet the claim language, which recites generating

“a selected one of a plurality of pump voltages.” *Id.*

11. I believe that Dr. Brogioli’s reasoning is flawed because there is no justification for equating (a) the claimed “generat[ing] a selected one of a plurality of pump voltages” to (b) generating a plurality of pump voltages during pump operation for selection.

12. First, the claim language only requires the pumping circuit to generate *one* pump voltage. Dr. Brogioli repeatedly emphasizes that claim 1 requires the pumping circuit to generate *multiple* different pump output voltages. EX. 2013, ¶¶45, 46, 48. I do not see how the ’241 Patent supports Dr. Brogioli’s observation. Not only does claim 1 expressly recites “one” voltage to be generated, the ’241 Patent expressly contemplates the charge pump circuit generating “*one or more* pump voltages.” EX-1001, 3:7-12 (emphasis added); *see also* 4:64-67. In my opinion, a POSITA, with full and accurate understanding of the ’241 Patent, would not have excluded the scenario of a pumping circuit generating a single output voltage from the scope of claim 1.

13. Further, even if the generated one voltage according to the ’241 Patent is a result of selection from multiple candidate voltages, the claim language does not require that the selection take place contemporaneously with generation of the voltages, i.e., during the operation of the pumping circuit. In other words, the claim does not require the multiple candidate voltages be available for selection

when the pumping circuit is in operation, otherwise referred to as at runtime.

14. I believe that a POSITA would have known that some circuits would allow generating an output voltage according to configurations selected *prior to* circuit runtime, such as during the design, manufacture, or installation phases of the circuit. Doluca's teachings about the selection of the K value, which I have explained in my earlier declaration, provide an example of such circuits, EX-1003, ¶83, and Dr. Brogioli admitted that K is "a mathematical design criteria that Doluca used to design the charge pump control circuitry." Ex. 2013, ¶47. With the understanding that the selection of K—whether at the design phase or some different time—results in the selection of an output voltage of Doluca's charge pump circuit, a POSITA would have found that Doluca's teachings about choosing K satisfy the claim limitation in question. Dr. Brogioli's statement "[t]here is no K input to the Doluca capacitor plate voltage generation circuitry to allow that circuitry to generate any other voltage than that in the range of 6.1 V to 6.1 V plus a small offset voltage" is irrelevant to the claim language at issue here. *Id.*

B. Selectively coupling a load out of multiple loads does not require dynamically selecting a pump voltage out of multiple pump voltages

15. In the POR, Patent Owner argues that claim 1 requires dynamically selecting from a plurality of pump voltages because the claim requires "[a] plurality of loads selectively coupleable to an output of the pumping circuit" and

“each load [be] associated with a specific pump voltage.” POR, 7-8 and 29-30. In this context, Dr. Brogioli opines that the Doluca-Buti combination does not meet the claim limitation because each of transistors 42, 48, 54, and 60 of Buti are not separately “associated with a specific pump output voltage” and are not “selectively activated.” EX. 2013, ¶¶48-51, 62-63.

16. I disagree with both Patent Owner’s reasoning and Dr. Brogioli’s opinion. While I will address the operations of Buti’s transistors 42, 48, 54, and 60 later in this declaration, I note that it is technically unsound for Patent Owner to consider the dynamic selection of a specific pump voltage *as a consequence* of the dynamic selection of a load. POR, 7 (“Based on the totality of the claim, it requires that the loads and consequently the output voltage of the pumping circuit be dynamically selectable”). Different from the principle offered by Patent Owner, the ’241 Patent determines the target pump output voltage first (e.g., for performing a reading, programming, or erasing instruction, EX-1001, 1:13-15), and then selects a load to minimize voltage ripple for the target pump output voltage. *Id.* at 4:5-8.

17. Because the target pump output voltage is determined *prior to* the selection of load, it is technically and logically incorrect for Patent Owner to say that the *earlier* determination of pump voltage is a consequence of the *later* selection of load. Thus, regardless of whether the *later* selection of load is done

dynamically or statically, the *earlier* determination of pump voltage is not required to occur in the same manner, i.e., dynamically or statically.

18. To support its arguments, Patent Owner asserts that the claim limitation “load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit” reinforces the position that “the output voltage of the pumping circuit has to be dynamically selectable.” POR, 8-9 (quoting EX-1001, 8:24-26). To this end, Patent Owner relies on Dr. Brogioli’s analysis of the ’241 Patent’s structural description of the claimed “load selector means,” based on the following paragraph:

When an instruction for either VA, VB, or VC is received by a controller (not shown), the controller (not shown) generates the enable control signal EN_A, EN_B or EN_C that selects an appropriate load for this voltage that gives the minimum voltage ripple. **Only one load can be selected at a time.** For example, if voltage VA is selected, EN_A causes the first switch 320 to close, connecting the first load to the output terminal of the charge pump circuit 300. The remaining loads 326 and 330 are disconnected from the output terminal because their respective switches 324 and 328 are open.

EX-1001, 4:52-62 (emphasis added). *See also* EX. 2013, ¶¶66-67,

19. Reading the above paragraph, I do not think a POSITA would have come to the conclusion that Patent Owner and Dr. Brogioli have advanced. Instead, from the language “one load can be selected at a time” and “if voltage VA is selected, EN_A causes the first switch 320 to close,” a POSITA would have understood that this paragraph merely precludes closing (e.g., toggling) multiple switches from an Off state to an On state at the same time. What this paragraph does not suggest or preclude is the possibility that one or more other switches are closed at different times – either earlier or later, i.e., having additional loads coupled to the charge pump output either before or after the closing of the instant switch. For example, while this paragraph precludes toggling switches 320 and 324 at the same time, the paragraph does not preclude toggling switch 320 at a first time and toggling switch 324 at a later time, after which both load A 322 and load B 326 are coupled to the charge pump output.

20. The above understanding is corroborated by the illustration and discussion with respect to FIG. 10 of the '241 Patent, which “shows a method 1000 usable especially with the circuits of FIGS. 3 and 7.” EX-1001, 7:6-8:14; *see also id.*, FIG. 10 (reproduced below).

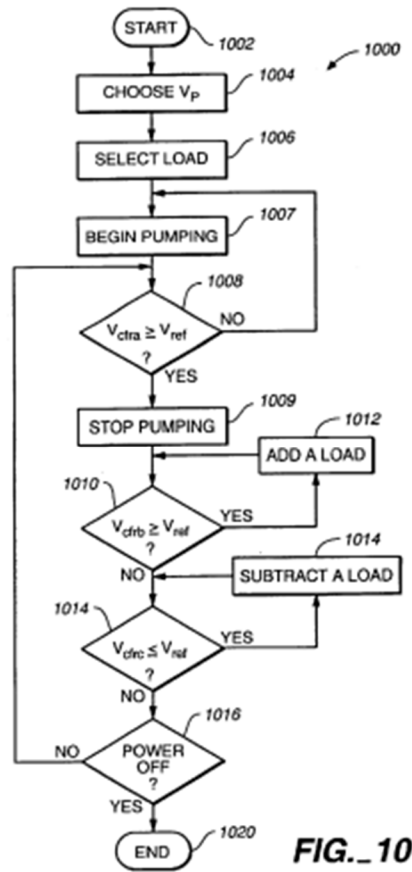


FIG. 10

EX-1001, FIG. 10

21. Here in FIG. 10 of the '241 Patent, the maximum ripple target output voltage V_{cfrb} is compared with reference voltage V_{ref} at step 1010. *Id.* at 7:6-30. If $V_{cfrb} \geq V_{ref}$, the method proceeds to step 1012 to add a load. *Id.* (emphasis added). The loop formed by steps 1010 and 1012 continues until $V_{cfrb} < V_{ref}$, i.e., the ripple is reduced to below a threshold.

22. By illustrating steps 1010 and 1012 as a loop, the '241 Patent expressly contemplates repeating the addition of a load at step 1012, as would have been readily appreciated by a POSITA. This is further evidenced by the express

description in the '241 Patent: “At step 1012, the circuit 600 adds a load so that voltage ripple can be reduced. *This Step continues* until the Voltage ripple is reduced and then the circuit 600 goes to the next Step.” *Id.* at 7:61-64.

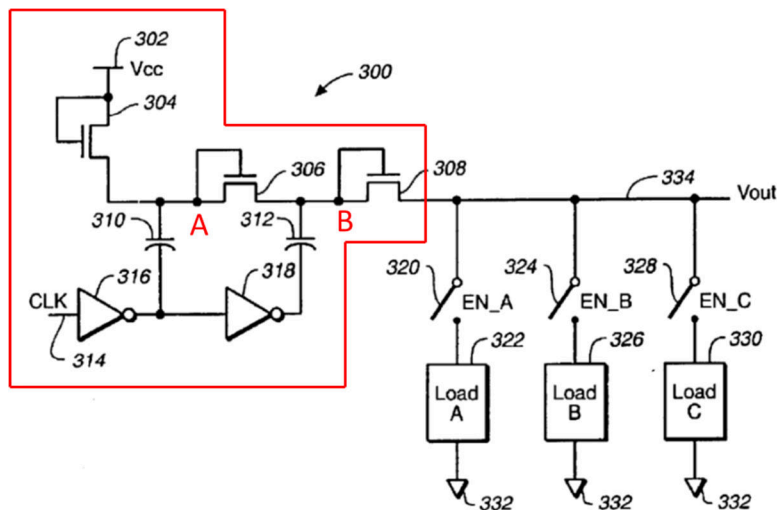
23. In both the drawing and the text, the '241 Patent unambiguously allows coupling multiple loads to the charge pump output, while only stating that multiple switches are not toggled at once. Accordingly, I believe that a POSITA would have found Patent Owner and Dr. Brogioli's following assertion to be incorrect: that the corresponding structure of the claimed “load selector means” “requires coupling of each load to the output of the pumping circuit to be to the exclusion of the other loads.” POR, at 32; EX. 2013, ¶71. Patent Owner and Dr. Brogioli's further assertions relying on a misrepresentation of the '241 Patent's disclosure are also similarly unjustified.

C. Requiring the pumping circuit to be able to dynamically generate multiple output voltages is inconsistent with the disclosure of the '241 Patent

24. Claim 1 of the '241 Patent, directed to a “charge pump circuit,” recites three components: a pumping circuit, a plurality of loads, and a load selector means. EX-1001, claim 1. Mapping these components to the circuit of FIG. 3 of the '241 Patent (reproduced below with annotation), a POSITA would have understood that the “pumping circuit” corresponds to the circuit formed by elements 302-318 (in the red enclosure below), which is substantially the same as

the circuit 100 shown in FIG. 1, and also referenced in FIGS. 6 and 7 as pump 100.

See EX-1001, 1:23-54, 3:64-4:32, 5:45-6:21, and FIGS. 1, 3, 6 and 7. Indeed, I understand that, during his deposition, Dr. Brogioli acknowledged that this is the pumping circuit as recited in claim 1 of the '241 Patent. See EX-1024, p. 91, l. 8-p. 97, l. 12.



EX-1001, FIG. 3 (annotated)

25. As the '241 Patent notes, the pumping circuit in FIG. 3 is a two-stage charge pump with inverter 316, capacitor 310 and transistor 306 forming one stage, and inverter 318, capacitor 312 and transistor 308 forming a second stage. *Id.* The output voltage of the pumping circuit, which is delivered at the output terminal of the transistor 308, is the sum of the voltages at nodes A and B. EX-1001, 1:40-51. In general, the output voltage of a pumping circuit is dependent on the number of

stages. As can be seen from FIG. 3 (and also FIG. 1), the pumping circuit does not provide any mechanism to dynamically change the voltage that is provided at the output of the pumping circuit. Once the circuit is realized in hardware, it can be used to generate only one pump voltage; to generate different pump voltages, additional pump stages are needed. While the '241 Patent mentions that pumping circuit can have n stages where $n > 1$ (*see* EX-1001, 3:67-4:2, 4:30-32), a POSITA would have understood that changing the number of pump stages can be done during the circuit design phase, considering, e.g., how much voltage is needed from the pumping circuit. A POSITA would have understood that adding different pump stages require different designs of the pumping circuit, and different hardware implementations. The '241 Patent does not provide any teaching or suggestion that such different stages can be dynamically added or removed. Once the circuit is designed, manufactured and deployed with a fixed power supply V_{cc} , there is generally no mechanism to dynamically change the pumping circuit output voltage based on the disclosure the '241 Patent.

26. The mechanism disclosed in the '241 Patent that allows the charge pump circuit to adjust the output voltage during operation is through the selection of loads, which are external to the pumping circuit. As clearly shown in FIG. 3, such external mechanism does not have an input to the “pumping circuit” and thus does not allow the “pumping circuit” to select among multiple output voltages

during runtime. Also, the adjustment is done to reduce the ripple for the one target output voltage as described with respect to FIGS. 4A-4C, but this does not allow selection of an altogether different charge pump output voltage. *See, e.g.*, 4:62-5:21 and FIGS. 4A-4C.

27. The embodiment of FIG. 7 of the '241 Patent and its corresponding description disclose two voltage dividers, one formed by resistors 704 and 706 and another formed by resistors 708 and 710. EX-1001, FIG. 7. Comparators 702 and 714 each compares a sample of the pump output voltage V_{out} with a reference voltage V_{ref} . *Id.* During the operation of circuit 700, resistors 704 and 706 and comparator 702 form a feedback loop to disable pump 100 when V_{out} becomes too high. *Id.* at 6:4-17. This feedback loop is similar to that illustrated in FIG. 6. The disabling of pump 100, though happening during the runtime of pump 100, does not affect the selection of pump output voltage or load.

28. Meanwhile, resistors 708 and 710 and comparator 714 form a control mechanism to “instruct[] the logic circuit 712 to add the load S 718” when the ripple on the output voltage V_{out} becomes excessive. *Id.* The addition of load S 718 is outside of pump 100 and is not a means for dynamically selecting the pump output voltage V_{out} .

29. In light of the embodiments given by the '241 Patent, it would have been clear to a POSITA that the pumping circuit of the '241 Patent is not

dynamically controlled for the selecting an output voltage. Dr. Brogioli's attack on Doluca, which relies on an observation "[t]here is no K input to the Doluca capacitor plate voltage generation circuitry ..." (for controlling Doluca's charge pump circuit), EX. 2013, ¶47, is thus unjustified. If Dr. Brogioli's observation could support Dr. Brogioli's purported distinction between Doluca and the claim language, EX. 2013, ¶47, then there being no control signal input to the "pumping circuit" in FIG. 3 or to pump 100 in FIG. 7 of the '241 Patent would lead to a similar—and incorrect—conclusion that the claim language of the '241 Patent is contradicted by its own embodiments. Clearly, this incorrect conclusion is due to the unwarranted equation between a) and b), *supra* ¶13, which is an unduly narrow reading of the claim language.

VI. THE DOLUCA-BUTI COMBINATION READS ON THE CLAIM LANGUAGE EVEN IF INTERPRETATED TO REQUIRE THE PUMPING CIRCUIT GENERATE A PLURALITY OF VOLTAGES FOR DYNAMIC SELECTION

A. Doluca's charge pump output voltage can be dynamically adjusted

30. Although, as I have stated above, I believe the claims of the '241 Patent do not require dynamic selection of an output voltage from multiple voltages, nevertheless such a feature is taught by Doluca and would have been present in the Doluca-Buti combination, as I explain below.

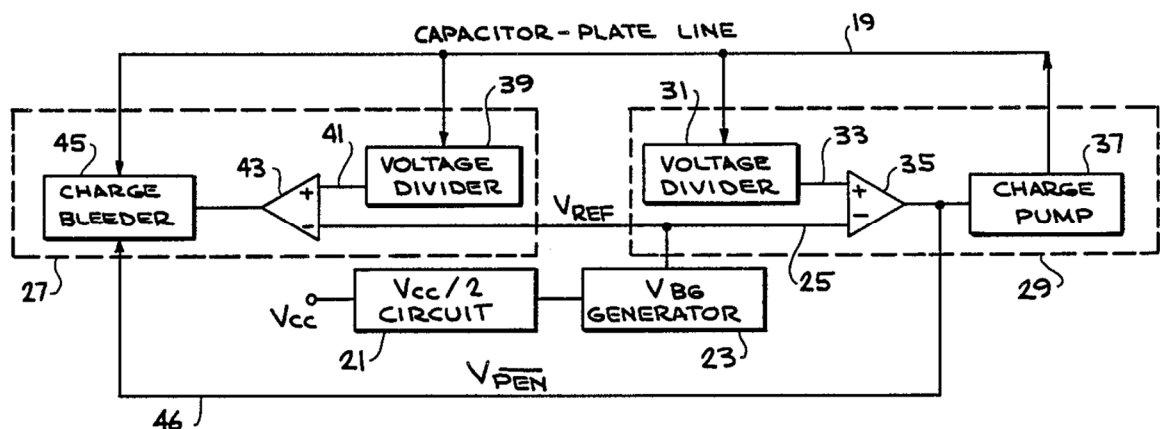
31. At the outset, I have explained that the '241 Patent provides no means

of dynamic voltage selection by adjusting the pumping circuit. *Supra*, ¶¶24-29.

Rather, any mechanism given in the '241 Patent is external to the pumping circuit.

In the embodiment of FIG. 7, for example, the mechanism includes comparator 702 and resistors 704 and 706, and comparator 714, resistors 708 and 710, and logic 712, all external to pump 100. *Supra*, ¶27. By taking samples of the pump output voltage and comparing the sample voltages with reference voltage V_{ref} , the mechanism allows either shutting down the pumping circuit 100 (using comparator 702), or adding load S 718 (using comparator 714 and logic 712) to suppress voltage ripple. *Id.*

32. If the above mechanism is considered a dynamic selection mechanism, then the Doluca-Buti combination also has a dynamic selection mechanism that reads on the claim limitation “generate a selected one of a plurality of pump voltages” of claim 1. This mechanism is illustrated in FIG. 2 of Doluca (reproduced below) for controlling the output voltage V_{CP} of charge pump 37.



EX-1006, FIG. 2

33. Specifically, Doluca teaches the voltage V_{CP} output by charge pump 37 as a function of the supply voltage V_{CC} and a value K : $V_{CP} = V_{CC}/2+K$, where K can be chosen between 3.5 and 4. EX-1006, 3:38-54. Doluca also explains that how the choice of K translates to the selection of voltage divider 31 whose output is compared to V_{ref} to set the charge pump 37 enable level. EX-1006, 4:18-52.

34. Accordingly, if a POSITA desired a dynamic voltage adjustment, Doluca could be implemented with dynamic adjustment of the voltage dividers 31 and 39, as a POSITA would have readily known. Then Doluca would allow dynamic selection of K and consequently dynamic selection of the output voltage V_{CP} from within a preselected range of voltages. *See, e.g., id.*, 7:33-8:14.

35. Alternatively, nothing in Doluca would prevent or discourage the dynamic adjustment of V_{BG} . In fact, Doluca leaves the implementation of the V_{BG} generator as an open design choice. *Id.* 3:62-4:3 (“Any of the known circuits for producing V_{BG} ... may be used as V_{BG} generator 23.”). Given that Doluca has expressly contemplated adjusting K to change V_{CP} , a POSITA would have been motivated to consider making V_{BG} adjustable based on V_{CP} .

36. To a POSITA, adjusting a circuit parameter based on the circuit’s output voltage is a classic example for feedback-based voltage regulation. Personally, being a professor in the art of electrical engineering (EE) and having helped many people develop ordinary skills in the art, I would expect any fresh EE

graduate to have the abilities and knowledge to implement a feedback-based control mechanism to dynamically change the output voltage of a circuit based on a dynamic voltage divider. Since Doluca has provided a motivation to make V_{BG} adjustable in order to regulate V_{CP} , *supra* ¶35, a POSITA would have no problem coming up with an implementation and combine it with Buti (the motivation for the combination is discussed later in this Declaration). The resultant circuit would have the capability of dynamically selecting a pump output voltage from a plurality of voltages, and would read on the claim language, even if narrowly interpreted as Patent Owner and Dr. Brogioli have argued. Further, as I have noted in my first declaration, several other references relied on in the petition also teach that the charge pump can output multiple different voltages. For example, Le teaches that its charge pump output voltage can have different voltage levels for program/erase operations of memory cells. EX-1008, 1:7-18, 1:51-2:34; EX-1003, ¶146. Ujiie teaches that its shunt regulator can output write voltage V_{pp1} or erase voltage V_{pp2} . EX-1009, ¶¶[18]-[25]; EX-1003, ¶148. Kuriyama describes that its charge pump can be turned on or off by comparing the output voltage with a reference voltage V_{ref} , and that the charge pump can output different voltages for write, erase or read operations. EX-1011, 4:42-5:18, 11:19-13:3, FIGS. 12-15; EX-1003, ¶¶161-166. Indeed, Dr. Brogioli has not disputed any of these teachings.

B. A POSITA would have been motivated to combine Buti with Doluca

37. In my earlier declaration, I had explained that a POSITA would have found it obvious to combine Buti and Doluca because, in part, Buti provides an example of a charge bleeder with operational details, which could supplement Doluca's description of bleeder 45. EX-1003, ¶¶70-72. However, according to Dr. Brogioli, because Doluca discloses current-regulating transistor 79 as part of its bleeder control circuit 27, there would not have been motivation to further look into Buti for other possible charge bleeder implementations. EX. 2013, ¶¶53-54.

38. I disagree with Dr. Brogioli's reasoning. First, the shunt regulator illustrated in FIG. 2 of Doluca is illustrated in a block diagram with no transistor-level detail, so this illustration would encourage—rather than discourage—a POSITA to look into other references that provide implementation details at the transistor level, such as Buti.

39. Second, Doluca describes that the “[t]ransistor 79 serves as a non-linear current regulator having a generally parabolic current-voltage characteristic.” EX-1006, 6:53-58, FIG. 5. This brief description does not sufficiently inform a POSITA about how to implement Doluca's bleeder control circuit 27 at the transistor level. A POSITA would know that the specific implementation of the bleeder circuit utilizing transistor 79 is highly non-linear and would need to examine the bleeder circuit in detail to properly design and size the circuit elements. Accordingly, Doluca's description of transistor 79 would not have

foreclosed a POSITA from looking elsewhere, such as Buti, for details about a charge bleeder circuit.

40. As I previously explained, Buti describes a bleeder circuit whose bleeding current is dependent upon the output voltage of a charge pump: When the output voltage increases too fast, the bleeder circuit turns on more bleeding paths to slow down the voltage ramp-up. EX-1003, ¶¶64-68, 71.

41. Further, Dr. Brogioli appears to consider Buti's voltage ramp-up rate regulation as distinct from voltage regulation as in Doluca. EX. 2013, ¶¶55-61. Dr. Brogioli makes a statement that Buti "is not directed at providing multiple different output voltages, e.g., for writing and erasing flash memory devices," but rather has a goal of regulating the ramp-up rate with respect to "a single output voltage of 12.95 V." *Id.* at ¶57.

42. While Buti provides a specific example for the pump output voltage to ultimately reach a stable 12.95 V, I disagree with Dr. Brogioli's proposition that Buti's regulation *during the ramp-up period* is distinguishable from Doluca's voltage regulation. The regulation in Buti regulates the voltage ramp-rate which a POSITA would understand *is* a form of voltage regulation. Moreover, a POSITA understands from basic feedback theory, that ramp-rate regulation is important and plays a role in voltage overshoot performance.

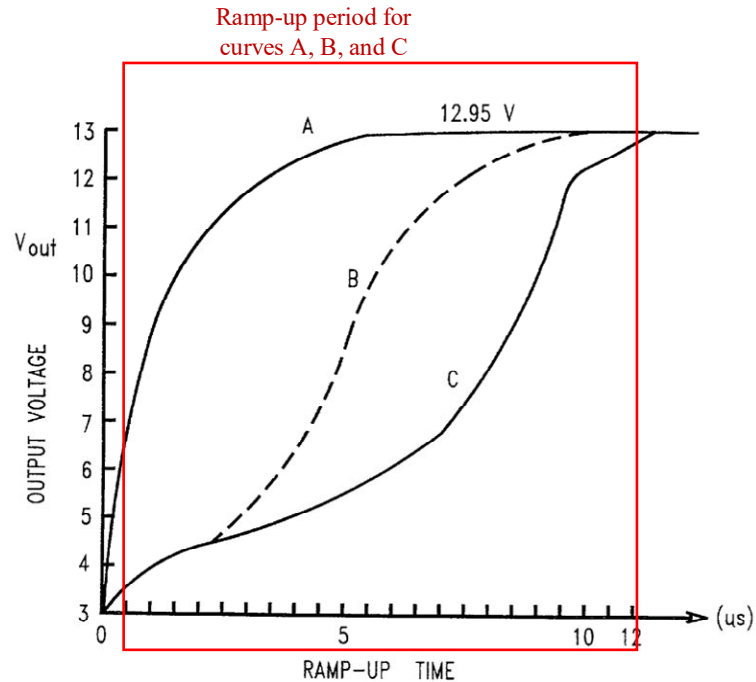


FIG. 6

EX-1005, FIG. 6 (annotated)

43. Accordingly, I believe that a POSITA would have found that Doluca and Buti both are directed to regulating the voltage at a charge pump output. A POSITA would further have noted that this teaching of Doluca and Buti is consistent with the '241 Patent. EX-1001, 3:1-22.

C. The Doluca-Buti combination teaches the claim limitation “a plurality of loads ... each load associated with a specific pump voltage”

44. Relying on a mapping of FETs 42, 48, 54, and 60 of Buti to four different loads, Dr. Brogioli argues that the charge bleeder of Buti does not have “a plurality of loads ... each load associated with a specific pump voltage.” EX.

2013, ¶¶62-65. Dr. Brogioli further disagrees with my opinion that these FETs in the Doluca-Buti combination circuit are “selectively activated or deactivated.” *Id.*

45. Dr. Brogioli appears to require the Doluca-Buti combination to operate in exactly the same way as Doluca. In analyzing the operations of FETs 42, 48, 54, and 60, he considers scenarios where “ V_{CP} is above 6.1 V” and where “[V_{CP}] goes below 6.1 V,” which are conditions for turning $\overline{VPEN}$ on or off, respectively. *Id.* at ¶62. The value of 6.1 V and the corresponding turning of $\overline{VPEN}$, are specific to Doluca’s “5 V V_{CC} DRAM device” as analyzed by Dr. Brogioli. *Id.* at ¶¶43-45, 47-48.

46. Dr. Brogioli then turns to FETs 42, 48, 54, and 60 in the circuit of the Doluca-Buti combination, and, by referring to Table 1 of Buti, notes that “transistor 42 will never turn on” and “transistors 48, 54 and 60 will never turn off” under the conditions set forth in Doluca. *Id.* at ¶62. Based on this, Dr. Brogioli concludes that the FETs in the Doluca-Buti combination circuit are not selectively activated or deactivated and are not “loads” that are each “associated with a specific pump voltage.”

47. Dr. Brogioli’s conclusion relies on a misconception that the Doluca-Buti combination must satisfy operating conditions and design specifics of both Doluca and Buti. According to this misconception, the Doluca-Buti combination must both comply with the 6.1 V voltage threshold for turning on or off $\overline{VPEN}$ in

Doluca's "5 V VCC DRAM device," and at the same time comply the specific voltage values shown in Table 1 of Buti to control the current paths. This is simply not what the combination is about. As I have noted in my previous Declaration, a POSITA would have combined Doluca and Buti to address various technical needs in related technologies, such as charge pump voltage regulation, and would have found it obvious to make routine and obvious modifications to the combined circuit. EX-1003, ¶¶69-72. The combined circuit should not be rigidly required to meet every detailed design and operation specific in both references.

48. I maintain my opinion that the Doluca-Buti combination renders obvious the claim limitation "a plurality of loads ... each load associated with a specific pump voltage." EX-1003, ¶¶85-86. This opinion stands true for mappings of the "plurality of loads" to FETs 42, 48, 54, and 60. As I have mentioned in my earlier Declaration, "each of FET loads 42, 48, 54, and 60 can be selectively activated, i.e., selectively coupled to charge pump 37," depending on the charge pump voltage V_{CP} . This would read on the claim language "a plurality of loads ... each load associated with a specific pump voltage." *Id.* Alternatively, each load corresponds a subset of FETs 42, 48, 54, and 60. For example, FET 42 can be considered a first load, FETs 42 and 48 can be considered a second load, FETs 42, 48, and 54 can be considered a third load, and FETs 42, 48, 54, and 60 can be considered a fourth load. Under this mapping, the four loads are

activated/deactivated one after another as the charge pump voltage V_{CP} increases/decreases. *Id.* at ¶¶85-91. This would also read on the claim language “a plurality of loads ... each load associated with a specific pump voltage.” A POSITA would have known that loads can be additive.

49. As I have discussed in my earlier declaration, to which Dr. Brogioli has not objected, a POSITA would have construed the claimed “load” either broadly to mean “a device that receives electrical power,” or narrowly to mean “a device that absorbs surplus charge to reduce voltage ripple when compared to a case without the device.” *Id.* at ¶¶45-47; *see also* Ex. 2013, ¶30. A POSITA would have understood that both mappings discussed above are consistent with the claim construction of “load,” whether under the broad version or under narrow version.

D. The Doluca-Buti combination teaches the claim limitation “load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit”

50. Dr. Brogioli has opined that the Doluca-Buti combination does not teach “load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit” because this means-plus-function limitation, as understood by Dr. Brogioli, requires only one load be coupled to the charge pump output at a time. Ex. 2013, ¶¶66-73.

51. However, as I have analyzed above and clearly evidenced by FIG. 10

of the '241 Patent, it is a fundamental misrepresentation of the '241 Patent's description to require only one load be coupled to the charge pump output at a time. *Supra* ¶¶18-23. Instead, as long as multiple switches are not toggled at the same time, the '241 Patent contemplates having more than one load coupled to the charge pump output. *Id.*

52. In view of the above, I maintain my opinion that the limitation “load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit” would have been obvious to a POSITA in view of the Doluca-Buti combination. EX-1003, ¶¶87-91.

VII. A POSITA WOULD HAVE BEEN MOTIVATED TO COMBINE LE WITH UJIE

53. Dr. Brogioli opines that a POSITA would not have been motivated to combine Le and Ujiie because Le's design goal of “minimiz[ing] the use of the shunting regulator to minimize power consumption within the memory device” would be countered by the use of Ujiie's shunt regulator. Ex. 2013, ¶¶84-88. As I explain below, Dr. Brogioli's opinion is misplaced.

54. I believe that it is inaccurate and misleading to characterize Le's design goal as “to minimize the use of the shunting regulator to minimize power consumption within the memory device.” *Id.* at ¶84. Le says no such thing whatsoever. Rather, as evidenced in numerous statements of Le, Le considers noise reduction from the use of a shunt regulator as another objective or advantage

of its disclosure. A few of such statements are reproduced below, with emphases added.

Accordingly, **there is a need for a low power, low noise means** of compensation for the variations in the VCC supply applied to the charge pump circuit ... (EX-1008, 4:15-18)

An advantage of the present invention is the ability of the charge pump and shunt regulator system to produce a lower noise output, as compared to conventional charge pump and regulator systems without compensation ... (*id.*, 4:60-63)

Consequently, the present invention provides a low power, efficient, **low noise** charge pump output voltage, for example, a charge pumped wordline or bitline voltage, which facilitates an accurate operation of flash memory cells despite fluctuations in the VCC supply voltage ... (*id.*, 5:22-27)

Consequently, a **shunt regulator circuit which may operate in conjunction with such a charge pump**

circuit will consume less power and regulate the charge pump output with less ripple than with conventional charge pump circuits ... (*id.*, 6:21-25).

In addition, the charge pump circuit of the present invention provides for a further **reduction in power consumption when used in conjunction with a shunt regulator** ... (*id.*, 10:51-53).

55. In short, there is overwhelming evidence that Le actually *contemplates and encourages* using a shunt regulator, which helps to reduce volage ripple, and in conjunction with Le's charge pump embodiments help to reduce power consumption. Having a comprehensive and truthful understanding of Le, it would be false and disingenuous for a POSITA to contend the opposite.

56. Patent Owner and Dr. Brogioli assert that a POSITA would not have utilized the clamp diodes of Ujiie as a shunt regulator in conjunction with Le's charge pump circuit because the feedback and response time delays of the shunt regulator would lead to greater ripple and a higher degree of noise spikes and valleys. POR, 39-41 (citing Ex. 2013, ¶¶85-88).

57. I disagree with the above assertion. As I analyzed above, reducing noise and reducing power consumption are two design goals in consideration, and

circuit designers in practice routinely make tradeoffs between competing design goals. A POSITA would not have lost motivation to combine circuits solely because of the potential need of tradeoffs.

58. Conversely, in my opinion, a POSITA would have been motivated to utilize the clamp diodes of Ujiie with Le in this respect. As a POSITA would have known, shunt regulators based on clamp diodes do not suffer from the same turn-on delay as a MOSFET-based shunt regulator might have due to the gate charge time and effects of parasitic capacitance of MOSFETs. Accordingly, when choosing among different types of shunt regulators to be combined with Le's charge pump circuit, a POSITA would have found that Ujiie's clamp diode-based shunt regulator has the advantages of short delay and good efficiency. I also note that Ujiie teaches that the breakdown voltages of the clamp diodes in its shunt regulator can be customized according to the output voltage of the charge pump circuit. *See* EX-1009, ¶¶22, 26. This would have strengthened a POSITA's motivation to combine Le and Ujiie. I also note that Le or Ujiie does not disclose any voltage range. Indeed, neither reference specifies different voltage ranges in which particular types of shunt regulators should or should not be used.

59. Dr. Brogioli also takes issue with my explanation about using Kuriyama's control circuit to turn off the charge pump circuit in the combination of Le and Ujiie. Ex. 2013, ¶88. However, Dr. Brogioli relies on problems that are

faced by conventional charge pump systems to make his argument. I believe that a POSITA would have readily noted that these problems are addressed by Le's novel charge pump circuit that is used in the Le-Ujiie combination, as I have noted above. *Supra* ¶¶54-57. Dr. Brogioli's position is also based on Le's disclosure about the ripple caused due to the feedback-response delay of the shunt regulator as the charge pump circuit increases the output voltage, but this does not address turning off the entire charge pump circuit when the target output voltage is reached.

VIII. ADDITIONAL REMARKS

As my opinions in this declaration are made in response to the POR and Dr. Brogioli's declaration, I have not repeated my opinions on some of the secondary references, which were already addressed in my earlier declaration. To the extent the POR and Dr. Brogioli's declaration have purported claim constructions that I did not expressly address in my earlier declaration, my opinions set forth in the earlier declaration remain unchanged even under the newly-purported purported claim constructions.

I currently hold the opinions set expressed in this declaration. But my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

I hereby declare that all statements made of my own knowledge are true and

that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code.

Dated: June 13, 2024

By: 
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Lubbock, Texas