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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC.,
Petitioner,

v.

REALTEK SEMICONDUCTOR CORPORATION,
Patent Owner.

Case No. IPR2023-00920
U.S. Patent No. 8,006,218

PETITION FOR INTER PARTES REVIEW OF U.S. PATENT NO. 8,006,218

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TABLE OF EXHIBITS

Exhibit No.	Description
1001	U.S. Patent No. 8,006,218 ("'218 Patent" or "'218")
1002	File History for U.S. Patent No. 8,006,218
1003	Declaration of Dr. Vivek Subramanian ("Subramanian Decl.")
1004	Hailin Jiang et al., *Benefits and Costs of Power-Gating Technique*, Proceedings of the 2005 International Conference on Computer Design (ICCD 2005) ("Jiang")
1005	Wei Li et al., *LVS Verification across Multiple Power Domains for a Quad-Core Microprocessor*, ACM Transactions on Design Automation of Electronic Systems, Vol. 11, No. 2, pp. 490-500, (April 2006) ("Li")
1006	U.S. Patent No. 7,948,292 ("Chiu")
1007	Hailin Jiang et al., *Power/Ground Supply Network Optimization for Power-Gating*, Proceedings of the 2006 International Conference on Computer Design (ICCD 2006) ("Jiang2")
1008	Hailin Jiang et al., *Power-Gating Aware Floorplanning*, Proceedings of the 8th International Symposium on Quality Electronic Design (ISQED 2007) ("Jiang3")
1009	Suhwan Kim et al., *Minimizing Inductive Noise in System-On-a-Chip with Multiple Power Gating Structures*, ESSCIRC 2004 - 29th European Solid-State Circuits Conference (IEEE Cat. No.03EX705), pp. 635-638 (2003) ("Kim")
1010	U.S. Patent No. 7,705,486 ("Lee")
1011	U.S. Patent Application 60/976,181 ("Chiu Provisional")
1012	Michael Keating et al., *Low Power Methodology Manual*, Springer (2007) (excerpts) ("LPMM")
1013	A. Bertolet et al., *A Pseudo-Hierarchical Methodology for High Performance Microprocessor Design*, Proceedings of the 1997 International Symposium on Physical Design, pp. 124–129 (April 1997) ("Bertolet")

Exhibit No.	Description
1014	Luca Benini et al., *Advanced power management techniques: going beyond intelligent shutdown*, Proceedings of the 2003 Asia and South Pacific Design Automation Conference, pp. 385–389 (January 2003) ("Benini")
1015	Yajun Ran et al., *Via-Configurable Routing Architectures and Fast Design Mappability Estimation for Regular Fabrics*, IEEE/ACM International Conference on Computer-Aided Design (2005) ("Ran")
1016	U.S. Patent No. 7,671,623 ("Blisson")
1017	Screen shot of AMD Innovation Timeline, (available at https://www.amd.com/en/corporate/innovations)
1018	U.S. Patent No. 6,925,627 ("Longway")
1019	U.S. Patent No. 7,260,805 ("Yan")
1020	Kimiyoshi Usami et al., *Low-power Design Methodology and Applications utilizing Dual Supply Voltages*, Proceedings of the ASP-DAC 2000: Asia and South Pacific Design Automation Conference (2000) ("Usami")
1021	Declaration of Dr. Sylvia Hall-Ellis ("Hall Ellis Decl.")
1022	Curriculum Vitae of Sylvia Dr. Sylvia Hall-Ellis
1023	Order Granting Motion to Stay, *Realtek Semiconductor Corp., v. Advanced Micro Devices, Inc.*, Case No. 4:22-cv-04769-JSW, Dkt. 61 (N.D. Cal. Apr. 24, 2023)
1024	U.S. Patent No. 6,903,389 ("Tai")
1025	Synopsys Press Release, *Synopsys Galaxy Platform Reduces Power Consumption of Industry-Leading Multi-Voltage Designs*, Jul. 19, 2006 (available at https://news.synopsys.com/index.php?s=20295&item=122684)
1026	Synopsys Press Release Index, July 18, 2006 through July 26, 2006 (available at https://news.synopsys.com/index.php?s=20295&l=10&year=2006&o=50)

Exhibit No.	Description
1027	Synopsys Press Release, *New Low Power Methodology Manual Demystifies Advanced Power Management*, May 29, 2007 (available at https://news.synopsys.com/index.php?s=20295&item=122821)
1028	Synopsys Press Release Index, May 24, 2007 through May 29, 2007 (available at https://news.synopsys.com/index.php?s=20295&year=2007&o=60)
1029	Complainant's Proposed Claim Constructions, In the Matter Of Certain Integrated Circuits, Components Thereof, And Products Containing The Same, Investigation No. 337-TA-1350 (May 1, 2023)
1030	Respondent Advanced Micro Devices, Inc.'s Proposed Claim Constructions, In the Matter Of Certain Integrated Circuits, Components Thereof, And Products Containing The Same, Investigation No. 337-TA-1350 (May 2, 2023)

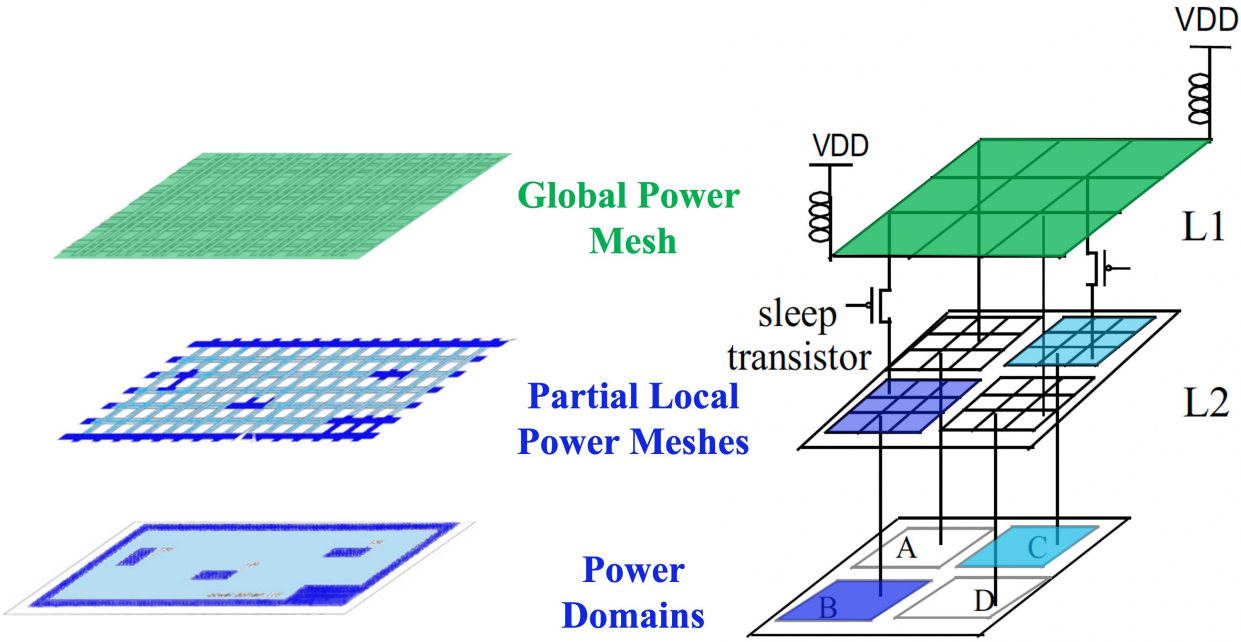
I. INTRODUCTION

Petitioner AMD is a global leader creating leading-edge semiconductor products, including high-end microprocessors, graphics processors, flash memories, and many other components that are widely used in consumer electronics products. AMD has a well-established history of innovation: it created the world's first 512K EEPROM in 1984, the first gigahertz CPU in 2000, the first 1GB GPU in 2006, first 5 GHz CPU in 2013, as well as many more industry firsts. EX1017.

Realtek sued AMD on three patents in the ITC and Northern District of California federal court, including the '218 Patent challenged here. Realtek asserted claims 12-18 and indicated it intends to assert the rest. The California case has been stayed in view of the ITC investigation.

Realtek's '218 Patent says its "invention discloses a power mesh arrangement method utilized in an integrated circuit having multiple power domains." EX1001, Abstract.

Realtek did not invent the patent's claimed dual power mesh arrangement, because IBM and Broadcom beat Realtek to it. The patent itself concedes "it is common practices [sic] to arrange multiple power domains in the chip circuitry." *Id*., 1:28-30. As shown below, the 2005 Jiang reference showed exactly this dual power domain configuration:



'218 Patent
Figs. 1, 5

Jiang Prior Art
Fig. 1(b)

Compare EX1001 at Figs. 1, 5 (excerpted, annotated, rotated) *with* EX1004 at Fig. 1(b) (annotated).

Broadcom's BCM1280 chip from 2006 (shown at right) also included multiple power domains and a power routing structure with global and partial local power meshes. EX1005, 490-93, Fig. 1.

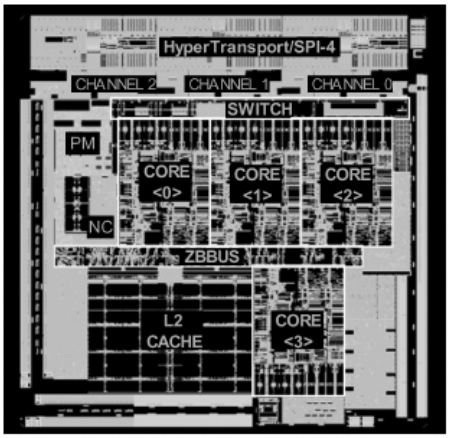


Fig. 1. Chip detailed floorplan.

The '218 Patent supposedly invented a power routing structure for a chip with multiple power domains that could be created using an automatic placement and routing (APR) tool. But IBM also got there first.

A decade before, IBM collaborated with Cadence Design Systems, makers of well-known APR tools, to publish a technique that "algorithmically generated" a multi-domain power distribution network. EX1013, 126. In similar research spanning the decade before the patent, Synopsis and ARM "recommend[ed] highly" and "wherever possible" using software tools to automatically create power routing structures for chips with multiple power domains. EX1012, 177. Indeed, well before the '218 Patent, even Patent Owner Realtek had created "multi-voltage designs with Synopsys' Galaxy™ design platform." EX1025.

The '218 Patent never should have issued. AMD respectfully requests cancellation of all claims.

II. STATEMENT OF PRECISE RELIEF REQUESTED FOR EACH CHALLENGED CLAIM

A. Claims & Statutory Grounds of Challenge (37 C.F.R. § 42.104(b)(1)-(2))

Petitioner requests review and cancellation of all claims 1-20. Claims 12-18 are currently asserted in the co-pending litigation, and Realtek indicated it seeks to assert the rest. As explained below, the Petition presents five grounds. Grounds 1-3 challenge all claims based primarily on the Jiang reference. Grounds 4-5 are based primarily on the Li reference.

Ground 1: Claims 12-18 are rendered obvious over Jiang in view of Jiang2 and Jiang3.

- Jiang (published at least as early as November 8, 2005) is prior art under § 102(b) (pre-AIA) because it is a printed publication that was published more than a year prior to November 15, 2007,[1] the earliest priority date claimed in the '218 Patent. EX1004; EX1021 ¶¶53-59; EX1001, [30].
- Jiang2 (published at least as early as November 18, 2005) is prior art under § 102(b) (pre-AIA) because it is a printed publication that was published more than a year before November 15, 2007. EX1007; EX1021 ¶¶67-73.
- Jiang3 (published at least as early as March 26, 2007) is prior art under § 102(a) (pre-AIA) because it is a printed publication that was published before November 15, 2007. EX1008; EX1021 ¶¶74-80.

Ground 2: Alternatively, claims 12-18 are rendered obvious over Jiang in view Jiang2 and Jiang3, and in further view of Li or Chiu.

- Li (published at least as early as April 1, 2006) is prior art under § 102(b) (pre-AIA) because it is a printed publication that was

[1] The '218 Patent claims priority to a November 15, 2007 Taiwanese application. EX1001, [30]. Petitioner reserves the right to challenge the '218's entitlement to this priority date should Patent Owner assert it.

published more than a year before November 15, 2007. EX1005; EX1021 ¶¶60-66.

- Chiu claims priority to a provisional application filed on September 28, 2007 and is prior art under § 102(e) (pre-AIA). EX1006, [60]; EX1011. Chiu's provisional application contains a largely identical disclosure to the utility application that issued as Chiu and is entitled to its earliest priority date. *Compare* EX1006 *with* EX1011.

Ground 3: Claims 1-11 and 19-20 are rendered obvious over any of the combinations in Grounds 1-2, in further view of Bertolet or the Low Power Methodology Manual (LPMM).

- Bertolet (published at least as early as April 1, 1997) is prior art under § 102(b) (pre-AIA) because it is a printed publication that was published more than a year before November 15, 2007. EX1013, 124; EX1021 ¶¶96-104.
- LPMM (published at least as early as June 4, 2007 or, alternatively, July 31, 2007) is prior art under § 102(a) (pre-AIA) because it is a printed publication that was published before November 15, 2007. EX1012; EX1027, 2; EX1021 ¶¶89-95.

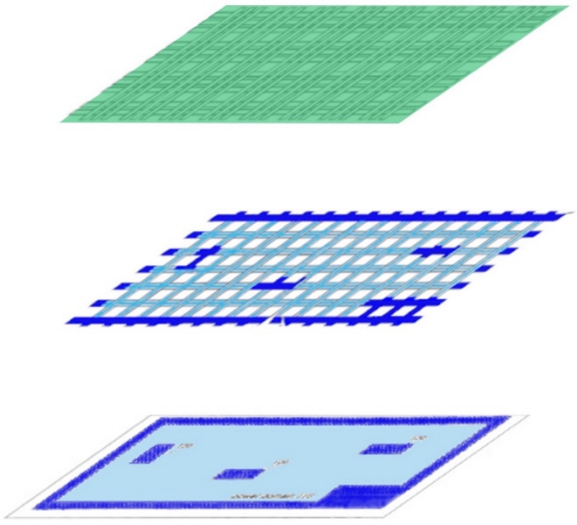
Ground 4: Claims 12-18 are rendered obvious over Li in view of Jiang.

Ground 5: Claims 1-11 and 19-20 are rendered obvious over Li in view of Jiang, Bertolet, and LPMM.

III. BACKGROUND

A. The '218 Patent

The '218 Patent describes "a power routing structure applicable to an integrated circuit having multiple power domains." EX1001, 2:4-6; *see also* EX1003 ¶¶39-45. As shown at right, the '218 Patent depicts and claims a circuit with two power domains (bottom layer) and two partial local power meshes (middle layer) based on the positions of those domains. EX1001, 1:51-58, Figs. 1, 5 (excerpted, annotated, rotated). "[A] global power mesh [(top layer)] [is] utilized for providing powers needed by" the two power domains. *Id.*, 1:57-58.

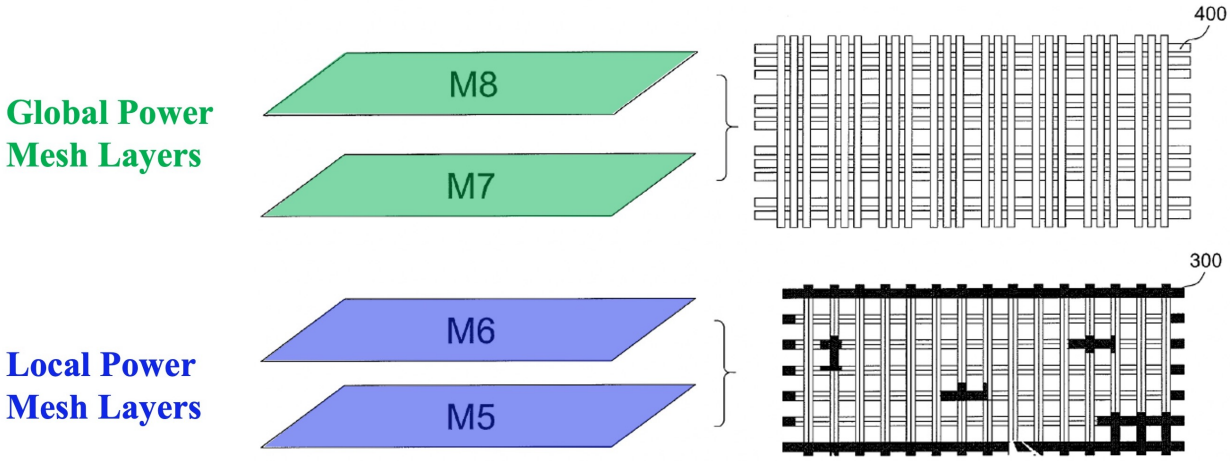


'218 Patent
Figs. 1, 5

Claims 12-18 recite a structure with a generic global power mesh and "first" and "second" partial local power meshes. The patent teaches that meshes are "web-like structures" that generally comprise "a plurality of horizontal power supply wires and a plurality of vertical power supply wires" on two metal layers. *Id.*, Figs. 3, 4, 3:44-51, 4:10-16, 4:21-25, 4:40-42. The "local power mesh … is evenly distributed"

and partitioned into two "partial local power meshes," each corresponding to a power domain. *Id*., 5:54-63.

The '218 Patent explains that a global-local power mesh arrangement requires at least four metal layers above the chip circuitry: two for the global power mesh, and two more for the partial local power meshes. *Id*., 4:53-58. Figure 5 shows the global power mesh that "suppl[ies] voltage to the entire chip" on metal layers 7 (horizontal wires) and 8 (vertical wires), and the partial local power meshes on metal layers 5 (horizontal wires) and 6 (vertical wires):



EX1001, Fig. 5 (annotated), 4:31-34, 4:64-5:7.

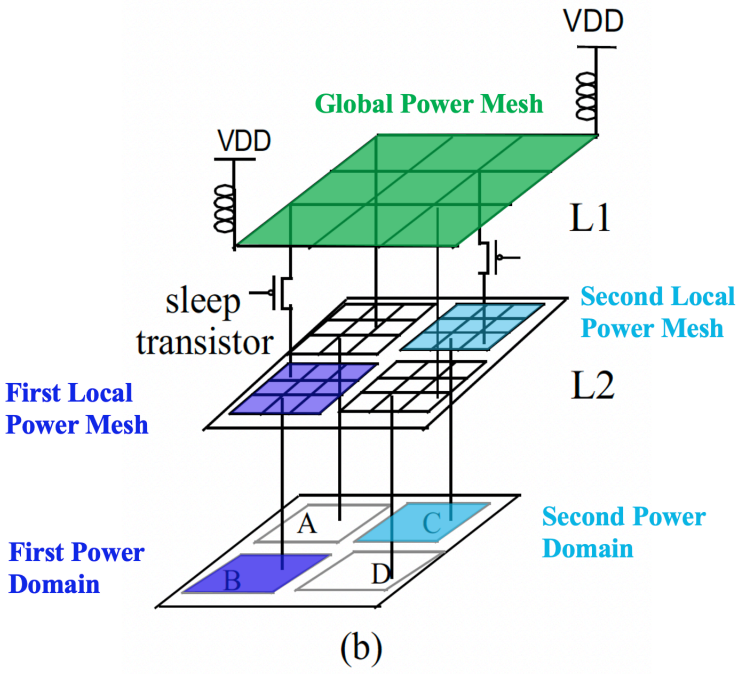
The remaining claims 1-11 and 19-20 recite a method for arranging that power structure with an "automatic placement and routing (APR) tool." *Id*., 6:59-64 (claim 1), 8:39-50 (claim 19). The patent acknowledges that APR tools were "well-known," but was under the misapprehension that the "(APR) tool can only support circuits having [sic] single power domain." *Id*., 1:36-39.

B. The Prior Art

None of the claimed features were new by the filing of the '218 Patent. Power routing structures for chips with multiple power domains, including global power meshes and partial local power meshes, and the use of APR tools to create such structures was well known to a POSITA. EX1003 ¶¶47-69.

1. Jiang (EX1004)

Jiang was a collaboration between researchers at IBM and University of California, Santa Barbara. EX1004, 1. Jiang describes a power-gated chip design with multiple power domains, corresponding "local power meshes," and a "global" power mesh:



EX1004, Fig. 1(b) (annotated), 1-2. It refers to the different power domains as "macros," with a "local power mesh[]" corresponding to each macro. *Id*., 1-2, Fig. 1(b). Above the "local power meshes" is a "global mesh" that is connected to an external power source (Vdd). *Id*. Jiang uses sleep transistors between some "local power meshes" and the "global mesh," allowing the "local power meshes" and their underlying power domains to be switched off. *Id*.

2. Jiang2 (EX1007) and Jiang3 (EX1008)

Jiang2 and Jiang3 further elaborate on Jiang's research on power distribution in power-gated chips. EX1007, 1; EX1008, 1. Jiang2 explains that a power-gated "chip is divided into several domains" and that "local power meshes are constructed for each" power domain. EX1008, 1; *see also* EX1007, 1. Jiang2 and Jiang3 also teach that "[e]ach domain is independently controlled by a sleep-transistor" and that these "sleep transistors are turned off to reduce the dynamic power and leakage power in a standby mode, and turned on in an active mode for normal operation." EX1007, 1; *see also* EX1008, 1 (similar).

3. Li (EX1005)

Li disclosed a Broadcom chip with a power routing system including a global power grid and multiple local power grids providing power to the power domains. EX1005, 491-93, Fig. 1.

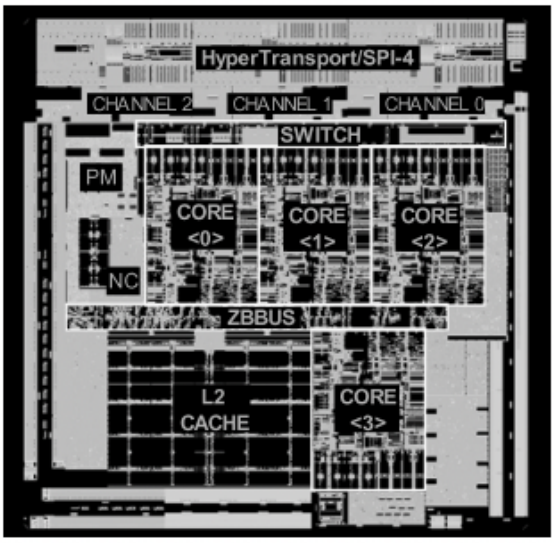


Fig. 1. Chip detailed floorplan.

Li explains that power routing structures were "designed to provide required voltages and currents to the transistors that perform the logic functions of a chip." *Id*., 492. Li's power routing structure supplied two different voltages, VDD_chip and VDD_switch, as well as Ground (GND). *Id*., 493. Li's power routing structure was built across numerous metal layers. This included a "top level" "power grid structure" with vertical power lines on one metal layer (metal-6) and horizontal power lines on another metal layer (metal-7), shown in Li's Figure 3, below. *Id*.

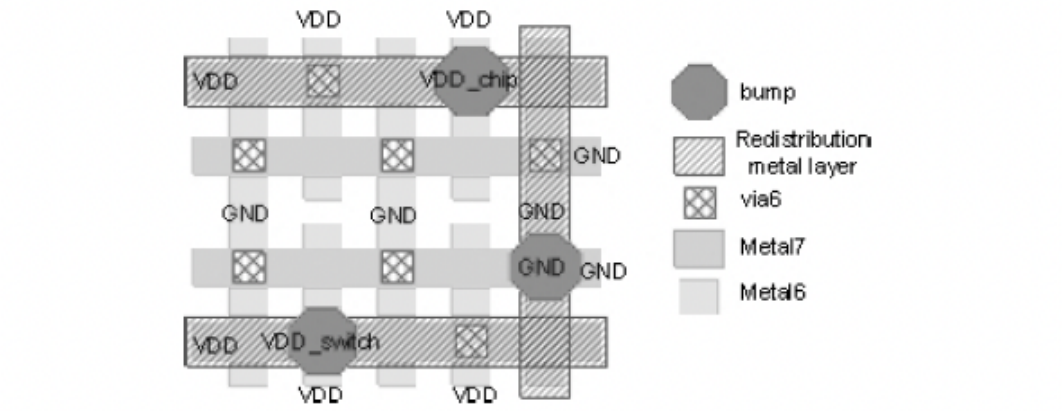


Fig. 3. Power and ground are distributed from the bumps onto the chip-level power grid through a redistribution metal layer.

Id., Fig. 3. Li's top-level power grid "distribut[es] power and ground across the chip." *Id.*, 493.

Li's multiple local grids included "power and ground lines in the local sections" routed on lower metal layers than the top-level grid (metal-2 through metal-5). *Id.*

Li also describes a tool for automatically completing the power routing structure in the Broadcom chip by "connecting local logic to the top-level power grid, to implement a complete full-chip power distribution network." *Id.*

4. Chiu (EX1006)

Chiu also discloses a power routing structure for an integrated circuit with multiple voltage (power) domains. EX1006, Abstract. Chiu's voltage domains receive separate voltage supplies but share a common ground supply.

In particular, Chiu describes a power "grid" on the "upper-most metal layers" of the chip comprising two "positive voltage supply grid[s]" (VDD1 and VDD2) and

one common ground, "negative voltage supply grid" (VSS). EX1006, 2:31-43, 2:50-61. This top-level grid is shown in Figure 7 below.

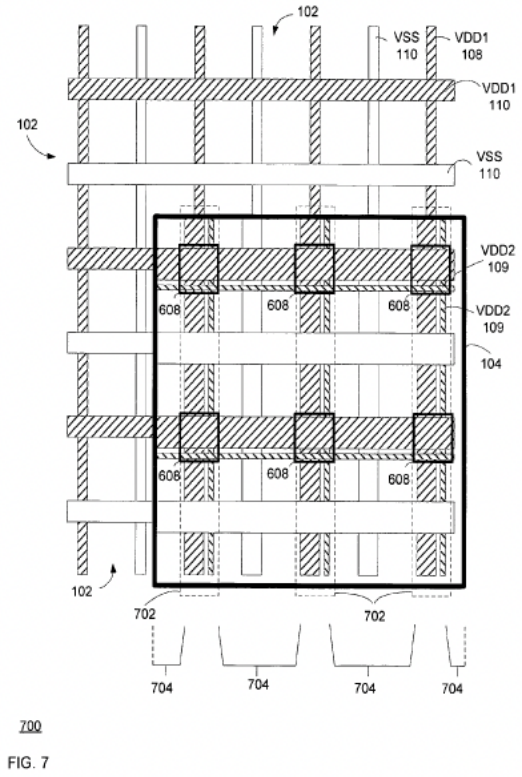


FIG. 7

Id., Fig. 7. Chiu's voltage supply VDD1 "powers the standard cells in the first and third voltage domains," while VDD2 powers the "cells in the second voltage domain." *Id*., 2:31-43. Chiu also discloses a ground supply "VSS" shown above. *Id*., 2:50-55; EX1003 ¶62. Chiu's separate voltages and common ground are supplied from this top-level grid to the power domains through multiple "power-ground rails (associated with the middle or lower layers of the integrated circuit) using a piece of metal called a via stack." EX1006, 2:55-61.

5. Bertolet (EX1013)

Bertolet, published 10 years before the '218 Patent's filing, discloses a "'pseudo-hierarchical' design approach … to manage the floorplan, placement, and routing optimization" of a power routing structure for an integrated circuit. EX1013, 124. Bertolet "algorithmically generated power distribution on five layers of metal" of an integrated circuit. *Id*., 125. In particular, Bertolet teaches a software tool that "algorithmically generated" a power distribution network. *Id*., 126. Bertolet's tool "provide[d] the capability to define multiple power terrains by area and level of metal." *Id.* Accordingly, two different areas of the chip could have "different power grids on metal levels three though five" but share the same global "common power grid on metal levels one and two." *Id*.

6. Low Power Methodology Manual (LPMM) (EX1012)

LPMM discusses the results of a decade-long collaborative research effort by ARM and Synopsys on integrated circuits and low power system architecture, including projects exploring multi-voltage circuits and power-gated routing structures. EX1012, xv-xvi.

LPMM discusses using power routing tools for the design of chips with multiple voltage domains. LPMM taught that most electronic design automation (EDA) "tools provide some level of automated power network synthesis (PNS) capability for the distribution of power across a design." *Id*., 177. LPMM further

"recommend[ed] highly" use of these tools for automated power network synthesis of a multi-voltage design. *Id*.; *see also id*., 178 ("sleep transistor power network can be synthesized using a power planning tool"). Indeed, LPMM warned that "[t]he number of concurrently changeable variables in a multi-voltage system is such that attempting to construct a power plan manually may result in a suboptimal result." *Id*., 177.

7. Analogous Art

Each of the above prior art references are analogous art to the claimed invention. EX1003 ¶70. Each is in the same field of endeavor as the '218 Patent because it is directed to power routing structures in integrated circuits, including those with multiple power domains. *Compare* EX1001, 1:8-11 *with* EX1004, 1-2; EX1005, 490-94; EX1006, Abstract, 1:42-2:61; EX1007, 1-2; EX1008, 1-2, 4-5; EX1012, 99, 177-78, 271; EX1013, 124-26. Additionally, each is reasonably pertinent to the problem addressed in the '218 Patent, providing a power routing structure with an automatic placement and routing tool. *Id*.; EX1003 ¶70.

C. Prosecution History of '218 Patent

The '218 Patent was filed on November 14, 2008. EX1001, 1. The examiner rejected the original claims as anticipated by U.S. Patent No. 7,000,214 ("Iadanza") or obvious over the combination of Iadanza and U.S. Patent No. 7,234,124 ("Chen"), and further rejected the methods in claims 1 and 19 as patent ineligible subject matter

for "claim[ing] an abstract idea" and "recit[ing] purely mental steps." EX1002, 104-15. Applicant conceded these rejections, amending the claims to require the global power mesh to include a plurality of horizontal power supply wires on one metal layer and a plurality of vertical power supply wires on a different metal layer, and amending the method claims 1 and 19 to add the use of an APR tool. *Id*., 131-40. The examiner allowed the amended claims. *Id*., 144-46. None of the prior art presented in this petition was considered during prosecution.

D. Claim Construction (37 C.F.R. § 42.104(b)(3))

In accordance with 37 C.F.R. § 42.100(b), each claim must be "construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b)."

Petitioner submits that no claim construction is necessary to find the claims unpatentable in view of the grounds in this Petition. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999). In the parallel ITC proceeding, both parties have submitted proposed constructions. EX1029; EX1030. Patent Owner proposes that "local power mesh" refers back to "partial local power mesh." EX1029, 1-2. Petitioner will accept Patent Owner's contention for purposes of this IPR. Otherwise, the Board need not adopt Petitioner's proposed constructions

for Petitioner to prevail. Thus, Petitioner proposes that the claim terms should be given their plain and ordinary meaning.[2]

IV. LEVEL OF SKILL AND KNOWLEDGE OF POSITA

A POSITA as of November 14, 2008, or November 15, 2007, would have had a bachelor's degree in computer science, electrical engineering, computer engineering, or a related field, and approximately two years of experience in the design, development, and/or testing of power distribution networks related to integrated circuits with multiple power domains, or the equivalent, with additional education and/or research substituting for experience and vice versa. EX1003 ¶¶33-38; *Chore-Time Equip., Inc. v. Cumberland Corp.*, 713 F.2d 774, 779 (Fed. Cir. 1983).

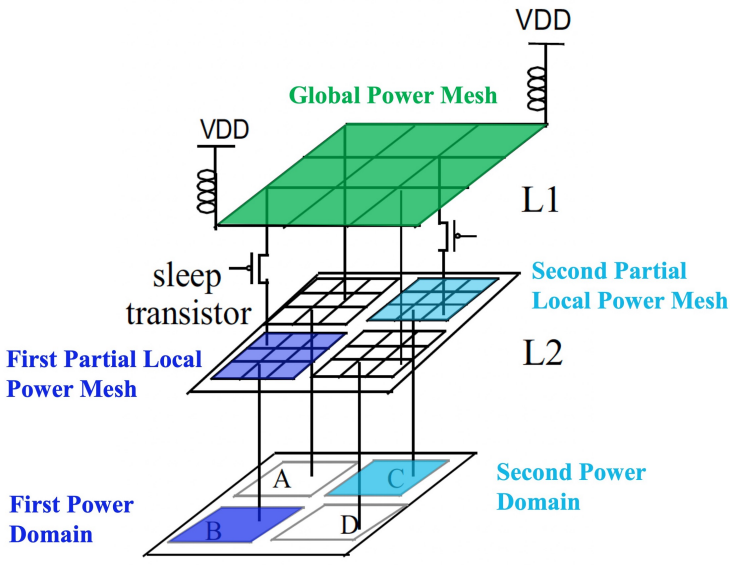
[2] Petitioner may propose constructions in this proceeding in response to Patent Owner's arguments.

V. REASONS FOR RELIEF REQUESTED UNDER 37 C.F.R. §§ 42.22(A)(2) AND 42.104(B)(4)

A. Grounds 1-2 – Claims 12-18 are obvious over Jiang in view of Jiang2 and Jiang3 (Ground 1), optionally in further view of Li or Chiu (Ground 2)

1. Claim 12[preamble]: "A power routing structure applied in an integrated circuit having multiple power domains, comprising:"

To the extent limiting, Jiang discloses the preamble. Jiang discloses a power routing structure for a power-gated integrated circuit with multiple macros, with partial local power meshes for each macro and a global power mesh above the partial local power meshes. EX1004, 1 ("In the power-gated chip, we have local power meshes for all macros, and sleep transistors are used to connect the local mesh to the global mesh."); *see also id.* (discussing "VLSI circuits"). This power routing structure is shown in Figure 1(b), below:



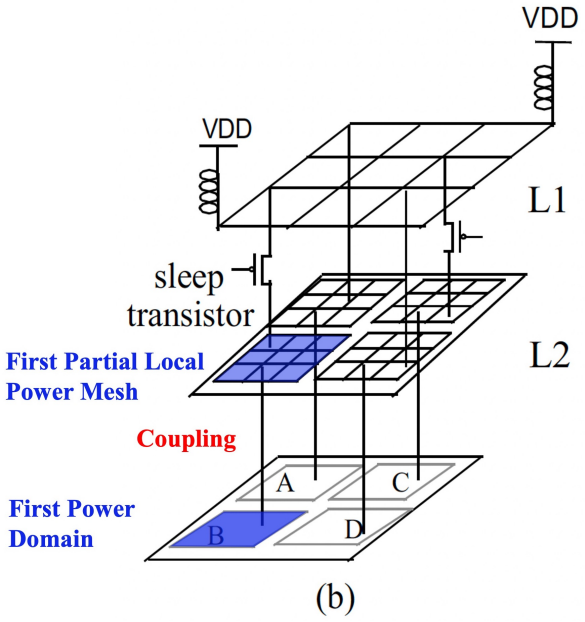
(b)

Id., Fig. 1(b) (annotated). Each of Jiang's "macros" is a power domain. *See, e.g.*, *id.*, 2 ("When a macro is active, the sleep transistor is turned on. Its size must be large enough to guarantee that the current drawn by the macro does not cause excessive voltage drop."); EX1003 ¶¶71-73. As Jiang2 explains, "[i]n a power-gating system, a circuit is divided into several power domains." EX1007, 1; *see also* EX1008, 1, 5 (referring to power domains as "macros").

Because Jiang, Jiang2, and Jiang3 address the design of power-gated integrated circuits with multiple power domains as discussed above in Section III.B.1-2 and because Jiang2 and Jiang3 specifically reference Jiang, a POSITA working on power routing for power-gated chips would readily look to Jiang2 and Jiang3 to understand the terminology in Jiang. EX1003 ¶73.

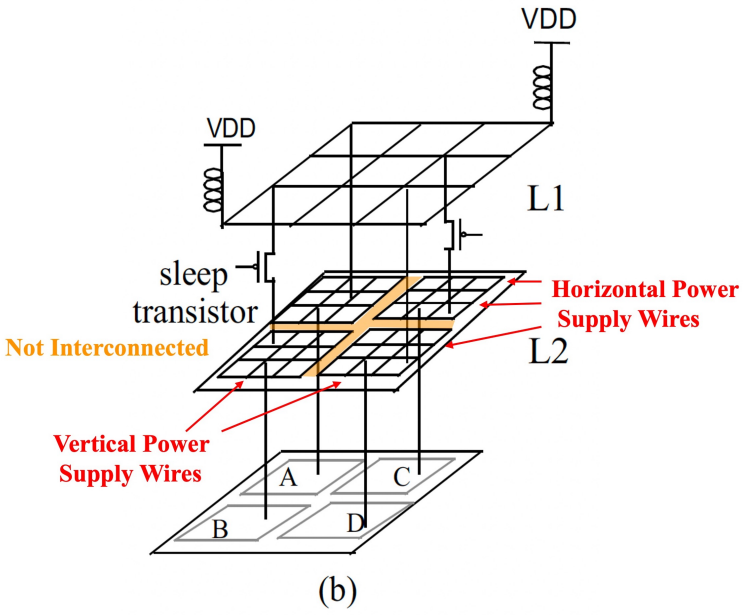
2. Claim 12[a]: "a first partial local power mesh having its position corresponding to the position of a first power domain and coupling to the first power domain;"

Jiang discloses this limitation. Jiang discloses that each macro (power domain) has its own partial local power mesh. EX1004, 1 ("In the power-gated chip, we have local power meshes for all macros ….). Jiang discloses that macro B (first power domain) is coupled to and corresponds in position with its first partial local power mesh, as shown in Jiang's Figure 1(b), below.



EX1004, Fig. 1(b) (annotated); *see also id.*, 1 (explaining that "sleep transistors are used to connect the local mesh to the global mesh" and "connect the gated blocks to the power supply"); EX1003 ¶74.

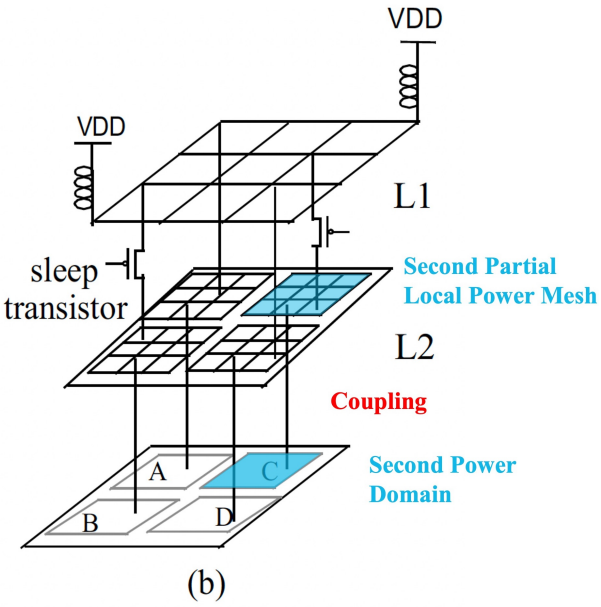
Jiang's "local power meshes" are "partial local power meshes." EX1003 ¶75. The '218 Patent describes the "partial local power meshes" as "web-like structures," which are "not interconnected," that "comprise[] a plurality of horizontal power supply wires and a plurality of vertical power supply wires" that are "only used to supply the powers needed" by their particular power domain. EX1001, 3:44-56. As seen in Figure 1(b), Jiang's "local power meshes" meet all these criteria.



EX1004, Fig. 1(b) (annotated), 1-2; EX1003 ¶¶75-76; *see also* EX1008, 1.

3. Claim 12[b]: "a second partial local power mesh having its position corresponding to the position of a second power domain and coupling to the second power domain; and"

Jiang discloses this limitation for the same reasons discussed above regarding limitation 12[a]. EX1004, 1; *see* §V.A.2, *supra*. Jiang's macro C (second power domain) is coupled to and corresponds in position with its second partial local power mesh, as shown in Jiang's Figure 1(b), below.

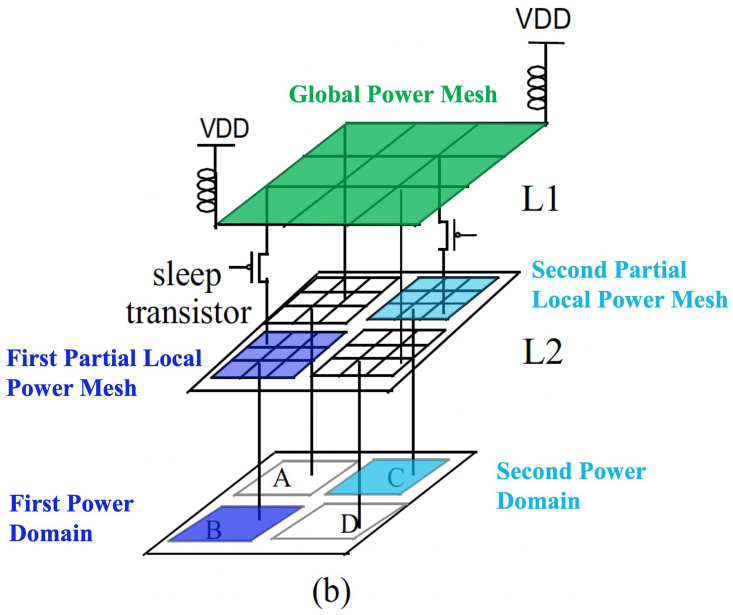


EX1004, Fig. 1(b) (annotated); EX1003 ¶77.

4. Claim 12[c]: "a global power mesh, coupling to the first local power mesh and the second local power mesh, to provide the power needed by the first power domain and the second domain separately;"

Jiang discloses this limitation.[3] Jiang discloses a "global mesh" that is coupled to the first and second partial local power meshes via the sleep transistors as shown in Figure 1(b) below. EX1004, 1 ("[S]leep transistors are used to connect the local mesh to the global mesh.").

[3] For purposes of this proceeding only, Petitioner will use Patent Owner's ITC position that the first and second "local power mesh[es]" refer to the first and second "partial local power mesh[es]," respectively. EX1029, 1.



EX1004, Fig. 1(b) (annotated); EX1003 ¶¶78-79.

Jiang discloses that the global power mesh provides the power (Vdd) needed by the first and second power domains. Jiang teaches that "[i]n the power-gated chip, we have local power meshes for all macros, and sleep transistors are used to connect the local mesh to the global mesh." EX1004, 1. Thus, Jiang discloses connecting global mesh power Vdd to the gated macros (power domains) through the sleep transistors and local meshes as depicted in Figure 1(b) above. *Id.*; EX1003 ¶80; *see also, e.g.*, EX1004, 6 (measuring voltage Vdd provided to the power domains).

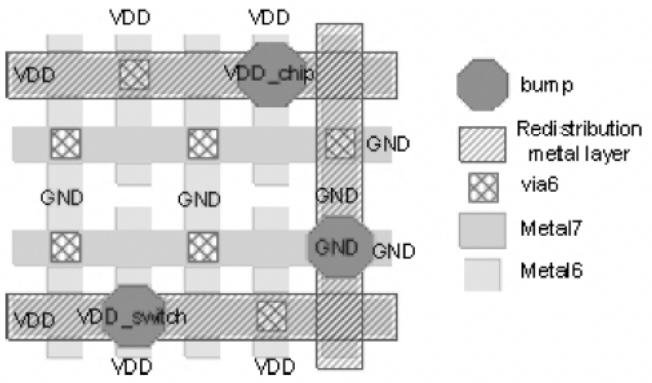
By gating the first and second partial local power meshes (and power domains) with sleep transistors, Jiang is able to power each domain "separately" by switching its respective sleep transistor. *See* EX1004, Abstract ("Power-gating is a

technique for saving leakage power by shutting off the idle blocks."); *see also id*., 1 (same), 2 (discussing "sleep transistors" being "turned on and off"); EX1003 ¶81.

Moreover, to the extent it is not disclosed, it would have been obvious for Jiang's sleep transistors to be independently operable. A POSITA would have known that a "strategy in which each power domain has an independent power gating structure is an effective means for reducing leakage power consumption in a system-on-a-chip." EX1009, 1 (abstract); *see also* EX1010, 1:37-43. Jiang2 teaches that "[i]n a power-gating system, a circuit is divided into several power domains" where "[e]ach domain is ***independently controlled*** by a sleep-transistor." EX1007, 1 (emphasis added). Similarly, Jiang3 teaches that it is "assume[d] that when power-gating is applied, the gated-blocks are ***individually power supplied***." EX1008, 4 (emphasis added). It would have been obvious for Jiang's sleep transistors to be independently operable as expressly disclosed in either Jiang2 or Jiang3.

Doing so would provide more granular control and help reduce power consumption. EX1003 ¶¶82-83 (citing EX1009, 1; EX1010, 1:37-43). Allowing each of Jiang's sleep transistors, and their respective partial local power meshes and power domains, to be switched independently would have been routine application of a known—indeed the "assume[d]"—functionality of the sleep transistors in Jiang with a reasonable expectation of success given its ubiquitous usage. EX1003 ¶¶84-85 (citing EX1008, 4).

Although not required by the claim, it also would have been obvious for Jiang's global power mesh to supply independent voltages to the first and second power domains. EX1003 ¶¶86-93. The '218 Patent concedes it was "common practice[] to arrange multiple power domains" in a chip where "different power domains are coupled to different powers." EX1001, 1:28-31; *see also* EX1012, 157 (Fig. 11-2). For example, Li discloses an integrated circuit with multiple power domains and global and partial local power meshes. EX1005, 493. Li's global power mesh comprises horizontal and vertical wires carrying independent supply voltages (VDD_chip and VDD_switch) and ground (GND) as illustrated in Figure 3 below. *Id*., 493-94.



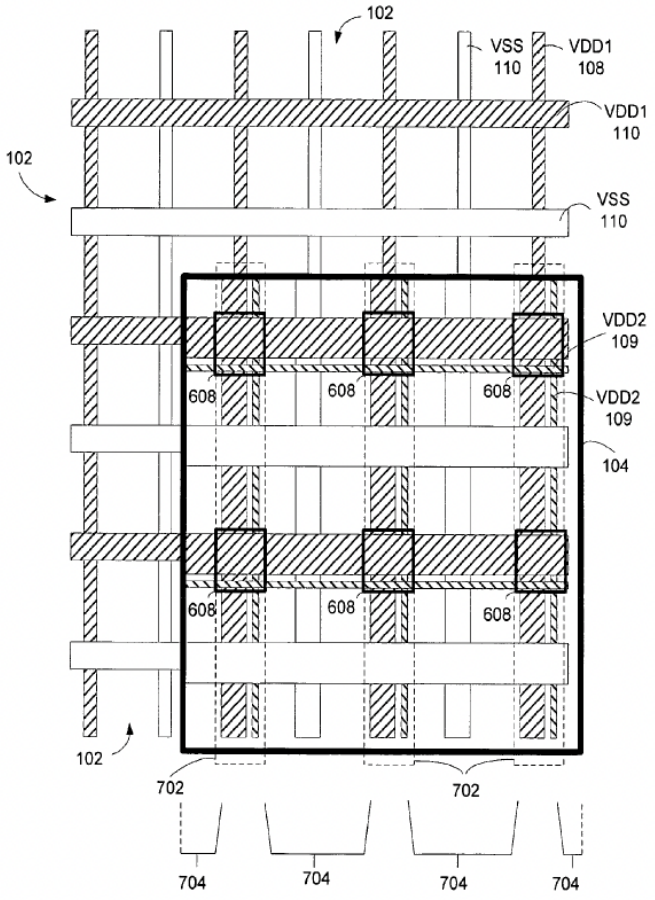
Id., Fig. 3.

Li's global power mesh supplies its separate voltages to the power domains via partial local power meshes. EX1005, 493 ("Metal-6 and metal-7 are extensively used in distributing power and ground across the chip. … This forms the power grid structure at the chip top level. The power and ground lines in the local sections are

grided on Metal-2 through Metal-5, on which the local power grids are formed at the block level."); *id*., 495 ("[T]here are two power supply inputs VDD_chip and VDD_switch at the package level in this design."); EX1003 ¶88.

Li explains that "[a]ll four CPU cores operate at the same supply voltage, VDD_chip …." EX1005, 495. But "VDD_switch provides power for all the internal logic of the node controller (NC), packet manager (PM), switch and HT/SPI-4 ports." *Id.*; *see also id.*, 493 ("As a result of function and logic requirements, there are multiple voltage regions across the chip."), 491 ("[T]he chip is divided into two logic voltage regions (1.1V)."), 492 (Table I: "Supply Voltages 1.1V, 2.5V and 3.3V"); EX1003 ¶88.

Similarly, Chiu discloses a chip with multiple voltage domains where a global power mesh supplies separate voltages (VDD1 and VDD2) to different domains as shown in Chiu's Figure 7, below.



EX1006, Fig. 7; *see also id*., 1:54-60, 2:55-61; EX1003 ¶89.

A POSITA would thus know to use multiple independent supply voltages in a global power mesh to supply separate partial local power meshes separately. EX1003 ¶¶85-90.

A POSITA would be motivated to supply independent voltages to Jiang's power meshes to supply its different power domains with different voltages to increase Jiang's power savings. EX1003 ¶¶90-93. Jiang uses the multiple power domains to reduce leakage current and save power. *E.g.*, EX1004, 1 (Jiang's power mesh "achieve[d] 47% leakage power saving while maintaining the same

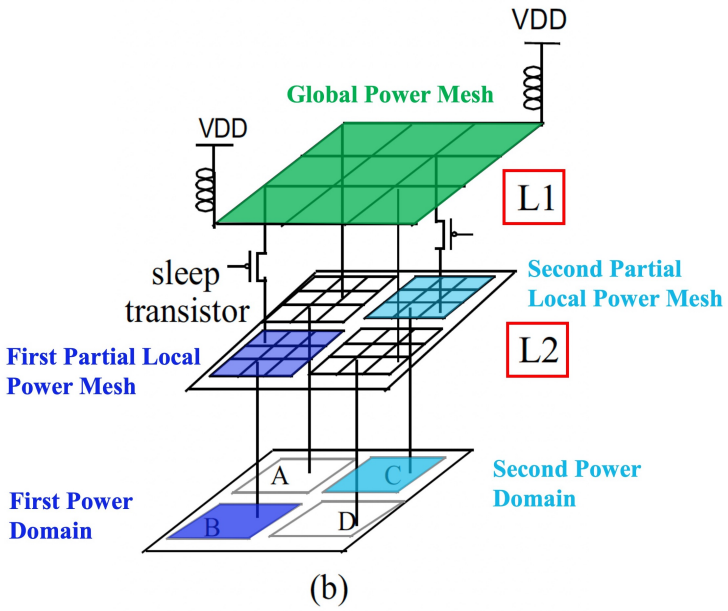
performance"); *id*. ("Power-gating is a technique for reducing leakage power by shutting off idle blocks."). Also, Li's power domains using separate voltages were optimized to save power. EX1005, 493 ("This design style enables power-saving capability with a selectable configuration, allowing the chip to be an optimal fit into a broad variety of applications."). Indeed, the '218 Patent admits that supplying "different powers… to the different circuits inside the chip" was conventional. EX1001, 1:26-28; *see also id.*, 1:30-33.

A POSITA would have known that using separate power supplies to supply higher voltages to portions of a chip, such as timing-critical blocks or input-output circuits, while supplying lower voltage to the rest would further save power. EX1003 ¶¶91-92 (citing EX1014, 3; EX1012, 16-17, 177-78; EX1010, 6:19-31 (discussing beneficial use of separate power supplies for power save mode)).

Applying independent supply voltages to Jiang's global power mesh would have been a routine application of a known feature to Jiang's device with a reasonable expectation of success, given that it was "common practice[]" as the '218 Patent admits. EX1003 ¶93 (citing EX1001, 1:26-33).

5. Claim 12[d]: "wherein the first partial local power mesh and the second partial local power mesh are positioned on the same metal layer while the global power mesh and the first local power mesh are positioned on different metal layers;"

Jiang discloses this limitation. Jiang discloses that the partial local power meshes are on the same metal layers ("L2"), while the global power mesh is on different metal layers ("L1"), as shown in Jiang's Figure 1(b) below.

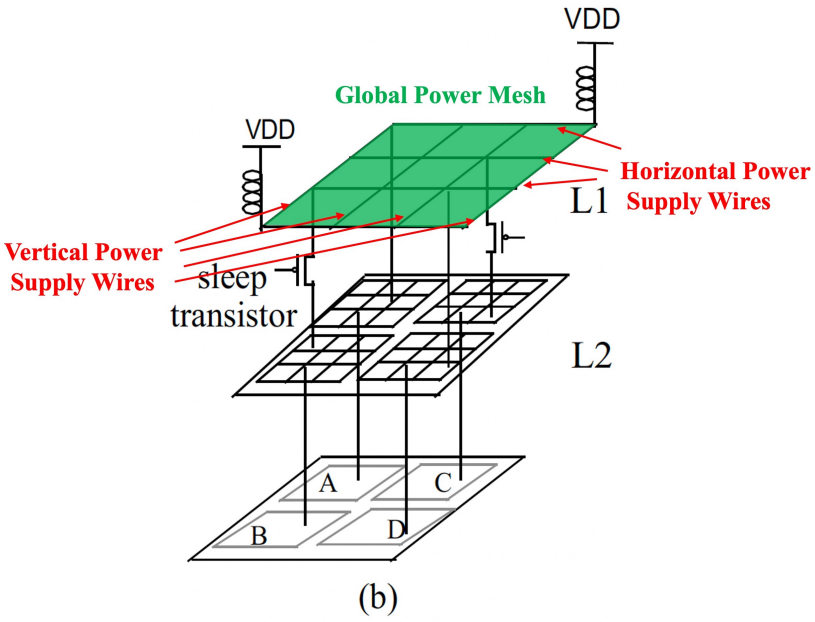


EX1004, Fig. 1(b) (annotated), 2 (referring to global mesh as "upper" and local meshes as "lower"); EX1003 ¶94.

As discussed below regarding limitation 12[e], a POSITA would understand Jiang to disclose, or at least render obvious, for global and partial local power mesh layers ("L1" and "L2") to each comprise at least two separate metal layers to separate horizontal and vertical power supply wires on different layers as shown in Figure 10. EX1003 ¶94.

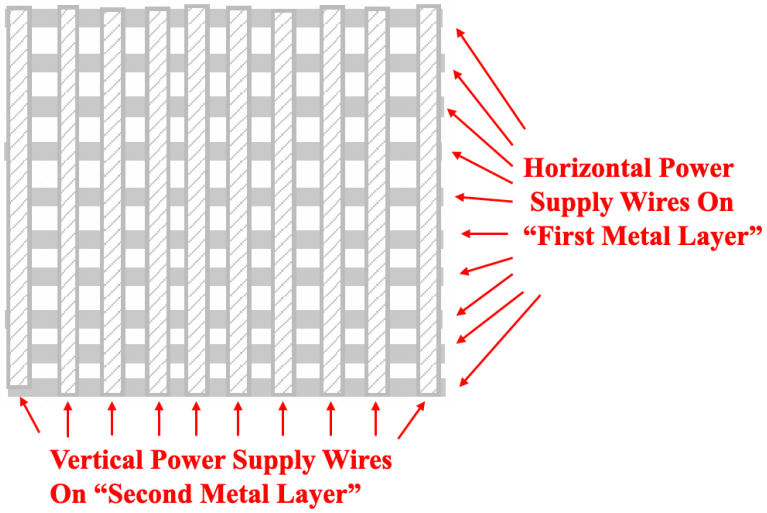
6. Claim 12[e]: "wherein the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer; and"

Jiang discloses this limitation. Jiang discloses that its global power mesh includes a plurality of horizontal and vertical power supply wires.

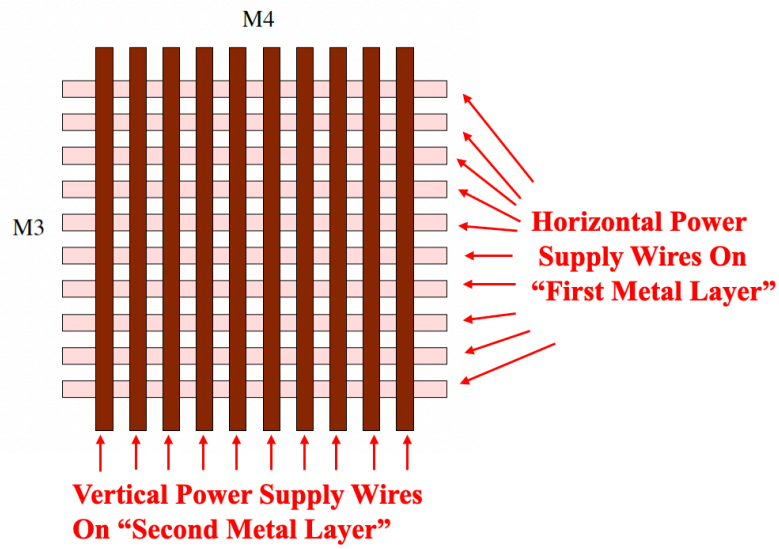


EX1004, Fig. 1(b) (annotated); *see also id.*, 7 (discussing the "horizontal and vertical segments" of the "power mesh"); EX1003 ¶95.

A POSITA would understand that the horizontal and vertical wires in the global power mesh would be on different layers ("a first metal layer" and "a second metal layer"). EX1003 ¶96. Indeed, Figure 10 shows Jiang's power meshes with the horizontal wires on one layer ("a first metal layer") and the vertical wires on a higher metal layer ("a second metal layer").



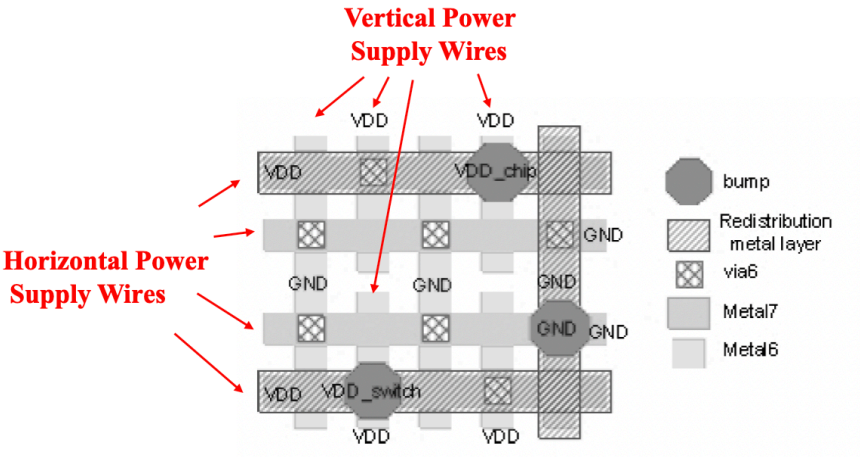
EX1004, Fig. 10 (excerpted, annotated). Jiang's Figure 10 shows that the vertical and horizontal wires are on different metal layers. EX1003 ¶96 (citing EX1005, Fig. 3; EX1006, Fig. 7). Indeed, one of Jiang's co-authors similarly depicted a power mesh with horizontal and vertical wires on different metal layers ("M3" and "M4," respectively), as shown below.



EX1015, Fig. 3(a) (shading in original; red annotations added); *see also id.*, 26.

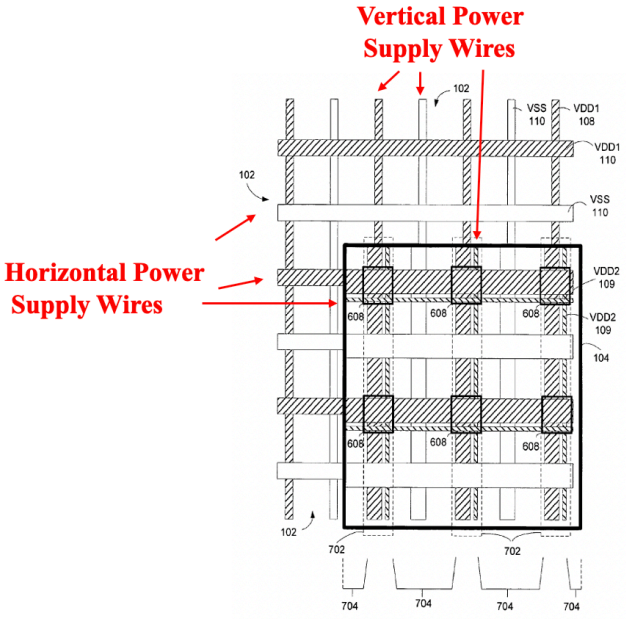
Alternatively, it would have been obvious to design Jiang's global power mesh with horizontal and vertical power supply wires on separate metal layers. It was well-known to route horizontal and vertical wires of a mesh on different layers as described above in Li and Chiu. *See* §V.A.4; EX1003 ¶97.

Both Li's and Chiu's global power meshes comprise horizontal and vertical wires routed on two different layers.



EX1005, Fig. 3 (annotated); *see also id.*, 493 ("Ground (GND) and power (VDD_chip, VDD_switch) lines are routed alternately on Metal-6 in the vertical direction and Metal-7 in the horizontal direction."); EX1003 ¶98.

Similarly, Chiu teaches a global power mesh with horizontal wires on a first metal layer and vertical wires on a second, lower, metal layer, as shown below in Figure 7.



EX1006, Fig. 7 (annotated); *see also id.*, 5:15-18 ("[T]he substantially horizontal members are typically located in a higher metal layer than the corresponding substantially vertical members of the power supply grids."); EX1003 ¶99.

As Dr. Subramanian explains, this concept "was a well-known basic feature of integrated circuit design." EX1003 ¶100 (citing EX1016, 8:57-59 ("Typically, a routing grid is a meshing of horizontal and vertical metal rails on two metallization layers, which covers the core of the circuit."); EX1018, Fig. 9, 9:17-23 (describing an "upper power grid" on two metal layers with vertical power rails on one layer and horizontal power rails on an adjacent metal layer)).

As discussed above in limitation 12[c], a POSITA would be motivated to apply the global power mesh teachings of Li or Chiu to Jiang to provide independent voltage supplies to Jiang's different power domains. *See* §V.A.4. A POSITA would

further understand that routing horizontal and vertical power wires on different metal layers, as shown in Li and Chiu, would be necessary to prevent the global power mesh from shorting. EX1003 ¶101.

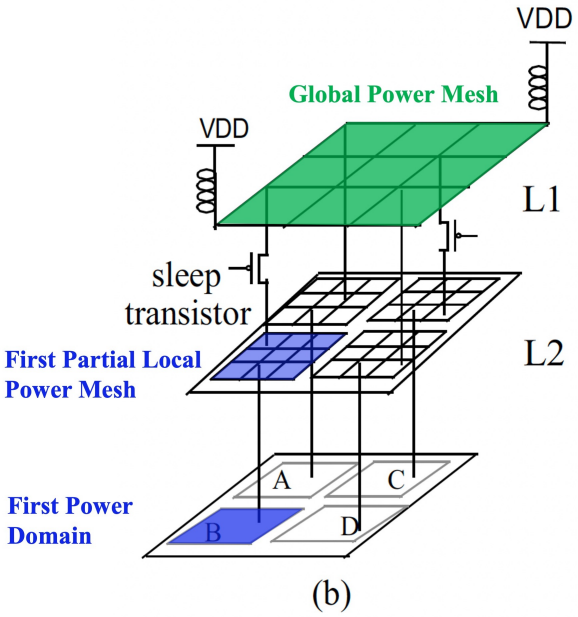
Finally, to the extent not disclosed in Jiang, routing power grid wires horizontally and vertically on alternating metal layers would have been routine application of a known—indeed the "normal"—routing structure with a reasonable expectation of success especially given its ubiquitous usage. EX1003 ¶102.

7. Claim 12[f]: "wherein the first metal layer and the second metal layer are different layers."

As discussed in 12[e], Jiang discloses that its horizontal and vertical power wires are on different layers (a first metal layer, and a different, second metal layer). Alternatively, it would have been obvious to use different first and second metal layers for all the reasons explained regarding limitation 12[e]. EX1003 ¶103; *see* §V.A.6, *supra*.

8. Claim 13: "The power routing structure according to claim 12, wherein the global power mesh is positioned above the first local power mesh."

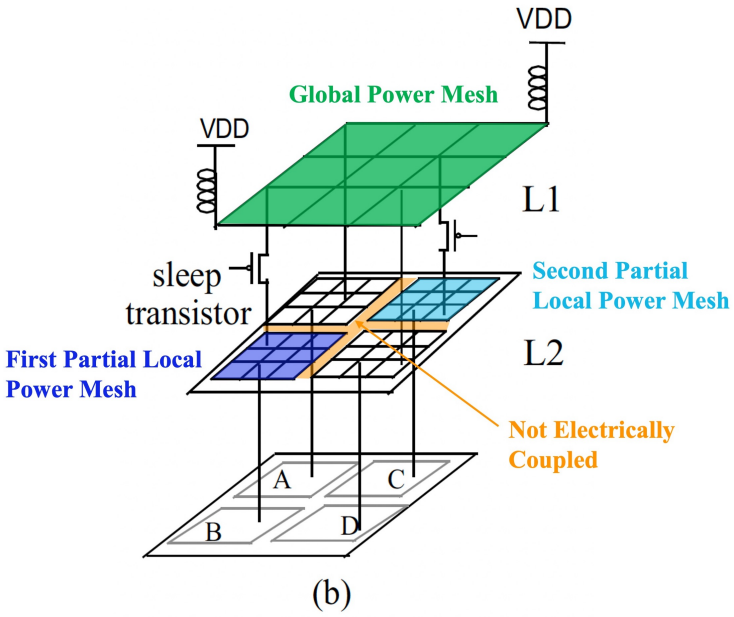
Jiang discloses this limitation. Jiang discloses a global power mesh positioned above a first partial local power mesh and above all power domains, as shown in Figure 1(b), below.



EX1004, Fig. 1(b) (annotated), 2 (referring to global mesh as "upper" and local meshes as "lower"); EX1003 ¶104.

9. Claim 14: "The power routing structure according to claim 13, wherein the first local power mesh and the second local power mesh are not electrically coupled."

Jiang discloses this limitation. Jiang's Figure 1(b) shows no wire on L2 connecting the first and second partial local power meshes.



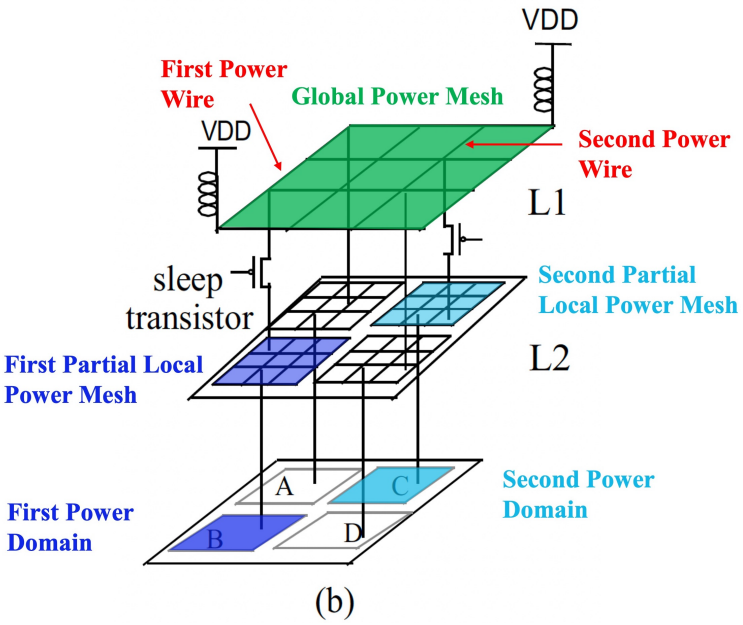
EX1004, Fig. 1(b) (annotated); EX1003 ¶105.

Alternatively, as explained in 12[c], Jiang's sleep transistors can disconnect the partial local power mesh from the global power mesh. EX1004, Abstract, 1, 2. Accordingly, when either sleep transistor is off, the first and second partial local power meshes would not be electrically coupled. EX1003 ¶106.

Finally, although not required by the claim, it would have been obvious to combine Jiang with either Li's or Chiu's multi-voltage layout so that Jiang's first and second partial local power meshes received separate supply voltages from different wires in the global power mesh, as explained above regarding 12[c]. In this scenario, the global power mesh would still be above the first partial local power mesh because that is Jiang's structure as well as Li's and Chiu's. EX1003 ¶107 (citing EX1005, 493; EX1006, 2:55-61).

10. Claim 15: "The power routing structure according to claim 12, wherein the global power mesh comprises: at least one ground wire; at least one first power wire that provides the power needed by the first power domain; and at least one second power wire that provides the power needed by the second power domain."

This limitation is obvious over Jiang optionally in view of Li or Chiu. Jiang's global power mesh includes horizontal and vertical power wires. EX1004, Fig. 1(b); *see also id.*, 7. Jiang's global power mesh also comprises at least one first power wire that provides power needed by the first power domain and at least one second power wire that provides power needed by the second power domain.



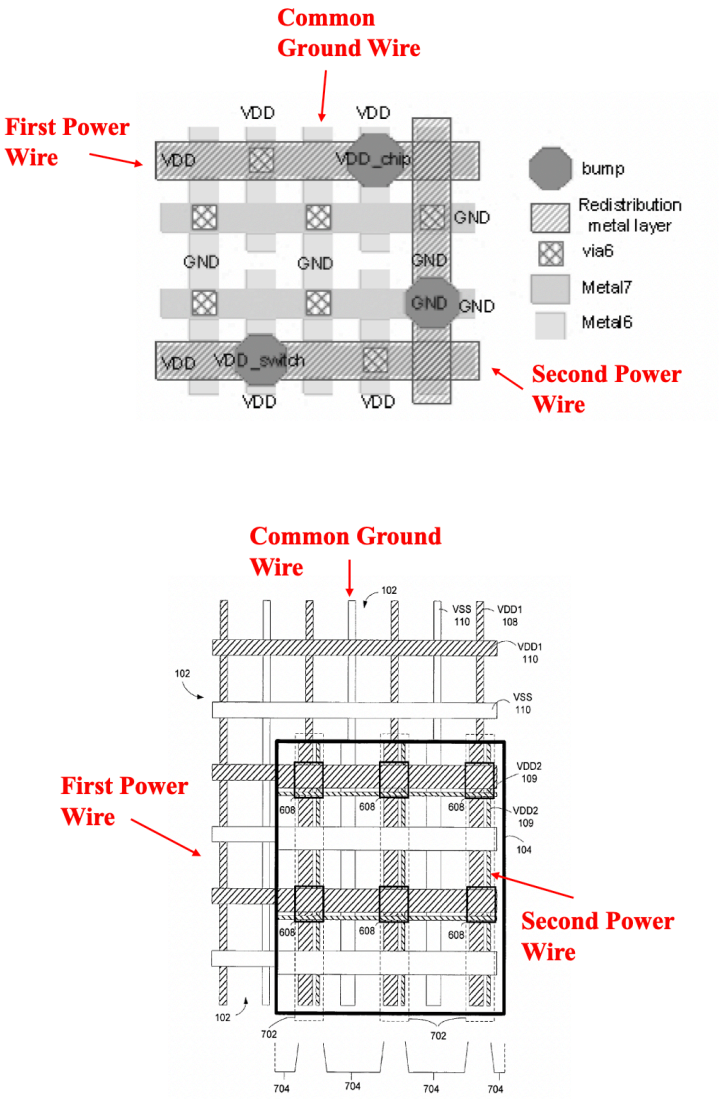
EX1004, 1-2, Fig. 1(b) (annotated); EX1003 ¶108.

To the extent not inherent, it would have been obvious to also provide at least one ground wire as part of Jiang's global power mesh. Circuits, including Jiang's power domains, require a ground connection. EX1003 ¶109 (citing EX1012, 271

("A power domain is functional only if the primary power and ground supply nets are specified."); EX1001, 3:59-60 (discussing "the ground potential … needed by the power domain")). It was known to provide that ground through a global power mesh, as demonstrated in Li and Chiu. EX1005, 493-94, Fig. 3; EX1006, 2:50-61 ("Implicit in the above discussion is the need and use of a negative voltage supply grid" such as "voltage supply grid VSS 110" which is a ground connection), Fig. 7; *see also* EX1018, 9:17-23. A POSITA would have been motivated to provide the ground connection as part of the global power mesh because a ground is necessary for the circuit to function, and routing the ground through the global power mesh was a routine practice for efficient use of metal layers with a known and understood expectation of success. EX1003 ¶109.

Alternatively, although not required by the claim, it would have been obvious to power Jiang's two power domains by two power wires that are not electrically coupled as disclosed in Li or Chiu and as explained above in 12[e]. As discussed, it would have been obvious to apply the teachings regarding Li's or Chiu's global power mesh to Jiang to supply separate voltages to Jiang's different domains. Li and Chiu each disclose a plurality of power wires and a common ground wire. A POSITA would understand that in the scenario where the first and second power domains required separate voltages, one power wire from one voltage supply would

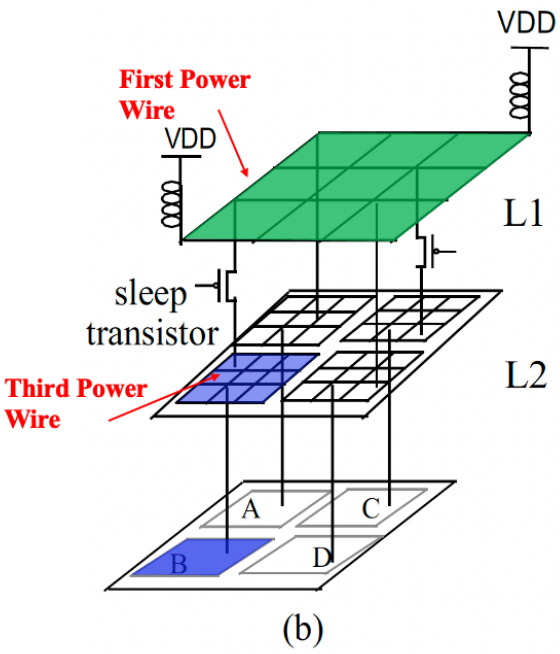
supply the first domain, and another power wire from the other voltage supply would supply the second domain, as shown below and as discussed in 12[c] and 12[e].



EX1005, Fig. 3 (annotated); EX1006, Fig. 7 (annotated); EX1003 ¶¶110-11.

11. Claim 16: "The power routing structure according to claim 15, wherein the first partial local power mesh comprises: at least one first local ground wire that couples to the ground wire of the global power mesh; and at least one third power wire that couples to the first power wire and the first power domain."

Jiang discloses at least one third power wire that couples to the first power wire and the first power domain, as illustrated in Jiang's Figure 1(b).



EX1004, Fig. 1(b) (annotated). When the switch is closed, Jiang's third power wire couples to both the first power wire and the first power domain as shown in the figure. EX1003 ¶112.

While Jiang does not explicitly disclose a ground wire, to the extent not inherent, it would have been obvious for a POSITA to include a ground. As discussed above regarding claim 15, it would have been obvious to also provide at least one ground wire as part of Jiang's global power mesh to provide the ground

needed by Jiang's power domains. EX1003 ¶113. A POSITA would have further found it obvious to include at least one first local ground wire in Jiang's first partial local power mesh to supply the ground needed by the first power domain. The ground wire would necessarily couple to the ground of the global power mesh, such as in Li or Chiu, as discussed in claim 15 and thus to all ground wires in the global power mesh.

Indeed, it was known that partial local power meshes could include local ground wires. For example, Li teaches a power routing structure with "ground lines in the local sections" of its power grid. EX1005, 493. A POSITA would have been motivated to include at least one first local ground wire in Jiang's first partial local power mesh to connect the global ground wire to Jiang's first power domain. EX1003 ¶¶114-15. Additionally, a POSITA would have had a reasonable expectation of success in adding this ground wire because supplying ground wires via global and partial local power meshes was a known technique as discussed above.

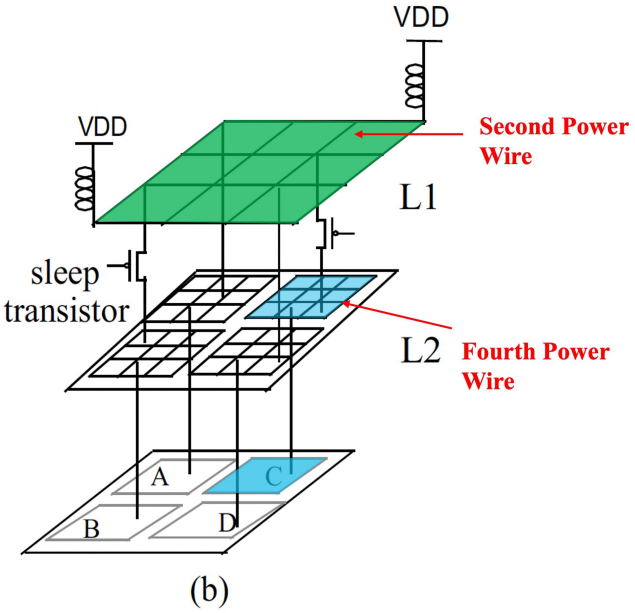
A POSITA would further understand that these ground and power wires in the partial local power mesh would have to be coupled to the first power domain to provide ground and power to the first power domain. Jiang shows the power connection from the first partial local power mesh to the first power domain. A POSITA would have known that a corresponding ground connection would also be

present if the ground is supplied through the global and partial local power meshes as discussed above. Adding a ground wire to Jiang's first partial local power mesh would have been routine application of a known functionality of a power-ground distribution network with a reasonable expectation of success especially given its common usage. EX1003 ¶115.

Alternatively, this limitation would have been obvious in view of the separate supply voltages of Li or Chiu for all the reasons explained above regarding limitation 12[e]. EX1003 ¶116.

12. Claim 17: "The power routing structure according to claim 16, wherein the second partial local power mesh comprises: at least one second local ground wire that couples to the ground wire of the global power mesh; and at least one fourth power wire that couples to the second power wire and the second power domain."

Jiang discloses a fourth power wire that couples to the second power wire and the second power domain, as illustrated in Jiang's Figure 1(b).



EX1004, Fig. 1(b) (annotated); EX1003 ¶117.

Adding the at least one second local ground wire that couples to the ground wire of the global power mesh would have been obvious for the reasons discussed above regarding claim 16. EX1003 ¶118.

Alternatively, this limitation would have been obvious in view of the separate supply voltages of Li or Chiu for all the reasons explained above regarding limitation 12[e]. EX1003 ¶119.

13. Claim 18: "The power routing structure according to claim 17, wherein the first local ground wire and the second local ground wire share the same ground wire of the global power mesh."

Jiang would necessarily use a single ground supply for its single voltage supply. Even if independent voltages were used, it would have been obvious for a POSITA to use a common ground in Jiang's global and partial local power meshes

in view of Li or Chiu for simplicity and to ensure reliable circuit operation. EX1003 ¶¶120-21. As explained above, both Li and Chiu use a common ground. EX1005, 493 ("[The Broadcom chip] is designed with two power supply inputs and one ground input at the package level."), Fig. 3 (showing single ground in both Metal6 and Metal7); EX1006, Figs. 6, 7 (showing a single negative supply grid VSS (110)); *see also* EX1012, 85 (describing a chip using a common ground); EX1003 ¶120.

A POSITA would understand that in a system with a single ground supply, all the ground wires in the global power mesh would be shared by the ground wires in the partial local power meshes. EX1003 ¶121.

B. Ground 3 – Claims 1-11 and 19-20 are obvious over each of Grounds 1-2 in further view of Bertolet and the Low Power Methodology Manual

1. Claim 1

Claim 1 differs from claim 12 in that it describes using an automatic placement and routing (APR) tool in a power routing arrangement method for creating a power routing structure that would be met by the routing structure in claim 12. EX1003 ¶¶122-23 (citing EX1001).

Claim 1's first and second power domains, first and second partial local power meshes, and global power mesh are disclosed and/or rendered obvious for the reasons discussed above regarding limitations 12[preamble], 12[a]-[c], 12[e]-[f]. *See* §§V.A.1-4, V.A.6-7; EX1003 ¶124.

Regarding claim 1's "power routing arrangement method," to the extent the preamble is limiting, a POSITA would understand that using a particular arrangement for power routing is a power routing arrangement method, satisfying the preamble. EX1003 ¶125. Also, using a power routing arrangement method to form Jiang's routing structure would have been obvious because a POSITA knew to employ a power routing arrangement method when designing integrated circuits. *Id*. For example, LPMM and Bertolet both discuss such methods that could be used to form the power routing structure in Jiang, as discussed in more detail below. EX1012, 177-78; EX1013, 126.

Additionally, a POSITA would have found it obvious to form and couple Jiang's power meshes as shown in Jiang's Figure 1(b) with an APR tool. As the '218 Patent admits, APR tools were "well-known." EX1001, 1:37; EX1003 ¶126. For example, Bertolet describes using a program to "algorithmically generate[]" "a power distribution network." EX1013, 126. Bertolet explains that this "algorithm provides the capability to define multiple power terrains by area and level of metal." *Id*. Indeed, Bertolet explains that the algorithm can generate a routing structure including a global "common power grid on metal levels one and two" and multiple local "power grids on metal levels three through five." *Id*.

Similarly, LPMM teaches that a multi-voltage design can be synthesized using an APR tool, and "recommend[s] highly" that one do so "wherever possible."

EX1012, 177-78 ("Today, the sleep transistor power network can be synthesized using a power planning tool PNS [PNS] that considers all the three components."); EX1003 ¶127.

A POSITA would find it obvious to use an APR tool to form Jiang's power meshes, including the first partial local power mesh, and couple the entire power routing structure based on LPMM and/or Bertolet. Using an APR tool would save time and effort in chip design. EX1003 ¶128. Indeed, LPMM recommends implementing a "multi-voltage design" using an "automated power network synthesis" "wherever possible." EX1012, 177. In fact, LPMM warns that "[t]he number of concurrently changeable variables in a multi-voltage system is such that attempting to construct a power plan manually may result in a suboptimal result." *Id.*; *see also id.*, 178 ("Recommendations: Use a power planning tool which supports switch cells to create the sleep transistor power network including switch cell insertion and placement."); EX1024, 5:28-32 ("Place and route tools are significantly faster and provide more flexibility and control in the place and route process ….").

Additionally, a POSITA would have had a reasonable expectation of success in using an APR tool, as taught in Bertolet or LPMM, to form Jiang's meshes and couple them to Jiang's power domains. Indeed, LPMM specifically teaches that "power-gating design" such as a "sleep transistor power network can be synthesized

using a power planning tool." EX1012, 178. Similarly, Bertolet confirms that a "power distribution network" like Jiang's, with global and local grids on different metal layers, can be "algorithmically generated." EX1013, 126; EX1004, 1-2. Additionally, using an APR tool to form and couple Jiang's power meshes would be no more than using "well-known" techniques to achieve a predictable outcome. EX1003 ¶129.

Furthermore, by July 2006, well before the earliest '218 Patent application was filed, Patent Owner itself had successfully designed multi-voltage power routing structures using a commercially available APR tool. *Id*. (citing EX1025 ("Realtek Semiconductor Corp. … and others have successfully taped out more than 15 multi-voltage designs with Synopsys' Galaxy™ design platform RTL-to-GDSII advanced low-power solution."); EX1026); *see also* EX1020, 3 (using "automated techniques" to generate a "row-by-row dual-V_{DD}" mesh), Fig. 4. Given this fact, the '218 Patent's assertion that this was not possible (EX1001, 1:37-39) is simply incorrect.

Accordingly, claim 1 is obvious over Jiang in view of Jiang2 and Jiang3, optionally in further view of Li or Chiu, and in further view of Bertolet and LPMM. EX1003 ¶130

2. Claim 2: "The arrangement method according to claim 1, wherein the first partial local power mesh and the second partial local power mesh are positioned on the same metal layer."

This limitation is disclosed or rendered obvious for the reasons discussed regarding limitation 12[d]. *See* §V.A.5; EX1003 ¶131.

3. Claim 3: "The arrangement method according to claim 2, wherein the global power mesh and the first local power mesh are positioned on different metal layers."

This limitation is disclosed or rendered obvious for the reasons discussed regarding limitation 12[d]. *See* §V.A.5; EX1003 ¶132.

4. Claim 4: "The arrangement method according to claim 3, wherein the global power mesh is positioned above the first local power mesh."

This limitation is disclosed or rendered obvious for the reasons discussed regarding claim 13. *See* §V.A.8; EX1003 ¶133.

5. Claim 5: "The arrangement method according to claim 2, wherein the first partial local power mesh and the second partial local power mesh are not electrically coupled."

This limitation is disclosed or rendered obvious for the reasons discussed regarding claim 14. *See* §V.A.9; EX1003 ¶134.

6. Claim 6: "The arrangement method according to claim 1, wherein the global power mesh comprises at least one ground wire, at least one first power wire that provides power to the first power domain, and at least one second power wire that provides power to the second power domain."

This limitation is disclosed or rendered obvious for the reasons discussed regarding claim 15. *See* §V.A.10; EX1003 ¶135.

7. Claim 7: "The arrangement method according to claim 6, wherein the first partial local power mesh comprises: at least one first local ground wire that couples to the ground wire of the global power mesh; and at least one third power wire that couples to the first power wire and the first power domain."

This limitation is disclosed or rendered obvious for the reasons discussed regarding claim 16. *See* §V.A.11; EX1003 ¶136.

8. Claim 8: "The arrangement method according to claim 7, wherein the second partial local power mesh comprises: at least one second local ground wire that couples to the ground wire of the global power mesh; and at least one fourth power wire that couples to the second power wire and the second power domain."

This limitation is disclosed or rendered obvious for the reasons discussed regarding claim 17. *See* §V.A.12; EX1003 ¶137.

9. Claim 9: "The arrangement method according to claim 8, wherein the first local ground wire and the second local ground wire share the same ground wire of the global power mesh."

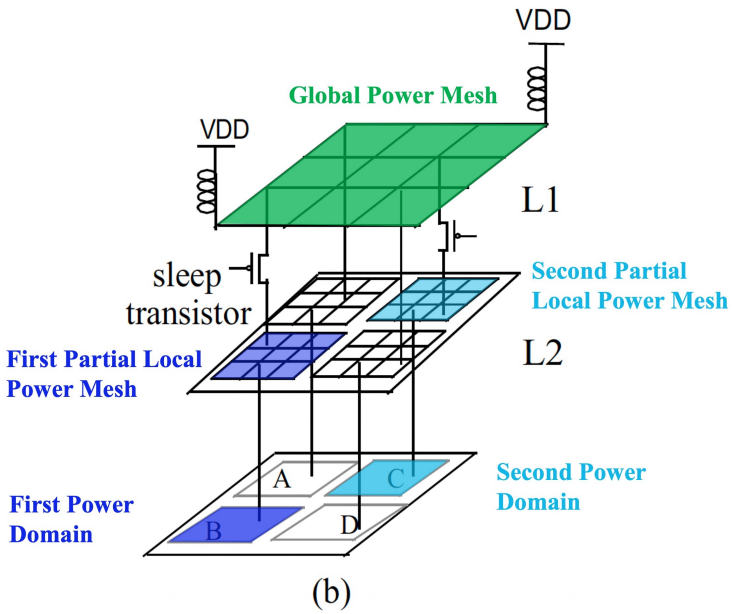
This limitation is disclosed or rendered obvious for the reasons discussed regarding claim 18. *See* §V.A.13; EX1003 ¶138.

10. Claim 10: "The arrangement method according to claim 1, wherein the positions of the first partial local power mesh and the second partial local power mesh correspond to the first power domain and the second power domain, respectively."

This limitation is disclosed or rendered obvious for the reasons discussed regarding limitations 12[a]-12[b]. *See* §§V.A.2-3; EX1003 ¶139.

11. Claim 11: "The arrangement method according to claim 1, wherein the global power mesh is distributed evenly above the first local power mesh and the area of the second local power mesh."

Jiang discloses this limitation. As shown in Figure 1(b), Jiang's global power mesh is distributed evenly above all partial local power meshes.



EX1004, Fig. 1(b) (annotated); EX1003 ¶140; *see also* EX1004, 2 (referring to global power mesh as "upper"). Jiang's Figure 10 also shows evenly distributed power meshes.

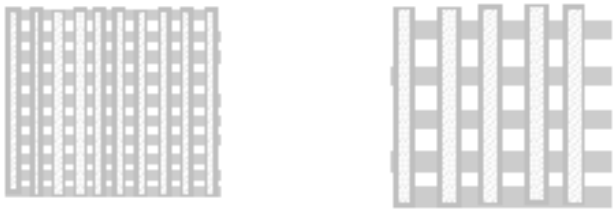


Figure 10. Power mesh granularity

EX1004, Fig. 10.

12. Claim 19[preamble]: "A power routing arrangement method applied in an integrated circuit having multiple power domains, the arrangement method comprising:"

To the extent the preamble is limiting, it is obvious over the combination for the same reasons discussed regarding claim 1. *See* §1V.B.1; EX1003 ¶141.

13. Claim 19[a]: "providing a global power mesh, positioned above a first power domain and a second power domain, comprising at least one first power wire that provides the voltage needed by the first power domain, at least one second power wire that provides the voltage needed by the second power domain, and at least one ground wire that provides the ground potential needed by the first power domain and the second power domain by an automatic placement and routing (APR) tool;"

The combination discloses or renders obvious the global power mesh as claimed for the reasons discussed regarding limitation 12[c] and claims 13 and 15. *See* §§V.A.4, V.A.8, V.A.10; EX1003 ¶142.

It would have been obvious to provide claim 19's global power mesh and power routing structure with an APR tool for the reasons provided with respect to claim 1. *See* §V.B.1; EX1003 ¶143.

14. Claim 19[b]: "coupling the first power wire and the ground wire of the global power mesh to the first power domain by the APR tool; and"

The combination renders obvious that the first power wire and ground wire are coupled to the first domain for the reasons discussed regarding claims 16 and 18. *See* §§V.A.11, V.A.13; EX1003 ¶144; *see also* §V.B.13V.B.13 (describing obviousness of using APR tool). Additionally, Li discloses an "in-house automated procedure" for "connecting local logic to the top-level power grid" further motivating use of an APR tool in this application. EX1005, 493; EX1003 ¶144.

15. Claim 19[c]: "coupling the second power wire and the ground wire of the global power mesh to the second power domain by the APR tool;"

The combination renders obvious that the second power wire and ground wire are coupled to the second power domain for the reasons discussed regarding claims 16-18 and 19(b). *See* §§V.A.11-13, V.B.14; EX1003 ¶145; *see also* §V.B.13 (describing obviousness of using APR tool).

16. Claim 19[d]: "wherein the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer; and"

The combination discloses or renders this limitation obvious for the same reasons discussed regarding limitation 12[e]. *See* §V.A.6; EX1003 ¶146.

17. Claim 19[e]: "wherein the first metal layer and the second metal layer are different layers."

The combination discloses or renders this limitation obvious for the same reasons discussed regarding limitation 12[f]. *See* §V.A.7; EX1003 ¶147.

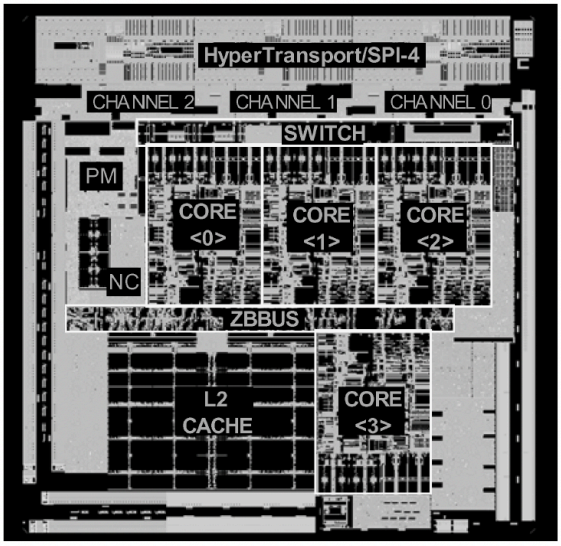
18. Claim 20: "The arrangement method according to claim 19, wherein the first power domain and the second power domain share the same ground wire of the global power mesh."

The combination discloses or renders this limitation obvious for the same reasons discussed regarding claim 18. *See* §V.A.13; EX1003 ¶148.

C. Ground 4 – Claims 12-18 are obvious over Li in view of Jiang

1. Claim 12[preamble]: "A power routing structure applied in an integrated circuit having multiple power domains, comprising:"

To the extent limiting, Li discloses the preamble. Li discloses a power routing structure for an integrated circuit "designed with multiple power domains," namely the Broadcom chip, shown below.



EX1005, Fig. 1, 491 ("A system on a chip (SOC) BCM1280 has been designed with four 64-bit MIPS™ CPU cores. … Each single core … forms a separate processor region. Therefore, … each core is now built in a unique voltage region."); *see also id*. ("the chip is divided into two logic voltage regions"); *id*., 491-92 (discussing "the multi-power-domain power grid" of the Broadcom chip); *id*., 492 (Table I: "Supply Voltages 1.1V, 2.5V and 3.3V"). Li teaches that its "multiple voltage regions across the chip" help "enable[] power-saving capability with a selectable configuration, allowing the chip to be an optimal fit into a broad variety of applications." *Id.*, 493; EX1003 ¶149.

Li describes a global power grid, as shown in Li's Figure 3 below, and multiple local grids.

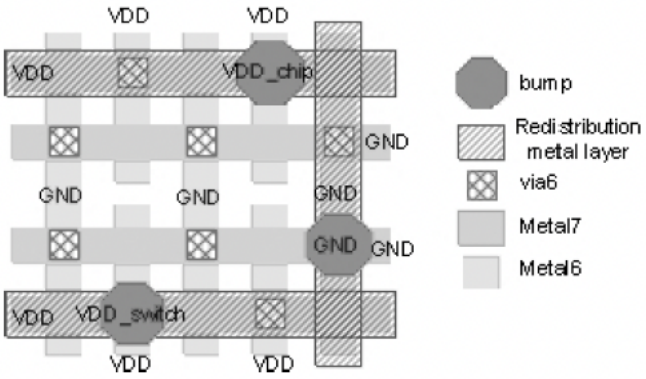
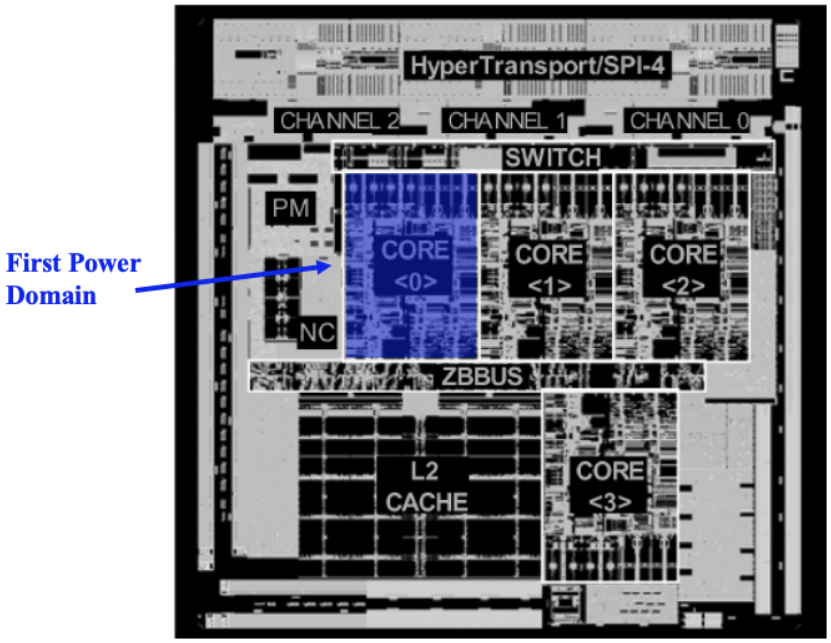


Fig. 3. Power and ground are distributed from the bumps onto the chip-level power grid through a redistribution metal layer.

EX1005, Fig. 3, 493 (describing the global and local power grids); EX1003 ¶150.

2. Claim 12[a]: "a first partial local power mesh having its position corresponding to the position of a first power domain and coupling to the first power domain;"

Li discloses or renders obvious this limitation. Li discloses that "each core is now built in a unique voltage region." EX1005, 491; *see also id*., 493 ("[T]here are multiple voltage regions across the chip."). Accordingly, a POSITA would understand that Core <0>, as shown in Figure 1, is a "first power domain."



Id., Fig. 1 (annotated). Cores <1>, <2>, and <3> could also be the claimed "first power domain." EX1003 ¶151.

Li also discloses a plurality of "local power grids," which are local power meshes, in the "local sections" on metal layers 2-5. EX1005, 493. Because Li describes multiple local power grids on the same four metal layers, those local power grids are necessarily partial in that they cannot cover the entire chip without running

into each other. Moreover, the local power grids would also necessarily correspond to the position of their respective power domains because otherwise they could not supply power to the power domains. *See id.* ("The power and ground lines in the local sections are grided on Metal-2 through Metal-5, on which the local power grids are formed at the block level. The local power grids are left floating until final assembly at the full-chip level. At the final stage of the layout design, an in-house automated procedure is applied, connecting local logic to the top-level power grid, to implement a complete full-chip power distribution network."). A POSITA would understand that Li's local power grids sit above their respective domains and provide power vertically downward into the circuitry. EX1003 ¶¶152-53.

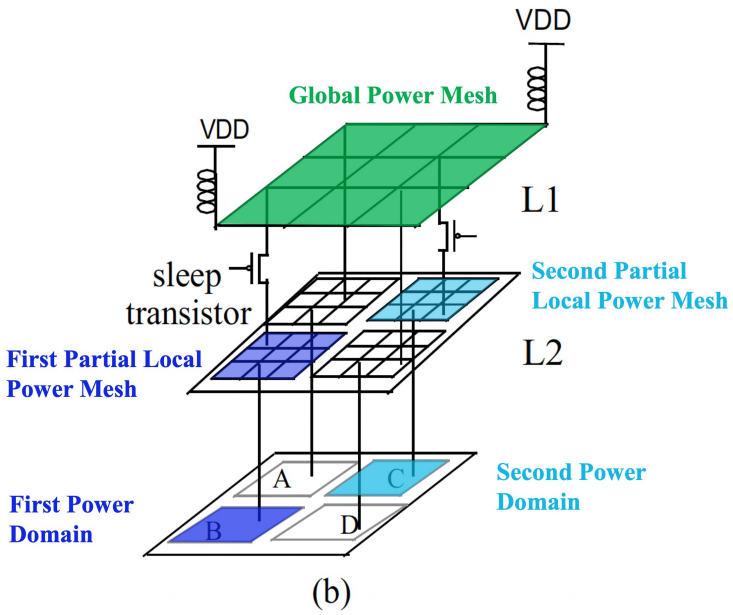
Additionally, it would have been obvious for Li's local power grids to be partial local power meshes having their positions correspond to the positions of their respective power domains. EX1003 ¶154. As Dr. Subramanian explains:

> [I]t was known to a POSITA that local grids covering the same surface area as the domains to which they supply power were preferable. A local grid covering more area than its underlying power domain is a waste of local grid resources and takes up valuable chip area that could be used for neighboring local grids or other purposes.

EX1003 ¶155 (citing EX1006, 9:14-18; EX1016, 5:14-18). Having Li's local power grids be partial local power meshes with positions corresponding to the position of

their respective power domains would have simply been combining prior art elements according to known methods to yield predictable results. EX1003 ¶155.

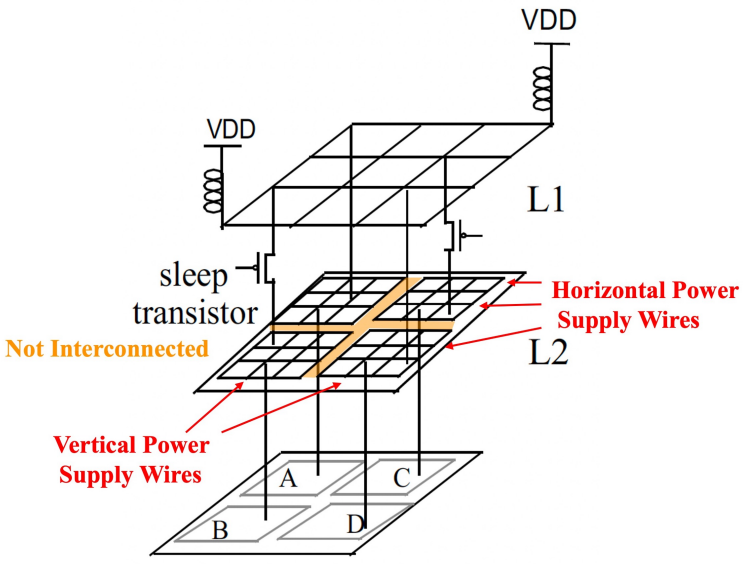
Indeed, Jiang's local grids correspond to the positions of its power domains.



EX1004, Fig. 1(b) (annotated). It would have been obvious for each of Li's local grids to similarly have its position correspond to the position of its respective power domain. Indeed, a POSITA would have understood that doing so would be a simple, straightforward, and efficient way to route power from the supply inputs to power domains in Li's circuit. EX1003 ¶156.

Alternatively, it would have been obvious for Li's local power grids to be implemented as partial local power meshes. As discussed above, the '218 Patent describes its partial local power meshes as "web-like structures," which are "not interconnected," that "comprise[] a plurality of horizontal power supply wires and a

plurality of vertical power supply wires." EX1001, 3:44-51. Li discloses that its global power grid is a web-like structure of horizontal and vertical power supply wires. EX1005, Fig. 3, 493. It would have been obvious for Li's local power grids to similarly be web-like structures of horizontal and vertical wires. EX1003 ¶157. Indeed, a POSITA would have known that a power grid is typically "a meshing of horizontal and vertical metal rails on two metallization layers." EX1016, 8:57-59; *see also* EX1019, 4:57-64, Fig. 2. Additionally, a POSITA would have known that in a power routing structure with a plurality of local grids, the local grids would not be interconnected. For example, Jiang teaches a power routing structure with a plurality of local power grids that are not interconnected, as shown in Jiang's Figure 1(b) below.



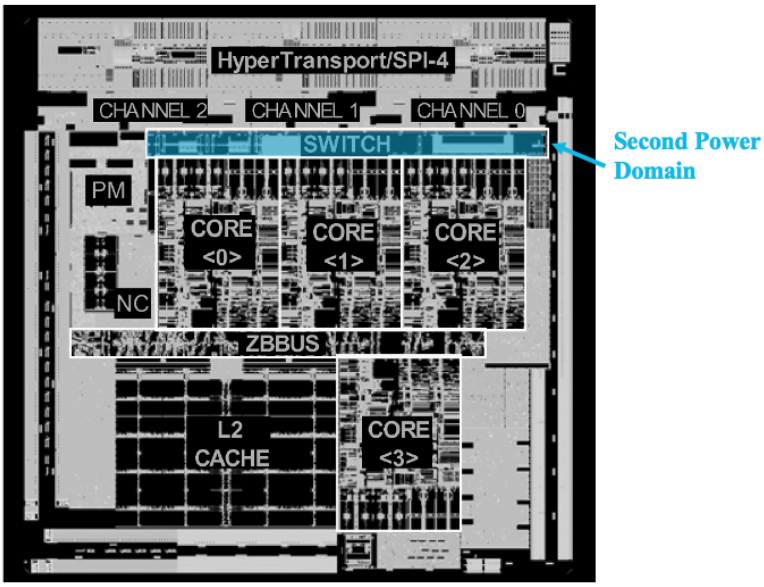
(b)

EX1004, Fig. 1(b) (annotated). This allows Jiang to save power by shutting off the power to idle power domains and their local power grids. EX1004, 1-2; EX1003 ¶¶157-58. A POSITA would have found it obvious for Li's local power grids similarly to be disconnected from one another to save power. EX1003 ¶158; EX1005, 493 (noting Li's "power-saving capability" as a result of its "multiple voltage region[]" design). For at least these reasons, a POSITA would understand that Li's local power grids meet the claimed "partial local power mesh" or that the combination renders them obvious. EX1003 ¶159 (citing EX1001, 3:44-51; EX1004, Fig. 1(b)).

3. Claim 12[b]: "a second partial local power mesh having its position corresponding to the position of a second power domain and coupling to the second power domain; and"

Li discloses, or at least renders obvious this limitation. Li discloses a "switch" in a separate power domain from the cores and receiving power from a separate voltage supply "VDD_switch" from the power received by Jiang's cores. EX1005, 495.

A POSITA would understand that Li's "switch," or the region powered by VDD_switch and encompassing the "switch," forms a second power domain, as illustrated below.



EX1005, Fig. 1 (annotated); EX1003 ¶¶160-61, 163.

As discussed above regarding Li and limitation [12.a], Li teaches a plurality of partial local power meshes (Li's "local power grids") on metal layers 2-5. EX1005, 493; EX1003 ¶162. It would have been obvious for Li's second power domain to have a partial local power mesh corresponding to its position for the same reasons discussed above regarding Li and limitation 12[a].

4. Claim 12[c]: "a global power mesh, coupling to the first local power mesh and the second local power mesh, to provide the power needed by the first power domain and the second domain separately;"

Li discloses this limitation. Li discloses a "top-level power grid" on metal layers 6-7 for "distributing power and ground across the chip," which constitutes a global power mesh. EX1005, 493. Li teaches that:

> Metal-6 and metal-7 [sic] are extensively used in distributing power and ground across the chip. Ground (GND) and power (VDD_chip, VDD_switch) lines are routed alternately on Metal-6 in the vertical direction and Metal-7 in the horizontal direction. This forms the power grid structure at the chip top level. … The local power grids are left floating until final assembly at the full-chip level. At the final stage of the layout design, an in-house automated procedure is applied, connecting local logic to the top-level power grid, to implement a complete full-chip power distribution network.

Id. Thus, Li describes coupling the first and second partial local power meshes to the global power mesh to provide the power needed by the first power domain and the second power domain. EX1003 ¶164.

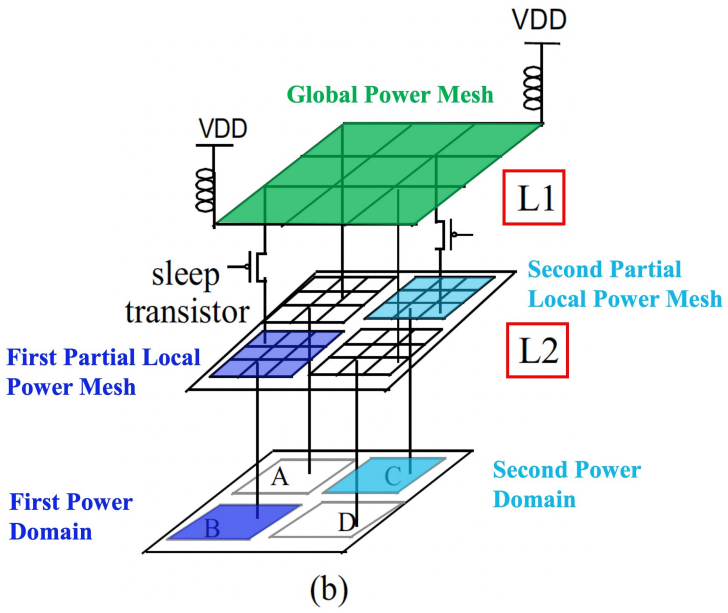
As discussed, Li's first power domain (Core <0>) and second power domain (switch) receive power from separate power supplies (VDD_chip and VDD_switch, respectively). EX1005, 495; EX1003 ¶165.

5. Claim 12[d]: "wherein the first partial local power mesh and the second partial local power mesh are positioned on the same metal layer while the global power mesh and the first local power mesh are positioned on different metal layers;"

This limitation is disclosed in Li, or at least rendered obvious by Li in view of Jiang. Li discloses that the "local power grids" are on the same metal layers ("Metal-2 through 5"), while the "top-level power grid" is on different metal layers ("Metal-6 and [M]etal-7"). EX1005, 493; EX1003 ¶166.

Alternatively, it would have been obvious for a POSITA to place these local grids on the same layers because doing so permits Li's local power grids to be housed on just two metal layers, using layers more efficiently and saving manufacturing cost. EX1003 ¶167. It was known to place different partial local power meshes on the same layers.

For example, Jiang discloses that its partial local power meshes are on the same layers ("L2"), while its global power mesh is on different layers ("L1") as illustrated below.



EX1004, Fig. 1(b) (annotated). Positioning Li's partial local power meshes on the same layers would have constituted combining prior art elements according to known methods to yield predictable results and would constitute a simple

substitution of one known element (local grids on different metal layers) for another (local grids on the same metal layers) to obtain predictable results. EX1003 ¶167.

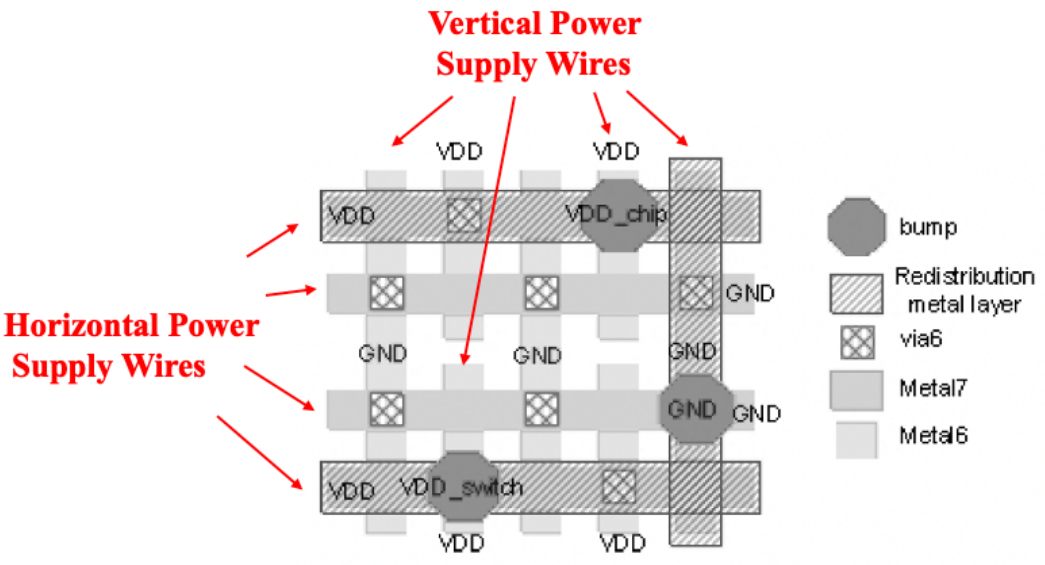
Additionally, using the same metal layers for Li's partial local power meshes would have been obvious because it was simply the use of a known technique (local grids on the same metal layers) to improve similar devices (multiple power domain integrated circuit power distribution systems) in the same way. It also would have constituted application of a known technique (local grids on the same metal layers) to a known device (multiple power domain integrated circuits) ready for improvement to yield predictable results. EX1003 ¶168.

Similarly, Li itself teaches at least some local power grids on the same metal layers because Li discloses multiple voltage domains across the chip, EX1005, 493, with only four metal layers (layers 2-5) to hold the local power grids. Thus, Li itself teaches the use of multiple local power grids on the same metal layers. EX1003 ¶166.

6. Claim 12[e]: "wherein the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer; and"

Li discloses this limitation. Li discloses with respect to the "top-level power grid," which is a global power mesh, "Ground (GND) and power (VDD_chip, VDD_switch) lines are routed alternately on Metal-6 in the vertical direction and

Metal-7 in the horizontal direction." EX1005, 493. This arrangement of horizontal and vertical power supply wires can be seen in Li's Figure 3, below.



EX1005, Fig. 3 (annotated); EX1003 ¶169.

7. Claim 12[f]: "wherein the first metal layer and the second metal layer are different layers."

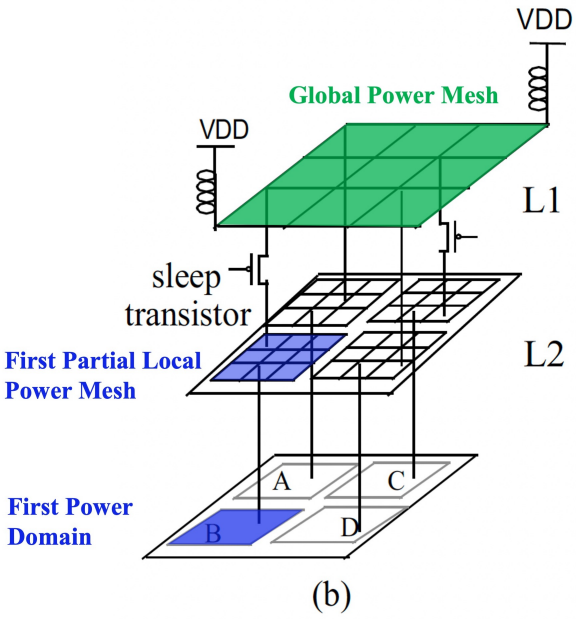
Li discloses this limitation as explained above regarding 12[e]. EX1005, 493-94; EX1003 ¶170.

8. Claim 13: "The power routing structure according to claim 12, wherein the global power mesh is positioned above the first local power mesh."

This limitation is disclosed in Li and rendered obvious by Li in view of Jiang. Li discloses that its global power mesh routes power all over the chip. EX1005, 493. Li further explains, "Metal-6 and metal-7 are extensively used in distributing power and ground across the chip. Ground (GND) and power (VDD_chip, VDD_switch)

lines are routed alternately on Metal-6 in the vertical direction and Metal-7 in the horizontal direction. This forms the power grid structure at the chip top level." *Id.* A POSITA would understand, therefore, that Li's global power mesh is above each of Li's local power grids (the partial local power meshes) on the chip, which are "grided on Metal-2 through Metal-5." *Id.*; EX1003 ¶171; *see also* §§V.C.2-3.

Additionally, this limitation would have been obvious over Li in view of Jiang. Jiang discloses that its global power mesh is positioned above its first partial local power mesh, as shown in Figure 1(b), below.



EX1004, Fig. 1(b) (annotated); EX1003 ¶172.

It would have been obvious for Li's global power mesh to be arranged in the same manner as that is a simple way to provide power to the partial local power meshes as Li expressly discloses. EX1003 ¶173. Indeed, positioning Li's global

power mesh above its partial local power meshes would have been a routine application of a known feature with a reasonable expectation of success. *Id*. (citing EX1018, 2:60-3:3 (discussing power grids formed above the circuit blocks they supply)). Li's description of its global power mesh as being at the "chip top level," EX1005, 493, if not an express description of this limitation, is at least an express motivation to use the known arrangement of Jiang.

Implementing Jiang's arrangement in Li would have involved combining prior art elements according to known methods to yield predictable results and simple substitution of one known element (global power mesh positioned above partial local power meshes) for another to obtain predictable results. Similarly, such substitution (to the extent any is involved) would have been the use of a known technique (global power mesh positioned above partial local power mesh) to a known device (Li's BCM1280) ready for improvement to yield a predictable result. A POSITA would have been motivated to place the global power mesh on the chip top level to simplify routing power into the chip from external power connections and based on Li's express statement that the global power mesh is at "chip top level." EX1003 ¶174; EX1005, 493.

9. Claim 14: "The power routing structure according to claim 13, wherein the first local power mesh and the second local power mesh are not electrically coupled."

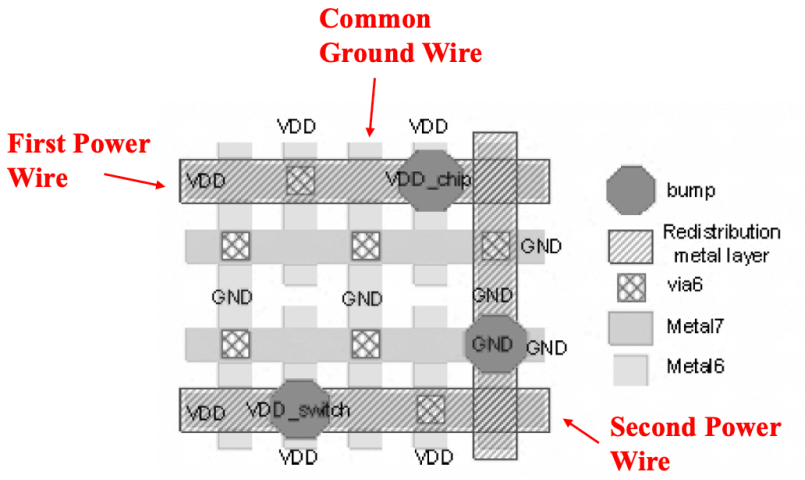
Li discloses this limitation. Li discloses that "the individual cores are electrically isolated from one another as well as the rest of the chip." EX1005, 494. Accordingly, a POSITA would understand that the first partial local power mesh (for Core<0>) is not electrically coupled to the second partial local power mesh (for the switch). EX1003 ¶175. Indeed, as these two domains receive power from different sources (VDD_chip and VDD_switch), their respective local power grids cannot be electrically coupled. EX1005, 491 ("[E]ach core is now built in a unique voltage region. In addition to the complexity of the multiple ground domains, the chip is divided into two logic voltage regions …."); *see also id*., 493 (same), 494 (Fig. 3 showing no connection between VDD_chip and VDD_switch).

10. Claim 15: "The power routing structure according to claim 12, wherein the global power mesh comprises: at least one ground wire; at least one first power wire that provides the power needed by the first power domain; and at least one second power wire that provides the power needed by the second power domain."

Li discloses a plurality of power and ground wires in its global power mesh ("Ground (GND) and power (VDD_chip, VDD_switch) lines"). EX1005, 493. Figure 3 below shows at least 3 ground wires on Metal 6 and at least two ground wires on Metal 7, satisfying the "at least one ground wire" requirement. Any or all

ground wires in the global power mesh, including others not shown in Figure 3, in Metal 6 and Metal 7 could be the "at least one ground wire."

Figure 3 also shows multiple VDD_chip and VDD_switch power wires in the global power mesh on Metal 6 and Metal 7. Because this "forms the power grid structure at the chip top level" and because Li discloses that the "local logic [is connected] to the top-level power grid, to implement a complete full-chip power distribution network," *id.*, Li discloses that at least one VDD_chip power wire provides the power needed by the first power domain, and at least one VDD_switch power wire provides the power needed by the second power domain. The required at least one first and second power wires could be any or all VDD_chip and VDD_switch power wires, respectively, in Metal 6 or Metal 7.



EX1005, Fig. 3 (annotated); *see also id.*, 495 ("VDD_chip provides power for all the internal logic except the node controller, packet manager, switch and HT/SPI-4

ports. … VDD_switch provides power for all the internal logic of the node controller (NC), packet manager (PM), switch and HT/SPI-4 ports."); EX1003 ¶¶176-77.

11. Claim 16: "The power routing structure according to claim 15, wherein the first partial local power mesh comprises: at least one first local ground wire that couples to the ground wire of the global power mesh; and at least one third power wire that couples to the first power wire and the first power domain."

Li discloses this limitation. Li discloses that the local power grids (partial local power meshes) are comprised of "power and ground lines" and are connected "to the top-level power grid, to implement a complete full-chip power distribution network." EX1005, 493. Thus, Li expressly discloses at least one first local ground wire in the first partial local power mesh is coupled to at least one ground wire of the global power mesh satisfying this limitation. EX1003 ¶178. Li also expressly discloses at least one third power wire in the first partial local power mesh that couples to at least one first power wire of the global power mesh (supplying VDD_chip) and the first power domain (Core <0>). EX1005, 493. Because the "at least one third power wire" can be all the power wires in the local grid, this limitation is necessarily satisfied by Li's local power grid, which is coupled to both the top-level global grid and the underlying power domain.

Alternatively, a POSITA would understand that Li's disclosure necessarily requires, or at least renders obvious that one of the local ground wires (ground lines) is coupled to at least one ground wire in the top-level power grid and that one of the

local power wires (power lines) is coupled to at least one power wire in the top-level power grid. Indeed, a POSITA would know that such connections would be necessary "to implement a complete full-chip power distribution network" as disclosed by Li. EX1005, 493. Without such connections, power would not flow, and the chip would be non-functional. EX1003 ¶179. Additionally, it would have been obvious to couple local ground and power wires to global ground and power wires, respectively, as Li expressly suggests. Li discloses that the "local power grids are left floating until final assembly at the full-chip level," when Li discloses "an in-house automated procedure is applied, connecting local logic to the top-level power grid, to implement a complete full-chip power distribution network." EX1005, 493. If the local power grids were not coupled to the top-level power grid, they would still be floating and useless.

12. Claim 17: "The power routing structure according to claim 16, wherein the second partial local power mesh comprises: at least one second local ground wire that couples to the ground wire of the global power mesh; and at least one fourth power wire that couples to the second power wire and the second power domain."

Li discloses or renders obvious this limitation with respect to the second power domain (switch) and VDD_switch and the second local ground wire and at least one fourth power wire for the same reasons discussed above regarding claim 16. *See* §V.C.11; EX1003 ¶180.

13. Claim 18: "The power routing structure according to claim 17, wherein the first local ground wire and the second local ground wire share the same ground wire of the global power mesh."

Li discloses or renders obvious this limitation. Li discloses that it has a "common" "ground reference GND." EX1005, 495. Accordingly, a POSITA would understand that the first and second partial local power meshes, and their local ground wires, would be connected to all the ground wires of the global power mesh and thus would all "share the same ground wire of the global power mesh" when powered up. EX1003 ¶181.

D. Ground 5 – Claims 1-11 and 19-20 are obvious over Li in view of Jiang and in further view of Bertolet and the Low Power Methodology Manual

1. Claim 1

Claim 1 differs from claim 12 in that it describes a power routing arrangement method for creating a power routing structure that would be met by the routing structure in claim 12 through the use of an automatic placement and routing (APR) tool. EX1003 ¶¶123 (citing EX1001), 182.

Claim 1's first and second power domains, first and second partial local power meshes, and global power mesh are disclosed and/or rendered obvious for the reasons discussed above regarding limitations 12[preamble], 12[a]-[c], 12[e]-[f]. *See* §§V.C.1-4, V.C.6-7; EX1003 ¶183.

Regarding claim 1's "power routing arrangement method," to the extent the preamble is limiting, Li describes "an in-house automated procedure" that is used to "connect[] local logic to the top-level power grid[] to implement a complete full-chip power distribution network." EX1005, 493. Further, a POSITA would understand that using a particular arrangement or structure for power routing is a power routing arrangement method satisfying the preamble. EX1003 ¶184.

Also, use of a power routing arrangement method with Li's routing structure would have been obvious because a POSITA was aware of the need to employ such a method when designing integrated circuits. EX1003 ¶185. For example, LPMM and Bertolet both discuss such methods that could be used to form the power routing structure in Li, as discussed in more detail below. EX1012, 177-78; EX1013, 126.

Additionally, a POSITA would have found it obvious to form and couple Li's power meshes as discussed above in §V.C with an APR tool. Indeed, Li itself teaches using an "in-house automated procedure" to couple its power grids and "implement a complete full-chip power distribution network." EX1005, 493. A POSITA would find it obvious that a similar automated procedure could be used to form Li's grids, including its global and partial local power meshes, in the first place. EX1003 ¶186.

As discussed in Section V.B.1, both Bertolet and LPMM teach the use of APR tools to generate power distribution networks, and LPMM specifically recommends

their use in this application. Thus, a POSITA would find it obvious to use an APR tool to form and couple Li's global and partial local power meshes based on LPMM and/or Bertolet for the same reasons discussed in Section V.B.1. EX1003 ¶187.

2. Claim 2: "The arrangement method according to claim 1, wherein the first partial local power mesh and the second partial local power mesh are positioned on the same metal layer."

This limitation is disclosed or rendered obvious for the reasons discussed regarding limitation 12[d]. *See* §V.C.5; EX1003 ¶188.

3. Claim 3: "The arrangement method according to claim 2, wherein the global power mesh and the first local power mesh are positioned on different metal layers."

This limitation is disclosed or rendered obvious for the reasons discussed regarding limitation 12[d]. *See* §V.C.5; EX1003 ¶189.

4. Claim 4: "The arrangement method according to claim 3, wherein the global power mesh is positioned above the first local power mesh."

This limitation is disclosed or rendered obvious for the reasons discussed regarding claim 13. *See* §V.C.8; EX1003 ¶190.

5. Claim 5: "The arrangement method according to claim 2, wherein the first partial local power mesh and the second partial local power mesh are not electrically coupled."

This limitation is disclosed or rendered obvious for the reasons discussed regarding claim 14. *See* §V.C.9; EX1003 ¶191.

6. Claim 6: "The arrangement method according to claim 1, wherein the global power mesh comprises at least one ground wire, at least one first power wire that provides power to the first power domain, and at least one second power wire that provides power to the second power domain."

This limitation is disclosed or rendered obvious for the reasons discussed regarding claim 15. *See* §V.C.10; EX1003 ¶192.

7. Claim 7: "The arrangement method according to claim 6, wherein the first partial local power mesh comprises: at least one first local ground wire that couples to the ground wire of the global power mesh; and at least one third power wire that couples to the first power wire and the first power domain."

This limitation is disclosed or rendered obvious for the reasons discussed regarding claim 16. *See* §V.C.11; EX1003 ¶193.

8. Claim 8: "The arrangement method according to claim 7, wherein the second partial local power mesh comprises: at least one second local ground wire that couples to the ground wire of the global power mesh; and at least one fourth power wire that couples to the second power wire and the second power domain."

This limitation is disclosed or rendered obvious for the reasons discussed regarding claim 17. *See* §V.C.12; EX1003 ¶194.

9. Claim 9: "The arrangement method according to claim 8, wherein the first local ground wire and the second local ground wire share the same ground wire of the global power mesh."

This limitation is disclosed or rendered obvious for the reasons discussed regarding claim 18. *See* §V.C.13; EX1003 ¶195.

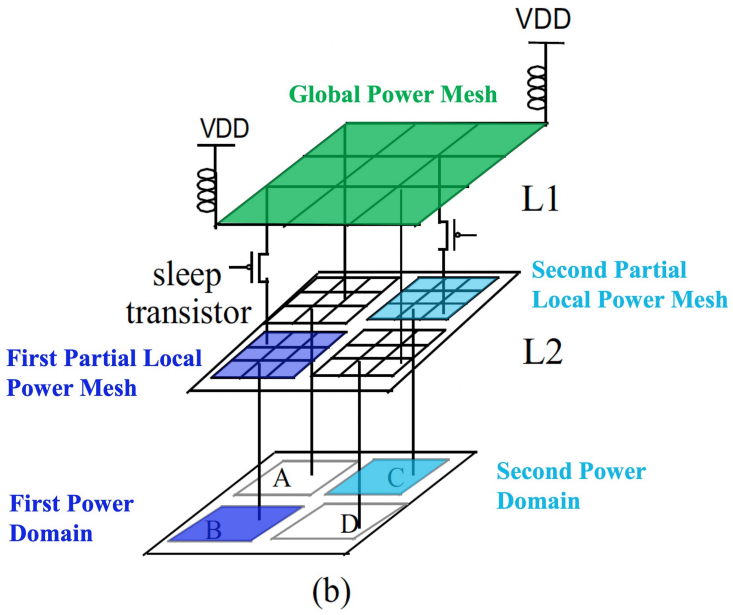
10. Claim 10: "The arrangement method according to claim 1, wherein the positions of the first partial local power mesh and the second partial local power mesh correspond to the first power domain and the second power domain, respectively."

This limitation is disclosed or rendered obvious for the reasons discussed regarding limitations 12[a]-12[b]. *See* §§V.C.2-3; EX1003 ¶196.

11. Claim 11: "The arrangement method according to claim 1, wherein the global power mesh is distributed evenly above the first local power mesh and the area of the second local power mesh."

Li discloses or renders obvious this limitation. Li explains, "Metal-6 and metal-7 are extensively used in distributing power and ground across the chip. Ground (GND) and power (VDD_chip, VDD_switch) lines are routed alternately on Metal-6 in the vertical direction and Metal-7 in the horizontal direction. This forms the power grid structure at the chip top level." EX1005, 493. A POSITA would understand, therefore, that Li's global power mesh is above each of the local power grids on the chip, which are in Metal-2 through Metal-5. *Id*. Accordingly, a POSITA would understand that Li's global power mesh is distributed evenly above each partial local power mesh in the pattern shown in Figure 3. EX1003 ¶197.

Alternatively, this limitation would have been obvious in view of Jiang. As shown in Figure 1(b), Jiang's global power mesh is distributed evenly above all partial local power meshes.



EX1004, Fig. 1(b) (annotated); *see also id.*, Fig. 10 (showing evenly-distributed meshes); EX1003 ¶198. It would have been obvious for Li's global power mesh to be arranged in the same manner for the reasons discussed regarding claim 13. *See* §V.C.8.

12. Claim 19[preamble]: "A power routing arrangement method applied in an integrated circuit having multiple power domains, the arrangement method comprising:"

To the extent the preamble is limiting, it is obvious over Li for the same reasons discussed regarding claim 1. *See* §V.D.1; EX1003 ¶199.

13. Claim 19[a]: "providing a global power mesh, positioned above a first power domain and a second power domain, comprising at least one first power wire that provides the voltage needed by the first power domain, at least one second power wire that provides the voltage needed by the second power domain, and at least one ground wire that provides the ground potential needed by the first power domain and the second power domain by an automatic placement and routing (APR) tool;"

The combination discloses or renders obvious the global power mesh as claimed for the reasons discussed regarding limitation 12[c] and claims 13 and 15. *See* §§V.C.4, V.C.8, V.C.10; EX1003 ¶200.

It would have been obvious to provide this global power mesh and all other features of the power routing structure of claim 19 with an APR tool for the reasons provided with respect to claim 1. *See* §V.D.1; EX1003 ¶201.

14. Claim 19[b]: "coupling the first power wire and the ground wire of the global power mesh to the first power domain by the APR tool; and"

The combination renders obvious that the first power wire and ground wire are coupled to the first domain for the reasons discussed regarding claims 16 and 18. *See* §§V.C.11, V.C.13; EX1003 ¶202; *see also* §V.D.13 (describing obviousness of using APR tool).

15. Claim 19[c]: "coupling the second power wire and the ground wire of the global power mesh to the second power domain by the APR tool;"

The combination renders obvious that the second power wire and ground wire are coupled to the second power domain for the same reasons discussed regarding

the first power domain in claims 16-18 and 19(b). *See* §§V.C.11-13, V.D.14; EX1003 ¶203; *see also* §V.D.13V.D.13 (describing obviousness of using APR tool).

16. Claim 19[d]: "wherein the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer; and"

The combination discloses or renders this limitation obvious for the same reasons discussed regarding limitation 12[e]. *See* §V.C.6; EX1003 ¶204.

17. Claim 19[e]: "wherein the first metal layer and the second metal layer are different layers."

The combination discloses or renders this limitation obvious for the same reasons discussed regarding limitation 12[f]. *See* §V.C.7; EX1003 ¶205.

18. Claim 20: "The arrangement method according to claim 19, wherein the first power domain and the second power domain share the same ground wire of the global power mesh."

The combination discloses or renders this limitation obvious for the same reasons discussed regarding claim 18. *See* §V.C.13; EX1003 ¶206.

VI. DISCRETION UNDER 35 U.S.C. §§ 314(A) AND 325(D)

Discretionary denial is inappropriate under §§ 314(a) and 325(d).

A. Discretionary Denial Under § 314(a) Is Inappropriate Under the *Fintiv* Factors.

A final written decision in this proceeding will come long before any trial in the Northern District of California case because that case has been stayed pending the ITC investigation. EX1023. Further, the Director has instructed that the Board

"will not discretionarily deny petitions based on applying *Fintiv* to a parallel ITC proceeding." Director Memorandum, *Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation*, at 7 (June 21, 2022). Thus, there is no basis to discretionarily deny institution under § 314(a).

B. Discretionary Denial Under 35 U.S.C. § 325(d) Is Unwarranted.

Denial under § 325(d) is unwarranted because the challenges presented in this petition are neither cumulative nor redundant to the '218 Patent's prosecution. *Advanced Bionics, LLC, v. Med-El Elektromedizinische Gerate GMBH*, IPR2019-01469, Paper 6, 6-8 (P.T.A.B. Feb. 13, 2020) (precedential). None of the art relied upon in this petition was previously presented to the Office. EX1001, 1. Moreover, the challenges in this petition are non-cumulative of the art the Examiner relied upon during prosecution and plainly teach the features Patent Owner alleged were missing in the Examiner's cited art. EX1002, 135-39.

VII. GROUNDS FOR STANDING

Petitioner hereby certifies that the '218 Patent is available for IPR. Specifically, (1) Petitioner is not an owner of the '218 Patent, *see* 37 C.F.R. § 42.101; (2) before the date on which this Petition was filed, neither Petitioner nor Petitioner's real-parties-in-interest filed a civil action challenging the '218 Patent's validity, *see* § 42.101(a); (3) Petitioner has not filed this Petition more than one year after the date on which the Petitioner, Petitioner's real party-in-interest or a privy, were

served with a complaint alleging infringement of the '218 Patent, *see* § 42.101(b); and (4) Petitioner, Petitioner's real parties-in-interest, or a privy are not estopped from challenging the claims on the petitioned grounds, *see* § 42.101(c).

VIII. MANDATORY NOTICES

Pursuant to 37 C.F.R. § 42.8(a)(1), the mandatory notices identified in 37 C.F.R. § 42.8(b) are provided below as part of this Petition.

A. Real Party-in-Interest (37 C.F.R. § 42.8(b)(1))

Petitioner Advanced Micro Devices, Inc. is the real party-in-interest.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

Petitioner is currently aware of the following matters related to the '218 Patent: *Realtek Semiconductor Corp. v. Advanced Micro Devices, Inc.*, No. 5:22-cv-04769 (N.D. Cal. 2022), and *In re Certain Integrated Circuits, Components Thereof, and Products Containing the Same*, Inv. No. 337-TA-1350 (USITC).

C. Lead and Backup Counsel (37 C.F.R. § 42.8(b)(3))

Petitioner provides the following designation of counsel:

Lead Counsel	Backup Counsel
Douglas R. Wilson (Reg. No. 54,542) doug.wilson@armondwilson.com Postal and Hand-Delivery Address: ARMOND WILSON LLP 13785 Research Blvd., Suite 125 Austin, Texas 78750 Telephone: (512) 267-1663	Michelle E. Armond (Reg. No. 53,954) michelle.armond@armondwilson.com Josepher Li (Reg. No. 74,998) josepher.li@armondwilson.com Patrick Maloney (Reg. No. 67,247) patrick.maloney@armondwilson.com

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Pursuant to 37 C.F.R. § 42.10(b), a Power of Attorney accompanies this Petition.

D. Service Information (37 C.F.R. § 42.8(b)(4))

Service information for lead and back-up counsel is above. Petitioner hereby consents to service by email at the following email address: ipr@armondwilson.com.

IX. CONCLUSION

For the reasons set forth above, AMD requests judgment cancelling claims 1-20 of U.S. Patent No. 8,006,218.

ARMOND WILSON LLP

Date: May 8, 2023

By: /Douglas R. Wilson/
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Attorneys for Advanced Micro Devices, Inc.

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. §42.24(d), the undersigned certifies that foregoing **PETITION FOR INTER PARTES REVIEW OF U.S. PATENT NO. 8,006,218**, exclusive of the parts exempted as provided in 37 C.F.R. §42.24(a), contains 13,686 words and therefore complies with the type-volume limitations of 37 C.F.R. §42.24(a).

ARMOND WILSON LLP

Date: May 8, 2023

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Attorneys for Advanced Micro Devices, Inc.

CERTIFICATE OF SERVICE

I hereby certify that a true and correct copy of the foregoing **PETITION FOR INTER PARTES REVIEW OF U.S. PATENT NO. 8,006,218 and EXHIBITS 1001-1030**, are being served on May 8, 2023, via overnight mail on the patent owner at the correspondence address of record for U.S. Patent No. 8,006,218, as addressed below:

Muncy, Geissler, Olds & Lowe, P.C.
125 S. Royal St.
Alexandria, VA 22314

A courtesy copy is also being served by electronic mail on counsel for the patent holder in the pending litigation:

Theodore Angelis (theo.angelis@klgates.com)
Elizabeth Weiskopf (elizabeth.weiskopf@klgates.com)
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Date: May 8, 2023

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