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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	3722/0536PUS1
First Inventor	Chia-Lin CHUANG
Title	A POWER MESH ARRANGEMENT METHOD UTILIZED IN AN ... HAVING MULTIPLE POWER DOMAINS
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☒ **Fee Transmittal Form** (e.g., PTO/SB/17)
(Submit an original and a duplicate for fee processing)
2. ☐ **Applicant claims small entity status.**
See 37 CFR 1.27.
3. ☒ **Specification** [Total Pages 14]
Both the claims and abstract must start on a new page
(For information on the preferred arrangement, see MPEP 608.01(a))
4. ☒ **Drawing(s)** (35 U.S.C. 113) [Total Sheets 6]
5. **Oath or Declaration** [Total Sheets]
 - a. ☒ Newly executed (original or copy)
 - b. ☐ A copy from a prior application (37 CFR 1.63(d))
(for continuation/divisional with Box 18 completed)
 - i. ☐ **DELETION OF INVENTOR(S)**
Signed statement attached deleting inventor(s)
name in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. ☐ **Application Data Sheet.** See 37 CFR 1.76
7. ☐ **CD-ROM or CD-R** in duplicate, large table or Computer Program (Appendix)
☐ Landscape Table on CD
8. **Nucleotide and/or Amino Acid Sequence Submission**
(if applicable, items a. - c. are required)
 - a. ☐ Computer Readable Form (CRF)
 - b. **Specification Sequence Listing on:**
 - i. ☐ CD-ROM or CD-R (2 copies); or
 - ii. ☐ Paper
 - c. ☐ Statements verifying identity of above copies

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P.O. Box 1450
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ACCOMPANYING APPLICATION PARTS

9. ☐ **Assignment Papers** (cover sheet & document(s))
Name of Assignee _____
Realtek Semiconductor Corp.
10. ☐ **37 CFR 3.73(b) Statement** ☐ **Power of Attorney**
(when there is an assignee)
11. ☐ **English Translation Document** (if applicable)
12. ☐ **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
☐ Copies of citations attached
13. ☐ **Preliminary Amendment**
14. ☐ **Return Receipt Postcard** (MPEP 503)
(Should be specifically itemized)
15. ☐ **Certified Copy of Priority Document(s)**
(if foreign priority is claimed)
16. ☐ **Nonpublication Request** under 35 U.S.C. 122(b)(2)(B)(i).
Applicant must attach form PTO/SB/35 or equivalent.
17. ☒ **Other: Petition Under 37 C.F.R. 1.47(b)**

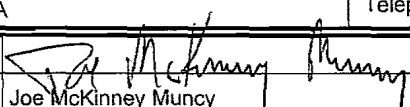
18. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: _____

Prior application information: Examiner _____ Art Unit: _____

19. CORRESPONDENCE ADDRESS

☒ The address associated with Customer Number: 60601 OR ☐ Correspondence address below

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This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).**FEE TRANSMITTAL**
For FY 2009☐ Applicant claims small entity status. See 37 CFR 1.27**TOTAL AMOUNT OF PAYMENT** (\$)1290.00**Complete if Known**

Application Number	NEW
Filing Date	November 14, 2008
First Named Inventor	Chia-Lin CHUANG
Examiner Name	Unknown
Art Unit	Unknown
Attorney Docket No.	3722/0536PUS1

METHOD OF PAYMENT (check all that apply)☐ Check ☒ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____☒ Deposit Account Deposit Account Number: 503828 Deposit Account Name: MG-IP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**☒ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☒ Credit any overpayments**WARNING:** Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.**FEE CALCULATION****1. BASIC FILING, SEARCH, AND EXAMINATION FEES**

Application Type	FILING FEES		SEARCH FEES		EXAMINATION FEES		Fees Paid (\$)
	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	
Utility	330	165	540	270	220	110	1090.00
Design	220	110	100	50	140	70	
Plant	220	110	330	165	170	85	
Reissue	330	165	540	270	650	325	
Provisional	220	110	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee (\$)	Small Entity Fee (\$)
Each claim over 20 (including Reissues)	52	26
Each independent claim over 3 (including Reissues)	220	110
Multiple dependent claims	390	195

Total Claims	Extra Claims	Fee (\$)	Fee Paid (\$)	Multiple Dependent Claims
20 - 20 or HP = 0	x	=	0	

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims	Extra Claims	Fee (\$)	Fee Paid (\$)
3 - 3 or HP = 0	x	=	0

HP = highest number of independent claims paid for, if greater than 3.

3. APPLICATION SIZE FEE

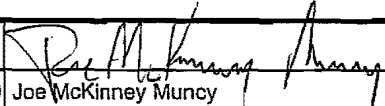
If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee (\$)	Fee Paid (\$)
20 - 100 = 0	/ 50 =	(round up to a whole number) x	=	

4. OTHER FEE(S)

Non-English Specification, \$130 fee (no small entity discount)

Other (e.g., late filing surcharge): Petition Under 37 CFR 1.117(g) 200.00**SUBMITTED BY**

Signature		Registration No. (Attorney/Agent) 32,334	Telephone 703-621-7140
Name (Print/Type)	Joe McKinney Muncy		Date November 14, 2008

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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AMD EX1002

AMD v. Realtek

Page 2

A Power Mesh Arrangement Method Utilized In An Integrated Circuit Having Multiple Power Domains

Background of the invention

(a) Field of the Invention

[0001] The invention relates to a power mesh arrangement method, particular to a power mesh arrangement method applied in an integrated circuit having multiple power domains.

(b) Description of the Related Art

[0002] As the circuitry of the integrated circuit becomes more and more complicate, there are possibilities that different portions of the circuitry of a chip need different voltages (powers) at the same time. For example, the chip circuitry may have two kinds of operating modes: the normal operating mode and the sleeping mode. During the normal operating mode, the entire chip circuitry uses the operating voltage for its normal operation. But during the sleeping mode, only part of the chip circuitry needs to be maintained in the normal operating mode. Therefore, the normal operating voltage is still used by these circuits for its operation while the other circuits of the chip only need a lower voltage for maintaining the sleeping mode operation.

[0003] Therefore, different powers need to be supplied to the different circuits inside the chip so that the circuits can perform different operations during the sleeping mode. Hence, it is common practices to arrange multiple power domains in the chip circuitry. In other words, circuits in different power domains are coupled to different powers respectively so that the circuits of different power domains use different powers to support the different operations that are just mentioned.

[0004] But, the traditional circuit design approach does not provide a simple rule or step for the circuit designer to plan and design the power routing of a circuit having multiple power domains. For example, the well-known automatic placement and routing (APR) tool can only support circuits having single power domain. Therefore, a circuit designer can only rely on the most primitive method to design the power routing of multiple power domains, such as the manual routing. Obviously, such design approach is not only complicated but also inefficient.

BRIEF SUMMARY OF THE INVENTION

[0005] Therefore, one object of the invention is to provide a power mesh arrangement method for the user to design power meshes having multiple power domains more easily and to solve the problems in the prior art.

[0006] One embodiment of the invention discloses a power routing arrangement method utilized in an integrated circuit having multiple power domains. The arrangement method includes: forming a first local power mesh according to the position of a first power domain; forming a second local power mesh according to the position of a second power domain; forming a global power mesh utilized for providing powers needed by the first and the second power domains; coupling the first local power mesh to the global power mesh and the first power domain; and coupling the second local power mesh to the global power mesh and the second power domain.

[0007] Another embodiment of the invention discloses a power routing structure applicable to an integrated circuit having multiple power domains. The power mesh structure includes: a first local power mesh coupling to a first power domain; a second local power mesh coupling to a second power domain; and a global power mesh coupling to the first power domain and the second power domain to provide powers needed by the first power domain and the second domain respectively.

[0008] Another embodiment of the invention discloses a power routing structure applicable to an integrated circuit having multiple power domains. The power routing structure includes a global power mesh that is positioned above a first power domain and a second power domain. The global power mesh comprises: at least one ground wire coupling to the first power domain and the second power domain to provide the ground potential needed by the first power domain and the second power domain; at least one first power wire coupling to the first power domain to provide the voltage needed by the first power domain; and at least one second power wire coupling to the second power domain to provide the voltage needed by the second power domain.

[0009] Another embodiment of the invention discloses a power routing arrangement method

utilized in an integrated circuit having multiple power domains. The arrangement method includes the following steps. At first, a global power mesh, positioned above a first power domain and a second power domain, that comprises at least one ground wire, at least one first power wire, and at least one second power wire, is provided. The first power wire provides the voltage needed by the first power domain, the second power wire provides the voltage needed by the second power domain, and the ground wire provides the ground potential needed by the first power domain and the second power domain. Then, the first power wire and the ground wire of the global power mesh are coupled to the first power domain. Finally, the second power wire and the ground wire of the global power mesh are coupled to the second power domain.

[0010] The invention provides a power mesh arrangement method and the related structure thereof for a user to easily complete the design of the power mesh of an integrated circuit having multiple power domains by following the arrangement method and its related structure. Besides, the power mesh arrangement method disclosed in the invention can be implemented in the APR tool easily so that the user can use the APR tool to automatically complete the circuit layout so as to increase the circuit design efficiency.

Brief description of the drawings

[0011] FIG. 1 shows a schematic diagram illustrating a chip having multiple power domains;

[0012] FIG. 2 shows the flow chart of the power routing arrangement method according to one embodiment of the invention;

[0013] FIG. 3 shows a schematic diagram illustrating a local power mesh according to one embodiment of the chip in FIG. 1;

[0014] FIG. 4 shows a schematic diagram illustrating a global power mesh according to one embodiment of the invention;

[0015] FIG. 5 shows a schematic diagram illustrating the relative positions of the local power mesh in FIG. 3 and the global power mesh in FIG. 4; and

[0016] FIG. 6 shows a schematic diagram illustrating the top view of the local power mesh in FIG. 3 and the global power mesh in FIG. 4.

DETAILED DESCRIPTION OF THE INVENTION

[0017] Please refer to FIG. 1 which 1 illustrates a chip 100 having multiple power domains. As shown in FIG. 1, the chip 100 has two different kinds of power domains 110, 120 where the power domain 110 is illustrated by the blank area and the power domain 120 is illustrated by the oblique line area.

[0018] As mentioned before, the power domains 110, 120 correspond to different powers that supply different voltages to the different circuits of the different power domains. It should be noted that, in the subsequent disclosure, the invention provides a power routing arrangement method and its related structure so that the user can complete the design of the power routing more easily.

[0019] FIG. 2 shows the flow chart of the power routing arrangement method according to one embodiment of the invention. The arrangement method of the invention comprises the following steps:

Step 200: arranging a first local power mesh according to the position of the power domain 110;

Step 210: arranging a second local power mesh according to the position of the power domain 120; and

Step 220: arranging a global power mesh that is positioned above the first local power mesh and the second local power mesh.

[0020] It should be noted that the invention utilizes the local power mesh and the global power mesh to form the power routing of the power domains 110, 120. Each of the local power meshes is placed according to the positions of the power domains 110, 120 respectively (Step 200, Step 210) and the global power mesh is distributed evenly above the local power meshes (Step 220). The global power mesh couples to the external power (such as: by way of the I/O pin of the chip) to conduct the external power into the chip while the local power mesh couples to the global power mesh and the chip circuitry (that is the internal circuits of the chip corresponding to the power domains 110, 120). Then, the external power will be inputted into the chip circuitry by way of the global power mesh and the local power meshes.

[0021] Please refer to FIG. 3 which shows a schematic diagram illustrating a local power mesh according to one embodiment of the invention. As shown in FIG. 3, the local power mesh can be partitioned into two different partial local power meshes 310, 320 at the positions corresponding to the positions of the power domains 110, 120. In one embodiment of the invention, the partial local power mesh 310 is placed on top of the power domain 110 and the partial local power mesh 320 is placed on top of the power domain 120. Thus, the partial local power meshes 310, 320 can couple to the power domains 110, 120 positioned below by way of the via holes (“via”).

[0022] Besides, as shown in FIG. 3, the partial local power meshes 310, 320 comprise web-like structures. It should be noted that the partial local power meshes 310, 320 are not interconnected (which means that the partial local power meshes 310, 320 are mutually insulated) to avoid mutual short-circuit that induces electrical uncertainty. Each of the partial local power meshes 310, 320 comprises a plurality of horizontal power supply wires and a plurality of vertical power supply wires. Please note that, as each of the partial local power meshes 310, 320 is only used to supply the powers needed by the power domains 110, 120, each of the horizontal and the vertical power supply wires only needs to comprise one ground wire and one power wire. For example, the partial local power meshes 310 comprises a power wire 311 to supply the working voltage V_{DD1} needed by the power domain 110 and a ground wire 312 to supply the ground potential V_{GND} needed by the power domain 110. On the other hand, the partial local power meshes 320 comprises a power wire 321 to supply the working voltage V_{DD1} needed by the power domain 120 and a ground wire 322 to supply the ground potential V_{GND} needed by the power domain 120.

[0023] As shown in FIG. 3, the power wire 311 and the ground wire 312 are drawn very close to each other, so are the power wire 321 and the ground wire 322. However, please note that the power wire 311 and the ground wire 312 do not touch each other (which means that the power wire 311 and the ground wire 312 are not electrically coupled) to avoid short-circuit that induces electrical uncertainty. Similarly, the power wire 321 and the ground wire 322 are also not electrically coupled to each other to avoid short-circuit that induces electrical uncertainty.

[0024] However, the above mentioned local power mesh 300 can be implemented by those

who are skilled in the art without difficulty. Generally speaking, one single metal layer is used to place only one directional routing (such as the above mentioned horizontal power supply wire or the vertical power supply wire) and the routing directions of two adjacent metal layers are mutually different. Thus, the embodiments of the invention can utilize adjacent metal layers to place the above mentioned local power mesh 300. Besides, the power wires and ground wires of adjacent metal layers having the same electrical property can be interconnected to each other by via.

[0025] Please refer to FIG. 4 which shows a schematic diagram illustrating a global power mesh 400 according to one embodiment of the invention. As shown in FIG. 4, the global power mesh 400 also comprises a web-like structure. Each global power mesh also comprises a plurality of horizontal power supply wires and a plurality of vertical power supply wires that are evenly distributed on top of the chip circuitry. In one embodiment of the invention, the global power mesh 400 is distributed just above the local power mesh 300 so that the global power mesh 400 can conduct the external power into the chip by via to couple to the local power mesh 300 located below.

[0026] Similarly, as the global power mesh 400 is to supply voltage to the entire chip, each of the horizontal and the vertical power supply wires must comprise one common ground wire 403 and two power wires 401, 402. The common ground wire 403 is used to supply the ground potential V_{GND} needed by the local power meshes 310, 320. The two power wires 401, 402 are used to supply the working voltages V_{DD1} , V_{DD2} needed by the local power meshes 310, 320, respectively.

[0027] Similarly, the global power mesh 400 can be implemented by those who are skilled in the art without difficulty. The embodiments of the invention can utilize adjacent metal layers to place the global power mesh 400. Besides, the power wires and the ground wires of adjacent metal layers having the same electrical property can be interconnected to each other by via.

[0028] Please refer to FIG. 5 which shows a schematic diagram illustrating the positions of the global power mesh 400 and the local power mesh 300 according to one embodiment of the invention. As shown in FIG. 5, the global power mesh 400 is placed above the local power mesh 300 and the partial local power meshes 310, 320 of the local power mesh are placed

separately above each power domain.

[0029] As mentioned previously, two metal layers are needed to implement either the global power mesh 400 or the local power mesh 300. In other words, the embodiments of the invention need at least four metal layers to implement the above mentioned global power mesh 400 and the local power mesh 300. However, at least four metal layers (such as: M5, M6, M7, M8 shown in FIG. 5) are generally reserved for interconnecting the conductive wires of the nodes inside the chip in advanced manufacturing processes. Therefore, the embodiments of the invention can utilize these metal layers to implement the global power mesh 400 and the local power mesh 300. For example, among the metal layers M5 ~ M8, the local power mesh 300 can be implemented on the lower metal layers M5 ~ M6 (such as one embodiment of the invention shown in FIG. 3: the horizontal power supply wire is placed on the metal layer M5 and the vertical power supply wire is placed on the metal layer M6). Then, the global power mesh 400 can be implemented on the corresponding metal layer M7 ~ M8 located above (similarly, such as one embodiment of the invention shown in FIG. 4: the horizontal power supply wire is placed on the metal layer M7 and the vertical power supply wire is placed on the metal layer M8).

[0030] Please refer to FIG. 6 which shows a schematic diagram illustrating the top view of the global power mesh 400 and the local power mesh 300. In one embodiment of the invention, the power supply wire 401 that couples to the external power V_{DD1} uses via (not shown in the figure) to couple to the power wire 311 located below so as to conduct the external power V_{DD1} to the chip circuitry. The power supply wire 403 that couples to the external power V_{DD2} uses via to couple to the power wire 321 located below so as to conduct the external power V_{DD2} to the chip circuitry. On the other hand, the common ground wire 402 also conducts the external ground potential V_{GND} to the chip circuitry by coupling to the ground wires 311, 312 located below by way of the via.

[0031] Thus, as the density of the global power mesh 400 and the partial local power meshes 310, 320 are sufficiently high, the mutually connecting relation between the global power mesh 400 and the partial local power meshes 310, 320 located below is guaranteed. Therefore, when the partial local power meshes 310, 320 are connected to the internal circuits in each of the power domains 110, 120, it is assured that the external powers V_{DD1}, V_{DD2} are definitely

inputted into the chip circuitry.

[0032] Besides, such structure still has other benefits. As was well-known by those who are skilled in the art, the lower metal layers are generally used for the placement of metal wires that connect the chip internal nodes, compared to the higher metal layers. Hence, the area of the lower metal layers are more precious than that of the higher metal layers. In the embodiments of the invention, the local power mesh 300 that utilizes less power supply wires (just one power wire and one ground wire) is designed to occupy less area in the lower metal layers M5, M6. The global power mesh 400 that utilizes more power supply wires (two power wires and one common ground wire) is placed in the more spacious higher metal layers M7 ~ M8 so that the area of the metal layers M5 ~ M6 can be released for the routing arrangement of other metal wires.

[0033] Based on the technical content disclosed in the invention so far, those who are skilled in the art should be able to understand and implement the above mentioned arrangement method and its related structure. For example, those who are skilled in the art can convert the arrangement method into an algorithm and build such an algorithm into a power routing development environment (such as the above mentioned APR tool) so that the APR tool can support the power routing design with multiple power domains.

[0034] As mentioned previously, the partial local power meshes 310, 320 have the positions corresponding to the positions of the power domains 110, 120 and are not electrically coupled to each other (that is, the partial local power meshes 310, 320 are insulated from each other) according to this embodiment of the invention. Thus, the following will describe a simple algorithm for the APR tool. Firstly, the local power mesh 300 is evenly distributed on top of the entire chip circuitry. Then, the partial local power meshes in the local power mesh 300 corresponding to the power domains 110, 120 are defined (such as partitioning the local power mesh 300 based on the positions of the power domains 110, 120 so that the plurality of partitioned power meshes are not electrically coupled to each other) to form the above mentioned partial local power meshes 310, 320. On the other hand, the approach to form the global power mesh 400 is much easier for the APR tool by just evenly distributing the global power mesh 400 on metal layers that are positioned higher.

[0035] Based on the above disclosure, those who are skilled in the art should be able to

develop a suitable APR tool to draw the power mesh automatically to thereby increase the circuit design efficiency.

[0036] It should be noted that the arrangement method and its related structure disclosed is just a preferred example of the invention and should not be construed as any limitation on the implementation of the invention. The local power mesh 300 can be omitted in the invention. Only the global power mesh 400 is used to conduct the external power into the chip. For example, the global power mesh 400 can be placed on the metal layers M5, M6 directly as shown in FIG. 4. If the density of the global power mesh is high enough as mentioned previously, it can be assured that all the circuits in the chip positioned below can be coupled to the global power mesh 400 by via to receive the ground potential V_{GND} and the working voltage V_{DD1} , V_{DD2} conducted by the global power mesh 400. Such equivalent changes and modifications of the present invention are considered to be within the scope of the present invention.

[0037] It is relatively easy to implement such structure during the design of the APR tool. For example, the APR tool just needs to evenly distribute the power mesh in the metal layers M5, M6 directly. Based on the disclosure up to now, those who are skilled in the art should be able to understand and implement the necessary APR tool and the power mesh. Therefore, further details related to the development of the APR tool will not be discussed hereinafter.

[0038] It should be noted that in comparison with the embodiment of the invention illustrated in FIG. 6, implementing the global power mesh that comprises two power wires and one common ground wire directly in the metal layers M5, M6 will consume a larger area on the metal layers M5, M6. But, as the global power mesh uses only one common ground wire to supply the ground potential to the various power domains, such implementation will not waste excess large area.

[0039] Compared to the prior art, the invention provides a power mesh arrangement method and its related structure so that a user can easily complete the design of the power mesh for an integrated circuit having multiple power domains by following the arrangement method and its related structure described in the invention. Besides, the arrangement method disclosed in the invention can be implemented in the APR tool easily so that a user can use the APR tool to automatically complete the drawing of the circuit layout. Therefore, the efficiency for circuit

design is increased.

[0040] Although the description of the invention is by way of above-mentioned examples of embodiment, however, it should not be construed as any limitation on the scope of the invention. Various modifications or changes can be performed by those who are skilled in the art without deviating from the scope of the invention.

WHAT IS CLAIMED IS:

1. A power routing arrangement method applied in an integrated circuit having multiple power domains, the arrangement method comprising:

forming a first partial local power mesh according to the position of a first power domain of the integrated circuit;

forming a second partial local power mesh according to the position of a second power domain of the integrated circuit;

forming a global power mesh that is utilized to provide the power needed by the first and the second power domains;

coupling the first partial local power mesh to the global power mesh and the first power domain; and

coupling the second partial local power mesh to the global power mesh and the second power domain.

2. The arrangement method according to claim 1, wherein the first partial local power mesh and the second partial local power mesh are positioned on the same metal layer.

3. The arrangement method according to claim 2, wherein the global power mesh and the first local power mesh are positioned on different metal layers.

4. The arrangement method according to claim 3, wherein the global power mesh is positioned above the first local power mesh.

5. The arrangement method according to claim 2, wherein the first partial local power mesh and the second partial local power mesh are not electrically coupled.

6. The arrangement method according to claim 1, wherein the global power mesh comprises at least one ground wire, at least one first power wire that provides power to the first power domain, and at least one second power wire that provides power to the second power domain.

7. The arrangement method according to claim 6, wherein the first partial local power mesh comprises: at least one first local ground wire that couples to the ground wire of the global power mesh; and at least one third power wire that couples to the first power wire and the first power domain.

8. The arrangement method according to claim 7, wherein the second partial local power

mesh comprises: at least one second local ground wire that couples to the ground wire of the global power mesh; and at least one fourth power wire that couples to the second power wire and the second power domain.

9. The arrangement method according to claim 8, wherein the first local ground wire and the second local ground wire share the same ground wire of the global power mesh.

10. The arrangement method according to claim 1, wherein the positions of the first partial local power mesh and the second partial local power mesh correspond to the first power domain and the second power domain, respectively.

11. The arrangement method according to claim 1, wherein the global power mesh is distributed evenly above the first local power mesh and the area of the second local power mesh.

12. A power routing structure applied in an integrated circuit having multiple power domains, comprising:

- a first partial local power mesh having its position corresponding to the position of a first power domain and coupling to the first power domain;

- a second partial local power mesh having its position corresponding to the position of a second power domain and coupling to the second power domain; and

- a global power mesh, coupling to the first local power mesh and the second local power mesh, to provide the power needed by the first power domain and the second domain separately;

wherein the first partial local power mesh and the second partial local power mesh are positioned on the same metal layer while the global power mesh and the first local power mesh are positioned on different metal layers.

13. The power routing structure according to claim 12, wherein the global power mesh is positioned above the first local power mesh.

14. The power routing structure according to claim 13, wherein the first local power mesh and the second local power mesh are not electrically coupled.

15. The power routing structure according to claim 12, wherein the global power mesh comprises: at least one ground wire; at least one first power wire that provides the power needed by the first power domain; and at least one second power wire that provides the power

needed by the second power domain.

16. The power routing structure according to claim 15, wherein the first partial local power mesh comprises: at least one first local ground wire that couples to the ground wire of the global power mesh; and at least one third power wire that couples to the first power wire and the first power domain.

17. The power routing structure according to claim 16, wherein the second partial local power mesh comprises: at least one second local ground wire that couples to the ground wire of the global power mesh; and at least one fourth power wire that couples to the second power wire and the second power domain.

18. The power routing structure according to claim 17, wherein the first local ground wire and the second local ground wire share the same ground wire of the global power mesh.

19. A power routing arrangement method applied in an integrated circuit having multiple power domains, the arrangement method comprising:

providing a global power mesh, positioned above a first power domain and a second power domain, comprising at least one first power wire that provides the voltage needed by the first power domain, at least one second power wire that provides the voltage needed by the second power domain, and at least one ground wire that provides the ground potential needed by the first power domain and the second power domain;

coupling the first power wire and the ground wire of the global power mesh to the first power domain; and

coupling the second power wire and the ground wire of the global power mesh to the second power domain.

20. The arrangement method according to claim 19, wherein the first power domain and the second power domain share the same ground wire of the global power mesh.

A Power Mesh Arrangement Method Utilized In An Integrated Circuit Having Multiple Power Domains

ABSTRACT OF THE INVENTION

[0041] The invention discloses a power mesh arrangement method utilized in an integrated circuit having multiple power domains. The arrangement method includes: forming a first partial local power mesh according to a position of a first power domain; forming a second partial local power mesh according to a position of a second power domain; forming a global power mesh, utilized for providing powers needed by the first and the second power domains; coupling the first partial local power mesh to the global power mesh and the first power domain; and coupling the second partial local power mesh to the global power mesh and the second power domain.

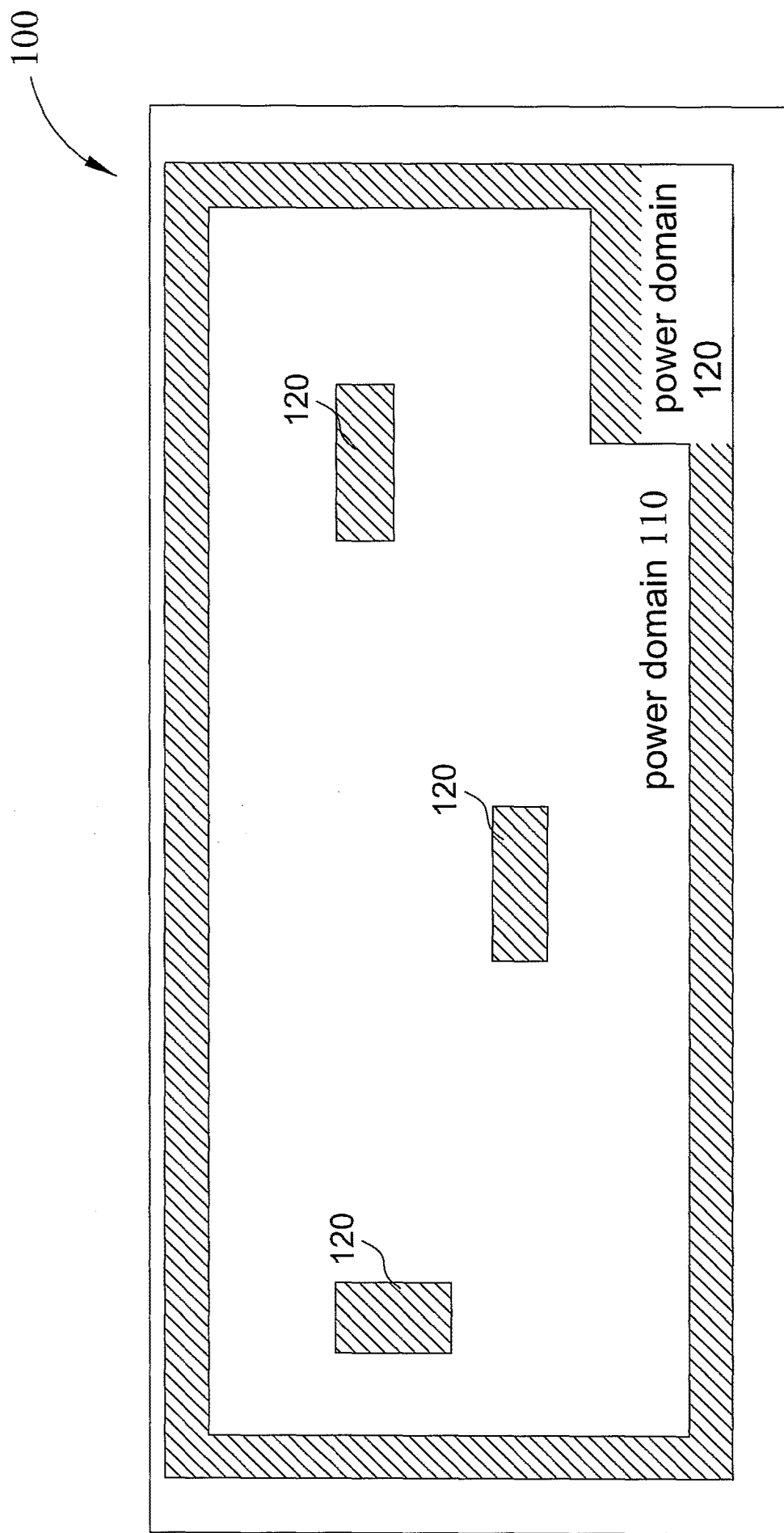


FIG. 1

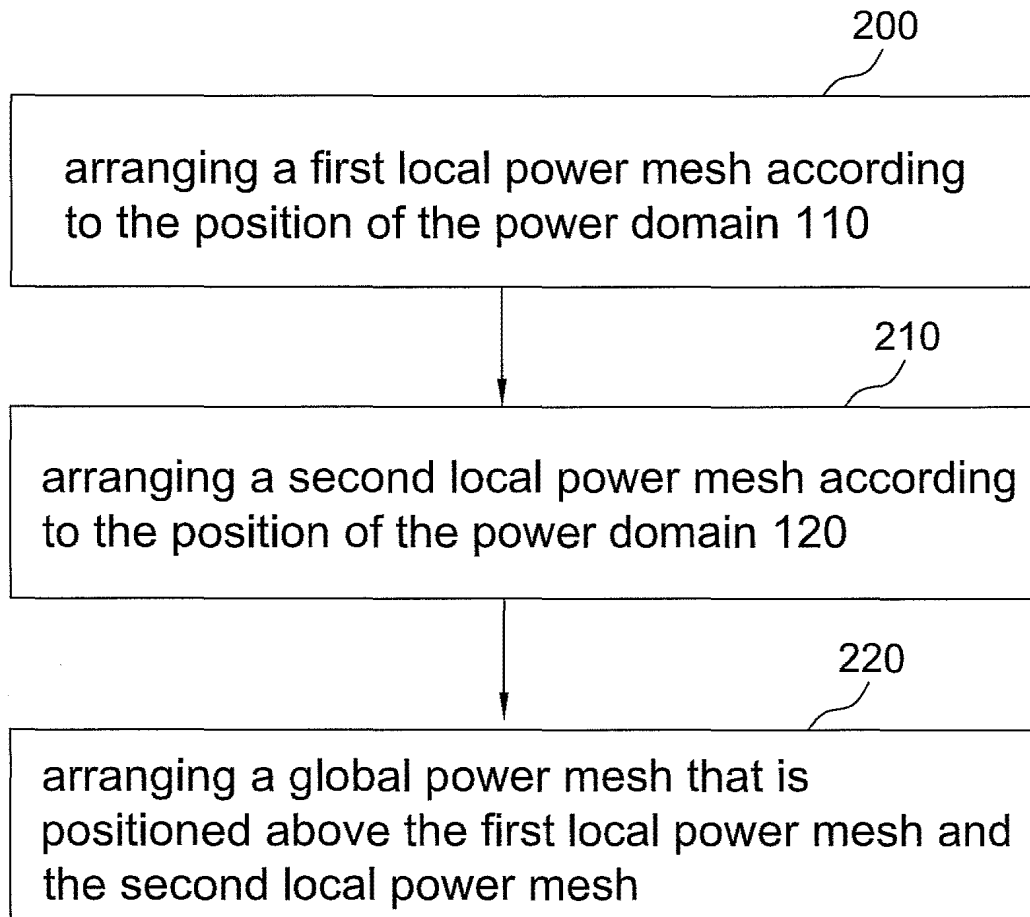


FIG. 2

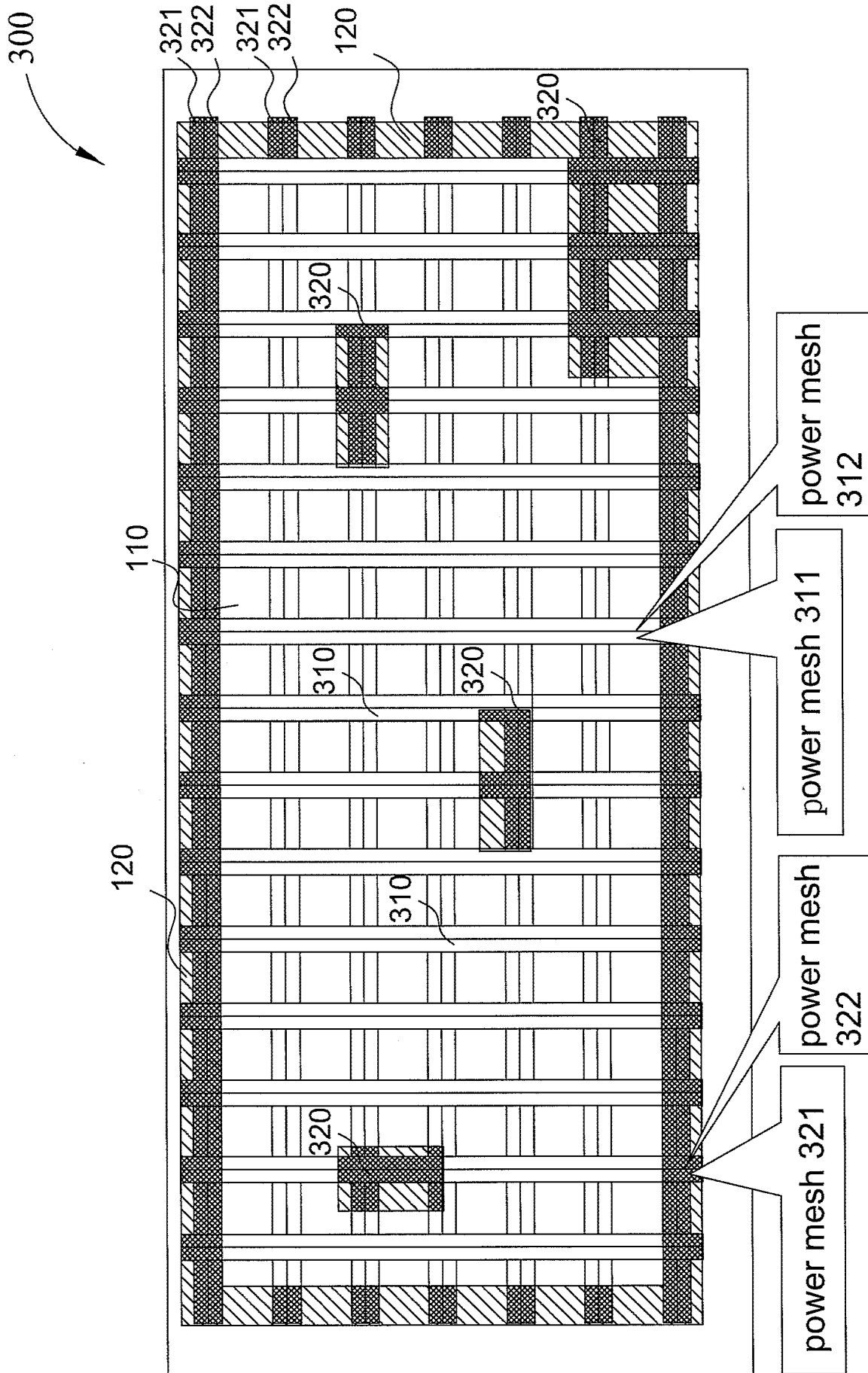


FIG. 3

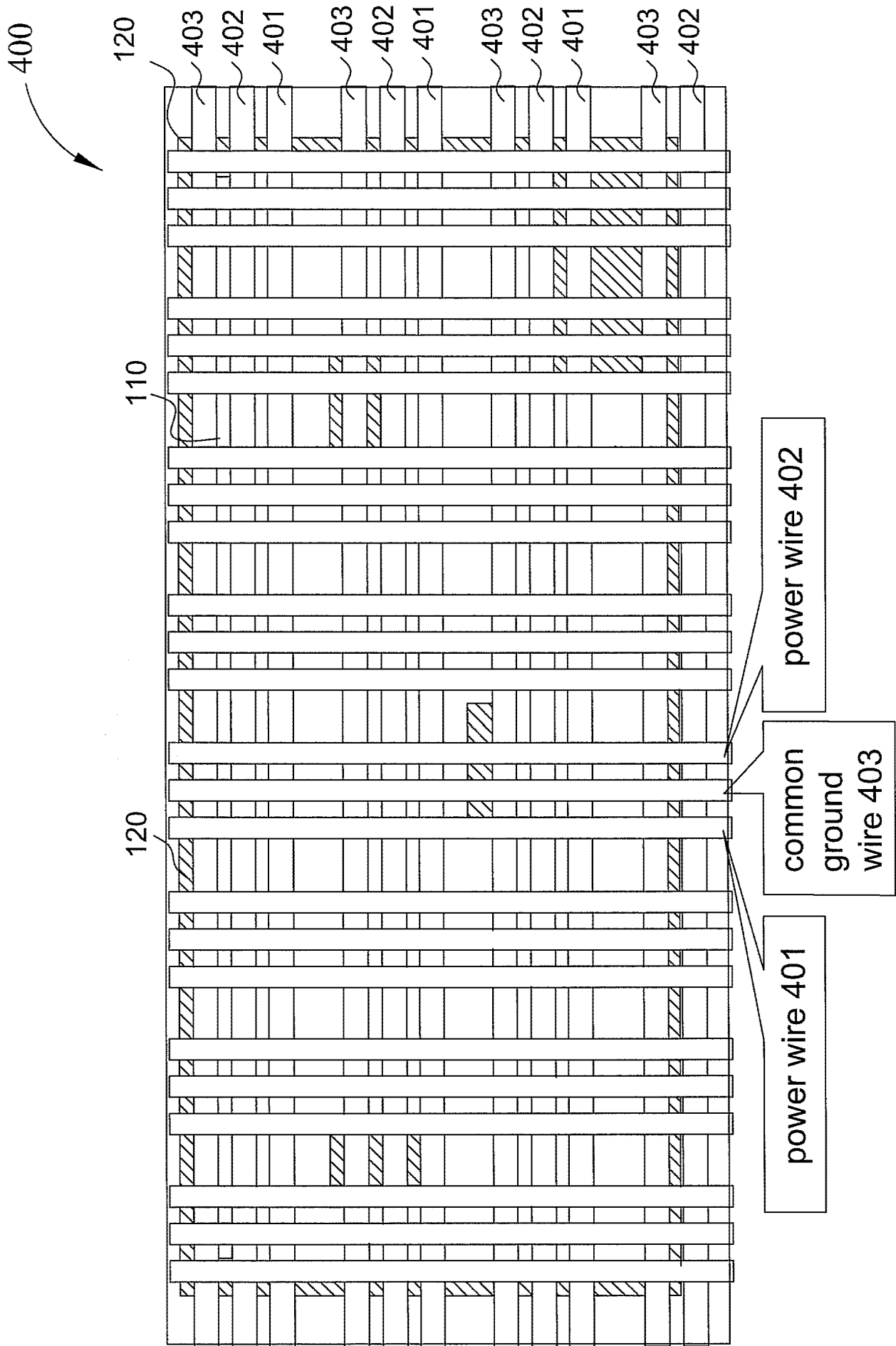


FIG. 4

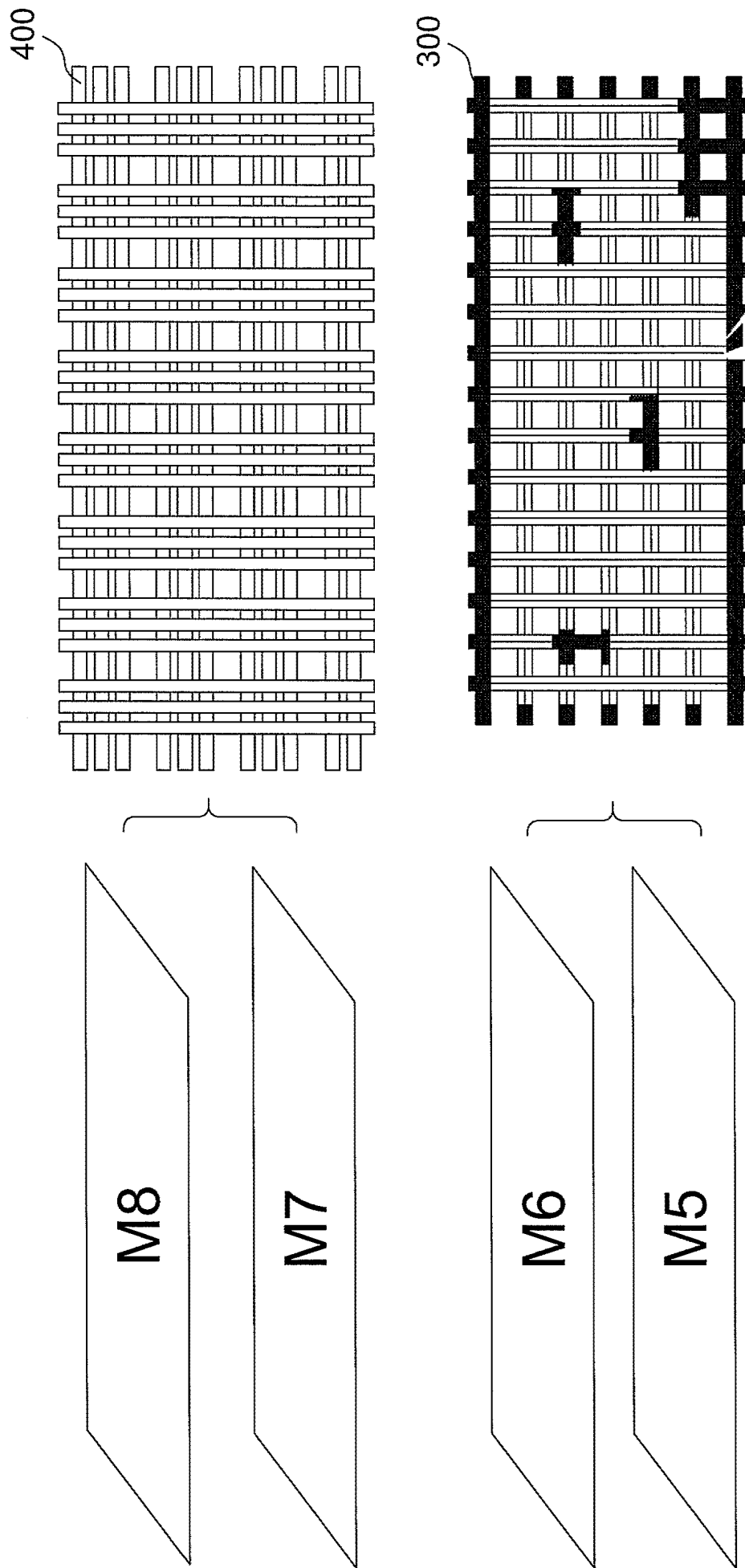


FIG. 5

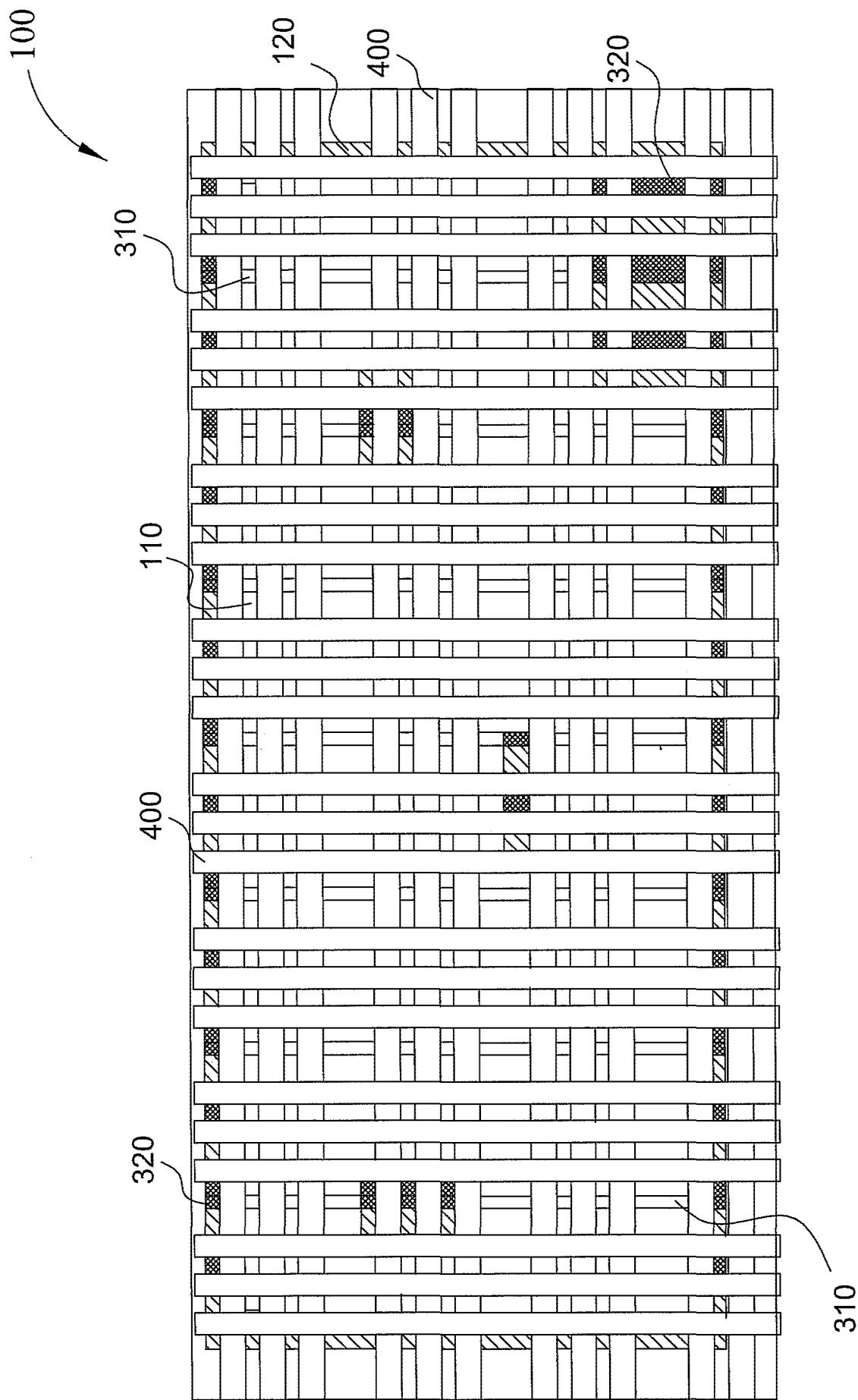


FIG. 6

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	3722/0536PUS1
First Inventor	Chia-Lin CHUANG
Title	A POWER MESH ARRANGEMENT METHOD UTILIZED IN AN ... HAVING MULTIPLE POWER DOMAINS
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☒ **Fee Transmittal Form** (e.g., PTO/SB/17)
(Submit an original and a duplicate for fee processing)
2. ☐ **Applicant claims small entity status.**
See 37 CFR 1.27.
3. ☒ **Specification** [Total Pages 14]
Both the claims and abstract must start on a new page
(For information on the preferred arrangement, see MPEP 608.01(a))
4. ☒ **Drawing(s)** (35 U.S.C. 113) [Total Sheets 6]
5. **Oath or Declaration** [Total Sheets]
 - a. ☒ Newly executed (original or copy)
 - b. ☐ A copy from a prior application (37 CFR 1.63(d))
(for continuation/divisional with Box 18 completed)
 - i. ☐ **DELETION OF INVENTOR(S)**
Signed statement attached deleting inventor(s)
name in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. ☐ **Application Data Sheet.** See 37 CFR 1.76
7. ☐ **CD-ROM or CD-R** in duplicate, large table or Computer Program (Appendix)
☐ Landscape Table on CD
8. **Nucleotide and/or Amino Acid Sequence Submission**
(if applicable, items a. - c. are required)
 - a. ☐ Computer Readable Form (CRF)
 - b. **Specification Sequence Listing on:**
 - i. ☐ CD-ROM or CD-R (2 copies); or
 - ii. ☐ Paper
 - c. ☐ Statements verifying identity of above copies

ADDRESS TO: Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

ACCOMPANYING APPLICATION PARTS

9. ☐ **Assignment Papers** (cover sheet & document(s))
Name of Assignee _____
Realtek Semiconductor Corp.
10. ☐ **37 CFR 3.73(b) Statement** ☐ **Power of Attorney**
(when there is an assignee)
11. ☐ **English Translation Document** (if applicable)
12. ☐ **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
☐ Copies of citations attached
13. ☐ **Preliminary Amendment**
14. ☐ **Return Receipt Postcard** (MPEP 503)
(Should be specifically itemized)
15. ☐ **Certified Copy of Priority Document(s)**
(if foreign priority is claimed)
16. ☐ **Nonpublication Request** under 35 U.S.C. 122(b)(2)(B)(i).
Applicant must attach form PTO/SB/35 or equivalent.
17. ☒ **Other: Petition Under 37 C.F.R. 1.47(b)**

18. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76:

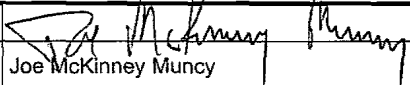
☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: _____

Prior application information: Examiner _____ Art Unit: _____

19. CORRESPONDENCE ADDRESS

☒ The address associated with Customer Number: 60601 OR ☐ Correspondence address below

Name	Muncy, Geissler, Olds & Lowe, PLLC				
Address	PO Box 1364				
City	Fairfax	State	VA	Zip Code	22038-1364
Country	USA	Telephone	703-621-7140	Email	mailroom@mg-ip.com

Signature		Date	November 14, 2008
Name (Print/Type)	Joe McKinney Muncy	Registration No. (Attorney/Agent)	32,334

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).**FEE TRANSMITTAL**
For FY 2009☐ Applicant claims small entity status. See 37 CFR 1.27**TOTAL AMOUNT OF PAYMENT** (\$)1290.00**Complete if Known**

Application Number	NEW
Filing Date	November 14, 2008
First Named Inventor	Chia-Lin CHUANG
Examiner Name	Unknown
Art Unit	Unknown
Attorney Docket No.	3722/0536PUS1

METHOD OF PAYMENT (check all that apply)☐ Check ☒ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____☒ Deposit Account Deposit Account Number: 503828 Deposit Account Name: MG-IP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**☒ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☒ Credit any overpayments**WARNING:** Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.**FEE CALCULATION****1. BASIC FILING, SEARCH, AND EXAMINATION FEES**

Application Type	FILING FEES		SEARCH FEES		EXAMINATION FEES		Fees Paid (\$)
	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	
Utility	330	165	540	270	220	110	1090.00
Design	220	110	100	50	140	70	
Plant	220	110	330	165	170	85	
Reissue	330	165	540	270	650	325	
Provisional	220	110	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee (\$)	Small Entity Fee (\$)
Each claim over 20 (including Reissues)	52	26
Each independent claim over 3 (including Reissues)	220	110
Multiple dependent claims	390	195

Total Claims	Extra Claims	Fee (\$)	Fee Paid (\$)	Multiple Dependent Claims
20 - 20 or HP = 0	x	=	0	

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims	Extra Claims	Fee (\$)	Fee Paid (\$)
3 - 3 or HP = 0	x	=	0

HP = highest number of independent claims paid for, if greater than 3.

3. APPLICATION SIZE FEE

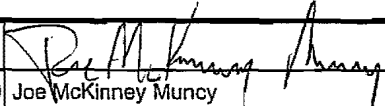
If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee (\$)	Fee Paid (\$)
20 - 100 = 0	/ 50 =	(round up to a whole number) x	=	

4. OTHER FEE(S)

Non-English Specification, \$130 fee (no small entity discount)

Other (e.g., late filing surcharge): Petition Under 37 CFR 1.117(g) 200.00**SUBMITTED BY**

Signature		Registration No. (Attorney/Agent) 32,334	Telephone 703-621-7140
Name (Print/Type)	Joe McKinney Muncy	Date November 14, 2008	

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

AMD EX1002

AMD v. Realtek

Page 24

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Chuang, Chia-Lin	Examiner:
Application No.:	Art Unit:
Filed:	Confirmation Number:
Title: A power mesh arrangement method utilized in an integrated circuit having multiple power domains	
Attorney Docket No.: 3722/0536PUS1	

MS PETITION

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

PETITION UNDER 37 C.F.R § 1.47(b)

Dear Sir:

This petition is for Realtek Semiconductor Corporation to make the application on behalf of the non-signing inventor, Chia-Lin CHUANG.

1. Declaration

Attached is a Declaration listing the non-signing inventor's name, residence, citizenship, and last known address, and signed by Chao-Cheng Lee, VP of Engineering for Realtek Semiconductor Corporation.

2. Proof of Proprietary Interest

Attached is a copy of an employment agreement and English translation thereof, wherein the non-signing inventor agrees to assign to his employer all inventions made during employment. Also, on the attached "Notice for Signature of Patent Documents" (in Chinese and English), Xing-Ci Tien confirms that the present invention was invented by Chia-Lin CHUANG during his employment at Realtek Semiconductor Corporation. On

the attached "Release Certificate," the dates of Chia-Lin CHUANG's employment with Realtek Semiconductor Corporation are confirmed.

It is noted that the present application is identified on various documents as "96A-022," "A power mesh arrangement method utilized in an integrated circuit having multiple power domains," and "YAPTO Ref. No. 07P040-US."

3. Proof of the Pertinent Facts

Attached is a Statement of Facts signed by Xing-Ci Tien, an IP and Legal Dept. Assistant of Realtek Semiconductor Corporation, setting forth the pertinent facts regarding the non-signing inventor's refusal to sign the Declaration. In this Statement of Facts, Xing-Ci Tien sets forth that a diligent effort was made to have insert name of non-signing inventor sign the Declaration, but that Chia-Lin CHUANG expressly refused to sign the Declaration, and that the executed documents were not received from Chia-Lin CHUANG.

In support of this Statement of Facts, attached is a copy of July 29, 2008 e-mail to the non-signing inventor, together with an English translation thereof, forwarding the papers to be signed, and requesting their return.

Also attached are a copy of a letter dated August 6, 2008 ("Notice for Signature of Patent Documents") forwarding a copy of the application to the non-signing inventor, together with an English translation thereof. A copy of the postal "Acknowledge of Receipt" for this letter, together with an English translation thereof, confirming delivery of the papers to the non-signing inventor, is also attached.

4. Proof that Action is Necessary to Preserve the Rights of the Parties or to Prevent Irreparable Damage

The present application claims priority of insert country of priority application Application No. 096143160 filed in Taiwan, R.O.C. on Nov. 15, 2007. Accordingly, a filing date is necessary to make a claim for priority under 35 U.S.C. § 119.

5. Inventor's Last Known Address

The inventor's last known address is as follows:

Chia-Lin Chuang
167-1, Changchun St.
300 Hsinchu City, Taiwan, R.O.C.

6. Fee Payment (37 C.F.R. § 1.17(g))

The U.S. Patent and Trademark Office is authorized to charge the undersigned's credit card the \$200.00 petition fee required under 37 CFR § 1.17(g).

A *bona fide* attempt is being made to comply with the provisions of 37 C.F.R. 1.47.

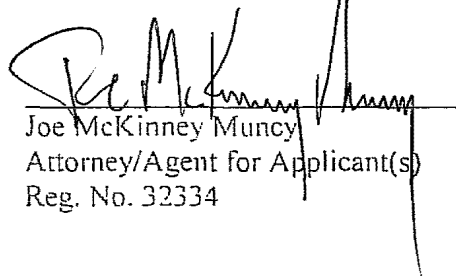
Should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Joe McKinney Muncy, Applicants' Attorney, at 703.621.7140 so that such issues may be resolved as expeditiously as possible.

Application No.
Attorney Docket No. 3722/0536PUS1
Page 4 of 4

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-3828 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; in particular, extension of time fees.

Date: November 14, 2008

Respectfully submitted,



Joe McKinney Muncy
Attorney/Agent for Applicant(s)
Reg. No. 32334

Muncy, Geissler, Olds & Lowe, PLLC
PO Box 1364
Fairfax, VA 22038-1364
Tel. 703.621.7140
mailroom@mg-ip.com

Enclosures: Executed Declaration
Contract of Employment with English Translation
Release Certificate
Statement of Facts
E-mail dated July 29, 2008 with English Translation
Letter dated August 6, 2008 with English Translation
Postal Acknowledge of Receipt with English Translation

MUNCY, GEISSLER, OLDS & LOWE, PLLC

P.O. Box 1364 • Fairfax, Virginia 22038-13647
 Telephone: (703) 621-7140 • Facsimile: (703) 621-7155

PLEASE NOTE:
 YOU MUST
 COMPLETE THE
 FOLLOWING

COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT AND DESIGN APPLICATIONS

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one inventor is named below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Insert Title:

A POWER MESH ARRANGEMENT METHOD UTILIZED IN AN INTEGRATED CIRCUIT HAVING MULTIPLE POWER DOMAINS

Fill in Appropriate

the specification of which is attached hereto. If not attached hereto, the application is identified by the attorney docket number as set forth above and/or the following:

Information -
 For Use Without
 Specification
 Attached:

The specification was filed on _____ as
 United States Application Number _____;
 and amended on _____ (if applicable) and/or
 the specification was filed on _____ as PCT
 International Application Number _____; and was
 amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representative or assigns more than twelve months (six months for designs) prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows.

I hereby claim foreign priority benefits under Title 35, United States Code, §119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

Priority Claimed

Insert Priority
 Information:
 (if appropriate)

<u>096143160</u> (Number)	<u>Taiwan, R.O.C.</u> (Country)	<u>11 / 15 / 2007</u> (Month/Day/Year Filed)	☒ Yes	☐ No
<u> </u> (Number)	<u> </u> (Country)	<u> </u> (Month/Day/Year Filed)	☐ Yes	☐ No
<u> </u> (Number)	<u> </u> (Country)	<u> </u> (Month/Day/Year Filed)	☐ Yes	☐ No
<u> </u> (Number)	<u> </u> (Country)	<u> </u> (Month/Day/Year Filed)	☐ Yes	☐ No

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional applications(s) listed below.

Insert Provisional
 Application(s):
 (if any)

<u> </u> (Application Number)	<u> </u> (Filing Date)
<u> </u> (Application Number)	<u> </u> (Filing Date)

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed More than 12 Months (6 Months for Designs) Prior to the Filing Date of This Application:

Insert Requested
 Information:
 (if appropriate)

Country	Application Number	Date of Filing (Month/Day/Year)
<u> </u>	<u> </u>	<u> </u>
<u> </u>	<u> </u>	<u> </u>

I hereby claim the benefit under Title 35, United States Code, §120 of any United States and/or PCT application(s), including for continuation-in-part application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States and/or PCT application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to the patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

Insert Prior U.S.
 Application(s):
 (if any)

<u> </u> (Application Number)	<u> </u> (Filing Date)	<u> </u> (Status - patented, pending, abandoned)
<u> </u> (Application Number)	<u> </u> (Filing Date)	<u> </u> (Status - patented, pending, abandoned)

I hereby appoint the practitioners at CUSTOMER NO. 60601 as my attorneys or agents to prosecute this application and/or an international application based on this application and to transact all business in the United States Patent and Trademark Office connected therewith and in connection with the resulting patent based on instructions received from the entity who first sent the application papers to the practitioners, unless the inventor(s) or assignee provides said practitioners with a written notice to the contrary:

Send Correspondence to:

CUSTOMER NO. 60601 (MUNCY, GEISSLER, OLDS & LOWE, PLLC)

Telephone: (703) 621-7140

Facsimile: (703) 621-7155

PLEASE NOTE:
YOU MUST
COMPLETE
THE
FOLLOWING:
↓

Full Name of First
or Sole Inventor:
Insert Name of
Inventor
Insert Date This
Document is Signed

Insert Residence
Insert Citizenship

Insert Post Office
Address

Full Name of Second
Inventor, if any:
see above

Full Name of Third
Inventor, if any:
see above

Full Name of Fourth
Inventor, if any:
see above

Full Name of Fifth
Inventor, if any:
see above

Full Name of Sixth
Inventor, if any:
see above

GIVEN NAME/FAMILY NAME CHUANG, CHIA-LIN	INVENTOR'S SIGNATURE <i>Chao-chay Lee</i> (VP of Engineering)	DATE* OCT 08 2008
Residence (City, State & Country) No. 167-1, chang-chun Street, Hsinchu City, Taiwan, R.O.C.		CITIZENSHIP Taiwan, R.O.C.
MAILING ADDRESS (Complete Street Address including City, State & Country) No. 2, Innovation Rd. II, Science-Based Industrial Park, Hsinchu 300, Taiwan R.O.C.		
GIVEN NAME/FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)		CITIZENSHIP
MAILING ADDRESS (Complete Street Address including City, State & Country)		
GIVEN NAME/FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)		CITIZENSHIP
MAILING ADDRESS (Complete Street Address including City, State & Country)		
GIVEN NAME/FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)		CITIZENSHIP
MAILING ADDRESS (Complete Street Address including City, State & Country)		
GIVEN NAME/FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)		CITIZENSHIP
MAILING ADDRESS (Complete Street Address including City, State & Country)		
GIVEN NAME/FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)		CITIZENSHIP
MAILING ADDRESS (Complete Street Address including City, State & Country)		
GIVEN NAME/FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)		CITIZENSHIP
MAILING ADDRESS (Complete Street Address including City, State & Country)		

*DATE OF SIGNATURE

CONTRACT OF EMPLOYMENT

File: B0502-B2

Contract made and entered into on this 1st day of July, 2003 by and between **Realtek Semiconductor Corporation** (hereinafter referred to as "the Employer") and **Chuang, Chia-Lin** (hereinafter referred to as "the Employee").

Whereas the Employer agrees to hire the Employee as its employee, while the Employee agrees to work for the Employer under the terms and conditions hereunder. It is mutually agreed as follows:

Article 1

Scope of Service

1. Due to practical demand of business, the Employer hereby hire the Employee to act as its CAD Engineer in charge of the underlying jobs:
 - 1) _____;
 - 2) _____; and
 - 3) _____.
2. In addition to the jobs referred to above, the Employer is, as the case may be, entitled to adjust jobs and duties of the Employee, and the Employee shall not withhold it for any cause.

Article 2

Working Hours

Please tick one of the following options:

- ☐ Normal Shift: 08:00 AM ~ 05:30 PM from Monday thru Friday.
- ☐ 4 Teams/2 Shifts (Day): 07:30 AM ~ 07:30 PM.
- ☐ 4 Teams/2 Shifts (Night): 07:30 PM ~ 07:30 AM.

With respect to the Normal Shift, first-grade director of the respective section or department is entitled to make a flexible adjustment in regard to working hours in order to satisfy the requirements of different jobs or different areas without limitation by the working hours referred to above.

In principle, average working hours must meet the basic requirement for 42.50 hours a week.

After execution of the Contract, in case the Employer adjusts working hours of its employees, working hours of the Employee are adjustable as well.

Article 3

The Employee hereby agrees that the Employer is entitled to change her workplace or to order her to take a business trip out of the workplace.

Article 4

Salary and Wage

Monthly Pay_____; Commuter's Allowance_____; Shift Allowance:_____.

After execution of the Contract, adjustment of salary or payment of annual bonus or performance bonus of the Employee all shall subject to the Work Rules of the Employer or announcement published by the Employer.

Both parties agree that the monthly pay shall be made before 5th day of the succeeding month. Should the payment date be Sunday or a public holiday, the payment shall be made on the day before such payment date. As for the method of payment, the Employee agrees with that of the Employer.

Article 5

Prohibition of Competitive Business

During the term of employment, the Employee shall do her duty faithfully and shall not concurrently do other job other than that for the Employer. Moreover, the Employee shall not have any act infringing or violating rights or interests of the Employer.

Article 6

Probation

The Employee hereby agrees with a probationary period for 30 days, which will be counted from her installation day. If the Employee fails to pass the evaluation of the Employer during probationary period, the Contract shall be terminated shortly after the Employer gives a notice to the Employee, but the Employer shall still pay the salary of such probationary period to the Employee.

Article 7

Covenant on Work

The Employee hereby agrees and is willing to overwork owing to practical need of work or to adjust her original functions, working hours or workplace due to practice demand of business or to be transferred to any affiliated company of the Employer. However, such adjustments must be reasonable and is related to the specialty of the Employee.

Article 8

Agreement on Copyright

As for any invention, utility model or new style completed by the Employee at her post, its patent application right as well as patent right shall be belonging to the Employer.

As for any invention, utility model or new style completed by the Employee relative to her post, its patent application right as well as patent right shall be belonging to the Employer.

As for any invention, utility model or new style completed by the Employee irrelative to her post, its patent application right as well as patent right shall be belonging to the Employee. However, if such invention, utility model or new style is completed by taking advantage of resources or experiences of the Employer, the Employer is entitle to make such invention, utility model or new style (hereinafter collectively referred to as "the Invention") embody on its business provided that the Employer pays a reasonable remuneration to the Employee.

As for other inventions or ideas relative to her post, such as: subject matters relating to copyright, trade secret or semiconductor chip layout, their rights all shall be belonging to the Employer. In the event that the Employer desires to apply for registration of related intellectual property at home or abroad in regard to such rights, the Employee shall unconditionally provide necessary documents, help and cooperation to complete such registration no matter if the Employee is still working at or has resigned from the Employer.

The Employee shall advise the Employer shortly after she completes the Invention as set forth in the first or second sub-paragraph of the present article at her post or irrelative to her post.

With respect to the Invention as set forth in the first or second sub-paragraph, where any third party makes any opposition or institutes any lawsuit, the Employee shall extend necessary helps to the Employer either during the term or termination of the Contract, such as: verbal or written inquiries and opinions or witness at court. However, all costs and expenses arisen therefrom shall be for account of the Employer.

Article 9

Commitment to Confidentiality

For all trade secrets of the Employer that the Employer acquires or knows at her job or post, the Employee is obligated to fulfill non-disclosure obligations. Meanwhile, the Employee shall enter into a Non-Disclosure Agreement with the Employer on her installation day. Such Agreement shall be incorporated and integrated into the Contract, being binding to both parties.

Article 10

Compliance with Rules and Regulations

Unless otherwise expressly specified in the Contract, both rights and obligations of the Employee all shall be subject to Work Rules of the Employer. Not only is such Work Rules incorporated into the Contract, but also shall be binding to both parties. In case any matter is not stipulated in such Work Rules or such Work Rules are not perfect enough, it shall be subject to Labor Standard Law and other applicable civil rules and regulations.

Article 11

Effect of the Contract

In case any clause of the Contract doesn't hold true or is unenforceable, the effect of other clauses shall not be affected at all.

Article 12

Damages

If any party violates the Contract, other party may terminate the Contract on the basis of the provisions of the Contract and/or other applicable rules and regulations and is entitled to claim damages arisen therefrom.

If there are any damages on the part of the Employer because of violation of the Contract by the Employee. Under the circumstances, the Employer is

entitled to claim such damages against the Employee to the extent of losses sustained and interests lost by the Employer.

If the Employer might be damaged due to violation of the Contract by the Employee, the Employer is entitled to take back from the Employee all work owned by the Employer forthwith. In this context, the Employee shall not make any objection.

Article 13

Competent Court

Any dispute arisen from or relating to the Contract shall be negotiated by both parties in good faith. In the event of rupture of such negotiation, both parties agree that Taipei District Court shall be the first-instance competent court.

Article 14

The Contract is made in duplicate, one of which will be kept by each party respectively.

The Employer:

Realtek Semiconductor Corporation (sealed)

Representative: Yeh, Po-Len (sealed)

Address: No. 2, Innovation Rd. II, Hsinchu Science Park Hsinchu 300, Taiwan

The Employee:

Chuang, Chia-Lin (sealed)

ID Card No.: D120832646

Address: No. 167-1, Changchun St., Hsinchu City

聘 僱 契 約

FILE: B0502-B2

立契約書人瑞昇半導體股份有限公司（以下簡稱甲方）茲同意聘請 莊任霖（以下簡稱乙方）為甲方之員工，乙方亦同意依以下之條件為甲方服務，爰經雙方同意訂定本契約，以昭信守：

第一條：職務範圍

(一) 甲方因業務需要，聘請乙方擔任 CAD 工程師 職務：從事下列工作：

1. _____
2. _____
3. _____

(二) 除前述工作外，甲方於必要情形下，得變得調整乙方工作項目、職務，乙方不得無故拒絕。

第二條：工作時間（請勾選填入）

- ☐ 正常班：週一至週五上午八時正至下午五時三十分；
- ☐ 四班二輪（日）：早上七時三十分至晚上七時三十分；
- ☐ 四班二輪（夜）：晚上七時三十分至早上七時三十分；

在正常班中，為應不同之工作性質或不同地區的需要，各部門人員的工作時間，可由該部門一級主管做權宜調整，不受上述工作時間的限制。

原則上，平均一週工作的時數仍須達 42.5 小時的基本規定。

本契約生效後，若甲方調整其員工工作時間，乙方之工作時間亦隨同調整。

第三條：工作地點：

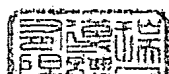
乙方同意甲方得變更其工作地點或命乙方出差外地。

第四條：薪資待遇

交通津貼 ○ 輪班津貼 ○

本契約生效後，乙方薪資待遇之調整或年節獎金、績效獎金之給與，依甲方工作規則或發佈之公告辦理。

雙方同意每月薪資於次月五日以前發放，如發放日遇星期日或國定假日時，則提前一日發放；其發放方式，乙方同意依甲方規定方式辦理。



第五條：兼職禁止

在聘約期間，乙方應盡忠職守，除經甲方同意外，不得兼任甲方職務以外之其他任何職務，亦不得有侵犯或違反甲方權益之行為。

第六條：試用期間

乙方同意自報到之日起三十日為試用期間，乙方於試用期間，經甲方考核不及格者，本契約於甲方通知乙方之時起終止，但乙方試用期間之薪資甲方仍應給付。

第七條：工作約定

乙方同意並願意配合甲方因工作需要之加班或因業務之需要而調整其原有職發、工作時間或工作地點或至甲方的關係企業任職。但前開之調整需係合理且與乙方專長相關者為限。

第八條：著作人約定

乙方於職務上所完成之發明、新型、新式樣，其專利申請權及專利權屬於甲方所有。乙方完成與職務有關之發明、新型、新式樣，其專利申請權及專利權屬於甲方所有。乙方完成之發明、新型、新式樣與職務無關，其專利申請權及專利權屬於乙方所有，但如係利用甲方之資源或經驗者，甲方得於支付乙方合理報酬後，於其事業實施乙方之發明、新型、新式樣（以下合稱創作）。

乙方其他職務上之創作或構想等，例如符合著作權、營業秘密或半導體晶片佈局保護之標的者，其權利皆歸甲方所有。

如甲方就前開歸屬於己之權利，欲申請國內外相關智慧財產權之註冊或登記時，乙方不論係在職中或離職後，應無條件提供必要之文件及協助，並配合甲方完成之。乙方不論係職務上或非職務上完成本條第一、二項之創作時，皆應立即通知甲方。

就本條第一、二項之創作，有第三人提出異議或訴訟時，不論其發生係在雙方僱傭期間內或僱傭關係終止後，乙方皆應提供甲方必要之協助，例如：口頭或書面之諮詢及意見、出庭作證等，但因此而生之費用，概由甲方負擔。

第九條：保密約定

乙方因工作或職務所知悉由甲方所有之營業秘密，乙方皆應負保密義務。乙方並應於報到時與甲方簽署保密契約書，該契約書之內容構成本契約之一部，有效拘束雙方當事人。

第十條：規章遵守

乙方得享之權利與應盡之義務，除本契約有特別規定外，悉參照甲方工作規則之規定，該工作規則內容構成本契約之一部，有效拘束雙方當事人。工作規則未規定或規定不全之部份，則從勞動基準法及民法等相關法令之規定。

第十一條：契約效力

本契約之條款，如部份無效或無法執行，不影響其他條款之效力。

第二十二條：損害賠償

當事人之一若違反本契約之規定時，他方當事人得依本契約及相關法令之規定行使其終止本契約或請求損害賠償之權利。

乙方違反本約定書之約定，致甲方受有損害，甲方得就其所受損害及所受利息，對乙方請求賠償損害。

乙方違反本約定書之約定，有使甲方受損害之虞時，甲方得立即收回乙方所有甲方之相關著作物，乙方絕無異議。

第二十三條 管轄法院

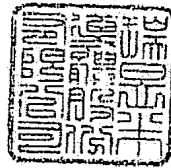
凡因本契約而生之爭議，雙方同意先本誠信原則磋商之，磋商不協時，雙方同意以台灣台北地方法院為第一審管轄法院。

第二十四條：本契約一式二份，雙方各執一份為憑。

訂契約書人：

甲 方：瑞昱半導體股份有限公司

代表人：葉博任



地 址：新竹科學園區工業東九路2號

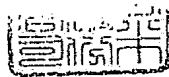
乙 方：莊佳霖



身份證字號：D120832646

地 址：新竹市長春街16731號

中 華 民 國： 92 年 7 月 1 日



MUNCY, GEISSLER, OLDS & LOWE, PLLC

UNITED STATES PATENT RIGHTS, OR
UNITED STATES PLUS ALL FOREIGN PATENT RIGHTS

ASSIGNMENT

Application No. _____

Filed _____

Insert Name(s)
of Inventor(s)

*** (Given Name FAMILY NAME (ALL CAPS)) ***

WHEREAS, CHUANG, CHIA-LIN

(hereinafter designated as the undersigned) has (have) invented certain new and useful improvements in

Insert Title
of InventionA POWER MESH ARRANGEMENT METHOD UTILIZED IN AN INTEGRATED CIRCUIT HAVING
MULTIPLE POWER DOMAINS

for which an application for Letters Patent of the United States of America has been executed by the undersigned (except in the case of a provisional application).

Insert Date
of Signing of
Application

IN AN INTEGRATED CIRCUIT HAVING MULTIPLE POWER DOMAINS

on _____; and

Insert Name
of AssigneeWHEREAS, Realtek Semiconductor Corp.Insert Address
of Assigneeof No. 2, Innovation Rd. II, Science-Based Industrial Park, Hsinchu 300, Taiwan R.O.C.

its heirs, successors, legal representatives and assigns (hereinafter designated as the Assignee) is desirous of acquiring the entire right, title and interest in and to said invention and in and to any Letters Patent(s) that may be granted therefor in the United States of America and

CHECK BOX
IF APPROPRIATE☐ in any foreign countries.

NOW, THEREFORE, in consideration of the sum of Ten Dollars (\$10.00) to the undersigned in hand paid, the receipt of which is hereby acknowledged, and other good and valuable consideration, the undersigned has (have) sold, assigned and transferred, and by these presents does sell, assign and transfer unto said Assignee the full and exclusive right to the said invention in the United States of America, its territories, dependencies and possessions and the entire right, title and interest in and to any and all Letters Patent(s) which may be granted therefor in the United States of America, its territories, dependencies and possessions, and if the box above is designated, in any and all foreign countries;

and to any and all divisions, reissues, continuations, conversions and extensions thereof for the full term or terms for which the same may be granted.

The undersigned agree(s) to execute all papers necessary in connection with this application and any continuing, divisional, conversion or reissue applications thereof and also to execute separate assignments in connection with such applications as the Assignee may deem necessary or expedient.

The undersigned agree (s) to execute all papers necessary in connection with any interference which may be declared concerning this application or continuation, division, conversion or reissue thereof or Letter Patent(s) or reissue patent issued thereon and to cooperate with the Assignee in every way possible in obtaining and producing evidence and proceeding with such interference.

The undersigned agree(s) to execute all papers and documents and to perform any act which may be necessary in connection with claims or provisions of the International Convention for the Protection of Industrial Property or similar agreements.

The undersigned agree(s) to perform all affirmative acts which may be necessary to obtain a grant of a valid United States of America patent(s) or a grant of a valid United States of America and any foreign patent(s) to the Assignee and to vest all rights therein hereby conveyed to said Assignee as fully and entirely as the same would have been held by the undersigned if this Assignment and sale had not been made.

The undersigned hereby authorize(s) and request(s) the Patent and Trademark Office Officials in the United States of America and in any foreign countries to issue any and all Letters Patents resulting from said application or any continuing, divisional conversion or reissue applications thereof to the said Assignee, as Assignee of the entire interest, and hereby covenants that he has (they have) the full right to convey the entire interest herein assigned, and that he has (they have) not executed, and will not execute, any agreement in conflict herewith.

The undersigned hereby grant(s) the law firm of Muncy, Geissler, Olds & Lowe, PLLC the power to insert on this Assignment any further identification which may be necessary or desirable in order to comply with the rules of the U.S. Patent and Trademark Office for recordation of this document.

The undersigned hereby covenant(s) that no assignment, sale, agreement or encumbrance has been or will be made or entered into which would conflict with this assignment.

In witness whereof, executed by the undersigned on the date(s) opposite the undersigned name(s).

Date <u>OCT 08 2008</u>	Name of Inventor <u>Chao-Chang Lee</u> (VP of Engineering) (signature) CHUANG, CHIA-LIN
Date _____	Name of Inventor _____ (signature)
Date _____	Name of Inventor _____ (signature)
Date _____	Name of Inventor _____ (signature)
Date _____	Name of Inventor _____ (signature)
Date _____	Name of Inventor _____ (signature)

瑞昱半導體股份有限公司

No. 2, INNOVATION ROAD II,
Hsinchu Science Park,
Hsinchu 300, Taiwan, R.O.C.

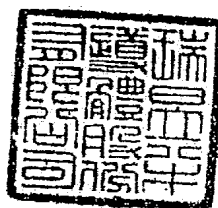
TEL : 03-5786211

300 新竹科學園區創新二路二號

日期: Jul. 30, 2008

離職證明 RELEASE CERTIFICATE

姓 名 NAME	莊佳霖 Chuang Chia-lin
性 別 SEX	男 Male
身 份 證 字 號 ID CARD NO.	D120832646
出 生 年 月 日 DATE OF BIRTH	63 年 06 月 13 日 Jun. 13, 1974
服 務 部 門 DEPARTMENT	研發中心 R&D Center
職 稱 TITLE	主任工程師 Principal Engineer
到 職 日 期 DATE OF EMPLOYMENT	92 年 07 月 01 日 Jul. 01, 2003
離 職 日 期 THE LAST DAY WORKED	96 年 10 月 12 日 Oct. 12, 2007
備 註 REMARK	



瑞昱半導體股份有限公司
Realtek Semiconductor Corp.

Statement of Facts

INVENTOR REFUSES TO SIGN

I, Tien, Xing-Ci, am a IP & Legal Dept. Assistant of Realtek Semiconductor Corporation, a company organized under the laws of Taiwan, R.O.C. and having a business address of No. 2, Innovation Rd. II, Science-Based Industrial Park, Hsinchu 300, Taiwan R.O.C..

I hereby attest that, I made an attempt to contact Chia-Lin CHUANG by telephone on July 28, 2008 to request sign of the application papers, but Chia-Lin CHUANG made an express oral refusal to sign the Declaration. Then attempt to contact via e-mail on July 29, 2008, but no response was received.

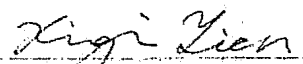
On August 06, 2008, I forwarded by registered mail 1) a complete copy of the specification, claims and drawings for Applicant doc.No.96A-022, and 2) Declaration and Assignment forms to be executed, to inventor Chia-Lin CHUANG. These papers were mailed to Chia-Lin CHUANG's last known address of No.167-1, Changchun St., Hsinchu City 300, Taiwan, R.O.C.. A copy of the registered mail receipt is attached hereto, as evidence of the mailing of the application papers to Chia-Lin CHUANG, together with a verified English language translation thereof.

On August 18, 2008, I received the notice of delivery, confirming that the above-noted application papers were delivered to Chia-Lin CHUANG on August 15, 2008. A copy of the notice of delivery, as evidence of receipt of the application papers by Chia-Lin CHUANG, is attached.

To date, the signed Declaration has not been received from Chia-Lin CHUANG.

Accordingly, it is respectfully submitted that the complete application papers were forwarded to Chia-Lin CHUANG, but that he refuses to join in the application by signing the Declaration.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.


(Signature) Xing-Ci Tien

OCT 02 2008

(Date)



田幸慈/Realtek
2008/07/29 PM 06:31

To solonchuang@gmail.com
cc "my_yeh[葉明郁]" <my_yeh@realtek.com.tw>
bcc "wmshiau[蕭王勉]" <wmshiau@realtek.com.tw>
Subject [Urgent] 關於您在瑞昱的專利提案

Dear 佳霖,

您的提案清單如下表。供您參考。

94A-222TW及96A-022TW文件已提交，目前要麻煩您補簽的文件則是藍色背景標示的六案，現關於96A-021TW 及 96A-023TW申請案我們已收到智慧局的補件通知，要求補呈專利申請權證明書，而該文件需發明人親自簽名，現將文件附呈如下，還請您協助簽名後在 07/30前傳真回瑞昱予我。另所附之 Assignment & Declaration & POA為美國申請案所需，亦麻煩您一併簽署及傳真了。謝謝！

據了解，一般公司給予新進員工簽署的契約，主要是避免將前公司之研發技術帶入新公司，而非要求員工不准予簽署專利申請證明書（此將違反您的專利姓名表示權），這些文件主要是聲明你為下表所列專利的發明人（您的發明權聲明），並依據專利法第七條第二款規定，您於瑞昱任職內所提之專利申請權屬於瑞昱（瑞昱的申請權證明），故並不會影響您予現任公司所簽訂之保密或營業秘密之契約（這些文件僅限於下列發明），反而將影響您的專利發明姓名表示權（如未能申請成功，您的研發生涯中將因而少了這些專利紀錄）。

以上如您仍有任何疑慮，儘請不吝與我聯絡。謝謝！

瑞昱編號	專利名稱	國別	創作人	部門
94A-222TW	積體電路電源佈局及其設計方法	TW	莊佳霖	研發中心
94A-222US	A Novel Methodogy for Power Mesh Construction	US	莊佳霖	研發中心
96A-021TW	電源供應網之規劃方法與積體電路佈局結構	TW	莊佳霖	研發中心
96A-021US	APR power structure - new method to improve connectivity between power mesh and sram macro	US	莊佳霖	研發中心
96A-022TW	電源供應網之規劃方法	TW	莊佳霖	研發中心
96A-022US	A power mesh arrangement method utilized in an integrated circuit having multiple power domains	US	莊佳霖	研發中心
96A-023TW	電源供應網之規劃方法與積體電路	TW	莊佳霖	研發中心
96A-023US	APR power structure - connection layer between power mesh and standard cell power trunk	US	莊佳霖	研發中心

PS：申請權證明書請簽署中文；Declaration & Assignment & POA 則請依文件所列印之英文拼音簽署。

僅需於姓名(signature)處簽名即可，其他部分無須填寫，且期亦請留空。【請單面列印】

 
 94A-222(元勤案號：5RTK200503US)-Assignment.doc 94A-222(元勤案號：5RTK200503US)-Declaration Form.DOC
 
 07P039-US(96A-021US)-Declaration.doc 07P039-TW(96A-021TW)-申請權證明書.doc
  
 07P039-US(96A-021US)-Assignment.doc 07P040-US(96A-022US)-Declaration.doc 07P040-US(96A-022US)-Assignment.doc
 
 07P041-TW(96A-023TW)-申請權證明書.doc 07P041-US(96A-023US)-Assignment.doc

 07P041-US(96A-023US)-Declaration.doc

Best regards,

=====

田幸慈 Xingci, Tien
IP & Legal Dept.
Realtek Semiconductor Corp.
瑞昱半導體股份有限公司
300 新竹科學園區創新二路二號

No.2, Innovation Rd.II
Hsinchu Science Park
Hsinchu 300, Taiwan
TEL: +886-3-5780211 ext. 5653
FAX: +886-3-5789458
E-mail: xingci@realtek.com.tw

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NOTICE:

This e-mail is sent by legal department of Realtek Semiconductor Corporation and may contain information that is confidential, protected as work product, or privileged communications. If you are not the intended recipient, please delete the e-mail and any attachments, destroy all hard copies thereof, and notify the sender immediately.

Xingci, Tien/Realtek
07/29/2007 PM 06:31

Dear Chia-Lin:

Regarding your proposals, please refer to the table hereunder.

Documents relating to 94A-222TW and 96A-022TW have been sent for application. Now, please sign documents in regard to Case 6 showing with blue background. With respect to 96A-021TW and 96A-023TW applications, we have received a notice for submitting other documents from the Intellectual Property Office. They asked us to submit a Certificate of Patent Application Right, which must be signed by the inventor in propria persona. I am now sending you such document for your signature. Please kindly send it back to me at Realtek by fax before 07/30 after you will have signed it. Meanwhile, I also send you Assignment, Declaration and POA necessary for US patent application, so please also sign and send the same by fax to me at the same time. Thanks a lot.

To my knowledge, most of companies always asked new employee to enter into a contract in order to bring R&D know-how from his previous company to new company, and such contract would not prevent you from signing a patent application certificate. (This will violate the right in expressing your name in the patent.) These documents only serve to declare that you are inventor of the underlying patents (declaration of your inventive right). In addition, on the basis of Article 7.2 of Patent Law, patent application rights that you proposed at Realtek are belonging to Realtek (Realtek's certificate of application right); as a result, it would not affect any non-disclosure or trade business agreement that you have entered into with your present employer (because these documents are only used for the underlying inventions.) If you fail to sign these documents, it would affect the right in expressing your name in the patent. (If the applications become unsuccessful, there will be no records of these patents in your R&D career.)

In case of any question, please don't hesitate to contact me at any time. Thank you.

Realtek' No.	Title of Patent	Country	Inventor	Department
94A-222 TW	A Novel Methodology for Power Mesh Construction	TW	Chuang, Chia-Lin	R&D Center
94A-222 US	A Novel Methodology for Power Mesh Construction	US	Chuang, Chia-Lin	R&D Center
96A-021 TW	APR Power Structure – New Method to Improve Connectivity between Power Mesh and Sram Macro	TW	Chuang, Chia-Lin	R&D Center
96A-021 US	APR Power Structure – New Method to Improve Connectivity between Power Mesh and Sram Macro	US	Chuang, Chia-Lin	R&D Center
96A-022 TW	A Power Mesh Arrangement Method Utilized in an Integrated Circuit Having Multiple Power Domains	TW	Chuang, Chia-Lin	R&D Center
96A-022 US	A Power Mesh Arrangement Method	US	Chuang,	R&D

	Utilized in an Integrated Circuit Having Multiple Power Domains		Chia-Lin	Center
96A-023 TW	APR Power Structure - Connection Lawyer between Power Mesh and Standard Cell Power Trunk	TW	Chuang, Chia-Lin	R&D Center
96A-023 US	APR Power Structure - Connection Lawyer between Power Mesh and Standard Cell Power Trunk	US	Chuang, Chia-Lin	R&D Center

PS:

- Certificate of Application Right: Please sign in Chinese;
- Declaration, Assignment and POA: Please sign in English as the spelling printed herein.
- Please just sign your name in the signature place, and it is not necessary to complete other spaces, and please leave date space blank.

94A-222 (IPTEC Ref No.: 5RTK200503US) Assignment.doc
94A-222 (IPTEC Ref No.: 5RTK200503US) Declaration Form.DOC
07P033-US (96A-021US) Declaration.doc
07P033-TW (96A-021TW) Certificate of Application Right.doc
07P039-US (96A-021US)Assignment.doc
07P040-US (96A-022US) Declaration.doc
07P040-US (96A-022US) Assignment.doc
07P041-TW (96A-023TW) Certificate of Application Tight.doc
07P041-US (96A-023US)Assignment.doc
07P041-US (96A-023US) Declaration.doc

Best regards,

Xingci, Tien
IP & Legal Dept.
Realtek Semiconductor Corp.
No. 2, Innovation Rd. II
Hsinchu Science Park
Hsinchu 300, Taiwan
Tel: +886-3-5780211 ext. 5653
Fax: +886-3-5789458
E-mail: xingci@realtek.com.tw

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REALTEK SEMICONDUCTOR CORPORATION

No. 2, Innovation Rd. II
Hsinchu Science Park
Hsinchu 300, Taiwan
Tel: +886-3-5780211
Fax: +886-3-5789458

NOTICE FOR SIGNATURE OF PATENT DOCUMENTS

Date: August 06, 2008

To: Mr. Chuang, Chia-Lin

Dear Mr. Chuang:

The following are the patents proposed and invented by you during your service at Realtek Semiconductor Corporation (From Jul. 11, 2003 through Oct. 12, 2007):

	Title of Invention	Proposed on
1. 94A-222	A Novel Methodology for Power Mesh Construction	11.07.2005
2. 96A-021	APR Power Structure – New Method to Improve Connectivity between Power Mesh and Sram Macro	03.26.2007
3. 96A-022	A Power Mesh Arrangement Method Utilized in an Integrated Circuit Having Multiple Power Domains	03.26.2007
4. 96A-023	APR Power Structure – Connection Layout between Power Mesh and Standard Cell Power Trunk	03.26.2007

The patent applications relating to the above inventions will be filed with US Patent Office, so we need to present the documents attached herewith in order to complete patent application procedure. Please kindly sign these documents, and return the same with the present letter in the postage-paid envelope by registered mail to Realtek Semiconductor Corporation before "Aug. 20, 2008". If we fail to receive such documents signed by you by the above date, we will consider that you are not willing to sign such documents.

- * To avoid loss of documents, please send us by fax No. 03-5789458 before mailing to us.

THANK YOU FOR YOUR KIND HELP!

Article 8 of Contract of Employment of Realtek Semiconductor Corporation provides as follows: As for any invention, the inventor relative to his post, its patent application right as well as patent right shall be belonging to Realtek. In the event that Realtek desires to apply for registration at home or abroad in regard to such rights, the inventor shall unconditionally provide necessary documents, help and cooperation to complete such registration no matter if he is still working at or has resigned from the Employer.

**REALTEK****瑞昱半導體股份有限公司**

300 新竹科學園區創新二路二號

No. 2, Innovation Rd. II, Hsinchu Science Park, Hsinchu 300, Taiwan

TEL: +886-3-5780211

FAX: +886-3-5789458

專利文件簽署通知函

致

通知日期：2008 年 08 月 06 日

莊佳霖 同仁 您好：

您於瑞昱半導體股份有限公司職內（2003 年 07 月 01 日至 2007 年 10 月 12 日）所提之專利：

	發明名稱	提案日期
1 94A-222	積體電路電源佈局及其設計方法	2005.11.07
2 96A-021	電源供應網之規劃方法與積體電路佈局結構	2007.03.26
3 96A-022	電源供應網之規劃方法	2007.03.26
4 96A-023	電源供應網之規劃方法與積體電路	2007.03.26
5		

已／將至

☐ 中華民國智慧財產局 ☒ 美國專利商標局 ☐ 中國知識產權局☐ 歐洲專利局 ☐ 日本特許廳 ☐ 其他（ ）

註冊申請，現需提交所附文件以完成專利申請之程序審查。煩請您協助將所附文件簽署後連同本通知函於 2008 年 08 月 20 日 前以所附回郵信封掛號寄回瑞昱半導體股份有限公司。如未能於上述期限前收到您簽署後的文件，將視為您無法或不願簽署。

※ 為避免文件遺失，可於寄出前將文件先行傳真至 03-5789458。

謝謝您的協助！

*依瑞昱半導體股份有限公司聘雇契約第八條所定：發明人於瑞昱職務上所完成之發明或完成與職務有關之發明，其專利申請權及專利權歸屬於瑞昱。如瑞昱欲將前述權利申請國內外專利之註冊或登記時，發明人不論在職中或離職後，應無條件提供必要之文件及協助，並配合瑞昱完成之。

Registered Mail No. 072954

Acknowledge of Receipt

To: Mr. Chuang, Chia-Lin

No. 167-I, Changchun St., 300 Hsinchu City

Signed by receiver

Signed by Postman

Sent from Pao Shan Post Office on Aug. 6, 2008 (sealed)

Received by Hsinch Post Office on Aug. 15, 2008 (sealed)

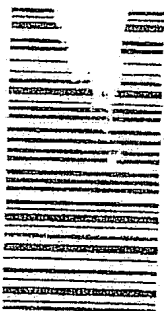
Address: No. 2, Innovation Rd. II, Hsinchu Science Park, Hsinchu 300, Taiwan

Company: Realtek Semiconductor Corp

Receipt: IP & Legal Dept.

Received by Realtek Semiconductor Corp. on Aug. 18, 2008 (sealed)

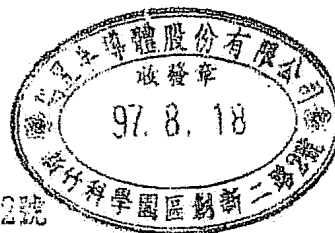
中華郵政掛號郵件收件回執		
郵件種類	號碼	(由郵局收寄人員填寫)
收件人姓名 地址(請寄)	206- 新竹市長春街167之1號 莊佳霖 小姐 先生	
年 月 日收到第 號 掛號郵件號 收件人蓋章	收寄局郵戳 投遞後郵戳	
(供查詢用填寫) 經查上述郵件已於 年 月 日妥投 君收訖 該機構收發單位代收訖 附上原掛號收據影印本一件 請查收 郵局 年 月 日		



072954 300032 16

99-00-00-36

(28,000字)(100字)05.2 95.7.180mm(13.2mm)01.147mm



郵遞區號

300

地址

新竹科學工業園區創新二路2號

瑞昱半導體股份有限公司

姓名

曾權志

小姐

先生

(寄件人姓名及詳細地址，請寄件人自行填寫)

MUNCY, GEISSLER, OLDS & LOWE, PLLC

P.O. Box 1364 • Fairfax, Virginia 22038-1364
Telephone: (703) 621-7140 • Facsimile: (703) 621-7155

PLEASE NOTE:
YOU MUST
COMPLETE THE
FOLLOWING

COMBINED DECLARATION AND POWER OF ATTORNEY
FOR PATENT AND DESIGN APPLICATIONS

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one inventor is named below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Insert Title: A POWER MESH ARRANGEMENT METHOD UTILIZED IN AN INTEGRATED CIRCUIT HAVING MULTIPLE POWER DOMAINS

Fill in Appropriate the specification of which is attached hereto. If not attached hereto, the application is identified by the attorney docket number as set forth above and/or the following:

Information - The specification was filed on _____ as
For Use Without United States Application Number _____
Specification and amended on _____ (if applicable) and/or
Attached: the specification was filed on _____ as PCT
International Application Number _____; and was
amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representative or assigns more than twelve months (six months for designs) prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows.

I hereby claim foreign priority benefits under Title 35, United States Code, §119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Insert Priority Information: (if appropriate)	Prior Foreign Application(s)	Priority Claimed
	<u>096143160</u> <u>Taiwan, R.O.C.</u> <u>11 / 15 / 2007</u>	☒ ☐
	(Number) (Country) (Month/Day/Year Filed)	Yes No
	<u> </u> <u> </u> <u> </u>	☐ ☐
	(Number) (Country) (Month/Day/Year Filed)	Yes No
	<u> </u> <u> </u> <u> </u>	☐ ☐
	(Number) (Country) (Month/Day/Year Filed)	Yes No
	<u> </u> <u> </u> <u> </u>	☐ ☐
	(Number) (Country) (Month/Day/Year Filed)	Yes No

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional applications(s) listed below.

Insert Provisional Application(s): (if any)	(Application Number)	(Filing Date)
	<u> </u>	<u> </u>
	(Application Number)	(Filing Date)

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed More than 12 Months (6 Months for Designs) Prior to the Filing Date of This Application:

Insert Requested Information: (if appropriate)	Country	Application Number	Date of Filing (Month/Day/Year)
	<u> </u>	<u> </u>	<u> </u>
	(Country)	(Application Number)	(Date of Filing)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States and/or PCT application(s), including for continuation-in-part application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States and/or PCT application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to the patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

Insert Prior U.S. Application(s): (if any)	(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)
	<u> </u>	<u> </u>	<u> </u>
	(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)

I hereby appoint the practitioners at CUSTOMER NO. 60601 as my attorneys or agents to prosecute this application and/or an international application based on this application and to transact all business in the United States Patent and Trademark Office connected therewith and in connection with the resulting patent based on instructions received from the entity who first sent the application papers to the practitioners, unless the inventor(s) or assignee provides said practitioners with a written notice to the contrary:

Send Correspondence to:

CUSTOMER NO. 60601 (MUNCY, GEISSLER, OLDS & LOWE, PLLC)

Telephone: (703) 621-7140

Facsimile: (703) 621-7155

PLEASE NOTE:
YOU MUST
COMPLETE
THE
FOLLOWING:

Full Name of First
or Sole Inventor
Inventor
Insert Date This
Document is Signed

Insert Residence
Insert Citizenship

Insert Post Office
Address

Full Name of Second
Inventor, if any:
see above

Full Name of Third
Inventor, if any:
see above

Full Name of Fourth
Inventor, if any:
see above

Full Name of Fifth
Inventor, if any:
see above

Full Name of Sixth
Inventor, if any:
see above

GIVEN NAME/FAMILY NAME CHUANG, CHIA-LIN		INVENTOR'S SIGNATURE <i>Chao-chang Lee</i> (VP of Engineering)	DATE* OCT 08 2008
Residence (City, State & Country) No. 167-1, chang-chun Street, Hsinchu City, Taiwan, R.O.C.		CITIZENSHIP Taiwan, R.O.C.	
MAILING ADDRESS (Complete Street Address including City, State & Country) No. 2, Innovation Rd. II, Science-Based Industrial Park, Hsinchu 300, Taiwan R.O.C.			
GIVEN NAME/FAMILY NAME		INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)		CITIZENSHIP	
MAILING ADDRESS (Complete Street Address including City, State & Country)			
GIVEN NAME/FAMILY NAME		INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)		CITIZENSHIP	
MAILING ADDRESS (Complete Street Address including City, State & Country)			
GIVEN NAME/FAMILY NAME		INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)		CITIZENSHIP	
MAILING ADDRESS (Complete Street Address including City, State & Country)			
GIVEN NAME/FAMILY NAME		INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)		CITIZENSHIP	
MAILING ADDRESS (Complete Street Address including City, State & Country)			
GIVEN NAME/FAMILY NAME		INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)		CITIZENSHIP	
MAILING ADDRESS (Complete Street Address including City, State & Country)			

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		A POWER MESH ARRANGEMENT METHOD UTILIZED IN AN INTEGRATED CIRCUIT HAVING MULTIPLE POWER DOMAINS		
First Named Inventor/Applicant Name:		Chia-Lin CHUANG		
Filer:		Joe McKinney Muncy/Mary Pat Egan		
Attorney Docket Number:		3722/0536PUS1		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Petition fee- 37 CFR 1.17(g) (Group II)	1463	1	200	200

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1290

Electronic Acknowledgement Receipt

EFS ID:	4293898
Application Number:	12271534
International Application Number:	
Confirmation Number:	4308
Title of Invention:	A POWER MESH ARRANGEMENT METHOD UTILIZED IN AN INTEGRATED CIRCUIT HAVING MULTIPLE POWER DOMAINS
First Named Inventor/Applicant Name:	Chia-Lin CHUANG
Customer Number:	60601
Filer:	Joe McKinney Muncy/Mary Pat Egan
Filer Authorized By:	Joe McKinney Muncy
Attorney Docket Number:	3722/0536PUS1
Receipt Date:	14-NOV-2008
Filing Date:	
Time Stamp:	16:56:54
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 1290
RAM confirmation Number	2438
Deposit Account	503828
Authorized User	MUNCY,JOE MCKINNEY

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

AMD EX1002

AMD v. Realtek

Page 56

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal of New Application	NPATL.pdf	75110	no	1
			cb2c74ee913ca674763ff5a1bdef6d05cc277231		
Warnings:					
Information:					
2	Fee Worksheet (PTO-06)	FeeTL.pdf	78004	no	1
			5df2dd843706fa6e8f63e8d79057fa5555e7c788		
Warnings:					
Information:					
3	Specification	specification.pdf	471753	no	10
			13bf614d1850a0eacfbfaea2865a234bcb1965ef		
Warnings:					
Information:					
4	Claims	claims.pdf	133474	no	3
			8fa18646832de7c96852706ca265d8fde8969705		
Warnings:					
Information:					
5	Abstract	abstract.pdf	22791	no	1
			725343bc6503cf483dcf42fe442d2c566952942e		
Warnings:					
Information:					
6	Drawings-only black and white line drawings	drawings.pdf	214035	no	6
			e440f8653122a3063cdf3589fc1f5c876e593ad99		
Warnings:					
Information:					
7	Petition for review by the Office of Petitions.	Petition.pdf	1265905	no	27
			cb7354806219498e2595f5ea5d2fd0aaf714ad92		
Warnings:					
Information:					
8	Oath or Declaration filed	declaration.pdf	267542	no	2
			52960add052471b86f8aedf22679c817660261b7		
Warnings:					
Information:					

9	Fee Worksheet (PTO-06)	fee-info.pdf	36772	no	2
			7ebacf8a1b5da1afdfc5654e54232def4d2c a555		
Warnings:					
Information:					
Total Files Size (in bytes):				2565386	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Filing Date: 11/14/08

Approved for use through 7/31/2006. OMB 0651-0032

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/271,534	
APPLICATION AS FILED – PART I						
(Column 1)		(Column 2)		SMALL ENTITY		OR
OTHER THAN SMALL ENTITY						
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		N/A	330
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A		N/A	540
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		N/A	220
TOTAL CLAIMS (37 CFR 1.16(i))	20	minus 20 =	x\$26		x\$52	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 =	x\$110		x\$220	
APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR				
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			195		390	
			TOTAL		TOTAL	1090
* If the difference in column 1 is less than zero, enter "0" in column 2.						
APPLICATION AS AMENDED – PART II						
(Column 1)		(Column 2)		(Column 3)		
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		SMALL ENTITY	
	Total (37 CFR 1.16(i))	*	Minus	**	=	RATE (\$)
	Independent (37 CFR 1.16(h))	*	Minus	***	=	ADDITIONAL FEE (\$)
	Application Size Fee (37 CFR 1.16(s))					X =
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					X =
					N/A	
					TOTAL ADD'T FEE	
(Column 1)		(Column 2)		(Column 3)		
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		SMALL ENTITY	
	Total (37 CFR 1.16(i))	*	Minus	**	=	RATE (\$)
	Independent (37 CFR 1.16(h))	*	Minus	***	=	ADDITIONAL FEE (\$)
	Application Size Fee (37 CFR 1.16(s))					X =
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					X =
					N/A	
					TOTAL ADD'T FEE	
					TOTAL ADD'T FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.						

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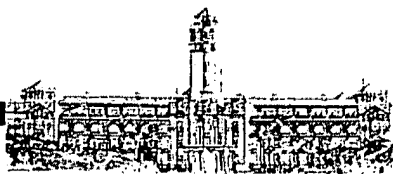
ENCLOSURES (Check all that apply)		
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT			
Firm Name	Muncy, Geissler, Olds & Lowe, PLLC		
Signature			
Printed name	Joe McKinney Muncy		
Date	November 18, 2008	Reg. No.	32334

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證明所附文件，係本局存檔中原申請案的副本，正確無訛，
請資料如下：

is to certify that annexed is a true copy from the records of this
of the application as originally filed which is identified hereunder:

請 日：西元 2007 年 11 月 15 日
tion Date Nov 15, 2007

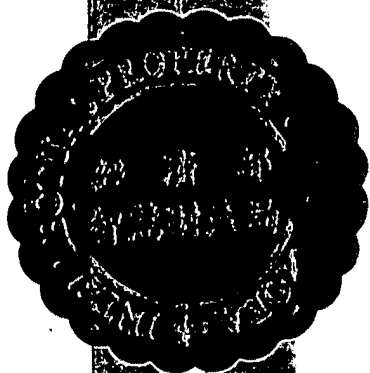
案 號：096143160
ion No.

請 人：瑞昱半導體股份有限公司
(s) REALTEK SEMICONDUCTOR CORP.

局 長
Director General

王美花

西元 2008 年 06 月 20 日
Jun 20, 2008



發明專利說明書

(本申請書格式、順序及粗體字，請勿任意更動，※記號部分請勿填寫)

※申請案號：

※申請日期：

※IPC 分類：

一、發明名稱： 電源供應網之規劃方法
A power mesh arrangement method utilized in an integrated circuit having multiple power domains

二、申請人： (共 1 人)

姓名或名稱：瑞昱半導體股份有限公司
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國籍：中華民國 / R.O.C.

三、發明人： (共 1 人)

姓名：莊佳霖 / CHUANG, CHIA-LIN

國籍：中華民國 / R.O.C.

四、聲明事項：

☐ 主張專利法第二十二條第二項 ☐ 第一款或 ☐ 第二款規定之事實，其事實發生日期為： 年 月 日。

☐ 主張專利法第二十七條第一項國際優先權：

【格式請依：受理國家（地區）；申請日；申請案號數 順序註記】

1.

2.

☐ 主張專利法第二十九條第一項國內優先權：

【格式請依：申請日；申請案號數 順序註記】

1.

2.

☐ 主張專利法第三十條生物材料：

☐ 須寄存生物材料者：

國內生物材料 【格式請依：寄存機構、日期、號碼 順序註記】

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☐ 不須寄存生物材料者：

所屬技術領域中具有通常知識者易於獲得時，不須寄存。

伍、中文發明摘要：

一種電源供應網之規劃方法，其係應用於一具有多個電源定義區之積體電路，該規劃方法包含有：根據該積體電路上一第一電源定義區之位置，形成一第一部分區域電源供應網；根據該積體電路上一第二電源定義區之位置，形成一第二部分區域電源供應網；形成一全域電源供應網，該全域電源供應網係用來提供該第一電源定義區所須之電源以及該第二電源定義區所須之電源；將該第一部分區域電源供應網耦接至該全域電源供應網以及該第一電源定義區；以及將該第二部分區域電源供應網耦接至該全域電源供應網以及該第二電源定義區。

陸、英文發明摘要：

A power mesh arrangement method utilized in an integrated circuit having multiple power domains is disclosed. The arrangement method includes: forming a first partial local power mesh according to a position of a first power domain; forming a second partial local power mesh according to a position of a second power domain; forming a global power mesh, utilized for providing powers needed by the first and the second power domains; coupling the first partial local power mesh to the global power mesh and the first power domain; and coupling the second partial local power mesh to the global power mesh and the second power domain.

柒、指定代表圖：

(一)本案指定代表圖為：第 (6) 圖。

(二)本代表圖之元件代表符號簡單說明：

100	晶片
110、120	電源定義區
300	區域電源供應網
310、320	部分區域電源供應網
400	全域電源供應網

捌、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

玖、發明說明：

【發明所屬之技術領域】

本發明係關於一種電源供應網路的規劃方法，尤指一種應用於具有多個電源定義區(multiple power domain)之積體電路之電源供應網路的規劃方法。

【先前技術】

在積體電路的領域中，由於電路日益複雜，在同一個晶片之中，不同的電路可能需要同時使用不同的電壓(電源)；舉例來說，晶片電路可能具有正常工作模式與睡眠模式兩種不同的運作模式，當晶片電路處於正常工作模式時，整體晶片電路皆使用工作電壓來進行正常操作；然而，當電路處於睡眠狀態(sleep mode)時，此電路中內部的部分電路可能仍然必須處於正常工作狀態，因此，對於此部分電路來說，仍須使用一般的工作電壓來維持運作；而另一方面，對於此部分電路之外的其他電路，則僅須較低的電壓，便可進行睡眠狀態下的運作。

因此，前述晶片電路便需要不同的電源，以分別提供不同的電壓至晶片內部的不同電路，如此方能使晶片電路於睡眠模式中進行不同的運作。因此，在實作上經常將一個晶片電路規劃為多個電源定義區(power domain)，換言之，處於不同電源定義區的電路係對應不同的電源，以允許不同電源定義區的電路使用不同的電源，來支援前述的運作。

但是，對於具有多個電源定義區的電路來說，習知的電路設計並未提供一個簡易的規則或步驟，以允許電路設計者能夠依詢一個既定的規則，來進行電源繞線(routing)的規劃與設計。舉例來說，習知的 APR(automatic placement and rounting)工具僅僅只能支援具有單一電源定義區之電路；亦即，若使用 APR 工具，僅能自動繪出只具有單一電源定義區之電路的電源繞線；因此，若要設計多個電源定義區的電源繞線，電路設計者便只能仰賴最原始的方式來進行設計，譬如直接以手繪的方式將繞線繪製出來，很明顯地，如此的設計方式不僅複雜而且又不具效率。

【發明內容】

因此，本發明的主要目的之一在於提供一種電源供應網的規劃方法，以允許使用者更簡單地將多電源定義區的電源供應網設計出來，以解決習知技術中的問題。

根據本發明之一實施例，係揭露一種電源繞線之規劃方法，其應用於一具有多個電源定義區(multiple power domain)之積體電路，該規劃方法包含有：根據該積體電路上一第一電源定義區之位置，形成一第一區域電源供應網(local power mesh)；根據該積體電路上一第二電源定義區之位置，形成一第二區域電源供應網；形成一全域電源供應網(global power mesh)，該全域電源供應網係用來提供該第一電源定義區所須之電源以及該第二電源定義區所須之電源；將該第一區域電源供應網耦接至該全域電

源供應網，並且將該第一區域電源供應網耦接至該第一電源定義區；以及將該第二區域電源供應網耦接至該全域電源供應網，並且將該第二區域電源供應網耦接至該第二電源定義區。

根據本發明之另一實施例，另揭露一種電源繞線架構，其係應用於一具有多個電源定義區(multiple power domain)之積體電路，該電源供應網(power mesh)架構包含有：一第一區域電源供應網(local power mesh)，耦接至一第一電源定義區(power domain)；一第二區域電源供應網，耦接至一第二電源定義區(power domain)；以及一全域電源供應網(global power mesh)，耦接至該第一區域電源供應網以及該第二區域電源供應網，用來分別提供該第一電源定義區與該第二定義區所須之電源。

根據本發明之另一實施例，另揭露一種電源繞線架構，其係應用於一具有多個電源定義區(multiple power domain)之積體電路，該電源繞線架構包含有：一全域電源供應網(global power mesh)，係位於一第一電源定義區以及一第二電源定義區之上，該全域電源供應網包含有：

至少一接地線，耦接至該第一電源定義區與該第二電源定義區，用來提供該第一電源定義區與該第二電源定義區所須之地電位；至少一第一電源線，耦接至該第一電源定義區，用來提供該第一電源定義區所須之電壓；以及至少一第二電源線，耦接至該第二電源定義區，用來提供該第二電源定義區所須之電壓。

根據本發明之另一實施例，另揭露一種電源繞線之規劃方法，其係應用於一具有多個電源定義區(multiple power domain)之積體電路，該規劃方法包含有：一全域電源供應網(global power mesh)，該全域電源供應網係位於一第一電源定義區以及一第二電源定義區之上，其包含有至少一接地線、至少一第一電源線、以及至少一第二電源線，其中該第一電源線係提供該第一電源定義區所須之電壓，以及該第二電源線係提供該第二電源定義區所須之電壓，該接地線係提供該第一電源定義區與該第二電源定義區所須之地電位；將該全域電源供應網之該第一電源線與該共用接地線耦接至該第一電源定義區；以及將該全域電源供應網之該第二電源線與該共用接地線耦接至該第二電源定義區。

本發明提供使用者一種電源供應網的規劃方法以相關結構，以允許使用者依循本發明的規劃方式與結構，輕易地將具有多個電源定義區之積體電路的電源供應網設計出來；此外，本發明規劃方法亦可實作於 APR 工具之中，如此一來，使用者便可藉由 APR 工具自動地將電源供應網的電路佈局(layout)繪出，更加地提升了電路設計的效率。

【實施方式】

請參閱第 1 圖，第 1 圖繪示了一個具有多個電源定義區的晶片 100。如第 1 圖所示，晶片 100 具有兩種不同的

電源定義區 110、120，其中，電源定義區 110 以空白區域顯示之，而電源定義區 120 則以斜線區域顯示之。

如前所述，電源定義區 110、120 係對應不同的電源，以供應不同的電壓至不同電源定義區 110、120 上的電路。在此請注意，於之後的揭露中，本發明提供了一種電源繞線的規劃方式與其相關結構，以允許使用者更加輕易地將電源繞線設計出來。

在此請參閱第 2 圖，第 2 圖為本發明之電源繞線規劃方式之一方法實施例的流程圖。本發明規劃方法包含下列步驟：

步驟 200：根據電源定義區 110 之位置，規劃一第一區域電源供應網(local power mesh)；

步驟 210：根據電源定義區 120 之位置，規劃一第二區域電源供應網(local power mesh)；

步驟 220：於第一區域電源供應網與第二區域電源供應網之上，規劃一全域電源供應網(global power mesh)。

在此請注意，本發明使用區域電源供應網以及全域電源供應網，來共同建構出電源定義區 110、120 的電源繞線；其中，各個區域電源供應網係依據各電源定義區 110、120 的位置來進行建置(步驟 200、步驟 210)，而全域電源供應網則是均勻的分布於區域電源供應網之上(步驟 220)。其中，全域電源供應網係耦接至外部電源(譬如透過晶片的 I/O 接腳)，以將外部電源導入晶片中，而區域電源供應網則是耦接至全域電源供應網與晶片電路(亦即所對應的電源定義區 110、120 之晶片內部電路)，如此一來，

外部電源便會藉由全域電源供應網與區域電源供應網，而輸入至晶片電路中。

請參閱第 3 圖，第 3 圖為區域電源供應網 300 之一實施例的示意圖。如第 3 圖所示，區域電源供應網可分為兩個不同的部份區域電源供應網 310、320，其位置係分別對應電源定義區 110、120 的位置；於本實施例中，部份區域電源供應網 310 係建置於電源定義區 110 的正上方，而部份區域電源供應網 320 則建置於電源定義區 120 的正上方，因此，部份區域電源供應網 310、320 便可藉由穿孔(via)耦接至下方的電源定義區 110、120。

此外，如第 3 圖所示，部份區域電源供應網 310、320 係為一網狀結構。在此請特別注意，部份區域電源供應網 310、320 彼此並沒有互相連接(這代表部份區域電源供應網 310、320 互相絕緣)，以避免彼此互相短路而導致電性的不確定。每個部份區域電源供應網 310、320 皆包含有複數條水平電源供應線與複數條垂直電源供應線。在此請注意，由於每個部份區域電源供應網 310、320 僅用來供應電源定義區 110、120 的電源；因此，於每一條水平電源供應線與垂直電源供應線中，僅須包含有一條接地線與一條電源線。舉例來說，對於部份區域電源供應網 310 來說，其所包含的電源線 311 係用來供應電源定義區 110 所需要的工作電壓 V_{DD1} ，而接地線 312 則是用來提供電源定義區 110 所須的地電位 V_{GND} ；另一方面，對於部份區域電源供應網 320 來說，其所包含的電源線 321 係用來供應電源定義區 120 所需要的工作電壓 V_{DD2} ，而接地線 322 則是

用來提供電源定義區 120 所須的地電位 V_{GND} 。

此外，雖然於第 3 圖中，電源線 311 與接地線 312 繪製的相當接近，並且電源線 321 與接地線 322 亦相當接近，然而，在此請注意，電源線 311 與接地線 312 彼此之間並無接觸(此代表電源線 311 與接地線 312 形成斷路)，以避免短路而導致電性的不確定；相同地，電源線 321 與接地線 322 彼此之間亦形成斷路，以避免短路而導致電性的不確定。

然而，前述的區域電源供應網 300 對於此領域具有通常知識者並不難實作；一般來說，單一個金屬層一般都是用來佈置一種方向的繞線(譬如前述的水平電源供應線或垂直電源供應線)，而相鄰兩金屬層的繞線走向則相互不同；因此，本發明可以利用相鄰的金屬層來建置前述的區域電源供應網 300，此外，於相鄰金屬層中具有相同電性的電源線與接地線彼此之間亦可藉由穿孔(via)相互連接。

在此請參閱第 4 圖，第 4 圖為全域電源供應網 400 之一實施例的示意圖。如第 4 圖所示，全域電源供應網 400 亦為一網狀結構，每個全域電源供應網 400 亦包含有複數條水平電源供應線與複數條垂直電源供應線，均勻地分布於晶片電路之上。於本實施例之中，全域電源供應網 400 係分布於前述區域電源供應網 300 之上，如此一來，全域電源供應網 400 便可透過穿孔(via)耦接至下方的區域電源供應網 300，以將外部電源導入晶片中。

相同地，由於全域電源供應網 400 必須同時供給整個晶片所須的電壓，因此，於全域電源供應網 400 的每一條

水平電源供應線與垂直電源供應線中，必須包含有至少一條共用接地線 403 與兩條電源線 401、402。其中，共用接地線 403 係用來提供對於區域電源供應網 310、320 所須的地電位 V_{GND} ，而兩條電源線 401、402 則分別用來供給部份區域電源供應網 310、320 所須的工作電壓 V_{DD1} 、 V_{DD2} 。

相同地，前述的全域電源供應網 400 對於此領域具有通常知識者亦不難實作；本發明亦可利用相鄰的金屬層來建置前述的全域電源供應網 400，此外，於相鄰金屬層中具有相同電性的電源線與接地線彼此之間亦可藉由穿孔(via)相互連接。

在此請參閱第 5 圖，第 5 圖繪示了全域電源供應網 400 與區域電源供應網 300 的位置示意圖。如第 5 圖所示，全域電源供應網 400 係位於區域電源供應網 300 的上層，而區域電源供應網之中的部份電源供應網 310、320 又位於各電源定義區的上層。

如前所述，全域電源供應網 400 或區域電源供應網 300 各需要兩層金屬層完成之；換句話說，本發明至少需要四層金屬層，來完成前述全域電源供應網 400 與區域電源供應網 300 的建置；然而，在先進製程中，一般都至少保留有四層金屬層(如第 5 圖所示的 M5、M6、M7、M8)，其可用來進行晶片內部各節點的導線連接，因此，本發明係利用這些金屬層來建置全域電源供應網 400 與區域電源供應網 300；舉例來說，於金屬層 M5~M8 之中，區域電源供應網 300 可建置於較低層的金屬層 M5~M6 上(譬如第 3 圖所

繪示的實施例，水平的電源供應線位於金屬層 M5，而垂直的電源供應線位於金屬層 M6)，而全域電源供應網 400 便相對應地建置於較高層的金屬層 M7~M8 上(相同地，如第 4 圖所繪示的實施例，水平的電源供應線位於金屬層 M7，而垂直的電源供應線位於金屬層 M8)。

在此請參閱第 6 圖，第 6 圖繪示了於全域電源供應網 400 與區域電源供應網 300 的俯視圖。於本實施例中，連接到外部電源 V_{DD1} 的電源供應線 401 係藉由穿孔(未繪示於圖中)連接到下層的電源線 311，以將外部電源 V_{DD1} 導入到晶片電路中；連接到外部電源 V_{DD2} 的電源供應線 403 係藉由穿孔連接到下層的電源線 321，以將外部電源 V_{DD2} 導入到晶片電路中；另一方面，連接到外部地電位 V_{GND} 的共用接地線 402 亦藉由穿孔連接到下層的接地線 311、321，以將接地電源 V_{GND} 導入到晶片電路中。

因此，當全域電源供應網 400、區域電源供應網 310、320 的密度夠高，就幾乎可以保證全域電源供應網 400 與下層部分電源供應網 310、320 彼此之間的連接關係，因此，當部分電源供應網 310、320 連接到各電源定義區 110、120 的內部電路時，便可確保外部電源 V_{DD1} 、 V_{DD2} 可以確實地輸入至晶片電路。

此外，這樣的架構還有一個優點。如業界所習知，相較於高層的金屬層，較低層的金屬層更常用來作為連接晶片內部節點的金屬導線佈置之用，因此，其面積便比高層金屬層的面積更來得珍貴；因此，本發明係將具有較少電

源供應線(僅具有一條電源線與一接地線)的區域電源供應網 300 建置於較低層的金屬層 M5、M6 中，以佔用較少的面積；另一方面，本發明係將具有較多電源供應線(具有兩電源線與一共用接地線)的全域電源供應網 400 建置於限制較寬鬆的金屬層 M7~M8 中，如此便可較佳地將金屬層 M5~M6 的面積釋放出來，以進行其他金屬導線的繞線佈置之用。

揭露至此，此領域具有通常知識者應可理解前述的規劃方式與其相關結構，並將前述的規劃方式實作出來，譬如，業者可將前述的規劃方式轉換為一演算法(algorithm)，並將此演算法內建於一電源繞線的開發環境之中(譬如前述的 APR 工具)，以使 APR 工具可以支援多個電源定義區的電源繞線設計。

如前所述，於本實施例中，部分區域電源供應網 310、320 係對應電源定義區 110、120 的位置，且彼此之間形成斷路(部份區域電源供應網 310、320 互相絕緣)；因此，對於 APR 工具來說，一個較簡易的演算法為：先將區域電源供應網 300 均勻地分佈於整體晶片電路之上，接著再從區域電源供應網 300 中將對應電源定義區 110、120 的部分電源供應網定義出來(譬如可根據電源定義區 110、120 的位置，將該區域電源供應網 300 進行切割，使切割後的數個電源供應網彼此之間形成斷路)，以形成前述的部分區域電源供應網 310、320。另一方面，對於 APR 工具來說，全域電源供應網 400 的形成方式較為簡單，僅須將全域電

源供應網 400 均勻地分布於更上層的金屬層即可。

根據前面的揭露，業者便可自行發展出一套合適的 APR 工具，以允許使用者利用 APR 工具，自動地將電源供應網繪製出來，如此便提升了電路設計的效率。

在此請注意，前面所揭露的電路結構與規劃方式僅為本發明之一較佳實施例，而非本發明的限制。於本發明之另一實施例中，本發明亦可省略區域電源供應網 300，僅建置全域電源供應網 400，以將外部電源導入晶片；舉例來說，本發明可直接如第 4 圖所示地將全域電源供應網 400 建置於金屬層 M5、M6 中，如前所述，若全域電源供應網 400 的密度夠稠密，那麼便可確保位於其下層的晶片電路皆可透過插孔(via)耦接至全域電源供應網 400，以接收全域電源供應網 400 所導入的地電位 V_{GND} 與工作電壓 V_{DD1} 、 V_{DD2} ，如此的相對應變化，亦屬本發明的範疇。

而這樣的結構對於 APR 工具的設計來說，也是相當簡易。舉例來說，APR 工具僅須直接將電源供應網均勻地分布於金屬層 M5、M6 之中即可。揭露至此，此領域具有通常知識者應可理解，並實作出其所須的 APR 工具以及電源供應網，故其相關的 APR 開發方式便不另贅述於此。

在此請注意，相較於第 6 圖所示的實施例，由於全域電源供應網包含有兩條電源線以及一條共用接地線，因此直接將其建置於金屬層 M5~M6 的做法，將消耗較大的金屬層 M5、M6 面積；但由於全域電源供應網僅使用一條共用接地線，來供應地電位至不同的電源定義區，因此並不

會造成過大的面積消耗。

相較於習知技術，本發明提供使用者一種電源供應網的規劃方法以相關結構，以允許使用者依循本發明的規劃方式與結構，輕易地將具有多個電源定義區之積體電路的電源供應網設計出來；此外，本發明規劃方法亦可實作於APR工具之中，如此一來，使用者便可藉由APR工具自動地將電源供應網的電路佈局(layout)繪出，更加地提升了電路設計的效率。

以上雖以實施例說明本發明，但並不因此限定本發明之範圍，只要不脫離本發明之要旨，該行業者可進行各種變形或變更。

【圖式簡單說明】

第1圖繪示了一個具有多個電源定義區的晶片。

第2圖為本發明之電源繞線規劃方式之一方法實施例的流程圖。

第3圖為對應第1圖晶片之一實施例的區域電源供應網示意圖。

第4圖為全域電源供應網之一實施例的示意圖。

第5圖為第3圖之區域電源供應網與第4圖之全域電源供應網的位置示意圖。

第6圖為第3圖之區域電源供應網與第4圖之全域電源供應網的俯視圖。

圖式編號

100	晶片
110、120	電源定義區
300	區域電源供應網
310、320	部份區域電源供應網
400	全域電源供應網

拾、申請專利範圍：

1. 一種電源繞線(routing)之規劃方法，其係應用於一具有多個電源定義區(multiple power domain)之積體電路，該規劃方法包含有：

根據該積體電路上一第一電源定義區之位置，形成一第一部份區域電源供應網(local power mesh)；

根據該積體電路上一第二電源定義區之位置，形成一第二部份區域電源供應網；

形成一全域電源供應網(global power mesh)，該全域電源供應網係用來提供該第一電源定義區所須之電源以及該第二電源定義區所須之電源；

將該第一部份區域電源供應網耦接至該全域電源供應網，並且將該第一部份區域電源供應網耦接至該第一電源定義區；以及

將該第二部份區域電源供應網耦接至該全域電源供應網，並且將該第二部份區域電源供應網耦接至該第二電源定義區。

2. 如申請專利範圍第 1 項所述之規劃方法，其中該第一部份區域電源供應網與該第二部份區域電源供應網係位於相同之金屬層。
3. 如申請專利範圍第 2 項所述之規劃方法，其中該全域電源供應網與該第一區域電源供應網係位於不同之金屬層。
4. 如申請專利範圍第 3 項所述之規劃方法，其中該全域電源供應網係位於該第一區域電源供應網之上。

5. 如申請專利範圍第 2 項所述之規劃方法，其中該第一部份區域電源供應網與該第二部份區域電源供應網彼此之間形成斷路。
6. 如申請專利範圍第 1 項所述之規劃方法，其中該全域電源供應網包含有至少一接地線、至少一第一電源線、以及至少一第二電源線，其中該第一電源線係提供該第一電源定義區所須之電源，以及該第二電源線係提供該第二電源定義區所須之電源。
7. 如申請專利範圍第 6 項所述之規劃方法，其中該第一部份區域電源供應網包含有至少一第一區域接地線與至少一第三電源線，該第三電源線係耦接至該第一電源線以及該第一電源定義區，該第一區域接地線耦接至該全域電源供應網之接地線。
8. 如申請專利範圍第 7 項所述之規劃方法，其中該第二部份區域電源供應網包含有至少一第二區域接地線與至少一第四電源線，該第四電源線係耦接至該第二電源線以及該第二電源定義區，該第二區域接地線耦接至該全域電源供應網之接地線。
9. 如申請專利範圍第 8 項所述之規劃方法，其中該第一部份區域接地線與該第二部份區域接地線共享(share)該全域電源供應網之同一接地線。
10. 如申請專利範圍第 1 項所述之規劃方法，其中該第一部份區域電源供應網以及該第二部份區域電源供應網之位置係分別對應於第一電源定義區以及該第二電源定義區。
11. 一種電源繞線架構，其係應用於一具有多個電源定義區(multiple power domain)之積體電路，該電源供應網(power mesh)架構包含有：
一第一部份區域電源供應網(local power mesh)，其位置係對應

一第一電源定義區(power domain)之位置，並且耦接至該第一電源定義區；

一第二部份區域電源供應網，其位置係對應一第二電源定義區(power domain)之位置，並且耦接至該第二電源定義區；以及

一全域電源供應網(global power mesh)，耦接至該第一區域電源供應網以及該第二區域電源供應網，用來分別提供該第一電源定義區與該第二定義區所須之電源；

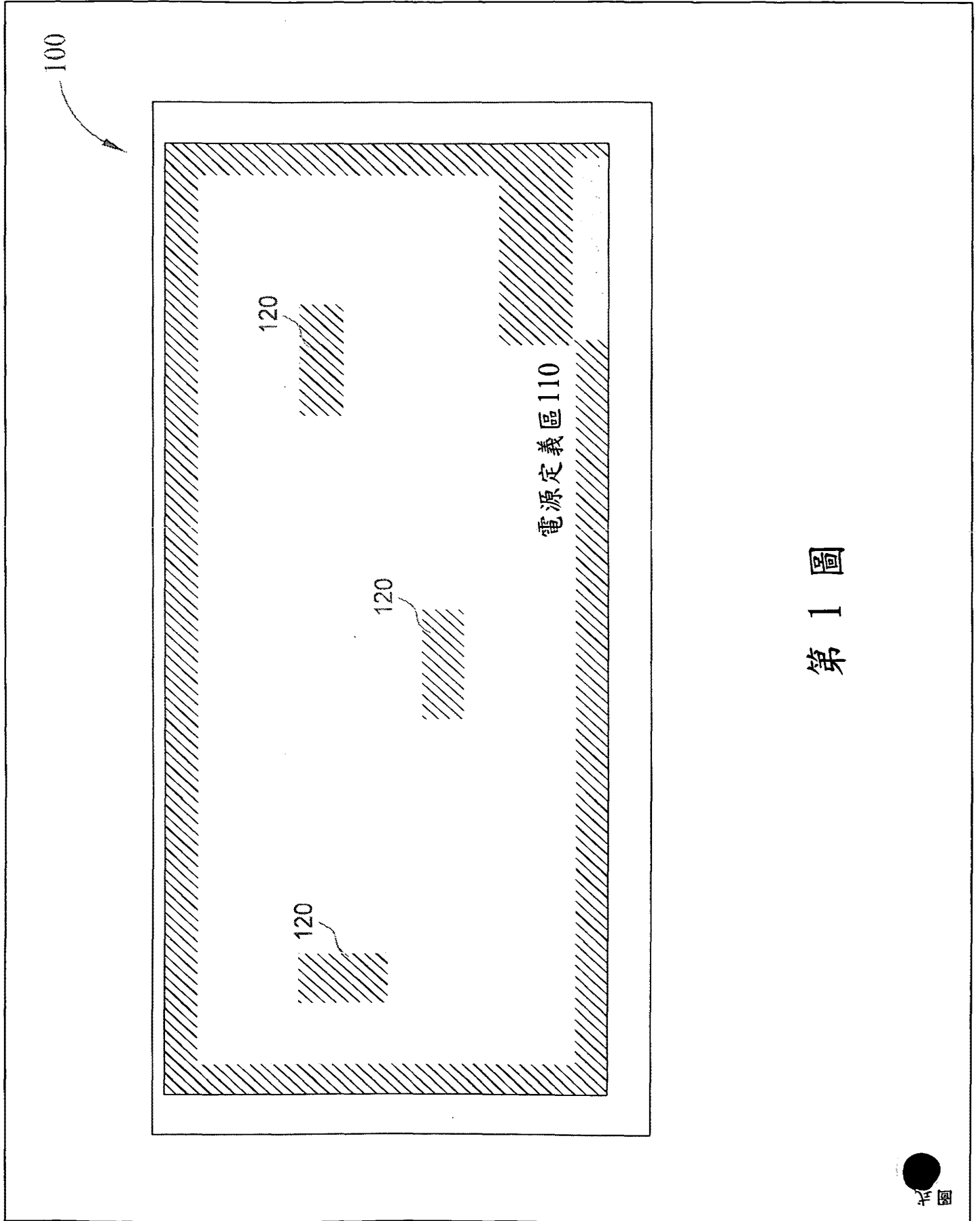
其中該第一部份區域電源供應網與該第二部份區域電源供應網係位於相同之金屬層，且該全域電源供應網與該第一區域電源供應網係位於不同之金屬層。

12. 如申請專利範圍第 11 項所述之電源繞線架構，其中該全域電源供應網係位於該第一區域電源供應網之上。
13. 如申請專利範圍第 12 項所述之電源繞線架構，其中該第一區域電源供應網與該第二區域電源供應網彼此之間形成斷路。
14. 如申請專利範圍第 11 項所述之電源繞線架構，其中該全域電源供應網包含有至少一接地線、至少一第一電源線、以及至少一第二電源線，其中該第一電源線係提供該第一電源定義區所須之電源，以及該第二電源線係提供該第二電源定義區所須之電源。
15. 如申請專利範圍第 14 項所述之電源繞線架構，其中該第一部份區域電源供應網包含有至少一第一區域接地線與至少一第三電源線，該第三電源線係耦接至該第一電源線以及該第一電

源定義區，該第一區域接地線耦接至該全域電源供應網之接地線。

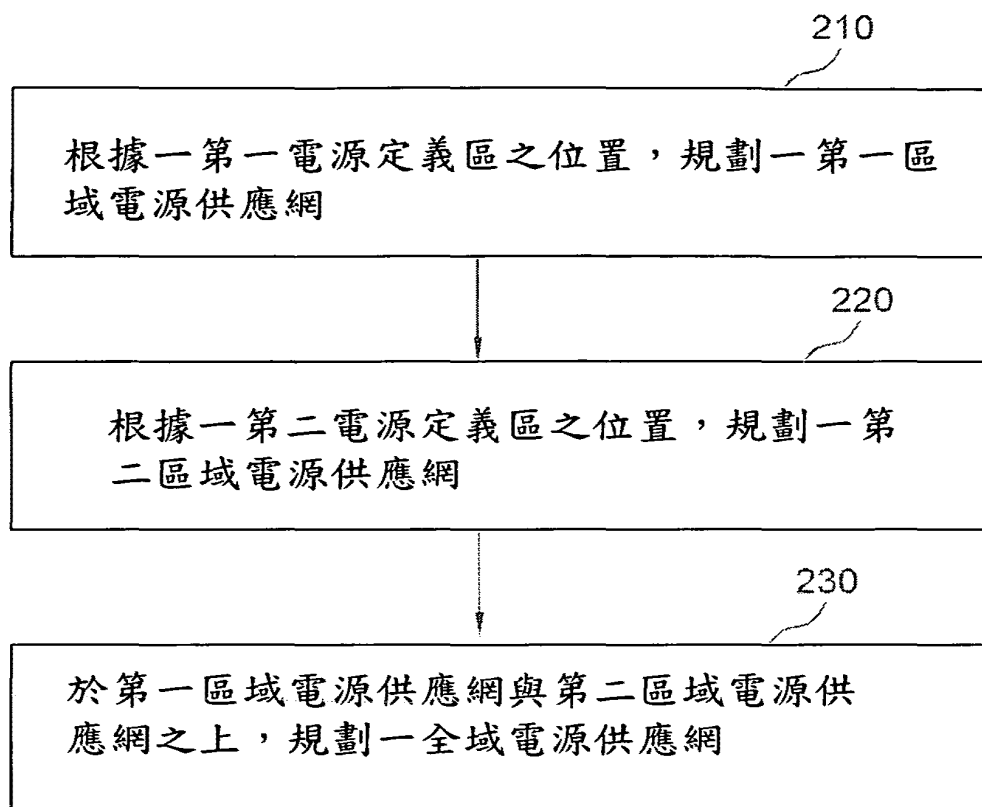
16. 如申請專利範圍第 15 項所述之電源繞線架構，其中該部份第二區域電源供應網包含有至少一第二區域接地線與至少一第四電源線，該第四電源線係耦接至該第二電源線以及該第二電源定義區，該第二區域接地線耦接至該全域電源供應網之接地線。
17. 如申請專利範圍第 16 項所述之電源繞線架構，其中該第一區域接地線與該第二區域接地線共享(share)該全域電源供應網之同一接地線。
18. 一種電源繞線之規劃方法，其係應用於一具有多個電源定義區(multiple power domain)之積體電路，該規劃方法包含有：
 - 一全域電源供應網(global power mesh)，該全域電源供應網係位於一第一電源定義區以及一第二電源定義區之上，其包含有至少一接地線、至少一第一電源線、以及至少一第二電源線，其中該第一電源線係提供該第一電源定義區所須之電壓，以及該第二電源線係提供該第二電源定義區所須之電壓，該接地線係提供該第一電源定義區與該第二電源定義區所須之地電位；
 - 將該全域電源供應網之該第一電源線與該接地線耦接至該第一電源定義區；以及
 - 將該全域電源供應網之該第二電源線與該接地線耦接至該第二電源定義區。

19. 如申請專利範圍第 17 項所述之規劃方法，其中該第一電源定義區與該第二電源定義區共享(share)該全域電源供應網之同一接地線。
20. 一種電源繞線架構，其係應用於一具有多個電源定義區(multiple power domain)之積體電路，該電源繞線架構包含有：
一全域電源供應網(global power mesh)，係位於一第一電源定義區以及一第二電源定義區之上，該全域電源供應網包含有：
至少一接地線，耦接至該第一電源定義區與該第二電源定義區，用來提供該第一電源定義區與該第二電源定義區所須之地電位；
至少一第一電源線，耦接至該第一電源定義區，用來提供該第一電源定義區所須之電壓；以及
至少一第二電源線，耦接至該第二電源定義區，用來提供該第二電源定義區所須之電壓。
21. 如申請專利範圍第 20 項所述之電源繞線架構，其中該第一電源定義區與該第二電源定義區共享(share)該全域電源供應網之同一接地線。

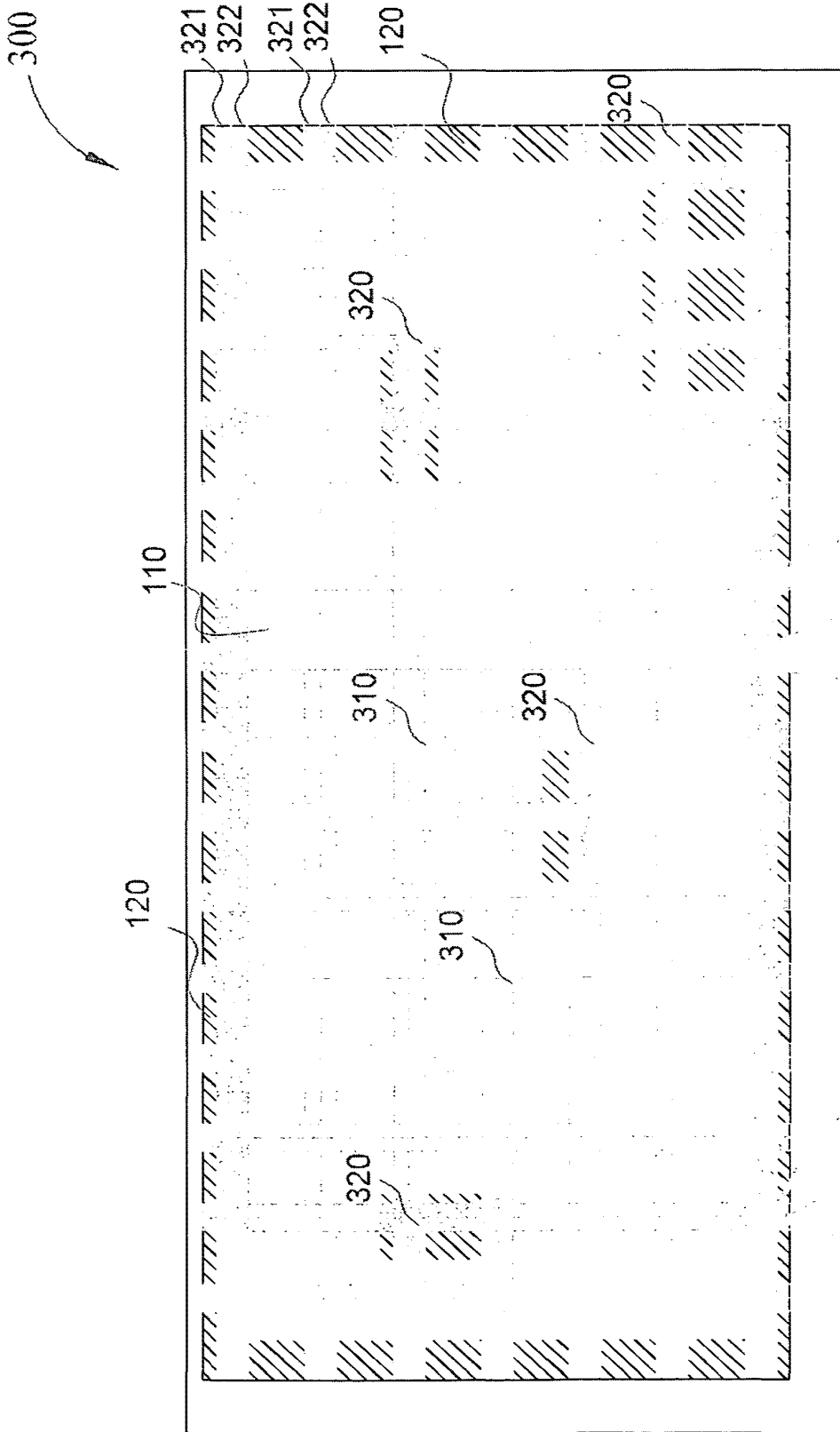


第 1 圖



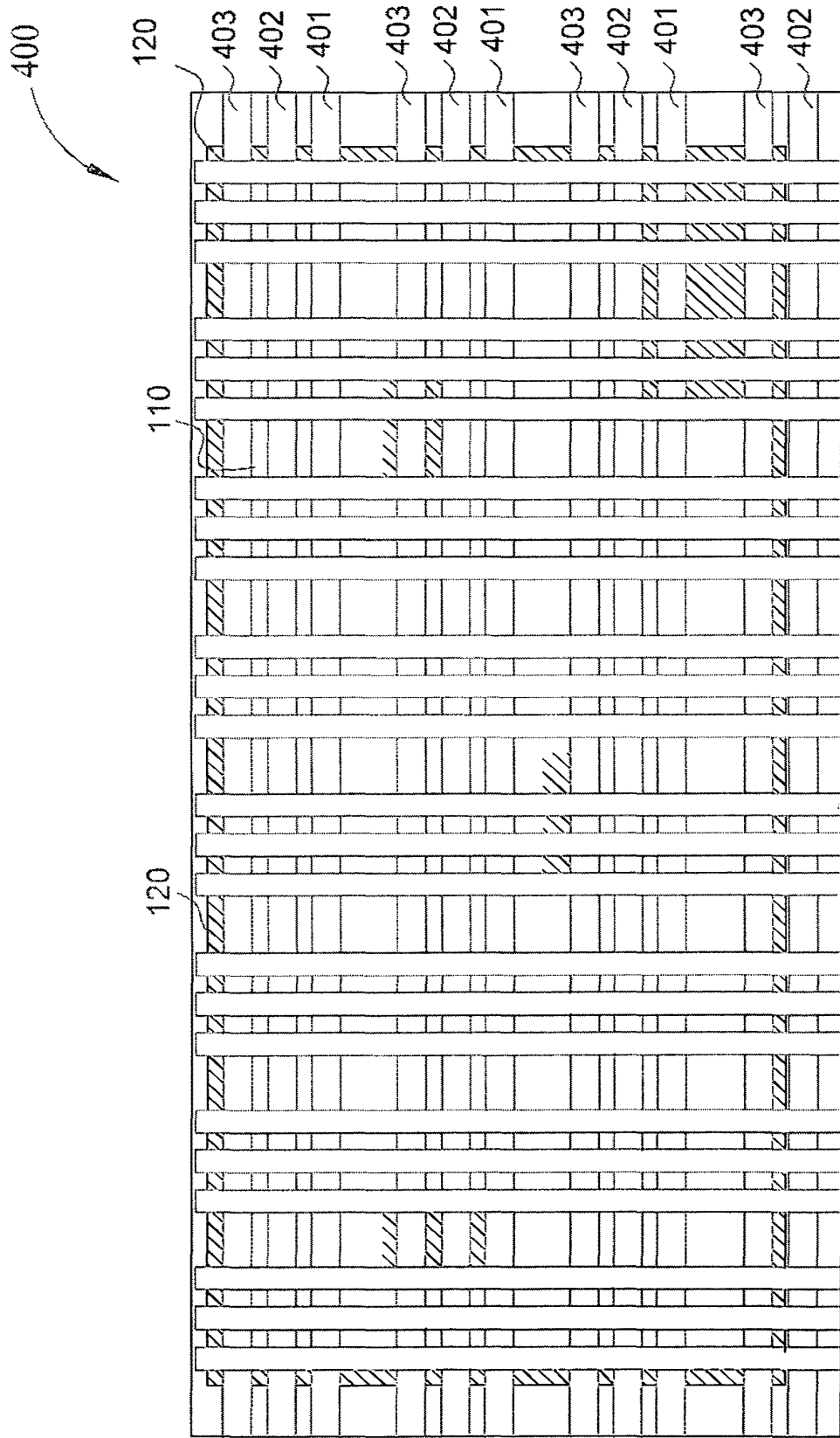


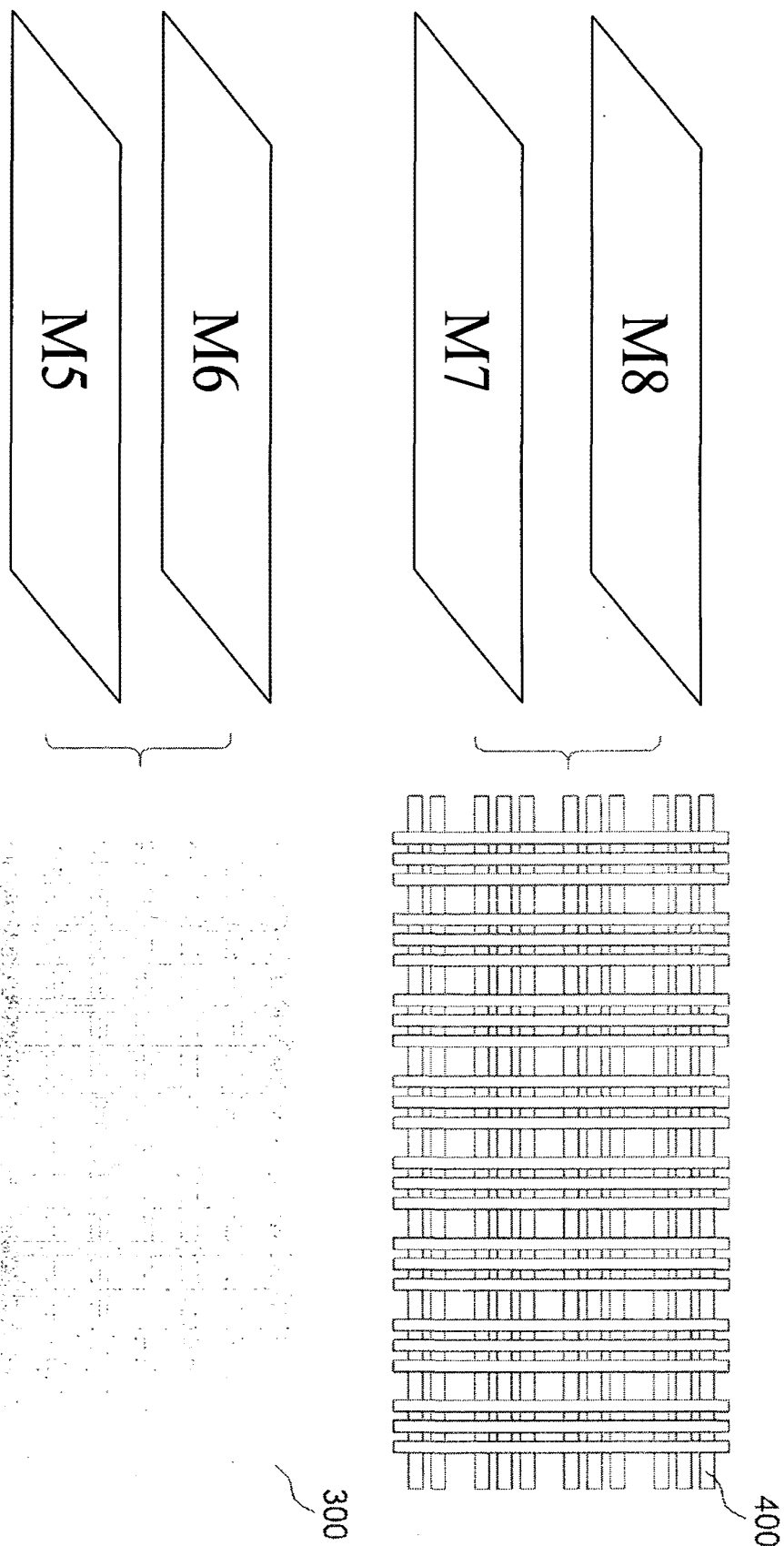
第 2 圖



第 3 圖

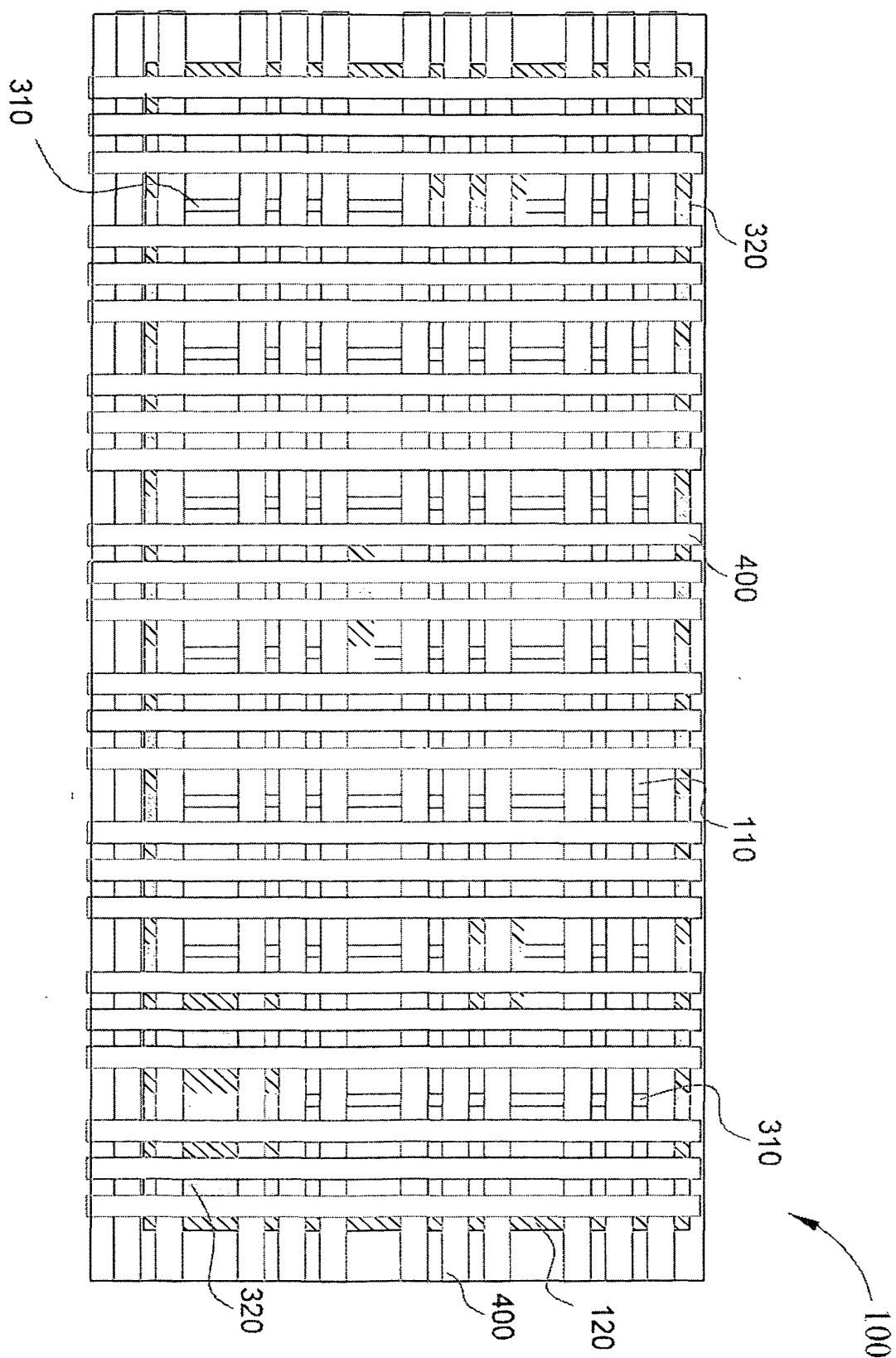
第 4 圖





第 5 圖

第 6 圖





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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
12/271,534	11/14/2008	2617	1090	3722/0536PUS1	20	3

CONFIRMATION NO. 4308

60601

Muncy, Geissler, Olds & Lowe, PLLC
P.O. BOX 1364
FAIRFAX, VA 22038-1364

FILING RECEIPT



OC000000033328675

Date Mailed: 12/01/2008

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Chia-Lin Chuang, Hsinchu City, TAIWAN;

Power of Attorney: The patent practitioners associated with Customer Number 60601

Domestic Priority data as claimed by applicant

Foreign Applications

TAIWAN 096143160 11/15/2007

If Required, Foreign Filing License Granted: 11/26/2008

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/271,534**

Projected Publication Date: 05/21/2009

Non-Publication Request: No

Early Publication Request: No

Title

POWER MESH ARRANGEMENT METHOD UTILIZED IN AN INTEGRATED CIRCUIT HAVING
MULTIPLE POWER DOMAINS

Preliminary Class

370

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER**Title 35, United States Code, Section 184****Title 37, Code of Federal Regulations, 5.11 & 5.15****GRANTED**

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where

the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).



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MUNCY GEISSLER OLDS & LOWE PLLC
PO BOX 1364
FAIRFAX VA 22038-1364

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DEC 19 2008

OFFICE OF PETITIONS

In re Application of :
Chia-Lin Chuang :
Application No. 12/271,534 : DECISION ACCORDING STATUS
Filed: November 14, 2008 : UNDER 37 CFR 1.47(b)
Attorney Docket No. 3722/0536PUS1 :

This is in response to the petition under 37 CFR 1.47(b), filed with the application on November 14, 2008.

The petition under 37 C.F.R. § 1.47(b) is GRANTED.

With the instant petition, Rule 47(b) applicant has attested that a copy of the application papers was forwarded to Chuang. However, Chuang made an oral refusal to sign the papers in a telephone conversation on July 28, 2008. Rule 47(b) applicant has included a statement from Tien, the person to whom the refusal was made.

The petition and declaration have been reviewed and determined to be in compliance with 37 C.F.R. § 1.47(b).

The application is hereby accorded Rule 47 status.

As provided in 37 C.F.R. § 1.47(c), the Office will provide notice of this application's filing to the non-signing inventor at the last known address provided in the petition. Notice will also be provided in the Official Gazette.

Telephone inquiries related to this decision may be directed to the undersigned at (571)272-3207.

A handwritten signature in black ink, appearing to read "Cliff Congo".

Cliff Congo
Petitions Attorney
Office of Petitions



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www.uspto.gov

CHIA-LIN CHUANG
167-1 CHANGCHUN ST
300 HSINCHU CITY
TAIWAN ROC

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DEC 19 2008

OFFICE OF PETITIONS

In re Application of :
Chia-Lin Chuang :
Application No. 12/271,534 :
Filed: November 14, 2008 : LETTER
Title: Power Mesh Arrangement Method :
Utilized in an Integrated Circuit :
Having Multiple Power Domains :

Dear Chia-Lin Chuang:

You are named as the inventor of the above-identified United States patent application filed under the provisions of 35 USC 116 (United States Code) and 37 CFR 1.47(b), Rules of Practice in Patent Cases. Should a patent be granted on the application you will be designated therein as the sole inventor.

As the named inventor you are entitled to inspect any paper in the file wrapper of the application, order copies of all or any part thereof (at a prepaid cost per 37 CFR 1.19) or make your position of record in the application. Alternatively, you may arrange to do any of the preceding through a registered patent attorney or agent presenting written authorization from you. If you care to join the application, agent of record would presumably assist you. Joining in the application would entail the filing of an appropriate oath or declaration by you pursuant to 37 CFR 1.63.

Telephone inquiries regarding this communication should be directed to Petitions Attorney Cliff Congo at (571)272-3207. Requests for information regarding your application should be directed to the File Information Unit at (703) 308-2733. Information regarding how to pay for and order a copy of the application, or a specific paper in the application, should be directed to the Certification Division at (703) 308-9726 or 1-800-972-6382 (outside the Washington D.C. area).

Cliff Congo
Petitions Attorney
Office of Petitions



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Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/271,534	11/14/2008	Chia-Lin Chuang	3722/0536PUS1

CONFIRMATION NO. 4308

PUBLICATION NOTICE



OC000000036093698

60601
Muncy, Geissler, Olds & Lowe, PLLC
P.O. BOX 1364
FAIRFAX, VA 22038-1364

Title:POWER MESH ARRANGEMENT METHOD UTILIZED IN AN INTEGRATED CIRCUIT HAVING MULTIPLE POWER DOMAINS

Publication No.US-2009-0132988-A1

Publication Date:05/21/2009

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	12/271,534
				Filing Date	Nov 14, 2008
				First Named Inventor	CHUANG, Chia-Lin
				Art Unit	2825
				Examiner Name	CHIANG, Jack
				Attorney Docket Number	3722/0536PUS1
Sheet	1	of	1		

[illegible][illegible]

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): CHUANG, Chia-Lin	Examiner: CHIANG, Jack
Application No.: 12/271,534	Art Unit: 2825
Filed: 14 Nov 2008	Confirmation Number: 4308
Title: A POWER MESH ARRANGEMENT METHOD UTILIZED IN AN INTEGRATED CIRCUIT HAVING MULTIPLE POWER DOMAINS	
Attorney Docket No.: 3722/0536PUS1	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

This Information Disclosure Statement is submitted:

- ☒ under 37 CFR 1.97(b), or
(within three months of filing national application or date of entry of international application; before mailing date of first office action on the merits; or before the mailing of a first Office action after the filing of a request for continued examination)
- ☐ under 37 CFR 1.97(c) together with either a:
☐ statement under 37 CFR 1.97(e), **or**
☐ a \$180.00 fee under 37 CFR 1.17(p),
(after the CFR 1.97(b) time period, but before final action or notice of allowance, whichever occurs first)
- ☐ under 37 CFR 1.97(d) together with a:
☐ statement under 37 CFR 1.97(e), **and**
☐ a \$180.00 fee set forth in 37 CFR 1.17(p).
(filed after final action or notice of allowance, whichever occurs first, but before payment of the issue fee)

Statement under 37 CFR 1.97(e) (if applicable):

☐ Each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not

more than three months prior to the filing of the information disclosure statement (37 CFR 1.97(e)(1)).

☐ No item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in § 1.56(c) more than three months prior to the filing of the information disclosure statement (37 CFR 1.97(e)(2)).

I. LIST OF PATENTS, PUBLICATIONS OR OTHER INFORMATION

The patents, publications, or other information submitted for consideration by the Office are listed on the PTO/SB/08 attached hereto.

II. COPIES (check at least one box)

a. ☒ Submitted herewith is a legible copy of (i) each foreign patent; (ii) each publication or that portion which caused it to be listed; and (iii) all other information or that portion which caused it to be listed.

b. ☒ Some or all of the documents listed on the PTO/SB/08 are not enclosed because they are either U.S. Patents or Published Applications or were cited in the International Search Report and copies should already be in the PTO file. If copies are needed, please contact the undersigned.

c. ☐ As provided in 37 CFR 1.98(d), some or all of the documents listed on the PTO/SB/08 are not enclosed because they were cited in the parent application(s). Accordingly, copies are not submitted herewith.

III. CONCISE EXPLANATION OF THE RELEVANCE
(check at least one box)

a. ☐ DOCUMENTS IN THE ENGLISH LANGUAGE

The attached patents, publications, or other information in the English language do not require a statement of relevancy.

b. ☒ DOCUMENTS NOT IN THE ENGLISH LANGUAGE

A concise explanation of the relevance of all patents, publications, or other information listed that is not in the English language is as follows: CN1411052 corresponds to US 6,901,566 and CN 1701436 corresponds to US 2005/0161810. Please be advised that an English Abstract is enclosed for both of the Chinese Documents.

c. ☐ ENGLISH LANGUAGE SEARCH REPORT

An English language version of the search report or action that indicates the degree of relevance found by the foreign office is attached, thereby satisfying the requirement for a concise explanation. See MPEP 609(III)(A)(3).

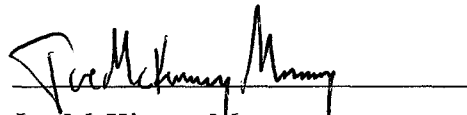
d. ☐ OTHER

The following additional information is provided for the Examiner's consideration.

It is requested that the information disclosed herein be made of record in this application. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account **50-3828** and please credit any excess fees to such deposit account.

Date: May 14, 2010

Respectfully submitted,


Joe McKinney Muncy
Attorney/Agent for Applicant(s)
Reg. No. 32334

Muncy, Geissler, Olds & Lowe, PLLC
PO Box 1364
Fairfax, VA 22038-1364
Tel. 703.621.7140
mailroom@mg-ip.com

Electronic Acknowledgement Receipt

EFS ID:	7612573
Application Number:	12271534
International Application Number:	
Confirmation Number:	4308
Title of Invention:	POWER MESH ARRANGEMENT METHOD UTILIZED IN AN INTEGRATED CIRCUIT HAVING MULTIPLE POWER DOMAINS
First Named Inventor/Applicant Name:	Chia-Lin Chuang
Customer Number:	60601
Filer:	Joe McKinney Muncy/Melody Prochazka
Filer Authorized By:	Joe McKinney Muncy
Attorney Docket Number:	3722/0536PUS1
Receipt Date:	14-MAY-2010
Filing Date:	14-NOV-2008
Time Stamp:	11:40:11
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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Warnings:					
Information:					
3	Foreign Reference	CN1411052.pdf	680858 7bf3b1ca7cb5826b269a24aee311947ddf70b363	no	16
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Information:					
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Information:					
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/271,534

11/14/2008

Chia-Lin Chuang

3722/0536PUS1

4308

60601 7590 01/19/2011
Muncy, Geissler, Olds & Lowe, PLLC
4000 Legato Road
Suite 310
FAIRFAX, VA 22033

EXAMINER

LEVIN, NAUM B

ART UNIT

PAPER NUMBER

2825

MAIL DATE

DELIVERY MODE

01/19/2011

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 12/271,534	Applicant(s) CHUANG, CHIA-LIN	
	Examiner NAUM LEVIN	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 November 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 November 2008 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☒ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413) |
| 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) ☒ Information Disclosure Statement(s) (PTO/SB/08) | 5) ☐ Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>5/14/10</u> . | 6) ☐ Other: _____ |

DETAILED ACTION

1. This office action is in response to application 12/271,534 filed on 11/14/2008.

Claims 1-20 are pending in the application.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Based upon consideration of all of the relevant factors with respect to the claim as a whole, claim 1 holds to claim an abstract idea, and is/are therefore rejected as ineligible subject matter under 35 U.S.C. 101. The rationale for this finding is explained below: a method that recites purely mental steps is descriptive material and is not statutory if the **steps in the body of claim** not claimed as method (1) tied to another statutory class (such as a particular apparatus) or (2) transform underlying subject matter (such as an article or materials) to a different state or thing (see MPEP 2106.01).

3. Based upon consideration of all of the relevant factors with respect to the claim as a whole, claim 19 holds to claim an abstract idea, and is/are therefore rejected as ineligible subject matter under 35 U.S.C. 101. The rationale for this finding is explained below: a method that recites purely mental steps is descriptive material and is not statutory if the **steps in the body of claim** not claimed as method (1) tied to another statutory class (such as a particular apparatus) or (2) transform underlying

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subject matter (such as an article or materials) to a different state or thing (see MPEP 2106.01).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 6-10, 15-18 and 20 are rejected under 35 U.S.C. 102 (b) as being unpatentable over Iadanza et al. (U.S. Patent 7,000,214).

5. As to claim 1 Iadanza discloses:

Claim 1 A power routing arrangement method applied in an integrated circuit having multiple power domains (Abstract), **the arrangement method comprising:**

forming a first partial local power mesh (the noise-modeling tool combines information from circuit level profile file 250 and netlist 240 to form a mesh model of the IC device in each voltage domain/power domain, for example, forms mesh for voltage domain/island 105/first partial local power mesh - col.10, ll.5-9; Fig.1 ... each voltage/power domain/island has internal (local) power distribution network/power mesh - col.2, ll.35-38) **according to the position of a first power domain of the integrated circuit** (according to, for example, a preliminary floorplan proposal to the modeling tool to override synthesis-generated voltage domain/power domain sizes and specify

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relative locations, e.g., position of voltage domain/island 105/first power domain of the IC – col.9, ll.61-67; col.10, ll.1-4; Fig.1);

forming a second partial local power mesh (the noise-modeling tool combines information from circuit level profile file 250 and netlist 240 to form a mesh model of the IC device in each voltage domain/power domain, for example, forms mesh for voltage domain/island 110/second partial local power mesh - col.10, ll.5-9; Fig.1 ... for each voltage/power domain/island internal (local) power distribution network/power mesh has been formed - col.2, ll.35-38)**according to the position of a second power domain of the integrated circuit** (according to, for example, a preliminary floorplan proposal to the modeling tool to override synthesis-generated voltage domain/power domain sizes and specify relative locations, e.g., position of voltage domain/island 110/second power domain of the IC – col.9, ll.61-67; col.10, ll.1-4; Fig.1);

forming a global power mesh that is utilized to provide the power needed by the first and the second power domains (power/voltage connections for chip level are defined/formed as global in voltage definition file 205 and as a result, VDD and VSS rails for logic inferred within block 500 (see FIG. 3) are connected to global sources/forming a global power mesh that is utilized to provide the power needed by the first and the second power domains - col.9, ll.25-37; Figs.1, 3);

coupling the first partial local power mesh to the global power mesh and the first power domain (coupling connection declaration 511/first partial local power mesh using logic instantiation coding section 502 to the chip-level connection

declaration 501/global power mesh and voltage domain/island 510/105/first power domain - col.4, ll.3-27; Figs.1, 3); **and**

coupling the second partial local power mesh to the global power mesh and the second power domain (coupling connection declaration 521/second partial local power mesh using logic instantiation coding section 502 to the chip-level connection declaration 501/global power mesh and voltage domain/island 520/110/second power domain - col.4, ll.3-17; col.4, ll.35-44; Figs.1, 3).

6. As to claims 6-10, 15-18, 20 Iadanza discloses:

Claims 6, 15 The arrangement method/structure, wherein the global power mesh comprises at least one ground wire, at least one first power wire that provides power to the first power domain, and at least one second power wire that provides power to the second power domain (col.5, ll.60-67; col.6, ll.1-25; Figs.1, 3-4);

Claims 7-9, 16-18, 20 The arrangement method/structure, wherein the first partial local power mesh comprises: at least one first local ground wire that couples to the ground wire of the global power mesh; and at least one third power wire that couples to the first power wire and the first power domain (col.3, ll.12-49; col.4, ll.3-27; col.5, ll.60-67; col.6, ll.1-25; Figs.1-4);

Claim 10 The arrangement method, wherein the positions of the first partial local power mesh and the second partial local power mesh correspond to the first

power domain and the second power domain, respectively (col.2, ll.35-38; col.9, ll.61-67; col.10, ll.1-9; Fig.1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 2-5, 11-14 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iadanza in view of Chen et al. (U.S. Patent 7,234,124).

8. As to claim 12 Iadanza discloses:

Claim 12 A power routing structure applied in an integrated circuit having multiple power domains (Abstract; col.1, ll.8-11; Fig.8), **comprising:**

a first partial local power mesh coupling to the first power domain(the noise-modeling tool combines information from circuit level profile file 250 and netlist 240 to form a mesh model of the IC device in each voltage domain/power domain, for example, forms mesh for voltage domain/island 105/coupling to first partial local power mesh - col.10, ll.5-9; Fig.1 ... each voltage/power domain/island has internal (local) power distribution network/power mesh - col.2, ll.35-38) **and having its position corresponding to the position of a first power domain** (according to, for example, a preliminary floorplan proposal to the modeling tool to override synthesis-generated voltage domain/power domain sizes and specify relative locations, e.g., position of

voltage domain/island 105/first power domain of the IC – col.9, ll.61-67; col.10, ll.1-4;
Fig.1);

a second partial local power mesh coupling to the first power domain(the noise-modeling tool combines information from circuit level profile file 250 and netlist 240 to form a mesh model of the IC device in each voltage domain/power domain, for example, forms mesh for voltage domain/island 110/coupling to second partial local power mesh - col.10, ll.5-9; Fig.1 ... each voltage/power domain/island has internal (local) power distribution network/power mesh - col.2, ll.35-38) **and having its position corresponding to the position of a second power domain** (according to, for example, a preliminary floorplan proposal to the modeling tool to override synthesis-generated voltage domain/power domain sizes and specify relative locations, e.g., position of voltage domain/island 110/second power domain of the IC – col.9, ll.61-67; col.10, ll.1-4; Fig.1);

a global power mesh, coupling the first partial local power mesh (using logic instantiation coding section 502 of the chip-level connection declaration 501/global power mesh to couple to connection declaration 511/first partial local power mesh and connection declaration 521/second partial local power mesh - col.4, ll.3-27; col.4, ll.35-44 Figs.1, 3); **and**

coupling the second partial local power mesh to the global power mesh and the second power domain (coupling connection declaration 521/second partial local power mesh using logic instantiation coding section 502 to the chip-level connection declaration 501/global power mesh and voltage domain/island

520/110/second power domain - col.4, ll.3-17; col.4, ll.35-44; Figs.1, 3) **to provide the power needed by the first and the second power domains separately**(power/voltage connections for chip level are defined/formed as global in voltage definition file 205 and as a result, VDD and VSS rails for logic inferred within block 500 (see FIG. 3) are connected to global sources/forming a global power mesh that is utilized to provide the power needed by the first and the second power domains separately - col.9, ll.25-37; Figs.1, 3);

Claim 19 A power routing arrangement method applied in an integrated circuit having multiple power domains (Abstract; col.1, ll.8-11), **the arrangement method comprising:**

providing a global power mesh (power/voltage connections for chip level are defined/provided as global in voltage definition file 205 and as a result, VDD and VSS rails for logic inferred within block 500 (see FIG. 3) are connected to global sources/forming a global power mesh that is utilized to provide the power needed by the first and the second power domains - col.9, ll.25-37; Figs.1, 3), **comprising at least one first power wire that provides the voltage needed by the first power domain** (as shown in Figs. 3 and 4, chip-level connection declaration 501/global power mesh provides at least one “WIRE VDD2”/first power wire supplying VDD voltage of 1.5V needed by the first voltage/island/power domain A/510/105 – col.5, ll.60-67; col.6, ll.1-25; Figs.1, 3-4), **at least one second power wire that provides the voltage needed by the second power domain** (as shown in Figs. 3 and 4, chip-level connection declaration 501/global power mesh provides at least one “WIRE”/second power wire

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supplying VDD voltage of 1.2V needed by the second voltage/island/power domain A/520/110 – col.5, ll.60-67; col.6, ll.1-25; Figs.1, 3-4), **and at least one ground wire that provides the ground potential needed by the first power domain and the second power domain** (as shown in Figs. 3 and 4, chip-level connection declaration 501/global power mesh provides VSS rail/at least one ground wire to the first voltage/island/power domain A/510/105 and second voltage/island/power domain A/520/110 - col.5, ll.60-67; col.6, ll.1-25; Figs.1, 3-4);

coupling the first power wire and the ground wire of the global power mesh to the first power domain (col.5, ll.60-67; col.6, ll.1-25; Figs.1, 3-4); **and**

coupling the second power wire and the ground wire of the global power mesh to the second power domain (col.5, ll.60-67; col.6, ll.1-25; Figs.1, 3-4).

With respect to claims 12 and 19 Iadanza teaches the features above but lacks a power routing structure/method, wherein global power mesh is positioned in a layer located above a layer where local power domain is positioned.

9. As to claims 12, 19 Chen in combination of Iadanza teaches:

A power routing structure/method, wherein global power mesh is positioned in a layer located above a layer where local power domains are positioned (a method and apparatus/structure for distributing and routing power in an integrated circuit having voltage islands, wherein chip-wide/second/global power grid is positioned on metal level/layer N, which is above a levels 1 to N-1, where a first/local power grid is generated/positioned for a voltage islands/local power domains – Abstract; col.1, ll.10-37; col.1, ll.58-64; Figs.1- 3).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Chen's teaching regarding the power routing structure/method, wherein global power mesh is positioned in a layer located above a layer where local power domain is positioned to improve Iadanza's invention by avoiding restriction placement of power service terminals contained within the voltage island circuits because of a locally sparse power grid, avoiding electromigration and IR drop violations and avoiding blocked pins and other wireability issues in multilayered IC (col.1, ll.42-51).

10. As to claims 2-5, 11 and 13-14 Chen in combination with Iadanza recites:

Claim 2 The arrangement method, wherein the first partial local power mesh and the second partial local power mesh are positioned on the same metal layer (see Iadanza – Fig.1);

Claims 3-4, 13 The arrangement method/structure, wherein the global power mesh and the first local power mesh are positioned on different metal layers and global power mesh is positioned above the first local power mesh (see Chen - Abstract; col.1, ll.10-37; col.1, ll.58-64; Figs.1-3);

Claims 5, 14 The arrangement method/structure, wherein the first partial local power mesh and the second partial local power mesh are not electrically coupled (see Chen - col.1, ll.10-37);

Claim 11 The arrangement method, wherein the global power mesh is distributed evenly above the first local power mesh (see Chen - Abstract; col.1, ll.58-64; col.2, ll.28-42; Figs.1-2).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NAUM LEVIN whose telephone number is (571)272-1898. The examiner can normally be reached on 6:30 am - 2:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, JACK CHIANG can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/NAUM LEVIN/
Primary Examiner, Art Unit 2825

Notice of References Cited	Application/Control No. 12/271,534		Applicant(s)/Patent Under Reexamination CHUANG, CHIA-LIN	
	Examiner NAUM LEVIN		Art Unit 2825	Page 1 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-4,811,237 A	03-1989	Putatunda et al.	716/127
*	B	US-6,493,859 B1	12-2002	Gould et al.	716/127
*	C	US-6,538,314 B1	03-2003	Buffet et al.	257/691
*	D	US-6,725,439 B1	04-2004	Homsinger et al.	716/115
*	E	US-6,883,152 B2	04-2005	Bednar et al.	716/113
*	F	US-2005/0091629 A1	04-2005	Eisenstadt et al.	716/13
*	G	US-7,000,214 B2	02-2006	Iadanza et al.	716/104
*	H	US-2006/0184905 A1	08-2006	Floyd et al.	716/5
*	I	US-7,119,578 B2	10-2006	Correale et al.	326/81
*	J	US-2007/0094630 A1	04-2007	Bhooshan, Rishi	716/13
*	K	US-7,234,124 B2	06-2007	Chen et al.	716/127
*	L	US-7,296,251 B2	11-2007	Dhanwada et al.	716/113
*	M	US-7,610,572 B2	10-2009	Kanno et al.	716/138

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Notice of References Cited	Application/Control No. 12/271,534		Applicant(s)/Patent Under Reexamination CHUANG, CHIA-LIN	
	Examiner NAUM LEVIN		Art Unit 2825	Page 2 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-7,694,241 B1	04-2010	Jadcherla et al.	716/127
*	B	US-7,760,011 B2	07-2010	Wang et al.	327/544
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

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CONFIRMATION NO. 4308

SERIAL NUMBER 12/271,534	FILING or 371(c) DATE 11/14/2008 RULE 1.47	CLASS 716	GROUP ART UNIT 2825	ATTORNEY DOCKET NO. 3722/0536PUS1		
APPLICANTS Chia-Lin Chuang, Hsinchu City, TAIWAN; ** CONTINUING DATA ☒ None ☐ NL ***** ** FOREIGN APPLICATIONS ☒ Yes ☐ NL ***** TAIWAN 096143160 11/15/2007 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 11/26/2008						
Foreign Priority claimed ☒ Yes ☐ No 35 USC 119(a-d) conditions met ☒ Yes ☐ No Verified and Acknowledged /NAUM B LEVIN/ ☒ NL Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY TAIWAN	SHEETS DRAWINGS 6	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 3
ADDRESS Muncy, Geissler, Olds & Lowe, PLLC 4000 Legato Road Suite 310 FAIRFAX, VA 22033 UNITED STATES						
TITLE POWER MESH ARRANGEMENT METHOD UTILIZED IN AN INTEGRATED CIRCUIT HAVING MULTIPLE POWER DOMAINS						
FILING FEE RECEIVED 1090	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit			

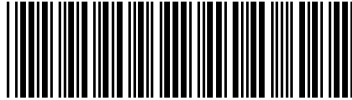
Search Notes 	Application/Control No. 12271534	Applicant(s)/Patent Under Reexamination CHUANG, CHIA-LIN
	Examiner NAUM LEVIN	Art Unit 2825

SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
EAST (US-PGPUB, USPAT, EPO, JPO, DERWENT, IBM_TDB) - See search history printouts	1/6/2011	N L

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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<i>Index of Claims</i> 	Application/Control No. 12271534	Applicant(s)/Patent Under Reexamination CHUANG, CHIA-LIN
	Examiner NAUM LEVIN	Art Unit 2825

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant		☐ CPA		☐ T.D.		☐ R.1.47			
CLAIM		DATE							
Final	Original	01/06/2011							
	1	✓							
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	19	✓							
	20	✓							

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	("20090132988").PN.	US-PGPUB; USPAT	OR	OFF	2011/01/04 08:24
S2	2068	local with (power voltage) with (mesh grid gridiron grating)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 08:30
S3	13116	(domain island) near3 (power voltage)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 08:31
S4	129	S2 and S3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 08:31
S5	516934	global	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 08:31
S6	53	S4 and S5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 08:31
S7	52286	plac\$5 with (routing wiring)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 08:32
S8	3	S6 and S7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 08:32
S9	3	S4 and S7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 08:40

S10	496	(domain island) with (power voltage) with (mesh grid gridiron grating)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 08:42
S11	53	S10 and S7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 08:42
S12	5274489	layer	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 08:43
S13	33	S11 and S12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 08:43
S14	908	slice near6 (mesh grid gridiron grating)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 09:38
S15	0	S14 and S3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 09:38
S16	1509	slice with (mesh grid gridiron grating)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 09:39
S17	0	S16 and S3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 09:39
S18	106429	(domain island region) near3 (power voltage)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 10:16
S19	14242	floorplan\$4 (floor adj plan \$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 10:17

S20	560	S18 and S19	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 10:17
S21	77702	(power voltage) with (mesh grid gridiron grating)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 10:18
S22	154	S20 and S21	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 10:18
S23	84158	cad cae eda	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 10:19
S24	3080066	cad cae eda automatic\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 10:20
S25	114	S22 and S24	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 10:20
S26	47	S23 and S25	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 10:20
S27	13394	local\$2 with (mesh grid gridiron grating)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 10:22
S28	7	S26 and S27	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 10:22
S29	1458	(domain island region) with ((power voltage) near3 (grid mesh gridiron grating))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 13:33

S30	400	S29 and S24	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 13:33
S31	46	S30 and S19	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/04 13:34
S33	2	((("20050161810") or ("6,901,566")).PN.	US-PGPUB; USPAT	OR	OFF	2011/01/05 07:37
S34	1226	(multi adj voltage) (multi- voltage) (multi adj supply) (multi-supply)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 09:00
S35	3507345	(domain island region)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 09:00
S36	405	S34 and S35	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 09:01
S37	369	(layer level) and S36	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 09:03
S38	178	(rout\$3 wir\$3) and S37	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 09:03
S39	3080066	cad cae eda automatic\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 09:04
S40	80	S39 and S38	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 09:04
S41	1178985	(mesh grid gridiron grating)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 09:09

S42	13	S40 and S41	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 09:09
S43	548761	power near4 consumption	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 10:04
S44	325	S43 and S34	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 10:04
S45	297	(layer level) and S44	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 10:04
S46	31	S45 and S41	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 10:04
S47	133466	(global bus rail) near4 (power supply voltage)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 10:10
S48	22918	S43 and S47	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 10:10
S49	19139	(layer level) and S48	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 10:10
S50	80	S40 and S34	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 10:11
S51	80	(layer level) and S50	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 10:11

S52	13	S51 and S41	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 10:11
S53	1201	levin.xa. levin.xp.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 10:32
S54	167	(mesh grid) and S53	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 10:33
S55	0	S54 and slice	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 10:33
S56	28	S54 and consumption	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 10:33
S57	15	S56 and S35	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 10:37
S58	2	S57 and S47	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 10:41
S59	186374	(layer m\$1) with (mesh grid gridiron grating)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 11:59
S60	538196	(layer m\$1) with (mesh grid gridiron grating distribution network)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 12:00
S61	27286	S60 and S43	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 12:00

S62	695264	(domain island)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 12:02
S63	6808	S61 and S62	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 12:03
S64	18363	(domain island) near4 (power voltage supply)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 12:03
S65	340	S61 and S64	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 12:03
S66	101	S65 and S47	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 12:04
S67	36	S66 and ic	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 12:04
S68	5	S66 and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 12:06
S69	13	S65 and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/05 12:13
S71	1	("7234124").PN.	US-PGPUB; USPAT	OR	OFF	2011/01/06 15:24
S72	0	(island with layer) and S71	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/06 15:24
S73	1	(island same layer) and S71	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/06 15:24

S74	1	island and layer and S71	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/06 15:27
S76	1	(island same (layer level)) and S71	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/06 15:30

EAST Search History (I nterference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S32	2	"Term Removed"	US-PGPUB; USPAT; UPAD	OR	OFF	2011/01/04 10:08
S70	2	"Term Removed"	US-PGPUB; USPAT; UPAD	OR	OFF	2011/01/05 10:14

1/ 6/ 2011 6:55:55 PM**C:\ Documents and Settings\ nlevin\ My Documents\ EAST\ Workspaces\ 12271534.w sp**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): CHUANG, Chia-Lin	Examiner: LEVIN, Naum B.
Application No.: 12/271,534	Art Unit: 2825
Filed: 14 Nov 2008	Confirmation Number: 4308
Title: A POWER MESH ARRANGEMENT METHOD UTILIZED IN AN INTEGRATED CIRCUIT HAVING MULTIPLE POWER DOMAINS	
Attorney Docket No.: 3722/0536PUS1	

MS AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Dear Sir:

In response to the Office Action of 19 Jan 2011, the following amendments and remarks are provided:

Amendments to the Claims; and
Remarks.

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A power routing arrangement method applied in an integrated circuit having multiple power domains, the arrangement method comprising:

forming a first partial local power mesh according to the position of a first power domain of the integrated circuit by an automatic placement and routing (APR) tool;

forming a second partial local power mesh according to the position of a second power domain of the integrated circuit by the APR tool;

forming a global power mesh that is utilized to provide the power needed by the first and the second power domains by the APR tool;

coupling the first partial local power mesh to the global power mesh and the first power domain by the APR tool; and

coupling the second partial local power mesh to the global power mesh and the second power domain by the APR tool;

wherein the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer; and

wherein the first metal layer and the second metal layer are different layers.

2. (Original) The arrangement method according to claim 1, wherein the first partial local power mesh and the second partial local power mesh are positioned on the same metal layer.

3. (Original) The arrangement method according to claim 2, wherein the global power mesh and the first local power mesh are positioned on different metal layers.

4. (Original) The arrangement method according to claim 3, wherein the global power mesh is positioned above the first local power mesh.

5. (Original) The arrangement method according to claim 2, wherein the first partial local power mesh and the second partial local power mesh are not electrically coupled.

6. (Original) The arrangement method according to claim 1, wherein the global power mesh comprises at least one ground wire, at least one first power wire that provides power to the first power domain, and at least one second power wire that provides power to the second power domain.

7. (Original) The arrangement method according to claim 6, wherein the first partial local power mesh comprises: at least one first local ground wire that couples to the ground wire of the global power mesh; and at least one third power wire that couples to the first power wire and the first power domain.

8. (Original) The arrangement method according to claim 7, wherein the second partial local power mesh comprises: at least one second local ground wire that couples to the ground wire of the global power mesh; and at least one fourth power wire that couples to the second power wire and the second power domain.

9. (Original) The arrangement method according to claim 8, wherein the first local ground wire and the second local ground wire share the same ground wire of the global power mesh.

10. (Original) The arrangement method according to claim 1, wherein the positions of the first partial local power mesh and the second partial local power mesh correspond to the first power domain and the second power domain, respectively.

11. (Original) The arrangement method according to claim 1, wherein the global power mesh is distributed evenly above the first local power mesh and the area of the second local power mesh.

12. (Currently Amended) A power routing structure applied in an integrated circuit having multiple power domains, comprising:

a first partial local power mesh having its position corresponding to the position of a first power domain and coupling to the first power domain;

a second partial local power mesh having its position corresponding to the position of a second power domain and coupling to the second power domain; and

a global power mesh, coupling to the first local power mesh and the second local power mesh, to provide the power needed by the first power domain and the second domain separately;

wherein the first partial local power mesh and the second partial local power mesh are positioned on the same metal layer while the global power mesh and the first local power mesh are positioned on different metal layers;

wherein the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer; and

wherein the first metal layer and the second metal layer are different layers.

13. (Original) The power routing structure according to claim 12, wherein the global power mesh is positioned above the first local power mesh.

14. (Original) The power routing structure according to claim 13, wherein the first local power mesh and the second local power mesh are not electrically coupled.

15. (Original) The power routing structure according to claim 12, wherein the global power mesh comprises: at least one ground wire; at least one first power wire that provides the power needed by the first power domain; and at least one second power wire that provides the power needed by the second power domain.

16. (Original) The power routing structure according to claim 15, wherein the first partial local power mesh comprises: at least one first local ground wire that couples to the ground wire of the global power mesh; and at least one third power wire that couples to the first power wire and the first power domain.

17. (Original) The power routing structure according to claim 16, wherein the second partial local power mesh comprises: at least one second local ground wire that couples to the ground wire of the global power mesh; and at least one fourth power wire that couples to the second power wire and the second power domain.

18. (Original) The power routing structure according to claim 17, wherein the first local ground wire and the second local ground wire share the same ground wire of the global power mesh.

19. (Currently Amended) A power routing arrangement method applied in an integrated circuit having multiple power domains, the arrangement method comprising:

providing a global power mesh, positioned above a first power domain and a second power domain, comprising at least one first power wire that provides the voltage needed by the first power domain, at least one second power wire that provides the voltage needed by the second power domain, and at least one ground wire that provides the ground potential needed by the first power domain and the second power domain by an automatic placement and routing (APR) tool;

coupling the first power wire and the ground wire of the global power mesh to the first power domain by the APR tool; and

coupling the second power wire and the ground wire of the global power mesh to the second power domain by the APR tool;

wherein the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer; and

wherein the first metal layer and the second metal layer are different layers.

20. (Original) The arrangement method according to claim 19, wherein the first power domain and the second power domain share the same ground wire of the global power mesh.

REMARKS

Claims 1-20 remain present in this application.

Claims 1, 12, and 19 have been amended. Favorable consideration of the application, as amended, is respectfully requested.

Entry of Amendments

It is respectfully submitted that the foregoing amendments do not contain new matter, nor do they raise new issues. Support for the foregoing changes to the claims can be found in the originally filed application. For example, claim 1 now recites, “wherein the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer; and wherein the first metal layer and the second metal layer are different layers.” Support for this change can be found in Figs. 4-5 and paragraphs [0025] - [0026]. Claims 1 and 19 now recite, “by an automatic placement and routing (APR) tool.” Support for this change can be found in paragraphs [0033] - [0039]. As such, the Examiner is respectfully requested to enter the same.

Rejection under 35 USC § 101

Claims 1 and 19 stand rejected under 35 USC 101. This rejection is respectfully traversed.

In particular, the Examiner asserts that the claims are “ineligible subject matter” and that the steps in the body of claim must be tied to another statutory class or transform underlying subject matter to a different state or thing. It is noted that independent claims 1 and 19 have been amended to connect each step to an automatic placement and routing (APR) tool. Thus, claims 1 and 19 are directed to statutory subject matter. Reconsideration and withdrawal of the 35 USC 101 rejection are respectfully requested.

Rejection under 35 USC 102

Claims 1, 6-10, 15-18, and 20 stand rejected under 35 USC 102(b) as being anticipated by Ladanza et al., U.S. Patent 7,000,214. This rejection is respectfully traversed.

In order to properly anticipate a claim under 35 U.S. C. § 102, each and every element of the claim in issue must be found, either expressly described or under principles of inherency, in a single prior art reference. Further, “[t]he identical invention must be shown in as complete detail as is contained in the ...claim[s].” See M.P.E.P. 2131 (8th Ed., Aug. 2001). Finally, “[t]he

elements must be arranged as required by the claim.” M.P.E.P. 2131 (8th Ed., Aug. 2001), p. 2100-69.

Independent claim 1 recites (emphasis added):

1. A power routing arrangement method applied in an integrated circuit having multiple power domains, the arrangement method comprising:

forming a first partial local power mesh according to the position of a first power domain of the integrated circuit by an automatic placement and routing (APR) tool;

forming a second partial local power mesh according to the position of a second power domain of the integrated circuit by the APR tool;

forming a global power mesh that is utilized to provide the power needed by the first and the second power domains by the APR tool;

coupling the first partial local power mesh to the global power mesh and the first power domain by the APR tool; and

coupling the second partial local power mesh to the global power mesh and the second power domain by the APR tool;

wherein the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer; and

wherein the first metal layer and the second metal layer are different layers.

It is respectfully submitted that Ladanza fails to teach or suggest at least the above-emphasized features of independent claim 1.

Ladanza is directed to a system and method for designing an integrated circuit having multiple voltage domains. In rejecting claim 1, the Examiner equates the global power mesh 400 of the present application to the chip-level connection declaration 501 of Ladanza (see page 5). However, Ladanza is silent on the structure of the chip-level connection declaration 501. Therefore, Ladanza fails to teach or suggest that “the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer, and wherein the first metal layer and the second metal layer are different layers,” as is recited in independent claim 1.

Independent claims 12 and 19 are allowable over the cited prior art for similar reasons to those set forth above in connection with independent claim 1.

In view of the foregoing amendments and remarks, it is respectfully submitted that the prior art utilized by the Examiner fails to teach or suggest the methods and structure of independent claims 1, 12, and 19, as well as their dependent claims. Reconsideration and withdrawal of the 35 USC 102(b) rejection are respectfully requested.

Rejection under 35 USC 103

Claims 2-5, 11-14, and 19 stand rejected under 35 USC 103 as being unpatentable over Ladanza in view of Chen et al., U.S. Patent 7,234,124. This rejection is respectfully traversed.

The Examiner has the burden under 35 U.S.C. § 103 to establish a prima facie case of obviousness. To establish a prima facie case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *MP.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d, 488, 20 USPQ2d 1438 (Fed. Cir. 1991)). In addition, the Examiner must, as one of the inquiries pertinent to any obviousness inquiry under 35 U.S.C. § 103, recognize and consider not only the similarities but also the critical differences between the claimed invention and the prior art. *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990), *reh'g denied*, 1990 U.S. App. LEXIS 19971 (Fed. Cir. 1990).

(A) Claims 12-18

Independent claim 12 recites (emphasis added):

12. A power routing structure applied in an integrated circuit having multiple power domains, comprising:
 - a first partial local power mesh having its position corresponding to the position of a first power domain and coupling to the first power domain;
 - a second partial local power mesh having its position corresponding to the position of a second power domain and coupling to the second power domain; and
 - a global power mesh, coupling to the first local power mesh and the second local power mesh, to provide the power needed by the first power domain and the second domain separately;
- wherein the first partial local power mesh and the second partial local power mesh are positioned on the same metal layer while the global power mesh and the first local power mesh are positioned on different metal layers;

wherein the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer; and
wherein the first metal layer and the second metal layer are different layers.

It is respectfully submitted that the combination of references cited by the Examiner fails to teach or suggest at least the above-emphasized features of independent claim 12.

As set forth above, Ladanza is silent on the structure of the chip-level connection declaration 501. In the Examiner's rejection of claim 12 (beginning on page 9 of the Office Action), the Examiner equates the global power mesh 400 and the local power mesh 300 of the present application as being comparable to the second power grid 22 and the first power grid 21 of Chen (FIG. 2). Applicant disagrees. In the present application (see paragraph [0020], for example), the global power mesh 400 couples to the external power (such as: by way of the I/O pin of the chip) to conduct the external power into the chip while the local power mesh 300 couples to the global power mesh 400 and the chip circuitry. In other words, the internal circuits of the chip correspond to the power domains 110, 120. Then, the external power will be inputted into the chip circuitry by way of the global power mesh 400 and the local power mesh 300.

In contrast, Chen has no electrical connections between the second power grid 22 and the first power grid 21 and no electrical connections between the VDD_g power network 11 and the VDD_i-VDD_n power networks 15 (see FIGS. 1 and 2). In addition, the VDD_g power network 11 and the VDD_i-VDD_n power networks 15 respectively have their own power sources.

"[E]ach and every element of the claimed invention [must] be taught by the references." *In re Royka*. It is respectfully submitted that Ladanza and Chen fail to teach or suggest that "the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer, and wherein the first metal layer and the second metal layer are different layers" as is recited in independent claim 12 of the present application. Thus, all elements of claim 12 are not taught by the combination of references utilized by the Examiner.

(B) Claims 19-20

Independent claim 19 recites (emphasis added):

19. A power routing arrangement method applied in an integrated circuit having multiple power domains, the arrangement method comprising:

providing a global power mesh, positioned above a first power domain and a second power domain, comprising at least one first power wire that provides the voltage needed by the first power domain, at least one second power wire that provides the voltage needed by the second power domain, and at least one ground wire that provides the ground potential needed by the first power domain and the second power domain by an automatic placement and routing (APR) tool;

coupling the first power wire and the ground wire of the global power mesh to the first power domain by the APR tool; and

coupling the second power wire and the ground wire of the global power mesh to the second power domain by the APR tool;

wherein the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer; and

wherein the first metal layer and the second metal layer are different layers.

It is respectfully submitted that the combination of references utilized by the Examiner fails to teach or suggest at least the above-emphasized features of independent claim 19.

For similar reasons to those discussed above in connection with claim 12, it is respectfully submitted that neither Ladanza nor Chen teach or suggest the method of independent claim 19 of the present invention.

In view of the foregoing amendments and remarks, it is respectfully submitted that the prior art utilized by the Examiner fails to teach or suggest the power routing structure and method of independent claims 12 and 19, respectively, as well as their dependent claims. Reconsideration and withdrawal of the 35 USC 103 rejections are respectfully requested.

Conclusion

Favorable reconsideration and an early Notice of Allowance are earnestly solicited.

Because the additional prior art cited by the Examiner has been included merely to show the state of the prior art and has not been utilized to reject the claims, no further comments concerning these documents are considered necessary at this time.

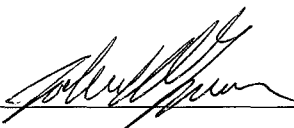
Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Joe McKinney Muncy, Applicants' Attorney, at 703.621.7140 so that such issues may be resolved as expeditiously as possible.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-3828 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; in particular, extension of time fees.

Date: April 19, 2011

Respectfully submitted,

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Joe McKinney Muncy
Attorney/Agent for Applicant(s)
Reg. No. 32334
ROBERT F. GNUSE
Registration #27295

Electronic Acknowledgement Receipt

EFS ID:	9913447
Application Number:	12271534
International Application Number:	
Confirmation Number:	4308
Title of Invention:	POWER MESH ARRANGEMENT METHOD UTILIZED IN AN INTEGRATED CIRCUIT HAVING MULTIPLE POWER DOMAINS
First Named Inventor/Applicant Name:	Chia-Lin Chuang
Customer Number:	60601
Filer:	Joe McKinney Muncy/Ashlyn Canfield
Filer Authorized By:	Joe McKinney Muncy
Attorney Docket Number:	3722/0536PUS1
Receipt Date:	19-APR-2011
Filing Date:	14-NOV-2008
Time Stamp:	17:42:39
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2011-04-19-Amendment.pdf	533921 a4257797dbb404d1d0a321174209863552b69388	yes	11

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	5
	Amendment/Req. Reconsideration-After Non-Final Reject	6	11
Warnings:			
Information:			
Total Files Size (in bytes):		533921	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/271,534		Filing Date 11/14/2008		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)			SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY		
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(j))	minus 20 =	*	X \$	=		X \$	=			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$	=		X \$	=			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.										
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	04/19/2011	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X \$	=		X \$52=	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X \$	=		X \$220=	0
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$	=		X \$	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$	=		X \$	=
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

Legal Instrument Examiner:
/CHRISTINE MOLLISH/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60601 7590 05/02/2011
Muncy, Geissler, Olds & Lowe, PLLC
4000 Legato Road
Suite 310
FAIRFAX, VA 22033

EXAMINER

LEVIN, NAUM B

ART UNIT

PAPER NUMBER

2825

DATE MAILED: 05/02/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/271,534

11/14/2008

Chia-Lin Chuang

3722/0536PUS1

4308

TITLE OF INVENTION: POWER MESH ARRANGEMENT METHOD UTILIZED IN AN INTEGRATED CIRCUIT HAVING MULTIPLE POWER DOMAINS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	08/02/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

60601 7590 05/02/2011
Muncy, Geissler, Olds & Lowe, PLLC
4000 Legato Road
Suite 310
FAIRFAX, VA 22033

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

12/271,534

11/14/2008

Chia-Lin Chuang

3722/0536PUS1

4308

TITLE OF INVENTION: POWER MESH ARRANGEMENT METHOD UTILIZED IN AN INTEGRATED CIRCUIT HAVING MULTIPLE POWER DOMAINS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	08/02/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
LEVIN, NAUM B	2825	716-127000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a **Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

1 _____

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☐ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s); (Please first reapply any previously paid issue fee shown above)

☐ A check is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/271,534	11/14/2008	Chia-Lin Chuang	3722/0536PUS1	4308
60601	7590	05/02/2011	EXAMINER	
Muncy, Geissler, Olds & Lowe, PLLC			LEVIN, NAUM B	
4000 Legato Road			ART UNIT	PAPER NUMBER
Suite 310			2825	
FAIRFAX, VA 22033				

DATE MAILED: 05/02/2011

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 370 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 370 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	12/271,534	CHUANG, CHIA-LIN	
	Examiner	Art Unit	
	NAUM LEVIN	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to Amendment 04/19/2011.
2. ☒ The allowed claim(s) is/are 1-20.
3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☒ All b) ☐ Some* c) ☐ None of the:
 1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
 - * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|--|
| 1. ☐ Notice of References Cited (PTO-892) | 5. ☐ Notice of Informal Patent Application |
| 2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | 6. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____. |
| 3. ☐ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____ | 7. ☐ Examiner's Amendment/Comment |
| 4. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 8. ☒ Examiner's Statement of Reasons for Allowance |
| | 9. ☐ Other _____. |

/NAUM LEVIN/
 Primary Examiner, Art Unit 2825

DETAILED ACTION

1. This office action is in response to application 12/271,534 and Amendment filed on 04/19/2011. Claims 1, 12 and 19 have been amended. Claims 1-20 remain pending in the application.

Allowable Subject Matter

2. Claims 1-20 are allowed over prior art of record.
3. Considered arguments supplied by Applicant in the Amendment on 04/19/2011 as persuasive.
4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NAUM B. LEVIN whose telephone number is (571)272-1898. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/NAUM LEVIN/
Primary Examiner, Art Unit 2825

<i>Index of Claims</i> 	Application/Control No. 12271534	Applicant(s)/Patent Under Reexamination CHUANG, CHIA-LIN
	Examiner NAUM LEVIN	Art Unit 2825

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant				☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE							
Final	Original	01/06/2011	04/29/2011						
	1	✓	=						
	2	✓	=						
	3	✓	=						
	4	✓	=						
	5	✓	=						
	6	✓	=						
	7	✓	=						
	8	✓	=						
	9	✓	=						
	10	✓	=						
	11	✓	=						
	12	✓	=						
	13	✓	=						
	14	✓	=						
	15	✓	=						
	16	✓	=						
	17	✓	=						
	18	✓	=						
	19	✓	=						
	20	✓	=						

Search Notes 	Application/Control No. 12271534	Applicant(s)/Patent Under Reexamination CHUANG, CHIA-LIN
	Examiner NAUM LEVIN	Art Unit 2825

SEARCHED			
Class	Subclass	Date	Examiner
716	120, 126, 127, 133	4/29/2011	N L
326	80	4/29/2011	N L

SEARCH NOTES		
Search Notes	Date	Examiner
EAST (US-PGPUB, USPAT, EPO, JPO, DERWENT, IBM_TDB) - See search history printouts	4/29/2011	N L

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
	USPGPUB, USPAT, UPAD text search - 04/29/11, see interference search printou	4/22/2011	N L

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BIB DATA SHEET

CONFIRMATION NO. 4308

SERIAL NUMBER 12/271,534	FILING or 371(c) DATE 11/14/2008 RULE 1.47	CLASS 716	GROUP ART UNIT 2825	ATTORNEY DOCKET NO. 3722/0536PUS1		
APPLICANTS Chia-Lin Chuang, Hsinchu City, TAIWAN; ** CONTINUING DATA ☐ None ☒ NL ***** ** FOREIGN APPLICATIONS *** ☐ Yes ☒ NL ***** TAIWAN 096143160 11/15/2007 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 11/26/2008						
Foreign Priority claimed ☒ Yes ☐ No 35 USC 119(a-d) conditions met ☒ Yes ☐ No Verified and Acknowledged /NAUM B LEVIN/ ☒ NL Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY TAIWAN	SHEETS DRAWINGS 6	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 3
ADDRESS Muncy, Geissler, Olds & Lowe, PLLC 4000 Legato Road Suite 310 FAIRFAX, VA 22033 UNITED STATES						
TITLE POWER MESH ARRANGEMENT METHOD UTILIZED IN AN INTEGRATED CIRCUIT HAVING MULTIPLE POWER DOMAINS						
FILING FEE RECEIVED 1090	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit			

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S77	32977	sleep\$3 near4 mode	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 09:52
S78	48262	((power voltage) near4 (mesh grid gridiron grating))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 09:57
S79	722	S77 and S78	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 09:57
S80	372	layer and S79	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 09:58
S81	7395	(global local) near4 (mesh grid gridiron grating)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 09:58
S82	36	S80 and S81	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 09:59
S96	66215	(inactive stand-by (low adj power) sleep) near6 mode	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 14:41
S97	57215	((power voltage) near6 (mesh grid gridiron grating))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 14:42
S98	1326	S96 and S97	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 14:42
S99	7395	(global local) near4 (mesh grid gridiron grating)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 14:43

S100	103	S99 and S98	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 14:43
S101	6172	local near4 (mesh grid gridiron grating)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 14:43
S102	88	S98 and S101	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 14:43
S103	5432105	layer	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 14:43
S104	43	S102 and S103	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 14:44
S105	12402	(power ground) with layer with direction	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 14:44
S106	0	S102 and S105	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 14:44
S107	318338	(power ground) with direction	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 14:45
S108	8	S104 and S107	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 14:45
S109	18597	power with ground with via	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 15:02
S110	4	S104 and S109	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 15:02
S111	7443	(inactive stand- by (low adj power) sleep \$4) and S97	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 15:08

S112	430	S111 and S101	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 15:08
S114	11	S112 and S109	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 15:09
S115	156312	plac\$5 same (routing routed wired wiring)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 15:13
S116	4	S114 and S115	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 15:13
S117	277	716/127.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 16:28
S118	968	716/126.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 16:32
S119	337	716/120.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 16:43
S120	448	716/133.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 16:49
S121	843	326/80.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/04/29 16:57

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S83	5855	CHUANG.in. (REALTEK adj SEMICONDUCTOR).as.	US- PGPUB; USPAT; UPAD	OR	ON	2011/04/29 09:37
S84	22292	((power voltage) near4 (mesh grid grideron network)).clm.	US- PGPUB; USPAT; UPAD	OR	ON	2011/04/29 09:39

S85	34	S83 and S84	US-PGPUB; USPAT; UPAD	OR	ON	2011/04/29 09:39
S86	5213	((local global) near4 (power voltage)).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2011/04/29 09:40
S87	1	S85 and S86	US-PGPUB; USPAT; UPAD	OR	ON	2011/04/29 09:40
S88	33834	((local global) near4 (mesh grid grideron network)).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2011/04/29 09:41
S89	1	S85 and S88	US-PGPUB; USPAT; UPAD	OR	ON	2011/04/29 09:41
S90	42787	((local global) with (mesh grid grideron network)).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2011/04/29 09:41
S91	1	S85 and S90	US-PGPUB; USPAT; UPAD	OR	ON	2011/04/29 09:41
S92	5954	((power voltage) near4 (mesh grid gridiron grating)).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2011/04/29 09:53
S93	8	S83 and S92	US-PGPUB; USPAT; UPAD	OR	ON	2011/04/29 09:54
S94	93529	(domain sleep\$3).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2011/04/29 09:56
S95	1	S93 and S94	US-PGPUB; USPAT; UPAD	OR	ON	2011/04/29 09:56

4/ 29/ 2011 5:20:55 PM

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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60601 7590 05/02/2011
Muncy, Geissler, Olds & Lowe, PLLC
4000 Legato Road
Suite 310
FAIRFAX, VA 22033

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/271,534	11/14/2008	Chia-Lin Chuang	3722/0536PUS1	4308

TITLE OF INVENTION: POWER MESH ARRANGEMENT METHOD UTILIZED IN AN INTEGRATED CIRCUIT HAVING MULTIPLE POWER DOMAINS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	08/02/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
LEVIN, NAUM B	2825	716-127000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 **Muncy, Geissler,**
2 **Olds, & Lowe, PLLC**
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

Realtek Semiconductor Corp.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Hsinchu, Taiwan, R.O.C.

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

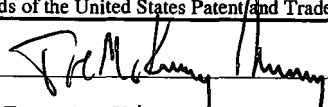
4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☒ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number **503828** (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature 
Typed or printed name **Joe McKinney Muncy**

Date **07/18/2011**
Registration No. **32334**

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Electronic Patent Application Fee Transmittal

Application Number:	12271534			
Filing Date:	14-Nov-2008			
Title of Invention:	POWER MESH ARRANGEMENT METHOD UTILIZED IN AN INTEGRATED CIRCUIT HAVING MULTIPLE POWER DOMAINS			
First Named Inventor/Applicant Name:	Chia-Lin Chuang			
Filer:	Joe McKinney Muncy/Floyd Canfield			
Attorney Docket Number:	3722/0536PUS1			
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1810

Electronic Acknowledgement Receipt

EFS ID:	10544309
Application Number:	12271534
International Application Number:	
Confirmation Number:	4308
Title of Invention:	POWER MESH ARRANGEMENT METHOD UTILIZED IN AN INTEGRATED CIRCUIT HAVING MULTIPLE POWER DOMAINS
First Named Inventor/Applicant Name:	Chia-Lin Chuang
Customer Number:	60601
Filer:	Joe McKinney Muncy/Floyd Canfield
Filer Authorized By:	Joe McKinney Muncy
Attorney Docket Number:	3722/0536PUS1
Receipt Date:	18-JUL-2011
Filing Date:	14-NOV-2008
Time Stamp:	17:48:35
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 1810
RAM confirmation Number	5064
Deposit Account	503828
Authorized User	MUNCY,JOE MCKINNEY

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

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Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

AMD EX1002

AMD v. Realtek

Page 163

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	2011-07-18-IF.pdf	182797 2cef7e7a2e651c8698f2b71d5114553a0221f59d	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	32150 3feee5b35bcbaf0ebcf5a188a8d333a15c1f56	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			214947		
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/271,534	08/23/2011	8006218	3722/0536PUS1	4308

60601 7590 08/03/2011
Muncy, Geissler, Olds & Lowe, PLLC
4000 Legato Road
Suite 310
FAIRFAX, VA 22033

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 370 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Chia-Lin Chuang, Hsinchu City, TAIWAN;

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Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Application Number	12/271,534
				Filing Date	Nov 14, 2008
				First Named Inventor	CHUANG, Chia-Lin
				Art Unit	2825
				Examiner Name	LEVIN, Naum B.
Sheet	1	of	1	Attorney Docket Number	3722/0536PUS1

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
		US-2006/0184808	08-17-2006	CHUA-EOAN et al.	
		US-			
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FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)				

Examiner Signature	Date Considered
-----------------------	--------------------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.¹ Applicant's unique citation designation number (optional).² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04.³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3).⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible.⁶ Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Electronic Acknowledgement Receipt

EFS ID:	11468343
Application Number:	12271534
International Application Number:	
Confirmation Number:	4308
Title of Invention:	POWER MESH ARRANGEMENT METHOD UTILIZED IN AN INTEGRATED CIRCUIT HAVING MULTIPLE POWER DOMAINS
First Named Inventor/Applicant Name:	Chia-Lin Chuang
Customer Number:	60601
Filer:	Joe McKinney Muncy/Ashlyn Canfield
Filer Authorized By:	Joe McKinney Muncy
Attorney Docket Number:	3722/0536PUS1
Receipt Date:	22-NOV-2011
Filing Date:	14-NOV-2008
Time Stamp:	17:10:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2011-11-22-IDS.pdf	145694 9633facd6addb95f2c92fa2687cec90249c80f5d	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Transmittal Letter	1	2
	Information Disclosure Statement (IDS) Form (SB08)	3	3
Warnings:			
Information:			
Total Files Size (in bytes):		145694	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): CHUANG, Chia-Lin	Examiner: LEVIN, Naum B.
Application No.: 12/271,534	Art Unit: 2825
Filed: 14 Nov 2008	Confirmation Number: 4308
Title: A POWER MESH ARRANGEMENT METHOD UTILIZED IN AN INTEGRATED CIRCUIT HAVING MULTIPLE POWER DOMAINS	Patent No.: 8,006,218 Issued: 23 Aug 2011
Attorney Docket No.: 3722/0536PUS1	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

This Information Disclosure Statement is being submitted after the patent has issued and should be placed in the application file in accordance with 37 CFR 1.97(i).

I. LIST OF PATENTS, PUBLICATIONS OR OTHER INFORMATION

The patents, publications, or other information submitted are listed on the PTO/SB/08 attached hereto.

II. COPIES

The document(s) listed on the PTO/SB/08 are not enclosed because they are either U.S. Patents or Published Applications.

III. CONCISE EXPLANATION OF THE RELEVANCE

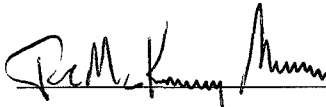
The attached patents, publications, or other information in the English language do not require a statement of relevancy.

It is requested that the information disclosed herein be placed in the application file. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account **50-3828** and please credit any excess fees to such deposit account.

Date: November 22, 2011

Respectfully submitted,

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