UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC.,
Petitioner,

v.

REALTEK SEMICONDUCTOR CORPORATION,
Patent Owner.

Case No. IPR2023-00920
U.S. Patent No. 8,006,218

DECLARATION OF VIVEK SUBRAMANIAN IN SUPPORT OF ADVANCED MICRO DEVICES, INC.'S PETITION FOR INTER PARTES REVIEW OF U.S. PATENT NO. 8,006,218

I, Vivek Subramanian, hereby declare as follows:

I. INTRODUCTION

1. I have prepared this Declaration in connection with Advanced Micro Devices, Inc.'s Petition for *Inter Partes* Review of U.S. Patent No. 8,006,218 ("the '218 Patent") (EX1001), which is to be filed concurrently with this Declaration.

2. In the course of preparing this Declaration, I reviewed the '218 Patent, its prosecution file history, as well as the other documents discussed in this Declaration.

3. I have been retained by Advanced Micro Devices, Inc. ("AMD" or "Petitioner") as an expert in the fields of integrated circuit design, including power arrangement methods and power routing structures for circuits with multiple power domains. I am being compensated at my normal consulting rate for my time. My compensation is not dependent on and in no way affects the substance of my statements in this Declaration. I have no financial interest in AMD, the '218 Patent or the owner of the '218 Patent.

II. QUALIFICATIONS

4. I received a bachelor's degree summa cum laude in electrical engineering from Louisiana State University in 1994. I received M.S. and Ph.D. degrees in electrical engineering, in 1996 and 1998, respectively, from Stanford University. Throughout the course of my education, including my B.S., M.S., and

Ph.D. degrees, I was involved in the design, fabrication, characterization, and modeling of semiconductor devices and integrated circuits, including specifically designing circuits that used multiple power supply voltages. For example, I have designed circuits with embedded nonvolatile memory that required different power supply voltages for the logic and memory subcircuits and used respective power distribution and associated domains to deliver these.

5. After completing my Ph.D., I held multiple appointments simultaneously between 1998 and 2000. I served as a Consulting Assistant Professor in the Electrical Engineering Department of Stanford University. I also served as a Visiting Research Engineer in the Department of Electrical Engineering and Computer Sciences at the University of California, Berkeley, where my research focused on 25nm metal oxide semiconductor field effect transistor (MOSFET) design and fabrication. I worked on technologies for high-performance transistor processes, and I published several papers as a direct outcome of this technology development.

6. In 2000, I became an assistant professor at the University of California, Berkeley in the Department of Electrical Engineering & Computer Sciences. In 2005, I was promoted to the position of tenured Associate Professor, and in 2011, I was promoted to full Professor. In 2018, I became a full Professor of Microtechnology at EPFL in Switzerland, where I lead the Laboratory for Advanced

Fabrication Technologies (LAFT). The lab focuses on the development and application of advanced additive fabrication techniques for realizing precision microelectronic and electromechanical systems. As of 2020, I have completed my move to EPFL and have therefore converted to an adjunct appointment at Berkeley.

7. My research has maintained a large effort on semiconductor devices and circuits, including working on various types of integrated circuit devices using multiple voltage distribution networks, as mentioned above.

8. I co-founded Matrix Semiconductor, Inc. in 1998. Matrix Semiconductors developed three-dimensional integrated circuits for programmable memory chips and cards. The company was eventually acquired by SanDisk. While at Matrix Semiconductor, I was involved with designing multi-voltage power routing structures for chips including multiple power domains.

9. Starting in 2004, I was a founding technical advisor for Kovio. I led the development of Kovio's first commercial RFID tag product, including the design of both the tag and the reader, and including the development of the underlying proprietary transistor technology. I led the development of Kovio's tag circuit technology. In this role, I was actively involved in the development of Kovio's first silicon tag, which included both embedded nonvolatile memory and logic circuitry, and used different power domains for the two circuit subsections. My involvement

with Kovio ended with Kovio's acquisition by Thin Film Electronics, but Kovio continues to focus on this area.

10. I co-founded Locix Inc. in 2014. Locix develops and sells a range of wireless-enabled products, including proprietary Wi-Fi-based RF localization systems and sub-GHz low-power wireless sensor networks. As CTO of Locix, I led the development of the entire Locix RF product portfolio. Locix developed a proprietary WiFi-based integrated circuit that included embedded memory for use in warehouse automation. This chip used multiple power domains for the different circuit blocks to enable operation at optimized low powers. I was actively involved in this development from first conception through finished product. I continued to be involved with Locix on a regular basis until late 2022, when it was sold to a third party.

11. I have authored or co-authored over 200 technical papers in international journals and conferences and have been named an inventor or co-inventor on more than 50 patents, many of which cover aspects of semiconductor device design and fabrication, including the design of circuits that required multiple voltage levels for different circuit subsections.

12. For further details regarding my employment and academic history, please refer to my curriculum vitae, attached hereto as Appendix A.

III. MATERIALS CONSIDERED

13. I have reviewed the '218 Patent and its file history. Additionally, and in addition to any other documents cited or referenced herein, I have reviewed the following materials in preparing this Declaration:

a. U.S. Patent No. 8,006,218 ("'218 Patent" or "'218") – EX1001

b. File History for U.S. Patent No. 8,006,218 – EX1002

c. Jiang, Hailin, et. al., *Benefits and Costs of Power-Gating Technique*, Proceedings of the 2005 International Conference on Computer Design (ICCD '05) ("Jiang") – EX1004

d. Li, Wei, et. al., *LVS Verification across Multiple Power Domains for a Quad-Core Microprocessor*, ACM Transactions on Design Automation of Electronic Systems, Vol. 11, No. 2, April 2006 ("Li") – EX1005

e. U.S. Patent No. 7,948,292 ("Chiu") – EX1006

f. Jiang, Hailin, et. al., *Power/Ground Supply Network Optimization for Power-Gating*, Proceedings of the 2006 International Conference on Computer Design (ICCD '06) ("Jiang2") – EX1007

g. Jiang, Hailin, et. al., *Power-Gating Aware Floorplanning*, Proceedings of the 8th International Symposium on Quality Electronic Design (ISQED '07) ("Jiang3") – EX1008

h. Kim, Suhwan, et. al., *Minimizing Inductive Noise in System-On-a-Chip with Multiple Power Gating Structures*, ESSCIRC 2004 - 29th European Solid-State Circuits Conference (IEEE Cat. No.03EX705), Estoril, Portugal, 2003, pp. 635-638 ("Kim") – EX1009

i. U.S. Patent No. 7,705,486 ("Lee") – EX1010

j. U.S. Patent Application 60/976,181 ("Chiu Provisional") – EX1011

k. Keating, Michael, et. al., *Low Power Methodology Manual*, Springer (2007) ("LPMM") (excerpts) – EX1012

l. Bertolet, A. et. al., *A Pseudo-Hierarchical Methodology for High Performance Microprocessor Design*, ISPD '97: Proceedings of the 1997 international symposium on Physical design, April 1997, pp. 124–129 ("Bertolet") – EX1013

m. Benini, Luca, et.al., *Advanced power management techniques: going beyond intelligent shutdown*, ASP-DAC '03: Proceedings

of the 2003 Asia and South Pacific Design Automation Conference, January 2003 pp. 385–389 ("Benini") – EX1014

n. Ran, Yajun, et. al., *Via-Configurable Routing Architectures and Fast Design Mappability Estimation for Regular Fabrics*, ICCAD-2005. IEEE/ACM International Conference on Computer-Aided Design, 2005 ("Ran") – EX1015

o. U.S. Patent No. 7,671,623 ("Blisson") – EX1016

p. U.S. Patent No. 6,925,627 ("Longway") – EX1018

q. U.S. Patent No. 7,260,805 ("Yan") – EX1019

r. Kimiyoshi Usami et al., Low-power Design Methodology and Applications utilizing Dual Supply Voltages, Proceedings of the ASP-DAC 2000: Asia and South Pacific Design Automation Conference (2000) ("Usami") – EX1020

s. U.S. Patent No. 6,903,389 ("Tai") – EX1024

t. Synopsys Press Release, Synopsys Galaxy Platform Reduces Power Consumption of Industry-Leading Multi-Voltage Designs, Jul. 19, 2006 (available at https://news.synopsys.com/index.php?s=20295&item=122684) – EX1025

u. Synopsys Press Release Index, July 18, 2006 through July 26, 2006 (available at https://news.synopsys.com/index.php?s=20295&l=10&year=2006&o=50) – EX1026

v. Complainant's Proposed Claim Constructions, In the Matter Of Certain Integrated Circuits, Components Thereof, And Products Containing The Same, Investigation No. 337-TA-1350 (May 1, 2023) – EX1029

w. Respondent Advanced Micro Devices, Inc.'s Proposed Claim Constructions, In the Matter Of Certain Integrated Circuits, Components Thereof, And Products Containing The Same, Investigation No. 337-TA-1350 (May 2, 2023) – EX1030

IV. RELEVANT LAW

14. I am not an attorney. For the purposes of this Declaration, I have been informed about certain aspects of the law that are relevant to my opinions. My understanding of the law is summarized below.

15. I have been informed and understand that determining whether a patent claim is valid requires a two-step analysis. First, the claim must be construed. Second, the properly construed claim must be compared to the prior art.

16. I have been informed and understand that claim construction is a matter of law and that the final claim constructions for this proceeding will be determined by the Patent Trial and Appeal Board.

17. I have been informed and understand that in the context of an *Inter Partes* review, claims are construed from the perspective of a person of ordinary skill in the art at the time of the purported invention (which is approximated based on the earliest priority date of the patent). I understand that absent disclaimer or express definition, claim terms are given their plain and ordinary meaning to a person of ordinary skill in the art in view of the specification and file history and knowledge of a person of skill in the art.

18. I have been informed and understand that a patent claim is invalid if it is anticipated by the prior art (*i.e.*, lacks novelty). I understand that anticipation requires the disclosure in a single prior art reference of every limitation of the claim, expressly or inherently, with the limitations arranged as specified in the claim.

19. I have been informed and understand that, although not expressly disclosed, subject matter may be inherently disclosed in a prior art reference where that subject matter is necessarily present in the expressly disclosed subject matter and would be understood to be so by those of ordinary skill in the art. I understand that the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic.

20. I have been informed and understand that a patent claim is obvious and therefore invalid if the claimed subject matter, as a whole, would have been obvious to a person of ordinary skill in the art as of the priority date of the patent based on

one or more prior art references and/or the knowledge of one of ordinary skill in the art. I understand that an obviousness analysis must consider (1) the scope and content of the prior art, (2) the differences between the claims and the prior art, (3) the level of ordinary skill in the pertinent art, and (4) secondary considerations, if any, of non-obviousness (such as unexpected results, industry praise, commercial success, long-felt but unmet need, failure of others, copying by others, and skepticism of experts).

21. I understand that a prior art reference may be combined with other references to disclose each element of the invention under 35 U.S.C. § 103. I understand that a reference may also be combined with the knowledge of a person of ordinary skill in the art, and that this knowledge may be used to combine multiple references. I further understand that a person of ordinary skill in the art is presumed to know the relevant prior art. I understand that the obviousness analysis may take into account the inferences and creative steps that a person of ordinary skill in the art would employ.

22. In determining whether a prior art reference would have been combined with other prior art or other information known to a person having ordinary skill in the art, I understand that the following principles may be considered:

23. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;

24. The substitution of one known element for another is likely to be obvious if it yields predictable results;

25. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;

26. The application of a known technique to a prior art reference that is ready for improvement, to yield predictable results;

27. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;

28. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and

29. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a "reasonable expectation of success" – not "absolute predictability" of success – in achieving the claimed invention by combining prior art references.

30. I am informed that whether a prior art reference invalidates a patent claim as obvious is determined from the perspective of a person of ordinary skill in the art. While there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, a suggestion to combine known elements to achieve the claimed invention may come from the prior art as a whole, or individually, as filtered through the knowledge of one skilled in

the art. In addition, the inferences and creative steps a person of ordinary skill in the art would employ are also relevant to the determination of obviousness.

31. When a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. If a person of ordinary skill in the art can implement a predictable variation and would see the benefit of doing so, that variation is likely to be obvious. In many fields, there may be little discussion of obvious combinations, and in these fields market demand – not scientific literature – may drive design trends. When there is a design need or market pressure and there are a finite number of predictable solutions, a person of ordinary skill in the art has good reason to pursue those known options.

32. It is my understanding that there is no rigid rule that a reference or combination of references must contain a "teaching, suggestion, or motivation" to combine references. But, I understand that the "teaching, suggestion, or motivation" test can be a useful guide in establishing a rationale for combining elements of the prior art. This test poses the question as to whether there is an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and it seeks to counter impermissible hindsight analysis.

V. LEVEL OF ORDINARY SKILL IN THE ART

33. Based on my review of the '218 Patent and my background and experience in the field of computer science, it is my opinion that one of ordinary skill in the art as of November 14, 2008 (the filing date of the application that resulted in the '218 Patent), or November 15, 2007 (the filing date listed for a Taiwanese application to which the '218 Patent claims priority) would be someone with a bachelor of science degree in computer science, electrical engineering, computer engineering, or a related field, and approximately two years of experience in the design and development of power distribution networks related to integrated circuits, or the equivalent, with additional education and/or research substituting for experience and vice versa.

34. I have been informed and understand that claim construction is viewed from the perspective of a person of ordinary skill in the art in question at the time of the invention. I have been asked to use November 15, 2007 as the priority date for the '218 Patent and thus the relevant date for determining a person of ordinary skill in the art. My opinions within this declaration would not change if the '218 Patent's proper priority date was November 14, 2008. Throughout this declaration, when I refer to one of ordinary skill, I am referring to one of ordinary skill in the art as of November 15, 2007 and November 14, 2008 unless otherwise specified.

35. The ’218 Patent generally relates to power routing structures, and power mesh arrangement methods, for integrated circuits having multiple power domains. EX1001, Abstract, 1:47-2:41.

36. Based on my education and experience, I am familiar with the level of knowledge that one of ordinary skill would have possessed during the relevant period of time.

37. In reaching this opinion as to the qualifications of the hypothetical person of ordinary skill in the art, I have considered the types of problems encountered in the art, the prior art solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the educational level of active workers in the field.

38. By the priority date of the ’218 Patent, I was a person who had more than ordinary skill in the art.

VI. OVERVIEW OF THE ’218 PATENT

39. The ’218 Patent stated that it would “provide a power mesh arrangement method for the user to design power meshes having multiple power domains more easily.” EX1001, 1:47-49. The ’218 Patent also described the prior art background in the technology area in which this purported invention occurred. For example, the ’218 Patent acknowledges that it was “common practice[]” for a chip to have “multiple power domains.” *Id*., 1:29-30. The ’218 Patent also

acknowledges that the reasons for having multiple power domains were known, including that at times "different powers need to be supplied to different circuits inside the chip," and that it was known to arrange "circuits in different power domains [that] are coupled to different powers to support … different operations." *Id*., 1:26-33. The '218 Patent also incorrectly asserts that "the well-known automatic placement and routing (APR) tool can only support circuits having single power domain [sic]." *Id*., 1:34-39.

40. To allegedly solve this "problem" identified in the '218 Patent, the patent claimed to have invented "a power routing arrangement method utilized in an integrated circuit having multiple power domains." *Id*., 1:51-53. The power routing arrangement method includes:

- "forming a first local power mesh according to the position of a first power domain;"
- "forming a second local power mesh according to the position of a second power domain;"
- "forming a global power mesh utilized for providing powers needed by the first and the second power domains; coupling the first local power mesh to the global power mesh and the first power domain; and"
- "coupling the second local power mesh to the global power mesh and the second power domain."

EX1001, 1:53-62.

41. Additionally, the '218 Patent proposed a "power routing structure" for "an integrated circuit having multiple power domains," including:

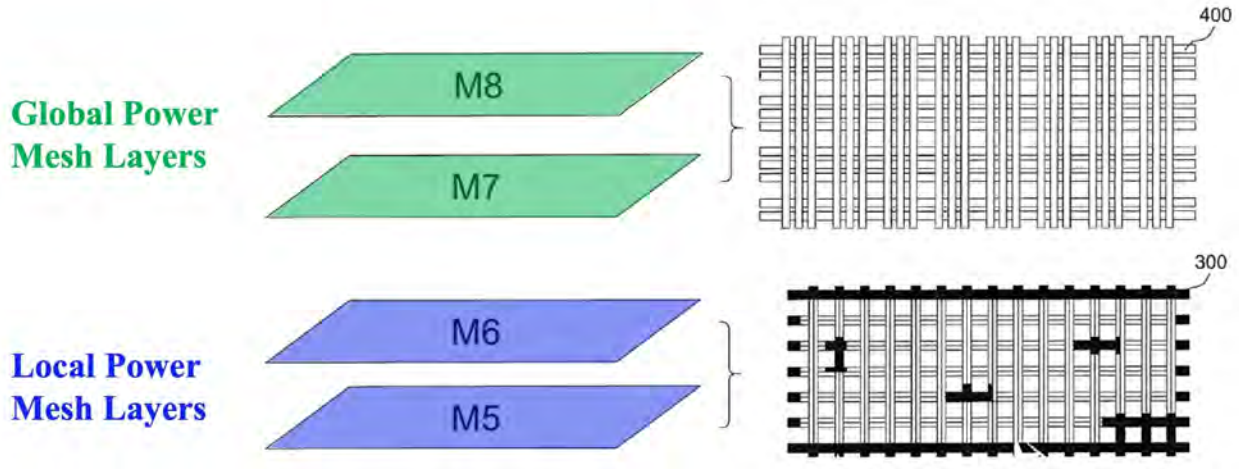
- "a first local power mesh coupling to a first power domain;"
- "a second local power mesh coupling to a second power domain; and"
- "a global power mesh coupling to the first power domain and the second power domain to provide powers needed by the first power domain and the second domain respectively."

Id., 1:63-2:3.

42. Although the '218 Patent does not contain an express definition of "mesh" or "power mesh," it describes power meshes as "web-like structures." *Id*., 3:44-45, 4:21-22. According to the '218 Patent, the meshes generally comprise "a plurality of horizontal power supply wires and a plurality of vertical power supply wires" on two metal layers. *Id*., Figs. 3, 4, 3:49-51, 4:10-16, 4:22-25, 4:40-42. The global power mesh "suppl[ies] voltage to the entire chip." *Id*., 4:31-33. Similarly, the '218's "local power mesh … is evenly distributed on top of the entire chip circuitry" and then partitioned into two "partial local power meshes," each corresponding to a power domain. *Id*., 5:54-63.

43. The '218 Patent also describes the placement of these power meshes in the overall integrated circuit architecture. The '218 Patent asserts that its global-

partial local power mesh arrangement requires at least four metal layers above the chip circuitry, two layers for the global power mesh, and two other layers for the partial local power meshes. *Id*., 4:53-58. Figure 5 from the '218 Patent shows the global power mesh placed on metal layers 7 and 8 and the partial local power meshes on metal layers 5 and 6.



EX1001, Fig. 5 (annotated).

44. The '218 Patent also describes "local" and "partial local" power meshes. Again, the '218 Patent does not provide an express definition of these terms. However, the '218 Patent does show partial local power mesh layers containing two partial local power meshes, a first partial local power mesh 310 (shown with white power wires) and a second partial local power mesh 320 (shown with dark grey power wires) in Figure 3 (annotated below). Although Figure 3 also shows "power mesh[es]" 311, 312, 321, and 322, the '218 Patent itself explains that these are actually power wires 311 and 321 and ground wires 312 and 322, such that a

POSITA would understand these are simply mislabeled in the figure. *See id.*, 3:56-64.

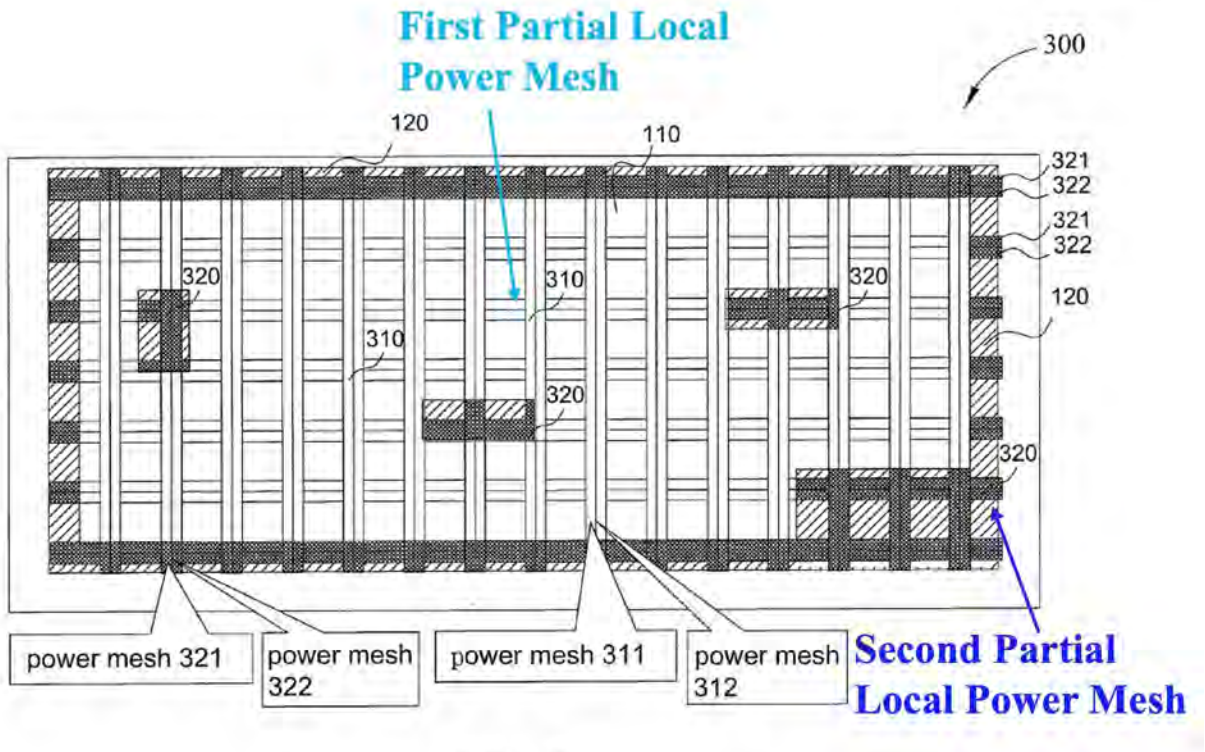


FIG. 3

EX1001, Fig. 3 (annotated).

45. The application that issued as the '218 Patent was filed on November 14, 2008. I see that the '218 Patent faced one rejection. In particular, the examiner rejected the original claims as anticipated by U.S. Patent No. 7,000,214 ("Iadanza") or obvious over the combination of Iadanza and U.S. Patent No. 7,234,124 ("Chen"). EX1002, 104-15. The examiner also rejected the methods in Claims 1 and 19 under 35 U.S.C. § 101 as ineligible subject matter as they "claim[ed] an abstract idea" and "recite[d] purely mental steps. *Id.*, 106-07. Applicant appeared to not dispute these

rejections, instead amending the claims to require the global power mesh to include a plurality of horizontal power supply wires on one metal layer, and a plurality of vertical power supply wires on a different metal layer, and amending the method Claims 1 and 19 to add the use of an APR tool. *Id*., 131-33, 137-38. After this, the examiner allowed the amended claims. *Id*., 144-46.

VII. CLAIM CONSTRUCTION ANALYSIS

46. In my opinion, the claims are unpatentable in view of the grounds discussed below based on the plain and ordinary meaning of the claim terms in view of the ’218 Patent specification. Where it is relevant, I have identified passages of the ’218 Patent that inform the plain and ordinary meaning of the claim limitations. I have reviewed AMD’s proposed claim constructions (EX1030) as well as Realtek’s (EX1029) submitted in the ITC. I understand that Realtek construes “first local power mesh” and “second local power mesh” to refer to “first partial local power mesh” and “second partial local power mesh,” respectively. EX1029, 1. I also understand Realtek to construe “local power mesh” to refer to “first partial local power mesh” or “second partial local power mesh” depending on the context in which the term appears in the claim. *Id.*, 2. I have been asked to assume these constructions are correct and have therefore used these constructions in my analysis. I also understand that AMD contends that “power mesh” means “[t]wo sets of parallel conductive metal wires that form a net or web-like structure” and that

"global power mesh" means "[a] power mesh distributed across the full area of the chip's circuitry for conducting external power into the chip." EX1030, 2. In my opinion, AMD's proposed constructions align with the ordinary meaning of these terms and thus my opinions would not change if those constructions were adopted. I also understand that AMD contends that "local power mesh" and "partial local power mesh" are indefinite. *Id.* While I offer no opinion on the indefiniteness of these terms in this proceeding, because the prior art discloses the same structures as in the preferred embodiment of the '218 Patent, in my opinion the prior art discloses these features as I explain below without regard to how these terms are construed or whether they have a definite meaning.

VIII. SUMMARY OF PRIOR ART

47. By November 2007, the use of power-gated chips was well known. An integrated circuit and the subcircuit blocks within it consume power. It makes sense, therefore, to divide an integrated circuit into power domains with a power-gating design for each power domain, such that when a power domain is unneeded, even for a very short amount of time, it can be powered down or switched off while the rest of the integrated circuit remains running. Many of the prior art references discuss this concept. Thus, the concept of using a partial local power mesh, which is power-gated, to supply a power domain was known.

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48. Similarly, the concept of using a global power mesh to supply partial local power meshes was also well known as demonstrated by the prior art discussed below. Jiang, Jiang2, Jiang3, Li, and Chiu disclose this concept in great detail. That is no surprise because using a top level global power mesh to supply partial local power meshes was a known design arrangement that was particularly appropriate for power-gated integrated circuits. Power-gated integrated circuits achieve their energy efficiency by powering down (or shutting off) unnecessary portions of the chip for periods of time while at least some portion of the rest of the chip remains powered up and functioning. The easiest way to power down a portion of the chip (a particular power domain) is to turn off its power supply using a sleep transistor, which can be done on either the positive or negative voltage supply side. But that also requires that its power supply (positive or negative) downstream of the sleep transistor be isolated from other power domains to shut off only the idle portion of the chip, thus necessitating local power grids to supply power domains.

49. As both Li and Chiu show, it was also known to use independent power supplies on the same chip to supply separate power domains separately. There are many reasons for this as explained below, but in summary, different circuits require different power supplies. In general, using the lowest voltage possible to power integrated circuits reduces overall power consumption of the integrated circuit. And power consumption before and during 2007 was a very significant consideration in

the design of integrated circuits and remains so today. Not all circuits, however, perform the same at the same voltage, such that some circuits will require a higher voltage to perform adequately than others. Thus, there was an understood need to have independent voltage supplies to the same integrated circuit where these and other considerations dictated independent voltage supplies. All these considerations were known and understood in November 2007 as demonstrated by the prior art discussed below.

50. Finally, using automated placement and routing ("APR") software to design power routing structures was very well known as even the '218 Patent concedes. The '218 Patent asserts that APR software only supports circuits having a single power domain. EX1001, 1:34-39. But as explained below, a POSITA understood how to use APR tools to design power routing structures with multiple power domains. Li provides such an example as do many other references as discussed below.

51. As a result, a POSITA would have been aware in November 2007 of power-gated chips having multiple power domains, global power meshes, partial local power meshes, the routing structures used in such meshes, separate power supplies on the same chip, and the use of automated placement and routing software to perform the placement and routing for chips having multiple power domains. I

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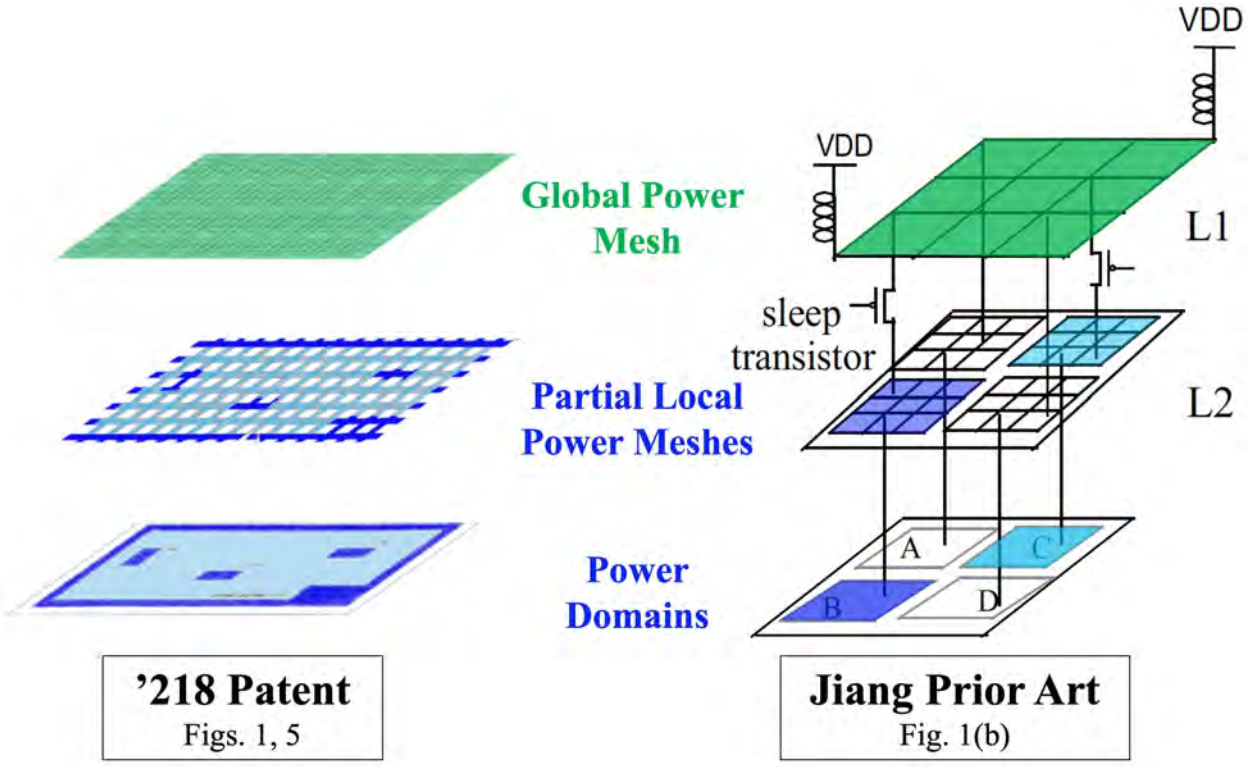
have been asked to assume that each of the references I discuss below and refer to as "prior art" are in fact prior art to the '218 Patent.

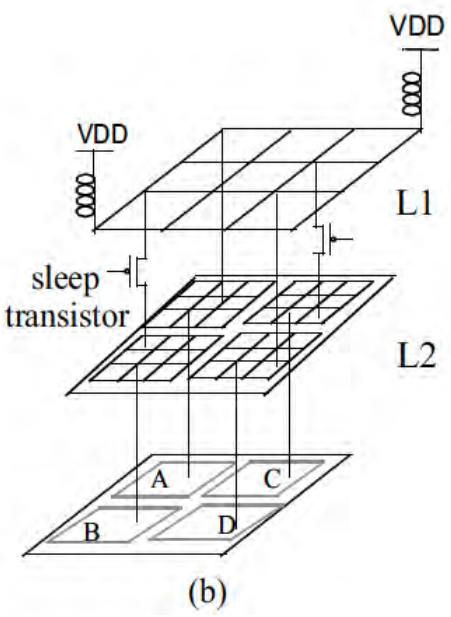
A. Summary of Jiang

52. Jiang provides an example of a power-gated multiple power domain integrated circuit design with global and partial local power meshes that provide precisely what the '218 Patent claims to have invented, as shown below:



Compare EX1001 at Figs. 1, 5 (excerpted, annotated, rotated) *with* EX1004 at Fig. 1(b) (annotated). The series of Jiang articles explore how to quantify and solve problems associated with power routing structures on multiple power domain integrated circuits with power-gating arrangements. Jiang is entitled, "Benefits and Costs of Power-Gating Technique." EX1004, 1. Jiang described mathematically

modeling the power distribution system in such chips. *Id.* Describing the basic structure of such chips, Jiang taught that "Power-gating is a technique for saving leakage power by shutting off the idle blocks." *Id.* Jiang's basic design is shown in Jiang's Figure 1(b) below.



EX1004, Fig. 1(b). Jiang referred to power domains as "macros" and included four such power domains in the Figure 1(b) example along with a "local power mesh[]" for each macro. *Id.*, 1-2, Fig. 1(b). Jiang also describes a "global mesh" above the "local power meshes" that is connected to external power sources, in this case "Vdd." *Id.* Jiang further discloses sleep transistors between some "local power meshes" and the "global mesh" as shown in Figure 1(b), allowing the "local power meshes" and their underlying power domains to be switched off. *Id.*

B. Summary of Jiang2 and Jiang3

53. Jiang2 and Jiang3 follow Jiang and continue the multiple power domain, power-gated integrated circuit discussion. Each of Jiang2 and Jiang3 list two of the three authors in Jiang. *Compare* EX1004, 1 *with* EX1007, 1; EX1008, 1. Jiang2 is entitled, "Power/Ground Supply Network Optimization for Power-Gating." EX1007, 1. It relates itself to Jiang by explaining that Jiang "discuss[es] and quantif[ies] the negative effects of power gating," while Jiang2 "present[s] a general algorithm to optimize the power/ground supply network for power-gating." *Id*. Jiang3 similarly characterized Jiang. EX1008, 1. Jiang3 is entitled, "Power-Gating Aware Floorplanning" and "present[s] an efficient measure which captures power-gating effects in floorplan stage." *Id*.

54. Jiang2 and Jiang3 also describe the same basic concept of a power-gated chip as Jiang. EX1007, 1; EX1008, 1. But these references also expand upon Jiang's teachings for power-gated chip design and power distribution systems in such chips. For example, Jiang2 and Jiang3 teach that a power-gated "chip is divided into several power domains" and that "local power meshes are constructed for each" power domain as described in Jiang. EX1007, 1; EX1008, 1. Jiang2 and Jiang3, however, further explain that "[e]ach domain is independently controlled by a sleep-transistor" and that these "sleep transistors are turned off to reduce the dynamic

power and leakage power in a standby mode, and turned on in an active mode for normal operation." EX1007, 1; *see also* EX1008, 1 (similar).

C. Summary of Li

55. Li is a technical publication describing Broadcom Corporation's BCM1280 chip, shown below.

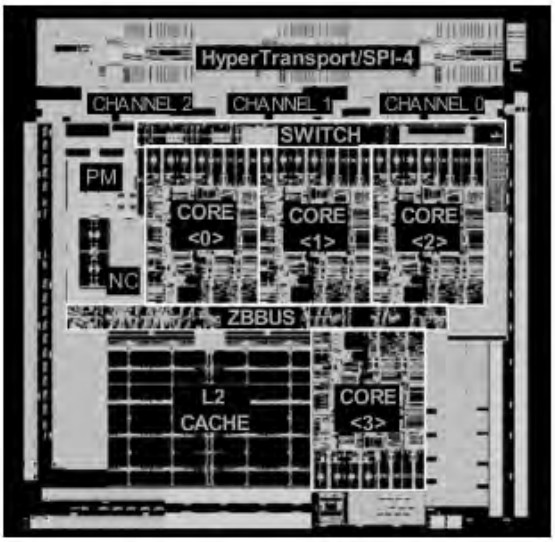


Fig. 1. Chip detailed floorplan.

EX1004, Fig. 1, 491-92. Li explained that the BCM1280 had multiple power domains and a hierarchical power routing system including a global power grid supplying power across the "top level" of the chip and multiple local power grids providing power to their respective power domains. *Id*., 491-93.

56. In particular, I will note that Li explained the very basic idea that power routing structures were "designed to provide required voltages and currents to the transistors that perform the logic functions of a chip." *Id*., 492. Li explained that the BCM1280 is a "system on a chip (SOC)" that includes "four 64-bit MIPS™ CPU

cores" along with "dedicated networking hardware." *Id.*, 491. These CPU cores and the dedicated networking hardware have different power requirements resulting in two independent voltage supplies to the chip. Li explains that the "chip is divided into two logic voltage regions (1.1V)." *Id.* The power routing structure in Li's BCM1280 chip supplied the two different voltages (VDD_chip) and (VDD_switch) as well as Ground (GND). *Id.*, 493. Li explained that this power routing structure was built across at least six metal layers. This included a "top level" "power grid structure" with vertical power lines on one metal layer (metal-6) and horizontal power lines on another metal layer (metal-7). *Id.* Li's layout is shown in Figure 3, below.

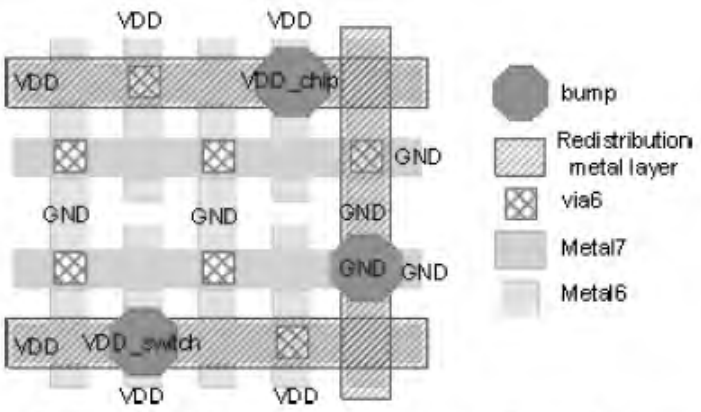


Fig. 3. Power and ground are distributed from the bumps onto the chip-level power grid through a redistribution metal layer.

Id., 494, Fig. 3. Li's top-level power grid "distribut[es] power and ground across the chip." *Id.*, 493.

57. I further note that Li teaches that its power distribution system included multiple local grids: "The power and ground lines in the local sections are grided on

Metal-2 through Metal-5, on which the local power grids are formed at the block level." *Id*.

58. Li also explains how its CPU cores are individually power-gated (on the ground side) and why individual CPU power gating is beneficial. Li states, "The CPU core is migrated from a previous twin-well process design, in which the power grid (VDD/GND) was designed and verified as global nets across the entire chip. In this quad-core microprocessor, four CPU cores are identical and each sits in a separate triple-well region. Each single core, isolated from the others by a triple-well, forms a separate processor region. Therefore, under the full-chip context, each core is now built in a unique voltage region." *Id.*, 491. Li explains that "[a] power switch structure is designed surrounding each core. … The power switch enables a single core to be turned on or off individually. This independently configurable feature is very desirable for a variety of applications that may have different power consumption requirements, as power dissipation limits have emerged as a major constraint in the design and application of microprocessors …." *Id.*, 494-95.

59. Li also describes an "in-house automated procedure" for completing the power routing structure in the BCM1280 by "connecting local logic to the top-level power grid, to implement a complete full-chip power distribution network." *Id*., 493. The design of the interconnections between the power domain and local grid and

local grid and global grid of this power routing structure is a placement and routing function, making Li's "in-house automated procedure" an APR tool.

D. Summary of Chiu

60. Chiu is U.S. Patent No. 7,948,292 B1 and is entitled, "Method and Apparatus for Buffering Signals in Voltage Domains." EX7, 1. Chiu discloses an integrated circuit with first and second voltage domains. *Id*., Abstract. Chiu explains that these voltage domains receive separate voltage supplies but share a common ground supply.

61. Chiu teaches that "[g]enerally, each of the voltage supply grids (positive and negative) in an integrated circuit are associated with the upper-most metal layers, are arranged in a grid (as further discussed below) and are coupled to cells and/or power-ground rails (associated with the middle or lower layers of the integrated circuit) using a piece of metal called a via stack." EX1006, 2:55-61. Thus, Chiu discloses a global grid at the chip top level as well as local "power-ground rails" in the middle or lower metal layers. Chiu also explains that this is "generally" the case for integrated circuits meaning that this was a common design practice in the industry.

62. Chiu also describes a specific power "grid" implementation comprising two "positive voltage supply grid[s]" (VDD1 and VDD2) and one common ground,

"negative voltage supply grid" (VSS). EX1006, 2:31-43, 2:50-61. Chiu's top-level grid is shown in Figure 7 below.

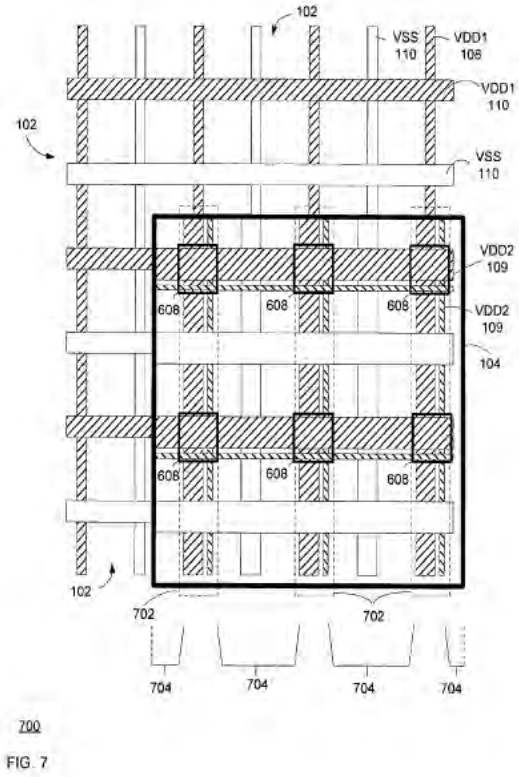


FIG. 7

Id., Fig. 7. Chiu teaches that the voltage supply VDD1 "powers the standard cells in the first and third voltage domains," while VDD2 powers the "cells in the second voltage domain." *Id.*, 2:31-43. VDD2 in Chiu's design is a "selectably on voltage supply grid," which is "capable of being powered up and powered down," which means that "the standard cells in the second voltage domain 104 are also capable of being selectively powered up and powered down." *Id.*, 2:35-43. Chiu further explains that "[i]mplicit in the above discussion is the need and use of a negative voltage supply grid," such as "supply grid VSS 110" shown in Chiu's Figure 1. *Id.*,

2:50-55. A POSITA would understand the negative voltage supply grid "VSS" to be the ground supply. *See e.g.*, EX1012, 85 (referring to the "common ground" supply as "VSS"); EX1018, 8:22-26, 9:17-23 (similar). With reference to Figure 8, Chiu also describes "power ground rails" and "voltage rails" in "intermediate metal layers of the integrated circuit." EX1006, 9:6-26. Chis explains that "[a]lthough the power-ground rails are illustrated as spanning the entire portion 800 of the second voltage domain 104, it is recognized that the power-ground rails are only necessary to the extent cells requiring this voltage for operation are placed in these regions." *Id.*, 9:14-18. Thus, Chiu teaches that the power-ground rails may be coextensive with the underlying power domain or may only extend across the power domain as far as underlying circuitry requires that particular power supply.

63. Thus, similar to Li, Chiu teaches a global power grid with two independent supply voltages as well as local power rails, including the use of power gating. Chiu also discloses that the power gating is applied to one of the voltage supplies and thus the local power rail(s) and power domain associated with that voltage supply.

E. <u>Summary of Bertolet</u>

64. Bertolet is a paper entitled, "A Pseudo-Hierarchical Methodology for High Performance Microprocessor Design" and was authored by A. Bertolet, among others. It describes a "'pseudo-hierarchical' design approach … to manage the

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floorplan, placement, and routing optimization" of a power routing structure for an integrated circuit. EX1013, 124. Bertolet disclosed a way to "algorithmically generate[] power distribution on five layers of metal" of an integrated circuit. *Id*., 125. Bertolet "algorithmically generated [the power distribution network] using a custom SKILL program." *Id*., 126. Bertolet explained that this tool "provide[d] the capability to define multiple power terrains by area and level of metal." *Id*. Accordingly, with this tool, two different areas of the chip could have "different power grids on metal levels three though five" but share the same global "common power grid on metal levels one and two." *Id*.

65. Bertolet thus acknowledges again the generic global grid with underlying local grids concept and explains that it was known to algorithmically generate such a design.

F. Summary of Low Power Methodology Manual (LPMM)

66. As explained above, technology constraints in the early 2000s and earlier were driving integrated circuits to reduce power consumption, which led to the use of power gating power domains to avoid providing power to idle blocks. LPMM resulted from a decade-long collaborative research effort by ARM, Inc. and Synopsys, Inc. on integrated circuits and low power system architecture necessitated by the drive to reduce power consumption, including projects exploring multi-voltage circuits and power-gated routing structures. EX1012, xv-xvi.

67. LPMM explains how the use of APR tools to design power routing structures for multiple independent supply voltages, multiple power domains, and power gating was known and indeed recommended. EX1012, 173-78.

68. LPMM taught that most electronic design automation (EDA) "tools provide some level of automated power network synthesis (PNS) capability for the distribution of power across a design." *Id.*, 177. LPMM "recommend[ed] highly that the implementation of a multi-voltage design utilize this type of PNS capability wherever possible." *Id*. Indeed, LPMM warned that "[t]he number of concurrently changeable variables in a multi-voltage system is such that attempting to construct a power plan manually may result in a suboptimal result both in terms of routing resources consumed and the voltage drop on the rails." *Id*.

69. Thus, LPMM taught the availability of APR tools for power routing in multiple independent voltage supply designs as well as the reasons such APR tools should be used.

G. Analogous Art

70. In my opinion, a POSITA would understand that each of the prior art references discussed above are analogous art to the claimed invention in the '218 Patent. As I explained in detail above, each of the prior art references teaches the use of power routing structures in integrated circuits and how to implement such structures. Generally, therefore, each of the references are directed to

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implementation of power routing structures in integrated circuits. Also, each of the references describes the use of multiple power domains in an integrated circuit and thus the power routing structures for such multiple power domain chips. Thus, in my opinion, each of these references are in the same field of endeavor as the '218 Patent, because they are directed to power routing structures in integrated circuits, including those with multiple power domains. *Compare* EX1001, 1:8-11, *with* EX1004, 1-2; EX1005, 490-94; EX1006, Abstract, 1:42-2:61; EX1007, 1-2; EX1008, 1-2, 4-5; EX1012, 177-78, 271; EX1013, 124-26. Additionally, in my opinion, the cited prior art is reasonably pertinent to the problem addressed in the '218 Patent, which I explained above is providing a power routing structure including a global power mesh and partial local power meshes that in the case of the method can be implemented with an automatic placement and routing tool. *Id*.

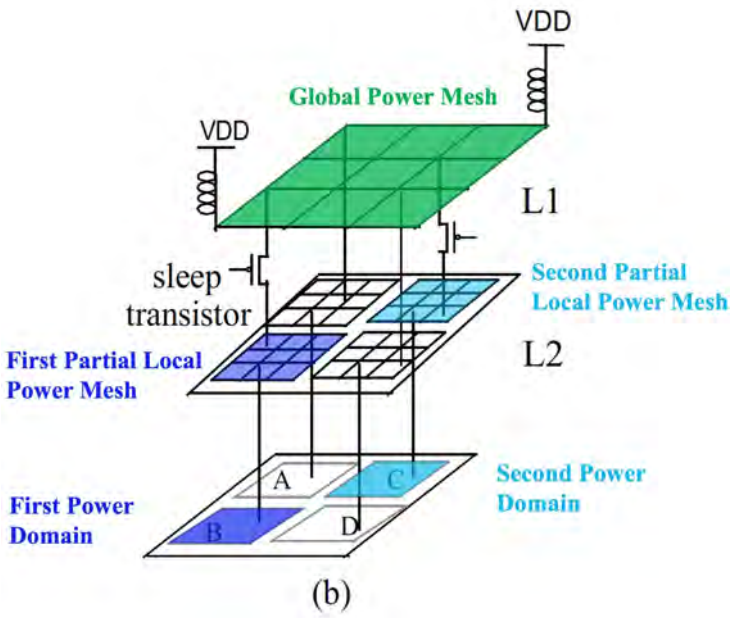
IX. GROUNDS 1-2 – CLAIMS 12-18 ARE OBVIOUS OVER JIANG IN VIEW OF JIANG2 AND JIANG3, OPTIONALLY IN FURTHER VIEW OF LI OR CHIU

71. In my opinion, claims 12-18 would have been obvious over each of the following grounds: (1) Jiang in view of Jiang2 and Jiang3; (2) Jiang in view of Jiang2, Jiang3, and in further view of Li or Chiu.

A. Claim 12[preamble]: "A power routing structure applied in an integrated circuit having multiple power domains, comprising:"

72. While I have been informed that claim preambles are not always limiting, to the extent it is limiting, Jiang discloses the preamble. Thus, I do not need

to determine whether the preamble in this case is limiting. Jiang discloses a power routing structure for a power-gated integrated circuit with multiple macros, with partial local power meshes for each macro and a global power mesh above the partial local power meshes. EX1004, 1 ("In the power-gated chip, we have local power meshes for all macros, and sleep transistors are used to connect the local mesh to the global mesh."); *see also id.* (discussing "VLSI circuits," which are integrated circuits). This power routing structure is shown in Figure 1b, below.



Id., Fig. 1(b) (annotated). It is my opinion that a POSITA would understand that each of the "macros" in Jiang's power-gated integrated circuit is a power domain. *See, e.g.*, EX1004, 2 ("When a macro is active, the sleep transistor is turned on. Its size must be large enough to guarantee that the current drawn by the macro does not cause excessive voltage drop."). For example, Jiang 2 explains "[i]n a power-gating

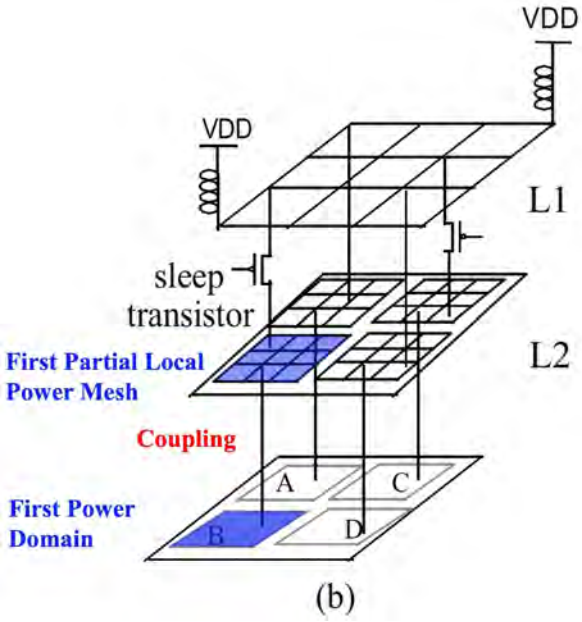
system, a circuit is divided into several power domains." EX1007, 1. Similarly, Jiang3 describes dividing a chip into multiple power domains and then refers to those power domains as "macros." *E.g.*, EX1008, 1 ("[T]he chip is divided into several domains and local power meshes are constructed for each of them."), 5 ("We used circuits from the MCNC and ISCAS benchmarks as basic macros and mapped them to the MCNC floorplan benchmarks. … We selected the gating status of macros in several ways to illustrate various situations.").

73. In my opinion, a POSITA working in the area of power routing for power-gated chips would look to all three of Jiang, Jiang2, and Jiang3 and would readily combine the teachings of all three references. Jiang, Jiang2, and Jiang3 address aspects of the design of power-gated integrated circuits with multiple power domains as discussed above in Section VIII.A-B. As I explained above, Jiang addresses the benefits and costs of power-gating in integrated circuits. Jiang2 provides an algorithm for optimization of the power/ground supply network for power-gated integrated circuits. Jiang3 describes how to quantify the effects of power-gating and mitigate those effects at the floorplanning stage of power routing structure design. Because all of these references focus on how to design power routing structures for power-gated chips, a POSITA working in this area would be aware of all three and would look to all three for information on how to design power routing structures for power-gated chips. Jiang2 and Jiang3 actually reference Jiang

expressly, further facilitating a POSITA locating all three references. Additionally, Hailin Jiang is the first named author on all three articles again making cross-referencing and finding all three simple for the POSITA researching in this space. Further, because Jiang2 and Jiang3 specifically reference Jiang, a POSITA working in the area of power routing for power-gated chips would readily look to the teachings of Jiang2 and Jiang3 to understand the terminology in Jiang.

B. Claim 12[a]: "a first partial local power mesh having its position corresponding to the position of a first power domain and coupling to the first power domain;"

74. Jiang discloses this limitation. Jiang discloses four macros (power domains) A, B, C, and D, and each macro has its own corresponding partial local power mesh. EX1004, 1 ("In the power-gated chip, we have local power meshes for all macros …."). I will use macro B as an example of a first power domain, although any of the power domains A, B, C, and D could be the first power domain. A POSITA would understand that Jiang discloses that macro B (the first power domain, which is annotated below) is coupled to and is directly below and coincident with its corresponding partial local power mesh (the first partial local power mesh), as shown in Jiang's Figure 1(b), below.

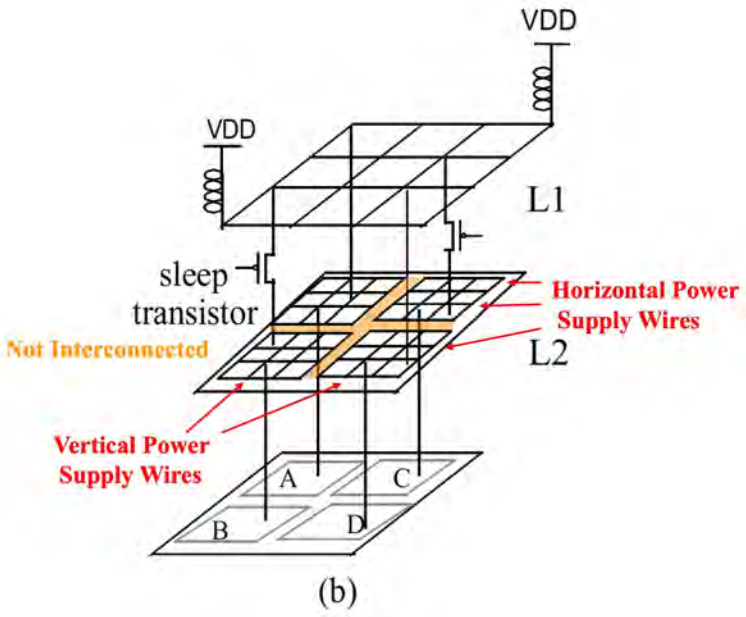


EX1004, Fig. 1(b) (annotated). For macro B, which is power-gated as shown in Figure 1(b), Jiang teaches that the "sleep transistors are used to connect the local mesh to the global mesh" and, accordingly "connect the gated blocks to the power supply." *Id.*, 1.

75. It is my opinion that a POSITA would understand the "local power meshes" disclosed in Jiang to meet the claimed "partial local power mesh." I note that the '218 Patent describes the "partial local power meshes" as "web-like structures," which are "not interconnected" with each other "which means that the partial local power meshes 310, 320 are mutually insulated." EX1001, 3:44-49. The partial local power meshes also "comprise[] a plurality of horizontal power supply wires and a plurality of vertical power supply wires" that are "only used to supply the powers needed" by their particular power domain. *Id.*, 3:49-54. While none of

these are an express definition of a "partial local power mesh" in the '218 Patent and thus not necessarily required of a "partial local power mesh," Jiang's "local power meshes" meet all these criteria. Thus, without regard to how "partial local power mesh" is construed or whether it is definite, Jiang's "local power meshes" meet the "partial local power mesh" criteria provided in the '218 Patent and thus satisfy the limitation.

76. As the figure below shows, the partial local power meshes in Jiang are "web-like structures," which are "not interconnected" with each other—*i.e.*, they are "mutually insulated" from each other. They also comprise a plurality of horizontal and vertical power supply wires that are only used to supply the powers need by their respective underlying power domains as shown below in Figure 1(b).



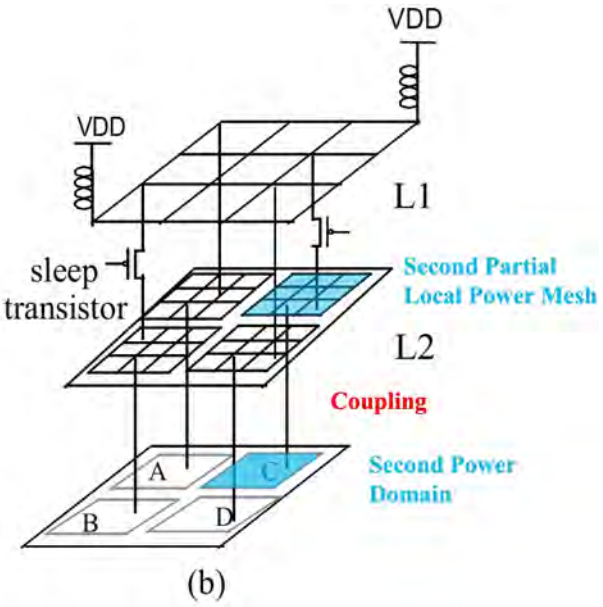
EX1004, Fig. 1(b) (annotated), 1-2; *see also* EX1008, 1. Figure 10 of Jiang (reproduced below) also shows the vertical and horizontal wires of the power meshes of Jiang and makes clear that such wires are on separate metal layers.

Figure 10. Power mesh granularity

EX1004, Fig. 10. Jiang states, "Fig. 10 shows power meshes of various granularity," *id.*, 7, thus again showing that the "local power mesh" in Figure 1(b) includes vertical and horizontal wires on different metal layers. Thus, however "partial local power mesh" might be defined, Jiang discloses "partial local power meshes."

C. Claim 12[b]: "a second partial local power mesh having its position corresponding to the position of a second power domain and coupling to the second power domain; and"

77. Jiang discloses this limitation for the same reasons I explained above regarding limitation 12[a]. EX1004, 1; *see* Section IX.B, *supra*. In this case I choose macro C as a second power domain, but any power domain other than the power domain selected for the first power domain could be the second power domain. Jiang discloses that macro C (the example second power domain) is coupled to and is directly below and coincident with its corresponding partial local power mesh (the second partial local power mesh), as shown in Jiang's Figure 1(b), below.



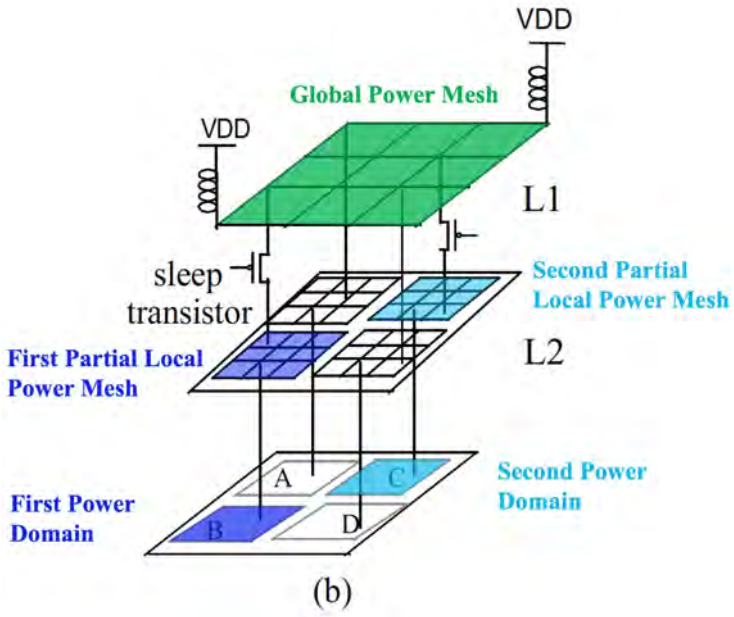
EX1004, Fig. 1(b) (annotated), 1-2; *see also* EX1008, 1. The example second partial local power mesh is a "partial local power mesh" for all the reasons I explained above regarding the first partial local power mesh.

D. Claim 12[c]: "a global power mesh, coupling to the first local power mesh and the second local power mesh, to provide the power needed by the first power domain and the second domain separately;"

78. Jiang discloses this limitation. As an initial matter, I see that some claims recite "***the*** first local power mesh" or "***the*** second local power mesh," even though the claims do not mention "***a*** first local power mesh" or "***a*** second local power mesh." *See, e.g.*, EX1001, 7:55-8:17 (cls. 12-14). As I explained above regarding claim construction, I have been asked to assume for the purposes of this declaration only that the first and second "local power mesh[es]" refer to the first

and second "partial local power mesh[es]" recited in limitations 12[a]-[b], respectively. I have assumed that for purposes of my analysis.

79. Jiang discloses that its chip contains a "global mesh" that is coupled to the first and second partial local power meshes via the sleep transistors. EX1004, 1 ("[S]leep transistors are used to connect the local mesh to the global mesh."). This is shown in Jiang's Figure 1(b) below.



EX1001, Fig. 1(b) (annotated).

80. Jiang teaches that the global power mesh shown in L1 in Figure 1(b) provides the power (Vdd) needed by macros B and C (the first and second power domains), as shown in Figure 1(b) above. Figure 1(b) shows the connections for providing power to the underlying macros, or power domains. Jiang also expressly states that "[i]n the standard chip, all logic circuits are connected to Vdd through a

hierarchical power mesh. … In the power-gated chip, we have local power meshes for all macros, and sleep transistors are used to connect the local mesh to the global mesh." EX1004, 1. As a result, a POSITA would understand from Jiang's disclosure that in the example in Figure 1(b), the global power mesh power Vdd connects to the gated macros (power domains) through the sleep transistors and partial local power meshes as depicted in Figure 1(b) above. *Id*. Confirming this understanding, Jiang further discloses measuring the voltage Vdd that is provided to the power domains, which of course, shows that Vdd is supplied to the underlying power domains. *See id*., 6.

81. A POSITA would understand that the point of adding sleep transistors to individual power meshes and their underlying power domains is to be able to turn off their power supply when the underlying macro is not needed. This saves power consumption by the integrated circuit. A POSITA would understand that Jiang's insertion of sleep transistors between the global power mesh and the first and second partial local power meshes enables the global power mesh to power each domain "separately" by selectively turning off each domain's sleep transistor when desired. *See* EX1004, Abstract ("Power-gating is a technique for saving leakage power by shutting off the idle blocks."); *see also id*., 1 (same); 2 (discussing "sleep transistors" being "turned on and off"). Turning off the power to the partial local power mesh will necessarily turn off the power to the macro underlying that partial local power

mesh as well, thus avoiding the current drain of keeping an idle macro powered up. In this way, Jiang teaches a global power mesh that is able to power the first and second power domains separately.

82. In my opinion, the use of sleep transistors in the connection between the global power mesh and the partial local power meshes in Jiang I have just described satisfies limitation 12[c]. Jiang discloses an individual sleep transistor to each partial local power mesh, such that each power-gated partial local power mesh is independently switchable between on or off. Jiang does not disclose any linkage between the individual sleep transistors, such that they would all be required to be in the same state at the same time.

83. Nevertheless, I have been asked to consider whether it would have been obvious for Jiang's sleep transistors to be independently operable if this were not already evident to a POSITA from Jiang's disclosure, which as I explained above is the case. In my opinion, independent operability of Jiang's sleep transistors would have been obvious as well as being understood from Jiang's disclosure. First, a POSITA would have known that a "multiple power domain strategy in which each power domain has an ***independent power gating structure*** is an effective means for reducing leakage power consumption in a system-on-a-chip." EX1009, 1 (abstract) (emphasis added); *see also* EX1010, 1:37-43 ("Since power consumption increases with higher number of gates, technology for reducing power consumption is desired.

To address such issues, multi-power domain technology is used for separating power domains among different functional blocks with control of turning on/off the power supplied to the multiple power domains depending on operating modes of the functional blocks.").

84. Second, Jiang2 teaches that "[i]n a power-gating system, a circuit is divided into several power domains" where "[e]ach domain is independently controlled by a sleep-transistor." EX1007, 1. Thus, Jiang2, using the same example as Jiang, states unequivocally that the power domains are "independently controlled." Jiang2 confirms my earlier opinion that a POSITA would understand this from Jiang's disclosure. Similarly, Jiang3 teaches that it is "assume[d] that when power-gating is applied, the gated-blocks are individually power supplied." EX1008, 4. Jiang3 thus also confirms my earlier opinion as to how a POSITA would understand Jiang.

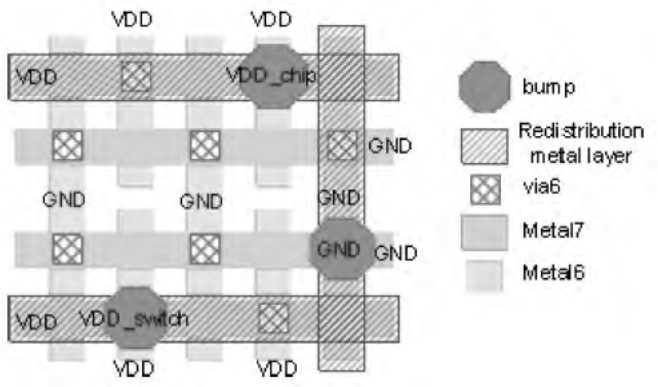
85. Additionally, to the extent Jiang did not disclose independent operability to a POSITA, it is my opinion that a POSITA would have found it obvious for Jiang's sleep transistors to be independently operable as expressly disclosed in either Jiang2 or Jiang3. Just as Jiang2, Jiang3, and Kim (EX1009) expressly teach, individual macros or blocks are assumed to be independently controlled for power gating purposes. Jiang's provision of a sleep transistor for each macro provides that independent control. To the extent this is not already understood

by a POSITA from Jiang, a POSITA would have recognized that providing independent control for each macro would provide more granular control and help reduce power consumption. EX1009, Abstract ("A multiple power domain strategy in which each power domain has an independent power gating structure is an effective means for reducing leakage power consumption in a system-on-a-chip."); *see also* EX1010, 1:37-43. It is my opinion that allowing each of Jiang's sleep transistors, and their respective partial local power meshes and power domains, to be powered on and off independently would have been routine application of a known—indeed the "assume[d]"—functionality of the sleep transistors in the Jiang device with a reasonable expectation of success especially given its ubiquitous usage. EX1008, 4.

86. I have also been asked to opine on whether it also would have been obvious for Jiang's global power mesh to supply independent voltages to the first and second power domains, such as separate Vdd1 and Vdd2, for example. I note that the '218 Patent acknowledges that it was "common practice[] to arrange multiple power domains" in a chip where "different power domains are coupled to different powers." EX1001, 1:28-31; *see also* EX1012, 157 (Fig. 11-2). In my opinion, supplying independent voltages to the first and second power domains also would have been obvious because it was a well known practice in the industry where

the underlying macros required different power supply voltages. There are many reasons why that might be the case for a particular integrated circuit.

87. For example, Li discloses such an arrangement. Li discloses an integrated circuit with multiple power domains (four CPUs as well as networking hardware in the BCM1280) and a power routing structure including global and partial local power meshes. EX1005, 493. Like Jiang, Li's global power mesh comprises horizontal and vertical wires, but Li's global power mesh carries two independent supply voltages (VDD_chip and VDD_switch) as well as ground (GND) as illustrated in Li's Figure 3, below. *Id*., 493-494.

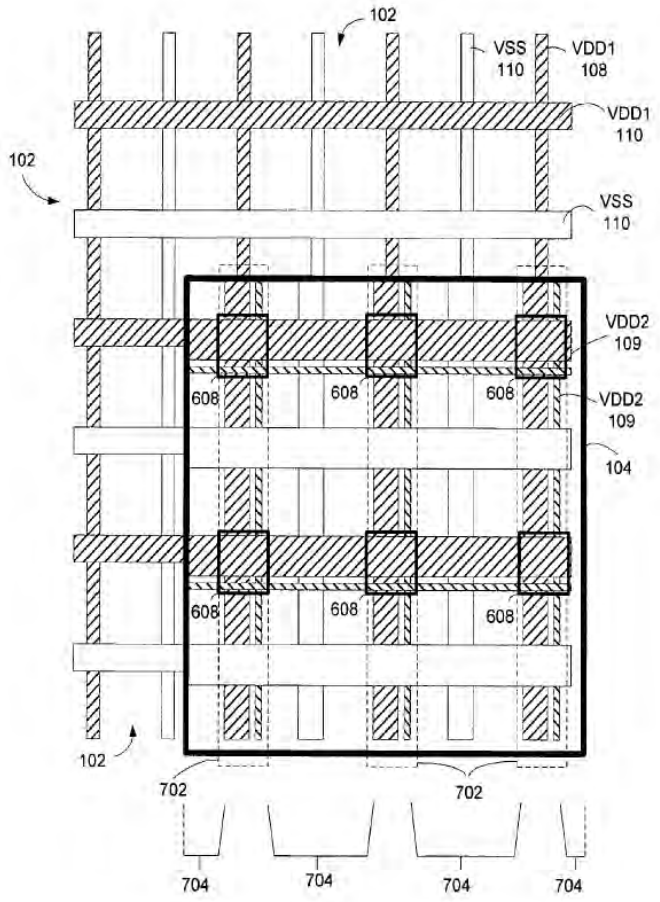


Id., Fig. 3.

88. Li teaches that the global power mesh provides these independent supply voltages (VDD_chip and VDD_switch) to different power domains through partial local power meshes. EX1005, 493 ("On the BCM1280, Metal-6 and metal-7 are extensively used in distributing power and ground across the chip. Ground (GND) and power (VDD_chip, VDD_switch) lines are routed alternately on Metal-

6 in the vertical direction and Metal-7 in the horizontal direction. This forms the power grid structure at the chip top level. The power and ground lines in the local sections are grided on Metal-2 through Metal-5, on which the local power grids are formed at the block level. The local power grids are left floating until final assembly at the full-chip level. At the final stage of the layout design, an in-house automated procedure is applied, connecting local logic to the top-level power grid, to implement a complete full-chip power distribution network."); *id*., 495 ("[T]here are two power supply inputs VDD_chip and VDD_switch at the package level in this design."). Li explains that "[a]ll four CPU cores operate at the same supply voltage, VDD_chip …." *Id*., 495. But "VDD_switch provides power for all the internal logic of the node controller (NC), packet manager (PM), switch and HT/SPI-4 ports." *Id*.; *see also id*., 493 ("As a result of function and logic requirements, there are multiple voltage regions across the chip."), 491 ("[T]he chip is divided into two logic voltage regions (1.1V)."), 492 (Table I: "Supply Voltages 1.1V, 2.5V and 3.3V").

89. Chiu also discloses an integrated circuit with multiple voltage domains where a global power mesh supplies separate voltages (VDD1 and VDD2) to different domains as shown in Chiu's Figure 7, below.



EX1006, Fig. 7; *see also id.*, 1:54-60, 2:55-61. Chiu also discloses the use of "power-ground rails (associated with the middle or lower layers of the integrated circuit)" to distribute power to the underlying cells of the integrated circuit. EX1006, 2:55-61; *see also id.*, Fig. 8, 9:7-26 ("FIG. 8 further illustrates a plurality of horizontal lines. Each of these horizontal lines represent: (1) a row boundary of the IC floor plan or layout; and (2) a power-ground rail. Power ground rails 810 are power-ground rails at the voltage level of the selectably on voltage supply grid VDD2 109. Power-ground rails 812 are power-ground rails at the voltage level of the negative voltage supply grid VSS 110. Although the power-ground rails are

illustrated as spanning the entire portion 800 of the second voltage domain 104, it is recognized that the power-ground rails are only necessary to the extent cells requiring this voltage for operation are placed in these regions. FIG. 8 further illustrates voltage rail 814 at the voltage level of the positive voltage supply grid VDD1 108. Voltage rail 814 is the voltage rail used by the buffer cells 400 to convey the voltage of the positive voltage supply grid VDD1 108 from the initially-placed buffer cell 400 in column 802 to each other buffer cell 400 in the buffer cell clusters 804. Each of power-ground rails 810, 812 and the voltage rail 814 are located in intermediate metal layers of the integrated circuit."). These local power-ground rails serve the same purpose as a partial local power mesh but just happen to be a single direction layer of wires (or rails) instead of two layers of perpendicular wires forming a mesh or grid as in Jiang.

90. Based on the teachings of Li and Chiu, a POSITA would be motivated to use multiple independent supply voltages as part of a global power mesh to supply separate partial local power meshes with independent supply voltages. The purpose of this arrangement in Li was to supply circuits requiring different voltages (chip versus switch). EX1005, 495 ("VDD_chip provides power for all the internal logic except the node controller, packet manager, switch and HT/SPI-4 ports. … VDD_switch provides power for all the internal logic of the node controller (NC), packet manager (PM), switch and HT/SPI-4 ports."). The purpose of this

arrangement in Chiu was to provide a separate voltage supply that could be selectively turned off at the global level thus turning off everything supplied by VDD2, which is the "selectably on voltage supply grid." EX1006, 1:57-65. However, Chiu also disclosed that "the another voltage supply grid VDD2 109 may be any other voltage grid that is always on (as compared to being selectably on) and/or that is at a different voltage level than the voltage level associated with the positive voltage supply grid VDD1 108." *Id.*, 2:3-8.

91. In my opinion, it would have been obvious to use multiple independent voltages in the power meshes of Jiang. In my opinion, a POSITA would be motivated to supply multiple independent voltages to the power grids of Jiang to power Jiang's different power domains with different voltages. For example, I note the '218 Patent acknowledges that it was known that "different powers need to be supplied to the different circuits inside the chip so that the circuits can perform different operations during the sleeping mode." EX1001, 1:26-28; *see also id*., 1:30-33 ("In other words, circuits in different power domains are coupled to different powers respectively so that the circuits of different power domains use different powers to support the different operations that are just mentioned."). To the extent that Jiang's macros required different voltages to function correctly, a POSITA would have been aware of examples of supplying different voltages via global and partial local power meshes and would have readily applied those teachings to Jiang

to supply different voltages to different macros. Implementation of different types of circuitry, such as the networking circuitry in Li in one or more of Jiang's macros and the CPU core circuitry in Li in a different macro, would have required different voltages just as they did in Li and thus would have necessitated implementation of global and partial local power meshes to supply the different voltages. Such systems, like the system on a chip in Li, were known in November 2007 and would motivate the use of multiple different voltage power supplies just as they did in Li.

92. Additionally, a POSITA would have known that providing for separate power supplies allows for powering certain portions of a chip at higher voltages, such as timing-critical blocks or input-output circuits, while powering the rest of the chip at a lower voltage to save power. EX1014, 3 ("In active state, supply voltage can be controlled to reduce power, albeit in the limited ranges allowed in aggressively scaled technologies. *Multiple-voltage* and *variable voltage* techniques have been developed to this purpose [11]. In multiple-voltage circuits two or more power supply voltages are distributed on chip. Similarly to the multiple-threshold scheme, timing-critical transistors can be powered at a high voltage, while most transistors are connected to the low voltage supply."); EX1012, 16-17, 177-78; EX1010, 6:19-31 (discussing beneficial use of separate power supplies for power save mode)). Powering those portions of a chip at the lowest voltage that can support their functionality saves overall power consumption on the chip because lower

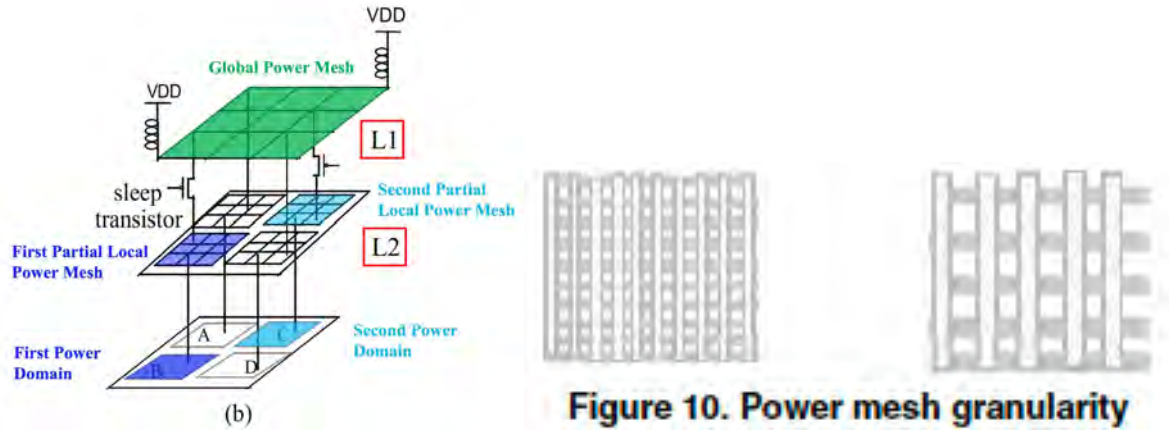
voltage translates into lower power consumption on a chip. EX1012, 16 ("Since dynamic power is proportional to V_{DD}^2, lowering V_{DD} on selected blocks helps reduce power significantly."); EX1005, 493 ("As a result of function and logic requirements, there are multiple voltage regions across the chip. This design style enables power-saving capability with a selectable configuration, allowing the chip to be an optimal fit into a broad variety of applications.").

93. Applying multiple independent supply voltages to Jiang's global power mesh would have been a routine application of a known feature to Jiang's device with a reasonable expectation of success. Indeed, as the '218 Patent acknowledges, such features were "common practice[]." EX1001, 1:26-33.

E. Claim 12[d]: "wherein the first partial local power mesh and the second partial local power mesh are positioned on the same metal layer while the global power mesh and the first local power mesh are positioned on different metal layers;"

94. Jiang discloses this limitation. As shown in Figure 1(b) below, Jiang discloses that the global power mesh is on L1 and the partial local power meshes are on L2. Jiang, however, also discloses in Figure 10 that each of these meshes consist of two metal layers. As shown in Figure 10, vertical lines are on an upper metal layer while horizontal lines are on a lower metal layer. Thus, a POSITA would understand L1 to include two metal layers and L2 to include two metal layers. A POSITA would also understand that the L1 metal layers are different from the L2

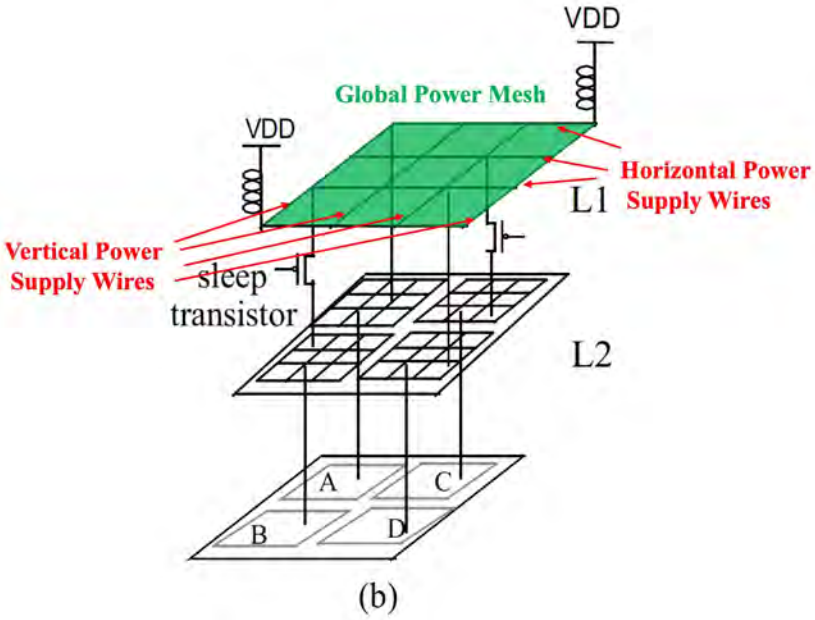
metal layers—*i.e.*, there is no overlap between L1 and L2 metal layers. The use of two metal layers for a mesh was commonplace in the integrated circuit industry.



EX1004, Fig. 1(b) (annotated), Fig. 10; *see also* EX1015 (similarly depicting multiple metal layers). Jiang also refers to its global mesh as "[t]he ***upper*** power mesh" and its local meshes as "[t]he ***lower*** power mesh," EX1004, 2 (emphases added), indicating that they are on different metal layers.

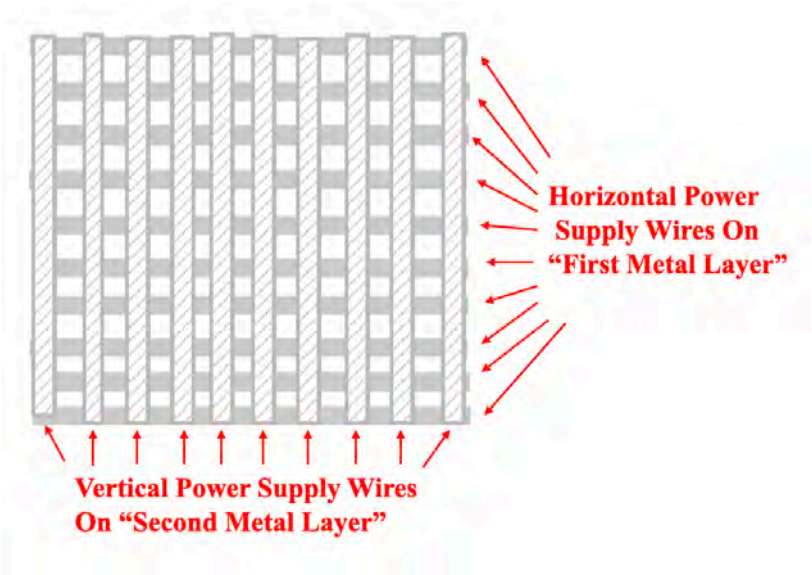
F. Claim 12[e]: "wherein the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer; and"

95. Jiang discloses this limitation. As I explained above regarding 12[d], Jiang discloses that its global power mesh includes a plurality of horizontal and vertical power supply wires which can be seen in Jiang's Figure 1(b), below.

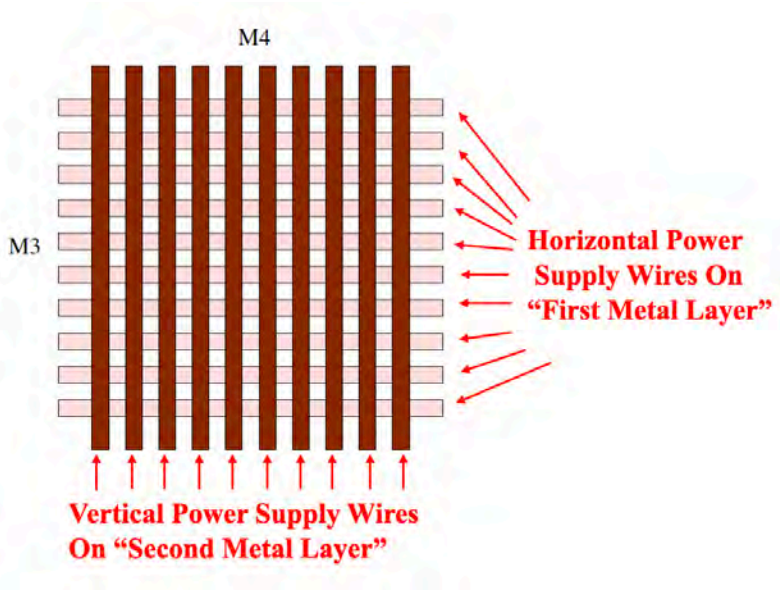


EX1004, Fig. 1(b) (annotated); *see also id.*, 7 (discussing the "horizontal and vertical segments" of the "power mesh").

96. As I explained above regarding 12[d], a POSITA would understand that the horizontal and vertical wires in the global power mesh would be on two different layers ("a first metal layer" and "a second metal layer"). Jiang's Figure 10 (excerpted below) shows a more detailed version of the power meshes in Jiang with the horizontal wires on one metal layer ("a first metal layer") and the vertical wires above the horizontal wires, on a higher metal layer ("a second metal layer").



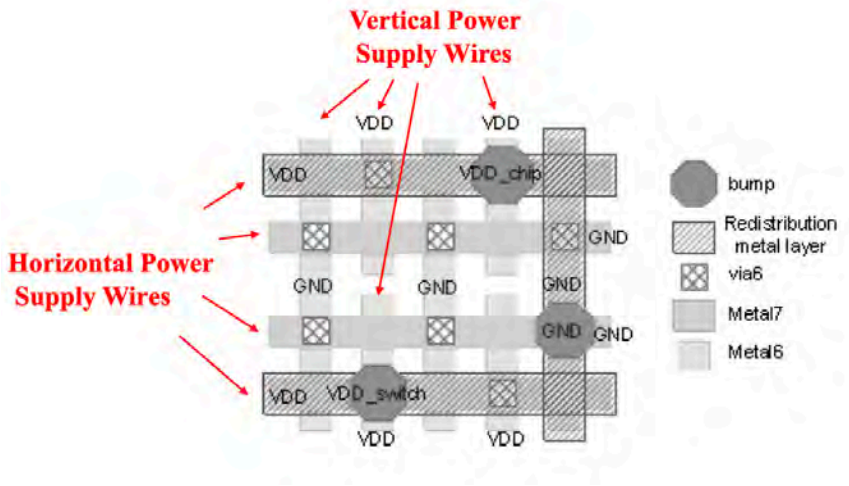
EX1004, Fig. 10 (excerpted, annotated). A POSITA would understand that Jiang's Figure 10 depicting the vertical power supply wires above the horizontal wires means that these wires are on different metal layers. The difference in cross hatching the vertical wires and shading the horizontal wires is intended to show these are different metal layers. This use of single direction wires on a single metal layer is ubiquitous in the industry. Both Li and Chiu also disclose single direction wires on a single metal layer. *See* EX1005, Fig. 3; EX1006, Fig. 7. Further, one of Jiang's co-authors similarly depicted a power mesh with horizontal and vertical power supply wires on two different metal layers ("M3" and "M4," respectively), as shown below.



EX1015, Fig. 3(a) (shading in original; red annotations added); *see also id*., 26.

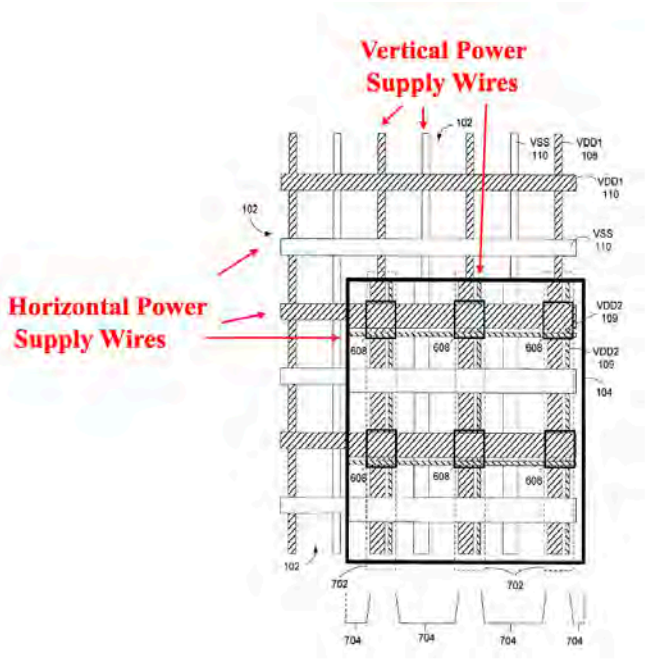
97. I have been asked to consider whether if Jiang's global power mesh did not include horizontal and vertical power supply wires on different metal layers it would have been obvious to use a global power mesh with this configuration in Jiang. In my opinion, the use of horizontal and vertical power supply wires on two different metal layers in Jiang's system would have been obvious. First, that is what Jiang actually discloses using. Second, as I explained above, it was well-known to route horizontal and vertical power supply wires of a mesh on two different layers as described above in Li and Chiu. *See* Section IX.D.

98. Li's global power mesh consists of horizontal and vertical wires where the horizontal and vertical wires are routed on two different metal layers as shown below in Figure 3 and stated expressly in Li.



EX1005, Fig. 3 (annotated); *see also id.*, 493 ("Ground (GND) and power (VDD chip, VDD switch) lines are routed alternately on Metal-6 in the vertical direction and Metal-7 in the horizontal direction. This forms the power grid structure at the chip top level.").

99. Similarly, Chiu teaches a global power mesh with horizontal power supply wires on a first metal layer and vertical power supply wires on a second, lower, metal layer, as shown below in Chiu's Figure 7.



EX1006, Fig. 7 (annotated); *see also id.*, 5:15-18 ("[T]he substantially horizontal members are typically located in a higher metal layer than the corresponding substantially vertical members of the power supply grids.").

100. This concept of using horizontal power supply wires on one metal layer and vertical power supply wires on a second, different metal layer was a well-known basic feature of integrated circuit design. For example, U.S. Patent No. 7,671,623 to Blisson states, "Typically, a routing grid is a meshing of horizontal and vertical metal rails on two metallization layers, which covers the core of the circuit." EX1016, 8:57-59. Similarly, U.S. Patent No. 6,925,627 to Longway includes Figure 9 (reproduced below) and explains the following:

> In the illustrated embodiment, the upper power grid occupies two upper metal layers. Alternating vertical power (VDD) rails 317 and vertical

ground (VSS) rails 318 are routed in an upper metal layer such as, for example, metal6. Alternating horizontal power (VDD) rails 319 and horizontal ground (VSS) rails 320 are routed in an adjacent upper metal layer such as, for example, metal5.

EX1018, 9:17-23.

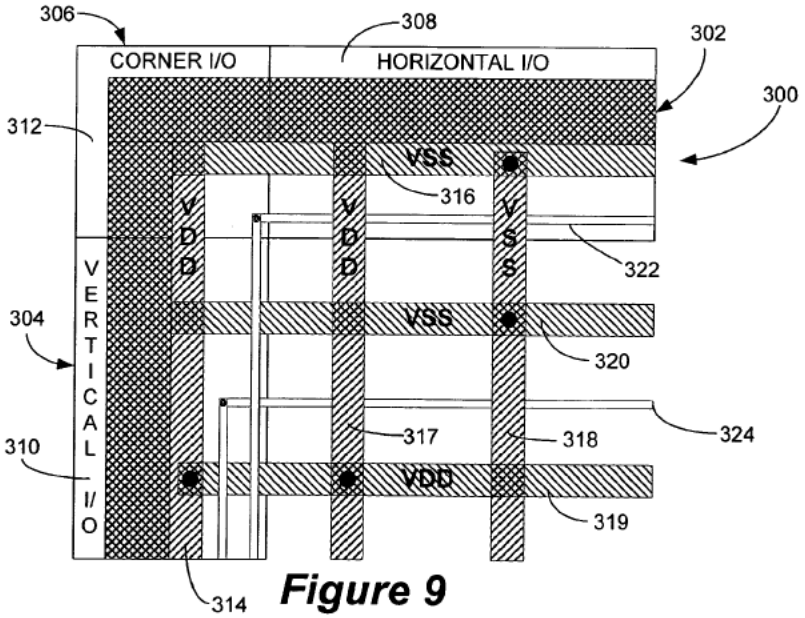


Figure 9

Id., Fig. 9. Thus, the use of single direction wires on a single metal layer to form a two-metal-layer grid of horizontal and vertical power supply wires was well known and commonplace in the industry by November 2007.

101. A POSITA would understand that routing horizontal and vertical power supply wires on different metal layers, as shown in Li and Chiu, would be necessary to prevent the global power mesh from shorting. Specifically, since positive voltage and ground are required at numerous points within a typical integrated circuit block, it is necessary to have pathways to distribute both VDD and VSS in horizontal and

vertical directions to cover the requisite two dimensional needs of the circuit. This cannot be achieved in a single layer of metal, since this would necessarily result in VDD and VSS lines shorting to each other. As such, it is common therefore to perform the routing on two layers, such that VDD and VSS can both be distributed over two directions without shorting to each other; whenever VDD and VSS need to cross, they are passed on different layers. An example of this is shown in Figure 9 of Longway (EX1018), which shows VDD and VSS lines passing each other horizontally and vertically without shorting, as would be obvious to a POSITA. Also, as I explained above in limitation 12[c], a POSITA would be motivated to apply the global power mesh teachings of Li or Chiu to Jiang to provide two voltage supplies to Jiang's different power domains. *See* Section IX.D. A POSITA would also understand that the separation of horizontal and vertical power supply wires on different metal layers is also necessary to prevent VDD1 from improperly contacting VDD2 and equalizing the two supply voltages that were intended to be separate. Similarly, this separation of horizontal and vertical power supply wires on different metal layers is also necessary to prevent improper contacting of VDD and GND during two-dimensional routing. These reasons, well understood by a POSITA in 2007, are why the use of single direction wires on a single metal layer was commonplace in integrated circuits.

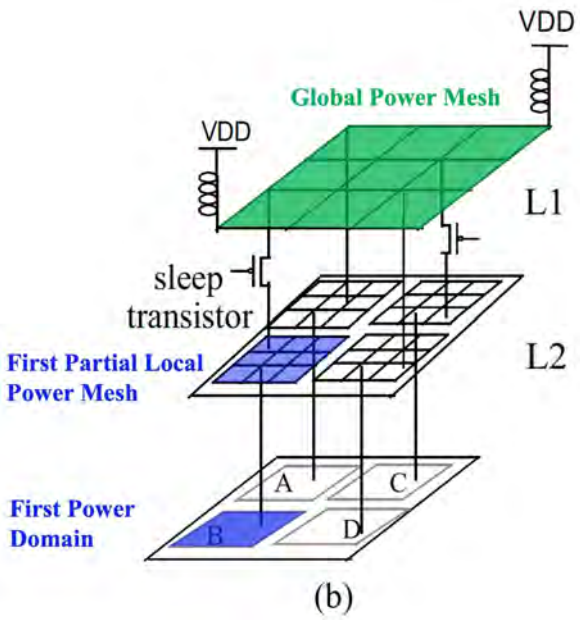
102. In my opinion, routing power grid wires horizontally and vertically on alternating metal layers in Jiang is disclosed by Jiang, but if it were not, its use in Jiang would have been routine application of a known—indeed the "normal"—routing structure in the Jiang device with a reasonable expectation of success especially given its ubiquitous usage.

G. Claim 12[f]: "wherein the first metal layer and the second metal layer are different layers."

103. As I explained in 12[e], Jiang discloses that its horizontal and vertical power wires are on different layers (a first metal layer, and a different, second metal layer). As I also explained in 12[e], even if Jiang did not disclose that, it would have been obvious to use different first and second metal layers for all the reasons explained regarding limitation 12[e]. *See* Section IX.F, *supra*.

H. Claim 13: "The power routing structure according to claim 12, wherein the global power mesh is positioned above the first local power mesh."

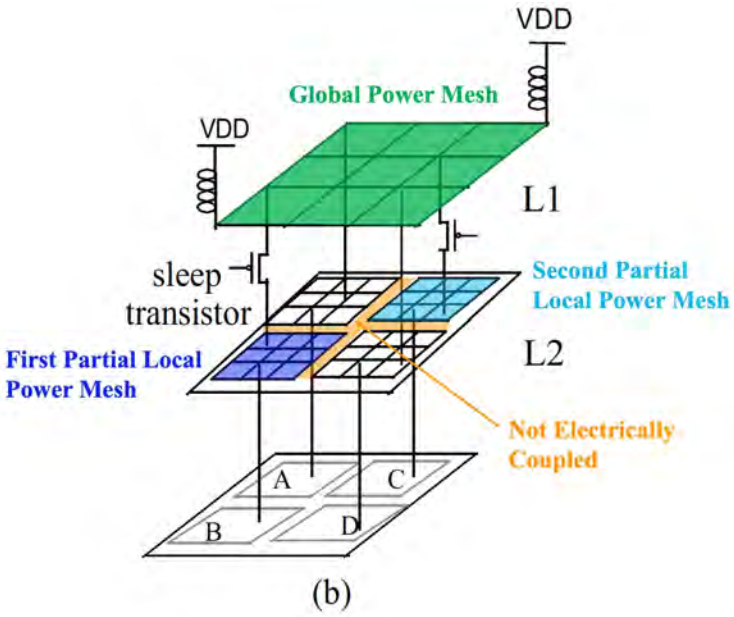
104. Jiang discloses the additional limitation of claim 13. Jiang discloses that its global power mesh is positioned above its first partial local power mesh and above all power domains, as can be seen in Figure 1(b), below.



EX1004, Fig. 1(b) (annotated). Jiang also refers to its global mesh as "[t]he ***upper*** power mesh" and its local meshes as "[t]he ***lower*** power mesh," EX1004, 2 (emphases added), indicating that the global power mesh is positioned above the first partial local power mesh.

I. Claim 14: "The power routing structure according to claim 13, wherein the first local power mesh and the second local power mesh are not electrically coupled."

105. Jiang discloses the additional limitation of claim 14. As shown in Jiang's Figure 1(b), there is a gap surrounding each partial local power mesh on L2 such that there are no interconnections between the power wires of these partial local power meshes. Thus, there is no electric coupling of one partial local power mesh to another on L2 in Jiang.



EX1004, Fig. 1(b) (annotated).

106. Each partial local power mesh in Jiang that is separated from the global power mesh by a sleep transistor is also further separated from electrical coupling to other partial local power meshes when its respective sleep transistor is turned off. As I explained regarding limitation 12[c], the sleep transistors in Jiang can disconnect the partial local power mesh from the global power mesh. EX1004, Abstract, 1, 2. A POSITA would understand that when either or both of the sleep transistors for macros B and C are turned off, the first and second meshes would not be electrically coupled for this additional reason. *Id*.

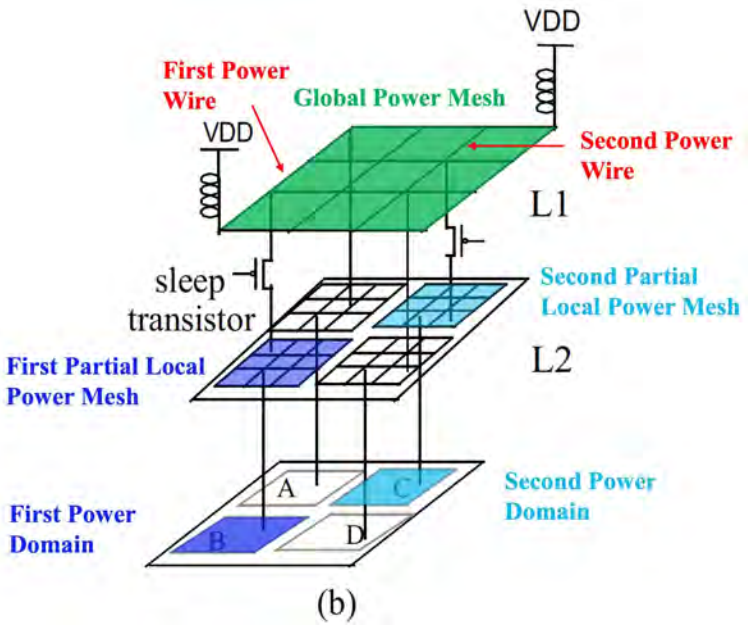
107. As I explained above regarding limitation 12[c], in my opinion, it would have been obvious to combine Jiang with either Li or Chiu's multi-voltage layouts so that Jiang's first and second partial local power meshes received separate supply

voltages from different wires in the global power mesh. A POSITA would understand that in this scenario, Jiang's global power mesh would still be above the first partial local power mesh as required by claim 13 because that is Jiang's structure as well as Li's and Chiu's. EX1005, 493 (describing the global power mesh on metal-6 and metal-7 forming "the power grid structure at the chip top level"); EX1006, 2:55-61 ("Generally, each of the voltage supply grids (positive and negative) in an integrated circuit are associated with the upper-most metal layers, are arranged in a grid (as further discussed below) and are coupled to cells and/or power-ground rails (associated with the middle or lower layers of the integrated circuit) using a piece of metal called a via stack.").

J. Claim 15: "The power routing structure according to claim 12, wherein the global power mesh comprises: at least one ground wire; at least one first power wire that provides the power needed by the first power domain; and at least one second power wire that provides the power needed by the second power domain."

108. The additional limitations of claim 15 would have been obvious over Jiang, or Jiang in view of Li or Chiu. As I explained above, Jiang discloses a global power mesh that includes a plurality of horizontal and vertical power wires on two different metal layers. EX1004, Figs. 1(b), 10; *see also id*., 7; Section IX.F. As I also explained above, Jiang discloses that its global power mesh provides the power needed by the first and second power domains and shows that in Figure 1(b). *See* Section IX.D. A POSITA would understand from those disclosures as well as Figure

1(b) that Jiang's global power mesh comprises at least one first power wire that provides the power needed by the first power domain and at least one second power wire that provides the power needed by the second power domain.



EX1004, Fig. 1(b) (annotated), 1-2.

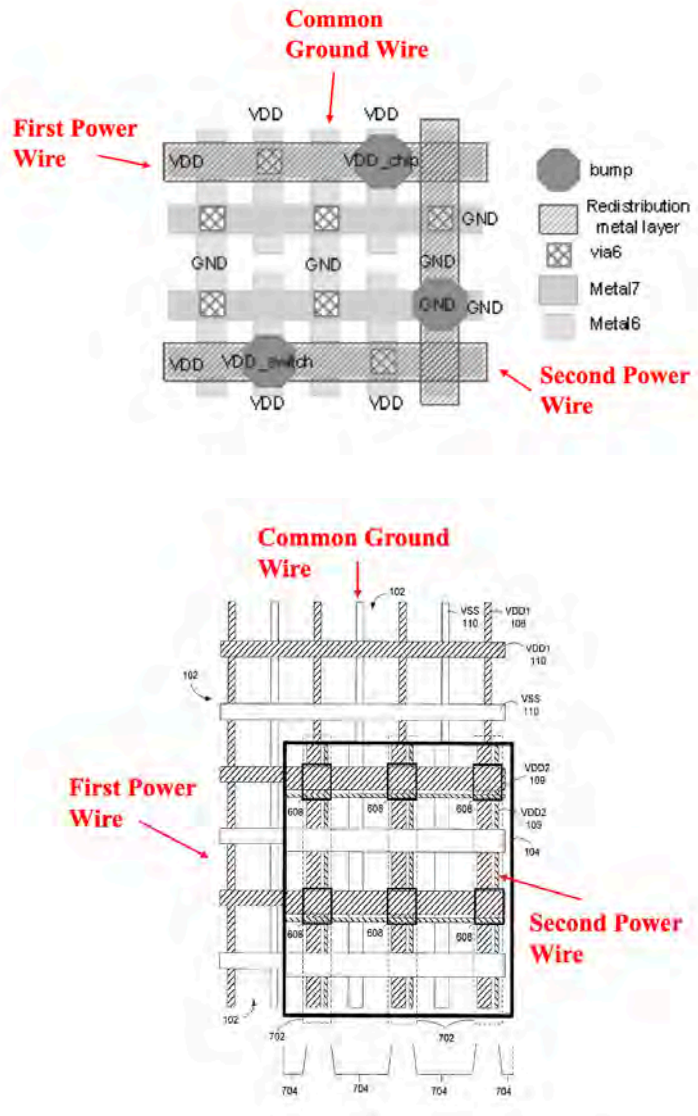
109. To the extent it is not inherent because a ground is required for the circuit to function, it is my opinion that it would have been obvious to also provide at least one ground wire as part of Jiang's global power mesh. A POSITA would understand circuits, including Jiang's power domains, require a ground connection. EX1012, 271 ("A power domain shall have one primary power net and one primary ground net. … A power domain is functional only if the primary power and ground supply nets are specified."); EX1001, 3:59-60 (discussing "the ground potential … needed by the power domain"). It was well known to supply the needed ground

connection through a global power mesh. That is how the needed ground is supplied in both Li and Chiu. EX1005, 493-94, Fig. 3; EX1006, 2:50-61 ("Implicit in the above discussion is the need and use of a negative voltage supply grid" such as "voltage supply grid VSS 110" which a POSITA would understand to be a ground connection), Fig. 7. Other references as well teach the use of the global power mesh to supply a ground connection. *E.g.*, EX1018, 9:17-23 ("[T]he upper power grid occupies two upper metal layers. Alternating vertical power (VDD) rails 317 and vertical ground (VSS) rails 318 are routed in an upper metal layer such as, for example, metal6. Alternating horizontal power (VDD) rails 319 and horizontal ground (VSS) rails 320 are routed in an adjacent upper metal layer such as, for example, metal5."). A POSITA would have been motivated to provide the ground connection as part of the global power mesh because a ground connection must be provided for the circuit to function, and routing the ground connection as part of the global power mesh was a routine practice for efficient use of metal layers with a known and well understood expectation of success as shown by its use in various prior art references.

110. Claim 15 does not require the first and second power wires to be tied to separate voltage supplies, but I have been asked to opine if this would have been obvious. It is my opinion that a POSITA would have found it obvious to power the two power domains by two power wires that are supplied by separate voltage

supplies as disclosed in Li or Chiu and for the reasons I explained above in 12[e]. *See* Section IX.F.

111. In this scenario, the two power wires supplying the separate voltage supplies to the two partial local power meshes and thus to the two underlying power domains would not be electrically coupled because the separate voltage supplies are independently provided. Both Li's and Chiu's global power meshes include a plurality of positive voltage supply wires and a common ground wire. A POSITA would understand that one of these positive voltage supply wires from one voltage supply would provide the power needed by the first domain, and another positive voltage supply wire from the other voltage supply would provide the power needed by the second power domain in this scenario, as shown below and as discussed in 12[c] and 12[e].

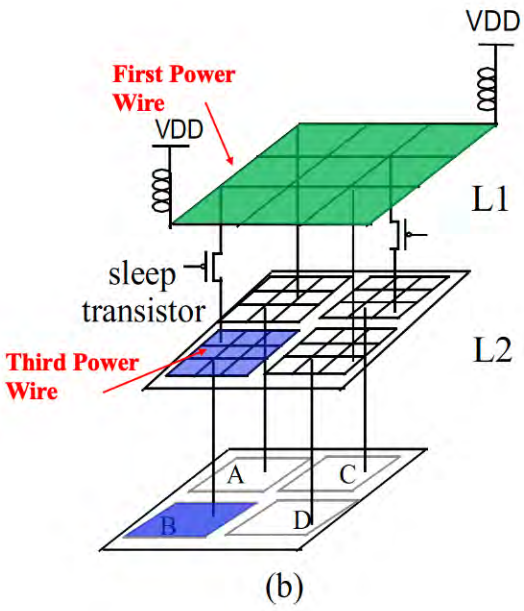


EX1005, Fig. 3 (annotated); EX1006, Fig. 7 (annotated).

K. Claim 16: "The power routing structure according to claim 15, wherein the first partial local power mesh comprises: at least one first local ground wire that couples to the ground wire of the global power mesh; and at least one third power wire that couples to the first power wire and the first power domain."

112. The additional limitations of claim 16 would have been obvious over Jiang or Jiang in view of Li or Chiu. Jiang discloses at least one third power wire

that couples to the first power wire and the first power domain, as illustrated in Jiang's Figure 1(b).



EX1004, Fig. 1(b) (annotated). When the sleep transistor switch is closed, Jiang's third power wire as labeled couples to both the first power wire and the first power domain as shown in the figure. *Id*. Moreover, the claim simply requires "at least one third power wire" such that the third power wire could be the entire collection of power wires in the partial local power mesh associated with macro B or any one or more of those power wires in the partial local power mesh associated with macro B.

113. To the extent a ground wire in Jiang's first partial local power mesh is not inherent because a ground is required for the circuit to function, it would have been obvious for a POSITA to include this. As I discussed above regarding claim

15, it would have been obvious to also provide at least one ground wire as part of Jiang's global power mesh to provide the ground supply needed by each of Jiang's power domains. *See* Section IX.J. To distribute that ground from the global power mesh to the power domains, a POSITA would have known to include ground wires in the partial local power meshes as well, which sit in between the global power mesh and the power domains. Thus, a POSITA would have found it obvious to include at least one first local ground wire in Jiang's first partial local power mesh to supply the ground reference needed by the underlying power domain. This at least one ground wire, which could be multiple ground wires, would necessarily couple to the common ground of the global power mesh of Li or Chiu as discussed in claim 15 and thus to all ground wires in the global power mesh.

114. Because ground is required for the circuit to function, it was known that not only could global power meshes include ground wires, but also partial local power meshes could include local ground wires. For example, Li discloses a power routing structure with "ground lines in the local sections" of its power grid. EX1005, 493. A POSITA would have been motivated to include ground wires in Jiang's first partial local power mesh to provide the ground potential required by Jiang's first power domain. EX1012, 271 ("A power domain is functional only if the primary power and ground supply nets are specified."); EX1001, 3:56-60 ("[T]he partial local power meshes 310 comprises [sic] a power wire 311 to supply the working

voltage V_{DD1} needed by the power domain 110 and a ground wire 312 to supply the ground potential V_{GND} needed by the power domain 110."). A POSITA would have included the ground wires in the partial local power mesh necessary to cover the underlying power domain, and there would necessarily have been at least one ground wire in the partial local power mesh. A POSITA would have had a reasonable expectation of success in adding this at least one ground wire to the partial local power mesh because supplying ground wires via global and partial local power meshes was a known technique as discussed above and as disclosed, for example, in Li and Chiu.

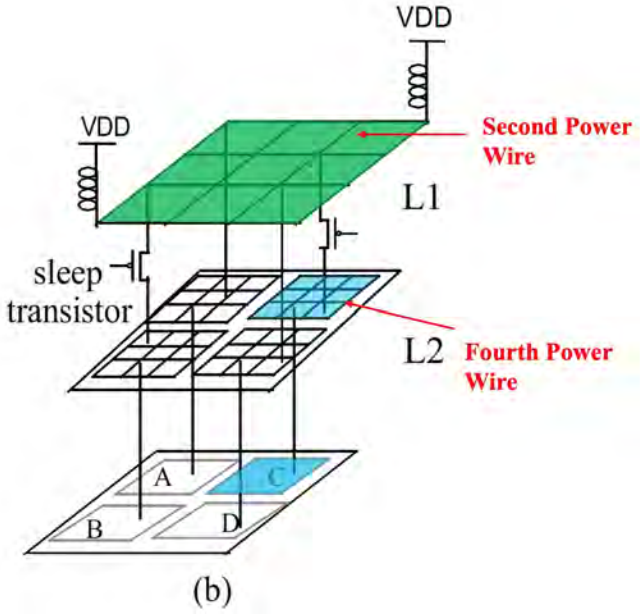
115. As I explained above, a POSITA's motivation for providing at least one ground wire in the partial local power mesh of Jiang would have been to supply the ground potential needed by the underlying power domain. Thus, a POSITA also would have understood that at least one ground wire in the partial local power mesh needed to be coupled to the first power domain for it to have any value in providing the ground potential needed by the first power domain. In the same manner, the POSITA would have understood that the power wires in the partial local power mesh needed to be coupled to the first power domain to have any value in providing the positive voltage supply needed by the power domain. Jiang shows the power connection from the first partial local power mesh to the first power domain in Figure 1(b). EX1004, Fig. 1(b). A POSITA would have known and expected that a

corresponding ground connection would also be present if the ground is supplied through the global and partial local power meshes as discussed above. For all the reasons I provided above regarding the well-known structure of global and partial local power meshes, adding a ground wire to Jiang's first partial local power mesh would have been routine application of a known functionality of a hierarchical power-ground distribution network with a reasonable expectation of success especially given its common usage. EX1005, 493.

116. In my opinion, this limitation also would have been obvious in view of the separate supply voltages of Li or Chiu, which would still require a ground supply for the first power domain, for all the reasons explained above regarding limitation 12[e]. *See* Section IX.F.

L. Claim 17: "The power routing structure according to claim 16, wherein the second partial local power mesh comprises: at least one second local ground wire that couples to the ground wire of the global power mesh; and at least one fourth power wire that couples to the second power wire and the second power domain."

117. Jiang discloses that the second partial local power mesh includes at least one fourth power wire that couples to the second power wire and the second power domain, as illustrated in Jiang's Figure 1(b). Again, because the fourth power wire is "at least one," it could be any one or even all the power wires included in the second partial local power mesh of Jiang identified below in light blue on L2.



EX1004, Fig. 1(b) (annotated).

118. It would have been obvious to a POSITA to add the at least one second local ground wire that couples to the ground wire of the global power mesh for all the same reasons I discussed above regarding claim 16. *See* Section IX.K.

119. In my opinion, this limitation also would have been obvious in view of the separate supply voltages of Li or Chiu for all the reasons explained above regarding limitation 12[e]. *See* Section IX.F. Additionally, even if separate supply voltages were used, a POSITA would understand that a ground supply was also necessary for all the reasons I provided above regarding claim 16. *See* Section IX.K.

M. Claim 18: "The power routing structure according to claim 17, wherein the first local ground wire and the second local ground wire share the same ground wire of the global power mesh."

120. First, Jiang's single voltage supply would have a single ground supply that was common to all local power meshes and all power domains. Second, even if Jiang were modified to use independent voltage supplies as in Li or Chiu, for all the reasons I provided above regarding claims 15-17, it would have been obvious for a POSITA to add a common ground supply to Jiang's global power mesh and partial local power meshes in view of Li or Chiu. *See* Sections IX.J-L. Both Li's and Chiu's ground supply is a common ground used throughout the chip. EX1005, 493 ("BCM1280 is designed with two power supply inputs and one ground input at the package level."), 494 (Fig. 3) (showing single ground in both Metal6 and Metal7); EX1006, Figs. 6, 7 (showing a single negative supply grid VSS (110)). The use of a common ground even for power-gated integrated circuits was known to a POSITA. *E.g.*, EX1012, 85 (describing a SALT chip with an ARM core and a USB core that are "independently power gated" and "thus they switch VDD and use a common ground").

121. A POSITA would understand that in a system with a single ground supply, all the ground wires in the global power mesh would be shared by all the ground wires in the partial local power meshes. That is because all of the ground wires in each partial local power mesh would be coupled to all of the ground wires

in the single common ground global power mesh. In other words, if the power routing system had a single ground supply, then the ground wires in each partial local power mesh would be coupled to the same mesh of ground wires in the global power mesh. Indeed, this ensures that a common ground is provided to the entire circuit, thus providing a strong equipotential as is needed for reliable circuit operation; indeed, this is the very purpose of using ground as a reference potential.

X. GROUND 3 – CLAIMS 1-11 AND 19-20 ARE OBVIOUS OVER JIANG IN VIEW OF JIANG2 AND JIANG3, OPTIONALLY IN FURTHER VIEW OF LI OR CHIU, AND IN FURTHER VIEW OF BERTOLET OR THE LOW POWER METHODOLOGY MANUAL

122. In my opinion, claims 1-11 and 19-20 would have been obvious over any of the combinations in Grounds 1-2, in further view of Bertolet or the Low Power Methodology Manual (LPMM).

A. Claim 1

123. Claim 1 is substantially similar to claim 12. As shown below, claim 1 differs from claim 12 in the following three ways: (1) claim 1 describes a power routing arrangement method instead of a power routing structure; (2) claim 1 requires the use of an automatic placement and routing (APR) tool for forming and coupling certain features; and (3) claim 12 provides the metal layer requirements for the local and global power meshes in 12[d], which are not in claim 1, rendering claim 1 broader in this respect than claim 12.

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Claim 1	Claim 12
[Preamble] A power routing arrangement method applied in an integrated circuit having multiple power domains, the arrangement method comprising:	[Preamble] A power routing structure applied in an integrated circuit having multiple power domains, comprising:
1[a] forming a first partial local power mesh according to the position of a first power domain of the integrated circuit **by an automatic placement and routing (APR) tool**;	12[a] a first partial local power mesh having its position corresponding to the position of a first power domain and coupling to the first power domain;
1[b] forming a second partial local power mesh according to the position of a second power domain of the integrated circuit **by the APR tool**;	12[b] a second partial local power mesh having its position corresponding to the position of a second power domain and coupling to the second power domain; and
1[c] forming a global power mesh that is utilized to provide the power needed by the first and the second power domains **by the APR tool**: 1[d] coupling the first partial local power mesh to the global power mesh and the first power domain **by the APR tool**; and 1[e] coupling the second partial local power mesh to the global power mesh	12[c] a global power mesh, coupling to the first local power mesh and the second local power mesh, to provide the power needed by the first power domain and the second domain separately;

Claim 1	Claim 12
and the second power domain **by the APR tool**;	
	12[d] wherein the first partial local power mesh and the second partial local power mesh are positioned on the same metal layer while the global power mesh and the first local power mesh are positioned on different metal layers;
1[f] wherein the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer, and	12[e] wherein the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer, and
1[g] wherein the first metal layer and the second metal layer are different layers.	12[g] wherein the first metal layer and the second metal layer are different layers.

EX1001, 6:59-7:15, 7:56-8:11.

124. Claim 1's first and second power domains, first and second partial local power meshes, and global power mesh are disclosed and/or rendered obvious for the reasons discussed above regarding limitations 12[preamble], 12[a]-[c], and 12[e]-[f]. *See* Sections IX.A-D, IX.F-G.

125. Regarding claim 1's "power routing arrangement method," again, I need not determine whether the preamble is limiting because it is disclosed or rendered obvious by the prior art asserted in Grounds 1-2. A POSITA would understand that simply using a particular arrangement or structure for power routing as disclosed in Jiang, Jiang2, Jiang3, Li, and Chiu is a power routing arrangement method thus satisfying the preamble. Also, use of a power routing arrangement method with Jiang's routing structure would have been obvious because a POSITA was well aware of the need to employ a power routing arrangement method when designing integrated circuits. It was a necessary step in the design of integrated circuits. In other words, to have a power routing arrangement one would need to provide a power routing structure, which would include simply selecting the structure in Jiang. A POSITA was well aware of the need to provide a power routing structure in integrated circuits. In addition to those disclosed in Jiang, Jiang2, Jiang3, Li, and Chiu, for example, LPMM and Bertolet both discuss such power routing arrangement methods that could be used to form the power routing structure in Jiang, as discussed in more detail below. EX1012, 177 ("Most EDA [Electronic Design Automation] tools provide some level of automated power network synthesis (PNS) capability for the distribution of power across a design. We recommend highly that the implementation of a multi-voltage design utilize this type of PNS capability wherever possible."); EX1013, 126 ("After custom macrocell placement,

a power distribution network is algorithmically generated using a custom SKILL program.").

126. Additionally, it is my opinion that a POSITA would have found it obvious to form and couple Jiang's power meshes as shown in Jiang's Figure 1(b) with an automatic placement and routing (APR) tool. In fact, that would have been the expectation of a POSITA in 2007. As the '218 Patent acknowledges, APR tools were "well-known." EX1001, 1:37. For example, Bertolet describes using a "custom SKILL program" to "algorithmically generate[]" "a power distribution network." EX1013, 126. Bertolet explains that this "algorithm provides the capability to define multiple power terrains by area and level of metal." *Id*. Indeed, Bertolet also explains that using the custom SKILL program, "Two other areas of the chip may share a common power grid on metal levels one and two, yet have different power grids on metal levels three through five." *Id*. Thus, it would have been possible to use Bertolet's custom SKILL program to create a global power mesh with underlying partial local power meshes.

127. Similarly, LPMM provides an example in Chapter 11 of designing the power distribution for "a multi-voltage power gated ARM1176JZF-S microprocessor." EX1012, 155. The ARM1176JZF-S uses three power domains each with a separate voltage supply as shown in Figure 11-2 below from LPMM.

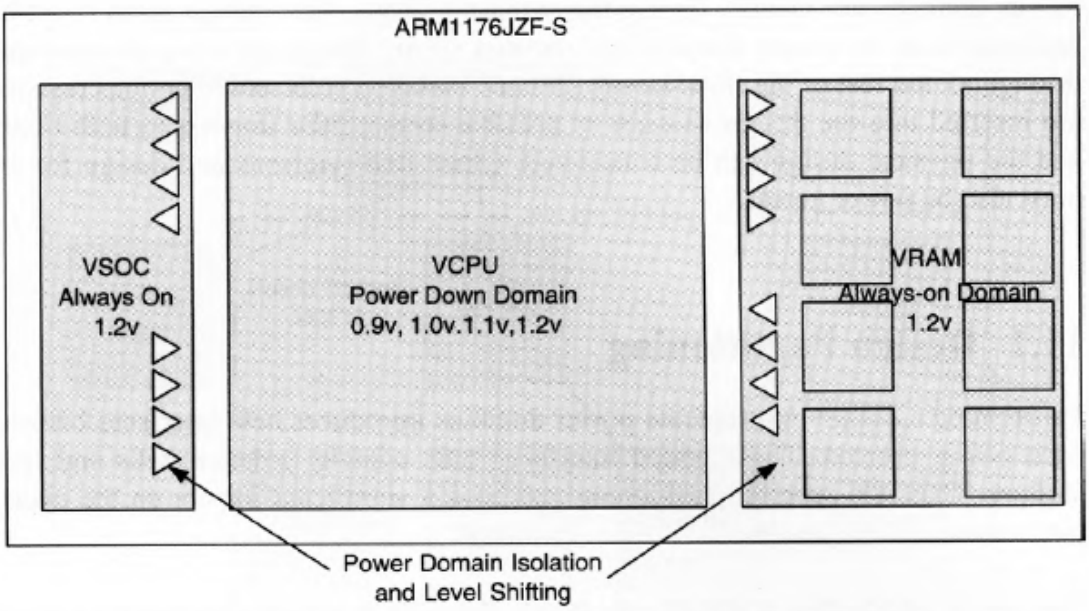


Figure 11-2 ARM1176JZF-S Multi-voltage, power gated design

Id., 157, Fig. 11-2. As LPMM explains, "VSOC always operates at full voltage …. The VCPU power domain can operate at a number of voltages and can be shutdown. VRAM operates at the same voltage as VSOC or is placed into retention if VCPU is shutdown." *Id.* Despite the complexity of this design, LPMM explains, "Since by definition, each power domain employs a different power strategy, it is likely that we will be routing different power rails to each voltage area." *Id.,* 177. Nevertheless, LPMM explains:

> Most EDA tools provide some level of automated power network synthesis (PNS) capability for the distribution of power across a design. We recommend highly that the implementation of a multi-voltage design utilize this type of PNS capability wherever possible. The number of concurrently changeable variables in a multi-voltage system

> is such that attempting to construct a power plan manually may result in a sub-optimal result both in terms of routing resources consumed and the voltage drop on the rails.

Id. Thus, LPMM expressly "recommend[s]" the use of an APR tool (Electronic Design Automation or EDA tool) for this application. *Id.* LPMM even explains that "[h]istorically, most power-gating designs used scripts to insert and place the switch cells, and create power straps and rails based on heuristic rules. Today, the sleep transistor power network can be synthesized using a power planning tool PNS [PNS] that considers all the three components." *Id.*, 178.

128. A POSITA in 2007 readily understood how to use APR tools to design power distribution networks on integrated circuits. Li disclosed an example of this, and Bertolet and LPMM confirm that understanding. In my opinion a POSITA knew to use an APR tool to form Jiang's power meshes, including forming the first partial local power mesh and coupling the components of the entire power routing structure. A POSITA would understand that using an automated tool for the placement and routing would save time and effort in the design of the chip and also avoid a less than optimal design. In fact, LPMM recommends implementing a "multi-voltage design" using an "automated power network synthesis" "wherever possible." EX1012, 177. Further, LPMM warns that "[t]he number of concurrently changeable variables in a multi-voltage system is such that attempting to construct a power plan manually may result in a suboptimal result both in terms of routing resources

consumed and the voltage drop on the rails." *Id*.; *see also id*., 178 ("Recommendations: Use a power planning tool which supports switch cells to create the sleep transistor power network including switch cell insertion and placement."). Indeed, a POSITA would know that "[p]lace and route tools are significantly faster and provide more flexibility and control on the place and route process." EX1024, 5:28-32; *see also id*., 5:32-34 (discussing the use of both "industry tools" and "proprietary tools").

129. Additionally, both Bertolet and LPMM would provide a POSITA with a reasonable expectation of success in using an APR tool to form the meshes of Jiang's sleep transistor power-gated routing structure and couple them together with Jiang's power domains. As I explained above, LPMM specifically recommends the usage of such a tool in the ARM1176JZF-S, which provides three separate voltage supplies along with power gating of two power domains. Further, Bertolet confirms that a "power distribution network" like Jiang's, with global and local grids on different metal layers, can be "algorithmically generated." EX1013, 126; EX1004, 1-2. Using an APR tool for Jiang's partial local power meshes would be no more than using "well-known" techniques to achieve a predictable outcome. *Id*., 177-78; EX1013, 126. Further supporting a POSITA's reasonable expectation of success, is the fact that prior to the '218 Patent in , Synopsys reported that "Realtek Semiconductor Corp. … and others have successfully taped out more than 15 multi-

voltage designs with Synopsys' Galaxy™ design platform RTL-to-GDSII advanced low-power solution." EX1025, 1. As shown from the index of Synopsys' press releases, this press release issued on July 19, 2006 (EX1026, 1), well before any application for the '218 Patent was filed. A POSITA would know that the RTL-to-GDSII design steps included placement and routing of the power routing network. Synopsis also reported that its platform "includes the most advanced low-power techniques, such as multi-voltage and MTCMOS power gating, as well as more commonly used techniques such as clock gating and multi-threshold voltages." *Id.* Accordingly, a POSITA would know that these numerous chip manufacturers had successfully placed and routed power routing networks for multi-voltage and power-gated chips automatically using the Synopsys Galaxy design platform. Power gating necessarily requires multiple power domains on the chip to permit some domains to continue operating while one or more are powered down (gated off) to save power. Indeed, well before the '218 Patent, a POSITA would have known that it was possible to use "automated techniques" in order to generate multi-voltage "row-by-row" meshes. EX1020, 3, Fig. 4

130. Accordingly, in my opinion, claim 1 would have been obvious over Jiang in view of Jiang2 and Jiang3, optionally in further view of Li or Chiu, and in further view of Bertolet and LPMM.

B. Claim 2: "The arrangement method according to claim 1, wherein the first partial local power mesh and the second partial local power mesh are positioned on the same metal layer."

131. This limitation is disclosed or rendered obvious for the reasons I discussed regarding limitation 12[d]. *See* Section IX.E.

C. Claim 3: "The arrangement method according to claim 2, wherein the global power mesh and the first local power mesh are positioned on different metal layers."

132. This limitation is disclosed or rendered obvious for the reasons I discussed regarding limitation 12[d]. *See* Section IX.E.

D. Claim 4: "The arrangement method according to claim 3, wherein the global power mesh is positioned above the first local power mesh."

133. This limitation is disclosed or rendered obvious for the reasons I discussed regarding claim 13. *See* Section IX.H.

E. Claim 5: "The arrangement method according to claim 2, wherein the first partial local power mesh and the second partial local power mesh are not electrically coupled."

134. This limitation is disclosed or rendered obvious for the reasons I discussed regarding claim 14. *See* Section IX.I.

F. Claim 6: "The arrangement method according to claim 1, wherein the global power mesh comprises at least one ground wire, at least one first power wire that provides power to the first power

domain, and at least one second power wire that provides power to the second power domain."

135. This limitation is disclosed or rendered obvious for the reasons I discussed regarding claim 15. *See* Section IX.J.

G. Claim 7: "The arrangement method according to claim 6, wherein the first partial local power mesh comprises: at least one first local ground wire that couples to the ground wire of the global power mesh; and at least one third power wire that couples to the first power wire and the first power domain."

136. This limitation is disclosed or rendered obvious for the reasons discussed regarding claim 16. *See* Section IX.K.

H. Claim 8: "The arrangement method according to claim 7, wherein the second partial local power mesh comprises: at least one second local ground wire that couples to the ground wire of the global power mesh; and at least one fourth power wire that couples to the second power wire and the second power domain."

137. This limitation is disclosed or rendered obvious for the reasons discussed regarding claim 17. *See* Section IX.L.

I. Claim 9: "The arrangement method according to claim 8, wherein the first local ground wire and the second local ground wire share the same ground wire of the global power mesh."

138. This limitation is disclosed or rendered obvious for the reasons discussed regarding claim 18. *See* Section IX.M.

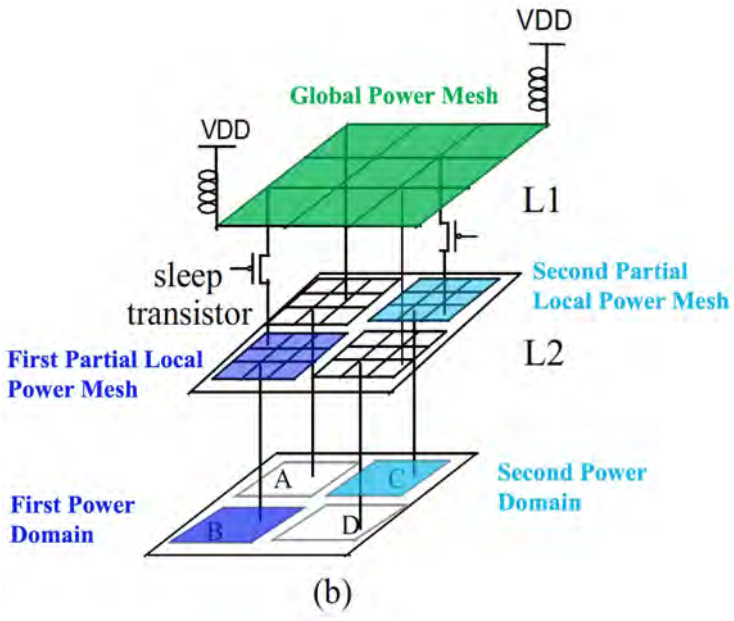
J. Claim 10: "The arrangement method according to claim 1, wherein the positions of the first partial local power mesh and the

second partial local power mesh correspond to the first power domain and the second power domain, respectively."

139. This limitation is disclosed or rendered obvious for the reasons discussed regarding limitations 12[a]-12[b]. *See* Sections IX.B-C.

K. Claim 11: "The arrangement method according to claim 1, wherein the global power mesh is distributed evenly above the first local power mesh and the area of the second local power mesh."

140. Jiang discloses this limitation. As can be seen in Figure 1(b), below, Jiang's global power mesh is distributed evenly above all partial local power meshes. The wires in the global power mesh are shown evenly distributed across the entire chip in both the vertical and horizontal directions.



EX1004, Fig. 1(b) (annotated). Jiang also refers to its global mesh as "[t]he ***upper*** power mesh" and its local meshes as "[t]he ***lower*** power mesh," EX1004, 2

(emphases added), indicating that the global mesh is above the local meshes. Figure 10 of Jiang also shows examples of the granularity of the power meshes used in Figure 1(b), and both levels of granularity show an even distribution of power wires across the design.

Figure 10. Power mesh granularity

Id., Fig. 10.

L. Claim 19[preamble]: "A power routing arrangement method applied in an integrated circuit having multiple power domains, the arrangement method comprising:"

141. To the extent the preamble is limiting, it is obvious over the combination for the same reasons I discussed regarding claim 1. *See* Section X.A.

M. Claim 19[a]: "providing a global power mesh, positioned above a first power domain and a second power domain, comprising at least one first power wire that provides the voltage needed by the first power domain, at least one second power wire that provides the voltage needed by the second power domain, and at least one ground wire that provides the ground potential needed by the first power domain and the second power domain by an automatic placement and routing (APR) tool;"

142. The combination discloses or renders obvious the global power mesh as claimed for the reasons discussed regarding limitation 12[c] and claims 13 and 15. *See* Sections IX.D, IX.H, IX.J.

143. In my opinion, it would have been obvious to provide this global power mesh and all other features of the power routing structure of claim 19 with an APR tool for the reasons I provided with respect to claim 1. *See* Section X.A.

N. Claim 19[b]: "coupling the first power wire and the ground wire of the global power mesh to the first power domain by the APR tool; and"

144. The combination renders obvious that the first power wire and ground wire are coupled to the first domain for the reasons discussed regarding claims 16 and 18. *See* Sections IX.K, IX.M. Further, it would have been obvious to use an APR tool in this application for the same reasons cited above regarding 19[a] and claim 1. *See* Section X.M. Additionally, Li discloses an "in-house automated procedure" for "connecting local logic to the top-level power grid," which, in my opinion, would further motivate use of such an APR tool in this application. EX1005, 493.

O. Claim 19[c]: "coupling the second power wire and the ground wire of the global power mesh to the second power domain by the APR tool;"

145. The combination renders obvious that the second power wire and ground wire are coupled to the second power domain for the reasons discussed regarding claims 16, 17, 18, and 19(b). *See* Sections IX.K-M. Further, it would have been obvious to use an APR tool in this application for the same reasons cited above regarding limitation 19[a] and claim 1. *See* Section X.M.

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P. Claim 19[d]: "wherein the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer; and"

146. The combination discloses or renders this limitation obvious for the same reasons discussed regarding limitation 12[e]. *See* Section IX.F.

Q. Claim 19[e]: "wherein the first metal layer and the second metal layer are different layers."

147. The combination discloses or renders this limitation obvious for the same reasons discussed regarding limitation 12[f]. *See* Section IX.G.

R. Claim 20: "The arrangement method according to claim 19, wherein the first power domain and the second power domain share the same ground wire of the global power mesh."

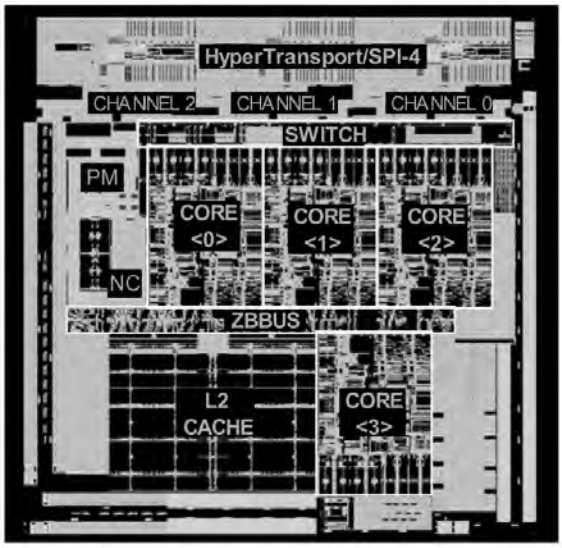
148. The combination discloses or renders this limitation obvious for the same reasons discussed regarding claim 18. *See* Section IX.M.

XI. GROUND 4 – CLAIMS 12-18 ARE OBVIOUS OVER LI IN VIEW OF JIANG

A. Claim 12[preamble]: "A power routing structure applied in an integrated circuit having multiple power domains, comprising:"

149. While I have been informed that claim preambles are not always limiting, to the extent it is limiting, Li discloses the preamble. Because Li discloses the preamble, I need not determine whether the preamble is limiting. Li's exemplary embodiment is the Broadcom BCM1280 chip shown below. The BCM1280 is a

system on a chip "with four 64-bit MIPS™ CPU cores … as well as on-die 1MB L2 cache, and dedicated networking hardware." EX1005, 491.



EX1005, Fig. 1. Li explains that "[e]ach single core, isolated from the others by a triple-well, forms a separate processor region. Therefore, under the full-chip context, each core is now built in a unique voltage region. In addition to the complexity of the multiple ground domains, the chip is divided into two logic voltage regions (1.1V)." *Id.*, 491. Li also lists three supply voltages for the chip: "1.1V, 2.5V and 3.3V." *Id.*, 492. Li teaches that its "multiple voltage regions across the chip" help "enable[] power-saving capability with a selectable configuration, allowing the chip to be an optimal fit into a broad variety of applications." *Id.*, 493.

150. Li describes the power routing structure for the BCM1280 chip including a global power grid, as shown in Li's Figure 3 below, and multiple local power grids.

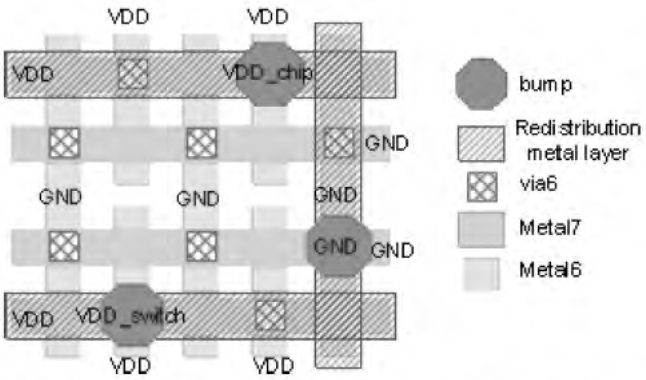


Fig. 3. Power and ground are distributed from the bumps onto the chip-level power grid through a redistribution metal layer.

EX1005, Fig. 3. Li explains:

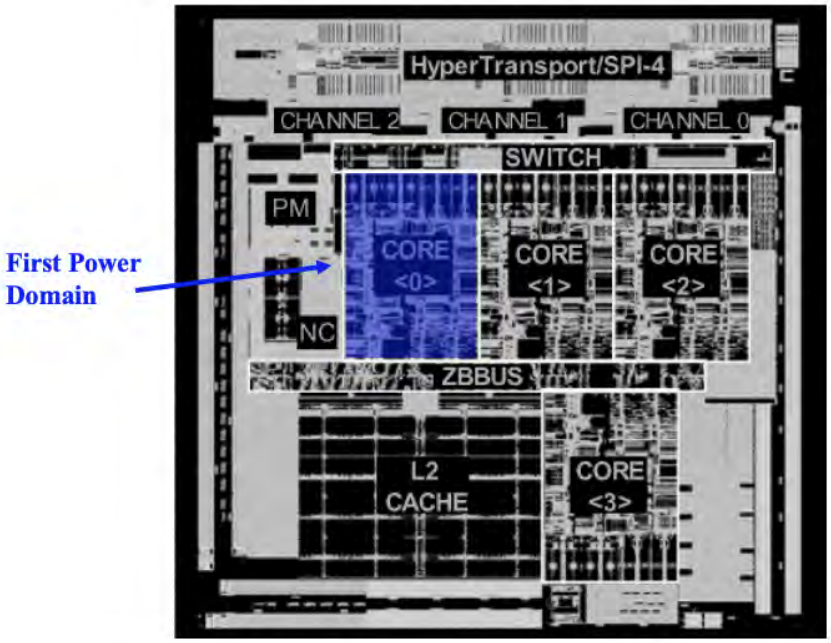
> On the BCM1280, Metal-6 and metal-7 are extensively used in distributing power and ground across the chip. Ground (GND) and power (VDD_chip, VDD_switch) lines are routed alternately on Metal-6 in the vertical direction and Metal-7 in the horizontal direction. This forms the power grid structure at the chip top level. The power and ground lines in the local sections are grided on Metal-2 through Metal-5, on which the local power grids are formed at the block level. . . . At the final stage of the layout design, an in-house automated procedure is applied, connecting local logic to the top-level power grid, to implement a complete full-chip power distribution network.

Id., 493.

B. Claim 12[a]: "a first partial local power mesh having its position corresponding to the position of a first power domain and coupling to the first power domain;"

151. Li discloses or at least renders obvious this limitation. Li explains, "In this quad-core microprocessor, four CPU cores are identical and each sits in a

separate triple-well region. Each single core, isolated from the others by a triple-well, forms a separate processor region. Therefore, under the full-chip context, each core is now built in a unique voltage region." EX1005, 491; *see also id.*, 493 ("[T]here are multiple voltage regions across the chip."). A POSITA would understand that each of the processor cores is a power domain, such that any one of them could be the first power domain. I will use Core <0> as a representative first power domain, but any of the cores could be the first power domain.



Id., Fig. 1 (annotated).

152. As I quoted above, Li teaches that the BCM1280 has a plurality of "local power grids" in the "local sections" on metal layers 2-5. EX1005, 493. Li explains that "[t]he power and ground lines in the local sections are grided on Metal-2 through Metal-5, on which the local power grids are formed at the block level."

Id. A POSITA would understand that Li's "grids" are "meshes" because just like the claimed "meshes," Li's "grids" are web-like structures comprised of horizontal and vertical power wires. EX1001, 3:44-56. Li describes its global grid as follows: "Ground (GND) and power (VDD chip, VDD switch) lines are routed alternately on Metal-6 in the vertical direction and Metal-7 in the horizontal direction. This forms the power grid structure at the chip top level."). EX1005, 493, Fig. 3. Li describes its local power grids in the same manner, stating that "power and ground lines in the local sections are grided on Metal-2 through Metal-5, on which the local power grids are formed at the block level." *Id.* A POSITA would thus understand that Li's local power grids, just like the global grids, consist of horizontal and vertical wires on at least two metal layers. Thus, a POSITA would understand that Li's local "grids" are "local power meshes," however that term might be construed.

153. Forming local power grids "at the block level" means that they are formed to correspond to the underlying circuitry that they will supply, such that they cover only a portion of the area of the BCM1280 chip. *See* EX1005, 493 ("The local power grids are left floating until final assembly at the full-chip level. At the final stage of the layout design, an in-house automated procedure is applied, connecting local logic to the top-level power grid, to implement a complete full-chip power distribution network."). Thus, these local grids are partial local power meshes in that, like the partial local power meshes of the '218 Patent, they do not cover the full

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area of the chip. Additionally, as Li describes a plurality of local power grids on the same four metal layers, a POSITA would understand that those local power grids are necessarily partial in that they cannot cover the entire chip without running into each other. A POSITA would therefore understand that Li's local power grids sit above the circuitry of their respective domains and provide power vertically downward into the circuitry.

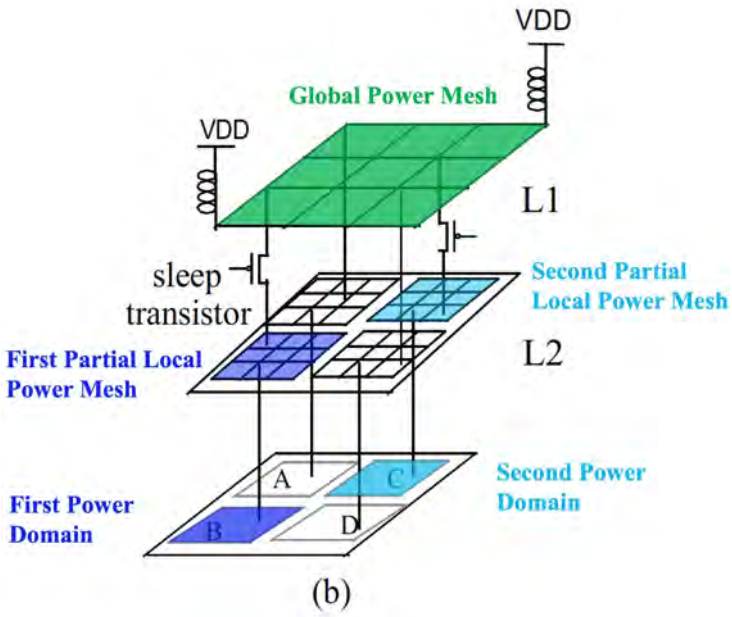
154. Additionally, in my opinion, it would have been obvious for each of Li's local power grids to be a partial local power mesh having its position correspond to the position of its respective power domain. Just like a global power grid must be above a local grid to supply power to the local grid, a local grid must be above its power domain to supply power to that domain. That is because power is supplied from a global grid to a local grid and from a local grid to a power domain vertically in an integrated circuit using vertical metal traces called "vias." *E.g.*, EX1006, 2:55-61 ("Generally, each of the voltage supply grids (positive and negative) in an integrated circuit are associated with the upper-most metal layers, are arranged in a grid (as further discussed below) and are coupled to cells and/or power-ground rails (associated with the middle or lower layers of the integrated circuit) using a piece of metal called a via stack.").

155. A POSITA would also know that a local power grid should be designed to correspond to the position of its power domains to be able to provide power to the

power domains. Indeed, it was known to a POSITA that local grids covering the same surface area as the domains to which they supply power were preferable. A local grid covering more area than its underlying power domain is a waste of local grid resources and takes up valuable chip area that could be used for neighboring local grids or other purposes. For these reasons, a POSITA knew to keep the area of partial local power meshes coincident with that of their underlying power domains. EX1006, 9:14-18 ("Although the power-ground rails are illustrated as spanning the entire portion 800 of the second voltage domain 104, it is recognized that the power-ground rails are only necessary to the extent cells requiring this voltage for operation are placed in these regions."); EX1016, 5:14-18 ("[T]he global routing grid can be partitioned into a plurality of areas, above and around the domains, so as to create one or a plurality of local routing grids, each above a respective supply domain and preferably having substantially the same surface area as the respective domain."). Having Li's local power grids be partial local power meshes with positions corresponding to the position of their respective power domains would have simply been combining prior art elements according to known methods to yield predictable results.

156. Confirming the preference for partial local power meshes to match the surface area of their underlying power domains, Jiang discloses a power routing

design for a chip with multiple power domains where each local grid corresponds to the position of (*i.e.*, covers the same surface area as) its power domain.

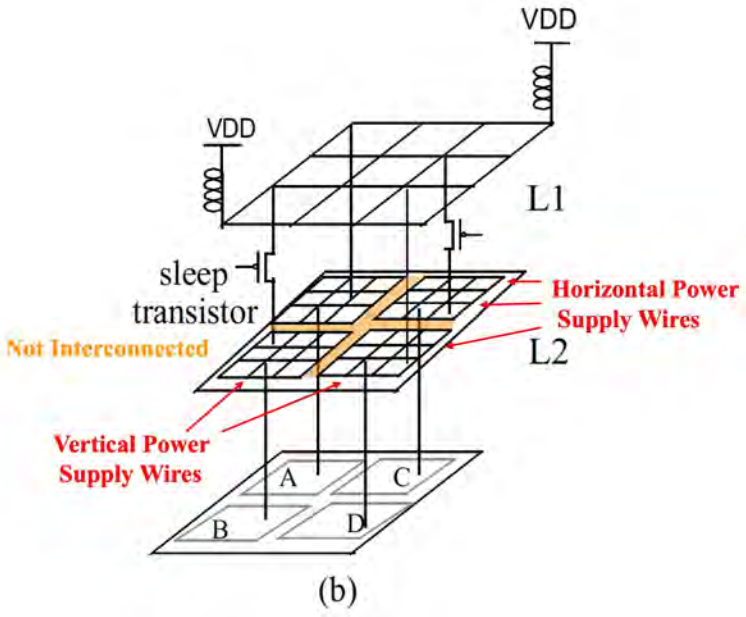


EX1004, Fig. 1(b) (annotated). To the extent Li does not already disclose this, it would have been obvious for each of Li's local grids to similarly have its position correspond to the position of its respective power domain. Indeed, a POSITA would have understood that doing so would be preferable in terms of efficient use of chip surface area and mesh resources and would be necessary to supply the power to the power domains in Li's circuit.

157. As I explained above, in my opinion, Li discloses that its local grids are partial local power meshes. Nevertheless, I have been asked to opine on whether it would have been obvious for Li's local power grids to be implemented as partial local power meshes if Li did not disclose that. In my opinion, even if Li had not

disclosed that its local grids were partial local power meshes, it would have been obvious to make them partial. Li's global power grid is a web-like structure of horizontal and vertical power supply wires. EX1005, Fig. 3, 493. It would have been obvious for Li's local power grids to similarly be web-like structures of horizontal and vertical wires to the extent Li's use of the term "grid" does not already convey that to a POSITA. Indeed, it is my opinion that a POSITA would have known that a power grid is typically "a meshing of horizontal and vertical metal rails on two metallization layers." EX1016, 8:57-59; *see also* EX1019, 4:57-64 ("FIG. 2 illustrates circuit cell 210, which includes various circuit elements served via a local power grid. Interconnections between circuit elements within circuit cell 210 are made using, for example, metal 3 (M3) layer 220 and metal 4 (M4) layer 215. The metal 5 (M5) layer 225 is, in this example, part of a global power grid interconnecting circuit cell 210 with other circuit cells (not illustrated)."), Fig. 2 (showing vertical wires (220) on M3 and horizontal wires (215) on M4).

158. Additionally, a POSITA would have known that in a power routing structure with a plurality of local grids, the local grids would not be interconnected. For example, Jiang discloses a power routing structure with a plurality of local power grids that are not interconnected, as can be seen in Jiang's Figure 1(b) below.



EX1004, Fig. 1(b) (annotated). This isolation of partial local power meshes allows Jiang to switch off sleep transistors and thereby remove power from the partial local power mesh and the underlying power domain to save power. EX1004, 1-2; *see also* EX1007, 1 ("Power-gating is a technique for efficiently reducing leakage power by shutting off the idle blocks."). Interconnections of Jiang's partial local power meshes would completely thwart this operation by permitting power to bypass the sleep transistor and power the underlying power domain of a partial local power mesh. A POSITA would have found it obvious for Li's local power grids similarly to be disconnected from one another to permit power gating to function, which was a primary point of the BCM1280 in Li. EX1005, 493 (noting Li's "power-saving capability" as a result of its "multiple voltage region[]" design). Also, it makes no difference that the power-gating in Li was performed on the ground side, EX1005,

493-94, Fig. 4, because ground was conveyed through Li's global and local power grids, thus requiring its isolation on a local grid basis for power gating to function. *Id.*, 495 ("The different internal ground net for each core is separated from chip ground by an NMOS switch.").

159. Because the local power grids cannot be interconnected, it would have been obvious for them to be "partial" local power meshes. As I explained above, a POSITA knew that there was no reason to extend a partial local power mesh beyond its underlying power domain. EX1006, 9:14-18 ("Although the power-ground rails are illustrated as spanning the entire portion 800 of the second voltage domain 104, it is recognized that the power-ground rails are only necessary to the extent cells requiring this voltage for operation are placed in these regions."); EX1016, 5:14-18 ("[T]he global routing grid can be partitioned into a plurality of areas, above and around the domains, so as to create one or a plurality of local routing grids, each above a respective supply domain and preferably having substantially the same surface area as the respective domain."). Extending a partial local power mesh beyond the bounds of its underlying power domain wastes power mesh resources and chip surface area, which could be used for other purposes as I explained above. Thus, a POSITA would have been motivated to minimize the extension of partial local power meshes into areas they were not needed and thus to make the local power meshes "partial." That is why Li refers to the formation of local grids "at the block

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level," which a POSITA would understand means that local grids are formed to correspond to their respective circuit blocks. If Li had not said that, it still would have been obvious to limit the partial local power mesh to the underlying power domains for all the reasons I just explained. For at least these reasons, a POSITA would understand that Li's local power grids meet the claimed "partial local power mesh" or that the combination renders them obvious. EX1001, 3:44-51; EX1004, Fig. 1(b).

C. Claim 12[b]: "a second partial local power mesh having its position corresponding to the position of a second power domain and coupling to the second power domain; and"

160. Li discloses, or at least renders obvious this limitation. Li discloses a "switch" in a separate power domain from the cores and receiving power from a separate voltage supply "VDD_switch" from the power received by Jiang's cores. EX1005, 495.

161. A POSITA would understand that Li's "switch" forms or is at least part of a second power domain, as illustrated below. The second power domain powered by VDD_switch is separate from the first power domain of Core <0>, which is powered by VDD_chip.

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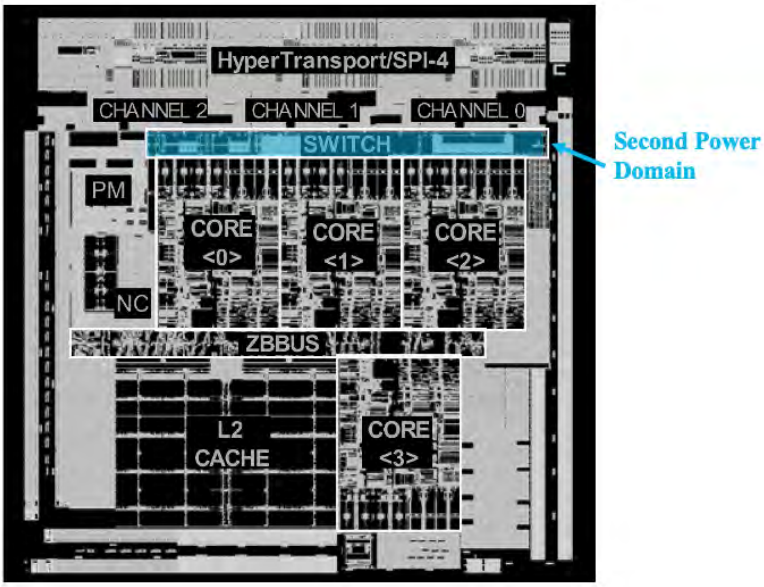

EX1005, Fig. 1 (annotated).

162. As I explained above regarding Li and limitation 12[a], Li teaches a plurality of partial local power meshes (Li's "local power grids") on metal layers 2-5. EX1005, 493. It also would have been obvious for Li's second power domain to have a partial local power mesh corresponding to its position for the same reasons discussed above regarding Li and limitation 12[a]. *See* Section XI.B.

163. Alternatively, a POSITA would understand that all of Li's components that receive VDD_switch could be in the same power domain and constitute the second power domain, and it would have been obvious to have a corresponding partial local power mesh for this power domain as well for the same reasons discussed above regarding Li and 12[a]. *See* Section XI.B.

D. Claim 12[c]: "a global power mesh, coupling to the first local power mesh and the second local power mesh, to provide the power needed by the first power domain and the second domain separately;"

164. Li discloses this limitation. Li discloses a "top-level power grid" on metal layers 6-7 for "distributing power and ground across the chip," which constitutes a global power mesh. EX1005, 493. In particular, Li teaches that:

> On the BCM1280, Metal-6 and metal-7 [sic] are extensively used in distributing power and ground across the chip. Ground (GND) and power (VDD_chip, VDD_switch) lines are routed alternately on Metal-6 in the vertical direction and Metal-7 in the horizontal direction. This forms the power grid structure at the chip top level. … The local power grids are left floating until final assembly at the full-chip level. At the final stage of the layout design, an in-house automated procedure is applied, connecting local logic to the top-level power grid, to implement a complete full-chip power distribution network.

Id. Li's final sentence in the quoted passage describing connecting local logic to the top-level power grid necessarily also includes connecting the local power grids to the top-level power grid and the local logic. Otherwise, it would remain "floating." Thus, Li describes coupling the first partial local power mesh and the second partial local power mesh to the global power mesh to provide the power needed by the first power domain and the second power domain.

165. As I explained above, Li's first power domain (Core <0>) and second power domain (switch) receive power from separate power supplies (VDD_chip and

VDD_switch, respectively) and thus are necessarily supplied separately. EX1005, 495.

E. Claim 12[d]: "wherein the first partial local power mesh and the second partial local power mesh are positioned on the same metal layer while the global power mesh and the first local power mesh are positioned on different metal layers;"

166. This limitation is disclosed in Li, or at least rendered obvious by Li in view of Jiang. Li discloses that the "local power grids" are on the same metal layers ("Metal-2 through 5"), while the "top-level power grid" is on different metal layers ("Metal-6 and [M]etal-7"). EX1005, 493. Li's local power grids necessarily overlap in metal layers because there are multiple local power grids, each requiring two metal layers, and only four metal layers for all local power grids. To the extent overlap is not inherent between the first and second partial local power meshes in Li, a POSITA would have understood Li to disclose overlap in local power grids' use of metal layers suggesting that this was an efficient way to use chip surface area.

167. Alternatively, it would have been obvious for a POSITA to place Li's local power grids on the same two metal layers because doing so permits Li's local power grids to be housed on just two metal layers, providing a more efficient use of metal layers in the integrated circuit by making two of Li's four metal layers used for local grids available for other uses or potentially eliminated from the design altogether and saving manufacturing cost through optimization of the amount of metallization used for power routing. A POSITA knew it was possible to place

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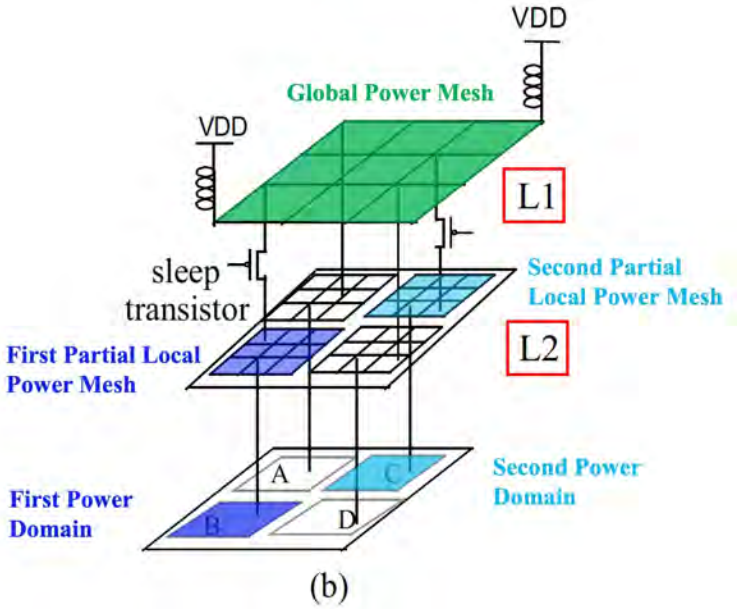
different partial local power meshes on the same metal layers. For example, Jiang discloses that its partial local power meshes are on the same layers ("L2"), while its global power mesh is on different layers ("L1") as illustrated below.



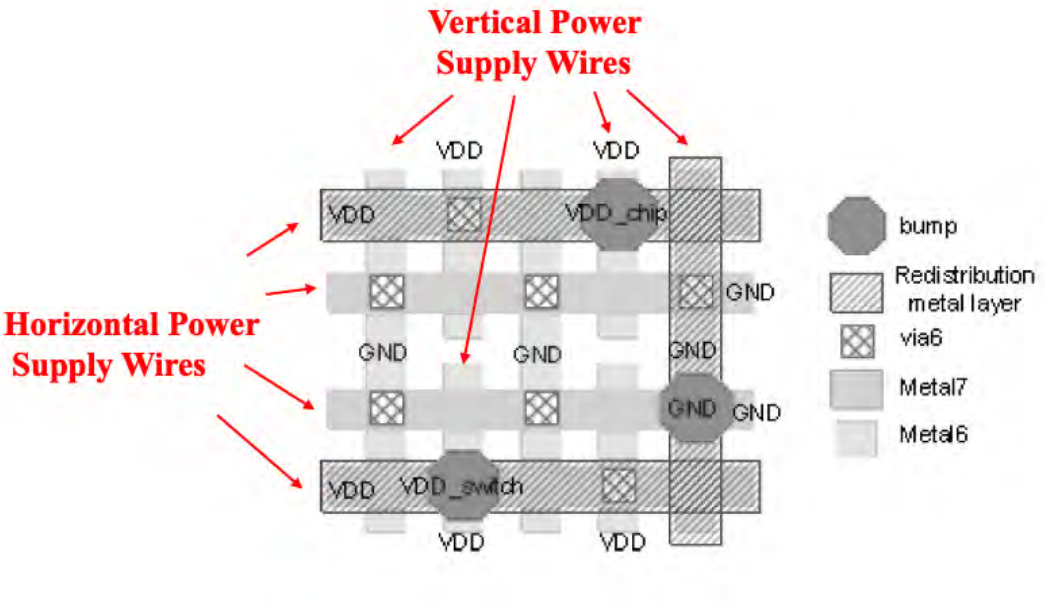
EX1004, Fig. 1(b) (annotated). Positioning Li's partial local power meshes on the same layers would have constituted combining prior art elements according to known methods to yield predictable results and would constitute a simple substitution of one known element (local grids on different metal layers) for another (local grids on the same metal layers) to obtain predictable results.

168. Additionally, it is my opinion that using the same metal layers for Li's partial local power meshes would have been obvious because it was simply the use of a known technique (local grids on the same metal layers) to improve similar devices (multiple power domain integrated circuit power distribution systems) in the

same way. It also would have constituted application of a known technique (local grids on the same metal layers) to a known device (multiple power domain integrated circuits) ready for improvement to yield predictable results.

F. Claim 12[e]: "wherein the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer; and"

169. Li discloses this limitation. Li discloses with respect to the "top-level power grid," which is a global power mesh, "Ground (GND) and power (VDD_chip, VDD_switch) lines are routed alternately on Metal-6 in the vertical direction and Metal-7 in the horizontal direction." EX1005, 493. This arrangement of horizontal and vertical power supply wires can be seen in Li's Figure 3, below.



EX1005, Fig. 3 (annotated).

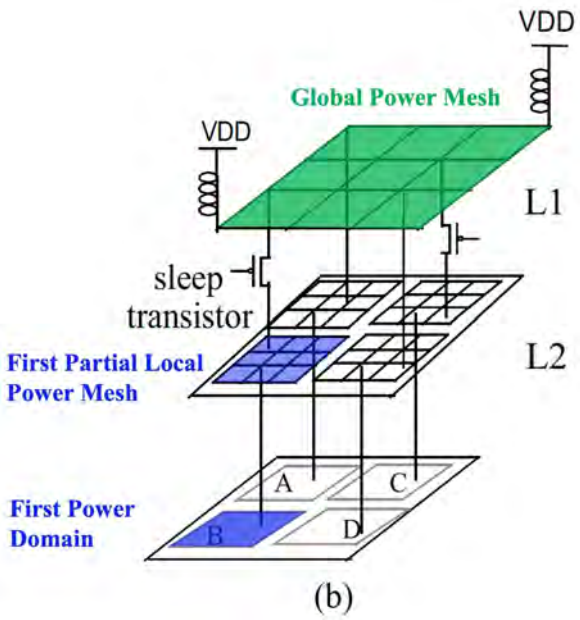
G. Claim 12[f]: "wherein the first metal layer and the second metal layer are different layers."

170. Li discloses that its first and second metal layers are different layers, "Metal-7" and "Metal-6." EX1005, 493-94.

H. Claim 13: "The power routing structure according to claim 12, wherein the global power mesh is positioned above the first local power mesh."

171. This limitation is disclosed in Li and rendered obvious by Li in view of Jiang. Li discloses that its global power mesh routes power all over the chip. EX1005, 493. Li further explains, "On the BCM1280, Metal-6 and metal-7 are extensively used in distributing power and ground across the chip. Ground (GND) and power (VDD_chip, VDD_switch) lines are routed alternately on Metal-6 in the vertical direction and Metal-7 in the horizontal direction. This forms the power grid structure at the chip top level." *Id*. A POSITA would understand, therefore, that Li's global power mesh is above each of Li's local power grids (the partial local power meshes) on the chip, which are "grided on Metal-2 through Metal-5." *Id*.; *see also* Sections XI.B-D.

172. Additionally, this limitation would have been obvious over Li in view of Jiang. Jiang discloses that its global power mesh is positioned above its first partial local power mesh, as shown in Figure 1(b), below.



EX1004, Fig. 1(b) (annotated).

173. It would have been obvious for Li's global power mesh to be arranged in the same manner as that is a simple and straightforward way for its global power mesh to provide power to the partial local power meshes as Li expressly discloses. Indeed, positioning Li's global power mesh above its partial local power meshes would have been a routine application of a known feature with a reasonable expectation of success. EX1018, 2:60-3:3 (discussing power grids formed above the circuit blocks they supply). Li's description of its global power mesh as being at the "chip top level," EX1005, 493, if not an express description of this limitation, is at least an express motivation to use the known arrangement of Jiang.

174. Implementing Jiang's arrangement in Li would have simply involved combining prior art elements according to known methods to yield predictable

results and would have constituted simple substitution of one known element (global power mesh positioned above local power mesh) for another to obtain predictable results. Similarly, such substitution (to the extent any substitution is involved) would have simply been the use of a known technique (global power mesh positioned above local power mesh) to a known device (Li's BCM1280) ready for improvement to yield a predictable result. A person of ordinary skill in the art would have been motivated to place the global power mesh on the chip top level to simplify routing power into the chip from external power connections and based on Li's express statement that the global power mesh is at "chip top level." EX1005, 493.

I. Claim 14: "The power routing structure according to claim 13, wherein the first local power mesh and the second local power mesh are not electrically coupled."

175. Li discloses this limitation. Li discloses that "the individual cores are electrically isolated from one another as well as the rest of the chip." EX1005, 494. Accordingly, a POSITA would understand that the first partial local power mesh (for first power domain Core<0>) is not electrically coupled to the second partial local power mesh (for second power domain switch). If the partial local power meshes for each core or the switch were interconnected, the cores could not be described as "electrically isolated from one another as well as the rest of the chip" as Li describes them. *Id*. Indeed, as these two power domains receive power from separate voltage sources (VDD_chip and VDD_switch), they are not electrically coupled. EX1005,

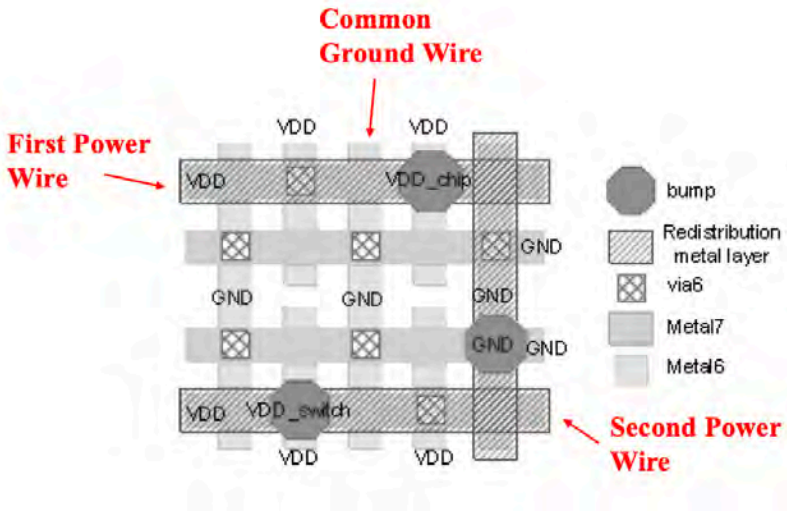
491 ("[E]ach core is now built in a unique voltage region. In addition to the complexity of the multiple ground domains, the chip is divided into two logic voltage regions …."); *see also id*., 493 (same), 494 (Fig. 3) (showing no connection between VDD_chip and VDD_switch).

J. Claim 15: "The power routing structure according to claim 12, wherein the global power mesh comprises: at least one ground wire; at least one first power wire that provides the power needed by the first power domain; and at least one second power wire that provides the power needed by the second power domain."

176. Li discloses a plurality of power and ground wires in its global power mesh ("Ground (GND) and power (VDD_chip, VDD_switch) lines"). EX1005, 493. Figure 3 below shows at least 3 ground wires on Metal 6 and at least two ground wires on Metal 7, satisfying the "at least one ground wire" requirement. Any or all of the ground wires in the global power mesh including others not shown in Figure 3 in Metal 6 and Metal 7 could be the "at least one ground wire."

177. Figure 3 also shows multiple VDD_chip and VDD_switch power wires in the global power mesh on Metal 6 and Metal 7. Both the VDD_chip and VDD_switch wires are "power wire[s]." Li discloses that the global grid including Metal 6 and Metal 7 "forms the power grid structure at the chip top level." EX1005, 493. Li also discloses that the "local logic [is connected] to the top-level power grid, to implement a complete full-chip power distribution network." *Id.* As I explained above, the local logic connects to the top-level power grid (global power mesh)

through the partial local power meshes, and Li expressly discloses that the local logic (power domains) are powered by the power wires in the top-level power grid (global power mesh). Thus, Li discloses that at least one VDD_chip power wire provides the power needed by the first power domain, and at least one VDD_switch power wire provides the power needed by the second power domain. The required at least one first and second power wires could be any VDD_chip and VDD_switch power wire, respectively, in Metal 6 or Metal 7 including all of them.



EX1005, Fig. 3 (annotated); *see also id.*, 495 ("VDD_chip provides power for all the internal logic except the node controller, packet manager, switch and HT/SPI-4 ports. … VDD_switch provides power for all the internal logic of the node controller (NC), packet manager (PM), switch and HT/SPI-4 ports.").

K. Claim 16: "The power routing structure according to claim 15, wherein the first partial local power mesh comprises: at least one first local ground wire that couples to the ground wire of the global power mesh; and at least one third power wire that couples to the first power wire and the first power domain."

178. Li discloses this limitation. Li discloses that the local power grids (partial local power meshes) include "power and ground lines." EX1005, 493. Li also states:

> The power and ground lines in the local sections are grided on Metal-2 through Metal-5, on which the local power grids are formed at the block level. The local power grids are left floating until final assembly at the full-chip level. At the final stage of the layout design, an in-house automated procedure is applied, connecting local logic to the top-level power grid, to implement a complete full-chip power distribution network.

Id. Thus, Li explains that the global power grid connects to the local logic (power domains) through the local power grids. Because a POSITA understood that power grids are made up of grids of power wires, a POSITA would understand that Li expressly discloses at least one first local ground wire (and potentially many) in the first partial local power mesh is coupled to at least one ground wire (and potentially many) of the global power mesh satisfying this limitation. Li also expressly discloses at least one third power wire (and potentially many) in the first partial local power mesh that couples to at least one first power wire (and potentially many) of the global power mesh (supplying VDD_chip) and the first power domain (Core

<0>). *Id*. Because the "at least one third power wire" can be all the power wires in the local grid, this limitation is necessarily satisfied by Li's local power grid, which is coupled to both the top-level global grid and the underlying power domain.

179. Alternatively, a POSITA would understand that Li's disclosure necessarily requires, or at least renders obvious, that one of the local ground wires (ground lines) in the local power grid is coupled to at least one ground wire in the top-level power grid, and that one of the local power wires (power lines) in the local power grid is coupled to at least one power wire in the top-level power grid. Indeed, a POSITA would know that such connections would be necessary "to implement a complete full-chip power distribution network" as disclosed by Li. EX1005, 493. Without such connections, a POSITA would understand that power would not flow, and the chip would be non-functional. Additionally, it would have been obvious to couple local ground and power wires to global ground and power wires, respectively, as Li expressly teaches. Li discloses that the "local power grids are left floating until final assembly at the full-chip level," when Li discloses "an in-house automated procedure is applied, connecting local logic to the top-level power grid, to implement a complete full-chip power distribution network." EX1005, 493. If the local power grids were not coupled to the top-level power grid, they would still be floating and useless contrary to Li's disclosure.

L. Claim 17: "The power routing structure according to claim 16, wherein the second partial local power mesh comprises: at least one second local ground wire that couples to the ground wire of the global power mesh; and at least one fourth power wire that couples to the second power wire and the second power domain."

180. Li discloses or renders obvious this limitation with respect to the second power domain (switch) and VDD_switch and the second local ground wire and at least one fourth power wire for the same reasons discussed above regarding claim 16. *See* Section XI.K.

M. Claim 18: "The power routing structure according to claim 17, wherein the first local ground wire and the second local ground wire share the same ground wire of the global power mesh."

181. Li discloses or renders obvious this limitation. Li discloses that it has a "common" "ground reference GND." EX1005, 495. Accordingly, a POSITA would understand that the first and second partial local power meshes, and any or all of their local ground wires, would be connected to the common ground wires of the global power mesh and thus would all "share the same ground wire of the global power mesh" as long as they are powered up (*i.e.*, not switched off).

XII. GROUND 5 – CLAIMS 1-11 AND 19-20 ARE OBVIOUS OVER LI IN VIEW OF JIANG AND IN FURTHER VIEW OF BERTOLET OR THE LOW POWER METHODOLOGY MANUAL

A. Claim 1

182. As I previously explained, claim 1 differs from claim 12 in that claim 1 describes a power routing arrangement method for creating a power routing structure

that would be met by the routing structure in claim 12 using an automatic placement and routing (APR) tool. *See* Section X.A.

183. Claim 1's first and second power domain, first and second partial local power meshes, and global power mesh are disclosed and/or rendered obvious for the reasons discussed above regarding limitations 12[preamble], 12[a]-[c], 12[e]-[f]. *See* Sections XI.A-D, XI.F-G.

184. Regarding claim 1's "power routing arrangement method," to the extent the preamble is limiting, Li describes "an in-house automated procedure" that is used "[a]t the final stage of the layout design" to "connect[] local logic to the top-level power grid[] to implement a complete full-chip power distribution network." EX1005, 493. Li's "in-house automated procedure" for performing layout design is an APR tool. Further, it is my opinion that a POSITA would understand that the act of using a particular arrangement or structure for power routing is a power routing arrangement method satisfying the preamble.

185. A POSITA designing an integrated circuit understands that power needs to be supplied for the chip to function and that power has to be routed on the chip for that power to be supplied to the logic circuits. A POSITA designing a chip also understands that some routing structure has to be selected to provide the needed routing. Thus, Li's teaching about a specific routing structure informs a POSITA that Li's routing structure could be selected for use in a new chip design such that it

would have been obvious to a POSITA to perform a power routing arrangement method with Li's routing structure—*i.e.*, to select Li's routing structure for use in a design. Both LPMM and Bertolet confirm that the need to route power in a chip design was known to a POSITA. EX1012, 177 ("With a physical topology in place we can now begin to consider how to provide power to the various voltage areas in the design."); EX1013, 126 ("After custom macrocell placement, a power distribution network is algorithmically generated using a custom SKILL program.").

186. Additionally, a POSITA would have found it obvious to form and couple Li's power meshes as discussed above with an automatic placement and routing (APR) tool. I discussed Li's power meshes in detail in Section XI regarding claims 12-18. As I explained above, Li itself teaches using an "in-house automated procedure" at "the final stage of the layout design" to couple its power grids and "implement a complete full-chip power distribution network." EX1005, 493. It is my opinion that a POSITA would find it obvious that a similar automated procedure could be used to form Li's grids, including its global and partial local power meshes, in the first place.

187. As I explained in Section X.A, both Bertolet and LPMM teach the use of APR tools to generate power distribution networks, and LPMM specifically recommends their use in applications like Li with multiple voltage supplies, multiple power domains, and even varying voltage levels within a voltage supply.

Accordingly, a POSITA would find it obvious to use an APR tool in order to form and couple Li's local and global power meshes based on LPMM and/or Bertolet for the same reasons discussed above. *See* Section X.A. Li's use of its own tool provides a reasonable expectation of success in doing so as does LPMM's teaching that a design is likely to "sub-optimal" without it. EX1012, 177.

B. Claim 2: "The arrangement method according to claim 1, wherein the first partial local power mesh and the second partial local power mesh are positioned on the same metal layer."

188. This limitation is disclosed or rendered obvious for the reasons I discussed regarding limitation 12[d]. *See* Section XI.E.

C. Claim 3: "The arrangement method according to claim 2, wherein the global power mesh and the first local power mesh are positioned on different metal layers."

189. This limitation is disclosed or rendered obvious for the reasons I discussed regarding limitation 12[d]. *See* Section XI.E.

D. Claim 4: "The arrangement method according to claim 3, wherein the global power mesh is positioned above the first local power mesh."

190. This limitation is disclosed or rendered obvious for the reasons I discussed regarding claim 13. *See* Section XI.H.

E. Claim 5: "The arrangement method according to claim 2, wherein the first partial local power mesh and the second partial local power mesh are not electrically coupled."

191. This limitation is disclosed or rendered obvious for the reasons I discussed regarding claim 14. See Section XI.I.

F. Claim 6: "The arrangement method according to claim 1, wherein the global power mesh comprises at least one ground wire, at least one first power wire that provides power to the first power domain, and at least one second power wire that provides power to the second power domain."

192. This limitation is disclosed or rendered obvious for the reasons I discussed regarding claim 15. *See* Section XI.J.

G. Claim 7: "The arrangement method according to claim 6, wherein the first partial local power mesh comprises: at least one first local ground wire that couples to the ground wire of the global power mesh; and at least one third power wire that couples to the first power wire and the first power domain."

193. This limitation is disclosed or rendered obvious for the reasons I discussed regarding claim 16. *See* Section XI.K.

H. Claim 8: "The arrangement method according to claim 7, wherein the second partial local power mesh comprises: at least one second local ground wire that couples to the ground wire of the global power mesh; and at least one fourth power wire that couples to the second power wire and the second power domain."

194. This limitation is disclosed or rendered obvious for the reasons I discussed regarding claim 17. *See* Section XI.L.

I. Claim 9: "The arrangement method according to claim 8, wherein the first local ground wire and the second local ground wire share the same ground wire of the global power mesh."

195. This limitation is disclosed or rendered obvious for the reasons I discussed regarding claim 18. *See* Section XI.M.

J. Claim 10: "The arrangement method according to claim 1, wherein the positions of the first partial local power mesh and the second partial local power mesh correspond to the first power domain and the second power domain, respectively."

196. This limitation is disclosed or rendered obvious for the reasons I discussed regarding limitations 12[a]-12[b]. *See* Sections XI.B-C.

K. Claim 11: "The arrangement method according to claim 1, wherein the global power mesh is distributed evenly above the first local power mesh and the area of the second local power mesh."

197. Li discloses or renders obvious this limitation. Li explains, "On the BCM1280, Metal-6 and metal-7 are extensively used in distributing power and ground across the chip. Ground (GND) and power (VDD_chip, VDD_switch) lines are routed alternately on Metal-6 in the vertical direction and Metal-7 in the horizontal direction. This forms the power grid structure at the chip top level." EX1005, 493. To distribute power and ground "across the chip," Li's "top level" grid must extend "across the chip." Thus, Li's global power mesh is distributed across the chip. By contrast, "[t]he power and grounds lines in the local sections are grided on Metal-2 through Metal-5, on which the local power grids are formed at the

block level." *Id.* A POSITA would understand, therefore, that Li's global power mesh is above each of the local power grids on the chip, which are in Metal-2 through Metal-5. Li's global power mesh is distributed evenly because it has a regular pattern of ground and power wires occurring within the global power mesh as shown in Figure 3 from Li.

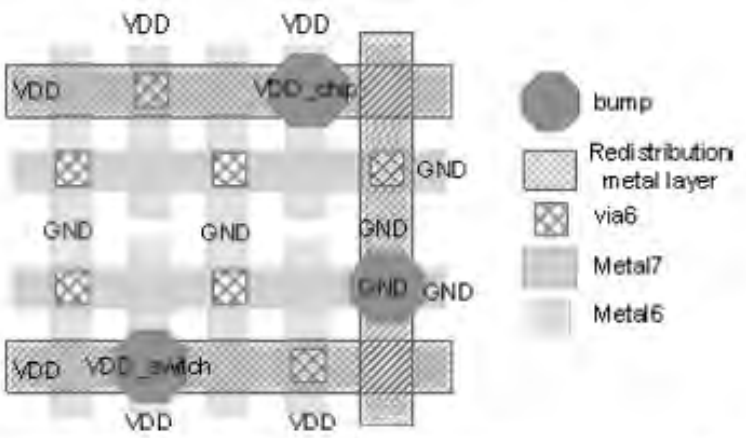
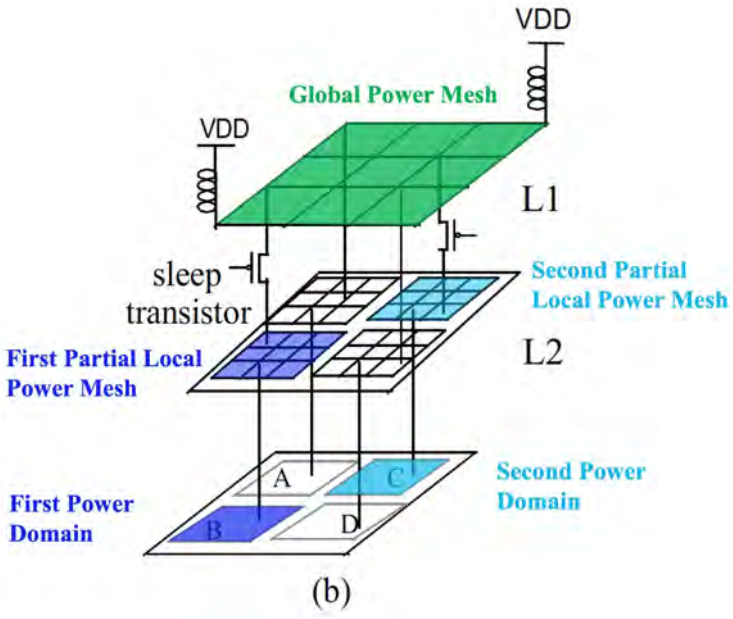


Fig. 3. Power and ground are distributed from the bumps onto the chip-level power grid through a redistribution metal layer.

Id., Fig. 3. Accordingly, a POSITA would understand that Li's global power mesh is distributed evenly above each partial local power mesh in the pattern shown in Figure 3.

198. Alternatively, a POSITA would have found this limitation obvious in view of Jiang. As shown in Figure 1(b), Jiang's global power mesh is distributed evenly above all partial local power meshes.



EX1004, Fig. 1(b) (annotated). Figure 10 also shows the even distribution in the power meshes.

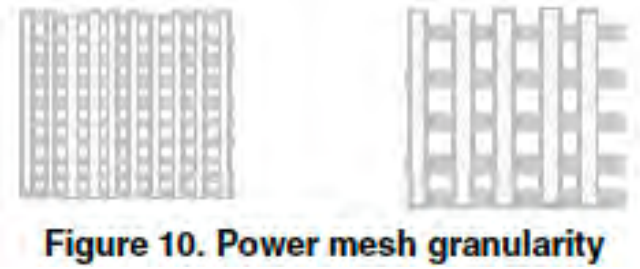


Figure 10. Power mesh granularity

Id., Fig. 10. It would have been obvious for Li's global power mesh to be arranged in the same manner for the reasons discussed regarding claim 13 and to simplify the design by providing a uniform pattern across the surface as shown in Jiang Figure 10. *See* Section XI.H.

L. Claim 19[preamble]: "A power routing arrangement method applied in an integrated circuit having multiple power domains, the arrangement method comprising:"

199. To the extent the preamble is limiting, it is obvious over Li for the same reasons I discussed regarding limitation 1[preamble]. *See* Section XII.A.

M. Claim 19[a]: "providing a global power mesh, positioned above a first power domain and a second power domain, comprising at least one first power wire that provides the voltage needed by the first power domain, at least one second power wire that provides the voltage needed by the second power domain, and at least one ground wire that provides the ground potential needed by the first power domain and the second power domain by an automatic placement and routing (APR) tool;"

200. The combination discloses or renders obvious the global power mesh as claimed for the reasons discussed regarding limitation 12[c] and claims 13 and 15. *See* Sections XI.D, XI.H, XI.J.

201. It would have been obvious to provide this global power mesh and all other features of the power routing structure of claim 19 with an APR tool for the reasons provided with respect to claim 1. *See* Section XII.A (citing Section X.A).

N. Claim 19[b]: "coupling the first power wire and the ground wire of the global power mesh to the first power domain by the APR tool; and"

202. The combination renders obvious that the first power wire and ground wire are coupled to the first domain for the reasons discussed regarding claims 16 and 18. *See* Sections XI.K, XI.M; *see also* Section XII.M (referencing claim 1's discussion of the obviousness of using an APR tool).

O. Claim 19[c]: "coupling the second power wire and the ground wire of the global power mesh to the second power domain by the APR tool;"

203. The combination renders obvious that the second power wire and ground wire are coupled to the second power domain for the reasons discussed regarding claims 16-18 and 19(b). *See* Sections XI.K, XI.L, XI.M; *see also* Section XII.M (referencing claim 1's discussion of the obviousness of using an APR tool).

P. Claim 19[d]: "wherein the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer; and"

204. The combination discloses or renders this limitation obvious for the same reasons discussed regarding limitation 12[e]. *See* Section XI.F.

Q. Claim 19[e]: "wherein the first metal layer and the second metal layer are different layers."

205. The combination discloses or renders this limitation obvious for the same reasons discussed regarding limitation 12[f]. *See* Section XI.G.

R. Claim 20: "The arrangement method according to claim 19, wherein the first power domain and the second power domain share the same ground wire of the global power mesh."

206. The combination discloses or renders this limitation obvious for the same reasons discussed regarding claim 18. *See* Section XI.M.

XIII. CONCLUSION

207. Based on the foregoing, it is my opinion that claims 1-20 of the '218 Patent are rendered obvious as discussed above.

208. In signing this Declaration, I recognize that the Declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be called upon to testify in deposition or before the Patent Trial and Appeal Board. If called upon to testify, I would testify truthfully and competently to all matters stated in this Declaration.

209. I reserve the right to supplement my opinions in the future to respond to any arguments that Patent Owner raises and to take into account new information as it becomes available to me.

210. I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true and that such statements are made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: May 8, 2023

Vivek Subramanian

Vivek Subramanian

APPENDIX A

Vivek Subramanian

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Austin, TX 78750, USA

Education

3 / 96 - 6 / 98 **Ph.D. in Electrical Engineering, Stanford University**
Stanford, California
Honors earned: Graduate Fellowship, Eastman Kodak Company

9 / 94 - 3 / 96 **MS in Electrical Engineering, Stanford University**
Stanford, California

8 / 90 - 5 / 94 **BS in Electrical Engineering, Louisiana State University**
Baton Rouge, Louisiana
Honors earned: Summa cum laude, College Honors, Outstanding Senior, Junior and Sophomore, Honors College

Professional Experience

2018 - present **École polytechnique fédérale de Lausanne**
Switzerland

8/18 – present: Professor of Microengineering

2000 - present **Department of Electrical Engineering & Computer Sciences, University of California**
Berkeley, CA

7/20 to date: Adjunct Professor
7/18 – 6/20: Chancellor's Professor
7/11 – 6/20: Professor
7/05 – 7/11: Associate Professor
7/00-7/05: Assistant Professor
Research, teaching and service in EECS Department
Honors Earned:
2015 IEEE Kiyo Tomiyasu Award
Best in session and best in track awards, 2013 IMAPS Microelectronics Conference
Outstanding paper award, 2012 IMAPS Microelectronics Conference
2008 Printed Electronics Champion, Printed Electronics USA Conference, November 2008
Outstanding Teaching Award, EECS Department, UC Berkeley, 2005
Best paper award, 2004 IEEE Device Research Conference
Nominated to MIT's Technology Review top 100 young innovators list (TR100), 2002
National Science Foundation Young Investigator (CAREER) Award, FY2002,
Nominated to National Academy of Engineering's *Frontiers of Engineering*, 2002
Winner of 2002 Paul Rappaport Award for best paper in an IEEE EDS Journal

2009 - present **Adjunct Professor, Sunchon National University**
Sunchon, Korea
2013 to date: Adjunct Professor, BK21 Program
2009-2013: Adjunct Professor and Principal Investigator, WCU Program
Initiated, managed, and contributed to large multinational research program focused on printed electronics, including displays, energy devices, and RFID

2000 - present **Independent Consultant**
Orinda, CA
Consultant to the semiconductor industry and its associated fields in the following areas:
Memory technology and design, Silicon Process Technology
Display / Imager and Flexible Electronics Technology, RFID Technology
Intellectual Property Consulting
Technology Evaluation / Venture Capital due diligence

2014- present

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Founder and CTO, Locix Inc.
San Bruno, CA
Senior leadership role in venture-funded startup company working on wireless networking

2004 – 2013 **Founding Scientific Advisor, Kovio, Inc.**
Sunnyvale, CA
Scientific advising to printed electronics startup company

2008 - 2011 **Chief Technical Advisor, QuSwami, Inc.**
San Francisco, CA
Scientific advising to energy conversion device startup company
Served as CTO from July 2010-June 2011

1998 - 2000 **Consulting Assistant Professor, Electrical Engineering Department, Stanford University.**
Stanford, CA
Advisory role for research group of Prof. Krishna C. Saraswat

1998-2000 **Visiting Research Engineer, Electrical Engineering Department, University of California.**
Berkeley, CA
Research into 25nm MOSFET technologies for giga-scale integration

1998 - 2000 **Founder, Matrix Semiconductor, Inc.**
Santa Clara, CA
Co-founder and technical advisor of startup company working on high-density memory technology
Honors Earned:
Nominated to Scientific American's SA50 List for Visionary Technology
Finalist for 2003 World Technology Award for Information Technology Hardware
Winner, 2005 EDN Innovation Award

1998 **Co-instructor, Electrical Engineering Department, Stanford University.**
Stanford, CA
Co-teaching of EE311, Advanced Integrated Circuit Fabrication Processes

1997 **Intern, Advanced Product Research and Development Laboratory, Motorola Inc.**
Austin, TX
Research into process development issues affecting SiGe SEMFET devices

1996 **Head Teaching Assistant EE410: IC Fabrication Laboratory, Stanford University**
Stanford, CA
Coordination and instruction of EE410, graduate level laboratory course.

1994-1998 **Research Assistant, Electrical Engineering, Stanford University**
Stanford, CA
Research into crystallization of amorphous Si and SiGe films using low thermal budget processes.

Professional Affiliations and Activities

Technical Program Committee, IEEE Electronic Components and Technology Conference, 2014 to 2016
Chair, Scientific Advisory Board, iPACK, Royal Institute of Technology (KTH), Sweden, 2011 to 2016
Tampere Institute of Technology Faculty Search Committee, Finland, 2013
University of Oulu Faculty Search Committee, Finland, 2013
Served as external thesis committee member for several universities world-wide, including University of Cape Town (South Africa), Tampere Institute of Technology (Finland), Technical University of Eindhoven (Netherlands), Indian Institute of Science (India), Indian Institute of Technology (India), 2009 to date
Associate Editor, IEEE Journal of Display Technology, 2008 to date
Technical Program Chair, Large Area, Organic, and Printed Electronics Conference, 2012-2013
Scientific Committee, Large Area, Organic, and Printed Electronics Conference, 2009-2011
Scientific Committee, International Conference on Printed and Flexible Elecronics, 2009-2013
IEEE Electron Devices Society Organic Electronics Committee, 2003 - 2005
Executive Committee, International Electron Device Meeting, 2003 to 2009
Technical Program Committee, International Electron Device Meeting, 2001-2002
Technical Program Committee member, Device Research Conference, 2000-2002
Technical Program Committee member, VLSI-TSA Conference, 2005
Member, Institute of Electrical and Electronic Engineers

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List of Patents, Publications and Presentations

Patents

1. "Systems and methods for using ranging to determine locations of wireless sensor nodes based on radio frequency communications between the nodes and various RF-enabled devices", T. Ylamurto, M. Seth, L. Kong, V. Subramanian, US Patent 10,551,479
2. "Systems and methods for providing communications within wireless sensor networks based on a periodic beacon signal", T. Ylamurto, V, Pavate, E. Alon, V. Subramanian, US Patent 10,536,901
3. "Systems and methods for using radio frequency signals and sensors to monitor environments", T. Bakhishev, V. Subramanian, V. Pavate T. Ylamurto, US Patent 10,514,704.
4. "Systems and methods for using radio frequency signals and sensors to monitor environments", T. Bakhishev, V. Subramanian, V. Pavate T. Ylamurto, US Patent 10,504,364
5. "Systems and methods for coarse and fine time of flight estimates for precise radio frequency localization in the presence of multiple communication paths", M. Seth, L. Kong, T. Ylamurto, V. Subramanian, US Patent 10,470,156
6. "Methods and apparatus for monitoring wound healing using impedance spectroscopy", M. Maharbiz, V. Subramanian, A. C. Arias, S. Swisher, A. Liao, M. Lin, F. Pavinatto, Y. Khan, D. Cohen, E. Leeflang, S. Roy, M. Harrison, D. Young, US Patent 10,463,293
7. "Systems and methods for using radio frequency signals and sensors to monitor environments", T. Bakhishev, V. Subramanian, V. Pavate T. Ylamurto, US Patent 10,156,852.
8. "Systems and methods for determining locations of wireless sensor nodes in a tree network architecture having mesh-based features", L. Kong, T. Bakhishev, T. Ylamurto, V. Subramanian, M. Seth, US Patent 10,104,508.
9. "Systems and methods for providing wireless asymmetric network architectures of wireless devices with power management features", V. Subramanian, E. Alon, V. Pavate, US Patent 10,028,220.
10. "Random delay generation for thin-film transistor based circuits", V Subramanian, M Mao, Z Wang, US Patent 9,985,664
11. "Systems and methods for determining locations of wireless sensor nodes in a network architecture having mesh-based features for localization", L. Kong, T. Bakhishev, T. Ylamurto, V. Subramanian, M. Seth, US Patent 9,846,220
12. "Systems and methods for determining locations of wireless sensor nodes in a tree network architecture having mesh-based features", L. Kong, T. Bakhishev, T. Ylamurto, V. Subramanian, M. Seth, US Patent 9,763,054
13. "Through silicon vias and thermocompression bonding using inkjet-printed nanoparticles", V. Subramanian and J. Sadie, US Patent 9,717,145
14. "Systems and methods for providing wireless asymmetric network architectures of wireless devices with anti-collision features", V. Subramanian, E. Alon, V. Pavate, US Patent 9,706,489
15. "Systems and methods for determining locations of wireless sensor nodes in an asymmetric network architecture", V. Subramanian, E. Alon, V. Pavate, US Patent 9,529,076
16. "Systems and methods for providing wireless sensor networks with an asymmetric network architecture", V. Subramanian, E. Alon, V. Pavate, US Patent 9,380,531
17. "Transparent metal oxide nanoparticle compositions, methods of manufacture thereof and articles comprising the same", V. Subramanian, S. K. Volkman, US Patent 9,343,202
18. "Three-dimensional nonvolatile memory and method of fabrication", M. G. Johnson, T. H. Lee, V. Subramanian, P. M. Farmwald, J. M. Cleeves, US Patent 9,214,243
19. "Dense arrays and charge storage devices", T. H. Lee, V. Subramanian, J. M. Cleeves, I. G. Kouznetsov, M. G. Johnson, P. M. Farmwald, US Patent 9,171,857
20. "Print compatible designs and layout schemes for printed electronics", Z. Wang, V. Subramanian, L. Cleveland, US Patent 9,155,202
21. "Wireless devices including printed integrated circuitry and methods for manufacturing and using the same", P. Smith, C. Choi, V. Pavate, J. M. Cleeves, V. Subramanian, R. Young, V. Biviano, US Patent 9,004,366.

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22. “Dense arrays and charge storage devices “, T. H. Lee, V. Subramanian, J. M. Cleeves, M. G. Johnson, P. M. Farmwald, I. Kouznetzov, US Patent, 8,981,457.
23. “High reliability surveillance and/or identification tag/devices and methods of making and using the same”, V. Subramanian, P. Smith, V. Pavate, A. Kamath, C. Choi, A. Chandra, J. M. Cleeves, US Patent, 8,933,806.
24. “Surveillance devices with multiple capacitors”, P. Smith, C. Choi, J. M. Cleeves, V. Subramanian, A. Kamath, S. Molesa, US Patent, 8,912,890.
25. “Pillar-shaped nonvolatile memory and method of fabrication”, M. G. Johnson, T. H. Lee, V. Subramanian, P. M. Farmwald, J. M. Cleeeves, US Patent 8,897,056
26. “Dense arrays and charge storage devices”, T. H. Lee, V. Subramanian, J. M. Cleeves, I. G. Kouznetsov, M. G. Johnson, P. M. Farmwald, US Patent 8,853,765
27. “Dense arrays and charge storage devices”, T. H. Lee, V. Subramanian, J. M. Cleeves, I. G. Kouznetsov, M. G. Johnson, P. M. Farmwald, US Patent 8,823,076
28. “Random delay generation for thin-film transistor based circuits”, V. Subramanian, M. Mao, Z. Wang, US Patent 8,810,298
29. “Vertically stacked field programmable nonvolatile memory and method of fabrication”, M. Johnson, T. Lee, V. Subramanian, M. Farmwald, and J. M. Cleeves, US Patent 8,503,215
30. “Process-variation tolerant series-connected NMOS and PMOS diodes, and standard cells, tags, and sensors containing the same”, V. Subramanian, P. Smith, US Patent 8,471,308
31. “Printed compatible designs and layout schemes for printed electronics”, Z. Wang, V. Subramanian, L. Cleveland, US Patent 8,383,952
32. “Method for making surveillance devices with multiple capacitors”, P. Smith, C. Choi, J. M. Cleeves, V. Subramanian, A. Kamath, S. Molesa, US Patent 8,296,943
33. “High reliability surveillance and/or identification tag/devices and methods of making and using the same”, V. Subramanian, P. Smith, V. Pavate, A. Kamath, C. Choi, A. Chandra, and J. M. Cleeves, US Patent 8,264,359
34. “High reliability surveillance and/or identification tag/devices and methods of making and using the same”, V. Subramanian, P. Smith, V. Pavate, A. Kamath, C. Choi, A. Chandra, and J. M. Cleeves, US Patent 8,227,320
35. “Vertically stacked field programmable nonvolatile memory and method of fabrication”, M. Johnson, T. Lee, V. Subramanian, M. Farmwald, and J. M. Cleeves, US Patent 8208282
36. “Reliable tag deactivation”,J. M. Cleeves, V. Subramanian, US Patent 8138921
37. “Combined static and dynamic frequency divider chains using thin film transistors”, V. Subramanian, US Patent 8085068
38. “Process-variation tolerant diode, standard cells including the same, tags and sensors containing the same, and methods for manufacturing the same”, V. Subramanian, P. Smith, US Patent 7932537
39. “Three terminal nonvolatile memory Device with vertical gated diode”, T. H. Lee, V. Subramanian, J. M. Cleeves, M. G. Johnson, P. M. Farmwald, I. G. Kouznetsov, US Patent 7825455
40. “Vertically stacked field programmable nonvolatile memory and method of fabrication”, V. Subramanian, J. M. Cleeves, US Patent 7816189
41. “Multi-mode tags and methods of making and using the same”, P. Smith, J. M. Cleeves, V. Pavate, V. Subramanian, US Patent 7750792
42. “Method of manufacturing complementary diodes”, V. Subramanian, P. Smith, US Patent 7528017
43. “Vertically stacked field programmable nonvolatile memory and method of fabrication”, V. Subramanian, J. M. Cleeves, US Patent 7319053
44. “Vertically stacked field programmable nonvolatile memory and method of fabrication”, V. Subramanian, J. M. Cleeves, US Patent 7265000
45. “Vertically stacked field programmable nonvolatile memory and method of fabrication”, V. Subramanian, J. M. Cleeves, US Patent 7160761
46. “Vertically stacked field programmable nonvolatile memory and method of fabrication”, V. Subramanian, J. M. Cleeves, US Patent 7157314

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47. “Dense arrays and charge storage devices”, T. H. Lee, V. Subramanian, J. M. Cleeves, A. J. Walker, C. Petti, I. Kouznetzov, M. G. Johnson, P. M. Farmwald. B. Herner, US Patent 7129538

48. “Patterning three dimensional structures”, C. K. Li, J. N. Knall, M. A. Vyvoda, J. M. Cleeves, V. Subramanian, US Patent 7071565

49. “Monolithic three dimensional array of charge storage devices containing a planarized layer”, T. H. Lee, V. Subramanian, J. M. Cleeves, A. J. Walker, C. J. Petti, I. G. Kouznetzov, M. G. Johnson, P. M. Farmwald, and B. Herner, US Patent 6881994

50. “Thermal processing for three dimensional circuits”, V. Subramanian, J. M. Cleeves, J. N. Knall, C. K. Li, and M. A. Vyvoda, US Patent 6,770,939

51. “Vertically stacked field programmable nonvolatile memory and method of fabrication”, M. G. Johnson, T. H. Lee, V. Subramanian, and P. M. Farmwald, US Patent 6780711

52. “Multigate semiconductor device with vertical channel current and method of fabrication”, J. M. Cleeves and V. Subramanian, US Patent 6677204

53. “Thermal processing for three dimensional circuits”, V. Subramanian, J. M. Cleeves, J. N. Knall, C. K. Li, and M. A. Vyvoda, US Patent 6624011

54. “Multigate semiconductor device with vertical channel current and method of fabrication”, J. M. Cleeves and V. Subramanian, US Patent 6580124

55. “Patterning three dimensional structures”, C. K. Li, J. N. Knall, M. A. Vyvoda, J. M. Cleeves, and V. Subramanian, US Patent 6627530

56. “Low cost three-dimensional memory array”, M. Johnson, T. Lee, V. Subramanian, P. Farmwald, J. Knall, US Patent 6515888

57. “Integrated circuit structure including three-dimensional memory array”, M. Johnson, T. Lee, V. Subramanian, P. M. Farmwald, J. M. Cleeves, US Patent 6385074.

58. “FINFET transistor structures having double gate channel extending vertically from a substrate and methods of manufacture”, C. Hu, T-J. King, V. Subramanian, L. Chang, X. Huang, Y-K. Choi, J. T. Kedzierski, N. Lindert, J. Bokor, W-C. Lee, US Patent 6413802

59. “Vertically stacked field programmable nonvolatile memory and method of fabrication”, M. Johnson, T. Lee, V. Subramanian, M. Farmwald, and J. M. Cleeves, US Patent 6185122.

60. “Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication”, M. Johnson, T. Lee, V. Subramanian, M. Farmwald, and J. M. Cleeves, US Patent 6034882.

61. “Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication”, M. Johnson, T. Lee, V. Subramanian, M. Farmwald, and J. M. Cleeves, US Patent 6351406.

62. “Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication”, M. Johnson, T. Lee, V. Subramanian, M. Farmwald, and J. M. Cleeves, US Patent 6483736.

Invited Magazine Articles, Books, Chapters, and Monographs

1. Chapter in “Inkjet Technology for Digital Fabrication”, Editors: Ian M. Hutchings, Graham D. Martin, Wiley, ISBN: 978-0470681985

2. Chapter in “Applications of Organic and Printed Electronics: A Technology-Enabled Revolution (Integrated Circuits and Systems), Editor: E. Cantatore, ISB: 978-1-461-43159-6

3. Chapter in “Inkjet-based Micromanufacturing”, Editors: Korvink, Smith, Shin, Wiley, ISBN: 978-3-527-31904-6

4. Chapter in “Organic Electronics II. More Materials and Applications", Editor: H. Klauk, Wiley, ISBN: 978-3-527-32647-1

5. Chapter in “Transparent Electronics: From Synthesis to Applications”, Editors: A. Facchetti and T. Marks, Wiley, ISBN: 978-0-470-99077-3, 2010.

6. Chapter in “The chemistry of inkjet inks”, Editor: S. Magdassi, World Scientific Publishing Company, ISBN: 978-9812818218, 2009

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7. Chapter in "Organic Field-Effect Transistors", Editors: Z. Bao, and J. Locklin, CRC Press, ISBN: 978-0849380808, 2007
8. "Developments in printed RFID", V. Subramanian, Pira Publishing, UK, 2006.
9. "3D Chips: Future Possibilities", V. Subramanian, Silicon India, Feb 2003, pp. 24-25

Invited Conference Presentations

1. ***Invited,*** "Materials, Process, and Device Innovations for High-Performance Printed Electronics", PRINSE'18 – The 5th Printed Intelligence Industry Seminar on Manufacturing Solutions for Customer Needs and Vision to the Future, Oulu, Finland, Jan 31-Feb 1, 2018.
2. ***Invited¸*** "Highly scaled gravure printed organic transistors for high-performance printed organic electronics", High-frequency printed and direct-written organic-hybrid integrated circuits (HEROIC) Workshop, Milan, Italy, Nov 8-10, 2017.
3. ***Keynote,*** "Printed Electronics: Innovations in Materials, Processes, and Devices", Association of International Metallizers, Coaters, and Laminators (AIMCAL) R2R Conference USA 2017, Tampa, FL, Oct-15-18, 2017.
4. ***Invited,*** "High-performance gravure printed organic transistors", 2017 European Materials Research Society Meeting, Strasbourg, France, May 22-26, 2017
5. ***Invited,*** "Printed Electronics: Innovations in Materials, Processes, and Devices", 2017 International Thin Film Transistor Conference (ITC 2017), Austin, TX, February 23-24, 2017.
6. ***Invited,*** "High-speed Printing of Transistors: From Inks to Devices", 2016 International Society of Coating Science and Technology Symposium (ISCST), Pittsburgh, PA, September 18-21, 2016.
7. ***Keynote***, "Printed Electronics: Innovations in Materials, Processes, and Devices", 2016 Canadian Printable Flexible Wearable electronics Symposium (CPES2016), April 19-20, Oakville, Canada
8. ***Keynote***, "Printed Electronics: Innovations in Materials, Processes, and Device", 2016 Society of Vacuum Coaters Techcon, Indianapolis, IN, May 10-13, 2016.
9. ***Invited***, Subramanian, Vivek, Chung, Seungjun, Grau, Gerd and Scheideler, William J., "71-2: Invited Paper: Printed Transistors and MEMS for Large-Area Electronics", 2016 Society for Information Display Symposium, San Francisco, May 20-27, 2016.
10. ***Keynote,*** "Printed Electronics: Innovations in Materials, Processes, and Devices", 31st Philippine Chemistry Congress, Iloilo, Philippines, April 13-15, 2016.
11. ***Keynote,*** "Advanced Processes, Materials, and Devices for Emerging Printed Electronics Applications", 3rd Swiss Conference on Printed Electronics and Functional Materials, Neuchatel, Switzerland, Oct 1-2, 2015.
12. ***Invited,*** "High-performance printed organic transistors: Materials, processes, and devices", V. Subramanian, G. Grau, H. Kang, and R. Kitsomboonloha, 2015 American Chemical Society National Meeting and Exposition, Boston, MA, Aug 17th, 2015.
13. ***Invited***, Subramanian, Vivek, Jaewon Jang, William Scheideler, and Sarah Swisher. "39.1: Invited Paper: Printed Inorganic Transistors Based on Transparent Oxides." In SID Symposium Digest of Technical Papers, vol. 46, no. 1, pp. 587-590. 2015.
14. ***Plenary,*** "Printed Electronics: Advanced Technologies Enabling New Applications", 2015 Flexible and Printed Electronics Conference, Monterey, CA, February 23-26, 2015.
15. ***Invited***, "High-resolution gravure printing of organic thin film transistors for high-performance printed electronic systems", V. Subramanian, R. Kitsomboonloha, J. Cen, H. Kang, G. Grau, and W. J. Scheideler, Materials Research Society Fall Meeting, Boston, MA, Dec 3, 2014.
16. ***Invited,*** "Advanced printed electronics technologies for novel ubiquitous human interactive systems", 2014 CMOS Emerging Technologies Research Symposium, Grenoble, France, July 6-8, 2014.
17. ***Invited,*** "Printed Electronics: A pathway to functionally-rich systems", 64th annual IEEE Electronic Components and Technology Conference, Orland, FL, May 27, 2014.
18. ***Invited***, "Printed Electronics: The Confluence of Printing and Semiconductors", Canadian Printed Electronics Symposium, Montreal, Canada, April 9, 2013.

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19. ***Invited "***Modeling, scaling, and integration of gravure printing for fast switching Organic FETs", V. Subramanian, S. J. S. Morris, H. Kang, Materials Research Society Fall 2012 Meeting, Boston, MA, Nov 25-30, 2012

20. ***Invited***, "Printed Nanoparticles as routes to high-performance printed conductors: Synthesis, Printing Processes, and Device Applications", V. Subramanian, H. Kang, R. Kitsomboonloha, and S. K. Volkman, The 2012 International Conference on Flexible and Printed Electronics ICFPE2012, Tokyo, Japan, September 6th - 8th, 2012

21. ***Invited*** "Advanced Printing Processes for High-Performance Printed Transistors", V. Subramanian, Flextech Workshop on Printing Electronics - Ink and Substrate Interactions, Kalamazoo, MI, August 1-2, 2012

22. ***Invited*** "High-performance Printed Transistors: Materials, Processes, and Devices", V. Subramanian, 2nd CPEM International Symposium "Organic Semiconductors and Printed Electronics", Gyeonggi, South Korea, May 10th, 2012.

23. ***Invited*** "Highly-Scaled Gravure and Inkjet Printed Organic Transistors: Tools, Processes, and Devices", Hongki Kang & Vivek Subramanian, 2012 Flextech Flexible Electronics and Display Conference, Phoenix, AZ, Feb 5-9, 2012.

24. ***Plenary*** "Nanomaterials for printed electronics: synthesis, design, and applications", V. Subramanian, International Conference on Nano Science and Nano Technology, Sunchon, Korea, November 11th, 2011.

25. ***Invited*** "Advances in scaling of printed transistors", V. Subramanian, International Seminar on Printed Electronics, Seoul, Korea, June 8th, 2011.

26. ***Invited*** "High-Performance Fully Printed Transistors: Materials, Processes, and Device Characteristics", V. Subramanian, H. Tseng, R. Kitsomboonloha, and A. de la Fuente Vornbrock, 2011 Electrochemical Society Meeting, Montreal, Canada, May 2011

27. ***Invited*** "From Droplets to Devices: Printed Transistor Processes, Integration, and Characteristics", Vivek Subramanian, Daniel Soltman, Huai-Yuan Tseng, Rungrot Kitsomboonloha and Alejandro de la Fuente Vornbrock, Materials Research Society Spring Meeting, San Francisco, CA, April 2011

28. ***Keynote*** "Printed electronics: Innovations in tools, materials, devices, and applications", V. Subramanian*,* 2011 Korea Printed Electronics Association (KoPeA) meeting, Seoul, Korea, March 2011

29. ***Keynote*** "Printed RF tags and sensors: the confluence of printing and semiconductors", V. Subramanian, F. Liao, and H-Y. Tseng, The European Microwave Integrated Circuits Conference 2010, Paris, France, September 2010.

30. ***Invited*** "Droplet-on-demand direct patterning of active materials: materials, modeling, and integration", V. Subramanian, The 2010 IEEE Lithography Workshop, Kuai, Hawaii, November 2010

31. ***Plenary*** "Printed electronics: where are we, and where are we going", V. Subramanian, 2010 Large Area Organic, and Printed Electronics Convention (LOPE-C), Frankfurt, Germany, June 2010.

32. ***Keynote*** "Printed RFID: Technology Trends and Outlook", V. Subramanian, IEEE International Conference on RFID 2010, Orlando, Florida, April 2010.

33. ***Invited*** "Mechanistic studies on sintering of nanoparticles for formation of solution-processed thin films", 2010 Spring meeting of the Materials Research Society, San Francisco, CA, April 2010.

34. ***Invited*** "Printed Electronics: the confluence of printing and semiconductors", Vivek Subramanian, 2009 International Conference on Flexible and Printing Electronics, Jeju Island, Korea, Nov 2009.

35. ***Invited*** "Organic Transistor Vapor and Biosensors – Technology Status and Implementation Issues", Vivek Subramanian, Frank Liao, Lakshmi Jagannathan, Electrochemical Society Meeting, Vienna, Austria, October 2009.

36. ***Invited*** "Printed transistors for low-cost electronics: the confluence of printing and printable electronic materials", Vivek Subramanian, Alejandro de la Fuente Vornbrock, Steven Molesa, Daniel Soltman, Huai-Yuan Tseng, and Steven K. Volkman, SPIE Optics + Photonics, August 2-6, 2009, San Diego, CA

37. Invited "Printed Zinc Oxide Based Electronics: Materials, Devices, and Outlook", V. Subramanian, S. K. Volkman, and D. R. Redinger, LOPE-C, June 23-25, 2009, Frankfurt, Germany

38. Invited "Printed Devices for Low-Cost Electronics: Technology Status and Outlook", V. Subramanian, PETEC Inaugural Event, March 17, 2009, Durham, United Kingdom

39. invited "Printed Electronic Tags and Sensors for Smart Packaging Applications", Vivek Subramanian, Josephine Chang, Lakshmi Jagannathan, Frank Liao, Steve Molesa, David Redinger, Daniel Soltman, Huai-Yuan Tseng, Steve Volkman, Shong Yin, 2009 Flexible Electronics and Display Conference, Phoenix, AZ, Feb 2-5, 2009.

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40. ***invited*** "Electronic Nose Sensors for Consumer Packaging", V. Subramanian, IDTechEx Printed Electronics USA, San Jose, CA, Dec 2-5, 2008.

41. ***invited*** "Solution-Processed Transparent Transistors for Low-Cost, Flexible Displays", V. Subramanian, S. K. Volkman, and D. R. Redinger, LEOS 2008: The 21st Annual Meeting of the IEEE Lasers and Electro-Optics Society, Newport Beach, CA, 9-13 November, 2008.

42. ***invited*** "Organic chemical and biosensors for smart packages", V. Subramanian, IDTechEx Printed Electronics Asia, Tokyo, Japan, Oct 8-9, 2008.

43. ***invited*** "Printed Electronics for Low-Cost Tags, Displays, and Sensors", V. Subramanian, 1st International Conference on R2R Printed Electronics, Seoul, Korea, April 30-May 2, 2008.

44. ***invited*** "Printed organic RFID tags: technology, roadmaps, and challenges", V. Subramanian, 1st Plastic Electronics Asia Conference and Showcase, Seoul, Korea, June 24-26, 2008

45. ***invited*** "Power supply considerations and solutions for printed electronic tags and sensors", V. Subramanian, IDTechEx Printed Electronics Europe, Dresden, Germany, April 8-9, 2008

46. ***invited*** "Printed Chemical and Biosensors: Technology, Design and Challenges", GOSPEL Workshop on Plastic Chemical Sensors, Dresden, Germany, April 9, 2008

47. ***Plenary*** "Printed Electronics For Low-Cost Electronic Systems: Technology Status and Application Development", Vivek Subramanian, Josephine B. Chang, Alejandro de la Fuente Vornbrock, Daniel C. Huang, Lakshmi Jagannathan, Frank Liao, Brian Mattis, Steven Molesa, David R. Redinger, Daniel Soltman, Steven K. Volkman, Qintao Zhang, 38th European Solid State Device Research Conference, Edinburgh, Scotland, September 15-19, 2008

48. ***invited*** "Printed Organic Transistors for Low-cost Tags, Displays, and Sensors: Technology, Modeling and Challenges", Vivek Subramanian, Alejandro de la Fuente Vornbrock, Huai-Yuan Tseng and Shong Yin, Materials Research Society Fall Meeting, Boston, MA, Dec 1-4, 2008.

49. ***invited*** "Printed Electronics for Low-Cost Tags and Sensors", Vivek Subramanian, Sixth Annual Workshop on Microelectronics and Electron Devices, April 18, 2008.

50. ***invited*** "Printed organic RF tags, chemical sensors and biosensors", Vivek Subramanian, International Symposium for Flexible Electronics and Display, Hsinchu, Taiwan, Nov 18, 2007.

51. ***invited*** "Printed Tags and Sensors for RFID: Opportunities and Challenges", Vivek Subramanian, Printed Electronics USA 2007, San Francisco, CA, Nov 14, 2007.

52. ***invited*** "Printed RFID Tags: Materials, Processes, and Devices", Vivek Subramanian, Daniel Soltman, Daniel Huang, Steven Molesa, 2007 AiChE Annual Meeting, Salt Lake City, UT, Nov. 8, 2007.

53. ***invited*** "Printed organic RFID tags: technology, roadmaps, and challenges", Vivek Subramanian, 3rd Global Plastic Electronics Conference and Showcase, Frankfurt, Germany, Oct 30, 2007.

54. ***invited*** "Printed organic transistors: technology, characteristics, and modeling", Vivek Subramanian, Alejandro de la Fuente Vornbrock, Daniel Soltman, Huai-Yuan Tseng, and Steve Molesa, 212th meeting of the Electrochemical Society, Washington, DC, Oct 8, 2007.

55. ***invited*** "Printed electronic tags and sensors - device, materials, and circuit issues", Vivek Subramanian, 2007 Organic Electronics Conference and Exhibition, Frankfurt, Germany, Sept 25, 2007.

56. ***invited*** "Inkjet printing of transistors, diodes, and passive components for smart tags", Vivek Subramanian, Innovations in Inkjet: 3rd DPI Inkjet Workshop, Eindhoven Institute of Technology, Netherlands, June 28-29, 2007.

57. ***invited*** "Printed organic transistors", A. de la Fuente and V. Subramanian, Industry Forum on Printed Electronics, Chicago, IL, April 23-24, 2007

58. ***invited*** "From Materials to Circuits: Implications of printed materials on printed RFID", V. Subramanian, 2007 Pira printed RFID conference, Frankfurt, Germany, June 4-6, 2007.

59. ***keynote*** "Droplet on demand lithography: An enabling technology for low-cost electronics", V. Subramanian, A. de la Fuente Vornbrock, S. Molesa, D. Redinger, Q. Zhang, and S. K. Volkman, SPIE Advanced lithography, 27th February, 2007

60. ***invited*** "Printed RFID tags: performance needs and technology trends", V. Subramanian, 2007 IDTechEx Smart labels USA , Boston, MA, Febraury 20-23, 2007.

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61. ***keynote*** "Printed Organic Transistors for low-cost tagging and sensing applications", V. Subramanian, J. Chang, A. de la Fuente Vornbrock, S. Molesa, D. Soltman, and Q. Zhang. 6th International IEEE Conference on Polymers and Adhesives in Microelectronics and Photonics, Tokyo, January 15th-18th, 2007.

62. ***invited*** "Nano Inks for Printed RFID", V. Subramanian, Pira Nanoscale Inks and Pigment Technologies Conference, Chicago, IL, Sept 27-28, 2006.

63. ***invited*** "Toward Printed RFID: Materials, Processes, and Devices", V. Subramanian, 5th Annual Printed Electronics and Displays Conference and Trade Fair, Las Vegas, Oct 11-13, 2006.

64. ***invited*** "Inkjetted Organic Transistors for Smart Tagging Applications", Vivek Subramanian, Jean M. J. Frechet, Steven Molesa, Josephine Chang, Amanda R. Murphy, Alejandro de la Fuente Vornbrock, Steven Volkman, 2006 AiChE Annual Meeting, Nov 17th, 2006

65. ***invited focal paper*** "All-printed electronics: Materials, Devices, and Circuit Implications", V.Subramanian, J. Chang, S. Molesa, D. Redinger, and S. Volkman, Digital Fabrication 2006, Denver, CO, Sept 17-22, 2006.

66. ***invited*** "Printed transistors and passive components for low-cost electronics applications", V. Subramanian, J. B. Chang, S. E. Molesa, S. K. Volkman, and D. R. Redinger, International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA) April, 2006, pp. 68-9.

67. ***invited*** "Advanced printed materials and devices for RFID applications", V. Subramanian, IDTechEx Printed Electronics Europe, April 19-21, 2006.

68. ***invited*** "Printed Electronic Nose Vapor Sensors for Consumer Product Monitoring", V. Subramanian, J. Lee, V. Liu, S. Molesa, IEEE International Solid State Circuits Conference, Paper 15.3, February, 2006.

69. ***invited*** "Nanotechnology in Printed Electronics: Nanoparticles, Nanorods, and Nanowhy", V. Subramanian, Pira Pack Electronics Conference, January 25-26, 2006.

70. ***invited*** "All-printed RFID Tags: Materials, Devices, and Circuit Implications", Vivek Subramanian, Paul C. Chang, Daniel Huang, Josephine B. Lee, Steven E. Molesa, David R. Redinger, and Steven K. Volkman, VLSI Design, 2006, Hyderabad India, Jan 2006.

71. ***invited*** "Printed organic transistors: materials and technology", Vivek Subramanian, Pacifichem 2005: American Chemical Society Pacific Basin meeting, December 15-20, 2005, Honolulu, HI,

72. ***invited*** "Low-cost arrayed gas sensors for environmental monitoring". Vivek Subramanian, Josephine Lee and Vincent Liu, Materials Research Society Fall Symposium, Paper S2.1, Boston, MA, December 2005.

73. ***invited*** "Prospects for All-printed RFID: Materials, Devices, Circuits", V. Subramanian, International Workshop on Radio Frequency Identification (RFID) and Wirelss Sensors, 11-13 November, 2005, Kanpur, India.

74. ***invited*** "Printed electronics for low-cost tagging applications", V. Subramanian, 2005 International Symposium on Flexible Electronics and Display, Hsinchu, Taiwan, October 2005.

75. ***invited*** "Printed electronic nose gas sensors", Vivek Subramanian, Plastic Electronics 2005, Frankfurt, Germany, Oct 4-5, 2005

76. ***invited*** "Uses of nanotechnology in printed electronics", Vivek Subramanian, Printed Electronics 205, Pira International, Thistle Marble Arch, London, UK, Sept 14-15, 2005

77. ***invited*** "Printed organic transistors for low-cost RFID applications", Vivek Subramanian, Proceedings of SPIE-The International Society for Optical Engineering vol. 5940, (594013/1-594013/9) , pp. 170-178, 2005.

78. ***invited*** "Advanced printed materials and devices for ultra-low-cost RFID", Vivek Subramanian, Printed RFID: Achieving low cost tags through printed electronics – Pira International, Gatwick, Surrey, UK, May 10-11, 2005.

79. ***Plenary session invited talk*** "Printed Organic Transistors for Ultra-low-cost RFID Applications", Vivek Subramanian, Paul C. Chang, Josephine B. Lee, Steven E. Molesa, and Steven K. Volkman, Polytronic 2004: 4th International IEEE Conference on Polymers and Adhesives in Microelectronics and Photonics, Portland, Oregon, USA, 12 September 2004.

80. ***invited*** "Materials, Device, and Circuits Issues for low-cost printed RFID", V. Subramanian, 2nd Cintelliq Organic Semiconductor Conference, 2004 (OSC-2004), Cambridge, England, October 2004.

81. ***invited*** "All-printed flexible organic thin film transistors: Current status and outlook for the future", V. Subramanian, J. M. J. Fréchet, P. C. Chang, D. C. Huang, J. B. Lee, F. Liao, B. A. Mattis, S. Molesa, A. R. Murphy, D. R. Redinger, and S. K. Volkman, 206th meeting of the Electrochemical Society, Honolulu, HI, October 2004.

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82. ***invited*** "Nanoscale organic transistors: towards gain in molecular devices", V. Subramanian, P. C. Chang, J. B. Lee, T. Le, A. Murphy, J. M. J. Frechet, and A. Liddle, 2004 IEEE Nanoscale Devices and Systems Integration Conference, Miami, FL, 2004.

83. ***invited*** "Towards Printed Low-Cost RFID Tags: Device, Materials and Circuit Technologies", V. Subramanian, 2nd Advanced Technology Workshop on Printing an Intelligent Future: Printed Organic and Molecular Electronic Technologies, Boston, MA, March 16-19, 2003.

84. ***invited*** "Prospects for organic semiconductor based devices and circuits: applications, performance, and reliability considerations", V. Subramanian, 2002 Topical Research Conference on Reliability, Oct 2002.

85. ***invited*** "FinFET - quasi-planar double-gate MOSFET", S. H. Tang, L. Chang, N. Lindert, Y-K. Choi, W-C. Lee, X. Huang, V. Subramanian, J. Bokor, T-J. King, C. Hu, 20001 IEEE International Solid-State Circuits Conference Digest of Technical Papers, pp. 118-119, 437, 2001.

86. ***invited*** "3-D ICs with Multiple Si Layers: Performance Analysis, and Technology", K. Saraswat, K. Banerjee, A. Joshi, P. Kalavade, S. Souri, and V. Subramanian, *presented at* The Fifth International Symposium on Low and High Dielectric Constant Materials: Materials Science, Processing, and Reliability Issues, 197th meeting of the Electrochemical Society, Toronto, Ontario, Canada, May 14-18, 2000.

87. ***invited*** "Novel 3-D Structures", K. C. Saraswat, S. J. Souri, V. Subramanian, A. R. Joshi, and A. W. Wang, 1999 IEEE International SOI Conference Proceedings, pp. 54-55.

88. ***invited*** "Seeding Technology for High Performance TFTs", K. C. Saraswat and V. Subramanian, Proceedings of the Electronic Display Forum 98, EIAJ/SEMI, Yokohama, April 1998, pp. 2.7-2.15.

89. ***invited*** "A Low-Temperature Polycrystalline Si TFT Technology for Large-Area AMLCD Drivers", K. C. Saraswat, V. Subramanian, and S. Jurichich, Polycrystalline Thin Films III - Structure, Texture, Properties, and Applications, MRS Symposium Proceedings pp 439-449, 1997.

90. ***invited*** "A low temperature polycrystalline SiGe CMOS TFT technology for large area AMLCD drivers", K. C. Saraswat, S. Jurichich, T.-J. King, V. Subramanian, and A. Wang, Proceedings of Thin Film Transistor Technologies III, ECS Symposium, 1996, pp. 186-196.

Journal Papers

1. ***invited*** Gerd Grau and Vivek Subramanian, "Dimensional scaling of high-speed printed organic transistors enabling high-frequency operation", Flex. Print. Electron. 2020, Vol. 5 014013

2. ***invited*** William Scheideler and Vivek Subramanian, "Printed flexible and transparent electronics: enhancing low-temperature processed metal oxides with 0D and 1D nanomaterials", 2019 Nanotechnology 30 272001

3. R. Kumar, K. M. Johnson, N. X. Williams, V. Subramanian, "Scaling Printable Zn–Ag2O Batteries for Integrated Electronics", Adv. Energy Mater. 2019, 1803645.

4. William J. Scheideler, Matthew W. McPhail, Rajan Kumar, Jeremy Smith, and Vivek Subramanian, "Scalable, High-Performance Printed InOx Transistors Enabled by Ultraviolet-Annealed Printed High-k AlOx Gate Dielectrics", ACS Applied Materials & Interfaces 2018 10 (43), 37277-37286.

5. J. Smith, S. Chung, J. Jang, C. Biao, V. Subramanian, "Solution-processed complementary resistive switching arrays for associative memory", IEEE Transactions on Electron Devices 64 (10), pp 4310, 2017

6. A. Zeumault, V. Subramanian, "Use of high-k encapsulation to improve mobility in trap-limited metal oxide semiconductors", physica status solidi (b) 254 (10), 1700124, 2017

7. A. Zeumault, W. Scheideler, V. Subramanian, "Electrostatic tuning of spray-deposited ZnO for controlled mobility enhancement", Advanced Functional materials, 27 (30), pp. 1701021, 2017

8. W. J. Scheideler, R. Kumar, A. R. Zeumault, V. Subramanian, "Low-Temperature-Processed Printed Metal Oxide Transistors Based on Pure Aqueous Inks", Advanced Functional Materials 2017, 1606062.

9. Jaewon Jang, Vivek Subramanian, "Effect of electrode material on resistive switching memory behavior of solution-processed resistive switches: Realization of robust multi-level cells", Thin Solid Films, Volume 625, Pages 87-92, 1 March 2017.

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10. S. Chung, M. A. U. Karim, H. J. Kwon, W. Scheideler and V. Subramanian, “A High-Speed Inkjet-Printed Microelectromechanical Relay With a Mechanically Enhanced Double-Clamped Channel-Beam,” Journal of Microelectromechanical Systems, vol. 26, no. 1, pp. 95-101, Feb. 2017.
11. G. Grau, E. J. Frazier, and V. Subramanian, “Printed unmanned aerial vehicles using paper-based electroactive polymer actuators and organic ion gel transistors”, Nature Microsystems & Nanoengineering, vol 2, pp. 16032, 2016
12. ***invited*** Gerd Grau, Jialiang Cen, Hongki Kang, Rungrot Kitsomboonloha, William J Scheideler, and Vivek Subramanian “Gravure-printed electronics: recent progress in tooling development, understanding of printing physics, and realization of printed devices”, IOP Journal of Flexible and Printed Electronics, vol. 1, No. 2, pp. 023002, 2016
13. Scheideler, William J., Jeremy Smith, Igal Deckman, Seungjun Chung, Ana Claudia Arias, and Vivek Subramanian. "A robust, gravure-printed, silver nanowire/metal oxide hybrid electrode for high-throughput patterned transparent conductors." Journal of Materials Chemistry C 4, no. 15 (2016): 3248-3255.
14. Karim, Muhammed Ahosan Ul, Seungjun Chung, Elad Alon, and Vivek Subramanian. "Fully Inkjet-Printed Stress-Tolerant Microelectromechanical Reed Relays for Large-Area Electronics." Advanced Electronic Materials (2016).
15. Khan, Yasser, Felippe J. Pavinatto, Monica C. Lin, Amy Liao, Sarah L. Swisher, Kaylee Mann, Vivek Subramanian, Michel M. Maharbiz, and Ana C. Arias. "Bioelectronic Interfaces: Inkjet-Printed Flexible Gold Electrode Arrays for Bioelectronic Interfaces (Adv. Funct. Mater. 7/2016)." Advanced Functional Materials 26, no. 7 (2016): 981-981.
16. Jang, Jaewon, Seungjun Chung, Hongki Kang, and Vivek Subramanian. "P-type CuO and Cu 2 O transistors derived from a Sol–Gel Copper (II) acetate monohydrate precursor." Thin Solid Films (2016).
17. Grau, Gerd, and Vivek Subramanian. "Fully High-Speed Gravure Printed, Low-Variability, High-Performance Organic Polymer Transistors with Sub-5 V Operation." Advanced Electronic Materials (2016).
18. Zeumault, Andre, and Vivek Subramanian. "Mobility Enhancement in Solution-Processed Transparent Conductive Oxide TFTs due to Electron Donation from Traps in High-k Gate Dielectrics." Advanced Functional Materials (2016).
19. Zeumault, Andre, William Scheideler, Gerd Grau, Jeremy Smith, and Vivek Subramanian. "Patterning of Solution-Processed, Indium-Free Oxide TFTs by Selective Spray Pyrolysis." Advanced Electronic Materials (2015).
20. Jang, Jaewon, Hongki Kang, Himamshu C. Nallan Chakravarthula, and Vivek Subramanian. "Fully Inkjet-Printed Transparent Oxide Thin Film Transistors Using a Fugitive Wettability Switch." Advanced Electronic Materials 1, no. 7 (2015).
21. Grau, Gerd, Rungrot Kitsomboonloha, Hongki Kang, and Vivek Subramanian. "High performance printed organic transistors using a novel scanned thermal annealing technology." Organic Electronics 20 (2015): 150-157.
22. Zeumault, Andre, and Vivek Subramanian. "Improved Technique for Quantifying the Bias-Dependent Mobility of Metal-Oxide Thin-Film Transistors." Electron Devices, IEEE Transactions on 62, no. 3 (2015): 855-861.
23. Swisher, Sarah L., Steven K. Volkman, and Vivek Subramanian. "Tailoring Indium Oxide Nanocrystal Synthesis Conditions for Air-Stable High-Performance Solution-Processed Thin-Film Transistors." ACS applied materials & interfaces 7, no. 19 (2015): 10069-10075.
24. Koo, Hyunmo, Wookyu Lee, Younchang Choi, Junfeng Sun, Jina Bak, Jinsoo Noh, Vivek Subramanian, Yasuo Azuma, Yutaka Majima, and Gyoujin Cho. "Scalability of carbon-nanotube-based thin film transistors for flexible electronic devices manufactured using an all roll-to-roll gravure printing system." Scientific reports 5 (2015).
25. “Perpendicular Magnetization Switching via Current induced Spin-Orbit Torques on Flexible Substrate”, O.J. Lee, L. You, J. Jang, V. Subramanian, S. Sahahuddin, Bulletin of the American Physical Society 60, 2015.
26. “High-Performance Inkjet-Printed Four-Terminal Microelectromechanical Relays and Inverters”, Seungjun Chung, Muhammed Ahosan Ul Karim, Hyuk-Jun Kwon, and Vivek Subramanian, Nano Letters, 15 (5), pp 3261–3266, 2015.
27. ***Invited*** Subramanian, Vivek, Jialiang Cen, Alejandro de la Fuente Vornbrock, Gerd Grau, Hongki Kang, Rungrot Kitsomboonloha, Daniel Soltman, and Huai-Yuan Tseng. "High-Speed Printing of Transistors: From Inks to Devices." Proceedings of the IEEE 103, no. 4 (2015): 567-582.
28. Scheideler, William J., Jaewon Jang, Muhammed Ahosan Ul Karim, Rungrot Kitsomboonloha, Andre Zeumault, and Vivek Subramanian. "Gravure-Printed Sol–Gels on Flexible Glass: A Scalable Route to Additively Patterned Transparent Conductors." ACS applied materials & interfaces 7, no. 23 (2015): 12679-12687.

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29. Lee, OukJae, Long You, Jaewon Jang, Vivek Subramanian, and Sayeef Salahuddin. "Flexible spin-orbit torque devices." Applied Physics Letters 107, no. 25 (2015): 252401.

30. Kitsomboonloha, Rungrot, Hongki Kang, Gerd Grau, William Scheideler, and Vivek Subramanian. "MHz-Range Fully Printed High-Performance Thin-Film Transistors by Using High-Resolution Gravure-Printed Lines." Advanced Electronic Materials 1, no. 12 (2015).

31. Swisher, Sarah L., Monica C. Lin, Amy Liao, Elisabeth J. Leeflang, Yasser Khan, Felippe J. Pavinatto, Kaylee Mann et al. "Impedance sensing device enables early detection of pressure ulcers in vivo." Nature communications 6 (2015).

32. "A Stencil Printed, High Energy Density Silver Oxide Battery Using a Novel Photopolymerizable Poly(acrylic acid) Separator", K. Braam and V. Subramanian, Advanced Materials, Vol. 27, 689-694, 2015

33. "Megahertz-class printed high mobility organic thin-film transistors and inverters on plastic using attoliter-scale high-speed gravure-printed sub-5μm gate electrodes", H. Kang, R. Kitsomboonloha, K. Ulmer, L. Stecker, G. Grau, J. Jang, V. Subramanian, Organic Electronics, vol. 15, 3639-3647, 2014.

34. "Exploitation of the coffee-ring effect to realize mechanically enhanced inkjet-printed microelectromechanical relays with U-bar-shaped cantilevers", S Chung, MAU Karim, M Spencer, HJ Kwon, CP Grigoropoulos, E Alon, V. Subramanian, Applied Physics Letters 105 (26), 261901, 2014.

35. "Printed Transistors on Paper: Towards Smart Consumer Product Packaging", G. Grau, R. Kitsomboonloha, S. L. Swisher, H. Kang, and V. Subramanian, Advanced Functional Materials, Vol. 24, 5067-5074, 2014.

36. "Cell Filling in Gavure Printing for Printed Electronics, J. Cen, R. Kitsomboonloha, and V. Subramanian, vol. 30, 13716-13726, 2014.

37. "Systematic Design of Jettable Nanoparticle-based inkjet inks: Rheology, Acoustics, and Jettability", H. C. Nallan, J. A. Sadie, R. Kitsomboonloha, S. K. Volkman, and V. Subramanian, Langmuir, vol. 30, 13470-13477, 2014.

38. "Three-dimensional Inkjet-printed Interconnects using Functional Metallic Nanoparticle Inks", J. A. Sadie, V. Subramanian, Advanced Functional Materials, vol. 24, 6834-6842, 2014.

39. "Electrical Characteristics of multilayer MoS_2 transistors at real operating temperatures with different ambient conditions", H-J. Kwon, J. Jang, S. Kim, V. Subramanian, and C. P. Grigoropoulos, Applied Physics Letters, vol. 105, 15205, 2014.

40. "Lubrication-related residue as a fundamental process scaling limit to gravure printed electronics", R. Kitsomboonloha and V. Subramanian, Langmuir, vol. 30, 3612-3624, 2014.

41. "Roll-to-roll gravure with nanomaterials for printing smart packaging", M. Jung, J. Kim, H. Koo, W. Lee, V. Subramanian, G. Cho, Journal of Nanoscience and Nanotechnology, vol. 14, 1303-1317, 2014.

42. "Measurement and analysis of 1/f noise under switched bias in organic thin film transistors", H. Kang and V. Subramanian, Applied Physics Letters, 104, 023301, 2014.

43. "A new switching device for printed electronics: Inkjet-printed Microelectromechanical Relay", E. S. Park, Y. Chen, T. J. K. Liu, and V. Subramanian, Nano Letters, 13 (11), 5355-5360, 2013.

44. "Inkjet printing of precisely defined features using contact-angle hysteresis", Dan Soltman, Ben Smith, S.J.S. Morris, Vivek Subramanian, Journal of Colloid and Interface Science, Volume 400, Pages 135–139, 2013

45. "Transparent High-Performance Thin Film Transistors from Solution-Processed SnO2/ZrO2 Gel-like Precursors", J. Jang, R. Kitsomboonloha, S. L. Swisher, E. S. Park, H. Kang, and V. Subramanian, Advanced Materials, 25 (7), pp. 1042-1047, 2013.

46. "Femtoliter-Scale Patterning by High-Speed, Highly Scaled Inverse Gravure Printing", R Kitsomboonloha, SJS Morris, X Rong, V Subramanian, Langmuir 28 (48), 16711-16723, 2012

47. "Resistance Switching Characteristics of Solid Electrolyte Chalcogenide Ag2Se Nanoparticles for Flexible Nonvolatile Memory Applications", J. Jang, F. Pan, K. Braam, and V. Subramanian, Advanced Materials, 24, pp. 3573-3576, 2012

48. "High-Performance Printed Transistors Realized Using Femtoliter Gravure-Printed Sub-10 μm Metallic Nanoparticle Patterns and Highly Uniform Polymer Dielectric and Semiconductor Layers", H. Kang, R. Kitsomboonloha, J. Jang, and V. Subramanian, Advanced Materials, 24, pp. 3065–3069, 2012

49. "All Printed Edge-Triggered Register Using Single Walled Carbon Nanotube-Based Thin Film Transistor" J. Noh, M. Jung, K. Jung, G. Lee, S. Lim, D. Kim, V. Subramanian, G. Cho, Journal of Nanoscience and Nanotechnology, 12, pp. pp. 4261-4264, 2012

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50. "Effect of sintering conditions on mixed ionic-electronic conducting properties of silver sulfide nanoparticles". Shong Yin, Kazuya Terabe, Michael F. Toney, and Vivek Subramanian, J. Appl. Phys. 111, 053530 (2012)

51. "Characterization and optimization of a printed, primary silver-zinc battery", Kyle Braam, Steven K. Volkman, Vivek Subramanian, Journal of Power Sources, vol. 199, pp. 367-372, 2012.

52. "Mechanistic Studies on Sintering of Silver Nanoparticles", Steven K. Volkman, Shong Yin, Teymur Bakhishev, Kanan Puntambekar, Vivek Subramanian, Michael F. Toney, Chemistry of Materials, vol. 23, pp 4634–4640, 2011.

53. "Fully Gravure-Printed D Flip-Flop on Plastic Foils Using Single-Walled Carbon-Nanotube-Based TFTs", J. Noh, M. Jung, K. Jung, G. Lee, J. Kim, S. Lim, D. Kim, Y. Choi, Y. Kim, V. Subramanian, G. Cho, Electron Device Letters, IEEE , vol.32, pp.638-640, 2011

54. "Measurement, analysis, and modeling of 1/f noise in pentacene thin film transistors", H. Kang, L. Jagannathan, V. Subramanian, Applied Physics Letters, vol., 99, pp 062106-062108, 2011.

55. "A Detailed Study of the Forming Stage of an Electrochemical Resistive Switching Memory by KMC Simulation", F. Pan, S. Yin, V. Subramanian, IEEE Electron Device Letters, IEEE , vol.32, pp.949-951, 2011

56. "High-speed organic transistors fabricated using a novel hybrid-printing technique", H-Y. Tseng, B. Purushothaman, J. Anthony, V. Subramanian, Organic Electronics, Vol. 12, pp. 1120-1125, 2011.

57. "AM Radio Circuit Using Printed Electronic Components", J. Noh, J. Kim, N. Lim, J. Kim, V. Subramanian, G. Cho, Journal of Nanoscience and Nanotechnology, Volume 11, pp. 4384-4388, 2011

58. "All Inkjet-Printed, Fully Self-Aligned Circuits for Low-Cost Applications", H-Y. Tseng and V. Subramanian, Organic Electronics, Vol. 12, pp. 249-256, 2011

59. "Modeling of printed single walled carbon nanotube thin film transistors for attaining optimized clock signals", Jinsoo Noh, Minhun Jung, Kyunghwan Jung, Soyeon Lim, Gwangyong Lee, Vivek Subramanian, Ashley D. Leonard, James Tour, and Gyoujin Cho, J. Appl. Phys. 108, pp. 102811, 2010

60. "Fully gravure and ink-jet printed high speed pBTTT organic thin film transistors", Alejandro de la Fuente Vornbrock, Donovan Sung, Hongki Kang, Rungrot Kitsomboonloha, Vivek Subramanian, Organic Electronics, 11, pp. 2037-2044, 2010

61. "Scalability of Roll-to-Roll Gravure-Printed Electrodes on Plastic Foils", Jinsoo Noh, Dongsun Yeom, Chaemin Lim, Hwajin Cha, Jukyung Han, Junseok Kim, Yongsu Park, Vivek Subramanian, Gyoujin Cho, IEEE Transactions on Electronics Packaging Manufacturing, vol. 33, pp. 275 – 283, 2010

62. "Methodology for inkjet printing partially wetting films", D. Soltman, B. Smith, H. Kang, S. Morris, and V. Subramanian, Langmuir, 26, pp. 15686-15693, 2010

63. "Hydrostatic optimization of inkjet-printed films", H. Kang, D. Soltman, and V. Subramanian, Langmuir, 26, pp 11568–11573, 2010

64. ***Invited*** "Printed Electronics: The Challenges Involved in Printing Devices, Interconnects, and Contacts", J. Perelaer, P. J. Smith, D. Mager, D. Soltman, S. K. Volkman, V. Subramanian, J. G. Korvink, U. S. Schubert, J. Mat. Chem., J. Mater. Chem., 20, pp. 8446-8453, 2010

65. "Quantification of Thin Film Crystallographic Orientation Using X-ray Diffraction with an Area Detector", Jessy L. Baker, Leslie H. Jimison, Stefan Mannsfeld, Steven Volkman, Shong Yin, Vivek Subramanian, Alberto Salleo, A. Paul Alivisatos and Michael F. Toney, Langmuir, 2010, 26 (11), pp 9146–9151

66. "Thickness Changes in Polythiophene Gas Sensors Exposed to Vapor", F. Liao, M.F. Toney, and V. Subramanian, Sensors and Actuators B, 148, pp. 74-80, 2010

67. "Physical Discrimination of Amine Vapor Mixtures Using Polythiophene Gas Sensor Arrays", F. Liao, S. Yin, M.F. Toney, V. Subramanian, Sensors and Actuators B, 150, pp. 254-263, 2010

68. "Solution-Processable alpha-omega-Distyryl Oligothiophene Semiconductors with Enhanced Environmental Stability", C. E. Mauldin, K. Puntambekar, A. R. Murphy, F. Liao, V. Subramanian, J.M.J. Fréchet, D.M. DeLongchamp, D.A. Fischer, D.A. M.F. Toney, Chemistry of Materials, vol. 21, 4831—4835, 2009.

69. ***invited*** "Solution-processed Zinc Oxide Transistors for Low-Cost electronics Applications", V. Subramanian, T. Bakhishev, D. R. Redinger, and S. K. Volkman, IEEE Journal of Display Technology, Vol. 5 , pp. 525 – 530, 2009

AMD EX1003
AMD v. Realtek
Page 139

70. “Investigation of Gold Nanoparticle Inks for Low-Temperature Lead-Free Packaging Technology”, T. Bakhishev and V. Subramanian, Journal of Electronic Materials, vol. 38, pp. 2720, 2009.

71. “Label-free low-cost disposable DNA hybridization detection systems using organic TFTs”, Biosensors and Bioelectronics, vol. 25, pp. 972, 2010.

72. “DNA detection using organic thin film transistors: Optimization of DNA immobilization and sensor sensitivity”, Lakshmi Jagannathan, Vivek Subramanian, Biosensors and Bioelectronics, vol. 25, pp. 288, 2009.

73. “First-Principles Studies of the Dynamics of [2]Rotaxane Molecular Switches”, Kinyip Phoa, J. B. Neaton, Vivek Subramanian, Nano Letters, 9, pp. 3225-3229, 2009.

74. “Patternable polymer bulk heterojunction photovoltaic cells on plastic by rotogravure printing”, Jau M. Ding, Alejandro de la Fuente Vornbrock, Ching Ting and Vivek Subramanian,, Solar Energy and Materials, 93, pp. 459-464, 2009.

75. “Scaling and Optimization of Gravure-Printed Nanoparticle Lines for Printed Electronics”, D. C. Sung, A. de la Fuente Vornbrock, V. Subramanian, IEEE Transactions on Components and Packaging Technologies, 33, pp. 105 – 114, 2010.

76. “Selective Growth of Zinc Oxide Nanorods on Inket printed seed patterns”, R. Kitsomboonloha, S. Baruah, M. T. Z. Myint, V. Subramanian, and J. Dutta, “ Journal of Crystal Growth, 311, pp. 2352-2358, 2009

77. “Inkjet printed line morphologies and temperature control of the coffee ring effect”, Dan Soltman and Vivek Subramanian, Langmuir, vol 24(5), pp. 2224-2231, 2008.

78. “High-Performance Chemical-Bath-Deposited Zinc Oxide Thin-Film Transistors”, D. Redinger and V. Subramanian, IEEE Transactions on Electron Devices, 54, pp. 1301-1307, 2007.

79. “DNA hybridization detection with organic thin film transistors: Toward fast and disposable DNA microarray chips”, Qintao Zhang and Vivek Subramanian, Biosensors and Bioelectronics, 22, pp. 3182-3187, 2007.

80. “Performance recovery and optimization of poly(3-hexylthiophene) transistors by thermal cycling”, B. A. Mattis, P. C. Chang, and V. Subramanian, Synthetic Metals, 156, pp. 1241-1248, 2006.

81. “Printable polythiophene gas sensor array for low-cost electronic noses”, Josephine B. Chang, Vincent Liu, Vivek Subramanian, Kevin Sivula, Christine Luscombe, Amanda Murphy, Jinsong Liu, and Jean M. J. Fréchet J. Appl. Phys. 100, 014506 (2006)

82. “Effect of active layer thickness on bias stress effect in pentacene thin-film transistors”, Josephine B. Chang and Vivek Subramanian Appl. Phys. Lett. 88, 233513 (2006)

83. “Correlating molecular design to microstructure in thermally convertible oligothiophenes: the effect of branched versus linear end groups”, D. M. DeLongchamp, Y. Jung, D. A. Fischer, E. K. Lin, P. Chang, V. Subramanian, A. R., Murphy, J. M. J. Frechet., Journal of Physical Chemistry B, vol.110, no.22, 8 June 2006, pp. 10645-50.

84. “Inkjetted Crystalline Single-Monolayer Oligothiophene OTFTs”, P. C. Chang,, S. E. Molesa, A. R. Murphy, J. M. J. Fréchet, and V. Subramamian, IEEE Transactions on Electron Devices, vol. 53, pp. 594-600, 2006.

85. ***selected for cover:*** “Direct correlation of organic semiconductor film structure to field-effect mobility”, D. M. DeLongchamp, S. Sambasivan, D. A. Fischer, E. K. Lin, P. Chang, A. R. Murphy, J. M. J. Frechet, V. Subramanian, Advanced Materials, vol. 17, 2340-344, 2005.

86. “Self-Assembly, Molecular Ordering, and Charge Mobility in Solution-Processed Ultrathin Oligothiophene Films”, A. R. Murphy, P. C. Chang, P. VanDyke, J. Liu, J. M. J. Fréchet, V. Subramanian, D. M. DeLongchamp, S. Sambasivan, D. A. Fische, E. K. Lin, Chem. Mater., vol. 17, pp. 6033-41, 2005.

87. “Printed organic transistors for ultra-low-cost RFID applications”, V. Subramanian, P.C. Chang, J. B. Lee, S. E. Molesa, S. K. Volkman, IEEE Transactions on Components & Packaging Technologies, vol. 28, pp. 742-727, 2005.

88. ***invited*** “Progress towards development of all-printed RFID tags: Materials, Processes, and Devices”, Vivek Subramanian, Jean M. J. Fréchet , Paul C. Chang, Daniel Huang, Josephine B. Lee, Steven E. Molesa, Amanda R. Murphy, David R. Redinger, and Steven K. Volkman, Proceedings of the IEEE, vol. 93, pp. 1330-1338, 2005.

89. “10-nm channel length pentacene transistors”, Josephine Lee, Paul Chang, Alex Liddle, and Vivek Subramanian, IEEE Transactions on Electron Devices, vol. 52, pp. 1874-1879, 2005.

90. “Organic TFTs as gas sensors for electronic nose applications”, F. Liao, C. Chen, and V. Subramanian, Sensors and Actuators B-Chemical. Vol. 107, pp. 849-855, 2005.

AMD EX1003
AMD v. Realtek
Page 140

91. “Nanoscale device isolation of organic transistors via electron-beam lithography”, Brian A. Mattis, Yunan Pei, and Vivek Subramanian, Appl. Phys. Lett., vol. 86, pp. 769-772, 2005.

92. “Weave Patterned Organic Transistors on Fiber for E-Textiles”, Josephine B. Lee and Vivek Subramanian, IEEE Transactions on Electron Devices, vol. 62, pp. 269, 2005.

93. “An ink-jet-deposited passive component process for RFID”, D. Redinger, R. Farshchi, and V. Subramanian, IEEE Transactions on Electron Devices, vol. 51, pp. 1978, 2004.

94. “Film Morphology and Thin Film Transistor Performance of Solution Processed Oligothiophenes”, Paul C. Chang, Josephine Lee, Daniel Huang, Vivek Subramanian, Amanda R. Murphy, and Jean M. J. Fréchet,„ J. Chem. Mat., vol. 16, pp. 4783, 2004.

95. “Organic Thin Film Transistors from a Soluble Oligothiophene Derivative Containing Thermally Removable Solubilizing Groups”, Amanda R. Murphy, Jean M. J. Frechet, Paul Chang, Josephine Lee,and Vivek Subramanian, J. Am. Chem. Soc. vol. 126, pp. 1596, 2004.

96. “Plastic-compatible low-resistance printable gold nanoparticle conductors for flexible electronics”, D. Huang, F. Liao, S. Molesa, D. Redinger, and V. Subramanian, Journal of the electrochemical society, Vol. 150, pp. 412, 2003.

97. “Observation of dopant-mediated intermixing at Ge/Si Interface”, H. Takeuchi, P. Ranade, V. Subramanian, and T-J. King, Applied Physics Letters, Vol. 80, pp. 3706-3708, 2002.

98. “A novel elevated source/drain PMOSFET formed by Ge-B/Si Intermixing”, P. Ranade, H. Takeuchi, V. Subramanian, and T-J. King, IEEE Electron Device Letters, Vol. 23, pp. 218-220, 2002.

99. “Design and Fabrication of 50 nm Ultra-Thin Body P-MOSFETs with a Silicon-Germanium Heterostructure Channel". Y-C. Yeo, V. Subramanian, J. Kedzierski, P. Xuan, T-J. King, J. Bokor, and C. Hu, IEEE Transactions on Electron Devices, 49, pp. 279 –286, 2002 (IEEE Paul Rappaport Award for best paper in an IEEE Electron Device Society Journal).

100. “Observation of Boron and Arsenic Mediated Interdiffusion Across Germanium/Silicon Interfaces”, P. Ranade, H. Takeuchi, V. Subramanian and T.-J. King, Electrochemical and Solid-State Letters, Vol. 5, no. 2, pp. G5-G7, 2002.

101. “Sub-50nm P-Channel FinFET”, X. Huang, W-C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y-K. Choi, K. Asano, V. Subramanian, T-J. King, J. Bokor, and C. Hu, IEEE Transactions on Electron Devices, Vol. 48, pp. 880-886, 2001.

102. “A 20 nm gate-length ultra-thin body p-MOSFET with silicide source/drain.” J. Kedzierski, P. Xuan, V. Subramanian, E. Anderson, J. Bokor, T.-J. King, and C. Hu, Superlattices and Microstructures, Vol. 28, pp.445-452, 2000.

103. “Ultrathin-body SOI MOSFET for deep-sub-tenth micron era”, Y-K. Choi, K. Asano, N. Lindert, V. Subramanian, T-J. King, J. Bokor, C. Hu , IEEE Electron Device Letters , Vol. 21, pp. 254-255, 2000.

104. “Nanoscale Ultra-Thin-Body Silicon-on-Insulator P-MOSFET with a SiGe/Si Heterostructure Channel”, Y. C. Yeo, V. Subramanian, J. Kedzierski, P. Xuan, T-J. King, J. Bokor, and C. Hu, IEEE Electron Device Letters, Vol. 21, pp. 161-163, 2000.

105. “Low-leakage Germanium-seeded Laterally-crystallized Single-grain 100nm TFTs for Vertical Integration Applications”, V. Subramanian, M. Toita, N. R. Ibrahim, S. J. Souri and K. C. Saraswat, IEEE Electron Device Letters, Vol. 20, pp. 341-343, 1999.

106. “High Performance Germanium-Seeded Laterally Crystallized TFTs for Vertical Device Integration”, V. Subramanian and K. C. Saraswat, IEEE Transactions on Electron Devices. Vol. 18, pp. 1934-1939, 1998.

107. “Optimization of Silicon-Germanium TFTs through the control of amorphous precursor characteristics”, V. Subramanian and K. C. Saraswat, IEEE Transactions on Electron Devices, vol. 45, pp. 1690-1695, 1998.

108. “Controlled Two-Step Solid Phase Crystallization for High Performance Polysilicon TFTs”, V. Subramanian, P. Dankoski, L. Degertekin, B. T. Khuri-Yakub, and K. C. Saraswat, IEEE Electron Device. Letters, vol. 18, pp. 378-81, 1997

109. “In-Situ Monitoring of Crystallinity and Temperature During Rapid Thermal Crystallization of Silicon on Glass”, V. Subramanian, L. Degertekin, P. Dankoski, B. T. Khuri-Yakub, and K. C. Saraswat, Journal of the Electrochemical Society, vol. 144, 1997, pp. 2216-2221.

110. “The Effect of Ionizing Radiation Damage on Transconductance of Short Channel Insulated Gate Field Effect Transistors”, Subramanian & Bhattacharya, Japanese Journal of Applied Physics I, vol. 34 (1995), pp. 1809

AMD EX1003
AMD v. Realtek
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111. "Chemical Contamination of Thin Oxides and Native Silicon for use in Modern Device Processing", Subramanian et al, International Journal of Electronics, vol. 78 (1995), pp. 519

Conference Presentations

1. R. Kumar, E. Kedzie, B. D. McCloskey, and V. Subramanian, "Characterizing Zn Corrosion in Printed Zn-Air batteries Via Operando Dems, XRD, and XAS", Electrochemical Conference on Energy and the Environment: Bioelectrochemistry and Energy Storage, MA2019-04 July 21-26, 2019, Glasgow, Scotland
2. Carlos Biaou, Matt McPhail, Vivek Subramanian and Oscar Dubon, "Comprehensive Multifactorial Studies on the Degradation of Perovskite Solar Cells in Operation", 2019 Spring Materials Research Society Meeting, Phoenix, AZ, April 22-26, 2019.
3. Rajan Kumar, Jessica E. Nichols, Bryan D. McCloskey, and Vivek Subramanian, "Low-Temperature-Processing of Printed Cathodes for Aqueous Metal-Air Batteries", ECS AiMES 2018 Meeting, September 30, 2018 - October 4, 2018, Cancun, Mexico
4. N. Deka and V. Subramanian, "First demonstration of vacuum-sealed fully integrated BEOL-compatible field emission devices for Si integrated high voltage applications," 2018 76th Device Research Conference (DRC), Santa Barbara, CA, 2018, pp. 1-2.
5. "Inkjet-printed MEM relays for active solar cell routing", S Patel, WJ Scheideler, MAU Karim, V Subramanian, Micro Electro Mechanical Systems (MEMS), 2018 IEEE, 616-619
6. "Back-channel engineering of ultrathin printed indium oxide transistors for carbon dioxide sensing", Y. Kobayashi, W. Scheideler, V. Subramanian, 2017 Materials Research Society Fall Meeting, Boston, MA, Nov 28, 2017.
7. "Morphological Control of Gravure Printed Perovskite Films", M. McPhail and V. Subramanian, 2017 Materials Research Society Fall meeting, Boston, MA, Nov 29, 2017.
8. "Improving high-speed nanomaterial printing with sub-process-decoupled gravure printer design", W. Scheideler, V. Subramanian, ASME 2017 Conference on Smart Materials, Adaptive Structures, and Intelligent Systems, Snowbird, UT, Sept 18-20, 2017
9. "Development of a printed cathode and catalyst layer for printed zinc-air batteries, R. Kumar, N. Williams, and V. Subramanian, 232nd ECS Meeting, National Harbor, MD, Oct 1-5, 2017.
10. "UV-annealing-enhanced stability in high-performance printed InOx transistors, W. Scheideler, V. Subramanian, 2017 IEEE Electron Devices Technology and Manufacturing Conference (EDTM), Toyama, Japan, Feb 28-Mar 2, 2017.
11. "Inkjet-printed Four-Terminal Microelectromechanical Relays for 3-Dimensional Logic Applications" S. Cheung, M. Karim, H-J Kwon, T. Lee, and V. Subramanian, 2017 Spring Meeting of the Materials Research Society, Pheonix, AZ, April 17-21, 2017.
12. "Fluid mechanical proximity effects in high-resolution gravure printing for printed electronics", G Grau, WJ Scheideler, V Subramanian, 69th Annual Meeting of the APS Division of Fluid Dynamics, Portland, OR, Nov 20-22, 2016
13. "Systematic Ink Design and Solubility Enhancement via Genetic Algorithm for Nanoparticle-based Inkjet Inks", J. Sadie, H. Nallan, S. Volkman, V. Subramanian, NIP & Digital Fabrication Conference (Vol. 2015, No. 1, pp. 439-442). Society for Imaging Science and Technology.
14. M. Ahosan Ul Karim, S. Chung, E. Alon, V. Subramanian, "Stress-tolerant fully inkjet-printed Reed Relays", IEEE International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS) (pp. 568-571), 2015.
15. "High-resolution gravure printed lines: proximity effects and design rules", G. Grau, W. J. Scheideler, V. Subramanian, SPIE Organic Photonics+ Electronics (pp. 95690B-95690B). International Society for Optics and Photonics, 2015
16. Grau, Gerd, Rungrot Kitsomboonloha, and Vivek Subramanian. "Fabrication of a high-resolution roll for gravure printing of 2μm features." In SPIE Organic Photonics+ Electronics, pp. 95680M-95680M. International Society for Optics and Photonics, 2015.
17. Zeumault, Andre, and Vivek Subramanian. "Interpretation of subthreshold swing and threshold voltage in solution-processed zinc oxide TFTs." In Device Research Conference (DRC), 2015 73rd Annual, pp. 179-180. IEEE, 2015.
18. Zeumault, Andre, and Vivek Subramanian. "Anomalous process temperature scaling behavior of sol-gel ZrO x gate dielectrics: Mobility enhancement in ZnO TFTs." In Device Research Conference (DRC), 2015 73rd Annual, pp. 203-204. IEEE, 2015.

AMD EX1003
AMD v. Realtek
Page 142

19. Scheideler, William J., Andre Zeumault, and Vivek Subramanian. "Engineering high-k La x Zr 1− x O y dielectrics for high-performance fully-solution-processed transparent transistors." In Device Research Conference (DRC), 2015 73rd Annual, pp. 205-206. IEEE, 2015.

20. "Fully Printed Transient Silver-Zinc Primary Battery", Nishita Deka, Kyle Braam, Vivek Subramanian, 2015 Spring Meeting of the Materials Research Society, San Francisco, CA, April 6-10, 2015.

21. "Perpendicular Magnetization Switching via Current induced Spin-Orbit Torques on Flexible Substrate", OukJae Lee, Long You, JaeWon Jang, Vivek Subramanian, Sayeef Salahuddin. 2015 Spring Meeting of the Materials Research Society, San Francisco, CA, April 6-10, 2015.

22. "Direct Patterning of Sol-Gel-Enhanced Silver Nanowire Electrodes by Gravure Printing", William Joseph Scheideler, Vivek Subramanian, 2015 Spring Meeting of the Materials Research Society, San Francisco, CA, April 6-10, 2015.

23. "Development of Oxidation-Resistant Cu/Ag Alloyed Particles for Realization of Low-Resistance, Low-Cost Printed Conductors", Steven K Volkman, Vivek Subramanian, 2015 Spring Meeting of the Materials Research Society, San Francisco, CA, April 6-10, 2015.

24. "Perpendicular Magnetization Switching via Current induced Spin-Orbit Torques on Flexible Substrate", OukJae Lee, Long You, Jaewon Jang, Vivek Subramanian, Sayeef Salahuddin, APS Bulletin of the American Physical Society. APS March Meeting 2015 Volume 60, Number 2. San Antonio, TX, March 2–6, 2015

25. "Gravure-Printing Transparent Sol-Gel Conductors on Flexible Glass Substrates", William Joseph Scheideler, Jaewon Jang, Vivek Subramanian, 2014 Fall Meeting of the Materials Research Society, Boston, MA, Nov 30 – Dec 6, 2014.

26. "High performance printed organic transistors using a novel scanned thermal annealing technology," G. Grau, R. Kitsomboonloha, H. Kang, and V. Subramanian, LOPE-C, Munich, 2014.

27. "High-Performance Organic TFTs using High-Resolution Gravure Printed Electrodes", R. Kitsomboonloha, H. Kang, V. Subramanian, 2013 Fall Meeting of the Materials Research Society, Boston, Ma, Dec 1-6, 2013

28. "Effect of Substrate Roughness on the Performance of Printed OTFTs on Paper Substrates", G. Grau and V. Subramanian, 2013 Fall Meeting of the Materials Research Society, Boston, Ma, Dec 1-6, 2013.

29. "Simulation and Experimental Characterization of Cell Filling During Highly-Scaled Gravure Printing for Printed Electronics Applications", A. Cen, R. Kitsomboonloha, and V. Subramanian, 2013 Fall Meeting of the Materials Research Society, Boston, Ma, Dec 1-6, 2013.

30. ***Best paper award*** "Droplet-on-demand Inkjet-Filled TSVs as a pathway to cost-efficient chip stacking", J. Sadie, N. Quack, M. Wu, and V. Subramanian, IMAPS 2013 - 46th International Symposium on Microelectronics, Orlando, FL, Sept 30 – Oct 3, 2013.

31. "Through silicon vias and thermocompression bonding using inkjet-printed gold nanoparticles for heterogeneous MEMS Integration", N. Quack, J. Sadie, V. Subramanian, and M. C. Wu, The 17th International Conference on Solid-State Sensors, Actuators and Microsystems, Barcelona, Spain, June 16-20, 2013.

32. "Micro-relay reliability improvement by inkjet-printed microshell encapsulation", Yenhao Chen, Eung Seok Park, I-Ru Chen, Louis Hutin, Vivek Subramanian, Tsu-Jae King Liu, The 17th International Conference on Solid-State Sensors, Actuators and Microsystems, Barcelona, Spain, June 16-20, 2013.

33. "Understanding the Enhanced Mobility of Transparent Metal-Oxide Semiconductor Thin-Film Transistors Utilizing High-k Dielectrics" Andre Zeumault, Jaewon Jang, Vivek Subramanian, 2013 Large Area, Organic and Printed Electronics Conference (LOPE-C), Munich, Germany, June 11-13, 2013.

34. "High Performance Solution-Processed Thin-Film Transistors Based on In2O3 Nanocrystals: Investigating Effects of Annealing Conditions and Gate Dielectric", Sarah L. Swisher, Steve Volkman, and Vivek Subramanian, 2013 Large Area, Organic and Printed Electronics Conference (LOPE-C), Munich, Germany, June 11-13, 2013.

35. "Printed Transistors on Paper: Towards Smart Consumer Product Packaging", Gerd Grau, Rungrot Kitsomboonloha, Sarah Swisher, Hongki Kang and Vivek Subramanian, 2013 Large Area, Organic and Printed Electronics Conference (LOPE-C), Munich, Germany, June 11-13, 2013.

36. "Inkjetted Inorganic Transistors using a Sol-gel Processed SnO2 Semiconductor and Sb-doped SnO2 Electrodes", Jaewon Jang, Eung Seok Park, Hongki Kang and Vivek Subramanian, Materials Research Society Fall 2012 Meeting, Boston, MA, Nov 25-30, 2012

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37. ***Best Paper Award*** "Demonstration of Inkjet Printed Nanoparticle-based Inks for Solder Bump Replacement", Jacob Sadie, Steven Volkman, and Vivek Subramanian, 45th International Symposium on Microelectronics (IMAPS 2012), San Diego, CA, September 9 - 13, 2012

38. "Experimental study of the residue film in direct gravure printing of electronics", Rungrot Kitsomboonloha, Umut Ceyhan, SJS Morris, Vivek Subramanian, 65th Annual Meeting of the APS Division of Fluid Dynamics, Volume 57, Number 17, San Diego, California, November 18–20, 2012

39. "Lubrication analysis of the nanometric coating film deposited during gravure printing", Umut Ceyhan, Rungrot Kitsomboonloha, SJS Morris, Vivek Subramanian, 65th Annual Meeting of the APS Division of Fluid Dynamics, Volume 57, Number 17, San Diego, California, November 18–20, 2012

40. "A Simple Model of Highly Scaled Gravure Printing", R. Kitsomboonloha, S. Morris and V. Subramanian, 2012 Large Area Organic and Printed Electronics Conference (LOPE-C), Munich, Germany, July 2012

41. "Development and characterization of an air-stable printed silver-zinc battery", K. Braam, S. K. Volkman, and V. Subramanian, 2012 Large Area Organic and Printed Electronics Conference (LOPE-C), Munich, Germany, July 2012.

42. "A very reliable multilevel YSZ resistive switching memory", F. Pan, J. Jang, and V. Subramanian, 70th Annual Device Research Conference (DRC), 18-20 June 2012, pp. 217 - 218

43. "High performance solution-processed thin-film transistors based on In2O3 nanocrystals", S. L. Swisher, S. Volkman, K. Braam, J. Jang, V. Subramanian, 70th Annual Device Research Conference (DRC), 18-20 June 2012, pp. 241 - 242

44. "A Mixed-Signal EEG Interface Circuit For Use In First Year Electronics Courses,", V. Lee, J. Monski, W. Williams, B. Muthuswamy, T. Swiontek, M. Maharbiz, V. Subramanian, F. Kovac, Proceedings of the 2012 IEEE International Symposium on Circuits and Systems (ISCAS), pp. 2689 – 2692, May 2012.

45. "A novel Yittrium Stabilized Zirconia based resistive switching memory", Feng Pan, Jaewon Jang, Vivek Subramanian, 2012 Spring Materials Research Meeting.

46. "Resistance Switching Memory Device with Ag2Se Nano-particle Aqueous Ink", Jaewon Jang, Feng Pan, Kyle Braam and Vivek Subramanian, 2012 Spring Materials Research Meeting.

47. "Highly-Scaled Gravure Printed organic TFTs with 10μm channel length on Plastic with 300 kHz operation", Hongki Kang, Rungrot Kitsomboonloha, Jaewon Jang, and Vivek Subramanian, 2012 Spring Materials Research Meeting.

48. "Inkjet-Printed Microshell Encapsulation: A New Zero-Level Packaging Technology", Eung Seok Park, Jaeseok Jeon, Vivek Subramanian, and Tsu-Jae King Liu, The 25th International Conference on Micro Electro Mechanical Systems, Paris, France, January 29 – February 2, pp. 257-230,2012.

49. "Inkjet-Printed Micro-Electro-Mechanical Switches", Eung Seok Park, Yenhao Chen, Tsu-Jae King Liu, and Vivek Subramanian, 2011 International Electron Device Meeting, 29.2.1-29.2.4, 2011.

50. "A New Candidate for High Performance Transparent Electronic Circuits: Sol-gel Based SnO2/ZrO2 Thin Film Transistors", Jaewon Jang, Rungrot Kitsomboonloha, and Vivek Subramanian, 2011 International Electron Device Meeting, 14.7.1-14.7.3, 2011

51. "Measurement, analysis, and modeling of 1/f noise in pentacene TFTs ", H. Kang and V. Subramanian, 2011 Large Area, Organic, and Printed Electronic Convention (LOPE-C), Frankfurt, Germany, June 2011.

52. "Inkjet Printed Heaters and Resistive Temperature Detectors for Biological Microfluidic Applications", Lakshmi Jagannathan, Samantha Cronier, Walter Li, Dwight Williams, Vivek Subramanian, 2011 Large Area, Organic,and Printed Electronic Convention (LOPE-C), Frankfurt, Germany, June 2011

53. "A comprehensive simulation study on metal conducting filament formation in resistive switching memories", F. Pan, S. Yin, and V. Subramanian, 3rd International Memory Workshop, May 22nd-25th, Monterey, CA, 2011.

54. "Rotational optical alignment for array based free space board-to-board optical interconnect with zero power hold", J. Chou, Y. Kyoungsik, T. Bakhishev, D. Horsley, T. Walmsley, S. Mathai, M. Tan, S.Y. Wang, V. Subramanian, M. Wu, 2010 IEEE 23rd International Conference on Micro Electro Mechanical Systems (MEMS), , pp.807-810, 24-28 Jan. 2010

55. "Electrical Characterization of close-packed ZnSe Nanoparticle Films", J. Jang, V. Subramanian, Materials Research Society Fall Meeting, December, 2010

56. "Synthesis, growth, and phase transitions in iron sulfide nanoparticles", J. Jang, V. Subramanian, Materials Research Society Fall Meeting, December 2010

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57. “Methodology for Inkjet Printing Partially Wetting Films”, D. Soltman, B. Smith, H. Kang, S. Morris, and V. Subramanian, IS&T Digital Fabrication conference, Austin, TX, Sept. 19-23, 2010.

58. “A Kinetic Monte Carlo study on the dynamic Switching properties of Electrochemical Metallization RRAMs during the SET Process”, F. Pan, V. Subramanian, The International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Bologna, Italy, Sept 6 – 8, 2010.

59. “A 2D Kinetic Monte Carlo simulation of resistive switching and filament formation in electrochemical RRAMs”, F. Pan and V. Subramanian, 2010 IEEE Device Research Conference.

60. “Highly-scale gravure-printed pBTTT organic field-effect transistors: Device characteristics and Bias Stability Analysis”, R. Kitsomboonloha, A. de la Fuente and V. Subramanian, 2010 Large Area Organic, and Printed Electronics Convention (LOPE-C), Frankfurt, Germany, June 2010.

61. “Downscaling of all inkjet printed, fully self-aligned organic circuits”, H-Y. Tseng and V. Subramanian, 2010 Large Area Organic, and Printed Electronics Convention (LOPE-C), Frankfurt, Germany, June 2010.

62. “Methodology for two dimensional pattern generation in inkjet printing”, D. Soltman and V. Subramanian, 2010 Large Area Organic, and Printed Electronics Convention (LOPE-C), Frankfurt, Germany, June 2010.

63. “Solution-Processed Non-volatile Filament Memory Based on ZnO Nanoparticle Films”, T. Bakhishev and V. Subramanian, 2010 Large Area Organic, and Printed Electronics Convention (LOPE-C), Frankfurt, Germany, June 2010.

64. “Printable Ag2O Cathodes for Silver-Zinc Batteries”, K. Braam, S. K. Volkman, and V. Subramanian, 2010 Spring meeting of the Materials Research Society, San Francisco, CA, April 2010.

65. “Ink-Jet Printed Conductors Based on Reduced Graphene Oxide”, T. Bakhishev, J. T. Robinson, P. E. Sheehan, Z. Wei and V. Subramanian, 2010 Spring meeting of the Materials Research Society, San Francisco, CA, April 2010.

66. “Hydrostatic concerns in inkjet-printed films”, H. Kang, D. Soltman, and V. Subramanian, 2010 Spring meeting of the Materials Research Society, San Francisco, CA, April 2010.

67. “Dielectric Breakdown and Kinetic Monte Carlo Simulation of Metal Filament Retention RESET Processes for Resistive Switches “, F. Pan and V. Subramanian, 2010 Spring meeting of the Materials Research Society, San Francisco, CA, April 2010.

68. “Considerations for pattern generation in inkjet-printed electronics”, Dan Soltman, Hongki Kang, Vivek Subramanian, SPIE Advanced Lithography, San Jose, CA, February, 2010

69. “All Inkjet Printed Self-Aligned Transistors and Circuits Applications”, Huai-Yuan Tseng and Vivek Subramanian, 2009 International Electron Device Meeting, Baltimore, MD., Dec, 2009

70. “Printed detection and resonant circuit for AM radio”, Jinsoo Noh; Namsoo Lim; Jaeyoung Kim; Subramanian, V.; Gyoujin Cho; IEEE International Symposium on Assembly and Manufacturing, pp.167-170, 17-20 Nov. 2009

71. “Optimization of inkjet-based process modules for printed transistor circuits”, Huai-Yuan Tseng, Shong Yin, Vivek Subramanian, Digifab, Louisville, KY, October 2009

72. “All Inkjet Printed Self-Aligned Transistors for Low Cost RFID Applications”, Huai-Yuan Tseng, Vivek Subramanian, 2009 IEEE Device Research Conference

73. “Printing and scaling of metallic traces and capacitors using a laboratory-scale rotogravure press”, Alejandro de la Fuente Vornbrock, Jau M. Ding, Donovan Sung, Huai-Yuan Tseng, Vivek Subramanian, 2009 Flexible Electronics and Display Conference, Phoenix, AZ, Feb 2-5, 2009.

74. “Effect of Pentacene Film Formation on Detection Behavior of Organic Transistor DNA Microarrays:, Lakshmi Jagannathan and Vivek Subramanian, Materials Research Society Fall Meeting, Boston, MA, Dec 1-4, 2008

75. “Microstructure of Pentacene Films from a Pentacene Precursor”, Daniel C Huang, Shong Yin, Kanan Puntambekar, Mike Toney and Vivek Subramanian, Materials Research Society Fall Meeting, Boston, MA, Dec 1-4, 2008

76. “Solution Processed Silver Sulfide Filament Memories”, Shong Yin and Vivek Subramanian, Materials Research Society Fall Meeting, Boston, MA, Dec 1-4, 2008

77. “The Dielectric-Integrated Monolayer Field Effect Transistor (DI-mFET)”, Kinyip Phoa and Vivek Subramanian, 2008 Semiconductor Research Corporation TechCon, Austin, TX, Nov 3-4, 2008.

78. “Pentacene Characterization for Optimum DNA Immobilization”, Lakshmi Jagannathan, Vivek Subramanian, 2008 Semiconductor Research Corporation TechCon, Austin, TX, Nov 3-4, 2008

79. “Effect of Pentacene Film Formation on Detection Behavior of Organic Transistor DNA Microarrays”, Lakshmi Jagannathan and Vivek Subramanian, Materials Research Society Fall Meeting, Boston, MA, Dec 1-4, 2008.

80. “Microstructure of Pentacene Films from a Pentacene Precursor”, Daniel C Huang, Shong Yin, Kanan Puntambekar, Mike Toney and Vivek Subramanian, Materials Research Society Fall Meeting, Boston, MA, Dec 1-4, 2008

81. “Experimental and Theoretical Studies for the Optimization of Polythiophene Gas Sensor Array”, F. Liao, V. Subramanian, 214th Meeting of The Electrochemical Society, Honolulu, HI, Oct 12-17, 2008.

82. “A Novel Solder Based on Metallic Nanoparticle Inks for Low-Temperature Packaging Technology”, T. Bakhishev and V. Subramanian, 2009 TMS Annual Meeting & Exhibition, San Francisco, CA, Feb 15-19, 2009

83. “Label-free low-cost disposable DNA hybridization detection systems using organic TFTs”, Qintao Zhang, Vivek Subramanian, 2007 IEEE International Electron Device Meeting, Washington DC, Dec 10-12, 2007.

84. “Printable DNA sensor using organic transistors”, Qintao Zhang and Vivek Subramanian, Transducers 2007, Lyon, France, 3EH5.P, 2007.

85. “Organic Transistors of Molecular Integrated Semiconductor-insulator Monolayer Films Using a Room Temperature Self-assembly Process”, Kanan Puntambekar, Kinyip Phoa, Vivek Subramanian, Amanda Murphy, Clayton Mauldin, Jean M. J. Frechét, Dean M. DeLongchamp, Daniel Fischer and Michael F. Toney, Materials Research Society Spring 2007 Meeting, O11.4, 2007.

86. “Stacked Low-Power Field-Programmable Antifuse Memories for RFID on Plastic”, B. Mattis, V. Subramanian, 2006 International Electron Device Meeting, 2006, 11.7

87. “A field-programmable antifuse memory for RFID on plastic”, B. Mattis and V. Subramanian, 2006 IEEE Device Research Conference, June 2006.

88. “Iodine-doped pentacene schottky diodes for high-frequency RFID rectification”, D. Huang and V. Subramanian, 2006 IEEE Device Research Conference, June 2006.

89. “Low-Voltage Inkjetted Organic Transistors for Printed RFID and Display Applications”, S. E. Molesa, A. de la Fuente Vornbrock, P. C. Chang, V. Subramanian, University of California Berkeley, Berkeley, CA, IEEE International Electron Device Meeting Technical Digest, pp. 5.4.1-5.4.4, 2005.

90. “Monolayer Formation in Oligothiophene Based OTFTs”, Paul Chang, Amanda R. Murphy, Jean M. J. Frechet and Vivek Subramanian, 2005 Materials Research Society Fall Symposium, Paper M7.7, Boston MA, December, 2005.

91. “A novel high-Q printed inductor technology for RFID applications”, David Redinger and Vivek Subramanian, 2005 Materials Research Society Fall Symposim, Paper M8.7, Boston MA, December 2005.

92. “Solution-processed ZnO nanowire-network thin film transistors for transparent electronics”, Teymur Bakhishev, Steven K Volkman and Vivek Subramanian, 2005 Materials Research Society Fall Symposium, Paper DD5.5, Boston MA, December, 2005.

93. “Polythiophene Thin-film Transistor Array for Gas Sensing”, J. B. Lee, M. Heeney, S. Tierney, I. McCulloch, A. Murphy, J. Liu, J. Frechet, and V. Subramanian, 63rd IEEE Device Research Conference Digest, Vol 1, pp. 147-148, 2005.

94. “Measuring Structure and Order Development in Organic Semiconductor Films with Soft X-Ray Spectroscopy”, D. M. DeLongchamp, E. K. Lin, D. Fischer, S. Sambasivan, B. M. Vogel, J. M. J. Frechet, V. Subramanian, and A. R. Murphy, 2005 Annual AIChE Meeting, Cincinnati, OH, Oct 31 – Nov1, 2005.

95. “A high-performance all-inkjetted organic transistor technology”, Steven E. Molesa, Steven K. Volkman, David R. Redinger, Alejandro de la Fuente Vornbrock, and Vivek Subramanian, 2004 IEEE International Electron Device Meeting Technical Digest, pp. 1072, 2004.

96. “A novel transparent air-stable printable n-type semiconductor technology using ZnO nanoparticles”, Steven K. Volkman, Steven E. Molesa, Josephine B. Lee, Brian A. Mattis, Alejandro de la Fuente Vornbrock, Teymur Bakhishev, and Vivek Subramanian, 2004 IEEE International Electron Device meeting Technical Digest, pp. 769, 2004.

97. “Structure and order development in organic semiconductor films”, Dean M DeLongchamp, Erin Jablonski, Sharadha Sambasivan, Daniel Fischer, Eric K Lin, Steven Volkman, Paul Chang, Vivek Subramanian, 2004 Annual AIChE Meeting, Austin, TX, Nov 7-12, 2004.

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AMD v. Realtek
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98. ***Best paper award*** "Single-monolayer inkjetted oligothiophene organic TFTs exhibiting high performance and low leakage", P. C. Chang,, S. E. Molesa, A. R. Murphy, J. M. J. Fréchet, and V. Subramanian, 62nd IEEE Device Research Conference Conference Digest, Pages 183 - 184 vol.1, 2004.

99. "High-performance inkjet-printed pentacene transistors for ultra-low-cost RFID applications.", Steven Molesa, Mark Chew, David Redinger, Steven K Volkman, and Vivek Subramanian, 2004 Mat. Res. Soc. Spring Meeting

100. "Ink-Jetted Silver/Copper Conductors for Printed RFID Applications", Steven K. Volkman, Yunan Pei, David Redinger, Shong Yin, and Vivek Subramanian, Flexible Electronics 2004—Materials and Device Technology, edited by Norbert Fruehauf, Babu R. Chalamala, Bruce E. Gnade, and Jin Jang (Mater. Res. Soc. Symp. Proc. 814, Warrendale, PA , 2004), I7.8

101. "The role of film thickness in organic thin film transistor gas sensors", Christopher Chen, Frank Liao, and Vivek Subramanian, 2004 Mat. Res. Soc. Spring Meeting.

102. "Organic TFT Gas Sensors for Electronic Nose Applications", Frank Liao, Chris Chen, and Vivek Subramanian, 2004 Mat. Res. Soc. Spring Meeting.

103. "10nm organic FETs: scaling phenomena and characterization", Josephine Lee, Paul Chang, Alex Liddle, and Vivek Subramanian, 2004 Mat. Res. Soc. Spring Meeting.

104. "Nanoscale Patterning of Organic and Molecular Electron Devices through Radiation-induced Film Modification", Brian Alexander Mattis, Yunan Pei and Vivek Subramanian, 2004 Mat. Res. Soc. Spring Meeting.

105. "Crystalline Organic Semiconducting Thin Films Cast From a Novel Thermolytic Thiophene Oligomer", Paul C. Chang, Amanda R. Murphy, Josephine B. Lee, Jean M.J. Fréchet, and Vivek Subramanian, Flexible Electronics 2004—Materials and Device Technology, edited by Norbert Fruehauf, Babu R. Chalamala, Bruce E. Gnade, and Jin Jang (Mater. Res. Soc. Symp. Proc. 814, Warrendale, PA , 2004), I12.4.

106. "Measurements of the transient photoconductivity of single crystals of pentacene", C. Weber, M. Langner, J. Orenstein, T. Le, V. Subramanian, V. Butko, A. Ramirez, American Physical Society, Annual APS March Meeting 2003, March 3-7, 2003, , abstract #Y16.015

107. "Organic transistors on fibers: A first step towards electronic textiles", Josephine B. Lee and Vivek Subramanian, IEEE International Electron Device Meeting Technical Digest, pp. 8.3.1, 2003.

108. "Inkjetted Passive Components on Plastic Substrate for RFID", D. Redinger, R. Farshchi, and V. Subramanian, 2003 IEEE Device Research Conference Conference Digest, pp. 187-188, 2003.

109. "Effect of Thermal Cycling on performance of poly(3-hexyl)thiophene transistors", B. Mattis, P. Chang, and V. Subramanian, Proceedings of the Materials Research Society Spring 2003 meeting, Symposium: Organic and Polymeric Materials and Devices, Editors: Paul W.M. Blom, Neil C. Greenham, Christos D. Dimitrakopoulos, C. Daniel Frisbie, MRS Proceedings Volume 771, L10.35, 2003.

110. "High-quality inkjet-printed multilevel interconnects and inductive components on plastic for ultra-low-cost RFID applications", S. Molesa, D. Redinger, D. Huang, and V. Subramanian, Proceedings of the Materials Research Society Spring 2003 meeting, Symposium H: Flexible Electronics--Materials and Device Technology, Editors: Norbert Fruehauf, Babu R. Chalamala, Bruce E. Gnade, Jin Jang, MRS Proceedings Volume 769, H8.3, 2003.

111. "Inkjetted organic transistors using a novel pentacene precursor", S. Volkman, S. Molesa, B. Mattis, P. C. Chang, and V. Subramanian, Proceedings of the Materials Research Society Spring 2003 meeting, Symposium H: Flexible Electronics--Materials and Device Technology, Editors: Norbert Fruehauf, Babu R. Chalamala, Bruce E. Gnade, Jin Jang, MRS Proceedings Volume 769, H11.7, 2003.

112. "Flexonics", J. Canny, J. Risner, and V. Subramanian, presented at The Fifth International Workshop on Algorithmic Foundations of Robotics, 2002.

113. "Inkjetted gold conductors for electronics on plastics", Daniel C. Huang, Frank Liao, and Vivek Subramanian, presented at Materials Research Society Spring 2002 meeting.

114. "Applications of Printing Technology in Organic Electronics and Display Fabrication", V. Subramanian, presented at the Half Moon Bay Maskless Lithography Workshop, DARPA/SRC, Half Moon Bay, CA, Nov 9-10, 2000.

115. "A 20 nm Gate-Length Ultra-Thin Body p-MOSFET with Silicide Source/Drain", J. Kedzierski, P. Xuan, V. Subramanian, E. Anderson, J. Bokor, T.-J. King, and C. Hu, presented at the Silicon Nanolectronics Workshop 2000.

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AMD v. Realtek
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116. "60nm Planarized Ultra-thin Body Solid Phase Epitaxy MOS-FETs", P. Xuan, J. Kedzierski, V. Subramanian, J. Bokor, T-J. King, C. Hu, 58th Annual Device Research Conference Digest, Pages 67 – 68, 2000.

117. "High performance 200nm single-grain TFTs fabricated using a self-aligned germanium seeding technology", P. Kalavade, A. R. Joshi, V. Subramanian and K. C. Saraswat, presented at the 2000 Materials Research Society Spring Symposium.

118. "Nanoscale SiGe-Channel Ultra-Thin-Body Silicon-on-Insulator P-MOSFETs", Y-C. Yeo, V. Subramanian, J. Kedzierski, P. Xuan, T-J. King, J. Bokor, and C. Hu, presented at the 1999 International Semiconductor Device Research Symposium.

119. "Ultra-thin body SOI MOSFET for Deep-sub-tenth Micron Era", Y-K. Choi, K. Asano, N. Lindert, V. Subramanian, T-J. King, J. Bokor and C. Hu, 1999 IEEE International Electron Device Meeting Technical Digest, pp. 919-921, 1999.

120. "Sub 50-nm FinFET: PMOS", X. Huang, W-C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y-K. Choi, K. Asano, V. Subramanian, T-J. King, J. Bokor and C. Hu, 1999 IEEE International Electron Device Meeting Technical Digest, pp. 67-70, 1999.

121. "A bulk-Si-compatible ultrathin-body SOI technology for sub-100nm MOSFETs", V. Subramanian, J. Kedzierski, N. Lindert, H. Tam, Y. Su, J. McHale, K. Cao, T-J. King, J. Bokor, and C. Hu, Proceedings of the 57th Annual Device Research Conference, pp. 28-29, 1999.

122. "Process issues for deep-submicron electron beam lithography at the Stanford Nanofabrication Facility", V. Subramanian and M. King, Electron Beam Lithography for Nanostructure Fabrication Workshop, Cornell University, Ithaca, NY, January 14-15, 1999.

123. "Laterally Crystallized Polysilicon TFTs Using Patterned Light Absorption Masks", V. Subramanian and K. C. Saraswat, Proceedings of the 55th Annual Device Research Conference, 1997, pp. 54-55.

124. "A Novel Technique for 3-D Integration: Ge-seeded Laterally Crystallized TFTs", V. Subramanian and K. C. Saraswat, 1997 Symposium on VLSI technology Digest of Technical Papers, 1997, pp. 97-98.

125. "Response surface characterization of the deposition of LPCVD SiGe for solid-phase crystallized poly-TFTs", V. Subramanian, K. C. Saraswat, H. Hovagimian, and J. Mehlhaff , Proceedings of the Second International Workshop in Statistical Metrology, 1997, pp. 94-97.

126. "Design and Characterization of SiGe TFT Devices and Process using Stanford's Test Chip Design Environment", M. V. Kumar, V. Subramanian, K. C. Saraswat, J. D. Plummer, and W. Lukaszek, Proceedings of the 1997 IEEE International Conference on Microelectronic Test Structures, pp. 143-145.

127. "Response surface optimization for high-performance solid-phase crystallized silicon-germanium thin film transistors", V. Subramanian, K. C. Saraswat, H. Hovagimian, and J. Mehlhaff, Proceedings of the SPIE - The International Society for Optical Engineering, vol.3014, p. 127-32, 1997.

128. "Optimization and Modeling of Silicon-Germanium Thin Film Transistors for AMLCD Applications using a Plackett-Burman Experimental Design V. Subramanian, K. C. Saraswat, H. Hovagimian, and J. Mehlhaff, First International Workshop on Statistical Metrology, Honolulu, Hawaii, June 9, 1996

129. "Accelerated Breakdown in Thin Oxide Films due to Interfacial Stress and Carrier Depletion", V. Subramanian, N. Bhat, and K. C. Saraswat, Materials Reliability in Microelectronics VI, MRS Symposium proceedings, 1996, pp. 323-328

130. "A Novel Technique for In-Situ Monitoring of Crystallinity and Temperature during Rapid Thermal Annealing of Thin Si/Si-Ge films on Quartz/Glass", V. Subramanian, L. Degertekin, P. Dankoski, B. T. Khuri-Yakub, and K. C. Saraswat, Flat Panel Display Materials II, MRS Symposium, pp.267-72, 1996.

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