

Benefits and Costs of Power-Gating Technique

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Abstract

Power-gating is a technique for saving leakage power by shutting off the idle blocks. However, without good understanding and careful design, negative effects of power gating may overwhelm the potential gain and may make the technique not worth the effort. In this paper, we report on our study of the benefits and costs of the power-gating technique in terms of power, area, and performance. We model and analyze several strongly related parameters such as sleep-transistor size, decap area, and supply voltage level. We also report on our experiments to demonstrate how the gated area, circuit behavior and power mesh granularity affect the power gating technique at the system level. Experimental results show that, by compromising 4% of the total area and 5% of the dynamic power, we can achieve 47% leakage power saving while maintaining the same performance. With technology scaling down, the saving is significant. We conclude that we can benefit from the power-gating technique in future technology nodes.

1. Introduction

With the advent of portable electronic devices and high density VLSI circuits, power dissipation has emerged as a major design concern. Simultaneously, technological advances result in shrinking of the minimum feature size as well as in lowering of the supply and threshold voltages which cause a dramatic increase of the leakage current. Leakage power has now become a major component of the total power dissipation in CMOS circuits[6][9].

Power-gating is a technique for reducing leakage power by shutting off the idle blocks. Implementation of power-gating requires a multi-threshold CMOS process. Logic blocks are implemented using low- V_t , high-performance transistors whereas high- V_t transistors (called sleep transistors) connect the gated blocks to the power supply [1]. Power-gating

is not a cost-free technique. Negative effects include a combination of noise, performance penalty, area and power overhead, etc. In this paper, we study and quantify the benefits and costs of the power-gating technique in terms of area and power. We also consider the impact of scaling trends on the applicability of power gating. In [2], the authors evaluate limitations and power-savings of three leakage-power reduction techniques and address the outlook for scaling technology. However, although they mention sleep transistors, the focus of the paper is on using phase-locked loops (PLLs) as voltage regulators to gate power supply. The phenomena occurring in circuits power-gated with sleep transistors are not addressed in that work. Moreover, the studies are performed on small test circuits (such as 32-bit 2-input NOR gate) which may not capture all the phenomena of a system-level power-gating technique. To the best of our knowledge, our work is the first one addressing the system-level trade-off in sleep-transistor-based power-gating technique.

The remainder of this paper is organized as follows. In section 2, we briefly introduce the costs and benefits of a sleep-transistor-based power-gating technique. In section 3, we characterize and model each effect in detail, explaining the simulation flow used to evaluate the trade-off. In section 4 we show the experimental results and scaling trend. Section 5 concludes the work.

2. Comparison two power supply systems

Here we consider a standard chip (Fig1(a)) and a power-gated chip (Fig1(b)) both implementing the same functionality. In the standard chip, all logic circuits are connected to Vdd through a hierarchical power mesh. The entire chip is fully powered at all times. In the power-gated chip, we have local power meshes for all macros, and sleep transistors are used to connect the local mesh to the global mesh.

When a macro is active, the sleep transistor is turned on. Its size must be large enough to guarantee that the current drawn by the macro does not cause excessive voltage drop. If we want to maintain the same performance with and without power-gating, in the gated chip the V_{dd} has to be raised by $\pm V$ to counteract the voltage drop across the sleep transistor. However, increasing the supply voltage increases the dynamic and leakage power consumption, which may nullify the intended power savings.

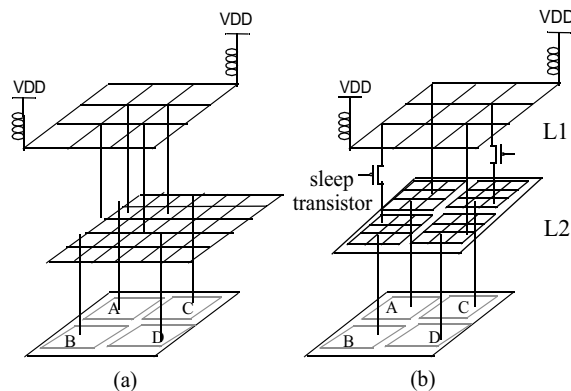


Figure 1. Power supply system (a) normal power supply system (b) power-gating system

Also, when sleep transistors are turned on and off, considerable power supply currents are drawn in a short period of time, which may result in large voltage fluctuations on the power grid. This *power-gating noise (PGN)* affects the reliability of systems-on-chips (SoCs), especially for advanced CMOS technologies with narrow noise margins. We need to add extra decoupling capacitance (decap) to reduce the *PGN* and take into account the additional leakage currents associated with the intentionally introduced capacitors. At the same time, the switching sleep transistors consume more dynamic power.

In a chip without power-gating, the non-switching part of the circuit serves as a decoupling capacitor and reduces the power grid noise. However, in the power-gated chip, the gated macros are disconnected from the power supply during their idle state, which prevents them from acting as a decap for the active circuit. Thus the non-gated macros adjacent to the gated circuitry may need extra decap to guarantee that power grid noise remains within tolerable

margins. The gated macros not only stop providing decap to other macros, but also act as an obstacle for decap insertion. Extra decap will enlarge the chip size and again consume more leakage power.

We will now consider the chip shown in Fig.1. Region I contains the gated macros B and C, whereas region II consists of ungated macros A and D. We qualitatively compare the leakage, dynamic power, decap and sleep transistor area of those two regions. We normalize the data to that of an ungated chip which realizes the same functionality as the gated chip. The trade-off in terms of power and area for power-gating systems can be summarized in Table.1.

Table 1. Power-gating vs. non-power-gating

	non-power-gating chip region		power-gated chip region	
	I	II	I	II
P(leakage)	1	1	↓	↑
P(dyn)	1	1	↑	↑
Area(decap)	1	1	1	↑
Area(st)	N/A	N/A	↑	N/A

We notice that the benefit comes only from saving in the leakage power of gated circuits, and the costs include: 1) area consumed by the extra decap and sleep transistors; 2) dynamic power of both regions and leakage consumption of non-gated circuit and decaps. In our study, we will attempt to quantify these benefits and costs.

3. Characterization of power gating technique

3.1. Power-gating modeling

The power-gating model is shown as Fig.2. The upper power mesh can be modeled as a linear RL network excited by constant voltage sources. The lower power mesh is composed of a linear RC network excited by time-varying current sources which represent the switching currents drawn by the logic circuits. We use a simple triangle waveform to model the current profiles. C is the on-chip decou-

pling capacitor which is provided by the non-switching part of the logic circuit.

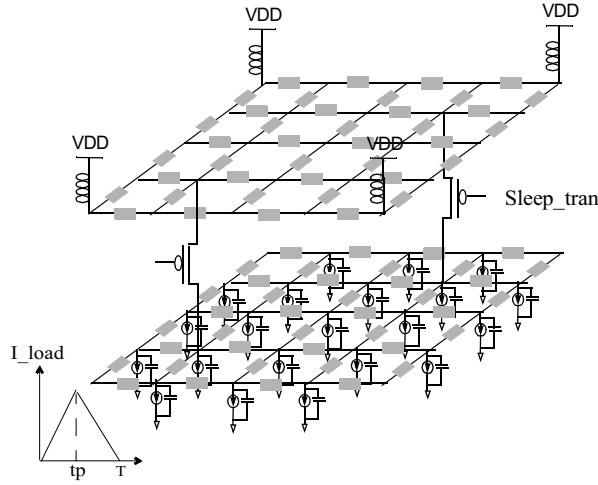


Figure 2. Power gating modeling

In the traditional power network analysis for the ungated chip, sleep transistors are replaced by vias (resistors). So the entire system is a linear RLC network excited by the voltage and current sources. The modified Nodal Analysis (MNA) formulation can be used to solve this system. However, when sleep transistors are introduced, the power network is no longer linear. We use HSPICE to simulate the power-gating noise at the moment the sleep transistors are turned on and off; and we use ALSIM, the IBM linear power network analyzer, to simulate the voltage delivery behavior when sleep transistors are on and can be modeled as resistances.

3.2. Sleep-transistor sizing

In our model, we assume distributed sleep transistors, one per gated block. When sleep transistors are absent, the delay of a single gate can be approximated by [3]

$$T_d = \frac{C_L V_{dd}}{|V_{dd} - V_{tL}| \zeta} \quad (\text{EQ 1})$$

where C_L is the load capacitance at the gate's output, V_{tL} is the threshold voltage in the low V_t block, and ζ is the velocity saturation index for modeling short channel effects [4]. In the presence of a sleep transistor, the gate propagation delay increases to

$$T_d^{ST} = \frac{C_L / V_{dd} - V_{ST} 0}{|V_{dd} - V_{ST} - V_{tL}| \zeta} \quad (\text{EQ 2})$$

where V_{ST} is the voltage drop on the sleep transistor. To eliminate the performance loss caused by the sleep transistor, V_{dd} has to be increased to V_{dd}^{ST} such that

$$\frac{C_L V_{dd}}{|V_{dd} - V_{tL}| \zeta} = \frac{C_L / V_{dd}^{ST} - V_{ST} 0}{|V_{dd}^{ST} - V_{ST} - V_{tL}| \zeta} \quad (\text{EQ 3})$$

We assume $\zeta = 1$ and define *supply increase ratio* as

$$\xi = \left(\frac{V_{dd}^{ST}}{V_{dd}} - 1 \right) \quad (\text{EQ 4})$$

and we get

$$V_{ST} = \xi V_{dd} \quad (\text{EQ 5})$$

The sleep transistor operates in its linear region and the current can be expressed as

$$I_{ST} = \sigma_p C_{ox} \left(\frac{W}{L} \right)_{ST} \left[|V_{dd}^{ST} - V_{tH}| V_{ST} - \frac{V_{ST}^2}{2} \right] \quad (\text{EQ 6})$$

Substituting for V_{ST} , the size of sleep transistors can be expressed as

$$\left(\frac{W}{L} \right)_{ST} = \frac{I_{ST}}{\sigma_p C_{ox} \xi V_{dd} / V_{dd}^{ST} - V_{tH} - 0.5 \xi V_{dd}} \quad (\text{EQ 7})$$

where V_{tH} is the threshold voltage of the sleep transistor. The total sleep transistors' size of one gated block can be approximated by

$$\frac{I_{MAX}}{\sigma_p C_{ox} \xi V_{dd} / V_{dd}^{ST} - V_{tH} - 0.5 \xi V_{dd}} \quad (\text{EQ 8})$$

where I_{MAX} is the *maximum switching current* generated by the gated circuit.

We notice that the sleep transistor size is related to the increased V_{dd} . Thus the higher the supply voltage, the smaller the required sleep transistor; but also the more power consumed. Performance can be traded also. If we allow some performance loss (PL), supply voltage may not necessarily increase. These parameters should be decided according to design requirements.

3.3. Power saving vs. cost

The purpose of power-gating is to save leakage power when blocks are idle. However, power-gating itself incurs power cost. If that cost is comparable or even larger than the savings, then the power-gating technique is not worth the effort. The work reported in [5] estimates the minimum idle time when considering the overhead associated with the leakage reduction technique. However, if the supply voltage is increased to counteract the performance loss of power-gating, as analyzed in section 3.2, the minimum idle time is no longer sufficient to characterize the trade-off between the cost and benefit.

Fig.3(a) depicts the circuit's power gating schedule. t_{sleep} is the sleep time, t_{active} is the active time, t_r and t_f are the transition times. We have two power supply schemes: (a) power-gating and (b) no-power-gating. Circuits are divided into two regions (I) consisting of gated circuits and (II) of non-gated circuits. Fig.3 (b)-(e) shows the power comparisons in particular regions. The dark line illustrates the power consumed in the power-gated chip, and the light line indicates power consumed in the ungated chip. From the comparisons, we get the leakage power saving $+P_1$ in region I; the leakage power overhead $+P_2$, and dynamic power overhead $+P_3$ in region II

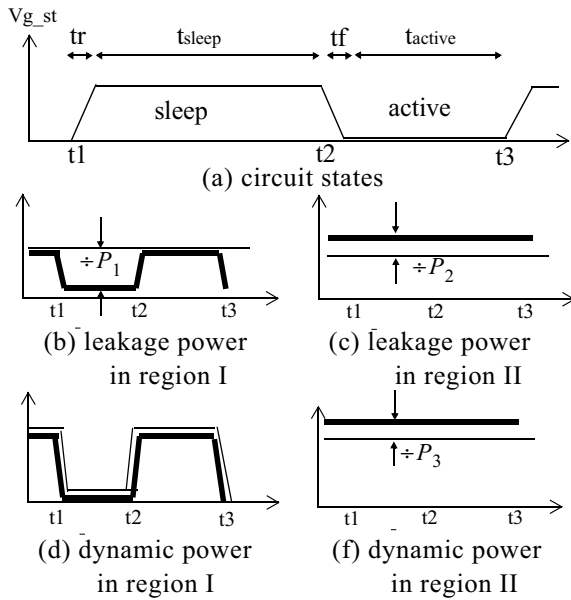


Figure 3. Power saving and cost

We define E_{tr} and E_{tf} to be the energies dissipated by sleep transistor during the time periods t_r and t_f . To make the power-gating scheme worthwhile, the power balance must satisfy the following inequality:

$$+P_1 \{t_{sleep}\} + P_2 + P_3 \{t_{sleep} + t_{active}\} + E_{tr} + E_{tf} \quad (\text{EQ 9})$$

From Eq.9, we note that not only should the sleep time be long enough, but also the active time cannot be longer than a certain period. We define an active ratio:

$$\zeta = t_{active} / t_{sleep}$$

The designer can select the value of ζ and observe power saving as a function of t_{sleep} . The waveform will reach a maximum saving value after

a certain value of t_{sleep} . We can also fix t_{active} to explore the effect of ζ .

3.4. Power estimation

3.4.1. Dynamic power, Dynamic power is consumed by the switching of the circuit and of the sleep transistor. The dynamic power consumed by the circuit as

$$P_{dynamic}^{ckt} = \sum_{k=1}^N C_{gk} f^2 V_{dd}^2 S \quad (\text{EQ 10})$$

where C_{gk} is the capacitance of the k th gate, which is also the load capacitance of its parent gate. S is an empirically determined switching factor characterizing the circuit's switching activity. f is the operating frequency and V_{dd} is the supply voltage. In this paper, we focus only on relative comparisons rather than precise calculations; our estimations are rough but sufficient to observe the trends. For more accuracy, we can perform logic simulation, obtain switching probabilities of each gate and use individual weights S_k on each C_{gk} .

The dynamic power consumed by the sleep transistor is obtained from HSPICE on a simple model shown in the Fig.4. C_{DS} is the total drain-source capacitance of the non-switching part of the gated circuit. A step signal V_g is applied to trigger the sleep transistor. HSPICE reports the average power dissipation P_{avr} during the time T . To get $E_{st} = E_{tr} + E_{tf}$ (Section 3.3), we have

$$E_{st} = P_{avr} T. \quad (\text{EQ 11})$$

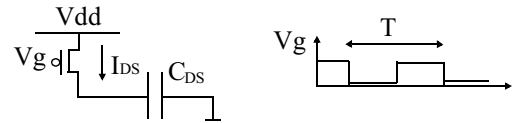


Figure 4. The model for dynamic power

3.4.2. Leakage power, There are two major leakage mechanisms in scaled devices: subthreshold leakage I_{sub} and gate leakage I_g . [10]. Both of these leakage components are increasing very rapidly with technology scaling. Furthermore, to get sufficiently large capacitance, decaps are usually made from thin gate-oxide MOS transistors with long and wide channels. These decaps will leak more as technology continues scaling down.

Circuit leakage is caused by two mechanisms: gate-leakage and decap-leakage. Gate-leakage characterizes the leakage of logic gates and is input-pat-

tern-dependent. Decap leakage is pattern-independent. We use HSPICE to simulate the average leakage for a variety of standard cells used in circuits. Probability of pattern occurrence should be weighted in simulation. To compute the decap leakage, we run simulations and determine the unit leakage per σm^2 . The total leakage of a circuit is estimated as

$$I_{leak} = \frac{1}{1-S} \sum_{i \in allgates} I_i^{gate} + I_{unit}^{decap} (WL) \quad (EQ 12)$$

where WL is total decap area, S is the empirical switching factor. Leakage power is expressed as

$$P_{leak} = V_{dd} I_{leak} \quad (EQ 13)$$

When supply voltage increases, I_{leak} will increase exponentially

$$I_{sub} = I_0 \exp\left(\frac{q(V_{gs} - V_T)}{nT_t}\right) \left(1 - \exp\left(\frac{-V_{ds}}{V_t}\right)\right) \quad (EQ 14)$$

where $I_0 = \sigma_0 C_{ox} \frac{W}{L} V_t e^{1.8}$, V_t is the thermal voltage, and n is the subthreshold slope coefficient.

3.5. Decap insertion

Power grid noise is caused by simultaneous switching of the core logic and I/O buffers. Sleep transistors introduce power-gating noise when they are switching on and off. By adding decoupling capacitors, we can dramatically reduce both power gating noise and simultaneous switching noise. Decaps come from on-chip non-switching capacitors C_{ckt} or thin-oxide capacitors C_{ox} which are purposely inserted. The on-chip decap is extracted from each logic block and is known before floorplanning. If C_{ckt} is not sufficient for noise immunity, more C_{ox} s are added. We model the C_{ox} insertion as illustrated in Fig.5. Decap can be added peripherally around a block (Fig.5. b) or can be evenly distributed within the block (Fig.5. c).

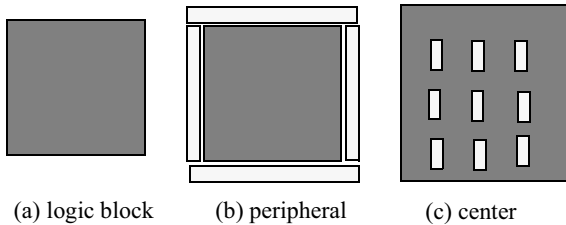


Figure 5. Decap insertion

We apply a greedy algorithm to implement decap insertion:

- 1 Given a set of blocks with their areas, minimum and maximum height/width ratios, and the switching current profiles modeled as piece-wise-linear functions, we apply floorplanning.
- 2 After floorplanning, we know each block's location and the topology of power grid. We simulate the whole chip and obtain the noise distribution. We determine a grid node P on which the worst-case noise occurs.
- 3a (*Peripheral insertion*) The boundary decap tile is considered as a pure capacitance block. For a node P , we calculate the noise sensitivity to decap placed on every side of each block: $\frac{\epsilon}{C_{ij}} V_{noise} / p0$, $i = 13 * N$
 $j = 1323334$. N is the total number of blocks in the chip. j represents four sides of a block. C_{ij} is a decap added to the i th block, on the j th side. We insert decap to a block and size which results in maximum elimination of noise.
- 3b (*Central insertion*) We calculate the noise sensitivity to decap of each block for node P : $\frac{\epsilon}{C_i} V_{noise} / p0$. We select the one resulting in the greatest noise reduction and insert decap into the corresponding block.
- 4 We simulate the chip with added decap to update the noise distribution. If the worst case noise is already within the noise margin, we go to step 5; otherwise, back to step 3.
- 5 We update the area of each block with inserted decaps and apply a refinement floorplanning (with hard blocks) to adjust the blocks' location.

3.6. Simulation flow

Our complete simulation flow is shown in Fig.6. We begin with a set of blocks and perform the initial floorplanning. Next we follow two branches. One is for the regular power supply chip and the other is for the power-gated chip. In the former one, we do the power grid noise analysis and decap insertion to keep the noise within the margin. In the latter one, we first size the sleep transistors and increase V_{dd} to ensure the same performance. Power grid noise analysis combined with decap insertion are per-

formed to meet the noise margin. Finally, we compare the saving and overhead of those two designs.

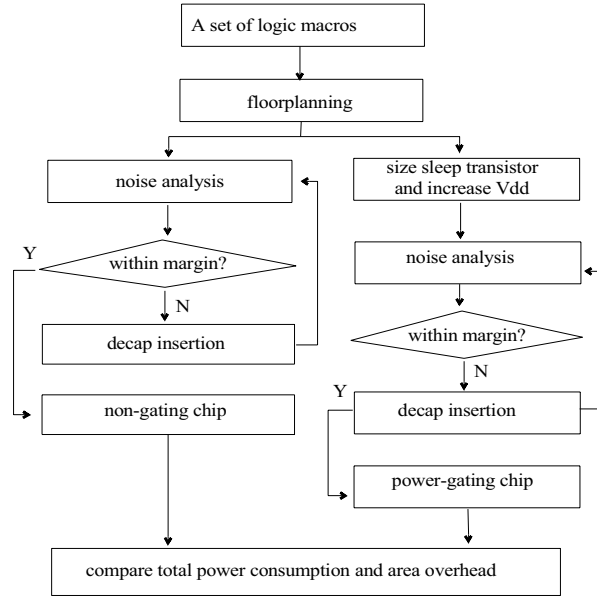


Figure 6. Evaluating power-gating technique

4. Experiments

We implement 26 circuits (from MCNC and ISCAS benchmarks respectively) as the basic logic blocks. The initial floorplan of those blocks is shown as in Fig.7.

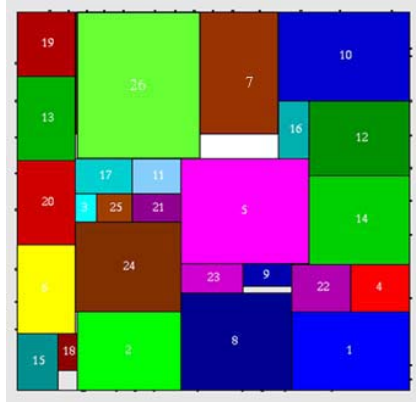


Figure 7. Floorplan of 26 circuits(1x0.9mm²)

For each block, we collected following data from standard cell library and simulation:

C_l : loading capacitance, for dynamic power estimation;

$I_{profile}$: current profile, for noise analysis;

I_{leak} : leakage current, for leakage power estimation;

C_{decap} : decoupling capacitance, for noise analysis and power estimation.

We used Tcl programming language to develop our simulation flow, which includes HSPICE and ALSIM. We ran all the experiments on a P4 2.4GHz PC with Linux. The test circuits were first implemented in 0.13 σ m technology. The temperature was 25 $\forall$ C.

1. Power-gating vs. no-power-gating

In this experiment, we gated half of the circuits (blocks whose geometric centers were on the left half of the chip) and compared it with non-power-gated chip in terms of power and area. Table.2 shows the parameters of the initial chip. The noise is beyond the acceptable margin (we assume 10% of Vdd), so decap insertion is necessary. We implement both center decap insertion and peripheral decap insertion.

Table 2. Initial chip

Vdd(V)	Vnoise(V)	Cload(pF)	P_dyn(mW)	P_leak(mW)
1.5	0.25	398	143	13.7

Table 3. Comparison between w/ and w/o power-gating

		no-gating	power-gating	b/c(%)
Center Decap Insertion	Vdd(V)	1.5	1.54	
	ST(%)	0	4	-4
	Decap(pF)	481	529	
	(%)	2.4	2.66	-0.2
	Pdyn(mW)	143	150	-4.98
Peripheral Decap Insertion	Pleak(mW)	13.9	7.75	44.24
	Vdd	1.5	1.54	
	ST(%)	0	4	-4
	Decap(pF)	567	850	
	(%)	2.85	4.21	-1.36
	Pdyn(mV)	143	150	-4.98
	Pleak(mV)	14.0	8.89	+36.5

The comparison results are reported in Table 3. Vdd is increased to 1.54V to meet the same target frequency. The relative area overheads introduced by the sleep transistors and decaps are listed in rows 3, 5, 9 and 11. The last column indicates the benefit (positive number) and cost (negative number) of the power-gating technique. For example, for the center decap insertion strategy, by compromising 4.2% area and 4.98% dynamic power, we can achieve 44.24% saving in leakage power. Experimental

results show that, in general, the center decap insertion is better than the peripheral one.

We note that the energy consumed by switching of sleep transistors (which is around 7.5nJ) is not counted in the dynamic power calculation reported in Table 3. Generally speaking, we need to use Eq.9 to decide when savings are possible. However, in this case the absolute cost of dynamic power (7mW) exceeds the absolute saving of leakage power(6.15mW), so the total power cannot be saved. In a later experiment, however, we will see that with technology scaling down, power-gating to reduce leakage does save the total power.

2. Gating-effects vs. gated-area

We did a study on the impact of gated area on gating effects. First, we built a chip whose current distribution was uniform. Then we varied the ratio of gated to non-gated area from 20% to 100%, as shown in Fig.8. Table 4 summarizes the results. All the data have been normalized to the ungated system. Leakage power decreases with increase in gated-to-ungated ratio. The interesting thing is that the area overhead and the dynamic power overhead do not keep increasing. The reason is as follows: First, as the gated area increases, the sleep transistor size is increasing. More efforts, such as increasing Vdd and inserting decap, are required to counteract its impact on the active circuits. However, at the same time that the area of the active circuits is decreasing, their impact begins to diminish. This means that after reaching a certain gating ratio, we begin saving at an increasing rate.

Figure 8. Fated circuits in grey area

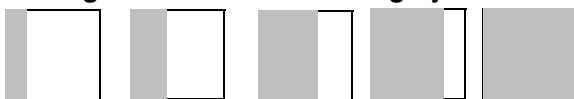


Table 4. Gated-area vs. gating-effects

gated area		20%	40%	60%	80%	100%
Area	NG	1	1	1	1	1
	G	1.03	1.05	1.16	1.16	1.15
P dynamic	NG	1	1	1	1	1
	G	1.02	1.04	1.06	1.04	1.02
P leakage	NG	1	1	1	1	1
	G	0.73	0.66	0.53	0.29	0.08

3. Gating-effect vs. gated-circuits

In this experiment, we studied the effect of circuit behavior on the power-gating result. We re-floorplanned the 26 logic blocks in such a way that

big-current drawing blocks were placed in region B, and small current-drawing blocks in region S, as shown in Fig.9. Then we gated one region and kept the other active. The comparisons are shown in Table.5. In general, gating big current-drawing blocks saves more leakage power but at a higher overhead cost of area and dynamic power.

Figure 9. Circuits have different behavior in different regions

S	B
B	S

Table 5. Gated circuits with different behavior

	ST(%)	Decap	P_dynamic	P_leakage
NG	N/A	1	1	1
gate_B	7	1.14	1.06	0.42
gate_S	3	1.06	1.04	0.73

4. Gating-effect vs. power-mesh-granularity

In this experiment, we studied the impact of the power mesh granularity on power-gating result. We kept the area of power mesh constant and changed the width of horizontal and vertical segments. Fig.10 shows power meshes of various granularity. We used meshes of several granularities on the same gated system. Fig 11 shows the decap insertion results for such meshes. $M \times N$ stands for a mesh of m rows and n columns. The y-axis data is normalized to the ungated system. The stable curve implies that if we keep the power mesh area constant, the noise incurred by power-gating does not change much with mesh granularity.

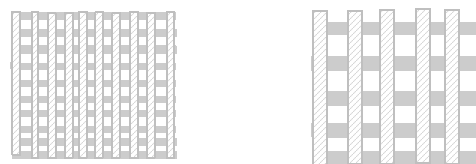


Figure 10. Power mesh granularity

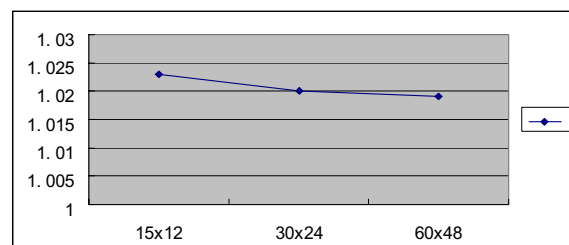


Figure 11. inserted decap

5. Technology trends

Fig 12 shows how technology affects power-gating. We observe that dynamic power decreases and leakage power increases for technology moving 130nm to 70nm. The difference in leakage power between power-gated and ungated systems is becoming larger than the difference in dynamic power, which implies a promising future for the power-gating technique. At the same time, we note that the power density is increasing for both power-gated and ungated systems, as shown in Fig 13, but the growth is slower for the power-gated chips than for the ungated, which suggests that in the future the low-power designs will favor the power-gating techniques.

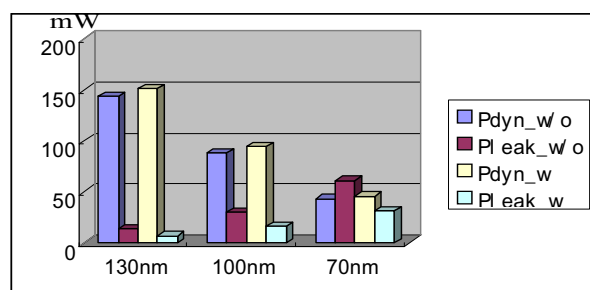


Figure 12. Technology trend

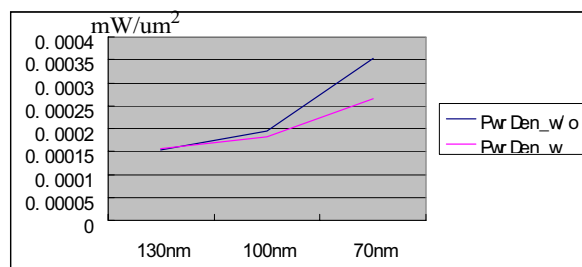


Figure 13. Power density

5. Conclusions

In this paper, we have discussed the findings of our studies on the benefits and costs incurred by the power-gating technique. We demonstrated that there are several components strongly related to power-gating, such as sleep transistor size, decap area, and supply voltage V_{dd} level. We modeled these components and analyzed the effects they caused. We showed experimentally how the gated area, circuit behavior and power mesh granularity affect the power budget of the gating technique at the system level. Our experimental results show that, by com-

promising the 4% of total area and 5% of the dynamic power, we can reduce leakage power by 47% while keeping the same performance. With technology scaling down, the absolute value of power saving will out weigh the absolute value of power cost. Therefore, we conclude that power-gating is a promising low-power technique for the next generation technology.

6. Acknowledgement

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