

Minimizing Inductive Noise in System-On-a-Chip with Multiple Power Gating Structures

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Abstract

A multiple power domain strategy in which each power domain has an independent power gating structure is an effective means for reducing leakage power consumption in a system-on-a-chip. During an individual power gating structure power-mode transition, however, serious inductive noise is introduced that may affect normal operation of neighboring circuits. We present a novel power gating structure in which inductive noise is reduced through gradual turn-on and turn-off of its sleep transistor. Experimental simulation results with PowerSpice fixtured in different package models demonstrate the effectiveness of the proposed power gate switching noise reduction technique.

1. Introduction

The multi-threshold CMOS (MTCMOS) circuit [1], called a “power gating structure”, is a well-known technique for reducing leakage power in standby mode. By turning off the sleep transistor during the sleep period, however, all of the internal capacitive nodes of logic block and virtual VDD (VVDD) node is discharged down to a steady state value near GND. During the power-mode transition, the instantaneous charge current through the sleep transistor operated in saturation region creates current surges. Because of the self-inductance of the off-chip bonding wires and the on-chip parasitic inductance inherent to the power rails, current surges result in voltage fluctuations in the on-chip power rails. If the magnitude of the voltage surge/droop is greater than the noise margin of a circuit, the circuit may erroneously latch the wrong value or switch at the wrong time.

Inductive noise, also known as simultaneous switching noise, has been a phenomenon traditionally associated to input/output buffers and internal circuitry [2, 3, 4]. Recently, inductive noise problems due to clock gating have been introduced in [5, 6]. Until now, however, inductive noise originating from the power-mode transition between active and standby modes of a power gating structure was not seriously considered, even though it may become an important issue in the design of a system-on-a-chip (SOC)

employing multiple power gating domains to control leakage power.

In this paper, we first address test chip measurements that indicate inductive noise induced by quick turn-on of the sleep transistor in a conventional power gating structure. Then we propose a novel power gating structure in which inductive noise is reduced through gradual turn-on and turn-off of its sleep transistor. In PowerSpice simulation with different package models, quantitative comparison is made between the proposed power gating structure and a conventional one. Our power gating structures reduce the magnitude of voltage fluctuations in the power rails, as well as the time required to stabilize them.

2. Test Chip Measured Results

In this section, we address the measured result of a test chip designed and implemented to evaluate a conventional power gating structure. Specifically, we show the seriousness of inductive noise induced by instant turn-on of the sleep transistor in conventional power gating structure.

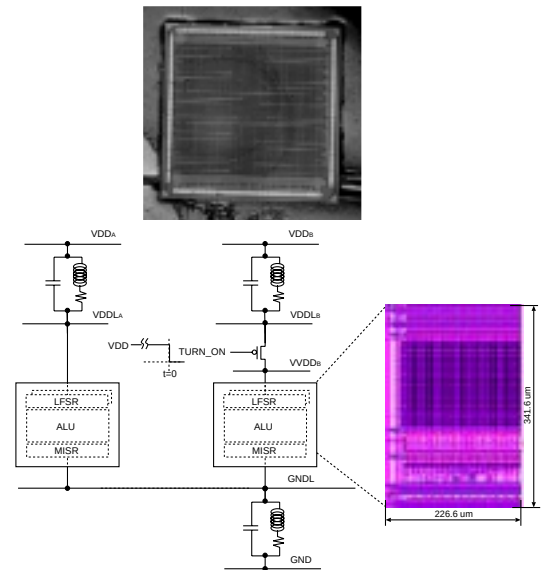


Figure 1. Microphoto and block diagram of test chip used to evaluate a conventional power gating structure.

Figure 1 shows a microphotograph and block diagram of the test chip designed and implemented in $0.13\mu\text{m}$ CMOS technology. Two identical DSP 40-bit arithmetic units (ALUs) were compared, one powered by the $VDDL_A$ grid and the other by $VVDD_B$ serially connected to the $VDDL_B$ grid through a sleep transistor. The sleep transistor is sized at less than 1% of the total ALU PMOS and NMOS width and is composed of parallel instantiation of standard cells. The ALU critical path is through a saturating adder with data inputs supplied by two 40-bit linear feedback shift registers (LFSRs) that generate random patterns with approximately 50% average switching factor. Each element in the pipeline includes a data transition barrier to prevent unneeded switching of elements when they are clock gated. Results are transferred from the output register to a multiple input signature register (MISR). Repeated tests are made at discrete supply voltages ranging from 0.9V to 1.5V in which clock frequency is increased until an error signature is detected by the MISR. The highest non-failing frequency is recorded at each supply voltage. Standby leakage power is measured by stopping the clocks and recording supply current.

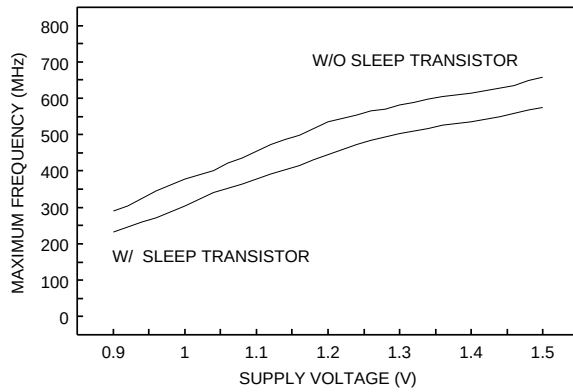


Figure 2. Performance penalty.

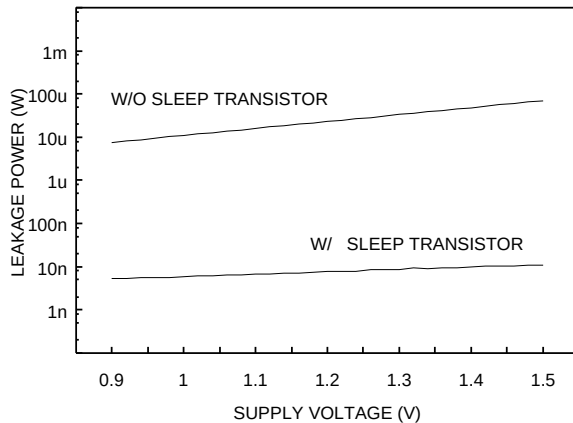


Figure 3. Leakage saving benefit.

The measured test results, comparing the performance and leakage power consumption of the two ALUs are shown in Figures 2 and 3, respectively. In Figure 2, it

is observed that the relatively small sleep transistor incurs a performance penalty on the circuit ranging from 23% at the lowest operating frequency to 13% at the highest. This sizing of the sleep transistor, however, provides large reduction in leakage power, ranging from nearly three orders of magnitude at the lowest supply voltage to nearly four orders of magnitude at the highest as is shown in Figure 3.

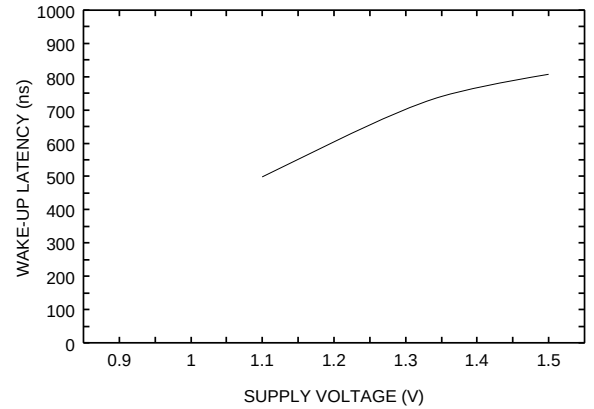


Figure 4. Non-failing wake-up latency.

We also measure the time required to bring the circuit out of sleep mode and operate at 95% of the maximum operating frequency for a given supply voltage, “wake-up latency”. It effectively excludes the inductive noise due to clock gating from our measurement, since the measured performance degradation due to clock gating itself was around 5%. Initially, we turn off a sleep transistor by $|V_{GS}| = 0$ and wait until all of internal nodes and $VVDD$ node is completely discharged. Then, we turn on the sleep transistor by $|V_{GS}| = VDD$ and measure the shortest non-failing wake-up latency. The test is repeated at discrete supply voltages. Results are shown in Figure 4, with wake-up times ranging from 498.38 ns to 807.042 ns over the measured supply range.

It demonstrates the seriousness of inductive noise due to power gating structure in terms of performance. To make it worse, the other circuits sharing the same power rails are disturbed similarly.

3. Proposed Power Gating Structure

In this section, we propose a novel power gating structure that reduces the magnitude of peak current and voltage glitches in the power rails as well as the minimum time required to stabilize power and ground rails.

In the previously published power gating structures, as shown in Figure 5(a), sleep transistor is implemented with a single transistor or a set of transistors [7, 8, 9]. The sleep transistor that consists of a set of transistors is effectively a single transistor, since the transistors share both $VDDL$ and $VVDD$ nodes, as well as a gate-input signal. In standby mode, the sleep transistor operates in the cut-off region. During this mode, the leakage current is

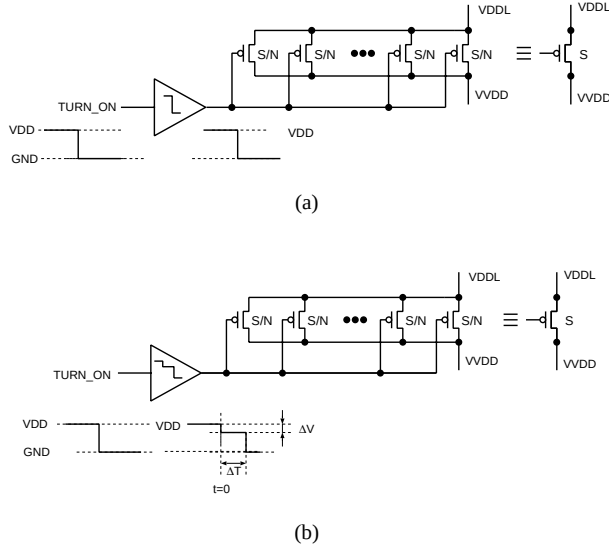


Figure 5. Sleep transistor part of (a) conventional and (b) proposed power gating structures.

limited by the sleep transistor with a high threshold voltage and a proportionally smaller width. By turning off the sleep transistor during the sleep period, all of internal capacitive loads of logic block and VVDD node are discharged down to a steady state value near GND. It causes all of PMOS pull-up paths of logic block turned on, even though NMOS pull-down ones are turned off.

As the sleep transistor is turned on, however, all of discharged internal capacitive loads of the logic block and VVDD node begins to simultaneously charge through the switched PMOS pull-up paths of logic blocks and sleep transistor. The switching activity of entire capacitive loads at that moment is close to 1.0. As a result, a large instantaneous current flows through the PMOS pull-up paths and sleep transistor. The current surge creates inductively induced voltage fluctuations in the power rails.

To solve this wake-up noise problem originating from the power-mode transition between standby and active mode of a power gating structure, we propose a novel power gating structure of Figure 5(b) that consists of a sleep transistor whose $|V_{GS}|$ gradually increases with multiple voltage steps. Our power gate structure minimizes the instantaneous current flow through the sleep transistor by dynamically controlling its $|V_{GS}|$ and V_{DS} . The sleep transistor turn-on and turn-off procedure of ours consists of a relaxation stage and complete turn-on stage. During the relaxation stage, the sleep transistor is weakly turned on with $|V_{GS}| = \Delta V$ ($0 < \Delta V < VDD$), until its V_{DS} is significantly reduced. During the complete turn-on stage, the sleep transistor is completely turned on with $|V_{GS}| = VDD$. When the V_{DS} of the sleep transistor is small enough, the instantaneous current is less sensitive to the variation in $|V_{GS}|$, thus allowing increase of the $|V_{GS}|$ in a non-uniform stepwise manner without increasing instantaneous peak current.

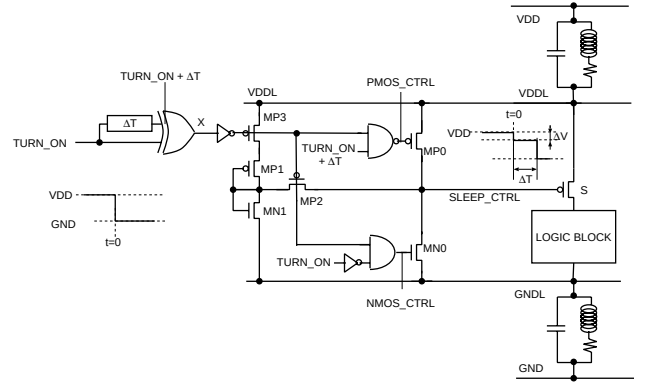


Figure 6. Block diagram of proposed gating structure.

Figure 6 shows a block diagram of our power gating structure with a circuit that generates stepwise voltages. When TURN_ON signal become low, the relaxation stage is initiated, and a pulse of ΔT is generated at node X. The ΔT is controlled by any delay components such as a serially connected shift register. During this time, the transistor MP0 and MN0 are turned off, and MP3 turns on the current reference circuit of diode-connected devices MP1 and MN1, generating the intermediate voltage of SLEEP_CTRL $VDD - \Delta V$, which is determined by $\frac{W}{L}$ ratios of MP1 and MN1. The current through MP1 is then multiplied by the ratio of MP1 and total sleep transistor size S , allowing precise current control during the power-mode transition of the sleep transistor. When the V_{DS} is reduced significantly, the complete turn-on state is initiated and $|V_{GS}|$ becomes VDD.

4. Simulation Results

In this section, several parameters are defined to characterize the effects of inductive noise caused by the transition between active and standby modes implemented with a power gating structure. Then, in terms of these parameters, the proposed power gating structure is compared to a conventional one by simulating the circuits fixtured in two package models.

Figure 7 shows the block diagram of the circuit used for the comparison and parameters defined to characterize the impact of inductive noise caused by the power-mode transition. The circuit is the same as implemented on the test chip, described in Section 2. $V_{MIN}/VDDL$ and $V_{MAX}/VDDL$ are, respectively, the lowest and highest voltage levels of the bounce on the VDDL rail. $V_{MIN}/GNDL$ and $V_{MAX}/GNDL$ are, respectively, the lowest and highest voltage levels of the bounce on the GNDL rail. T_S is the minimum time required for both the VDDL and GNDL rails to be stabilized within $\pm 5\%$ of nominal and defines the minimum delay before the ALU will operate at its specified performance. The measurement of T_S is started at the falling edge of TURN_ON signal of each power gating structure.

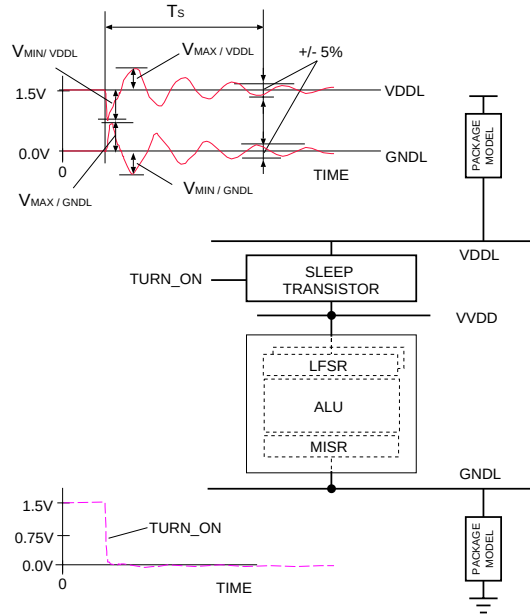


Figure 7. Block diagram of experimental macro used to evaluate our power gating structure, compared to a conventional one.

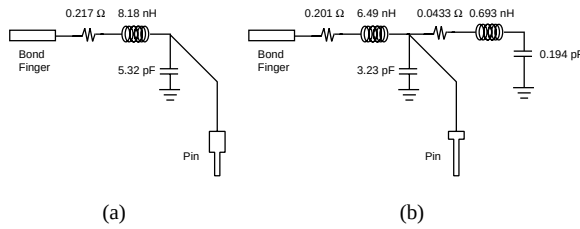


Figure 8. Electrical characteristics of (a) DIP-40 and (b) PGA108M packages supported by MOSIS.

Experimental simulations are made with VDD fixed at 1.5V and are repeated with MOSIS DIP-40 and PGA108M package models of Figure 8.

Table 1. Relative inductive noise reduction.

	MOSIS DIP-40	MOSIS 108PGA
$V_{MAX}/VDDL$	79.09%	79.36%
$V_{MIN}/VDDL$	67.53%	67.66%
$V_{MAX}/GNDL$	50.76%	56.21%
$V_{MIN}/GNDL$	76.72%	83.39%
T_S	74.44%	78.55%

The simulation results, in which the size of the transistors in the stepwise voltage generation part of our power gating structure is tuned for the intermediate voltage of SLEEP_CTRL and ΔT to be set as 0.8V and 6.0 ns, are summarized in Table 1. Values shown for all parameters are performance gains, i.e. reduced bounce or turn-on latency, of the proposed power gating structure rela-

tive to the conventional one. In particular, the maximum magnitude of voltage glitches on power rails in the 40-bit ALUs with our power gating structure is reduced by up to 79.09% and 83.39%, respectively, compared to the ALU with conventional one. At the same time, the time required for power rails to stabilize is reduced by up to 74.44% and 78.55%, depending on package models.

5. Conclusions

This paper investigates the inductive noise caused by instantaneous charge current through a sleep transistor during the mode transition of the power gating structure. We propose a novel power gating structure in which the inductive noise is reduced through gradual turn-on an turn-off of its sleep transistor. In PowerSpice simulation with different package models, our power gating structures reduce the magnitude of voltage fluctuations in the power rails, as well as the time required to stabilize them.

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