UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC.,
Petitioner

v.

REALTEK SEMICONDUCTOR CORPORATION,
Patent Owner

Case No. IPR2023-00920
Patent 8,006,218

DECLARATION OF SYLVIA D. HALL-ELLIS, PH.D.

I. INTRODUCTION

1. My name is Sylvia D. Hall-Ellis. I have been retained as an expert by Advanced Micro Devices, Inc. (referred to herein as "AMD").

2. I have written this Declaration at the request of AMD to provide my expert opinion regarding the authenticity and public availability of several publications. My Declaration sets forth my opinions in detail and provides the bases for my opinions regarding the public availability of these publications.

3. I reserve the right to supplement or amend my opinions, and bases for them, in response to any additional evidence, testimony, discovery, argument, and/or other additional information that may be provided to me after the date of this Declaration.

4. I am being compensated for my time spent working on this matter at my normal consulting rate of $350 per hour, plus reimbursement for any additional reasonable expenses. My compensation is not in any way tied to the content of this Declaration, the substance of my opinions, or the outcome of this proceeding. I have no other interests in this proceeding or with any of the parties.

5. All of the materials that I considered are discussed explicitly in this Declaration.

II. QUALIFICATIONS

6. I am currently an Adjunct Professor in the School of Information at San José State University. I obtained a Master of Library Science from the University of North Texas in 1972 and a Ph.D. in Library Science from the University of Pittsburgh in 1985. Over the last fifty years, I have held various positions in the field of library and information resources. I was first employed as a librarian in 1966 and have been involved in the field of library sciences since, holding numerous positions.

7. I am a member of the American Library Association ("ALA") and its Association for Library Collections & Technical Services ("ALCTS") Division, and I served on the Committee on Cataloging: Resource and Description (which wrote the new cataloging rules) and as the chair of the Committee for Education and Training of Catalogers and the Competencies and Education for a Career in Cataloging Interest Group. I also served as the Chair of the ALCTS Division's Task Force on Competencies and Education for a Career in Cataloging. Additionally, I served as the Chair for the ALA Office of Diversity's Committee on Diversity, as a member of the REFORMA National Board of Directors, and as a member of the Editorial Board for the ALCTS premier cataloging journal, *Library Resources and Technical Services,* and as a Co-Chair of the Membership

AMD EX1021
AMD v. Realtek - Page 3

Committee for the Library Research Round Table (LRRT) of the American Library Association. Currently I serve as a member of the LRRT Nominating Committee.

8. I have also given over one-hundred presentations in the field, including several on library cataloging systems and Machine-Readable Cataloging ("MARC") standards. My current research interests include library cataloging systems, metadata, and organization of electronic resources.

9. I have been deposed twenty-eight times: (1) *Symantec Corp. vs. Finjan*, *Inc.,* Petition for *Inter Partes Review* of U.S. Patent No. 7,613,926, May 26, 2016, on behalf of Symantec Corp.; (2) *Symantec Corp. vs. Finjan*, *Inc.,* 14-cv-299-HSG (N.D. Cal.), on behalf of Symantec Corp., September 14, 2017; (3) one deposition for ten matters: *Intellectual Ventures I LLC vs. AT&T Mobility LLC*; AT&T Mobility II LLC, New Cingular Wireless Services, Inc., SBC Internet Services, Inc., Wayport, Inc., and Cricket Wireless LLC, C.A. No. 12-193 (LPS); *Intellectual Ventures II LLC vs. AT&T Mobility LLC*; AT&T Mobility II LLC, New Cingular Wireless Services, Inc., SBC Internet Services, Inc., Wayport, Inc., and Cricket Wireless LLC, C.A. No. 13-1631 (LPS); *Intellectual Ventures I LLC vs. T-Mobile USA, Inc. and T-Mobile US, Inc.,* C.A. No. 13-1632 (LPS); *Intellectual Ventures II LLC vs. T-Mobile USA, Inc. and T-Mobile US, Inc.,* C.A. No. 13-1633 (LPS); *Intellectual Ventures I LLC, vs. Nextel Operations, Inc., Sprint Spectrum L.P., Boost Mobile, LLC and Virgin Mobile USA, L.P.,* C.A. No. 13-1634

(LPS); *Intellectual Ventures II LLC vs. Nextel Operations, Inc., Sprint Spectrum L.P., Boost Mobile, LLC and Virgin Mobile USA, L.P.,* C.A. No. 13-1635 (LPS); *Intellectual Ventures I LLC, vs. United States Cellular Corporation*, C.A. No. 13-1636 (LPS); *Intellectual Ventures I LLC vs. United States Cellular Corporation*, C.A. No. 13-1637 (LPS); *Intellectual Ventures II LLC vs. AT&T Mobility LLC*, *AT&T Mobility II LLC, New Cingular Wireless Services, Inc.,* C.A. No. 15-799 (LPS); *Intellectual Ventures I LLC vs. T-Mobile USA, Inc. and T-Mobile US, Inc.,* C.A. No. 15-800 (LPS), on behalf of AT&T Mobility LLC; AT&T Mobility II LLC, Boost Mobile, LLC Cricket Wireless LLC, Nextel Operations, Inc., New Cingular Wireless Services, Inc., SBC Internet Services, Inc., Sprint Spectrum L.P., T-Mobile USA, Inc., T-Mobile US, Inc., United States Cellular Corporation Virgin Mobile USA, L.P., and Wayport, Inc., November 15, 2016; (4) *Hitachi Maxell, LTD., v. Top Victory Electronics (Taiwan) Co. Ltd., et al.,* 2:14-cv-1121 JRG-RSP (E.D. Texas), on behalf of Top Victory Electronics (Taiwan) Co. LTD, *et. al.,* January 20, 2016; (5) *Sprint Spectrum, L.P. vs. General Access Solutions, Ltd*., Petition for *Inter Partes Review* of U.S. Patent No. 7,173,916, on behalf of Sprint Spectrum L.P., July 13, 2018; (6) *Nichia Corporation vs. Vizio, Inc*., 8:16-cv-00545; on behalf of Vizio, Inc., October 12, 2018; (7) *Intellectual Ventures I LLC, vs. T-Mobile USA, Inc., T-Mobile US, Inc., Ericsson Inc., and Telefonaktiebolaget LM Ericsson*, 2:17-cv-00557 (JRG), on behalf of T-Mobile

USA, Inc., T-Mobile US, Inc., Ericsson Inc., and Telefonaktiebolaget LM Ericsson, October 19, 2018; (8) Pfizer, Inc. vs. Biogen, Inc., Petition for *Inter Partes Review* of U.S. Patent No. 8,821,873, on behalf of Pfizer, November 3, 2018; (9) *Finjan, Inc. vs. ESET, LLC and ESET SPOL. S.R.O.,* 3:17-cv-00183-CAB-BGS, on behalf of ESET, January 15, 2019; (10) *Finjan, Inc. vs. Cisco Systems, Inc.,* 5:17-cv-00072-BLF-SVK, on behalf of Cisco Systems, Inc., September 6, 2019; (11) *Facebook, Inc., Instagram, LLC and Whatsapp Inc. vs. Blackberry Limited*, Petition for *Inter Partes Review* of U.S. Patent No. 9,349,120 B2, on behalf of Facebook, Inc., Instagram, LLC and Whatsapp Inc. December 20, 2019; (12) *3Shape A/S and 3Shape Inc. v. Align Technology, Inc.,* Petition for *Inter Partes Review* of U.S. Patent No. 7,156,661, IPR 2020-00222 and IPR 2020-00223, August 10, 2020, on behalf of 3Shape A/S and 3Shape Inc.; (13) *Finjan Inc. v. Rapid7, Inc. and Rapid7 LLC*, Northern District of Delaware; 1:18-cv-01519-MN, September 15, 2020; (14) *VLSI Technology LLC v. Intel Corporation*, Western District of Texas, 6:19-cv-00254, 6:19-cv-00255, 6:19-cv-00256, on behalf of Intel Corporation, September 23, 2020; (15) *Finjan Inc. v. Sonicwall, Inc.,* Northern District of California, 5:17-cv-04467-BLF-HRL, on behalf of Sonicwall, Inc., October 27, 2020; (16) *VLSI Technology, LLC v. Intel Corporation*, District of Delaware, 1:18-cv-00966-CFC-CJB, February 5, 2021, on behalf of the Intel Corporation; (17) *Unified Patents, LLC v. Good Kaisha IP*

Bridge 1, Petition for *Inter Partes Review* of U. S. Patent 7,817,868, February 11, 2021, on behalf of Unified Patents; (18) *Finjan, Inc. v. Qualsys, Inc.,* Northern District of California, 4:18-cv-07229-YGR, March 1, 2021, on behalf of Qualsys, Inc.; (19) *Qualcomm, Inc. v. Monterey Research LLC*, Petition for *Inter Partes Review* of U. S. Patent 6,534,805, May 6, 2021, on behalf of Qualcomm, Inc.; (20) *Hulu, LLC v. Sound View Innovations, LLC*, Petition for *Inter Partes Review* of U. S. Patent 5,806,062, May 14, 2021, on behalf of Hulu, LLC; (21) *VLSI Technology LLC v. Intel Corporation*, Western District of Texas, 6:19-cv-00254, 6:19-cv-00255 and 6:19-cv-00256, August 3, 2021, on behalf of Intel Corporation; (22) *Liquidia Technologies, Inc. v. United Therapeutics Corporation*, Petition for *Inter Partes Review* of U. S. Patent 10,716,793 B2, October 20, 2021, on behalf of Liquidia Technologies, Inc.; (23) *EcoFactor, Inc. v. Google, Inc.,* Western District of Texas, 6:20-cv-00075 (ADA), 6:20-0078-ADA, and 6:20-cv-00080 ADA, October 27, 2021, on behalf of Google, Inc.; (24) *Liquidia Technologies, Inc. v. United Therapeutics Corporation*, Petition for *Inter Partes Review* of U. S. Patent 10,716,793 B2, March 11, 2022, on behalf of Liquidia Technologies, Inc.; (25) *Juniper Networks, Inc. v. Swarm Technology LLC*, Petition for *Inter Partes Review* of U. S. Patent 9,852,004, May 5, 2022, on behalf of Juniper Networks, Inc.; (26) *ParkerVision, Inc. v. Intel Corporation*, Western District of Texas, 6:20-cv-108 (ADA), October 26, 2022, on behalf of the

Intel Corporation; (27) *CommScope v. TQ Delta*, Petition for *Inter Partes Review* of U. S. Patents 9,094,348 and 10,833,809, February 16, 2023, on behalf of CommScope; and, (28) *WSOU Investments d/b/a Brazos v. Salesforce.com, Inc.* for Western District of Texas, 6:20-cv-01164-ADA and 6:20-cv-01170-ADA, April 18, 2023, on behalf of Salesforce. I have not testified at trial.

10. My full *curriculum vitae* is submitted herewith as Exhibit 1022.

III. PRELIMINARIES

A. Scope of Declaration and Legal Standards

11. *Scope of this Declaration.* I am not an attorney and will not offer opinions on the law. I am, however, rendering my expert opinion on the authenticity of the documents referenced herein and on when and how each of these documents was disseminated or otherwise made available to the extent that persons interested and ordinarily skilled in the subject matter or art, exercising reasonable diligence, could have located the documents before November 15, 2007.

12. I am informed by counsel that an item is considered authentic if there is sufficient evidence to support a finding that the item is what it is claimed to be. I am also informed that authenticity can be established based on the contents of the documents themselves, such as the appearance, contents, substance, internal patterns, or other distinctive characteristics of the item, taken together with all of

the circumstances. I am further informed that an item is considered authentic if it at least 20 years old, in a condition that creates no suspicion of its authenticity, and in a place where, if authentic, it would likely be. Lastly, I have been informed that a document's authenticity can be established by comparison with an authentic specimen.

13. I am informed by counsel that a printed publication qualifies as publicly accessible as of the date it was disseminated or otherwise made available such that a person interested in and ordinarily skilled in the relevant subject matter could locate it through the exercise of ordinary diligence.

14. While I understand that the determination of public accessibility under the foregoing standard rests on a case-by-case analysis of the facts particular to an individual publication, I also understand that a printed publication is rendered "publicly accessible" if it is cataloged and indexed by a library such that a person interested in the relevant subject matter could locate it (*i.e.*, I understand that cataloging and indexing by a library is sufficient, though there are other ways that a printed publication may qualify as publicly accessible). One manner of sufficient indexing is indexing according to subject matter category. I understand that the cataloging and indexing by a single library of a single instance of a particular printed publication is sufficient, even if the single library is in a foreign country. I understand that, even if access to a library is restricted, a printed publication that

has been cataloged and indexed therein is publicly accessible so long as a presumption is raised that the portion of the public concerned with the relevant subject matter would know of the printed publication. I also understand that the cataloging and indexing of information that would guide a person interested in the relevant subject matter to the printed publication, such as the cataloging and indexing of an abstract for the printed publication, is sufficient to render the printed publication publicly accessible.

15. I understand that routine business practices, such as general library cataloging and indexing practices, can be used to establish an approximate date on which a printed publication became publicly accessible.

B. Persons of Ordinary Skill in the Art.

16. I am told by counsel that the subject matter of this proceeding relates to power routing structures and power arrangement methods for integrated circuits.

17. I have been informed by counsel that a "person of ordinary skill in the art at the time of the invention" ("POSITA") is a hypothetical person who is presumed to be familiar with the relevant field and its literature at the time of the inventions. This hypothetical person is also a person of ordinary creativity, capable of understanding the scientific principles applicable to the pertinent field.

18. I am told by counsel a POSITA would have had a bachelor's degree in computer science, electrical engineering, computer engineering, or a related field,

and approximately two years of experience in the design, development, and/or testing of power distribution networks related to integrated circuits with multiple power domains, or the equivalent, with additional education and/or research substituting for experience and vice versa. I have been further informed by counsel that a person of ordinary skill in the art would have been familiar with and able to understand the information known in the art relating to these fields, including the information disclosed in the publication discussed in this Declaration.

19. It is my opinion that such a person would have been engaged in research, learning, study, and practice in the field, and formal instruction so that bibliographic resources relevant to his or her research would be familiar. Before November 15, 2007, such a person would have had access to a vast array of long-established print resources in the field as well as to a rich set of online resources providing indexing information, abstracts, and full text services.

IV. LIBRARY PROFESSIONAL PRACTICES

20. In preparing this Declaration, I used authoritative databases, such as the OCLC bibliographic database, the Library of Congress Online Catalog, and the Library of Congress Subject Authorities, to confirm citation details of the various publications discussed. Unless I note otherwise below in reference to a specific serial publication, it is my expert opinion that this standard protocol was followed for the serial publication discussed below.

21. *Indexing*. A researcher may discover material relevant to his or her topic in a variety of ways. One common means of discovery is to search for relevant information in an index of periodicals and other publications. Having found relevant material, the researcher will then normally obtain it online, look for it in libraries, or purchase it from the publisher, a bookstore, a document delivery service, or other provider. Sometimes, the date of a document's public accessibility will involve both indexing and library date information. However, date information for indexing entries is often unavailable. This is especially true for online indices.

22. Indexing services use a wide variety of controlled vocabularies to provide subject access and other means of discovering the content of documents. The Library of Congress Subject Authorities includes standard forms of terms and cross references that are included in bibliographic records. Subject headings are terms that an individual seeking a document regardless of format can enter in the search bar of the online catalog. Subjects also connect an authenticated term (one included in the Library of Congress subject headings list) with related, broader, and narrower terms. The formats in which these access terms are presented vary from service to service.

23. Online indexing services commonly provide bibliographic information, abstracts, and full-text copies of the indexed publications, along with a list of the documents cited in the indexed publication. These services also often

AMD EX1021
AMD v. Realtek - Page 12

provide lists of publications that cite a given document. A citation of a document is evidence that the document was publicly available and in use by researchers no later than the publication date of the citing document. Prominent indexing services include the *IEEE Xplore* database, the *ACM Digital Library, ResearchGate,* and *Semantic Scholar*.

24. *ACM Digital Library*.[1] This index is produced by the Association for Computing Machinery, the world's largest scientific and educational computing society. The *ACM Digital Library* contains the full text of all AMC publications, hosted full-text publications from selected publishers, and the ACM Guide to Computing Literature—a comprehensive bibliography of computing literature beginning in the 1950s with more than a million entries. All metadata in the database are freely available on the Web, including abstracts, linked references, citing work, and usage statistics. Full-text articles are available with subscription.

25. *IEEE Xplore database*.[2] Librarians in academic, special, and large public libraries are familiar with the *IEEE Xplore* database. In working with undergraduate and graduate students, researchers, scientists, and the public, librarians are intimately familiar with the *IEEE Xplore* database and rely on its

[1] https://dl.acm.org/

[2] https://ieeexplore.ieee.org/Xplore/home.jsp

content for access to reliable, accurate publications. Established to serve as a database for the IEEE's ebooks, standards, conference papers, technical reports, and journal articles, and related documents dating from 1988 to the present and selectively from 1913 to 1987, *IEEE Xplore* is a scholarly research database that includes 5.8 million documents which is known for its reputable curation and maintenance of documents and publication information. The *IEEE Xplore* database accurately reports dates of publications and events and accurately reports locations of events in accordance with standard practices for major industry journals. Approximately 20,000 new documents are added to *IEEE Xplore* each month. Abstracts are free to access, but access to full text requires a subscription or institutional login.

26. The IEEE *Xplore* requires peer review before publishing content. I have used IEEE publications in print and online for nearly 50 years. Currently I have access to IEEE documents as part of the resources for faculty through the King Library at San José State University. In addition to covering material from the IEEE, the IEEE *Xplore* also covers materials from the Institution of Engineering and Technology. The *IEEE Xplore* digital library provides Web access to more than 5.3-million full-text documents from some of the world's most highly cited publications. Approximately 20,000 new documents are added to

AMD EX1021
AMD v. Realtek - Page 14

IEEE Xplore each month. Abstracts are free to access, but access to full text requires a subscription or institutional login.

27. *ResearchGate*. [3] A social networking site for scientists and researchers to share papers, ask and answer questions, and find collaborators., *ResearchGate* is the largest academic social network in terms of active users, although other services have more registered users, and a 2015–2016 survey suggests that almost as many academics have *Google Scholar* profiles.

28. Features available to *ResearchGate* members include following a research interest and the work of other individual participants, a blogging feature for users to write short reviews on peer-reviewed articles, private chat rooms for sharing data, editing documents, or discussing confidential topics, and a research-focused job board. *ResearchGate* indexes self-published information on user profiles and suggests members connect with others who have similar interests. Member questions are fielded to others who have identified relevant expertise on their profiles.

29. As of 2018, *ResearchGate* had more than 15 million users, with its largest user-bases coming from Europe and North America. Most of *ResearchGate's* users are involved in medicine, biology, engineering, computer science, agricultural sciences, and psychology. *ResearchGate* publishes a citation

[3] https://www.researchgate.net

AMD EX1021
AMD v. Realtek - Page 15

impact measurement in the form of an "RG Score," which is reported to be correlated with existing citation impact measures. *ResearchGate* does not charge fees for putting content on the site and does not require peer review.

30. *Semantic Scholar.*[4] A project developed at the Allen Institute for Artificial Intelligence and publicly released in November 2015, *Semantic Scholar* is designed to be an AI-backed search engine for scientific journal articles which uses a combination of machine learning, natural language processing, and machine vision to add a layer of semantic analysis to the traditional methods of citation analysis, and to extract relevant figures, entities, and venues from papers. *Semantic Scholar* is designed to highlight important, influential papers, and to identify the connections between them.

31. As of January 2018, following a 2017 project that added biomedical papers and topic summaries, the *Semantic Scholar* corpus included more than 40 million papers from computer science and biomedicine. In March 2018, Doug Raymond, who developed machine learning initiatives for the Amazon Alexa platform, was hired to lead the *Semantic Scholar* project. As of August 2019, the number of included papers had grown to more than 173 million after the addition of the Microsoft Academic Graph records, already used by Lens.org.

---

[4] https://www.semanticscholar.org

AMD EX1021
AMD v. Realtek - Page 16

V. ONLINE CATALOGS AND MARC RECORDS

32. MARC is a framework into which descriptive bibliographic data are transcribed to interact with the software in online library catalogs to provide access to books, journals, and other resources in the collection. The bibliographic data provide points of access and can be searched by a POSITA to identify and obtain resources in the library collection. An information seeker (or POSITA) can search a local online library catalog or the holdings of a group of libraries in a state or region or in the global catalog WorldCat.

33. MARC records are not designed for public viewing. Although a significant number of libraries provide access to the MARC version of a bibliographic record, the public display is designed to show information in a succinct manner that is quickly understood and useful to the information seeker. Libraries determine the default search for the online catalog to make the entry of search terms efficient and result in a successful search. Information seekers can enter a keyword, title, author, or standard number for the item. Libraries may also provide a search capability called "Summon" that allows the information seeker to enter known information about the item to conduct a search.

34. Learning to use an online library catalog begins in elementary school and continues through high school and post-secondary studies. Undergraduate students further develop their skills to use the online catalog at the academic

institution where they are studying through information literacy instruction which is provided by professional reference and user experience librarians. The skills required to search, identify, and obtain the resources identified in this Declaration/report are fundamental to using the online catalogs in libraries and information centers. Therefore, a POSITA who has attained the undergraduate and/or graduate educational levels described above (see paragraph 17) possesses the searching and retrieval skills needed to search library catalogs.

35. Professional catalog and metadata librarians prepare and enhance MARC records to provide points of access for each item in the library collection. Using a set of internationally adopted guidelines, rules for the assignment of classification numbers, and the assignment of subject headings from standardized lists, taxonomies, folksonomies, locally developed lists. An information seeker (including POSITAs) can search the online library catalog in a number of ways to identify a specific item or resources on a defined topic.

36. The continued development of the software that supports integrated online library catalogs resulted in the potential to search by an individual creator or author, title proper or variant title, a series that contains the desired item, subjects, corporate bodies responsible in part for the creation of an item, or standard identification numbers associated with the item (e.g., International Standard Book Numbers (ISBN), International Standard Serial Numbers (ISSN), and Publisher's

Numbers). Each of these data elements appears in a prescribed location within the MARC framework so that the software can parse, index, and display data elements resulting from a user-initiated search.

37. Examining the MARC records for a specific item reveals the comprehensive data transcribed about a particular item at the time that cataloging and classification occurred. In addition to the creator, title, subjects, and standard numbers, additional information may provide additional and relevant data depending on the type of resource. Understanding the full extent of bibliographic data for an item and the points of access associated with it provides essential information that can be used to determine the indexing and public availability for documents described in this Declaration.

VI. LIBRARY CATALOGING PRACTICES

38. I am fully familiar with the library cataloging standard known as the MARC standard, which is an industry-wide standard method of storing and organizing library catalog information.[5] MARC was first developed in the 1960s by the Library of Congress. A MARC-compatible library is one that has a catalog consisting of individual MARC records for each of its items. Today, MARC is the

[5] The full text of the standard is available from the Library of Congress at http://www.loc.gov/marc/bibliographic/.

primary communications protocol for the transfer and storage of bibliographic metadata in libraries.[6]

39. Since at least the early 1970s and continuing to the present day, MARC has been the primary communications protocol for the transfer and storage of bibliographic metadata in libraries.[7] As explained by the Library of Congress:

> You could devise your own method of organizing the bibliographic information, but you would be isolating your library, limiting its options, and creating much more work for yourself. Using the MARC standard prevents duplication of work and allows libraries to better share bibliographic resources. Choosing to use MARC

---

[6] Almost every major library in the world is MARC-compatible. *See, e.g.*, *MARC Frequently Asked Questions (FAQ)*, Library of Congress, https://www.loc.gov/marc/faq.html (last visited April 20, 2023) ("MARC is the acronym for MAchine-Readable Cataloging. It defines a data format that emerged from a Library of Congress-led initiative that began nearly forty years ago. It provides the mechanism by which computers exchange, use, and interpret bibliographic information, and its data elements make up the foundation of most library catalogs used today."). MARC is the ANSI/NISO Z39.2-1994 (reaffirmed 2016) standard for Information Interchange Format.

[7] A complete history of the development of MARC can be found in *MARC: Its History and Implications* by Henrietta D. Avram (Washington, DC: Library of Congress, 1975) and available online from the Hathi Trust (https://babel.hathitrust.org/cgi/pt?id=mdp.39015034388556;view=1up;seq=1; last visited April 20, 2023).

AMD EX1021
AMD v. Realtek - Page 20

> enables libraries to acquire cataloging data that is predictable and reliable. If a library were to develop a "home-grown" system that did not use MARC records, it would not be taking advantage of an industry-wide standard whose primary purpose is to foster communication of information.
>
> Using the MARC standard also enables libraries to make use of commercially available library automation systems to manage library operations. Many systems are available for libraries of all sizes and are designed to work with the MARC format. Systems are maintained and improved by the vendor so that libraries can benefit from the latest advances in computer technology. The MARC standard also allows libraries to replace one system with another with the assurance that their data will still be compatible.

Why Is a MARC Record Necessary? LIBRARY OF CONGRESS, http://www.loc.gov/marc/umb/um01to06.html#part2 (last visited April 20, 2023).

40. Thus, almost every major library in the world is MARC-compatible. *See, e.g.*, *MARC Frequently Asked Questions (FAQ)*, LIBRARY OF CONGRESS, https://www.loc.gov/marc/faq.html (last visited April 20, 2023) ("MARC is the acronym for MAchine-Readable Cataloging. It defines a data format that emerged from a Library of Congress-led initiative that began nearly fifty years ago. It provides the mechanism by which computers exchange, use, and interpret bibliographic information, and its data elements make up the foundation of most library catalogs used today."). MARC is the ANSI/NISO Z39.2-1994 standard

AMD EX1021
AMD v. Realtek - Page 21

(reaffirmed in 2016) for Information Interchange Format. The full text of the standard is available from the Library of Congress at http://www.loc.gov/marc/bibliographic/ (last visited April 20, 2023).

41. A MARC record comprises several fields, each of which contains specific data about the work. Each field is identified by a standardized, unique, three-digit code corresponding to the type of data that follow. For example, a work's title is recorded in field 245, the primary author or creator of the work is recorded in field 100, an item's International Standard Book Number ("ISBN") is recorded in field 020, an item's International Standard Serial Number ("ISSN") is recorded in field 022, an item's Library of Congress call number is recorded in field 050, and the publication date is recorded in field 260 under the subfield "c." *Id.*[8] If a work is a periodical, then its publication frequency is recorded in field 310, alternate publication frequency is recorded in field 321, and the publication dates (*e.g.*, the first and last publication) are recorded in field 362, which is also

[8] In some MARC records, field 264 is used rather than field 260 to record publication information. *See* http://www.loc.gov/marc/bibliographic/bd264.html (last visited April 20, 2023) ("Information in field 264 is similar to information in field 260 (Publication, Distribution, etc. (Imprint)). Field 264 is useful for cases where the content standard or institutional policies make a distinction between functions").

referred to as the enumeration/chronology field. *See* http://www.loc.gov/marc/bibliographic/bd3xx.html (last visited April 20, 2023).

42. MARC records also include several fields that include subject matter classification information. An overview of MARC record fields is available through the Library of Congress at http://www.loc.gov/marc/bibliographic/. For example, 6XX fields are termed "Subject Access Fields." *See* http://www.loc.gov/marc/bibliographic/bd6xx.html. Among these, for example, is the 650 field; this is the "Subject Added Entry – Topical Term" field. *See* http://www.loc.gov/marc/bibliographic/bd650.html. The 650 field is a "[s]ubject added entry in which the entry element is a topical term." *Id.* These authenticated subject entries "are assigned to a bibliographic record to provide access according to generally accepted thesaurus-building rules (*e.g.*, *Library of Congress Subject Headings* (LCSH), *Medical Subject Headings* (MeSH))." *Id.*

43. Further, MARC records include call numbers, which themselves indicate a subject and physical location within the library collections. For example, the 050 field is the "Library of Congress Call Number." *See* http://www.loc.gov/marc/bibliographic/bd050.html (last visited April 20, 2023). A defined portion of the Library of Congress Call Number is the classification number, and "source of the classification number is *Library of Congress Classification* and the *LC Classification-Additions and Changes*." *Id.* Thus,

AMD EX1021
AMD v. Realtek - Page 23

included in the 050 field is a subject matter classification. Each item in a library has a single classification number. A library selects a classification scheme (*e.g.*, the Library of Congress Classification scheme just described or a similar scheme such as the Dewey Decimal Classification scheme or the National Library of Medicine Classification scheme) and uses it consistently. When the Library of Congress assigns the classification number, it appears as part of the 050 field. If a local library assigns the classification number, it appears in a 090 field. In either scenario, the MARC record includes a classification number that represents a subject matter classification.

44. Each item in a library has a single classification number. A library selects a classification scheme (*e.g.*, the Library of Congress Classification scheme just described or a similar scheme such as the Dewey Decimal Classification scheme) and uses it consistently. When the Library of Congress assigns the classification number, it appears as part of the 050 field, as discussed above. For MARC records created by libraries other than the Library of Congress (*e.g.*, a university library or a local public library), the classification number may appear in a 09X (*e.g.*, 090) field. *See* http://www.loc.gov/marc/bibliographic/bd09x.html (last visited April 20, 2023).

45. The OCLC was created "to establish, maintain and operate a computerized library network and to promote the evolution of library use, of

AMD EX1021
AMD v. Realtek - Page 24

libraries themselves, and of librarianship, and to provide processes and products for the benefit of library users and libraries, including such objectives as increasing availability of library resources to individual library patrons and reducing the rate of rise of library per-unit costs, all for the fundamental public purpose of furthering ease of access to and use of the ever-expanding body of worldwide scientific, literary and educational knowledge and information."[9] Among other services, OCLC and its members are responsible for maintaining the WorldCat database (http://www.worldcat.org/), used by independent and institutional libraries throughout the world.

46. OCLC also provides its members online access to MARC records through its OCLC bibliographic database. When an OCLC member institution acquires a work, it creates a MARC record for this work in its computer catalog system in the ordinary course of its business. MARC records created at the Library of Congress were initially tape-loaded into the OCLC database through a subscription to MARC Distribution Services daily or weekly. Once the MARC record is created by a cataloger at an OCLC member institution or is tape-loaded from the Library of Congress, the MARC record is then made available to any

---

[9] Third Article, Amended Articles of Incorporation of OCLC Online Computer Library Center, Incorporated (available at https://www.oclc.org/content/dam/oclc/membership/articles-of-incorporation.pdf).

other OCLC members online, and therefore made available to the public. Accordingly, once the MARC record is created by a cataloger at an OCLC member institution or is tape-loaded from the Library of Congress or another library anywhere in the world, any publication corresponding to the MARC record has been cataloged and indexed according to its subject matter such that a person interested in that subject matter could, with reasonable diligence, locate and access the publication through any library with access to the OCLC bibliographic database or through the Library of Congress.

47. When an OCLC member institution creates a new MARC record, OCLC automatically supplies the date of creation for that record. The date of creation for the MARC record appears in the fixed field (008), characters 00 through 05. The MARC record creation date reflects the date on which, the item was first acquired or cataloged. Initially, field 005 of the MARC record is automatically populated with the date the MARC record was created in year, month, day format (YYYYMMDD) (some of the newer library catalog systems also include hour, minute, second (HHMMSS)). Thereafter, the library's computer system may automatically update the date in field 005 every time the library updates the MARC record (*e.g.*, to reflect that an item has been moved to a different shelving location within the library). Field 005 is visible when viewing a MARC record via an appropriate computerized interface, but when a MARC

AMD EX1021
AMD v. Realtek - Page 26

record is printed to hardcopy, no "005" label appears. The initial field 005 date (*i.e.*, the date the MARC record was created) does appear, however, next to the label "Entered."[10] The date upon which the most recent update to field 005 occurred also appears, next to the label "Replaced." Thus, when an item's MARC record has been printed to hardcopy—as is the case with the exhibits to this report—the date reflected next to the label "Entered" is necessarily on or after the date the library first cataloged and indexed the underlying item.

48. Once one library has cataloged and indexed a publication by creating a MARC record for that publication, other libraries that receive the publication do not create additional MARC records—the other libraries instead rely on the original MARC record. They may update or revise the MARC record to ensure accuracy, but they do not replace or duplicate it. This practice does more than save libraries from duplicating labor, it also enhances the accuracy of MARC records. It also allows librarians around the world to know that a particular MARC record is authoritative. In contrast, a hypothetical system wherein duplicative records were created would result in confusion as to which record is authoritative.

49. The date of creation of the MARC record by a cataloger at an OCLC

---

[10] In this report, I sometimes refer to the "Entered" entry as field 008, characters 00-05.

AMD EX1021
AMD v. Realtek - Page 27

member institution reflects when the underlying item is accessible to the public. Upwards of two-thirds to three-quarters of book sales to libraries come from a jobber or wholesaler for online and print resources. These resellers make it their business to provide books to their customers as fast as possible, often providing turnaround times of only a single day after publication. Libraries purchase a significant portion of the balance of their books directly from publishers themselves, which provide delivery on a similarly expedited schedule. In general, libraries make these purchases throughout the year as the books are published and shelve the books as soon thereafter as possible in order to make the books available to their patrons. Thus, books are generally available at libraries across the country within just a few days of publication.

50. *Journals.* Catalogers can create MARC records for all types of print, online, and digital resources. For example, MARC records cover serial publications, including both serially-published monographs and journals. OCLC hosts MARC records for more than 320 million serial publications. Serial publications are those publications that have the same collective title but are intended to be continued indefinitely with enumeration such as a volume or issue number, *e.g.*, magazines and journals. In the OCLC bibliographic database, the first issue of the serial publication is typically cataloged, but the date is left open-ended with the use of a punctuation mark such as a dash. Individual issues are not

AMD EX1021
AMD v. Realtek - Page 28

cataloged according to the current national cataloging rules outlined in *RDA: Resource and Access*. Instead, MARC records for serial publication in OCLC represent the entire run of the serial title. With knowledge of the first issue published, future issues can be predicted. In my extensive professional experience, is it highly unusual for a library to stop collecting and shelving a serial publication prior to the end of its publication run. If a subscription to a serial publication ends its run or is cancelled before the end of its run, the library will denote that it has stopped receiving new volumes by filling in the end date in the local MARC record.

51. The handling of printed journal subscriptions is shown on the covers of individual issues. As was the best practice among libraries, issues arrived at a central facility and were immediately received, verified as part of a subscription, checked in, and stamped with the institution's name and date. Determining that the issue was part of the library subscription ensured that the entire set of publications for the year had been received so that they could be professionally bound and retained. This process also verified that all of the published issues arrived so that the library staff did not have to request or claim an issue that did not arrive as expected. In large public libraries with branches and multi-campus libraries within academic institutions, the journals were sorted and delivered to the subscribing unit. The issues were frequently stamped again to acknowledge receipt. The new

AMD EX1021
AMD v. Realtek - Page 29

issue was placed in the public area; the older issue was stored so that it remained available.

52. The foregoing process has been standard library practice longer than I have been working in the profession. I first learned the steps in the process in the late 1970s and later supervised it. Although the checking in process has become automated and now links electronically to holdings records for the MARC record for each serial title, the manual stamping and placing the issue in a public area has not changed for 50 years. Unless I note otherwise below in reference to a specific serial publication, it is my expert opinion that this standard protocol was followed for each of the publications discussed below.

VII. PUBLICATIONS

A. PUBLICATION 1: "Benefits and Costs of Power-Gating Technique" by Hailin Jiang, Malgorzata Marek-Sadowska, and Sani R. Nassif. ("Jiang 2005")

53. Attached hereto as Attachment 1 is a copy of a conference paper published in the volume titled *2005 International Conference on Computer Design: Proceedings* found in the North Carolina State University at Raleigh Libraries. The conference paper titled "Benefits and Costs of Power-Gating Technique" by Hailin Jiang, Malgorzata Marek-Sadowska, and Sani R. Nassif (hereafter "Jiang 2005") appears beginning on page 559. The 2005 International Conference on Computer Design: Proceedings (ICCD '05) was held on October 2-

AMD EX1021
AMD v. Realtek - Page 30

5, 2005, in San José, California. Attachment 1 is a true and correct copy of the Jiang 2005 conference paper (pages 559-566). I obtained this copy of the conference paper from the North Carolina State University at Raleigh Libraries. Specifically, the text of the Jiang 2005 conference paper is complete; no pages are missing, and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. Attachment 1 was found within the custody of a library—a place where, if authentic, a copy of this conference proceedings volume would likely be. Attachment 1 is a true and correct copy in a condition that creates no suspicion about authenticity.

54. The Jiang 2005 conference paper is also available in the *ACM Digital Library*,[11] the *IEEE Xplore* database,[12] which indicated a publication date of October 31, 2005, and the digital repositories *ResearchGate*[13] and Semantic Scholar.[14]

---

[11] https://dl.acm.org/doi/10.1109/ICCD.2005.34.

[12] https://ieeexplore.ieee.org/document/1524207.

[13] https://www.researchgate.net/publication/4182370_Benefits_and_costs_of_power-gating_technique.

[14] https://www.semanticscholar.org/paper/Benefits-and-costs-of-power-gating-technique-Jiang-Marek-Sadowska/3b3f4b97ad8b0b07e5aee1edb27b52f1dc720d98.

55. Attached hereto as Attachment 1A is a true and correct copy of the MARC record for this conference proceedings volume from the North Carolina State University at Raleigh Libraries online catalog. The library ownership is indicated by the presence of the library's code (NRC) in field 994. The library continues to update this MARC record and enhanced the MARC record to meet current cataloging rules. The most recent enhancement to the MARC record occurred on November 18, 2005, as shown in field 005 ("20051118"). I personally identified and retrieved the library catalog record which is Attachment 1A.

56. Based on finding a copy of Attachment 1 in the North Carolina State University at Raleigh Libraries and MARC record in its online library catalog attached as Attachment A, it is my opinion that the book titled *2005 International Conference on Computer Design: Proceedings* was publicly available at the North Carolina State University at Raleigh Libraries as of November 8, 2005, as indicated in field 008 ("051108").

57. Attached hereto as Attachment 1B is a true and correct copy of the MARC record for the volume titled *2005 International Conference on Computer Design: Proceedings* obtained from the OCLC bibliographic database. I personally identified and retrieved the MARC record that is Attachment 1B. As previously noted, the library that created the record is recorded in field 040 with a unique library code. For Attachment 1B, that library code is "IXA," which means

that the MARC record for this conference proceedings volume was cataloged at the University of Texas – Austin Libraries. As can be seen in the "Entered" field in the MARC record for this exhibit, a cataloger at the University of Texas – Austin Libraries created OCLC record number 62240543 on November 8, 2005, as shown in the "Entered" field ("20051108"). The library continues to update this MARC record and enhanced the MARC record to meet current cataloging rules. The most recent enhancement to the MARC record occurred on June 9, 2022, as shown in the "Replaced" field ("20220609").

58. Attachment 1B further includes an entry in field 050 ("TK7888.4 $b .I23 2005")—as described above, a subject matter classification number consistent with the Library of Congress classification system (analogous to the Dewey Decimal classification system). Attachment 1B also shows that Attachment 1 was catalogued with four descriptor terms reading "Microcomputers $x Design and construction $v Congresses" (see Attachment 1C, Library of Congress subject heading sh85084804, Attachment 1D, Library of Congress subject heading sh87005579, and Attachment 1E, Library of Congress subject heading sh85031115), "Electronic digital computers $x Circuits $v Congresses" (see Attachment 1F, Library of Congress subject heading sh2009124809), "Integrated circuits $x Very large scale integration $v Congresses" (see Attachment 1G, Library of Congress subject heading sh2008104263), and "Computer engineering

$v Congresses" (see Attachment 1H, Library of Congress subject heading sh2009121192) in the 650 fields. Thus, as of its cataloging, the publication corresponding to the MARC record attached hereto as Attachment 1B was indexed according to its subject matter by virtue of at least two independently sufficient classifications: the field 050 entry and the field 650 entries. Further, as of November 8, 2005, the MARC record attached hereto as Attachment 1B was accessible through any library with access to the OCLC bibliographic database or the online catalog at a library that acquired the conference proceedings volume.

59. Attachment 1B indicates that the volume titled *2005 International Conference on Computer Design: Proceedings* as cataloged at the University of Texas – Austin Libraries is currently available from 11 libraries. For these reasons, it is my opinion that Attachment 1 was published and publicly accessible at least as early as November 8, 2005.

B. PUBLICATION 2: "LVS Verification across Multiple Power Domains for a Quad-Core Microprocessor" by Wei Li, Daniel Blakely, Scott Van Sooy, Kevin Dunn, David Kidd, and Robert Rogenmoser. ("Li")

60. Attached hereto as Attachment 2 is a copy of the journal article "LVS Verification across Multiple Power Domains for a Quad-Core Microprocessor" by Wei Li, Daniel Blakely, Scott Van Sooy, Kevin Dunn, David Kidd, and Robert Rogenmoser (hereafter "Li"). The Li article was published in Volume 11, Number 2 of the journal *ACM Transactions on Design Automation of Electronic*

Systems and was found in the University of Central Florida Libraries (Orlando, Florida). The Li article appears beginning on page 490 of this issue dated April 2006. Attachment 2 is a true and correct copy of the Li article (pages 490-500 of the full journal issue). Specifically, the text of the article is complete; no pages are missing, and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. The Li article is also available in the *ACM Digital Library*,[15] which records an online publication date of April 1, 2006. Attachment 2 was found within the custody of a library—a place where an authentic copy of this journal would likely be. Attachment 2 is a true and correct copy in a condition that creates no suspicion about its authenticity.

61. Attached hereto as Attachment 2A is a true and correct copy of the metadata record for the journal *ACM Transactions on Design Automation of Electronic Systems* in the University of Central Florida Libraries online catalog.[16] I personally identified and retrieved the MARC record that is Attachment 2A.

62. Based on finding a print copy of Attachment 2 in the University of

---

[15] https://dl.acm.org/doi/abs/10.1145/1142155.1142166.

[16] https://ucf-flvc.primo.exlibrisgroup.com/discovery/fulldisplay?docid=cdi_yonsei_eresources_16081&context=PC&vid=01FALSC_UCF:UCF&lang=en&search_scope=DN_and_CI&adaptor=Primo%20Central&tab=Everything&query=any,contains,1084-4309&mode=basic

Central Florida Libraries and MARC record in its online library catalog attached as Attachment 2A, it is my opinion that the Li article published in the journal *ACM Transactions on Design Automation of Electronic Systems* was publicly available on or shortly after July 24, 2006, as noted by the stamp on the cover. This date stamp has the general appearance of date stamps that libraries have long affixed to periodicals to show when an issue was received, verified, and checked in.

63. As noted in the holdings information, the University of Central Florida Libraries has received the journal *ACM Transactions on Design Automation of Electronic Systems* since January 1996 and continues to receive the publication. In view of the metadata record for Attachment 2, the Li article was publicly available on or shortly after July 24, 2006, because the serial title had been received, cataloged, and indexed in the University of Central Florida Libraries and made part of its online catalog database.

64. Attached hereto as Attachment 2B is a true and correct copy of the MARC record for the journal *ACM Transactions on Design Automation of Electronic Systems* obtained from the OCLC bibliographic database. As previously noted, the library that created the record is recorded in field 040 with a unique library code. For Attachment 2B, that library code is "NSD," which means that the MARC record for this serial was cataloged as part of the National Serials Data Program at the Library of Congress. As can be seen in the "Entered" field in

the MARC record for this exhibit, a cataloger in the Library of Congress created OCLC record number 33041249 on August 25, 1995, as shown in the "Entered" field ("19950825"). The library continues to update this MARC record and enhanced the MARC record to meet current cataloging rules. The most recent enhancement to Attachment 2B occurred on April 3, 2022, as shown in the "Replaced" field ("20220403"). I personally identified and retrieved the MARC record that is Attachment 2B. The "BLvl" entry in Attachment 2B is "s," which indicates that the journal *ACM Transactions on Design Automation of Electronic Systems* is a serial publication. Field 310 of Attachment 2B reads "Quarterly." Accordingly, the MARC record for Attachment 2 corresponds to the journal *ACM Transactions on Design Automation of Electronic Systems* from the time the serial title began publication and includes the date of the Li article.

65. Attachment 2B includes an entry in field 050 ("TK7869 $b .A25")—as described above, a subject matter classification number consistent with the Library of Congress classification system (analogous to the Dewey Decimal classification system)—and an entry in field 082 ("004"), a subject matter consistent with the Dewey Decimal classification system. Attachment 2B further includes four descriptor terms reading "Electronic systems $x Design $x Data processing $v Periodicals" (see Attachment 2C, Library of Congress subject heading sh85042373, Attachment 2D, Library of Congress subject heading

AMD EX1021
AMD v. Realtek - Page 37

sh85037197, Attachment 2E, Library of Congress subject heading sh85035857, and Attachment 2F, Library of Congress subject heading sh85099890),"Electronic circuit design $x Data processing $v Periodicals" (see Attachment 2G, Library of Congress subject heading sh85042278 and Attachment 2F, Library of Congress subject heading sh85099890), "Computer-aided design $v Periodicals" (see Attachment 2G, Library of Congress subject heading sh2009121170), and "Integrated circuits $x Design $x Data processing $v Periodicals" (see Attachment 2H, Library of Congress subject heading sh85067117, Attachment 2D, Library of Congress subject heading sh85037197, Attachment 2E, Library of Congress subject heading sh85035857, and Attachment 2F, Library of Congress subject heading sh85099890) in the 650 fields. Thus, as of its cataloging, the publication corresponding to the MARC record attached hereto as Attachment 2B was indexed according to its subject matter by virtue of at least three independently sufficient classifications: the field 050 entry, the field 082 entry, and the field 650 entries. As of August 25, 1995, the MARC record attached hereto as Attachment 2B was accessible through any library with access to the OCLC bibliographic database or the online catalog at a library that subscribed to the serial.

66. Attachment 2B indicates that the journal *ACM Transactions on Design Automation of Electronic Systems* as cataloged in the Library of Congress is currently available from 396 libraries. For these reasons, it is my opinion that

AMD EX1021
AMD v. Realtek - Page 38

Attachment 2 was published and accessible to the public at least as early as April 1, 2006, online and July 24, 2006, in print.

C. PUBLICATION 3: "Power/Ground Supply Network Optimization for Power-Gating" by Hailin Jiang and Malgorzata Marek-Sadowska. ("Jiang 2006")

67. Attached hereto as Attachment 3 is a copy of a conference paper published in the volume titled *International Conference on Computer Design 2006* found in the University of Wisconsin – Madison Libraries. The conference paper titled "Power/Ground Supply Network Optimization for Power-Gating" by Hailin Jiang and Malgorzata Marek-Sadowska (hereafter "Jiang 2006") appears beginning on page 332. The International Conference on Computer Design 2006 was held on October 1-4, 2006, in San José, California. Attachment 3 is a true and correct copy of the Jiang 2006 conference paper (pages 332-337). I obtained this copy of the conference paper from the University of Wisconsin Libraries. Specifically, the text of the Jiang 2006 conference paper is complete; no pages are missing, and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. Attachment 3 was found within the custody of a library—a place where, if authentic, a copy of this conference proceedings volume would likely be. Attachment 3 is a true and correct copy in a condition that creates no suspicion about authenticity.

68. The Jiang 2006 conference paper is also available in the *IEEE Xplore*

database[17] and was added on November 12, 2007.

69. Attached hereto as Attachment 3A is a true and correct copy of the MARC record for this conference proceedings volume from the University of Wisconsin – Madison Libraries online catalog. The library ownership is indicated by the presence of the library's name at the top of the screen. The volume titled *International Conference on Computer Design 2006* is cataloged as a part of series and is listed in the fifteenth field 762. The library continues to update this MARC record and enhanced the MARC record to meet current cataloging rules. The most recent enhancement to the MARC record occurred on April 2, 2023, as shown in field 005 ("20230402"). I personally identified and retrieved the library catalog record which is Attachment 3A.

70. Based on finding a copy of Attachment 3 in the University of Wisconsin – Madison Libraries and MARC record in its online library catalog attached as Attachment 3A, it is my opinion that the book titled *International Conference on Computer Design 2006* was publicly available at the University of Wisconsin – Madison Libraries as of November 18, 2005, as indicated in the "Entered" field of Attachment 3B.

71. Attached hereto as Attachment 3B is a true and correct copy of the MARC record for the volume titled *International Conference on Computer Design*

[17] https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=4380783.

AMD EX1021
AMD v. Realtek - Page 40

2006 obtained from the OCLC bibliographic database. I personally identified and retrieved the MARC record that is Attachment 3B. As previously noted, the library that created the record is recorded in field 040 with a unique library code. For Attachment 3B, that library code is "W2U," which means that the MARC record for this conference proceedings volume was cataloged at the Wilfrid Library at Laurier University (Waterloo, Ontario, Canada). As can be seen in the "Entered" field in the MARC record for this exhibit, a cataloger in the Wilfrid Library at Laurier University created OCLC record number 613544548 on November 18, 2005, as shown in the "Entered" field ("20051118"). The library continues to update this MARC record and enhanced the MARC record to meet current cataloging rules. The most recent enhancement to the MARC record occurred on April 28, 2022, as shown in the "Replaced" field ("20220428").

72. Attachment 3B further includes an entry in field 050 ("TK7888.3")—as described above, a subject matter classification number consistent with the Library of Congress classification system (analogous to the Dewey Decimal classification system). Attachment 3B also shows that Attachment 3 was catalogued with five descriptor terms reading "Computer engineering $v Congresses" (see Attachment 1H, Library of Congress subject heading sh2009121192), "Embedded computer systems $v Congresses" (see Attachment 3C, Library of Congress subject heading sh2008102939), "Integrated circuits $x

Very large scale integration $v Congresses" (see Attachment 1G, Library of Congress subject heading sh2008104263), "Electronic digital computers $x Circuits $v Congresses" (see Attachment 1F, Library of Congress subject heading sh2009124809), "Microcomputers $x Design and construction $v Congresses" (see Attachment 1C, Library of Congress subject heading sh85084804, Attachment 1D, Library of Congress subject heading sh87005579, and Attachment 1E, Library of Congress subject heading sh85031115) and in the 650 fields. Thus, as of its cataloging, the publication corresponding to the MARC record attached hereto as Attachment 3B was indexed according to its subject matter by virtue of at least two independently sufficient classifications: the field 050 entry and the field 650 entries. Further, as of November 18, 2005, the MARC record attached hereto as Attachment 3B was accessible through any library with access to the OCLC bibliographic database or the online catalog at a library that acquired the conference proceedings volume.

73. Attachment 3B indicates that the volume titled *International Conference on Computer Design 2006* as cataloged in the Wilfrid Library at Laurier University is currently available from 30 libraries. For these reasons, it is my opinion that Attachment 3 was published and publicly accessible at least as early as November 18, 2005.

AMD EX1021
AMD v. Realtek - Page 42

D. PUBLICATION 4: "Power-Gating Aware Floorplanning" by Hailin Jiang and Malgorzata Marek-Sadowska. ("Jiang 2007")

74. Attached hereto as Attachment 4 is a copy of a conference paper published in the volume titled *Eighth International Symposium on Quality Electronic Design: Proceedings* found in the Linda Hall Library of Science, Engineering & Technology (Kansas City, Missouri). The conference paper titled "Power-Gating Aware Floorplanning" by Hailin Jiang and Malgorzata Marek-Sadowska (hereafter "Jiang 2007") appears beginning on page 853. The Eighth International Symposium on Quality Electronic Design was held on March 26-28, 2007, in San José, California. Attachment 4 is a true and correct copy of the Jiang 2007 conference paper (pages 853-858). I obtained this copy of the conference paper from the Linda Hall Library of Science, Engineering & Technology. Specifically, the text of the Jiang 2007 conference paper is complete; no pages are missing, and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. Attachment 4 was found within the custody of a library—a place where, if authentic, a copy of this conference proceedings volume would likely be. Attachment 4 is a true and correct copy in a condition that creates no suspicion about authenticity.

75. The Jiang 2007 conference paper is also available in the *IEEE Xplore*

database,[18] added on April 10, 2007, the *ACM Digital Library*,[19] published March 26, 2007, and the digital repository *Semantic Scholar*.[20]

76. Attached hereto as Attachment 4A is a true and correct copy of the MARC record for this conference proceedings volume from the Linda Hall Library of Science, Engineering & Technology online catalog. The library ownership is indicated by the presence of the library's code (LHL) in field 049. The most recent enhancement to the MARC record occurred on May 6, 2008, as shown in field 005 ("20080506"). I personally identified and retrieved the library catalog record which is Attachment 4A.

77. Based on finding a copy of Attachment 4 in the Linda Hall Library of Science, Engineering & Technology and MARC record in its online library catalog attached as Attachment 4A, it is my opinion that the book titled *Eighth International Symposium on Quality Electronic Design: Proceedings* was publicly available at the Linda Hall Library of Science, Engineering & Technology as of June 6, 2007, as indicated in field 008 ("070606").

78. Attached hereto as Attachment 4B is a true and correct copy of the

---

[18] https://ieeexplore.ieee.org/document/4149140.

[19] https://dl.acm.org/doi/abs/10.1109/ISQED.2007.123.

[20] https://www.semanticscholar.org/paper/Power-Gating-Aware-Floorplanning-Jiang-Marek-Sadowska/045fb9ec269be637f3b10bfe73aa95b54b9176b9.

AMD EX1021
AMD v. Realtek - Page 44

MARC record for the volume titled *Eighth International Symposium on Quality Electronic Design: Proceedings* obtained from the OCLC bibliographic database. I personally identified and retrieved the MARC record that is Attachment 4B. As previously noted, the library that created the record is recorded in field 040 with a unique library code. For Attachment 4B, that library code is "LHL," which means that the MARC record for this conference proceedings volume was cataloged at the Linda Hall Library of Science, Engineering & Technology. As can be seen in the "Entered" field in the MARC record for this exhibit, a cataloger at the Linda Hall Library of Science, Engineering & Technology created OCLC record number 138289590 on June 6, 2007, as shown in the "Entered" field ("20070606"). The library continues to update this MARC record and enhanced the MARC record to meet current cataloging rules. The most recent enhancement to the MARC record occurred on June 10, 2022, as shown in the "Replaced" field ("20220610").

79. Attachment 4B further includes an entry in field 090 ("TK7874.75 $b .I565 2007")—as described above, a subject matter classification number consistent with the Library of Congress classification system (analogous to the Dewey Decimal classification system) and an entry in field 082 ("621.39/5")—as described above, a subject matter classification number consistent with the Dewey Decimal classification system. Attachment 4B also shows that Attachment 4 was catalogued with four descriptor terms reading "Integrated circuits $x Very large

scale integration $x Reliability $v Congresses" (see Attachment 4C, Library of Congress subject heading sh85067125, Attachment 4D, Library of Congress subject heading sh85112510, and Attachment 1E, Library of Congress subject heading sh85031115), "Integrated circuits $x Very large scale integration $x Design and construction $v Congresses" (see Attachment 4E, Library of Congress subject heading sh2008104743), "Integrated circuits $x Very large scale integration $x Computer-aided design $v Congresses" (see Attachment 4F, Library of Congress subject heading sh2008123907), and "Integrated circuits $x Very large scale integration $x Testing $x Quality control $v Congresses" (see Attachment 4G, Library of Congress subject heading sh2009127319, Attachment 4H, Library of Congress subject heading sh85109440, and Attachment 1E, Library of Congress subject heading sh85031115) and in the 650 fields. Thus, as of its cataloging, the publication corresponding to the MARC record attached hereto as Attachment 4B was indexed according to its subject matter by virtue of at least two independently sufficient classifications: the field 050 entry and the field 650 entries. Further, as of November 18, 2005, the MARC record attached hereto as Attachment 4B was accessible through any library with access to the OCLC bibliographic database or the online catalog at a library that acquired the conference proceedings volume.

80. Attachment 4B indicates that the volume titled *Eighth International Symposium on Quality Electronic Design: Proceedings* as cataloged at the Linda

Hall Library of Science, Engineering & Technology is currently available from 5 libraries. For these reasons, it is my opinion that Attachment 4 was published and publicly accessible at least as early as March 26, 2007.

E. PUBLICATION 5: "Minimizing Inductive Noise in System-On-a-Chip with Multiple Power Gating Structures" by Suhwan Kim, Stephen V. Kosonocky, Daniel R. Knebel, Kevin Stawiasz, David Heidel, and Mike Immediato. ("Kim")

81. Attached hereto as Attachment 5 is a copy of a conference paper published in the volume titled *ESSCIRC 2003: Proceedings of the 29th European Solid-State Circuits Conference* found in the Linda Hall Library of Science, Engineering & Technology (Kansas City, Missouri). The conference paper titled "Minimizing Inductive Noise in System-On-a-Chip with Multiple Power Gating Structures" by Suhwan Kim, Stephen V. Kosonocky, Daniel R. Knebel, Kevin Stawiasz, David Heidel, and Mike Immediato (hereafter "Kim") appears beginning on page 635. The 29th European Solid-State Circuits Conference was held on September 15-18, 2003, in Estorial, Portugal. Attachment 5 is a true and correct copy of the Kim conference paper (pages 635-638). I obtained this copy of the conference paper from the Linda Hall Library of Science, Engineering & Technology. Specifically, the text of the Kim conference paper is complete; no pages are missing, and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. Attachment 5 was found within the custody of a library—a place

where, if authentic, a copy of this conference proceedings volume would likely be. Attachment 5 is a true and correct copy in a condition that creates no suspicion about authenticity.

82. The Kim conference paper is also available in the *IEEE Xplore* database,[21] added on January 14, 2004, and the digital repository *ResearchGate*.[22]

83. Attached hereto as Attachment 5A is a true and correct copy of the MARC record for this conference proceedings volume from the Linda Hall Library of Science, Engineering & Technology online catalog. The library ownership is indicated by the presence of the library's code (LHL) in field 049. The most recent enhancement to the MARC record occurred on February 8, 2006, as shown in field 005 ("20060208"). I personally identified and retrieved the library catalog record which is Attachment 5A.

84. Based on finding a copy of Attachment 5 in the Linda Hall Library of Science, Engineering & Technology and MARC record in its online library catalog attached as Attachment 5A, it is my opinion that the book titled *ESSCIRC 2003: Proceedings of the 29th European Solid-State Circuits Conference* was publicly

---

[21] https://ieeexplore.ieee.org/document/1257215.

[22] https://www.researchgate.net/publication/224745461_Minimizing_inductive_noise_in_system-on-a-chip_with_multiple_power_Gating_structures.

AMD EX1021
AMD v. Realtek - Page 48

available at the Linda Hall Library of Science, Engineering & Technology as of January 5, 2004, as indicated in field 008 ("040105").

85. Attached hereto as Attachment 5B is a true and correct copy of the MARC record for the volume titled *ESSCIRC 2003: Proceedings of the 29th European Solid-State Circuits Conference* obtained from the OCLC bibliographic database. I personally identified and retrieved the MARC record that is Attachment 5B. As previously noted, the library that created the record is recorded in field 040 with a unique library code. For Attachment 5B, that library code is "LHL," which means that the MARC record for this conference proceedings volume was cataloged at the Linda Hall Library of Science, Engineering & Technology. As can be seen in the "Entered" field in the MARC record for this exhibit, a cataloger at the Linda Hall Library of Science, Engineering & Technology created OCLC record number 53977408 on January 5, 2004, as shown in the "Entered" field ("20040105"). The library continues to update this MARC record and enhanced the MARC record to meet current cataloging rules. The most recent enhancement to the MARC record occurred on March 11, 2023, as shown in the "Replaced" field ("20230311").

86. Attachment 5B further includes an entry in field 050 ("TK7871.85 $b .E887 2003")—as described above, a subject matter classification number consistent with the Library of Congress classification system (analogous to the

Dewey Decimal classification system) and an entry in field 082 ("621.38152")—as described above, a subject matter classification number consistent with the Dewey Decimal classification system. Attachment 5B also shows that Attachment 5 was catalogued with three descriptor terms reading "Semiconductors $v Congresses" (see Attachment 5C, Library of Congress subject heading sh2008111509), "Integrated circuits $v Congresses" (see Attachment 5D, Library of Congress subject heading sh2008104261), and "Solid state electronics $v Congresses" (see Attachment 5E, Library of Congress subject heading sh2008111513) in the 650 fields. Thus, as of its cataloging, the publication corresponding to the MARC record attached hereto as Attachment 5B was indexed according to its subject matter by virtue of at least three independently sufficient classifications: the field 050 entry, the field 082 entry, and the field 650 entries. Further, as of January 5, 2004, the MARC record attached hereto as Attachment 5B was accessible through any library with access to the OCLC bibliographic database or the online catalog at a library that acquired the conference proceedings volume.

87. Further supporting my opinion that Attachment 5 was publicly accessible to ordinarily skilled and interested researchers in the field is the fact that the book titled *ESSCIRC 2003: Proceedings of the 29th European Solid-State Circuits Conference* was registered with the U. S. Copyright Office as item TX0006054694 on October 27, 2004, and indicated a publication date of

September 16, 2003 (see Attachment 5F, U. S. Copyright Office Public Catalog). As noted above, this would have provided a POSITA with keyword searching capabilities and other tools to locate this book.

88. Attachment 5B indicates that the volume titled *ESSCIRC 2003: Proceedings of the 29th European Solid-State Circuits Conference* as cataloged at the Linda Hall Library of Science, Engineering & Technology is currently available from 17 libraries. For these reasons, it is my opinion that Attachment 5 was published and publicly accessible at least as early as January 5, 2004.

F. PUBLICATION 6: *Low Power Methodology Manual* by Michael Keating, David Flynn, Robert Aitken, Alan Gibbons, and Kaijian Shi. ("Keating")

89. Attached hereto as Attachment 6 is a copy of excerpts of a book titled *Low Power Methodology Manual* by Michael Keating, David Flynn, Robert Aitken, Alan Gibbons, and Kaijian Shi (hereafter "Keating") and issued by Springer Science+Media with a 2007 copyright date. Attachment 6 is a true and correct copy of the title page, copyright page, table of contents, and excerpts as held by the University of California – Berkeley Libraries. The excerpts include Chapter 2, "Standard Low Power Methods" (pp. 13-19); Chapter 3, "Multi-Voltage Design" (pp. 21-31); Chapter 7, "A Power Gating Example" (pp. 85-100); Chapter 11, "Implementing Multi-Voltage, Power Gated Designs" (pp. 155-186); and, Appendix B, "UPF Command Syntax" (pp. 267-292). I obtained Attachment 6

through counsel from the University of California – Berkeley Libraries. The text in Attachment 6 is complete; no pages are missing, and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. Attachment 6 is a true and correct copy in a condition that creates no suspicion about its authenticity.

90. Attached hereto as Attachment 6A is a true and correct copy of the MARC record for this monograph from the University of California – Berkeley Libraries online catalog. The library ownership is indicated by the presence of the library's code (CUY) in the 035 field. The library continues to update this MARC record and enhanced the MARC record to meet current cataloging rules. The most recent enhancement to the MARC record occurred on November 27, 2007, as shown in field 005 field ("20071127"). I personally identified and retrieved the library catalog record which is Attachment 6A.

91. Based on finding a print copy of the Keating book in the University of California – Berkeley Libraries and MARC record in its online library catalog attached as Attachment 6A, it is my opinion that the book titled *Low Power Methodology Manual* was publicly available on October 11, 2007, as shown in field 008 ("071011"). The International Standard Book Number (ISBN) on Attachment 8 (978-0-387-71818-7) matches the ISBN in the first field 020 of Attachment 6A. Therefore, Attachment 6 is the same book as the one that the

cataloger at the University of California – Berkeley Libraries used to create the MARC record that is Attachment 6A.

92. Attached hereto as Attachment 6B is a true and correct copy of the MARC record for the Keating book titled *Low Power Methodology Manual* obtained from the OCLC bibliographic database. I personally identified and retrieved the MARC record that is Attachment 6B. As previously noted, the library that created the record is recorded in field 040 with a unique library code. For Attachment 6B, that library code is "DLC," which means that the MARC record for this book was created at the Library of Congress. As can be seen in the "Entered" field in the MARC record for this exhibit, a cataloger at the Library of Congress created OCLC record number 156812961 on May 7, 2007, as shown in the "Entered" field ("20070507") as part of the Cataloging in Publication Program.[23] The library continues to update and enhance this MARC record to meet current cataloging rules. The most recent enhancement to Attachment 6B occurred on April 28, 2022, as shown in the "Replaced" field ("20220428"). I personally identified and retrieved the MARC record that is Attachment 6B.

93. Attachment 6B further includes an entry in field 050 ("TK7874.66 $b .L67 2007")—as described above, this includes a subject matter classification number consistent with the Library of Congress classification system (analogous to

[23] https://www.loc.gov/publish/cip/.

the Dewey Decimal classification system) and an entry in field 082 ("621.381")—as described above, this includes a subject matter classification number consistent with the Dewey Decimal classification system. Attachment 6B further includes two descriptor terms reading "Low voltage integrated circuits" (see Attachment 6C, Library of Congress subject heading sh95004622) and "Systems on a chip" (see Attachment 6D, Library of Congress subject heading sh2002000568) in the 650 fields. Thus, as of its cataloging, the publication corresponding to the MARC record attached hereto as Attachment 6B was indexed according to its subject matter by virtue of at least three independently sufficient classifications: the field 050 entry, the field 082 entry, and the field 650 entries. Further, as of May 7, 2007, the MARC record attached hereto as Attachment 6B was accessible through any library with access to the OCLC bibliographic database or the online catalog at a library that added this book to its collection.

94. Further supporting my opinion that Attachment 6 was publicly accessible to ordinarily skilled and interested researchers in the field is the fact that the book titled *Low Power Methodology Manual* was registered with the U.S. Copyright Office as item TX0007433405 on October 13, 2011, and indicated a publication date of July 31, 2007 (see Attachment 6E, U.S. Copyright Office Public Catalog). As noted above, this would have provided a POSITA with keyword searching capabilities and other tools to locate this book.

95. Attachment 6B indicates that the Keating book titled *Low Power Methodology Manual* as cataloged at the Library of Congress is currently available from 67 libraries. For these reasons, it is my opinion that Attachment 6 was published and accessible to the public at least as early as July 31, 2007.

G. PUBLICATION 7: "A Pseudo-Hierarchical Methodology for High Performance Microprocessor Design" by A. Bertolet, K. Carpenter, K. Carrig, A. Chu, A. Dean, F. Ferraiolo, S. Kenyon, D. Phan, J. Petrovick, G. Rodgers, D. Willmott, T. Bairley, Q, T. Decker, V. Girardi, B, Y. Lapid, M. Murphy, P. A. Scott, and R. Weiss. ("Bertolet")

96. Attached hereto as Attachment 7 is a copy of a conference paper published in the volume titled *Proceedings: 1997 International Symposium on Physical Design* found in the Georgia Institute of Technology Library (Atlanta, Georgia). The conference paper titled "A Pseudo-Hierarchical Methodology for High Performance Microprocessor Design" by A. Bertolet, K. Carpenter, K. Carrig, A. Chu, A. Dean, F. Ferraiolo, S. Kenyon, D. Phan, J. Petrovick, G. Rodgers, D. Willmott, T. Bairley, Q, T. Decker, V. Girardi, B, Y. Lapid, M. Murphy, P. A. Scott, and R. Weiss (hereafter "Bertolet") appears beginning on page 124. The 1997 International Symposium on Physical Design was held on April 14-16, 1996, in Napa Valley, California. Attachment 7 is a true and correct copy of the Bertolet conference paper (pages 124-19). I obtained this copy of the conference paper from the Georgia Institute of Technology Library. Specifically, the text of the Bertolet conference paper is complete; no pages are missing, and the

text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. Attachment 7 was found within the custody of a library—a place where, if authentic, a copy of this conference proceedings volume would likely be. Attachment 7 is a true and correct copy in a condition that creates no suspicion about authenticity.

97. The Bertolet conference paper is also available in the *ACM Digital Library*,[24] added on April 1, 1997.

98. Attached hereto as Attachment 7A is a true and correct copy of the metadata record for this conference proceedings volume from the Georgia Institute of Technology Library online catalog. The library ownership is indicated by the presence of the library's code (GAT) in field 049. I personally identified and retrieved the library catalog record which is Attachment 7A.

99. Attached hereto as Attachment 7B is a true and correct copy of the MARC record for the volume titled *Proceedings: 1997 International Symposium on Physical Design* obtained from the OCLC bibliographic database. I personally identified and retrieved the MARC record that is Attachment 7B. As previously noted, the library that created the record is recorded in field 040 with a unique library code. For Attachment 7B, that library code is "GAT," which means that the MARC record for this conference proceedings volume was cataloged at the

[24] https://dl.acm.org/doi/10.1145/267665.267702.

AMD EX1021
AMD v. Realtek - Page 56

Georgia Institute of Technology Library.

100. Based on finding a copy of Attachment 7 in the Georgia Institute of Technology Library and metadata record in its online library catalog attached as Attachment 7A, it is my opinion that the book titled *Proceedings: 1997 International Symposium on Physical Design* was publicly available at the Georgia Institute of Technology as of May 26, 1999, as indicated in the "Entered" field ("19990526").

101. As can be seen in the "Entered" field in the MARC record for this exhibit, a cataloger at the Georgia Institute of Technology Library created OCLC record number 41436664 on May 26, 1999. The library continues to update this MARC record and enhanced the MARC record to meet current cataloging rules. The most recent enhancement to the MARC record occurred on October 25, 2022, as shown in the "Replaced" field ("20221025").

102. Attachment 7B further includes an entry in field 050 ("TK7874.75 $b .I58 1997")—as described above, a subject matter classification number consistent with the Library of Congress classification system (analogous to the Dewey Decimal classification system). Attachment 7B also shows that Attachment 7 was catalogued with two descriptor terms reading "Integrated circuits $x Very large scale integration $v Congresses" (see Attachment 1G, Library of Congress subject heading sh2008104263) and "Integrated circuits $x Design and construction $v

AMD EX1021
AMD v. Realtek - Page 57

Congresses" (see Attachment 7C, Library of Congress subject heading sh2008104738) in the 650 fields. Thus, as of its cataloging, the publication corresponding to the MARC record attached hereto as Attachment 7B was indexed according to its subject matter by virtue of at least two independently sufficient classifications: the field 050 entry and the field 650 entries. Further, as of May 26, 1999, the MARC record attached hereto as Attachment 7B was accessible through any library with access to the OCLC bibliographic database or the online catalog at a library that acquired the conference proceedings volume.

103. Further supporting my opinion that Attachment 7 was publicly accessible to ordinarily skilled and interested researchers in the field is the fact that the book titled *Proceedings: 1997 International Symposium on Physical Design* was registered with the U. S. Copyright Office as item TX0005077849 on October 25, 1999, and indicated a publication date of March 31, 1997 (see Attachment 7D, U. S. Copyright Office Public Catalog). As noted above, this would have provided a POSITA with keyword searching capabilities and other tools to locate this book.

104. Attachment 7B indicates that the volume titled *Proceedings: 1997 International Symposium on Physical Design* as cataloged at the Georgia Institute of Technology Library is currently available from 6 libraries. For these reasons, it is my opinion that Attachment 7 was published and publicly accessible at least as early as April 1, 1997, and in print on May 26, 1999.

AMD EX1021
AMD v. Realtek - Page 58

H. PUBLICATION 8: "Advanced Power Management Techniques: Going Beyond Intelligent Shutdown" by Luca Benini. ("Benini")

105. Attached hereto as Attachment 8 is a copy of a conference paper published in the volume titled *Proceedings of the ASP-DAC 2003: Asia and South Pacific Design Automation Conference 2003* found in the University of Wisconsin – Madison Libraries. The conference paper titled "Advanced Power Management Techniques: Going Beyond Intelligent Shutdown" by Luca Benini (hereafter "Benini") appears beginning on page 385. The ASP-DAC 2003: Asia and South Pacific Design Automation Conference was held on January 21-24, 2004, in Kitakyushu, Japan. Attachment 8 is a true and correct copy of the Benini conference paper (pages 385-389). I obtained this copy of the conference paper from the University of Wisconsin – Madison Libraries. Specifically, the text of the Benini conference paper is complete; no pages are missing, and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. Attachment 8 was found within the custody of a library—a place where, if authentic, a copy of this conference proceedings volume would likely be. Attachment 8 is a true and correct copy in a condition that creates no suspicion about authenticity.

106. The Benini conference paper is also available in the *ACM Digital*

Library,[25] added on January 14, 2004.

107. Attached hereto as Attachment 8A is a true and correct copy of the MARC record for this conference proceedings volume from the University of Wisconsin – Madison Libraries online catalog. The library ownership is indicated by the presence of the library's name at the top of the screen. I personally identified and retrieved the library catalog record which is Attachment 8A.

108. Attached hereto as Attachment 8B is a true and correct copy of the MARC record for the volume titled *Proceedings of the ASP-DAC 2003: Asia and South Pacific Design Automation Conference 2003* obtained from the OCLC bibliographic database. I personally identified and retrieved the MARC record that is Attachment 8B. As previously noted, the library that created the record is recorded in field 040 with a unique library code. For Attachment 8B, that library code is "ZCU," which means that the MARC record for this conference proceedings volume was cataloged at the Columbia University Libraries (New York, New York). As can be seen in the "Entered" field in the MARC record for this exhibit, a cataloger at the Columbia University Libraries created OCLC record number 51906952 on March 24, 2003, as shown in the "Entered" field ("20030324"). The library continues to update this MARC record and enhanced the MARC record to meet current cataloging rules. The most recent enhancement

[25] https://dl.acm.org/doi/abs/10.1145/1119772.1119848.

to the MARC record occurred on February 16, 2023, as shown in the "Replaced" field ("20230216").

109. Attachment 8B further includes an entry in field 050 ("TK7874 $b .A759 2003")—as described above, a subject matter classification number consistent with the Library of Congress classification system (analogous to the Dewey Decimal classification system) and an entry in field 082 ("621.3815")—as described above, a subject matter classification number consistent with the Dewey Decimal classification system. Attachment 8B also shows that Attachment 8 was catalogued with two descriptor terms reading "Integrated circuits $x Computer-aided design $v Congresses" (see Attachment 8C, Library of Congress subject heading sh2009127317) and "Electronic circuit design $x Data processing $v Congresses" (see Attachment 8D, Library of Congress subject heading sh2008102924) in the 650 fields. Thus, as of its cataloging, the publication corresponding to the MARC record attached hereto as Attachment 8B was indexed according to its subject matter by virtue of at least three independently sufficient classifications: the field 050 entry, the field 082 entry, and the field 650 entries. Further, as of March 24, 2003, the MARC record attached hereto as Attachment 8B was accessible through any library with access to the OCLC bibliographic database or the online catalog at a library that acquired the conference proceedings volume.

110. Further supporting my opinion that Attachment 8 was publicly accessible to ordinarily skilled and interested researchers in the field is the fact that the book titled *Proceedings of the ASP-DAC 2003: Asia and South Pacific Design Automation Conference 2003* was registered with the U. S. Copyright Office as item TX0005705561 on March 20, 2003 and indicated a publication date of January 21, 2003 (see Attachment 8E, U. S. Copyright Office Public Catalog). As noted above, this would have provided a POSITA with keyword searching capabilities and other tools to locate this book.

111. Attachment 8B indicates that the volume titled *Proceedings of the ASP-DAC 2003: Asia and South Pacific Design Automation Conference 2003* as cataloged at the Columbia University Libraries is currently available from 14 libraries. For these reasons, it is my opinion that Attachment 8 was published and publicly accessible at least as early as January 21, 2003 online, and March 24, 2003 in print.

I. PUBLICATION 9: "Via-Configurable Routing Architectures and Fast Design Mappability Estimation for Regular Fabrics" by Yajun Ran and Malgorzata Marek-Sadowska. ("Ran")

112. Attached hereto as Attachment 9 is a copy of a conference paper published in the volume titled *ICCAD-2005: International Conference on Computer Aided Design* found in the University of Wisconsin – Madison Libraries. The conference paper titled "Via-Configurable Routing Architectures and Fast

AMD EX1021
AMD v. Realtek - Page 62

Design Mappability Estimation for Regular Fabrics" by Yajun Ran and Malgorzata Marek-Sadowska (hereafter "Ran") appears beginning on page 25. The ICCAD-2005: International Conference on Computer Aided Design was held on November 6-10, 2005, in San José, California. Attachment 9 is a true and correct copy of the Ran conference paper (pages 25-32). I obtained this copy of the conference paper from the University of Wisconsin – Madison Libraries. Specifically, the text of the Ran conference paper is complete; no pages are missing, and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. Attachment 9 was found within the custody of a library—a place where, if authentic, a copy of this conference proceedings volume would likely be. Attachment 9 is a true and correct copy in a condition that creates no suspicion about authenticity.

113. The Ran conference paper is also available in the *ACM Digital Library*,[26] added on May 31, 2005, the *IEEE Xplore database*,[27] added on December 15, 2005, and the digital repository *Semantic Scholar*.[28]

114. Attached hereto as Attachment 9A is a true and correct copy of the

[26] https://dl.acm.org/doi/10.5555/1129601.1129606.

[27] https://ieeexplore.ieee.org/document/1560035.

[28] https://www.semanticscholar.org/paper/Via-configurable-routing-architectures-and-fast-for-Ran-Marek-Sadowska/c6a0c551deced413a94b172cebc82f8296c11290.

MARC record for this conference proceedings volume from the University of Wisconsin – Madison Libraries online catalog. The library ownership is indicated by the presence of the library's name at the bottom of the screen. I personally identified and retrieved the library catalog record which is Attachment 9A.

115. Attached hereto as Attachment 9B is a true and correct copy of the MARC record for the volume titled *ICCAD-2005: International Conference on Computer Aided Design* obtained from the OCLC bibliographic database. I personally identified and retrieved the MARC record that is Attachment 9B. As previously noted, the library that created the record is recorded in field 040 with a unique library code. For Attachment 9B, that library code is "NRC," which means that the MARC record for this conference proceedings volume was cataloged at the North Carlina State University – Raleigh Libraries. As can be seen in the "Entered" field in the MARC record for this exhibit, a cataloger at the North Carolina State University – Raleigh Libraries created OCLC record number 6520971 on December 9, 2005, as shown in the "Entered" field ("20051209"). The library continues to update this MARC record and enhanced the MARC record to meet current cataloging rules. The most recent enhancement to the MARC record occurred on June 23, 2022, as shown in the "Replaced" field ("20220623").

116. Attachment 9B further includes an entry in field 050 ("TK7867 $b .I3713 2005")—as described above, a subject matter classification number

consistent with the Library of Congress classification system (analogous to the Dewey Decimal classification system) and an entry in field 082 ("621.3815")—as described above, a subject matter classification number consistent with the Dewey Decimal classification system. Attachment 9B also shows that Attachment 9 was catalogued with three descriptor terms reading "Electronic circuit design $x Data processing $v Congresses" (see Attachment 8D, Library of Congress subject heading sh2008102924), "Computer-aided design $v Congresses" (see Attachment 9C, Library of Congress subject heading sh2008101464), and "Electronic circuits $x Testing $v Congresses" (see Attachment 9D, Library of Congress subject heading sh85042282 and Attachment 1E, Library of Congress subject heading sh85031115) in the 650 fields. Thus, as of its cataloging, the publication corresponding to the MARC record attached hereto as Attachment 9B was indexed according to its subject matter by virtue of at least three independently sufficient classifications: the field 050 entry, the field 082 entry, and the field 650 entries. Further, as of December 9, 2005, the MARC record attached hereto as Attachment 9B was accessible through any library with access to the OCLC bibliographic database or the online catalog at a library that acquired the conference proceedings volume.

117. Further supporting my opinion that Attachment 9 was publicly accessible to ordinarily skilled and interested researchers in the field is the fact that

the book titled *ICCAD-2005: International Conference on Computer Aided Design* was registered with the U. S. Copyright Office as item TX0006287270 on November 22, 2005, and indicated a publication date of November 11, 2005 (see Attachment 9E, U. S. Copyright Office Public Catalog). As noted above, this would have provided a POSITA with keyword searching capabilities and other tools to locate this book.

118. Attachment 9B indicates that the volume titled *ICCAD-2005: International Conference on Computer Aided Design* as cataloged at the North Carolina State University – Raleigh Libraries is currently available from 46 libraries. For these reasons, it is my opinion that Attachment 9 was published and publicly accessible at least as early as May 31, 2005 online, and December 9, 2005 in print.

J. PUBLICATION 10: "Low-Power Design Methodology and Applications Utilizing Dual Supply Voltages" by Kimiyoshi Usami and Mutsunori Igarashi. ("Usami")

119. Attached hereto as Attachment 10 is a copy of a conference paper published in the volume titled *Proceedings of the ASP-DAC 2000: Asia and South Pacific Design Automation Conference, 2000* found in the Linda Hall Library of Science, Engineering & Technology (Kansas City, Missouri). The conference paper titled "Low-Power Design Methodology and Applications Utilizing Dual Supply Voltages" by Kimiyoshi Usami and Mutsunori Igarashi (hereafter

AMD EX1021
AMD v. Realtek - Page 66

"Usami") appears beginning on page 123. The ASP-DAC 2000: Asia and South Pacific Design Automation Conference, 2000 was held on January 25-28, 2000, in Yokohama, Japan. Attachment 10 is a true and correct copy of the Usami conference paper (pages 123-128). I obtained this copy of the conference paper from the Linda Hall Library of Science, Engineering & Technology. Specifically, the text of the Usami conference paper is complete; no pages are missing, and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. Attachment 10 was found within the custody of a library—a place where, if authentic, a copy of this conference proceedings volume would likely be. Attachment 10 is a true and correct copy in a condition that creates no suspicion about authenticity.

120. The Usami conference paper is also available in the *IEEE Xplore* database,[29] added on August 6, 2002, the *ACM Digital Library*,[30] added on January 28, 2000, and the digital repositories *ResearchGate*[31] and *Semantic Scholar*.[32]

121. Attached hereto as Attachment 10A is a true and correct copy of the

---

[29] https://ieeexplore.ieee.org/document/835082/similar#similar.

[30] https://dl.acm.org/doi/10.1145/368434.368590.

[31] https://www.researchgate.net/publication/221154567_Low-power_design_methodology_and_applications_utilizing_dual_supply_voltages.

[32] https://www.semanticscholar.org/paper/Low-power-design-methodology-and-applications-dual-Usami-Igarashi/4061ef9410a85234ae5c0301eb6d92fb2f04ff67.

MARC record for this conference proceedings volume from the Linda Hall Library of Science, Engineering & Technology online catalog. The library ownership is indicated by the presence of the library's code (LHL) in field 049. The most recent enhancement to the MARC record occurred on January 17, 2002, as shown in field 005 ("20020117"). I personally identified and retrieved the library catalog record which is Attachment 10A.

122. Based on finding a copy of Attachment 10 in the Linda Hall Library of Science, Engineering & Technology and MARC record in its online library catalog attached as Attachment 10A, it is my opinion that the book titled *Proceedings of the ASP-DAC 2000: Asia and South Pacific Design Automation Conference, 2000* was publicly available at the Linda Hall Library of Science, Engineering & Technology as of May 27, 1998, as indicated in field 005 ("980527").

123. Attached hereto as Attachment 10B is a true and correct copy of the MARC record for the volume titled *Proceedings of the ASP-DAC 2000: Asia and South Pacific Design Automation Conference* obtained from the OCLC bibliographic database. I personally identified and retrieved the MARC record that is Attachment 10B. As previously noted, the library that created the record is recorded in field 040 with a unique library code. For Attachment 10B, that library code is "DLC," which means that the MARC record for this conference

AMD EX1021
AMD v. Realtek - Page 68

proceedings volume was cataloged at the Library of Congress. As can be seen in the "Entered" field in the MARC record for this exhibit, a cataloger at the Library of Congress created OCLC record number 43950158 on May 27, 1998, as shown in the "Entered" field ("19980527"). The library continues to update this MARC record and enhanced the MARC record to meet current cataloging rules. The most recent enhancement to the MARC record occurred on November 30, 2022, as shown in the "Replaced" field ("20221130").

124. Attachment 10B further includes an entry in field 050 ("QA76.6 $b .A78 2000")—as described above, a subject matter classification number consistent with the Library of Congress classification system (analogous to the Dewey Decimal classification system). Attachment 10B also shows that Attachment 10 was catalogued with two descriptor terms reading "Integrated circuits $x Computer-aided design $v Congresses" (see Attachment 8C, Library of Congress subject heading sh2009127317) and "Electronic circuit design $x Data processing $v Congresses" (see Attachment 8D, Library of Congress subject heading sh2008102924) in the 650 fields. Thus, as of its cataloging, the publication corresponding to the MARC record attached hereto as Attachment 10B was indexed according to its subject matter by virtue of at least two independently sufficient classifications: the field 050 entry and the field 650 entries. Further, as of May 27, 1998, the MARC record attached hereto as Attachment 10B was

accessible through any library with access to the OCLC bibliographic database or the online catalog at a library that acquired the conference proceedings volume.

125. Further supporting my opinion that Attachment 10 was publicly accessible to ordinarily skilled and interested researchers in the field is the fact that the book titled *Proceedings of the ASP-DAC 2000: Asia and South Pacific Design Automation Conference* was registered with the U. S. Copyright Office as item TX0005102080 on April 13, 2000 and indicated a publication date of January 25, 2000 (see Attachment 10C, U. S. Copyright Office Public Catalog). As noted above, this would have provided a POSITA with keyword searching capabilities and other tools to locate this book.

126. Attachment 10B indicates that the volume titled *Proceedings of the ASP-DAC 2000: Asia and South Pacific Design Automation Conference* as cataloged at the Library of Congress is currently available from 28 libraries. For these reasons, it is my opinion that Attachment 10 was published and publicly accessible at least as early as January 28, 2000 online, and May 27, 1998 in print.

VIII. SUMMARY OF OPINIONS

127. In view of the foregoing, it is my opinion that the publications described above were publicly available no later than the corresponding date listed in the table below:

AMD EX1021
AMD v. Realtek - Page 70

Attachment	Publication	Publicly Available At Least As Early As
1	Jiang, Hailin, Malgorzata Marek-Sadowska, and Sani R. Nassif. "Benefits and Costs of Power-Gating Technique." In *2005 International Conference on Computer Design: Proceedings* (pp. 559-566). ICCD '05. Los Alamitos, CA: IEEE Computer Society, ©2005.	November 8, 2005
2	Li, Wei, Daniel Blakely, Scott Van Sooy, Kevin Dunn, David Kidd, and Robert Rogenmoser. "LVS Verification across Multiple Power Domains for a Quad-Core Microprocessor." *ACM Transactions on Design Automation of Electronic Systems*, vol. 11, no. 2 (April 2006): 490-500.	April 1, 2006
3	Jiang, Hailin, and Malgorzata Marek-Sadowska. "Power/Ground Supply Network Optimization for Power-Gating." In *International Conference on Computer Design 2006* (pp. 332-337). ICCD '06. Piscataway, NJ: IEEE, ©2006.	November 18, 2005
4	Jiang, Hailin, and Malgorzata Marek-Sadowska. "Power-Gating Aware Floorplanning." In Eighth *International Symposium on Quality Electronic Design: Proceedings* (pp. 853-860). ISQED '07. Los Alamitos, CA: IEEE Computer Society, ©2007.	March 26, 2007
5	Kim, Suhwan, Stephen V. Kosonocky, Daniel R. Knebel, Kevin Stawiasz, David Heidel, and Mike Immediato. "Minimizing Inductive Noise in System-On-a-Chip with Multiple Power Gating Structures." In *ESSCIRC 2003: Proceedings of the 29th European Solid-State Circuits Conference* (pp. 635-638). ESSCIRC 2004. Piscataway, NJ: IEEE, ©2003.	January 5, 2004
6	Keating, Michael, David Flynn, Robert Aitken, Alan Gibbons, and Kaijian Shi. *Low Power Methodology Manual*. New York: Springer Science + Business Media, 2007.	July 31, 2007

AMD EX1021
AMD v. Realtek - Page 71

Attachment	Publication	Publicly Available At Least As Early As
7	Bertolet, A., K. Carpenter, K. Carrig, A. Chu, A. Dean, F. Ferraiolo, S. Kenyon, D. Phan, J. Petrovick, G. Rodgers, D. Willmott, T. Bairley, Q, T. Decker, V. Girardi, B. Y. Lapid, M. Murphy, P. A. Scott, and R. Weiss. "A Pseudo-Hierarchical Methodology for High Performance Microprocessor Design." In *Proceedings: 1997 International Symposium on Physical Design* (pp. 124-129). ISPD '97. New York: Association for Computing Machinery, ©1997.	April 1, 1997
8	Benini, Luca. "Advanced Power Management Techniques: Going Beyond Intelligent Shutdown." In *Proceedings of the ASP-DAC 2003: Asia and South Pacific Design Automation Conference 2003* (pp. 385–389). ASP-DAC '03. Piscataway, NJ: Institute of Electrical and Electronics Engineers, ©2003.	January 21, 2003
9	Ran, Yajun, and Malgorzata Marek-Sadowska. "Via-Configurable Routing Architectures and Fast Design Mappability Estimation for Regular Fabrics." *In ICCAD-2005: International Conference on Computer Aided Design* (pp. 25-32). ICCAD '05. Piscataway, NJ: IEEE, ©2005.	May 31, 2005
10	Usami, Kimiyoshi, and Mutsunori Igarashi. "Low-Power Design Methodology and Applications Utilizing Dual Supply Voltages." In *Proceedings of the ASP-DAC 2000: Asia and South Pacific Design Automation Conference, 2000* (pp. 123-128). Piscataway, NJ: Institute of Electrical and Electronics Engineers, 2000.	May 27, 1998

AMD EX1021
AMD v. Realtek - Page 72

128. In signing this Declaration, I recognize that the Declaration will be filed as evidence in a case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

129. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Date: May 2, 2023

Sylvia D. Hall-Ellis, Ph.D.

AMD EX1021
AMD v. Realtek - Page 73

ATTACHMENT 1

Proceedings

2005 International Conference on Computer Design

02-05 October 2005

San Jose, California

Sponsored by

IEEE Computer Society Design Automation Technical Committee (DATC)

IEEE Circuits and Systems Society



Los Alamitos, California

Washington • Tokyo

Proceedings of the 2005 International Conference on Computer Design (ICCD'05)
0-7695-2451-6/05 $20.00 © 2005 IEEE

AMD EX1021
AMD v. Realtek - Page 75

Copyright © 2005 by The Institute of Electrical and Electronics Engineers, Inc.
All rights reserved.

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries may photocopy beyond the limits of US copyright law, for private use of patrons, those articles in this volume that carry a code at the bottom of the first page, provided that the per-copy fee indicated in the code is paid through the Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

Other copying, reprint, or republication requests should be addressed to: IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, P.O. Box 133, Piscataway, NJ 08855-1331.

The papers in this book comprise the proceedings of the meeting mentioned on the cover and title page. They reflect the authors' opinions and, in the interests of timely dissemination, are published as presented and without change. Their inclusion in this publication does not necessarily constitute endorsement by the editors, the IEEE Computer Society, or the Institute of Electrical and Electronics Engineers, Inc.

IEEE Computer Society Order Number P2451
ISBN 0-7695-2451-6
ISSN 1063-64040

Additional copies may be ordered from:

IEEE Computer Society
Customer Service Center
10662 Los Vaqueros Circle
P.O. Box 3014
Los Alamitos, CA 90720-1314
Tel: + 1 800 272 6657
Fax: + 1 714 821 4641
http://computer.org/cspress
csbooks@computer.org

IEEE Service Center
445 Hoes Lane
P.O. Box 1331
Piscataway, NJ 08855-1331
Tel: + 1 732 981 0060
Fax: + 1 732 981 9667
http://shop.ieee.org/store/
customer-service@ieee.org

IEEE Computer Society
Asia/Pacific Office
Watanabe Bldg., 1-4-2
Minami-Aoyama
Minato-ku, Tokyo 107-0062
JAPAN
Tel: + 81 3 3408 3118
Fax: + 81 3 3408 3553
tokyo.ofc@computer.org

Individual paper REPRINTS may be ordered at: reprints@computer.org

Editorial production by Danielle C. Martin

Cover art production by Joseph Daigle/Studio Productions

Printed in the United States of America by TBA

IEEE COMPUTER SOCIETY

IEEE

IEEE Computer Society
Conference Publishing Services
http://www.computer.org/proceedings/

Table of Contents

2005 International Conference on Computer Design (ICCD 2005)

Welcome Message xiv
Organizing Committee xv
Program Committees xvi
Additional Reviewers xviii

Keynote Presentation

Latency Lags Bandwidth 3
D. Patterson

1.1 Power and Thermal Considerations in Processor Design (I)

Temperature-Dependent Optimization of Cache Leakage Power Dissipation 7
P. Li, Y. Deng, and L. Pileggi

Architectural Considerations for Energy Efficiency 13
H. Dao, B. Zeydel, and V. Oklobdžija

Reducing the Latency and Area Cost of Core Swapping through Shared Helper Engines 17
A. Shayesteh, E. Kursun, T. Sherwood, S. Sair, and G. Reinman

Analytical Model for Sensor Placement on Microprocessors 24
K.-J. Lee, K. Skadron, and W. Huang

1.2 Interconnect Prediction and Optimization

Pre-layout Physical Connectivity Prediction with Application in Clustering-Based Placement 31
Q. Liu and M. Marek-Sadowska

Efficient Rectilinear Steiner Tree Construction with Rectilinear Blockages 38
Z. Shen, C. Chu, and Y.-M. Li

X-Routing Using Two Manhattan Route Instances 45
S. Ahmad, N. Jayakumar, V. Balasubramanian, E. Hursey, S. Khatri, and R. Mahapatra

1.3 System-Level Architecture

Hardware Support for Bulk Data Movement in Server Platforms 53
L. Zhao, R. Iyer, S. Makineni, L. Bhuyan, and D. Newell

Counter-Based Cache Replacement Algorithms 61
M. Kharbutli and Y. Solihin

AMD EX1021
AMD v. Realtek - Page 77
IEEE COMPUTER SOCIETY

Utilizing Horizontal and Vertical Parallelism with a No-Instruction-Set Compiler for Custom Datapaths 69
M. Reshadi, B. Gorjiara, and D. Gajski

Panel Discussion

Are Today's Verification Tools Able to Handle Current Design Challenges? 77
R. Goering, R. Faris, K. Larsen, H. Foster, and S. Swwan

2.1 Power Aware System Design

Energy-Efficient Color Approximation for Digital LCD Interfaces 81
A. Nourrachmat, S. Salerno, E. Macii, and M. Poncino

Application-Specific Power-Aware Workload Allocation for Voltage Scalable MPSoC Platforms 87
M. Ruggiero, A. Acquaviva, D. Bertozzi, and L. Benini

LCD Display Energy Reduction by User Monitoring 94
V. Moshnyaga and E. Morikawa

Frame Buffer Energy Optimization by Pixel Prediction 98
K. Patel, E. Macii, and M. Poncino

Energy and Performance Analysis of Mapping Parallel Multi-threaded Tasks for an On-Chip Multi-processor System 102
B.-C. Lai, P. Schaumont, W. Qin, and I. Verbauwhede

Near-Memory Caching for Improved Energy Consumption 105
N. AbouGhazaleh, B. Childers, D. Mossé, and R. Melhem

2.2 Physical-Aware System-Level Analysis and Synthesis

Physical Synthesis of Energy-Efficient Networks-on-Chip through Topology Exploration and Wire Style Optimization 111
Y. Hu, H. Chen, Y. Zhu, A. Chien, and C.-K. Cheng

A Formal Framework for Modeling and Analysis of System-Level Dynamic Power Management 119
S. Yardi, K. Channakeshava, M. Hsiao, T. Martin, and D. Ha

Efficient Implementation Selection via Time Budgeting: Complexity Analysis and Leakage Optimization Case Study 127
S. Ghiasi

Efficient Thermal Simulation for Run-Time Temperature Tracking and Management 130
H. Li, P. Liu, Z. Qi, L. Jin, W. Wu, S. Tan, and J. Yang

2.3 SoC Test Methods

A Flexible Design Methodology for Analog Test Wrappers in Mixed-Signal SoCs 137
A. Sehgal, S. Ozev, and K. Chakrabarty

AMD EX1021
AMD v. Realtek - Page 78
IEEE COMPUTER SOCIETY

Concurrent Core Test for Test Cost Reduction Using Merged Test Set and Scan Tree 143
G. Zeng and H. Ito

ChiYun Compact: A Novel Test Compaction Technique for Responses with Unknown Values 147
M. Chao, S. Wang, S. Chakradhar, and K.-T. Cheng

Accurate Diagnosis of Multiple Faults 153
Y.-C. Lin, F. Lu, and K.-T. Cheng

Quick Scan Chain Diagnosis Using Signal Profiling 157
J.-S. Yang and S.-Y. Huang

Fast Hierarchical Process Variability Analysis and Parametric Test Development for Analog/RF Circuits 161
F. Liu and S. Ozev

3.1 Reliable Circuit Design

Fault Tolerant Asynchronous Adder through Dynamic Self-Reconfiguration 171
S. Peng and R. Manohar

Error-Tolerance Memory Microarchitecture via Dynamic Multithreading Redundancy 179
L. Wang

A Soft Error Monitor Using Switching Current Detection 185
P. Ndai, A. Agarwal, Q. Chen, and K. Roy

3.2 High Level Synthesis

Applying Resource Sharing Algorithms to ADL-Driven Automatic ASIP Implementation 193
E. Witte, A. Chattopadhyay, O. Schliebusch, D. Kammler, R. Leupers, G. Ascheid, and H. Meyr

Statistical Analysis Driven Synthesis of Asynchronous Systems 200
K. Ohashi and M. Kaneko

Novel Low-Overhead Operand Isolation Techniques for Low-Power Datapath Synthesis 206
N. Banerjee, A. Raychowdhury, S. Bhunia, H. Mahmoodi, and K. Roy

3.3 Verification of SoCs with Datapaths and Software

Exploiting Vanishing Polynomials for Equivalence Verification of Fixed-Size Arithmetic Datapaths 215
N. Shekhar, P. Kalla, F. Enescu, and S. Gopalakrishnan

Incorporating Efficient Assertion Checkers into Hardware Emulation 221
M. Boulé and Z. Zilic

Assertion Checking of Behavioral Descriptions with Non-linear Solver 229
I. Ugarte and P. Sanchez

AMD EX1021
AMD v. Realtek - Page 79
IEEE COMPUTER SOCIETY

File System Interfaces for Embedded Software Development 232
B. Pisupati and G. Brown

Keynote Address

Yesterday and Tomorrow: A View on Progress in Computer Design 239
M. Flynn

4.1 Low Power Circuit Architecture

Ripple-Precharge TCAM: A Low-Power Solution for Network Search Engines 243
D. Vijayasarathi, M. Nourani, M. Akhbarizadeh, and P. Balsara

Low- and Ultra Low-Power Arithmetic Units: Design and Comparison 249
M. Vratonjic, B. Zeydel, and V. Oklobdžija

A Skewed Repeater Bus Architecture for On-Chip Energy Reduction in Microprocessors 253
M. Khellah, M. Ghoneima, J. Tschanz, Y. Ye, N. Kurd, J. Barkatullah, S. Nimmagadda, Y. Ismail, and V. De

Low-Power Design of 90-nm SuperH™ Processor Core 258
T. Yamada, M. Abe, Y. Nitta, K. Ogura, M. Kusaoke, M. Ishikawa, M. Ozawa, K. Takada, F. Arakawa, O. Nishii, and T. Hattori

4.2 Emerging Design Styles and Applications

Asynchronous IC Interconnect Network Design and Implementation Using a Standard ASIC Flow 267
B. Quinton, M. Greenstreet, and S. Wilton

Algorithmic and Architectural Design Methodology for Particle Filters in Hardware 275
A. Sankaranarayanan, R. Chellappa, and A. Srivastava

ALLCN: An Automatic Logic-to-Layout Tool for Carbon Nanotube Based Nanotechnology 281
W. Zhang and N. Jha

Automatic Synthesis of Composable Sequential Quantum Boolean Circuits 289
L.-K. Chang and F.-C. Cheng

4.3 Formal Verification – From Hardware to Software (Invited)

Model Checking C Programs Using F-Soft 297
F. Ivan i , I. Shlyakhter, A. Gupta, M. Ganai, V. Kahlon, C. Wang, and Z. Yang

Dealing with I/O Devices in the Context of Pervasive System Verification 309
M. Hillebrand, T. In der Rieden, and W. Paul

Towards the Formal Verification of Lower System Layers in Automotive Systems 317
S. Beyer, P. Böhm, M. Gerke, M. Hillebrand, T. In der Rieden, S. Knapp, D. Leinenbach, and W. Paul

AMD EX1021
AMD v. Realtek - Page 80
IEEE COMPUTER SOCIETY

5.1 Cache Memory Architecture

Restrictive Compression Techniques to Increase Level 1 Cache Capacity 327
P. Pujara and A. Aggarwal

The TM3270 Media-Processor Data Cache 334
J.-W. van de Waerdt, S. Vassiliadis, J.-P. van Itegem, and H. van Antwerpen

Mitigating Soft Errors in Highly Associative Cache with CAM-Based Tag 342
L. Hung, M. Goshima, and S. Sakai

5.2 Gate Timing and Power Analysis

VGTA: Variation—Aware Gate Timing Analysis 351
S. Abbaspour, H. Fatemi, and M. Pedram

Exact Lower Bound for the Number of Switches in Series to Implement a Combinational Logic Cell 357
F. Schneider, R. Ribas, S. Sapatnekar, and A. Reis

A Waveform Independent Gate Model for Accurate Timing Analysis 363
P. Li and E. Acar

Enhanced Dual-Transition Probabilistic Power Estimation with Selective Supergate Analysis 366
F. Hu and V. Agrawal

5.3 Performance Modeling

Methods for Modeling Resource Contention on Simultaneous Multithreading Processors 373
T. Moseley, J. Kihm, D. Connors, and D. Grunwald

Using Scratchpad to Exploit Object Locality in Java 381
C. Lebsack and J. Chang

Correlation between Detailed and Simplified Simulations in Studying Multiprocessor Architecture 387
K. Ibrahim

Simulating Commercial Java Throughput Workload: A Case Study 393
Y. Luo and L. John

6.1 Low Voltage Design

Minimum Energy Near-Threshold Network of PLA Based Design 399
N. Jayakumar and S. Khatri

Robust Design of High Fan-in/out Subthreshold Circuits 405
J. Chen, L. Clark, and Y. Cao

A Thermally-Aware Methodology for Design-Specific Optimization of Supply and Threshold Voltages in Nanometer Scale ICs 411
S.-C. Lin, N. Srivastava, and K. Banerjee

AMD EX1021
AMD v. Realtek - Page 81
IEEE COMPUTER SOCIETY

A Feasibility Study of Subthreshold SRAM across Technology Generations 417
A. Raychowdhury, S. Mukhopadhyay, and K. Roy

6.2 Physical-Aware Circuit Design

Variability-Driven Buffer Insertion Considering Correlations 425
A. Davoodi and A. Srivastava

A Dual Dielectric Approach for Performance Aware Gate Tunneling Reduction in Combinational Circuits 431
V. Mukherjee, S. Mohanty, and E. Kougianos

Supply Voltage Degradation Aware Analytical Placement 437
A. Kahng, B. Liu, and Q. Wang

Layout-Aware RF Circuit Synthesis Driven by Worst Case Parasitic Corners 444
A. Agarwal and R. Vemuri

6.3 Verification and Test for Sequential Circuits and Delay Fault Models

Extended Forward Implications and Dual Recurrence Relations to Identify Sequentially Untestable Faults 453
M. Syal, R. Arora, and M. Hsiao

Case Study of ATPG-Based Bounded Model Checking: Verifying USB 2.0 IP Core 461
Q. Qiang, C.-L. Chang, D. Saab, and J. Abraham

Towards Finding Path Delay Fault Tests with High Test Efficiency Using ZBDDs 464
M. Michael, K. Christou, and S. Tragoudas

Quality Transition Fault Tests Suitable for Small Delay Defects 468
M. Kumar and S. Tragoudas

A Novel Method of Improving Transition Delay Fault Coverage Using Multiple Scan Enable Signals 471
N. Devtaprasanna, A. Gunda, P. Krishnamurthy, S. Reddy, and I. Pomeranz

At-Speed Logic BIST Architecture for Multi-clock Designs 475
L.-T. Wang, X. Wen, P.-C. Hsu, S. Wu, and J. Guo

Hardware Efficient LBIST with Complementary Weights 479
L. Lai, J. Patel, T. Rinderknecht, and W.-T. Cheng

7.1 New Memory Technologies (Invited)

FRAM Memory Technology – Advantages for Low Power, Fast Write, High Endurance Applications 485
R. Bailey, G. Fox, J. Eliason, M. Depner, D. Kim, E. Jabillo, J. Groat, J. Walbert, T. Moise, S. Summerfelt, K. Udayakumar, J. Rodriquez, K. Remack, K. Boku, and J. Gertas

Thermal MRAM
J. Deak

AMD EX1021
AMD v. Realtek - Page 82
IEEE COMPUTER SOCIETY

Future Directions of Non-volatile Memory Technologies
A. Fazio

8.1 High Performance Designs

A High Performance Sub-pipelined Architecture for AES 491
H. Li and J. Li

Surfliner: A Distortionless Electrical Signaling Scheme for Speed of Light On-Chip Communications 497
H. Chen, R. Shui, C.-K. Cheng, and D. Harris

Partial-Parallel LDPC Decoder Based on High-Efficiency Message-Passing Algorithm 503
K. Shimizu, T. Ishikawa, N. Togawa, T. Ikenaga, and S. Goto

Fast Minimum and Maximum Selection 511
A. Grushin

8.2 Future VLSI Technologies and Their Impact

Three-Dimensional Cache Design Exploration Using 3DCacti 519
Y.-F. Tsai, Y. Xie, N. Vijaykrishnan, and M. Irwin

Implementing Caches in a 3D Technology for High Performance Processors 525
K. Puttaswamy and G. Loh

Architectural-Level Fault Tolerant Computation in Nanoelectronic Processors 533
W. Rao, A. Orailoglu, and R. Karri

8.3 Architecture for Verifiability (Invited)

Formal Verification and Its Impact on the Snooping versus Directory Protocol Debate 543
M. Martin

Deployment of Better Than Worst-Case Design: Solutions and Needs 550
T. Austin and V. Bertacco

9.1 Low Power Circuit Architecture (II)

Benefits and Costs of Power-Gating Technique 559
H. Jiang, M. Marek-Sadowska, and S. Nassif

A Dual-Vt Layout Approach for Statistical Leakage Variability Minimization in Nanometer CMOS 567
M. Ashouei, A. Chatterjee, A. Singh, and V. De

A Low-Overhead Virtual Rail Technique for SRAM Leakage Power Reduction 574
J. Kuang, H. Ngo, K. Nowka, J. Law, and R. Joshi

9.2 RF Wireless Technologies (Invited)

Tutorial on RF Technologies
D. Schmidt

AMD EX1021
AMD v. Realtek - Page 83
IEEE COMPUTER SOCIETY

9.3 Formal Verification Methods

State Set Management for SAT-Based Unbounded Model Checking 585
K. Chandrasekar and M. Hsiao

Reconsidering CEGAR: Learning Good Abstractions without Refinement 591
A. Gupta and E. Clarke

Formal Verification of Parametric Multiplicative Division Implementations 599
N. Kikkeri and P.-M. Seidel

Challenges in the Formal Verification of Complete State-of-the-Art Processors 603
N. Ayewah, N. Kikkeri, P.-M. Seidel, and S. Beyer

10.1 Power and Thermal Considerations in Processor Design (II)

RECAST: Boosting Tag Line Buffer Coverage in Low-Power High-Level Caches "for Free" 609
W.-H. Park, A. Moshovos, and B. Falsafi

Load-Store Queue Management: An Energy-Efficient Design Based on a State-Filtering Mechanism 617
F. Castro, D. Chaver, L. Pinuel, M. Prieto, F. Tirado, and M. Huang

Optimizing the Thermal Behavior of Subarrayed Data Caches 625
J. John, J. Hu, and S. Ziavras

VALVE: Variable Length Value Encoder for Off-Chip Data Buses 631
D. Suresh, B. Agrawal, W. Najjar, and J. Yang

Monitoring Temperature in FPGA Based SoCs 634
S. Velusamy, W. Huang, J. Lach, M. Stan, and K. Skadron

10.2 Instruction Issue, Scheduling and Prediction

Reducing the Energy of Speculative Instruction Schedulers 641
Y. Liu, G. Memik, and G. Reinman

A New Pointer-Based Instruction Queue Design and Its Power-Performance Evaluation 647
M. Ramírez, A. Cristal, A. Veidenbaum, L. Villa, and M. Valero

Power-Efficient Wakeup Tag Broadcast 654
J. Sharkey, K. Ghose, D. Ponomarev, and O. Ergin

SST: Symbiotic Subordinate Threading 662
R. Mameesh and M. Franklin

Memory Bank Predictors 666
S. Bieschewski, J.-M. Parcerisa, and A. González

Proceedings of the 2005 International Conference on Computer Design (ICCD'05)
0-7695-2451-6/05 $20.00 © 2005 IEEE

AMD EX1021
AMD v. Realtek - Page 84
IEEE COMPUTER SOCIETY

11.1 Circuit Consideration in Processor Design

H-SIMD Machine: Configurable Parallel Computing for Matrix Multiplication 671
X. Xu and S. Ziavras

Temperature-Sensitive Loop Parallelization for Chip Multiprocessors 677
S. Narayanan, G. Chen, M. Kandemir, and Y. Xie

Broadband Impedance Matching for Inductive Interconnect in VLSI Packages 683
B. LaMeres and S. Khatri

Temperature-Aware Voltage Islands Architecting in System-on-Chip Design 689
W.-L. Hung, G. Link, Y. Xie, N. Vijaykrishnan, N. Dhanwada, and J. Conner

11.2 Logic Optimization

Temporal Decomposition for Logic Optimization 697
N. Kitchen and A. Kuehlmann

Attacking Control Overhead to Improve Synthesized Asynchronous Circuit Performance 703
L. Plana, S. Taylor, and D. Edwards

An Improved Approach for Alternative Wires Identification 711
Y.-C. Chen and C.-Y. Wang

Author Index 717

AMD EX1021
AMD v. Realtek - Page 85
IEEE COMPUTER SOCIETY

This material may be protected by Copyright law (Title 17 U.S. Code)

Benefits and Costs of Power-Gating Technique

Hailin Jiang
ECE Department, UCSB
hailin@ece.ucsb.edu

Malgorzata Marek-Sadowska
ECE Department, UCSB
mms@ece.ucsb.edu

Sani R. Nassif
IBM Research Lab, Austin
nassif@us.ibm.com

Abstract

Power-gating is a technique for saving leakage power by shutting off the idle blocks. However, without good understanding and careful design, negative effects of power gating may overwhelm the potential gain and may make the technique not worth the effort. In this paper, we report on our study of the benefits and costs of the power-gating technique in terms of power, area, and performance. We model and analyze several strongly related parameters such as sleep-transistor size, decap area, and supply voltage level. We also report on our experiments to demonstrate how the gated area, circuit behavior and power mesh granularity affect the power gating technique at the system level. Experimental results show that, by compromising 4% of the total area and 5% of the dynamic power, we can achieve 47% leakage power saving while maintaining the same performance. With technology scaling down, the saving is significant. We conclude that we can benefit from the power-gating technique in future technology nodes.

1. Introduction

With the advent of portable electronic devices and high density VLSI circuits, power dissipation has emerged as a major design concern. Simultaneously, technological advances result in shrinking of the minimum feature size as well as in lowering of the supply and threshold voltages which cause a dramatic increase of the leakage current. Leakage power has now become a major component of the total power dissipation in CMOS circuits[6][9].

Power-gating is a technique for reducing leakage power by shutting off the idle blocks. Implementation of power-gating requires a multi-threshold CMOS process. Logic blocks are implemented using low-V_t, high-performance transistors whereas high-V_t transistors (called sleep transistors) connect the gated blocks to the power supply [1]. Power-gating is not a cost-free technique. Negative effects include a combination of noise, performance penalty, area and power overhead, etc. In this paper, we study and quantify the benefits and costs of the power-gating technique in terms of area and power. We also consider the impact of scaling trends on the applicability of power gating. In [2], the authors evaluate limitations and power-savings of three leakage-power reduction techniques and address the outlook for scaling technology. However, although they mention sleep transistors, the focus of the paper is on using phase-locked loops (PLLs) as voltage regulators to gate power supply. The phenomena occurring in circuits power-gated with sleep transistors are not addressed in that work. Moreover, the studies are performed on small test circuits (such as 32-bit 2-input NOR gate) which may not capture all the phenomena of a system-level power-gating technique. To the best of our knowledge, our work is the first one addressing the system-level trade-off in sleep-transistor-based power-gating technique.

The remainder of this paper is organized as follows. In section 2, we briefly introduce the costs and benefits of a sleep-transistor-based power-gating technique. In section 3, we characterize and model each effect in detail, explaining the simulation flow used to evaluate the trade-off. In section 4 we show the experimental results and scaling trend. Section 5 concludes the work.

2. Comparison two power supply systems

Here we consider a standard chip (Fig1(a)) and a power-gated chip (Fig1(b)) both implementing the same functionality. In the standard chip, all logic circuits are connected to Vdd through a hierarchical power mesh. The entire chip is fully powered at all times. In the power-gated chip, we have local power meshes for all macros, and sleep transistors are used to connect the local mesh to the global mesh.

Proceedings of the 2005 International Conference on Computer Design (ICCD'05)
0-7695-2451-6/05 $20.00 © 2005 IEEE

AMD EX1021
AMD v. Realtek - Page 86
IEEE COMPUTER SOCIETY

When a macro is active, the sleep transistor is turned on. Its size must be large enough to guarantee that the current drawn by the macro does not cause excessive voltage drop. If we want to maintain the same performance with and without power-gating, in the gated chip the V_{dd} has to be raised by $\div V$ to counteract the voltage drop across the sleep transistor. However, increasing the supply voltage increases the dynamic and leakage power consumption, which may nullify the intended power savings.

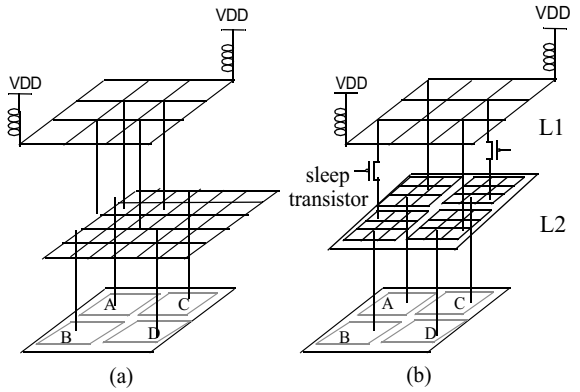


Figure 1. Power supply system (a) normal power supply system (b) power-gating system

Also, when sleep transistors are turned on and off, considerable power supply currents are drawn in a short period of time, which may result in large voltage fluctuations on the power grid. This *power-gating noise (PGN)* affects the reliability of systems-on-chips (SoCs), especially for advanced CMOS technologies with narrow noise margins. We need to add extra decoupling capacitance (decap) to reduce the *PGN* and take into account the additional leakage currents associated with the intentionally introduced capacitors. At the same time, the switching sleep transistors consume more dynamic power.

In a chip without power-gating, the non-switching part of the circuit serves as a decoupling capacitor and reduces the power grid noise. However, in the power-gated chip, the gated macros are disconnected from the power supply during their idle state, which prevents them from acting as a decap for the active circuit. Thus the non-gated macros adjacent to the gated circuitry may need extra decap to guarantee that power grid noise remains within tolerable margins. The gated macros not only stop providing decap to other macros, but also act as an obstacle for decap insertion. Extra decap will enlarge the chip size and again consume more leakage power.

We will now consider the chip shown in Fig.1. Region I contains the gated macros B and C, whereas region II consists of ungated macros A and D. We qualitatively compare the leakage, dynamic power, decap and sleep transistor area of those two regions. We normalize the data to that of an ungated chip which realizes the same functionality as the gated chip. The trade-off in terms of power and area for power-gating systems can be summarized in Table.1.

Table 1. Power-gating vs. non-power-gating

	non-power-gating chip region		power-gated chip region	
	I	**II**	**I**	**II**
P(leakage)	1	1	↓	↑
P(dyn)	1	1	↑	↑
Area(decap)	1	1	1	↑
Area(st)	N/A	N/A	↑	N/A

We notice that the benefit comes only from saving in the leakage power of gated circuits, and the costs include: 1) area consumed by the extra decap and sleep transistors; 2) dynamic power of both regions and leakage consumption of non-gated circuit and decaps. In our study, we will attempt to quantify these benefits and costs.

3. Characterization of power gating technique

3.1. Power-gating modeling

The power-gating model is shown as Fig.2. The upper power mesh can be modeled as a linear RL network excited by constant voltage sources. The lower power mesh is composed of a linear RC network excited by time-varying current sources which represent the switching currents drawn by the logic circuits. We use a simple triangle waveform to model the current profiles. C is the on-chip decou-

pling capacitor which is provided by the non-switching part of the logic circuit.

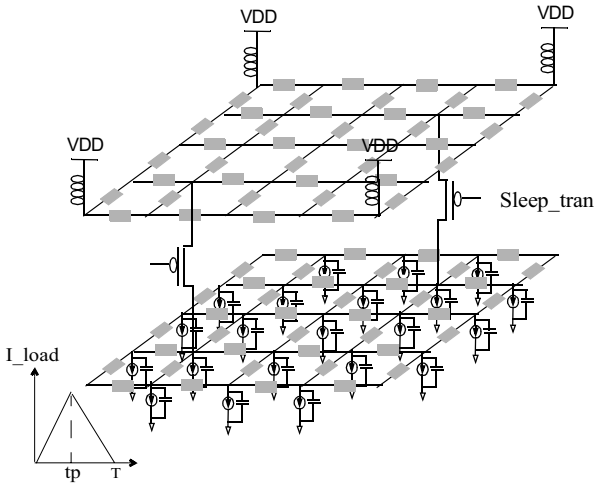


Figure 2. Power gating modeling

In the traditional power network analysis for the ungated chip, sleep transistors are replaced by vias (resistors). So the entire system is a linear RLC network excited by the voltage and current sources. The modified Nodal Analysis (MNA) formulation can be used to solve this system. However, when sleep transistors are introduced, the power network is no longer linear. We use HSPICE to simulate the power-gating noise at the moment the sleep transistors are turned on and off; and we use ALSIM, the IBM linear power network analyzer, to simulate the voltage delivery behavior when sleep transistors are on and can be modeled as resistances.

3.2. Sleep-transistor sizing

In our model, we assume distributed sleep transistors, one per gated block. When sleep transistors are absent, the delay of a single gate can be approximated by [3]

$$T_d = \frac{C_L V_{dd}}{/V_{dd} - V_{tL}0^{\zeta}} \qquad \text{(EQ 1)}$$

where C_L is the load capacitance at the gate's output, V_{tL} is the threshold voltage in the low V_t block, and ζ is the velocity saturation index for modeling short channel effects [4]. In the presence of a sleep transistor, the gate propagation delay increases to

$$T_d^{ST} = \frac{C_L/V_{dd} - V_{ST}0}{/V_{dd} - V_{ST} - V_{tL}0^{\zeta}} \qquad \text{(EQ 2)}$$

where V_{ST} is the voltage drop on the sleep transistor. To eliminate the performance loss caused by the sleep transistor, V_{dd} has to be increased to V_{dd}^{ST} such that

$$\frac{C_L V_{dd}}{/V_{dd} - V_{tL}0^{\zeta}} = \frac{C_L/V_{dd}^{ST} - V_{ST}0}{/V_{dd}^{ST} - V_{ST} - V_{tL}0^{\zeta}} \quad . \qquad \text{(EQ 3)}$$

We assume $\zeta = 1$ and define *supply increase ratio* as

$$\xi = \left(\frac{V_{dd}^{ST}}{V_{dd}} - 1\right) \qquad \text{(EQ 4)}$$

and we get

$$V_{ST} = \xi V_{dd}. \qquad \text{(EQ 5)}$$

The sleep transistor operates in its linear region and the current can be expressed as

$$I_{ST} = \sigma_p C_{ox} \left(\frac{W}{L}\right)_{ST} \left[/V_{dd}^{ST} - V_{tH}0 V_{ST} - \frac{V_{ST}^2}{2}\right] . \qquad \text{(EQ 6)}$$

Substituting for V_{ST}, the size of sleep transistors can be expressed as

$$\left(\frac{W}{L}\right)_{ST} = \frac{I_{ST}}{\sigma_p C_{ox} \xi V_{dd}/V_{dd}^{ST} - V_{tH} - 0.5\xi V_{dd}(} \qquad \text{(EQ 7)}$$

where V_{tH} is the threshold voltage of the sleep transistor. The total sleep transistors' size of one gated block can be approximated by

$$\frac{I_{MAX}}{\sigma_p C_{ox} \xi V_{dd}/V_{dd}^{ST} - V_{tH} - 0.5\xi V_{dd}0} \qquad \text{(EQ 8)}$$

where I_{MAX} is the *maximum switching current* generated by the gated circuit.

We notice that the sleep transistor size is related to the increased V_{dd}. Thus the higher the supply voltage, the smaller the required sleep transistor; but also the more power consumed. Performance can be traded also. If we allow some performance loss (PL), supply voltage may not necessarily increase. These parameters should be decided according to design requirements.

3.3. Power saving vs. cost

The purpose of power-gating is to save leakage power when blocks are idle. However, power-gating itself incurs power cost. If that cost is comparable or even larger than the savings, then the power-gating technique is not worth the effort. The work reported in [5] estimates the minimum idle time when considering the overhead associated with the leakage reduction technique. However, if the supply voltage is increased to counteract the performance loss of power-gating, as analyzed in section 3.2, the minimum idle time is no longer sufficient to characterize the trade-off between the cost and benefit.

AMD EX1021
AMD v. Realtek - Page 88
IEEE COMPUTER SOCIETY

Fig.3(a) depicts the circuit's power gating schedule. t_{sleep} is the sleep time, t_{active} is the active time, t_r and t_f are the transition times. We have two power supply schemes: (a) power-gating and (b) no-power-gating. Circuits are divided into two regions (I) consisting of gated circuits and (II) of non-gated circuits. Fig.3 (b)-(e) shows the power comparisons in particular regions. The dark line illustrates the power consumed in the power-gated chip, and the light line indicates power consumed in the ungated chip. From the comparisons, we get the leakage power saving $\div P_1$ in region I; the leakage power overhead $\div P_2$, and dynamic power overhead $\div P_3$ in region II

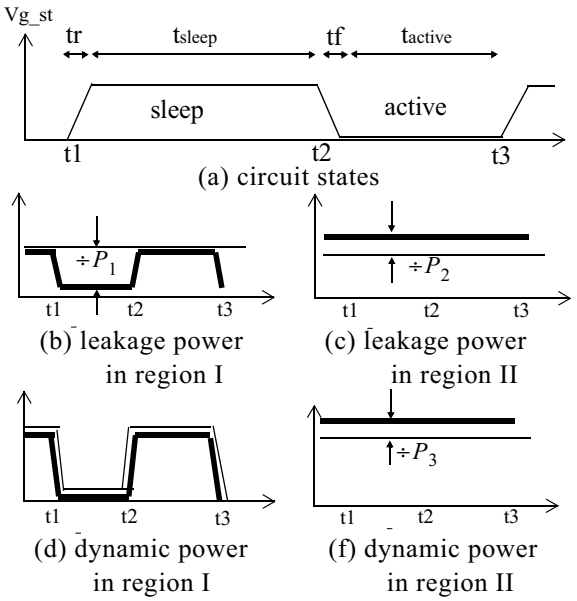


Figure 3. Power saving and cost

We define E_{tr} and E_{tf} to be the energies dissipated by sleep transistor during the time periods t_r and t_f. To make the power-gating scheme worthwhile, the power balance must satisfy the following inequality:

$$\div P_1 \{t_{sleep}\} / \div P_2 + \div P_3 0 / t_{sleep} + t_{active} 0 + E_{tr} + E_{tf} \quad \text{(EQ 9)}$$

From Eq.9, we note that not only should the sleep time be long enough, but also the active time cannot be longer than a certain period. We define an active ratio:

$$\zeta = t_{active} \aleph_{sleep}$$

The designer can select the value of ζ and observe power saving as a function of t_{sleep}. The waveform will reach a maximum saving value after a certain value of t_{sleep}. We can also fix t_{active} to explore the effect of ζ.

3.4. Power estimation

3.4.1. Dynamic power, Dynamic power is consumed by the switching of the circuit and of the sleep transistor. The dynamic power consumed by the circuit as

$$P_{dynamic}^{ckt} = \sum_{k} C_{gk} \{ f^2 V_{dd} \{ S \quad \text{(EQ 10)}$$

where C_{gk} is the capacitance of the *kth* gate, which is also the load capacitance of its parent gate. S is an empirically determined switching factor characterizing the circuit's switching activity. f is the operating frequency and V_{dd} is the supply voltage. In this paper, we focus only on relative comparisons rather than precise calculations; our estimations are rough but sufficient to observe the trends. For more accuracy, we can perform logic simulation, obtain switching probabilities of each gate and use individual weights S_k on each C_{gk}.

The dynamic power consumed by the sleep transistor is obtained from HSPICE on a simple model shown in the Fig.4. C_{DS} is the total drain-source capacitance of the non-switching part of the gated circuit. A step signal V_g is applied to trigger the sleep transistor. HSPICE reports the average power dissipation P_{avr} during the time T. To get $E_{st} = E_{tr} + E_{tf}$ (Section3.3), we have

$$E_{st} = P_{avr} \{ T. \quad \text{(EQ 11)}$$

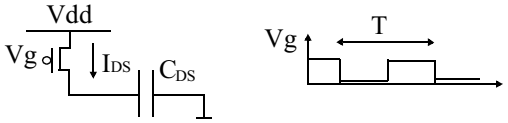


Figure 4. The model for dynamic power

3.4.2. Leakage power, There are two major leakage mechanisms in scaled devices: subthreshold leakage I_{sub} and gate leakage I_g. [10]. Both of these leakage components are increasing very rapidly with technology scaling. Furthermore, to get sufficiently large capacitance, decaps are usually made from thin gate-oxide MOS transistors with long and wide channels. These decaps will leak more as technology continues scaling down.

Circuit leakage is caused by two mechanisms: gate- leakage and decap-leakage. Gate-leakage characterizes the leakage of logic gates and is input-pat-

AMD EX1021
AMD v. Realtek - Page 89
IEEE COMPUTER SOCIETY

tern-dependent. Decap leakage is pattern-independent. We use HSPICE to simulate the average leakage for a variety of standard cells used in circuits. Probability of pattern occurrence should be weighted in simulation. To compute the decap leakage, we run simulations and determine the unit leakage per σm^2. The total leakage of a circuit is estimated as

$$I_{leak} = /1 - S0 \sum_{i \subset allgates} /I_i^{gate}0 + I_{unit}^{decap} \lceil WL \quad \text{(EQ 12)}$$

where WL is total decap area, S is the empirical switching factor. Leakage power is expressed as

$$P_{leak} = V_{dd} \lceil I_{leak} . \quad \text{(EQ 13)}$$

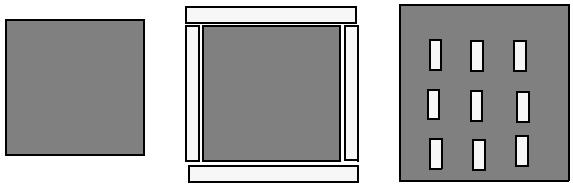
When supply voltage increases, I_{leak} will increase exponentially

$$I_{sub} = I_0 \exp\left(\frac{V_{gs} - V_T}{nT_t}\right) - \exp\left(\frac{-V_{ds}}{V_t}\right) \quad \text{(EQ 14)}$$

where $I_0 = \sigma_0 C_{ox}\left(\frac{W}{L}\right) V_t e^{1.8}$, V_t is the thermal voltage, and n is the subthreshold slope coefficient.

3.5. Decap insertion

Power grid noise is caused by simultaneous switching of the core logic and I/O buffers. Sleep transistors introduce power-gating noise when they are switching on and off. By adding decoupling capacitors, we can dramatically reduce both power gating noise and simultaneous switching noise. Decaps come from on-chip non-switching capacitors C_{ckt} or thin-oxide capacitors C_{ox} which are purposely inserted. The on-chip decap is extracted from each logic block and is known before floorplanning. If C_{ckt} is not sufficient for noise immunity, more C_{ox} s are added. We model the C_{ox} insertion as illustrated in Fig.5. Decap can be added peripherally around a block (Fig.5. b) or can be evenly distributed within the block(Fig.5. c).



(a) logic block (b) peripheral (c) center

Figure 5. Decap insertion

We apply a greedy algorithm to implement decap insertion:

1 Given a set of blocks with their areas, minimum and maximum height/width ratios, and the switching current profiles modeled as piece-wise-linear functions, we apply floorplanning.

2 After floorplanning, we know each block's location and the topology of power grid. We simulate the whole chip and obtain the noise distribution. We determine a grid node P on which the worst-case noise occurs.

3a (*Peripheral insertion*) The boundary decap tile is considered as a pure capacitance block. For a node P, we calculate the noise sensitivity to decap placed on every side of each block: $\frac{\in}{\in C_{ij}} V_{noise}/p0$, $i = 13* N$ $j = 1323334$. N is the total number of blocks in the chip. j represents four sides of a block. C_{ij} is a decap added to the *ith* block, on the *jth* side. We insert decap to a block and size which results in maximum elimination of noise.

3b (*Central insertion*) We calculate the noise sensitivity to decap of each block for node P: $\frac{\in}{\in C_i} V_{noise}/p0$. We select the one resulting in the greatest noise reduction and insert decap into the corresponding block.

4 We simulate the chip with added decap to update the noise distribution. If the worst case noise is already within the noise margin, we go to step 5; otherwise, back to step 3.

5 We update the area of each block with inserted decaps and apply a refinement floorplannning (with hard blocks) to adjust the blocks' location.

3.6. Simulation flow

Our complete simulation flow is shown in Fig.6. We begin with a set of blocks and perform the initial floorplanning. Next we follow two branches. One is for the regular power supply chip and the other is for the power-gated chip. In the former one, we do the power grid noise analysis and decap insertion to keep the noise within the margin. In the latter one, we first size the sleep transistors and increase Vdd to ensure the same performance. Power grid noise analysis combined with decap insertion are per-

AMD EX1021
AMD v. Realtek - Page 90
IEEE COMPUTER SOCIETY

formed to meet the noise margin. Finally, we compare the saving and overhead of those two designs.

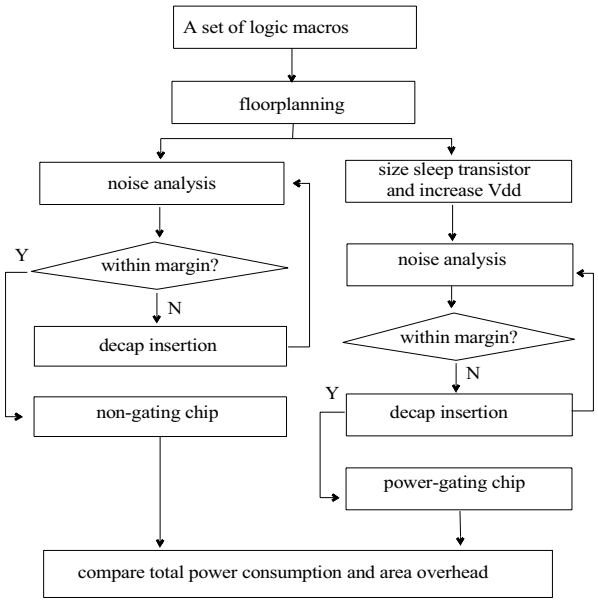


Figure 6. Evaluating power-gating technique

4. Experiments

We implement 26 circuits (from MCNC and ISCAS benchmarks respectively) as the basic logic blocks. The initial floorplan of those blocks is shown as in Fig.7.

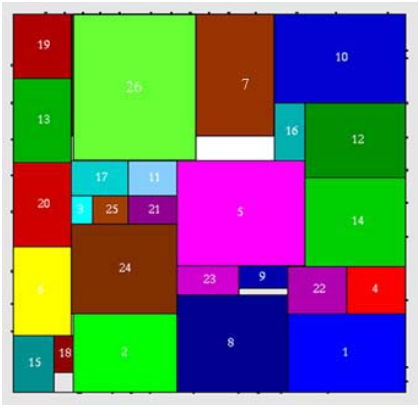


Figure 7. Floorplan of 26 circuits(1x0.9mm^2)

For each block, we collected following data from standard cell library and simulation:

C_l: loading capacitance, for dynamic power estimation;

$I_{profile}$: current profile, for noise analysis;

I_{leak} : leakage current, for leakage power estimation;

C_{decap} : decoupling capacitance, for noise analysis and power estimation.

We used Tcl programming language to develop our simulation flow, which includes HSPICE and ALSIM. We ran all the experiments on a P4 2.4GHz PC with Linux. The test circuits were first implemented in 0.13σm technology. The temperature was 25∀C.

1. Power-gating vs. no-power-gating

In this experiment, we gated half of the circuits (blocks whose geometric centers were on the left half of the chip) and compared it with non-power-gated chip in terms of power and area. Table.2 shows the parameters of the initial chip. The noise is beyond the acceptable margin (we assume 10% of Vdd), so decap insertion is necessary. We implement both center decap insertion and peripheral decap insertion.

Table 2. Initial chip

Vdd(V)	Vnoise(V)	Cload(pF)	P_dyn(mW)	P_leak(mW)
1.5	0.25	398	143	13.7

Table 3. Comparison between w/ and w/o power-gating

		no-gating	power-gating	b/c(%)
Center Decap Insertion	Vdd(V)	1.5	1.54	
	ST(%)	0	4	-4
	Decap(pF)	481	529	
	(%)	2.4	2.66	-0.2
	Pdyn(mW)	143	150	-4.98
	Pleak(mW)	13.9	7.75	44.24
Peri-pheral Decap Insertion	Vdd	1.5	1.54	
	ST(%)	0	4	-4
	Decap(pF)	567	850	
	(%)	2.85	4.21	-1.36
	Pdyn(mV)	143	150	-4.98
	Pleak(mV)	14.0	8.89	+36.5

The comparison results are reported in Table 3. Vdd is increased to 1.54V to meet the same target frequency. The relative area overheads introduced by the sleep transistors and decaps are listed in rows 3, 5, 9 and 11. The last column indicates the benefit (positive number) and cost (negative number) of the power-gating technique. For example, for the center decap insertion strategy, by compromising 4.2% area and 4.98% dynamic power, we can achieve 44.24% saving in leakage power. Experimental

AMD EX1021
AMD v. Realtek - Page 91
IEEE COMPUTER SOCIETY

results show that, in general, the center decap insertion is better than the peripheral one.

We note that the energy consumed by switching of sleep transistors (which is around 7.5nJ) is not counted in the dynamic power calculation reported in Table 3. Generally speaking, we need to use Eq.9 to decide when savings are possible. However, in this case the absolute cost of dynamic power (7mW) exceeds the absolute saving of leakage power(6.15mW), so the total power cannot be saved. In a later experiment, however, we will see that with technology scaling down, power-gating to reduce leakage does save the total power.

2. Gating-effects vs. gated-area

We did a study on the impact of gated area on gating effects. First, we built a chip whose current distribution was uniform. Then we varied the ratio of gated to non-gated area from 20% to 100%, as shown in Fig.8. Table 4 summarizes the results. All the data have been normalized to the ungated system. Leakage power decreases with increase in gated-to-ungated ratio. The interesting thing is that the area overhead and the dynamic power overhead do not keep increasing. The reason is as follows: First, as the gated area increases, the sleep transistor size is increasing. More efforts, such as increasing Vdd and inserting decap, are required to counteract its impact on the active circuits. However, at the same time that the area of the active circuits is decreasing, their impact begins to diminish. This means that after reaching a certain gating ratio, we begin saving at an increasing rate.

Figure 8. Fated circuits in grey area

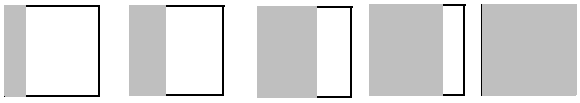


Table 4. Gated-area vs. gating-effects

gated area		20%	40%	60%	80%	100%
Area	NG	1	1	1	1	1
	G	1.03	1.05	1.16	1.16	1.15
P dynamic	NG	1	1	1	1	1
	G	1.02	1.04	1.06	1.04	1.02
P leakage	NG	1	1	1	1	1
	G	0.73	0.66	0.53	0.29	0.08

3. Gating-effect vs. gated-circuits

In this experiment, we studied the effect of circuit behavior on the power-gating result. We re-floorplanned the 26 logic blocks in such a way that big-current drawing blocks were placed in region B, and small current-drawing blocks in region S, as shown in Fig.9. Then we gated one region and kept the other active. The comparisons are shown in Table.5. In general, gating big current-drawing blocks saves more leakage power but at a higher overhead cost of area and dynamic power.

Figure 9. Circuits have different behavior in different regions

S	**B**
B	**S**

Table 5. Gated circuits with different behavior

	ST(%)	Decap	P_dynamic	P_leakage
NG	N/A	1	1	1
gate_B	7	1.14	1.06	0.42
gate_S	3	1.06	1.04	0.73

4. Gating-effect vs. power-mesh-granularity

In this experiment, we studied the impact of the power mesh granularity on power-gating result. We kept the area of power mesh constant and changed the width of horizontal and vertical segments. Fig.10 shows power meshes of various granularity. We used meshes of several granularities on the same gated system. Fig 11 shows the decap insertion results for such meshes. *MxN* stands for a mesh of m rows and n columns. The y-axis data is normalized to the ungated system. The stable curve implies that if we keep the power mesh area constant, the noise incurred by power-gating does not change much with mesh granularity.

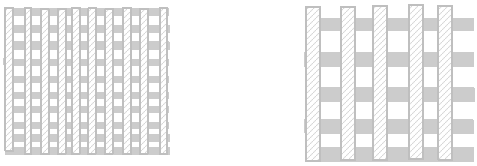


Figure 10. Power mesh granularity

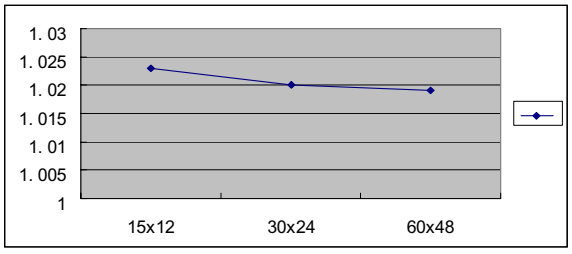


Figure 11. inserted decap

AMD EX1021
AMD v. Realtek - Page 92
IEEE COMPUTER SOCIETY

5. Technology trends

Fig 12 shows how technology affects power-gating. We observe that dynamic power decreases and leakage power increases for technology moving 130nm to 70nm. The difference in leakage power between power-gated and ungated systems is becoming larger than the difference in dynamic power, which implies a promising future for the power-gating technique. At the same time, we note that the power density is increasing for both power-gated and ungated systems, as shown in Fig 13, but the growth is slower for the power-gated chips than for the ungated, which suggests that in the future the low-power designs will favor the power-gating techniques.

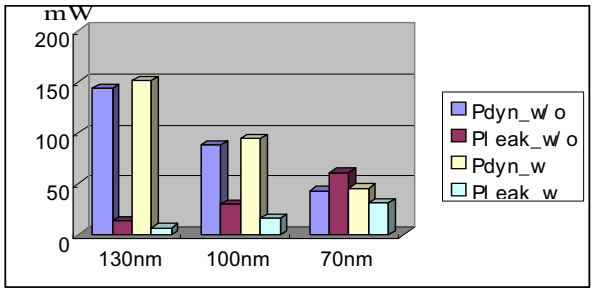


Figure 12. Technology trend

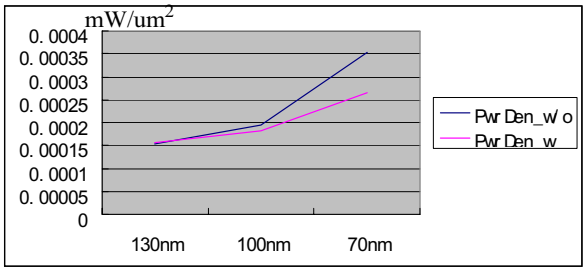


Figure 13. Power density

5. Conclusions

In this paper, we have discussed the findings of our studies on the benefits and costs incurred by the power-gating technique. We demonstrated that there are several components strongly related to power-gating, such as sleep transistor size, decap area, and supply voltage V_{dd} level. We modeled these components and analyzed the effects they caused. We showed experimentally how the gated area, circuit behavior and power mesh granularity affect the power budget of the gating technique at the system level. Our experimental results show that, by compromising the 4% of total area and 5% of the dynamic power, we can reduce leakage power by 47% while keeping the same performance. With technology scaling down, the absolute value of power saving will out weigh the absolute value of power cost. Therefore, we conclude that power-gating is a promising low-power technique for the next generation technology.

6. Acknowledgement

This work was supported in part by SRC grant # 1069 and in part by MICRO through IBM. We gratefully acknowledge equipment grant from Intel.

7. Reference

[1] S.Mutoh and et al, "A 1V power supply high-speed digital circuit technology with multi threshold voltage CMOS", *IEEE Journal of Solid-State Circuit,* pp. 847-854, 1995

[2] Y.Tsai, D.E.Duarte and et al, "Characterization and modeling of run-time techniques for leakage power reduction", *IEEE Trans on VLSI*, pp. 1221-1233, 2004

[3] M.Anish, S.Areibi and et al, "Dynamic and leakage power reduction in MTCMOS circuits using an automated efficient gate clustering technique", *Proc. of IEEE Design Automation Conference,* pp.480-485, 2002

[4] T.Sakurai and A.Newton, "Alpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas" *IEEE Journal of Solid-State Circuits,* vol25, pp. 584-594, 1990

[5] D.Duarte, Y.Tsai and et al, "Evaluating run-time techniques for leakage power reduction", *Proc. of the 15th International Conference on VLSI Design,* 2002

[6] R.M.Rao, J.L.Burns, and et. al, "Efficient Techniques for Gate Leakage Estimation", *ISPED,* pp. 100-103, 2003

[7] International Roadmap for Semiconductors, 2003 edition. *http://public.itrs.net*

[8] S.Mukhopadhyay and et. al. "Accurate estimation of total leakage current in scaled CMOS logic circuits based on compact current modeling", *DAC,* pp.169-174, 2003

[9] V. De and S. Borkar, "Technology and design challenges for low power and high performance," *ISLPED,* pp. 163-168, 1999

[10] S-C. Lin, A. Basu, and et al, "Impact of Off-state Leakage Current on Electromigration Design Rules for Nanometer Scale CMOS Technologies", *IEEE Annual International Reliability Physics Symposium,* pp. 74-78, 2004

ATTACHMENT 1A

001 ocm62240543
003 OCoLC
005 20051118111700.0
008 051108t20052005caua b 101 0 eng d
020 |a0769524516
022 |a1063-6404
035 |a(OCoLC)62240543
040 |aIXA|beng|cIXA|dOrLoB-B
049 |xrel
090 |aTK7888.4|b.I23 2005 e-book
1112 |aIEEE International Conference on Computer Design|n(23rd : |d2005 :|cSan Jose, Calif.)
24510|a2005 International Conference on Computer Design :|bproceedings : [VLSI in computers & processors] : 02-05 October, 2005, San Jose, CA /|csponsored by IEEE Computer Society Design Automation Technical Committee (DATC) ...[and others]
24614|aICCD 2005
24630|aInternational Conference on Computer Design
24630|aComputer Design
24630|aVLSI in computers & processors
264 1|aLos Alamitos, Calif. :|bIEEE Computer Society,|c[2005]
264 4|c©2005
300 |axix, 720 pages :|billustrations ;|c28 cm
336 |atext|btxt|2rdacontent
337 |aunmediated|bn|2rdamedia
338 |avolume|bnc|2rdacarrier
500 |a"IEEE Computer Society Order Number P2451"--T.p. verso.
504 |aIncludes bibliographical references and author index.
50500|tLatency lags bandwidth /|rD. Patterson -- |tTemperature-dependent optimization of cache leakage power dissipation /|rP. Li, Y. Deng and L. Pileggi -- |tArchitectural considerations for energy efficiency /|rH. Dao, B. Zeydel and V. Oklobdzija -- |tReducing the latency and area cost of core swapping through shared helper engines /|rA. Shayesteh, E. Kursun, T. Sherwood, S. Sair and G. Reinman -- |tAnalytical model for sensor placement on microprocessors /|rK.-J. Lee, K. Skadron and W. Huang -- |tPre-layout physical connectivity prediction with application in clustering-based placement /|rQ. Liu and M. Marek-Sadowska --
50580|tEfficient rectilinear Steiner tree construction with rectilinear blockages /|rZ. Shen, C. Chu and Y.-M. Li -- |tX-routing using two Manhattan route instances /|rS. Ahmad, N. Jayakumar, V. Balasubramanian, E. Hursey, S. Khatri and R. Mahapatra -- |tHardware support for bulk data movement in se

rver platforms /|rL. Zhao, R. Iyer, S. Makineni, L. Bhuyan and D. Newell -- |tCounter-based cache replacement algorithms /|rM. Kharbutli and Y. Solihin -- |tUtilizing horizontal and vertical parallelism with a no-instruction-set compiler for custom datapaths /|rM. Reshadi, B. Gorjiara and D. Gajski --

505 80 |tAre today's verification tools able to handle current design challenges? /|rR. Goering, R. Faris, K. Larsen, H. Foster and S. Swwan -- |tEnergy-efficient color approximation for digital LCD interfaces /|rA. Nourrachmat, S. Salerno, E. Macii and M. Poncino -- |tApplication-specific power-aware workload allocation for voltage scalable MPSoC platforms /|rM. Ruggiero, A. Acquaviva, D. Bertozzi and L. Benini -- |tLCD display energy reduction by user monitoring /|rV. Moshnyaga and E. Morikawa -- |tFrame buffer energy optimization by pixel prediction /|rK. Patel, E. Macii and M. Poncino --

505 80 |tEnergy and performance analysis of mapping parallel multi-threaded tasks for an on-chip multi-processor system /|rB.-C. Lai, P. Schaumont, W. Qin and I. Verbauwhede -- |tNear-memory caching for improved energy consumption /|rN. AbouGhazaleh, B. Childers, D. Mosse and R. Melhem -- |tPhysical synthesis of energy-efficient networks-on-chip through topology exploration and wire style optimization /|rY. Hu, H. Chen, Y. Zhu, A. Chien and C.-K. Cheng -- |tA formal framework for modeling and analysis of system-level dynamic power management /|rS. Yardi, K. Channakeshava, M. Hsiao, T. Martin and D. Ha --

505 80 |tEfficient implementation selection via time budgeting : complexity analysis and leakage optimization case study /|rS. Ghiasi -- |tEfficient thermal simulation for run-time temperature tracking and management /|rH. Li, P. Liu, Z. Qi, L. Jin, W. Wu, S. Tan and J. Yang -- |tA flexible design methodology for analog test wrappers in mixed-signal SoCs /|rA. Sehgal, S. Ozev and K. Chakrabarty -- |tConcurrent core test for test cost reduction using merged test set and scan tree /|rG. Zeng and H. Ito -- |tChiYun compact : a novel test compaction technique for responses with unknown values /|rM. Chao, S. Wang, S. Chakradhar and K.-T. Cheng -- |tAccurate diagnosis of multiple faults /|rY.-C. Lin, F. Lu and K.-T. Cheng --

505 80 |tQuick scan chain diagnosis using signal profiling /|rJ.-S. Yang and S.-Y. Huang -- |tFast hierarchical process variability analysis and parametric test development for analog/RF circuits /|rF. Liu and S. Ozev -- |tFault tolerant asynchronous adder through dynamic self-reconfiguration /|rS. Peng and R. Manohar -- |tError-tolerance memory microarchitecture via dynamic multithreading redundancy /|rL. Wang -- |t

A soft error monitor using switching current detection /|rP. Ndai, A. Agarwal, Q. Chen and K. Roy -- |tApplying resource sharing algorithms to ADL-driven automatic ASIP implementation /|rE. Witte, A. Chattopadhyay, O. Schliebusch, D. Kammler, R. Leupers, G. Ascheid and H. Meyr --

505 80 |tStatistical analysis driven synthesis of asynchronous systems /|rK. Ohashi and M. Kaneko -- |tNovel low-overhead operand isolation techniques for low-power datapath synthesis /|rN. Banerjee, A. Raychowdhury, S. Bhunia, H. Mahmoodi and K. Roy -- |tExploiting vanishing polynomials for equivalence verification of fixed-size arithmetic datapaths /|rN. Shekhar, P. Kalla, F. Enescu and S. Gopalakrishnan -- |tIncorporating efficient assertion checkers into hardware emulation /|rM. Boule and Z. Zilic -- |tAssertion checking of behavioral descriptions with non-linear solver /|rI. Ugarte and P. Sanchez -- |tFile system interfaces for embedded software development /|rB. Pisupati and G. Brown --

505 80 |tYesterday and tomorrow : a view on progress in computer design /|rM. Flynn -- |tRipple-precharge TCAM : a low-power solution for network search engines /|rD. Vijayasarathi, M. Nourani, M. Akhbarizadeh and P. Balsara -- |tLow- and ultra low-power arithmetic units : design and comparison /|rM. Vratonjic, B. Zeydel and V. Oklobdzija -- |tA skewed repeater bus architecture for on-chip energy reduction in microprocessors /|rM. Khellah, M. Ghoneima, J. Tschanz, Y. Ye, N. Kurd, J. Barkatullah, S. Nimmagadda, Y. Ismail and V. De -- |tLow-power design of 90-nm SuperH processor core /|rT. Yamada, M. Abe, Y. Nitta, K. Ogura, M. Kusaoke, M. Ishikawa, M. Ozawa, K. Takada, F. Arakawa, O. Nishii and T. Hattori --

505 80 |tAsynchronous IC interconnect network design and implementation using a standard ASIC flow /|rB. Quinton, M. Greenstreet and S. Wilton -- |tAlgorithmic and architectural design methodology for particle filters in hardware /|rA. Sankaranarayanan, R. Chellappa and A. Srivastava -- |tALLCN : an automatic logic-to-layout tool for carbon nanotube based nanotechnology /|rW. Zhang and N. Jha -- |tAutomatic synthesis of composable sequential quantum boolean circuits /|rL.-K. Chang and F.-C. Cheng -- |tModel checking C programs using F-soft /|rF. Ivancic, I. Shlyakhter, A. Gupta, M. Ganai, V. Kahlon, C. Wang and Z. Yang --

505 80 |tDealing with I/O devices in the context of pervasive system verification /|rM. Hillebrand, T. In der Rieden and W. Paul -- |tTowards the formal verification of lower system layers in automotive systems /|rS. Beyer, P. Bohm, M. Gerke, M. Hillebrand, T. In der Rieden, S. Knapp, D. Leinenbach and W. Paul -- |tRestrictive compression techniques to increase level 1 cache capacity /|rP. Pujara and A. Aggarwal -- |

tThe TM3270 media-processor data cache /**|r**J.-W. van de Waer dt, S. Vassiliadis, J.-P. van Itegem and H. van Antwerpen -- **|t**Mitigating soft errors in highly associative cache with CAM-based tag /**|r**L. Hung, M. Goshima and S. Sakai --

50580**|t**VGTA : variation - aware gate timing analysis /**|r**S. Abbas pour, H. Fatemi and M. Pedram -- **|t**Exact lower bound for th e number of switches in series to implement a combinational logic cell /**|r**F. Schneider, R. Ribas, S. Sapatnekar and A. Reis -- **|t**A waveform independent gate model for accurate ti ming analysis /**|r**P. Li and E. Acar -- **|t**Enhanced dual-trans ition probabilistic power estimation with selective superga te analysis /**|r**F. Hu and V. Agrawal -- **|t**Methods for modeli ng resource contention on simultaneous multithreading proce ssors /**|r**T. Moseley, J. Kihm, D. Connors and D. Grunwald -- **|t**Using scratchpad to exploit object locality in Java /**|r** C. Lebsack and J. Chang --

50580**|t**Correlation between detailed and simplified simulations i n studying multiprocessor architecture /**|r**K. Ibrahim -- **|t**S imulating commercial Java throughput workload : a case stud y /**|r**Y. Luo and L. John -- **|t**Minimum energy near-threshold network of PLA based design /**|r**N. Jayakumar and S. Khatri -- **|t**Robust design of high fan-in/out subthreshold circuits /**|r**J. Chen, L. Clark and Y. Cao -- **|t**A thermally-aware meth odology for design-specific optimization of supply and thre shold voltages in nanometer scale ICs /**|r**S.-C. Lin, N. Sriv astava and K. Banerjee -- **|t**A feasibility study of subthres hold SRAM across technology generations /**|r**A. Raychowdhury, S. Mukhopadhyay and K. Roy --

50580**|t**Variability-driven buffer insertion considering correlati ons /**|r**A. Davoodi and A. Srivastava -- **|t**A dual dielectric approach for performance aware gate tunneling reduction in combinational circuits /**|r**V. Mukherjee, S. Mohanty and E. K ougianos -- **|t**Supply voltage degradation aware analytical p lacement /**|r**A. Kahng, B. Liu and Q. Wang -- **|t**Layout-aware RF circuit synthesis driven by worst case parasitic corners /**|r**A. Agarwal and R. Vemuri -- **|t**Extended forward implicati ons and dual recurrence relations to identify sequentially untestable faults /**|r**M. Syal, R. Arora and M. Hsiao -- **|t**Ca se study of ATPG-based bounded model checking : verifying U SB 2.0 IP core /**|r**Q. Qiang, C.-L. Chang, D. Saab and J. Abr aham --

50580**|t**Towards finding path delay fault tests with high test eff iciency using ZBDDs /**|r**M. Michael, K. Christou and S. Trago udas -- **|t**Quality transition fault tests suitable for small delay defects /**|r**M. Kumar and S. Tragoudas -- **|t**A novel met hod of improving transition delay fault coverage using mult iple scan enable signals /**|r**N. Devtaprasanna, A. Gunda, P.

Krishnamurthy, S. Reddy and I. Pomeranz -- |tAt-speed logic BIST architecture for multi-clock designs /|rL.-T. Wang, X. Wen, P.-C. Hsu, S. Wu and J. Guo -- |tHardware efficient LB IST with complementary weights /|rL. Lai, J. Patel, T. Rind erknecht and W.-T. Cheng --

505 8 0 |tFRAM memory technology - advantages for low power, fast w rite, high endurance applications /|rR. Bailey, G. Fox, J. Eliason, M. Depner, D. Kim, E. Jabillo, J. Groat, J. Walber t, T. Moise, S. Summerfelt, K. Udayakumar, J. Rodriquez, K. Remack, K. Boku and J. Gertas -- |tThermal MRAM /|rJ. Deak -- |tFuture directions of non-volatile memory technologies /|rA. Fazio -- |tA high performance sub-pipelined architect ure for AES /|rH. Li and J. Li -- |tSurfliner : a distortio nless electrical signaling scheme for speed of light on-chi p communications /|rH. Chen, R. Shui, C.-K. Cheng and D. Ha rris --

505 8 0 |tPartial-parallel LDPC decoder based on high-efficiency me ssage-passing algorithm /|rK. Shimizu, T. Ishikawa, N. Toga wa, T. Ikenaga and S. Goto -- |tFast minimum and maximum se lection /|rA. Grushin -- |tThree-dimensional cache design e xploration using 3DCacti /|rY.-F. Tsai, Y. Xie, N. Vijaykri shnan and M. Irwin -- |tImplementing caches in a 3D technol ogy for high performance processors /|rK. Puttaswamy and G. Loh -- |tArchitectural-level fault tolerant computation in nanoelectronic processors /|rW. Rao, A. Orailoglu and R. Ka rri -- |tFormal verification and its impact on the snooping versus directory protocol debate /|rM. Martin --

505 8 0 |tDeployment of better than worst-case design : solutions a nd needs /|rT. Austin and V. Bertacco -- |tBenefits and cos ts of power-gating technique /|rH. Jiang, M. Marek-Sadowska and S. Nassif -- |tA dual-Vt layout approach for statistica l leakage variability minimization in nanometer CMOS /|rM. Ashouei, A. Chatterjee, A. Singh and V. De -- |tA low-overh ead virtual rail technique for SRAM leakage power reduction /|rJ. Kuang, H. Ngo, K. Nowka, J. Law and R. Joshi -- |tTut orial on RF technologies /|rD. Schmidt -- |tState set manag ement for SAT-based unbounded model checking /|rK. Chandras ekar and M. Hsiao -- |tReconsidering Cegar : learning good abstractions without refinement /|rA. Gupta and E. Clarke - -

505 8 0 |tFormal verification of parametric multiplicative division implementations /|rN. Kikkeri and P.-M. Seidel -- |tChallen ges in the formal verification of complete state-of-the-art processors /|rN. Ayewah, N. Kikkeri, P.-M. Seidel and S. Be yer -- |tReCast : boosting tag line buffer coverage in low- power high-level caches "for free" /|rW.-H. Park, A. Moshov os and B. Falsafi -- |tLoad-store queue management : an ene

rgy-efficient design based on a state-filtering mechanism /|rF. Castro, D. Chaver, L. Pinuel, M. Prieto, F. Tirado and M. Huang -- |tOptimizing the thermal behavior of subarrayed data caches /|rJ. John, J. Hu and S. Ziavras --

505 80 |tVALVE : variable length value encoder for off-chip data b uses /|rD. Suresh, B. Agrawal, W. Najjar and J. Yang -- |tM onitoring temperature in FPGA based SoCs /|rS. Velusamy, W. Huang, J. Lach, M. Stan and K. Skadron -- |tReducing the en ergy of speculative instruction schedulers /|rY. Liu, G. Me mik and G. Reinman -- |tA new pointer-based instruction que ue design and its power-performance evaluation /|rM. Ramire z, A. Cristal, A. Veidenbaum, L. Villa and M. Valero -- |tP ower-efficient wakeup tag broadcast /|rJ. Sharkey, K. Ghose , D. Ponomarev and O. Ergin -- |tSST : symbiotic subordinat e threading /|rR. Mameesh and M. Franklin -- |tMemory bank predictors /|rS. Bieschewski, J.-M. Parcerisa and A. Gonzal ez --

505 80 |tH-SIMD machine : configurable parallel computing for matr ix multiplication /|rX. Xu and S. Ziavras -- |tTemperature- sensitive loop parallelization for chip multiprocessors /|r S. Narayanan, G. Chen, M. Kandemir and Y. Xie -- |tBroadban d impedance matching for inductive interconnect in VLSI pac kages /|rB. LaMeres and S. Khatri -- |tTemperature-aware vo ltage islands architecting in system-on-chip design /|rW.-L . Hung, G. Link, Y. Xie, N. Vijaykrishnan, N. Dhanwada and J. Conner -- |tTemporal decomposition for logic optimizatio n /|rN. Kitchen and A. Kuehlmann -- |tAttacking control ove rhead to improve synthesized asynchronous circuit performan ce /|rL. Plana, S. Taylor and D. Edwards --

505 80 |tAn improved approach for alternative wires identification /|rY.-C. Chen and C.-Y. Wang.

596 |a14

650 0 |aMicrocomputers|0http://id.loc.gov/authorities/subjects/sh 85084804|xDesign and construction|0http://id.loc.gov/author ities/subjects/sh2002006372|vCongresses.|0http://id.loc.gov /authorities/subjects/sh99001533

650 0 |aElectronic digital computers|xCircuits|vCongresses.|0http ://id.loc.gov/authorities/subjects/sh2009124809

650 0 |aIntegrated circuits|xVery large scale integration|vCongre sses.|0http://id.loc.gov/authorities/subjects/sh2008104263

650 0 |aComputer engineering|vCongresses.|0http://id.loc.gov/auth orities/subjects/sh2009121192

655 7 |aConference papers and proceedings.|2lcgft

710 2 |aIEEE Computer Society.|bDesign Automation Technical Commi ttee.|0http://id.loc.gov/authorities/names/n91109047

918 |a1871992

```
918   |a1871992
918   |a1871992
918   |a1871992
994   |aZ0|bNRC
917   |au1871992
```

ATTACHMENT 1B

OCLC 62240543 **No holdings in XXX - 11 other holdings**

Books

						Rec Stat		**Entered**	20051108	**Replaced**	20220609120435.4
Type	a	**ELvl**	l	**Srce**	d	**Audn**		**Ctrl**		**Lang**	eng
BLvl	m	**Form**		**Conf**	1	**Biog**		**MRec**		**Ctry**	cau
		Cont	b	**GPub**		**LitF**	0	**Indx**	1		
Desc	a	**Ills**	a	**Fest**	0	**DtSt**	s	**Dates**	2005,		

040 IXA $b eng $c IXA $d YDXCP $d OCLCF $d OCLCQ $d OCL $d OCLCO
020 0769524516
020 9780769524511
050 4 TK7888.4 $b .I23 2005
090 $b
111 2 IEEE International Conference on Computer Design $n (23rd : $d 2005 : $c San Jose, Calif.)
245 10 2005 International Conference on Computer Design : $b proceedings : [VLSI in computers & processors] : 02-05 October, 2005, San Jose, CA / $c sponsored by IEEE Computer Society Design Automation Technical Committee (DATC) [and others].
246 14 ICCD 2005
246 30 International Conference on Computer Design
246 30 Computer Design
246 30 VLSI in computers & processors
260 Los Alamitos, Calif. : $b IEEE Computer Society, $c ©2005.
300 xix, 720 pages : $b illustrations ; $c 28 cm
336 text $b txt $2 rdacontent
337 unmediated $b n $2 rdamedia
338 volume $b nc $2 rdacarrier
500 "IEEE Computer Society Order Number P2451"--Title page verso.
504 Includes bibliographical references and author index.
650 0 Microcomputers $x Design and construction $v Congresses.
650 0 Electronic digital computers $x Circuits $v Congresses.
650 0 Integrated circuits $x Very large scale integration $v Congresses.
650 0 Computer engineering $v Congresses.
650 6 Ordinateurs $0 (CaQQLa)201-0035980 $x Circuits $0 (CaQQLa)201-0035980 $v Congrès. $0 (CaQQLa)201-0378219
650 6 Circuits intégrés à très grande échelle $0 (CaQQLa)201-0117255 $v Congrès. $0 (CaQQLa)201-0378219
650 6 Ordinateurs $0 (CaQQLa)201-0015833 $x Conception et construction $0 (CaQQLa)201-0015833 $v Congrès. $0 (CaQQLa)201-0378219
650 7 Computer engineering. $2 fast $0 (OCoLC)fst00872078
650 7 Electronic digital computers $x Circuits. $2 fast $0 (OCoLC)fst00907124
650 7 Integrated circuits $x Very large scale integration. $2 fast $0 (OCoLC)fst00975602
650 7 Microcomputers $x Design and construction. $2 fast $0 (OCoLC)fst01019653
655 7 Conference papers and proceedings. $2 fast $0 (OCoLC)fst01423772
710 2 IEEE Computer Society. $b Design Automation Technical Committee.

ATTACHMENT 1C

LIBRARY OF CONGRESS AUTHORITIES

LC control no.: sh 85084804
LCCN Permalink: https://lccn.loc.gov/sh85084804
HEADING: Microcomputers

000 00633cz a2200241n 450
001 4735254
005 20120327093812.0
008 860211i| anannbabn |b ana
010 __ |**a** sh 85084804
035 __ |**a** (DLC)sh 85084804
035 __ |**a** (DLC)81939
040 __ |**a** DLC |**c** DLC |**d** DLC
150 __ |**a** Microcomputers
450 __ |**a** Home computers
450 __ |**a** Micro computers
450 __ |**a** Micros (Microcomputers)
450 __ |**a** PCs (Microcomputers)
450 __ |**a** Personal computers
450 __ |**a** Small computers
550 __ |**w** g |**a** Minicomputers
670 __ |**a** Random House |**b** (micro (pl. micros) and PC)
906 __ |**t** 9244 |**u** te05 |**v** 0
953 __ |**a** xx00 |**b** ta25

Previous Next

Save, Print or Email Records (View Help)

Select Download Format: Text (Labelled Display) Press to SAVE or PRINT

Email Text (Labelled Display) to:
Press to SEND EMAIL

Help - Search - Search History - Headings List - Start Over



Library of Congress
URL: https://www.loc.gov/

Mailing Address:
101 Independence Ave, S.E.
Washington, DC 20540

URL: http://authorities.loc.gov/
Library of Congress Online Catalog
URL: https://catalog.loc.gov/

Questions, comments, error reports: Contact Us

ATTACHMENT 1D

LIBRARY OF CONGRESS AUTHORITIES

LC control no.: sh 87005579

LCCN Permalink: https://lccn.loc.gov/sh87005579

HEADING: Design and construction

000 00664cz a2200169n 450

001 4810729

005 20110729124740.0

008 870902n| bnannbbbn |n ann

010 __ |**a** sh 87005579

035 __ |**a** (DLC)sh 87005579

035 __ |**a** (DLC)157414

040 __ |**a** DLC |**c** DLC |**d** DLC

150 __ |**a** Design and construction

260 __ |**i** subdivision |**a** Design and construction |**i** under individual examinations and types of examinations and under types of structures, machines, equipment, etc., for works discussing their engineering, and/or construction, e.g. |**a** Automobiles--Design and construction

906 __ |**t** 8846 |**u** fk03 |**v** 0

952 __ |**a** 0 bib. record(s) to be changed

953 __ |**a** fj26 |**b** fj26

◀ Previous Next ▶

Save, Print or Email Records (View Help)

Select Download Format: Text (Labelled Display) Press to SAVE or PRINT

Email Text (Labelled Display) to: Press to SEND EMAIL

Library of Congress
URL: https://www.loc.gov/

Mailing Address:
101 Independence Ave,

Library of Congress Authorities
URL: http://authorities.loc.gov/
Library of Congress Online Catalog
URL: https://catalog.loc.gov/

Questions, comments, error reports: Contact Us

AMD EX1021
AMD v. Realtek - Page 108

 S.E.
Washington, DC 20540

ATTACHMENT 1E

LC control no.: sh 85031115

LCCN Permalink: https://lccn.loc.gov/sh85031115

HEADING: Congresses and conventions

000 01730cz a2200337n 450

001 4683355

005 20140118055927.0

008 860211i| anannbabn |b ana

010 __ |**a** sh 85031115

035 __ |**a** (DLC)sh 85031115

035 __ |**a** (DLC)30040

040 __ |**a** DLC |**c** DLC |**d** DLC |**d** WaU |**d** DLC

053 _0 |**a** AS

150 __ |**a** Congresses and conventions

360 __ |**i** subdivision |**a** Congresses |**i** under subjects; and names of individual congresses

450 __ |**a** Colloquia

450 __ |**a** Colloquiums

450 __ |**a** Conferences

450 __ |**a** Conventions (Congresses)

450 __ |**a** International conferences, congresses and conventions

450 __ |**a** Symposia

450 __ |**a** Symposiums

550 __ |**w** g |**a** Intellectual cooperation

550 __ |**a** Convention facilities

670 __ |**a** Random House Kernerman Webster's college dictionary, ©2010, via TheFreeDictionary.com, Aug. 29, 2013 |**b** (colloquium n., pl. -quiums, -quia a conference at which scholars or other experts present papers on and discuss a specific topic)

670 __ |**a** The American heritage dictionary of the English language, ©2000, via TheFreeDictionary.com, Aug. 29, 2013 |**b** (colloquium n. pl. colloquiums or colloquia 1. An informal meeting for the exchange of views. 2. An academic seminar on a broad field of study, usually led by a different lecturer at each meeting.)

670 __ |**a** Merriam-Webster online, Aug. 29, 2013 |**b** (colloqium plural colloquiums or -quia: a usually academic meeting at which specialists deliver addresses on a topic or on related topics and then answer questions relating to them)

906 __ |**t** 9921 |**u** te04 |**v** 0

910 __ |**a** Record saved by ec04 on 01/17/2014 at 16:02:37
910 __ |**a** Record saved by ec11 on 09/03/2013 at 08:55:33
953 __ |**a** xx00 |**b** sg08

Previous Next

Save, Print or Email Records (View Help)

Select Download Format: Text (Labelled Display) Press to SAVE or PRINT

Email Text (Labelled Display) to:
Press to SEND EMAIL

Help - Search - Search History - Headings List - Start Over



Library of Congress
URL: https://www.loc.gov/

Mailing Address:
101 Independence Ave, S.E.
Washington, DC 20540

Library of Congress Authorities
URL: http://authorities.loc.gov/
Library of Congress Online Catalog
URL: https://catalog.loc.gov/

Questions, comments, error reports: Contact Us

ATTACHMENT 1F

LIBRARY OF CONGRESS AUTHORITIES

LC control no.: sh2009124809

LCCN Permalink: https://lccn.loc.gov/sh2009124809

HEADING: Electronic digital computers Circuits Congresses

000 00472cz a2200169n 450
001 8045006
005 20110729162632.0
008 091006|| anannbabn |n ana
010 __ |**a** sh2009124809
035 __ |**a** (DLC)440650
035 __ |**a** (DLC)sh2009124809
040 __ |**a** DLC |**b** eng |**c** DLC
150 __ |**a** Electronic digital computers |**x** Circuits |**v** Congresses
667 __ |**a** Record generated for validation purposes.
670 __ |**a** Work cat.: Proceedings, c2003-
906 __ |**t** 8888 |**u** tc00 |**v** 0
953 __ |**a** tc00

◀ Previous Next ▶

Save, Print or Email Records (View Help)

Select Download Format: Text (Labelled Display) Press to SAVE or PRINT

Email Text (Labelled Display) to: Press to SEND EMAIL

Library of Congress
URL: https://www.loc.gov/

Mailing Address:
101 Independence Ave, S.E.
Washington, DC 20540

Library of Congress Authorities
URL: http://authorities.loc.gov/
Library of Congress Online Catalog
URL: https://catalog.loc.gov/

Questions, comments, error reports: Contact Us

AMD EX1021
AMD v. Realtek - Page 114

ATTACHMENT 1G

LIBRARY OF CONGRESS AUTHORITIES

LC control no.: sh2008104263

LCCN Permalink: https://lccn.loc.gov/sh2008104263

HEADING: Integrated circuits Very large scale integration Congresses

000 00507cz a2200169n 450
001 7450384
005 20110729160306.0
008 080211|| anannbabn |n ana
010 __ |**a** sh2008104263
035 __ |**a** (DLC)381067
035 __ |**a** (DLC)sh2008104263
040 __ |**a** DLC |**b** eng |**c** DLC
150 __ |**a** Integrated circuits |**x** Very large scale integration |**v** Congresses
667 __ |**a** Record generated for validation purposes.
670 __ |**a** Work cat.: Proceedings of the IEEE INDICON 2004, c2004
906 __ |**t** 8888 |**u** te00 |**v** 0
953 __ |**a** te00

◀ Previous Next ▶

Save, Print or Email Records (View Help)

Select Download Format: Text (Labelled Display) Press to SAVE or PRINT

Email Text (Labelled Display) to: Press to SEND EMAIL

Library of Congress
URL: https://www.loc.gov/

Mailing Address:
101 Independence Ave, S.E.
Washington, DC 20540

Library of Congress Authorities
URL: http://authorities.loc.gov/
Library of Congress Online Catalog
URL: https://catalog.loc.gov/

Questions, comments, error reports: Contact Us

AMD EX1021
AMD v. Realtek - Page 116

ATTACHMENT 1H

LIBRARY OF CONGRESS AUTHORITIES

LC control no.: sh2009121192
LCCN Permalink: https://lccn.loc.gov/sh2009121192
HEADING: Computer engineering Congresses

000 00480cz a2200169n 450
001 7982654
005 20110729162416.0
008 090811|| anannbabn |n ana
010 __ |**a** sh2009121192
035 __ |**a** (DLC)434629
035 __ |**a** (DLC)sh2009121192
040 __ |**a** DLC |**b** eng |**c** DLC
150 __ |**a** Computer engineering |**v** Congresses
667 __ |**a** Record generated for validation purposes.
670 __ |**a** Work cat.: Hardware and software design automation, 1991
906 __ |**t** 8888 |**u** tc00 |**v** 0
953 __ |**a** tc00

◀ Previous Next ▶

Save, Print or Email Records (View Help)

Select Download Format: Text (Labelled Display) Press to SAVE or PRINT

Email Text (Labelled Display) to: Press to SEND EMAIL

Library of Congress
URL: https://www.loc.gov/

Mailing Address:
101 Independence Ave, S.E.
Washington, DC 20540

Library of Congress Authorities
URL: http://authorities.loc.gov/
Library of Congress Online Catalog
URL: https://catalog.loc.gov/

Questions, comments, error reports: Contact Us

AMD EX1021
AMD v. Realtek - Page 118

ATTACHMENT 2

April 2006 • Volume 11 • Number 2

RECEIVED
UCF LIBRARY
JUL 24 2006
SERIALS

ACM Transactions on Design Automation of Electronic Systems

M. AYALA-RINCÓN C. H. LLANOS R. P. JACOBI R. W. HARTENSTEIN	251	Prototyping Time- and Space-Efficient Computations of Algebraic Operations over Dynamically Reconfigurable Systems Modeled by Rewriting-Logic
J. ABSAR F. CATTHOOR	282	Reuse Analysis of Indirectly Indexed Arrays
A. DASDAN I. HOM	306	Handling Inverted Temperature Dependence in Static Timing Analysis
Z. LI X. HONG Q. ZHOU J. BIAN H. H. YANG V. PITCHUMANI	325	Efficient Thermal-Oriented 3D Floorplanning and Thermal Via Planning for Two-Stacked-Die Integration
S. PADMANABAN S. TRAGOUDAS	346	Implicit Grading of Multiple Path Delay Faults
D. CHEN J. CONG J. XU	362	Optimal Simultaneous Module and Multivoltage Assignment for Low Power
H. ZHU C.-K. CHENG R. GRAHAM	387	On the Construction of Zero-Deficiency Parallel Prefix Circuits with Minimum Depth
M. T. KANDEMIR	410	Reducing Energy Consumption of Multiprocessor SoC Architectures by Exploiting Memory Bank Locality
F. SU S. OZEV K. CHAKRABARTY	442	Concurrent Testing of Digital Microfluidics-Based Biochips

Continued on back cover

AMD EX1021
AMD v. Realtek - Page 120

Continued from front cover.

D. ATIENZA J. M. MENDIAS S. MAMAGKAKIS D. SOUDRIS F. CATTHOOR	**465**	Systematic Dynamic Memory anagement Design Methodology for Reduced Me ory Footprint
W. LI D. BLAKELY S. VAN SOOY K. DUNN D. KIDD R. ROGENMOSER D. ZHOU	**490**	LVS Verification across Multiple Power Domains for a Quad-Core Microprocessor
J. A. CHEATHAM J. M. EMMERT S. BAUMGART	**501**	A Survey of Fault Tolerant Methodologies for FPGAs

AUTO *** ********** ORIGIN MIXED ADC 216
5954516 20 EXPIRE 0612 395 JUN2D 01 00/002
STATE UNIVERSITIES OF FLORIDA /TODAES-4 0005
UNIV.CENTRAL FLORIDA
LIBRARY - ACQ
P.O. BOX 162666

AMD EX1021
AMD v. Realtek - Page 121

ACM Transactions on Design Automation of Electronic Systems

ACM
1515 Broadway
New York, NY 1003
Tel.: (212) 869-7440
Fax: (212) 869-0481

TODAES Home Page: http://ww .acm.org/pubs/todaes

Editor-in-Chief

Nikil Dutt — Department of Computer Science / University of California / Ir ine, CA 92697 / email: dutt@uci.edu

Associate Editors

Francky Catthoor — *Low Power System Design, Platform Architecture Exploration for Multi-media ,and Wireless Systems* / IMEC / B-3001 Leuven, Belgium / email: catthoor@imec.be

Sreejit Chakravarty — *System Testing* / Intel / Santa Clara, CA 95054 / email: sreejit.chakravarty@intel.com

Kwang-Ting (Tim) Cheng — *System Testing, Design Synthesis, Design Verification* / Department of Electrical and Computer Engineering / University of California / Santa Barbara, CA 93106 / email: timcheng@ece.ucsb.edu

Peter Cheung — *High-level Synthesis, Reconfigurable Computing, and Low Power Design* / Department of Electrical and Electronic Engineering / Imperial College / London SW7 2BT, England / email: p.cheung@imperial.ac.uk

Kiyoung Choi — *Hardware/Software Codesign, High-level Synthesis, and Low-p wer System Design* / School of EECS / Seoul National University / Seoul 151-742, Kore / email: kchoi@azalea.snu.ac.kr

Steven German — *Design Verification* / IBM T.J. Watson Research Center / Yorktow Heights, NY 10598 / email: german@watson.ibm.com

Xiaobo Sharon Hu — *Hardware/Software Codesign, Real-time Systems, and Power/ nergy-aware Design* / Department of Computer Science and Engieering / University Notre Dame / Notre Dame, IN 46556 / email: hu@cse.nd.edu

TingTing Hwang — *Logic Synthesis* / Department of Computer Science / Tsing Hu University / Hsin-Chu 300, Taiwan / email: tingting@cs.nthu.edu.tw

Mahmut Taylan Kandemir — *Embedded Software, Memory System Design, and Power-aware rchitectures* / Department of Computer Science and Engineering / Pennsylvania State University / University Park, PA 16802 / email: kandemir@cse.psu.edu

Cheng-Kok Koh — *Physical Layout, Circuit Design and Synthesis* / School of Electric and Computer Engineering / Purdue University / 465 Northwestern Avenue / West afayette, IN 47907 / email: chengkok@purdue.edu

Sharad Malik — *System Design, Synthesis, and Verification* / Department of Electrical Engineering / Princeton University / Princeton, NJ 08544 / email: sharad@princeton.edu

Radu Marculescu — *System-level Synthesis and Optimization, Emerging Applications, and Design Methodologies* / Department of Electrical and Computer Engineering / Carnegie Mellon University / Pittsburgh, PA 15213 / email: radum@ece.cmu.edu

Dirk Stroobandt — *Embedded Systems, High-level Synthesis, and Reconfigurable Architectures* / Department of Electronics and Information Systems / Ghent University / B-9000 Gent, Belgium / email: dirk.stroobandt@elis.ugent.be

Hiroyuki Tomiyama — *System Design and High-level Synthesis* / Graduate School of Information Science / Nagoya University / Nagoya 464-8603, Japan / email: hiroyuki@acm.org

Sarma Vrudhula — *Low Power System Design, Formal Verification, and Built-in Self Test* / Department of Computer Science and Engineering / Arizona State University / Tempe, AZ 85281 / email: vrudhula@asu.edu

Martin D. F. Wong — *Physical Layout / Department of Electrical and Computer Engineering* / University of Illinois at Urbana-Champaign / Urbana, IL 61801 / email: mdfwong@uiuc.edu

Hans-Joachim Wunderlich — *System Testing* / Institut für Technische Informatik / University of Stuttgart / D-70569 Stuttgart, Germany / email: wu@informatik.uni-stuttgart.de

Information Director

Prabhat Mishra — Department of Computer and Information Science and Engineering / University of Florida / Gainesville, FL 32611 / email: mishra@acm.org

Editorial Assistant

Melanie Sanders — Department of Computer Science / University of California / Irvine, CA 92697 / email: msanders@ics.uci.edu

Headquarters Journals Staff

Mark Mandelbaum — Director of Publications
Jono Hardjowirogo — Publisher, Associate Director of Publications
Roma Simon — Managing Editor
Irma Strolia — Editorial Assistant
Media Content Marketing — Production

ACM Transactions on Design Automation of Electronic Systems (ISSN: 1084-4309) is published 4 times a year in January, April, July, and October by the Association for Computing Machinery (ACM), 1515 Broadway, New York, NY 10036. Periodicals class postage paid at New York, NY 10001, and at additional mailing offices. Printed in the U.S.A. POSTMASTER: Send address changes to *ACM Transactions on Design Automation of Electronic Systems*, ACM, 1515 Broadway, New York, NY 10036.

For manuscript submissions, subscription, and change of address information, see inside backcover.

Copyright © 2006 by the Association for Computing Machinery (ACM). Permission to make digital or hard copies of part or all of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. Copyrights for components of this work owned by others than ACM must be honored. Abstracting with credit is permitted. To copy otherwise, to republish, to post on servers, or to redistribute to lists, requires prior specific permission and/or a fee. Request permission to republish from: Publications Department, ACM, Inc. Fax +1 212-869-0481 or email permissions@acm.org. For other copying of articles that carry a code at the bottom of the first or last page or screen display, copying is permitted provided that the per-copy fee indicated in the code is paid through the Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

This material may be protected by Copyright law (Title 17 U.S. Code)

LVS Verification across Multiple Power Domains for a Quad-Core Microprocessor

WEI LI, DANIEL BLAKELY, SCOTT VAN SOOY, KEVEN DUNN, DAVID KIDD, and ROBERT ROGENMOSER
Broadcom Corp.
and
DIAN ZHOU
University of Texas at Dallas

A unique LVS (layout-versus-schematic) methodology has been developed for the verification of a four-core microprocessor with multiple power domains using a triple-well 90-nm CMOS technology. The chip is migrated from its previous generation that is for a twin-well process. Due to the design reuse, VDD and GND are designed as global nets but they are not globally connected across the entire chip. The standard LVS flow is unable to handle the additional design complexity and there seems to be no published literature tackling the problem. This paper presents a two-phase LVS methodology: a standard LVS phase where power and ground nets are defined as global nets and a multi-power-domain LVS phase where power and ground nets are treated as local nets. The first phase involves verifying LVS at the block level as well as the full-chip level. The second phase aims at verifying the integrity of the multi-power-domain power grid that is not covered in the first phase LVS. The proposed LVS methodology was successfully verified by real silicon.

Categories and Subject Descriptors: B.7.1 [**Integrated Circuits**]: Types and Design Styles—*Microprocessors and microcomputers; VLSI (Very large scale integration)*; B.7.2 [**Integrated Circuits**]: Design Aids—*Layout; verification*; J.6 [**Computer-Aided Engineering**]: *Computer-aided design (CAD)*

General Terms: Design, Verification

Additional Key Words and Phrases: LVS, physical verification, multi-core microprocessor

1. INTRODUCTION

As semiconductor technology advances into 90-nanometer and beyond, microprocessor design has evolved into today's very competitive battle to produce complex multicore architectures. Multiple processor cores on a single die can

Authors' addresses: W. Li, D. Blakely, S. Van Sooy, K. Dunn, D. Kidd, and R. Rogenmoster, Broadcom Corporation, 2451 Mission College Boulevard, Santa Clara, CA 95054; D. Zhou, Department of Electrical Engineering, The University of Texas at Dallas, Richardson, TX 75083; email: Weili@broadcom.com.

Permission to make digital or hard copies of part or all of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or direct commercial advantage and that copies show this notice on the first page or initial screen of a display along with the full citation. Copyrights for components of this work owned by others than ACM must be honored. Abstracting with credit is permitted. To copy otherwise, to republish, to post on servers, to redistribute to lists, or to use any component of this work in other works requires prior specific permission and/or a fee. Permissions may be requested from Publications Dept., ACM, Inc., 1515 Broadway, New York, NY 10036 USA, fax: +1 (212) 869-0481, or permissions@acm.org.
© 2006 ACM 1084-4309/06/0400-0490 $5.00

AMD EX1021
AMD v. Realtek - Page 123

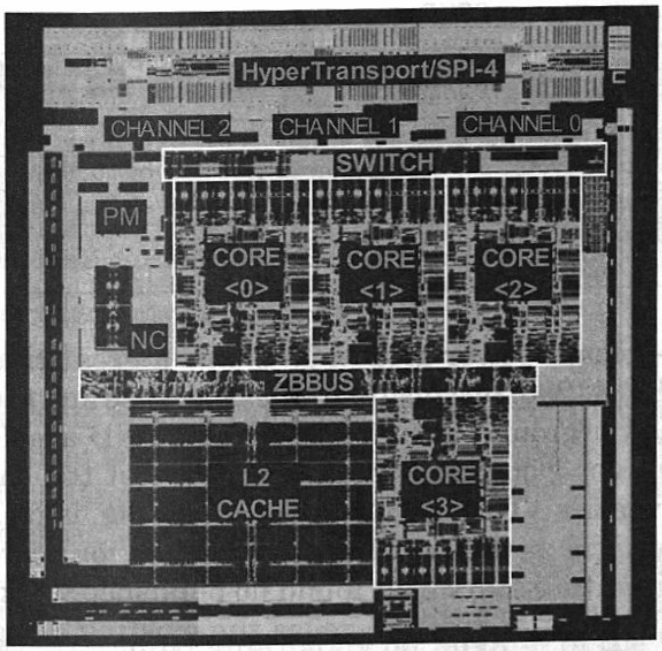


Fig. 1. Chip detailed floorplan.

operate in various ways to yield scalable performance in a complexity- and power-efficient manner [Brooks et al. 2000]. The combination of continually rising complexity of chip design and tightening time-to-market schedule has forced designers to seek new methods to accelerate the development process. The use of core-based designs, the reuse of existing IP, and efficient verification methodologies have all helped to expedite the processor design cycle.

A system on a chip (SOC) BCM1280 has been designed with four 64-bit MIPS™ CPU cores, operating at Giga-Hertz frequency, as well as an on-die 1MB L2 cache, and dedicated networking hardware [Sano 2002; Moll 2004]. Figure 1 shows a detailed floorplan of the chip. BCM1280 is implemented with 164 million transistors on a 13.9×14.1 mm^2 die. It is fabricated with a 90-nanometer triple-well bulk CMOS process with seven routing metal layers and a redistribution metal layer dedicated to power and ground nets from the package to the chip. The CPU core is migrated from a previous twin-well process design, in which the power grid (VDD/GND) was designed and verified as global nets across the entire chip. In this quad-core microprocessor, four CPU cores are identical and each sits in a separate triple-well region. Each single core, isolated from the others by a triple-well, forms a separate processor region. Therefore, under the full-chip context, each core is now built in a unique voltage region. In addition to the complexity of the multiple ground domains, the chip is divided into two logic voltage regions (1.1V). The previous generation chip, from which BCM1280 is migrated, was designed with one power supply only.

Due to the manual nature of the layout construction in a full-custom design, physical verification is very critical to the success of the chip design. One of the most important key steps to perform physical verification on the layout design is to verify that the layout matches the schematic. This is so called LVS (layout-versus-schematic), which involves checking the consistency between the original schematic netlist and the one extracted from the layout. Analyzing

AMD EX1021
AMD v. Realtek - Page 124

Table I. Process Characteristics

Process	Triple-Well Bulk CMOS P+ Substrate
Feature size	90 nm
Clock frequency	1 GHz
Metal Layers	7 copper layer 1 redistribution layer
Supply Voltages	1.1V, 2.5V and 3.3V
Typical Power	25W
Package	Flipchip

the multi-power-domain power grid in LVS was a great challenge to us during the design of BCM1280. Because of the design reuse and the implementation of the multiple power/ground domains, VDD and GND are designed as global nets, but they are not globally connected throughout the chip. The standard LVS flow, which verifies VDD and GND as global nets, is no longer functional in verifying power grid at the full-chip level for this four-core microprocessor. In an extensive literature search, we found no published work tackling the considered problem. Hence, in order to reuse the existing design and make the fewest changes to the reused design, we need to come up with a special LVS methodology. In this article, we present an LVS methodology for a four-core microprocessor designed with multiple power domains, given the fact that the microprocessor core is previously designed for a chip with a single ground domain.

The rest of this article is organized as follows: The process technology in manufacturing this chip is briefly introduced in Section 2. The structure of the power grid is described in Section 3. The implementation of multiple power and ground domains is discussed in Section 4. The LVS methodology is presented in detail in Section 5. We conclude the presented work in the last section with some final remarks.

2. PROCESS TECHNOLOGY

The BCM1280 is fabricated in a 90-nanometer triple-well CMOS technology on a P-substrate. The major process characteristics are shown in Table I.

Triple-well technology allows P-wells to be placed inside a deep N-well. This type of structure electrically isolates the wells from the substrate, providing a means to isolate the n-type devices that would normally exist in the P-substrate as in a twin-well design. When a triple-well CMOS technology is used, separate voltage lines can be used to connect to the NMOS and PMOS bulk regions. Then, these lines can be modulated to provide a back-bias voltage for regions that are not operating. Large blocks of a chip can be disabled when they are not needed in order to save energy by reducing leakage current. A cross-section picture of the triple-well structure is shown in Figure 2.

3. POWER DISTRIBUTION

Power distribution systems (power grid) are designed to provide required voltages and currents to the transistors that perform the logic functions of a chip. With every technology shrink, power distribution networks do not scale due to the fact that the current demand per unit area of a design is increased. As a result, more silicon area needs to be dedicated to distributing higher currents

AMD EX1021
AMD v. Realtek - Page 125

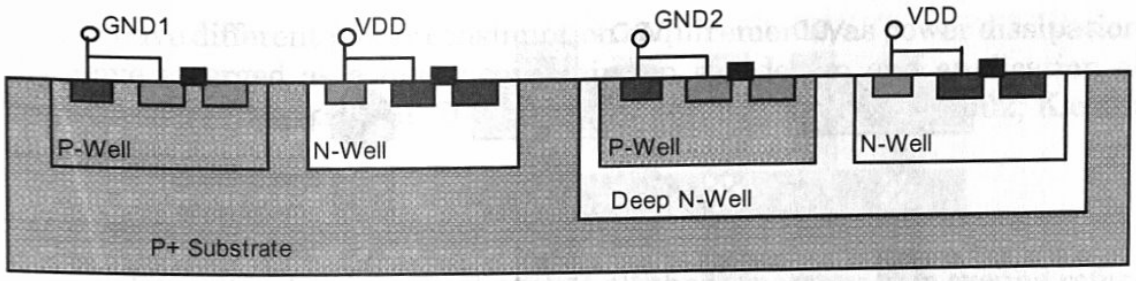


Fig. 2. Triple well structure provides an isolating N layer between the local P-well and the P-substrate.

at lower voltages [Kam et al. 2000]. Hence, power consumption has become a more and more critical issue in microprocessor design. An efficient power distribution network on large microprocessor is one of the key factors in achieving overall high performance targets of the chip.

On the BCM1280, Metal-6 and metal-7 are extensively used in distributing power and ground across the chip. Ground (GND) and power (VDD_chip, VDD_switch) lines are routed alternately on Metal-6 in the vertical direction and Metal-7 in the horizontal direction. This forms the power grid structure at the chip top level. The power and ground lines in the local sections are grided on Metal-2 through Metal-5, on which the local power grids are formed at the block level. The local power grids are left floating until final assembly at the full-chip level. At the final stage of the layout design, an in-house automated procedure is applied, connecting local logic to the top-level power grid, to implement a complete full-chip power distribution network.

Due to the trend of ever increasing die size in microprocessor design, efficient power delivery from the supply source to the chip has become very important. Flipchip technology is chosen for packaging this chip. Power and ground are supplied to the package through two VDD inputs (VDD_switch and VDD_chip) and one GND input, respectively. Pads arrayed across the active face of the die are used to connect to I/O, power and ground. Solder bumps are attached to pads. A redistribution metal layer is designated for distributing power and ground from the bump to the chip level power grid (Figure 3). With flipchip technology, power and ground bumps are connected directly to the on-chip power and ground distribution system; and these connections can be made across the entire die so power/ground is delivered wherever needed. This significantly reduces overall chip IR drop by eliminating the IR drop associated with delivering power and ground from peripheral wirebond pads.

4. MULTIPLE POWER/GROUND DOMAINS IMPLEMENTATION

BCM1280 is designed with two power supply inputs and one ground input at the package level. As a result of function and logic requirements, there are multiple voltage regions across the chip. This design style enables power-saving capability with a selectable configuration, allowing the chip to be an optimal fit into a broad variety of applications. For instance, for some applications where power consumption is a major concern, two of the four CPU cores and the correlated peripheral logic circuitry could be shut-off to achieve power efficiency.

AMD EX1021
AMD v. Realtek - Page 126

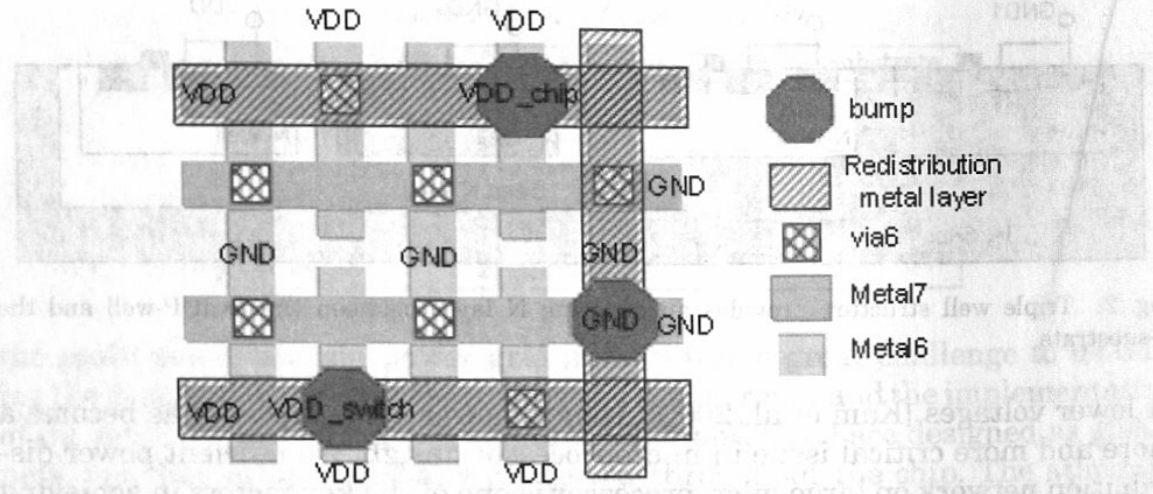


Fig. 3. Power and ground are distributed from the bumps onto the chip-level power grid through a redistribution metal layer.

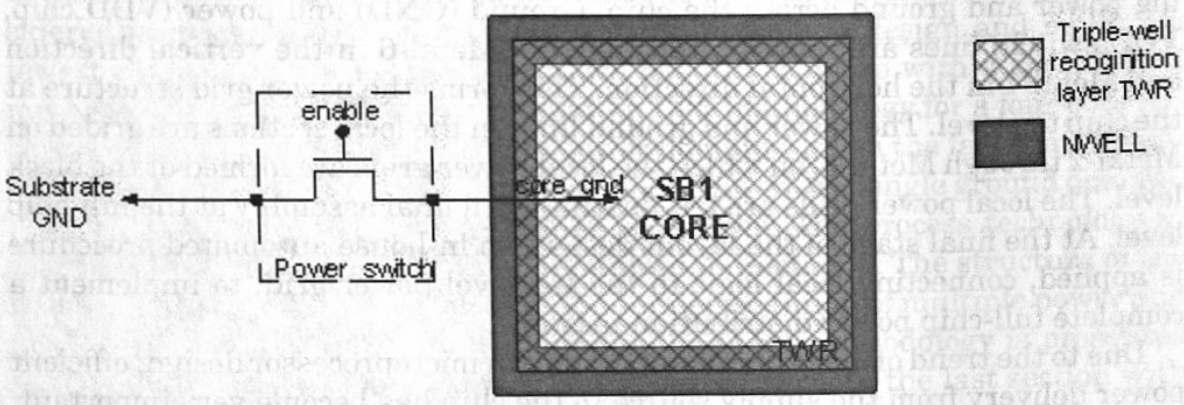


Fig. 4. An SB1 core inside triple-well with power switch.

4.1 Multiple Ground Domains Implementation

To take advantage of the triple-well technology, we have designed the chip with each microprocessor CPU core placed inside a triple well—a deep N-well, inside which the P-well is set apart from the P-substrate. Since the P-well connected to the core ground is isolated from the ground outside the core by a reverse biased deep N-well, the individual cores are electrically isolated from one another as well as the rest of the chip. As a result, BCM1280 has a total of four core grounds connected to the P-wells inside the four triple wells, respectively, and one chip ground connected to the P-substrate.

Figure 4 gives a top-down layout view of a processor core in the triple-well structure. This particular process offers a migration path for existing twin-well designs to triple-well structure by adding an NW-ring and a triple-well recognition layer (TWR) around the core. All N-wells inside the triple-well are shorted; therefore, they are all on the same potential.

A power switch structure is designed surrounding each core. As illustrated in Figure 4, the transistor's source is connected to the core ground inside the triple-well and the transistor's drain is tied to the chip ground inside the substrate. The power switch enables a single core to be turned on or off individually. This independently configurable feature is very desirable for a variety of applications

AMD EX1021
AMD v. Realtek - Page 127

that may have different power consumption requirements, as power dissipation limits have emerged as a major constraint in the design and application of microprocessors [Brooks et al. 2000; Kam et al. 2000; Iyer et al. 2002; Karnik et al. 2002].

4.2 Multiple Power Supplies Implementation

BCM1280 has several power supplies that all share the same chip ground reference. All require adequate external decoupling capacitors with low-inductance paths. The ground reference GND is common for all the power supplies. As we described in the previous section, there are two power supply inputs VDD_chip and VDD_switch at the package level in this design. VDD_chip provides power for all the internal logic except the node controller, packet manager, switch and HT/SPI-4 ports. All four CPU cores operate at the same supply voltage, VDD_chip, but use a different internal ground net for each core. The different internal ground net for each core is separated from chip ground by an NMOS switch. VDD_switch provides power for all the internal logic of the node controller (NC), packet manager (PM), switch and HT/SPI-4 ports.

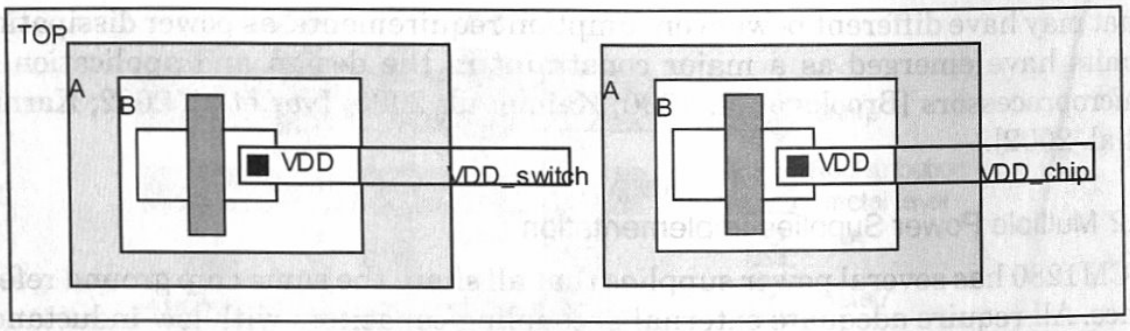
5. LVS METHODOLOGY

LVS is one of the most important physical verification steps in integrated circuit (IC) design. It serves to check the equivalency of a layout design against the corresponding schematic design. If the two designs are equivalent under the given LVS rule deck (LVS runset), then the LVS result is said to be "LVS clean". LVS tools first generate a netlist based on extracting the connectivity of an input layout stream file. The extracted netlist is then compared to the schematic netlist to ensure the two views match.

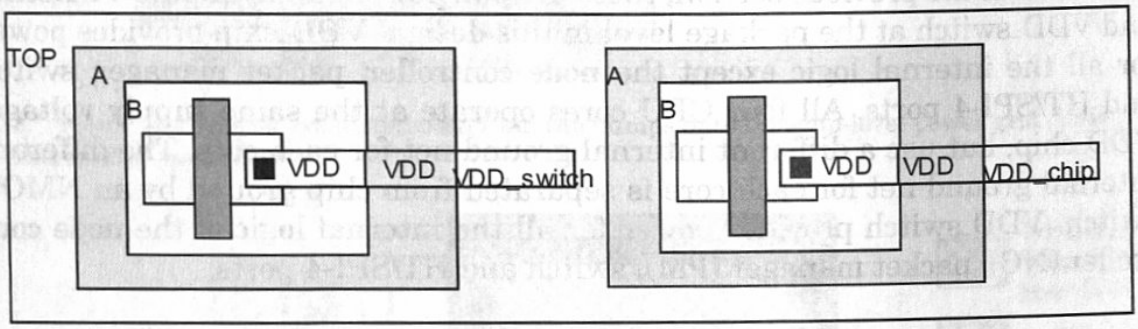
Typically, power nets are globally connected throughout the design, and so are ground nets. VDD and GND are designed as global nets at the block level, which is done to simplify the schematic level design process; treating them as local nets would require creating specific hierarchical ports for VDD and GND within each schematic. At the full-chip level, however, under the multiple power/ground domains scenario we described in the previous sections, VDD and GND can no longer be treated as global nets. LVS methodology for the block level now fails at the full-chip level. For example, a short on GND between the different processor cores cannot be detected because GND is considered to be global. The design team needed an LVS methodology that enabled each block to be independently verified during the development. They also needed the LVS flow to be capable of verifying the integrity of the chip level power grid with minimum impact in altering the design.

In this section, we discuss a two-stage LVS flow used in the BCM1280 full-chip LVS verification. It consists of a standard LVS stage (standard-LVS) where VDD and GND are defined as global nets; and a multi-power-domain LVS stage (MPD-LVS) where VDD and GND are verified as local nets. Standard-LVS would suffice for verification at the block level. HERCULES [HERCULES 2003], one of the well-known commercial LVS tool, is used for the LVS verification.

AMD EX1021
AMD v. Realtek - Page 128



(a) VDD is global net. LVS reports text shorts.



(b) VDD is local net. VDD needs to be texted at every level of the LVS equivalence point to get LVS clean.

Fig. 5. Global texts vs. local texts in hierarchical LVS processing.

5.1 Global Nets versus Local Nets in LVS

In hierarchical LVS, layout text is viewed hierarchically. In a schematic netlist, nets listed as global are assumed to be connected throughout the design during netlist comparison. Similarly, nets defined as global in layout are treated as global during netlist extraction. Global net names are dispersed through connections up the hierarchy. Local or nonglobal nets only specify a net's value for a particular hierarchical level. If two or more texts are attached to one net, LVS reports this as a *short*. A text *open* is reported, if different physical nets have the same text.

Figure 5 gives a layout example to illustrate how the LVS tool handles global texts and local texts. In Figure 5, cell TOP is the top block of the design, A is instantiated in TOP and B is placed inside A. In case 5(a), since VDD is declared as a global net, it is propagated from cell B all the way up through the hierarchy to the top level. This results in text shorts between VDD and VDD_switch, and between VDD and VDD_chip. There are two strategies, which can be utilized to solve the text conflicts in this particular case. One possible solution is that VDD needs to be treated as a local net, which would require VDD to be labeled at every LVS compare equivalence level in both the layout and the schematic. This is not desirable since it involves significant and time-consuming effort in redesigning the layout and the schematic. Another method is to use two LVS runs. In the first LVS run, VDD is kept as a global net and VDD_switch/VDD_chip labels are ignored. This will cause opens at the top level, which can be ignored at this stage, but the design can be verified without layout or schematic modifications. In the second LVS run, VDD is treated as a local net

AMD EX1021
AMD v. Realtek - Page 129

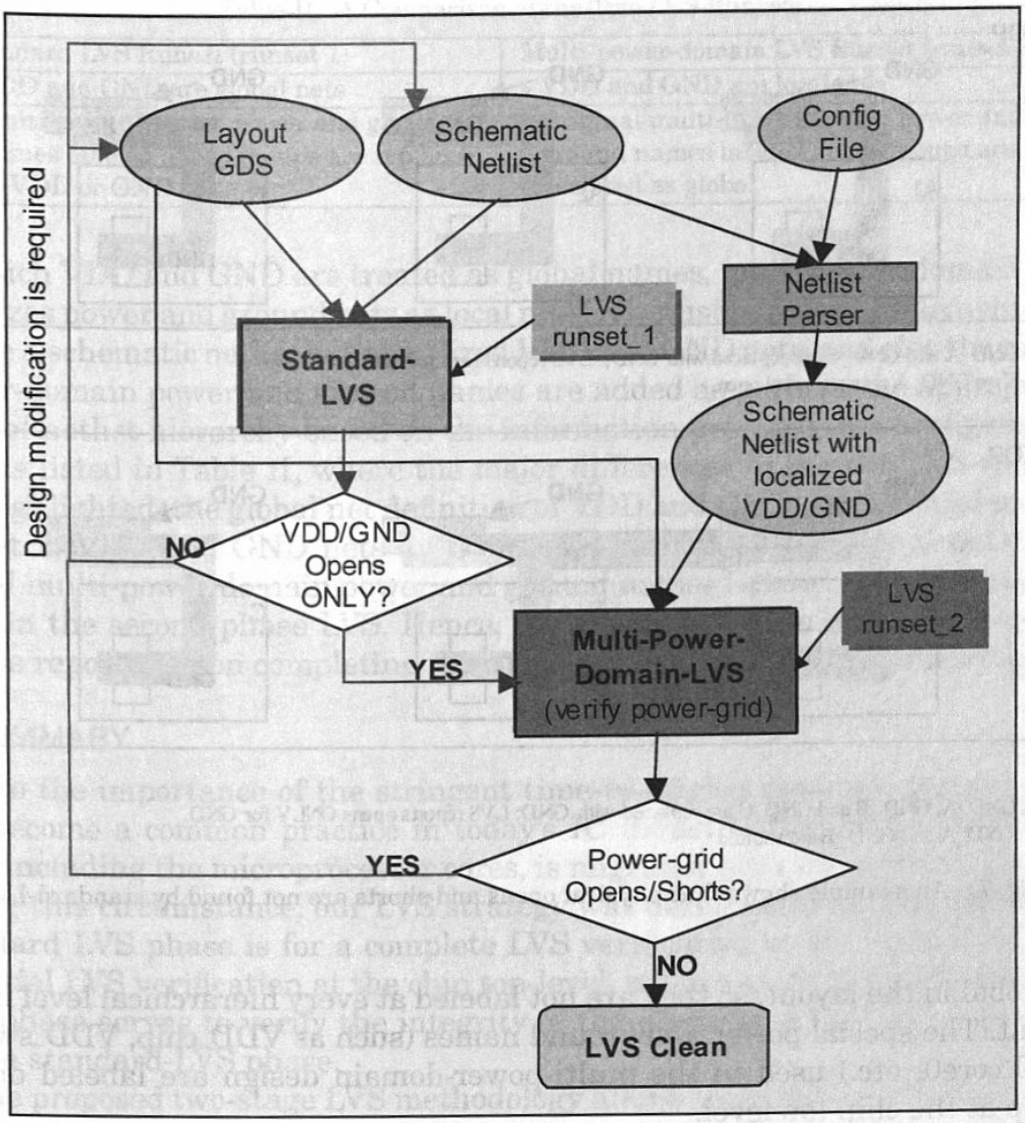


Fig. 6. Chip-level LVS verification flow chart.

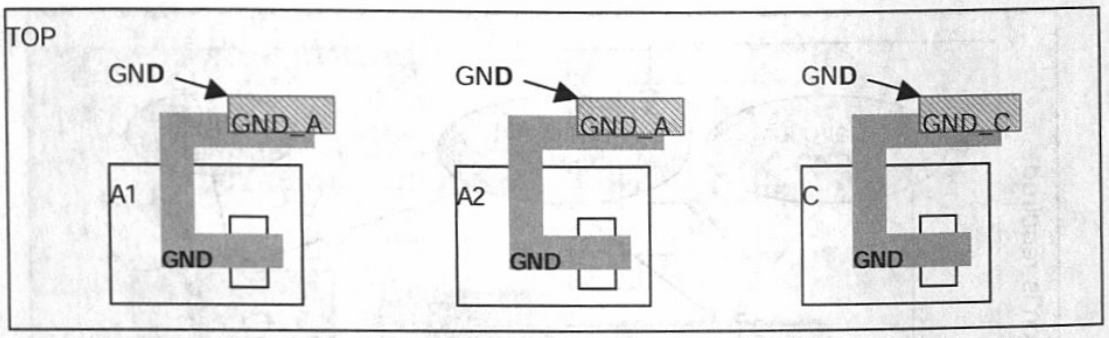
and VDD_switch/VDD_chip are treated as global nets. This ensures the opens from the first LVS run are not real and the transistors are connected to the correct power domain.

5.2 Detailed LVS Flow

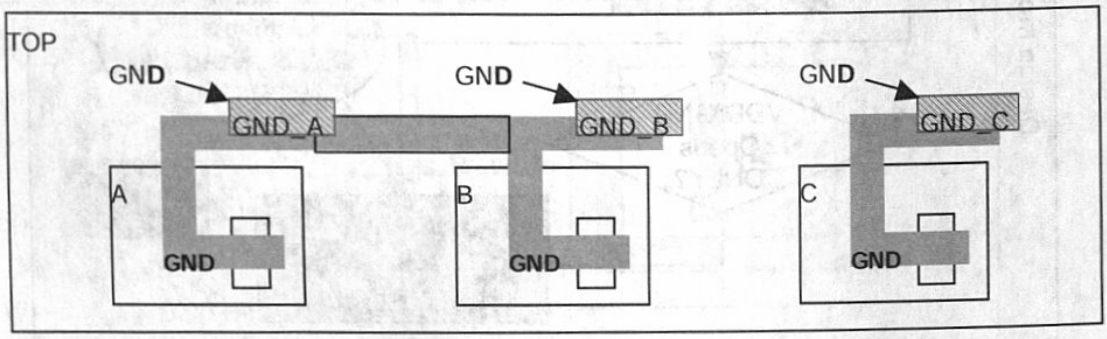
As Figure 6 shows, our LVS flow consists of two phases: a standard-LVS phase, to check the consistency between the layout and the schematic under a unitary power domain, and a multipower-domain LVS phase, to verify the top-level power grid is open/short free.

The original schematic that standard-LVS reads is a *SPICE* format netlist, where VDD and GND are specified as global names. They are assumed to be globally connected throughout the schematic netlist; therefore, they are not declared as ports in *subckt* definitions across all the netlist hierarchies. The layout stream file input to the LVS tool is in *GDSII* format. Global texts automatically propagate up and down the layout hierarchy. VDD and GND nets are designed

AMD EX1021
AMD v. Realtek - Page 130



(a) GND_A and GND_C are replaced with GND; LVS reports text opens for GND. Two GND_A nets are a real open.



(b) GND_A, GND_B and GND_C are replaced with GND; LVS reports opens ONLY for GND. GND_A and GND_B are shorted.

Fig. 7. An example shows that physical opens and shorts are not found by standard-LVS.

as global in the layout, so they are not labeled at every hierarchical level in the layout. The special power and ground names (such as VDD_chip, VDD_switch, GND_core0, etc.) used in the multi-power-domain design are labeled on the bump at the chip top level.

The LVS runset file is an ASCII file, which contains instructions for the LVS tool to get the input files and to perform the LVS check against a set of rules defined in the runset. In the LVS runset_1, power and ground names of the multi-power-domain are replaced with VDD and GND, respectively, and VDD and GND are declared as global names for both schematic and layout. During the standard-LVS run, since different power names are treated as VDD and different ground names are treated as GND, we expect to see text opens for VDD and also text opens for GND in the LVS error report. The standard-LVS is considered to be "clean" with VDD and GND text open errors only. However, we are not guaranteed that the text opens reported by LVS are the opens we created intentionally by replacing the texts. These could be real physical opens unintentionally added. It is also possible for the standard-LVS flow to hide real shorts, as illustrated in Figure 7. In the picture, A1, A2, A, B and C are placed inside TOP. All the top-level texts are replaced with GND. There are a real open for GND_A in Figure 7(a) and a real short for GND_A and GND_B in Figure 7(b). However, these real errors are masked by the text replacement.

Multi-power-domain LVS is the second phase of the LVS flow, which targets verifying the integrity of the chip-level power grid. Unlike the standard-LVS,

AMD EX1021
AMD v. Realtek - Page 131

Table II. A Comparison of the Two LVS Runsets

Standard LVS Runset (runset 1)	Multi-power-domain LVS Runset (runset 2)
• VDD and GND are global nets	• VDD and GND are local nets
• Multi-power-domain power and ground names labeled at the bumps are replaced to VDD or GND	• Original multi-power-domain power and ground names labeled at the bumps are declared as global

in which VDD and GND are treated as global names, multi-power-domain LVS analyzes power and ground nets as local nets. A netlist parser is implemented to create a schematic netlist with localized VDD and GND nets, and also the multi-power-domain power and ground names are added as ports at the appropriate level of netlist hierarchy based on the information provided in a configuration file. As listed in Table II, where the major differences in the two LVS runsets are highlighted, the global net definition of VDD and GND are removed in LVS runset_2; VDD and GND nets are now local just like other signal nets. The actual multi-power-domain power and ground names labeled at the bumps are used in the second phase LVS. Hence, any opens or shorts on the power-grid will be reported upon completing the multi-power-domain LVS verification.

6. SUMMARY

Due to the importance of the stringent time-to-market demand, design reuse has become a common practice in today's IC industry. Part of the BCM1280 chip, including the microprocessor cores, is migrated from the previous design. Under this circumstance, our LVS strategy was designed to use two phases. A standard LVS phase is for a complete LVS verification at the block-level and a partial LVS verification at the chip top-level, while a multiple-power-domain LVS phase serves to verify the integrity of the power grid that is not covered by the standard-LVS phase.

The proposed two-stage LVS methodology allows us to fully verify the entire chip with minimum changes to reused design data. The price we pay is to have two LVS runs before the tapeout and to manipulate the full-chip netlist to localize power and ground nets for the second LVS run. Theoretically, it is sufficient at the full-chip level to run only the multi-power-domain LVS to completely verify the chip, however, we find it useful in practice to run both LVS runs. When VDD and GND nets are treated as local nets in the multi-power-domain LVS verification, while they are physically designed as global nets, it would be very difficult for LVS debug. The standard-LVS run at the chip level is useful to debug LVS problems before the chip is fully LVS clean. In the future projects, it is likely that multiple-power-domain application will become our standard design flow. If this trend is to become a reality, we will need to design VDD and GND as local nets by texting them in the layout at every LVS equivalency hierarchical level, and design the schematics accordingly using localized VDD and GND nets.

The LVS methodology we present in this article was successfully employed on implementing BCM1280, a high-end embedded four-core multiprocessor designed with multiple power domains. The proposed LVS flow is efficient in delivering the verification results before the tapeout and it is verified by real

AMD EX1021
AMD v. Realtek - Page 132

silicon. In laboratory tests, we are able to successfully shut off power to any of the four CPU cores. This enables the BCM1280 to be used in many different applications.

ACKNOWLEDGMENTS

The authors acknowledge the contributions of the whole BCM1280 design team at Broadcom Broadband Microprocessor group. We feel privileged to present this work. Special thanks to Susan Kwan for her efforts in implementing the layout and debugging the LVS.

REFERENCES

BROOKS, D. M., BOSE, P., SCHUSTER S. E., JACOBSON, H., KUDVA, P. N., BUYUKTOSUNOGLU, A., WELLMAN, J. D., ZYUBAN, V., GUPTA, M., AND COOK, P. W. 2000. Power-aware microarchitecture: Design and modeling challenges for next-generation microprocessors. *IEEE Micro 20*, 6, 22–44.

*HERCULES User's Reference Manua*l 2003. Synopsys Inc.

IYER, A. AND MARCULESCU, D. 2002. Microarchitecture-level power management. *IEEE Trans. VLSI Syst. 10*, 3, 230–239.

KAM, T., RAWAT, S., KIRKPATRICK, D., ROY, R., SPIRAKIS, G. S., SHERWANI, N., AND PETERSON, C. 2000. EDA challenges facing future microprocessor design. *IEEE Trans. Comput. Aid. Des. Integ. Circ. Syst. 19*, 12, 1498–1506.

KARNIK, T., BORKAR, S., AND DE, V. 2002. Sub-90nm technologies—Challenges and opportunities for CAD. In *Proceedings of IEEE International Conference on Computer Aided Design* (San Jose, CA, Nov.). IEEE Computer Society Press, Los Alamitos, CA, 203–206.

MOLL, L. 2004. The next-generation line of Broadcom's SiByte™ multiprocessor SoCs. In *Proceedings of the Fall Microprocessor Forum* (San Jose, CA, Oct.).

SANO, B. 2002. Chip combines four 1GHZ cores. In *Microprocessor Report*.

Received September 2004; revised May 2005; accepted December 2005

AMD EX1021
AMD v. Realtek - Page 133

ATTACHMENT 2A

```
001    99958480156126
005    20221206164827.0
006    m     o  d
007    cr cnu
008    970923c19969999nyuqr pso     0   a0eng c
010    ##$asn 98034796
016    7#$a1501152-5 $2DE-600
022    ##$a1557-7309
035    ##$a(OCoLC)37668393
035    ##$a(CKB)958480156126
035    ##$a(CONSER)sn 98034796
035    ##$a(DE-599)ZDB1501152-5
037    ##$bACM, 1515 Broadway, New York, NY 10036
042    ##$apcc $ansdp
050    10$aISSN RECORD
050    14$aTK7869 $b.A25
082    10$a004 $213
130    0#$aACM transactions on design automation of electronic
systems (Online)
222    #0$aACM transactions on design automation of electronic
systems $b(Online)
245    10$aACM transactions on design automation of electronic
systems $h[electronic resource].
260    ##$aNew York, NY : $bACM, $cc1996-
310    ##$aQuarterly
362    0#$aVol. 1, no. 1 (Jan. 1996)-
500    ##$aTitle from title screen.
588    ##$aLatest issue consulted: V. 10, issue 3 (July 2005)
(viewed Sept. 1, 2005).
500    ##$aRefereed/Peer-reviewed
650    #0$aElectronic systems $xDesign $xData processing
$vPeriodicals.
650    #0$aElectronic circuit design $xData processing
$vPeriodicals.
650    #0$aComputer-aided design $vPeriodicals.
650    #0$aIntegrated circuits $xDesign $xData processing
$vPeriodicals.
710    2#$aAssociation for Computing Machinery.
776    ##$x1084-4309
906    ##$aJOURNAL
```

ATTACHMENT 2B

OCLC 33041249 **No holdings in XXX - 396 other holdings**

Continuing Resources

Rec Stat		**Entered**	19950825	**Replaced**	20220403101955.6						
Type	a	**ELvl**		**Srce**	c	**GPub**		**Ctrl**		**Lang**	eng
BLvl	s	**Form**		**Conf**	0	**Freq**	q	**MRec**		**Ctry**	nyu
S/L	0	**Orig**		**EntW**		**Regl**	r	**Alph**	a		
Desc	a	**SrTp**	p	**Cont**		**DtSt**	c	**Dates**	1996	9999	

010 96640883 $z sn 95002109
040 NSD $b eng $c NSD $d DLC $d WAU $d EYM $d CAS $d WAU $d IUL $d HUL $d IUL $d SYS $d LYU $d IUL $d MUQ $d DLC $d OCL $d NSD $d NLGGC $d OCLCQ $d UKMGB $d OCLCO $d DEFHM $d OCLCO $d OCLCA $d COF $d OCLCA $d TYC $d UX0 $d NJR $d OCLCF $d OCL $d CLS $d OCL $d AU@ $d OCLCA $d CBA $d OCLCQ $d ZAS $d CPO $d OCLCQ $d UKBTH $d OCLCO $d OKS $d AAA $d OCLCO
012 $j 0 $l y $m 0
016 7 009184111 $2 Uk
016 7 a1268193. $2 Uk
019 289713393 $a 663109373 $a 995508134 $a 1012043178 $a 1013339845 $a 1016187193 $a 1052912926 $a 1053980091 $a 1057969261 $a 1065369387 $a 1071685765 $a 1080759887 $a 1127520035 $a 1141228699 $a 1155326597 $a 1156796207 $a 1156855915 $a 1159644583 $a 1161454170 $a 1202964957 $a 1204708459
022 0 1084-4309 $l 1084-4309 $y 0734-2071 $2 1
030 ATASFO
037 $b Association for Computing Machinery, 1515 Broadway, New York, NY 10036 $c $$150.00 (non-members)
042 nsdp $a pcc
050 00 TK7869 $b .A25
082 10 004 $2 12
090 $b
210 0 ACM transact. des. automat. electron. syst.
222 0 ACM transactions on design automation of electronic systems
245 00 ACM transactions on design automation of electronic systems.
246 30 Design automation of electronic systems
246 30 Transactions on design automation of electronic systems
246 3 Association for Computing Machinery transactions on design automation of electronic systems
246 13 TODAES
260 New York, NY : $b Association for Computing Machinery, $c ©1996-
300 volumes : $b illustrations ; $c 25 cm
310 Quarterly
336 text $b txt $2 rdacontent
337 unmediated $b n $2 rdamedia
338 volume $b nc $2 rdacarrier
362 0 Vol. 1, no. 1 (Jan. 1996)-
500 Title from cover.
530 Also issued in an annual CD-ROM.
588 1 Vol. 6, no. 3 (July 2001).

650 0 Electronic systems $x Design $x Data processing $v Periodicals.
650 0 Electronic circuit design $x Data processing $v Periodicals.
650 0 Computer-aided design $v Periodicals.
650 0 Integrated circuits $x Design $x Data processing $v Periodicals.
650 6 Circuits électroniques $0 (CaQQLa)201-0035975 $x Calcul $0 (CaQQLa)201-0035975 $x Informatique $0 (CaQQLa)201-0380011 $v Périodiques. $0 (CaQQLa)201-0378307
650 6 Conception assistée par ordinateur $0 (CaQQLa)201-0124858 $v Périodiques. $0 (CaQQLa)201-0378307
650 7 Computer-aided design. $2 fast $0 (OCoLC)fst00872701
650 7 Electronic circuit design $x Data processing. $2 fast $0 (OCoLC)fst00906866
650 7 Integrated circuits $x Design $x Data processing. $2 fast $0 (OCoLC)fst00975544
650 7 Integrierte Schaltung $2 gnd $0 (DE-588)4027242-4
650 7 Entwurfsautomation $2 gnd $0 (DE-588)4312536-0
650 7 Zeitschrift $2 gnd $0 (DE-588)4067488-5
650 17 Automatisering. $2 gtt
650 17 Ontwerpen. $2 gtt
655 0 Computer network resources.
655 7 Periodicals. $2 fast $0 (OCoLC)fst01411641
655 7 Computer network resources. $2 lcgft
710 2 Association for Computing Machinery.
776 1 $t ACM transactions on design automation of electronic systems (CD-ROM) $w (DLC)sn 97048292 $w (OCoLC)37382570
776 08 $i Online version: $t ACM transactions on design automation of electronic systems (Online) $x 1557-7309 $w (DLC)sn 98034796 $w (OCoLC)37668393
850 DLC $a InU $a MiU $a WaU
856 41 $u http://www.acm.org/todaes/ $z Subscription required for access except for pre-prints and the most current issues

ATTACHMENT 2C

LIBRARY OF CONGRESS AUTHORITIES

LC control no.: sh 85042373
LCCN Permalink: https://lccn.loc.gov/sh85042373
HEADING: Electronic systems

000 00473cz a2200193n 450
001 4694270
005 20120323072914.0
008 860211|| anannbabn |b ana
010 __ |**a** sh 85042373
035 __ |**a** (DLC)sh 85042373
035 __ |**a** (DLC)40955
040 __ |**a** DLC |**c** DLC
053 _0 |**a** TK7870
150 __ |**a** Electronic systems
450 __ |**a** Systems, Electronic
550 __ |**w** g |**a** Electronic apparatus and appliances
550 __ |**w** g |**a** Electronics
906 __ |**t** 7932 |**u** fk07 |**v** 0
953 __ |**a** xx00

Previous Next

Save, Print or Email Records (View Help)

Select Download Format: Text (Labelled Display) Press to SAVE or PRINT

Email Text (Labelled Display) to: Press to SEND EMAIL



Library of Congress
URL: https://www.loc.gov/

Mailing Address:
101 Independence Ave, S.E.

Library of Congress Authorities
URL: http://authorities.loc.gov/
Library of Congress Online Catalog
URL: https://catalog.loc.gov/

Questions, comments, error reports: Contact Us

AMD EX1021
AMD v. Realtek - Page 140

Washington, DC 20540

ATTACHMENT 2D

LIBRARY OF CONGRESS AUTHORITIES

LC control no.: sh 85037197
LCCN Permalink: https://lccn.loc.gov/sh85037197
HEADING: Design

000 00646cz a2200217n 450
001 4689249
005 20120323072116.0
008 860211i| anannbabn |b ana
010 __ |**a** sh 85037197
035 __ |**a** (DLC)sh 85037197
035 __ |**a** (DLC)7125547
035 __ |**a** (DLC)sp 85037197
035 __ |**a** (DLC)356362
040 __ |**a** DLC |**c** DLC |**d** DLC
053 _0 |**a** NC703 |**c** Drawing
053 _0 |**a** NK1160 |**b** NK1590 |**c** Decoration
150 __ |**a** Design
360 __ |**i** subdivision |**a** Design |**i** under topical headings where the subdivision |**a** Design and construction |**i** is not appropriate
550 __ |**w** g |**a** Creation (Literary, artistic, etc.)
906 __ |**t** 0714 |**u** te04 |**v** 1
953 __ |**a** xx00 |**b** lg14

Previous Next

Save, Print or Email Records (View Help)

Select Download Format: Text (Labelled Display) Press to SAVE or PRINT

Email Text (Labelled Display) to: Press to SEND EMAIL

Help - Search - Search History - Headings List - Start Over



URL: https://www.loc.gov/

Mailing Address:
101 Independence Ave, S.E.
Washington, DC 20540

URL: https://catalog.loc.gov/

Questions, comments, error reports: Contact Us

ATTACHMENT 2E

LIBRARY OF CONGRESS AUTHORITIES

LC control no.: sh 85035857

LCCN Permalink: https://lccn.loc.gov/sh85035857

HEADING: Data processing

000 00614cz a2200157n 450

001 4687964

005 20110729104259.0

008 860211n| cnannbbbn |n ann

010 __ |**a** sh 85035857

035 __ |**a** (DLC)sh 85035857

035 __ |**a** (DLC)34649

040 __ |**a** DLC |**c** DLC |**d** DLC

150 __ |**a** Data processing

260 __ |**i** subdivision |**a** Data processing |**i** under subjects for comprehensive works on the recording and handling of information about a subject by means of mechanical or electronic equipment, e.g. |**a** English language--Data processing; Universities and colleges--Data processing

906 __ |**t** 8729 |**u** fk07 |**v** 0

953 __ |**a** xx00 |**b** fj26

Save, Print or Email Records (View Help)

Select Download Format: Text (Labelled Display) Press to SAVE or PRINT

Email Text (Labelled Display) to:

Press to SEND EMAIL

Library of Congress
URL: https://www.loc.gov/

Mailing Address:
101 Independence Ave, S.E.

Library of Congress Authorities
URL: http://authorities.loc.gov/
Library of Congress Online Catalog
URL: https://catalog.loc.gov/

Questions, comments, error reports: Contact Us

AMD EX1021
AMD v. Realtek - Page 146

Washington, DC 20540

ATTACHMENT 2F

LC control no.: sh 85099890

LCCN Permalink: https://lccn.loc.gov/sh85099890

HEADING: Periodicals

000 01324cz a2200337n 450

001 4749694

005 20120717060125.0

008 860211 | anannbabn |b ana

010 __ |**a** sh 85099890

035 __ |**a** (DLC)sh 85099890

035 __ |**a** (DLC)6226910

035 __ |**a** (DLC)sp 85099890

035 __ |**a** (DLC)314952

040 __ |**a** DLC |**c** DLC |**d** DLC

053 _0 |**a** AP |**c** General periodicals

053 _0 |**a** PN4700 |**b** PN5650 |**c** History

150 __ |**a** Periodicals

360 __ |**i** subdivision |**a** Periodicals |**i** under specific subjects, e.g. |**a** Engineering--Periodicals; United States--History--Periodicals

450 __ |**a** Journals (Periodicals)

450 __ |**a** Magazines

550 __ |**w** g |**a** Library materials

550 __ |**w** g |**a** Mass media

550 __ |**w** g |**a** Serial publications

550 __ |**a** Newspapers

550 __ |**a** Press

670 __ |**a** UMI business vocab. |**b** (Journals)

680 __ |**i** Here are entered works on the periodicals of the world and, with appropriate subdivisions, works on special aspects or sections of periodicals. Works on periodicals in a specific language, or in a specific country or larger area, are entered under the adjectival form of the language or area, e.g. |**a** Arabic periodicals; Canadian periodicals.

906 __ |**t** 0420 |**u** te03 |**v** 0

910 __ |**a** Proposal saved by tc03 on 05/14/2012 at 17:15:30

953 __ |**a** xx00 |**b** td14

906 __ |**t** 1206 |**v** 0

Previous Next

Save, Print or Email Records (View Help)

Select Download Format: Text (Labelled Display) Press to SAVE or PRINT

Email Text (Labelled Display) to:

Press to SEND EMAIL

Help - Search - Search History - Headings List - Start Over



Library of Congress
URL: https://www.loc.gov/

Mailing Address:
101 Independence Ave, S.E.
Washington, DC 20540

Library of Congress Authorities
URL: http://authorities.loc.gov/
Library of Congress Online Catalog
URL: https://catalog.loc.gov/

Questions, comments, error reports: Contact Us

ATTACHMENT 2G

LC control no.: sh 85042278
LCCN Permalink: https://lccn.loc.gov/sh85042278
HEADING: Electronic circuit design Data processing

000 00352cz a2200145n 450
001 4694178
005 20110729104924.0
008 860211|| anannbabn |n ana
010 __ |**a** sh 85042278
035 __ |**a** (DLC)sh 85042278
035 __ |**a** (DLC)40863
040 __ |**a** DLC |**c** DLC
150 __ |**a** Electronic circuit design |**x** Data processing
906 __ |**t** 7650 |**u** ---- |**v** 0
953 __ |**a** xx00

◀ Previous Next ▶

Save, Print or Email Records (View Help)

Select Download Format: Text (Labelled Display) Press to SAVE or PRINT

Email Text (Labelled Display) to: Press to SEND EMAIL



Library of Congress
URL: https://www.loc.gov/

Mailing Address:
101 Independence Ave, S.E.
Washington, DC 20540

Library of Congress Authorities
URL: http://authorities.loc.gov/
Library of Congress Online Catalog
URL: https://catalog.loc.gov/

Questions, comments, error reports: Contact Us

ATTACHMENT 2H

LIBRARY OF CONGRESS AUTHORITIES

LC control no.: sh2009121170
LCCN Permalink: https://lccn.loc.gov/sh2009121170
HEADING: Computer-aided design Periodicals

000 00458cz a2200169n 450
001 7982632
005 20110729162415.0
008 090811|| anannbabn |n ana
010 __ |**a** sh2009121170
035 __ |**a** (DLC)434607
035 __ |**a** (DLC)sh2009121170
040 __ |**a** DLC |**b** eng |**c** DLC
150 __ |**a** Computer-aided design |**v** Periodicals
667 __ |**a** Record generated for validation purposes.
670 __ |**a** Work cat.: Key solutions, c1992-
906 __ |**t** 8888 |**u** tc00 |**v** 0
953 __ |**a** tc00

◀ Previous Next ▶

Save, Print or Email Records (View Help)

Select Download Format: Text (Labelled Display) Press to SAVE or PRINT

Email Text (Labelled Display) to: Press to SEND EMAIL

Library of Congress
URL: https://www.loc.gov/

Mailing Address:
101 Independence Ave, S.E.
Washington, DC 20540

Library of Congress Authorities
URL: http://authorities.loc.gov/
Library of Congress Online Catalog
URL: https://catalog.loc.gov/

Questions, comments, error reports: Contact Us

AMD EX1021
AMD v. Realtek - Page 154

ATTACHMENT 2I

LC control no.: sh 85067117

LCCN Permalink: https://lccn.loc.gov/sh85067117

HEADING: Integrated circuits

000 01925cz a2200325n 450

001 4718165

005 20190825060112.0

008 860211|| anannbabn |a ana

010 __ |**a** sh 85067117

035 __ |**a** (DLC)sh 85067117

035 __ |**a** (DLC)64850

040 __ |**a** DLC |**c** DLC |**d** DLC

150 __ |**a** Integrated circuits

450 __ |**a** Chips (Electronics)

450 __ |**a** Circuits, Integrated

450 __ |**a** Computer chips

450 __ |**a** Microchips

550 __ |**w** g |**a** Electronic circuits

550 __ |**w** g |**a** Microelectronics

670 __ |**a** UMI business vocab.

670 __ |**a** Science & technology encyclopedia, the University of Chicago Press, 1999: |**b** (Integrated circuit (IC); Complete miniature electronic circuit incorporating semiconductor devices such as the transistor and resistor. The components of a monolithic integrated circuit occupy the surface layers of a single crystal of silicon (commonly called a silicon chip). Hybrid integrated circuits have separate components attached on a ceramic base. Components in both types are joined by conducting film. Among their many uses, integrated circuits are found in pocket calculators and microcomputers)

680 __ |**i** Here are entered works on devices created by microlithographic etching and film deposition on silicon compounds. Works on electronic components manufactured by printing electrically functional inks, which are usually polymers, on a substrate are entered under |**a** Printed electronics. |**i** Works on printing conductive paths printed on a substrate onto which individual components are mounted are entered under |**a** Printed circuits.

681 __ |**i** Note under |**a** Printed electronics; Printed circuits

906 __ |**t** 9413 |**u** te04 |**v** 0

910 __ |**a** Record saved by td14 on 09/08/2016 at 14:52:47
910 __ |**a** Record saved by td14 on 09/08/2016 at 14:41:58
910 __ |**a** Proposal saved by tc03 on 03/03/2016 at 14:55:55
952 __ |**a** LC-BRF
953 __ |**a** xx00 |**b** se01
906 __ |**t** 1602 |**v** 1

Previous Next

Save, Print or Email Records (View Help)

Select Download Format: Text (Labelled Display) Press to SAVE or PRINT

Email Text (Labelled Display) to:
Press to SEND EMAIL

Help - Search - Search History - Headings List - Start Over



Library of Congress
URL: https://www.loc.gov/

Mailing Address:
101 Independence Ave, S.E.
Washington, DC 20540

Library of Congress Authorities
URL: http://authorities.loc.gov/
Library of Congress Online Catalog
URL: https://catalog.loc.gov/

Questions, comments, error reports: Contact Us

ATTACHMENT 3

© 2006 IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE.

IEEE Catalog Number: 06CH37820C
ISBN: 1-4244-9707-X
ISSN: 1063-6404

Table of Contents

IEEE International Conference on Computer Design (ICCD 2006)

Copyright iv
Welcome Letter xii
Organizing Committee xiv
Program Committee xv
Additional Reviewers xvii

Keynote Addresses

Computer Architecture in the Many-Core Era 1
Bill Dally, Stanford University

Scaling Manufacturability Software to Thousands of Processors 2
Fabio Angelillis, Synopsys Inc.

~~~ Session 1 ~~~

Session 1.1 Microarchitecture Optimization

Chair: Tejas Karkhanis, AMD

Long-term Performance Bottleneck Analysis and Prediction 3
Fei Gao and Suleyman Sair

Dynamic Code Value Specialization Using the Trace Cache Fill Unit 10
Weifeng Zhang, Steve Checkoway, Bradley Calder and Dean Tullsen

Fast, Performance-Optimized Partial Match Address Compression for Low-Latency On-Chip Address Buses 17
Jiangjiang Liu, Krishnan Sundaresan and Nihar Mahapatra

Joint Performance Improvement and Error Tolerance for Memory Design Based on Soft Indexing 25
Shuo Wang and Lei Wang

A Low Power Highly Associative Cache for Embedded Systems 31
Chuanjun Zhang

Session 1.2 Timing Analysis

Chair: Florentin Dartu, Synopsys

On the Improvement of Statistical Timing Analysis 37
Rajesh Garg, Nikhil Jayakumar and Sunil Khatri

FA-STAC: A Framework for Fast and Accurate Static Timing Analysis with Coupling 43
Debasish Das, Ahmed Shebaita, Hai Zhou, Yehea Ismail and Kip Killpack

Reduction of Crosstalk Pessimism using Tendency Graph Approach 50
Murthy Palla, Klaus Koch, Jens Bargfrede, Manfred Glesner and Walter Anheier

Statistical Analysis of Power Grid Networks Considering Lognormal Leakage Current Variations with Spatial Correlation 56
Ning Mi, Jeffrey Fan and Sheldon Tan

Session 1.3 Advanced Circuits and Interconnections

Chair: Srinivas Raghvendra, Synopsys

RasP: An Area-efficient, On-chip Network 63
Simon Hollis and Simon W. Moore

Quantitative Prediction of On-chip Capacitive and Inductive Crosstalk Noise and Discussion on Wire Cross-Sectional Area Toward Inductive Crosstalk Free Interconnects 70
Yasuhiro Ogasahara, Masanori Hashimoto and Takao Onoye

CMOS Comparators for High-Speed and Low-Power Applications 76
Eric Menendez, Dumezie Maduike, Rajesh Garg and Sunil Khatri

A Reconfigurable CAM Architecture for Network Search Engines 82
Mehrdad Nourani, Deepak Vijayasarathi and Poras Balsara

Delay and Area Efficient First-level Cache Soft Error Detection and Correction 88
Karl Mohr and Lawrence Clark

~~~ Session 2 ~~~

Session 2 Special Session on Nano Technology (I)

Chair: Pranav Ashar, Real Intent Inc.

Automated Design of Microfluidics-Based Biochips: Connecting Biochemistry to Electronics CAD 93
Krishnendu Chakrabarty

~~~ Session 3 ~~~

Session 3.1 Technology-Aware Design

Chair: Suleyman Sair, North Carolina State University

Fast Speculative Address Generation and Way Caching for Reducing L1 Data Cache Energy 101
Dan Nicolaescu, Babak Salamat, Alex Veidenbaum and Mateo Valero

Customizable Fault Tolerant Caches for Embedded Processors 108
Subramanian Ramaswamy and Sudhakar Yalamanchili

Reduce Register Files Leakage Through Discharging Cells 114
Lingling Jin, Wei Wu, Jun Yang, Chuanjun Zhang and Youtao Zhang

Efficient Transient-Fault Tolerance for Multithreaded Processors using Dual-Thread Execution 120
Yi Ma and Huiyang Zhou

Session 3.2 Multiprocessors and Systems-on-Chip

Chair: Huiyang Zhou, University of Central Florida

Dynamic Co-Processor Architecture for Software Acceleration on CSoCs 127
Abhishek Mitra, Zhi Guo, Anirban Banerjee and Walid Najjar

Polaris: A System-Level Roadmap for On-Chip Interconnection Networks 134
Vassos Soteriou, Noel Eisley, Hangsheng Wang, Bin Li and Li-Shiuan Peh

A Performance and Power Analysis of WK-Recursive and Mesh Networks for Network-on-Chips 142
Dara Rahmati, Abbas Eslami Kiasari, Shaahin Hessabi and Hamid Sarbazi-Azad

Perceptron Based Consumer Prediction in Shared-Memory Multiprocessors 148
Sean Leventhal and Manoj Franklin

Session 3.3 Robust and Low-Power Design Styles

Chair: Larry Clark, Arizona State University

A Design Approach for Fine-grained Run-Time Power Gating using Locally Extracted Sleep Signals 155
Kimiyoshi Usami and Naoaki Ohkubo

Design Methodology of Regular Logic Bricks for Robust Integrated Circuits 162
Kim Yaw Tong and Lawrence Pileggi

An Active Decoupling Capacitance Circuit for Inductive Noise Suppression in Power Supply Networks 168
Sanjay Pant and David Blaauw

Implementing Tile-based Chip Multiprocessors with GALS Clocking Styles 174
Zhiyi Yu and Bevan Baas

~~~ Session 4 ~~~

Session 4 Special Session on Interconnect

Chair: Kee Sup Kim, Intel

Scale in Chip Interconnect requires Network Technology 180
Enno Wein

Interconnect Considerations For High Performance Network on Chip Designs 187
Uri Cummings

Addressing Multicore Communication Challenges Using NoC Technology 188
Drew Wingard

~~~ Session 5 ~~~

Session 5.1 Hardware and Software Scheduling Techniques

Chair: Jiangjiang Liu, Lamar University

Clustering-Based Microcode Compression 189
Edson Borin, Mauricio Breternitz Jr., Youfeng Wu and Guido Araujo

Improving Scalability and Complexity of Dynamic Scheduler through Wakeup-Based Scheduling 197
Kuo-Su Hsiao and Chung-Ho Chen

An Enhancement for a Scheduling Logic Pipelined over two Cycles 203
Ruben Gran, Enric Morancho, Angel Olive and Jose M. Llaberia

Session 5.2 Nanoscale Modeling + Synthesis

Chair: Azita Emami, Columbia University

Steady and Transient State Analysis of Gate Leakage Current in Nanoscale CMOS Logic Gates 210
Saraju Mohanty and Elias Kougianos

Efficient Transistor-Level Sizing Technique under Temporal Performance Degradation due to NBTI 216
Kunhyuk Kang, Haldun Kufluoglu, Muhammad Ashraful Alam and Kaushik Roy

Interconnect Matching Design Rule Inferring and Optimization through Correlation Extraction..... 222
Andrew Kahng and Rasit Topaloglu

Session 5.3 Power Issues in Test

Chair: Rob Aitken, ARM

Power-Constrained SOC Test Schedules through Utilization of Functional Buses..... 230
Fawnizu Azmadi Hussin, Tomokazu Yoneda, Alex Orailoglu and Hideo Fujiwara

RTL Scan Design for Skewed-Load At-speed Test under Power Constraints..... 237
Ho Fai Ko and Nicola Nicolici

Power Droop Testing 243
Ilia Polian, Alejandro Czutro, Sandip Kundu and Bernd Becker

A Highly-Guided X-Filling Method for Effective Low-Capture-Power Scan Test Generation 251
Xiaoqing Wen, Kohei Miyase, Tatsuya Suzuki, Yuta Yamato, Seiji Kajihara, Laung-Terng Wang and Kewal Saluja

~~~ Session 6 ~~~

Session 6 Special Session on Hardware Equivalence

Chair: Carl Pixley, Synopsys

Scalable Sequential Equivalence Checking across Arbitrary Design Transformations 259
Jason Baumgartner, Hari Mony, Viresh Paruthi, Robert Kanzelman and Geert Janssen

Seqver : A Sequential Equivalence Verifier for Hardware Designs 267
Daher Kaiss, Silvian Goldenberg, Ziyad Hanna and Zurab Khasidashvili

High-Level vs. RTL Combinational Equivalence: An Introduction 274
Alan Hu

~~~ Session 7 ~~~

Session 7.1 Functional Verification---Advances and Applications

Chair: Jason Baumgartner, IBM

Implicit Search-Space Aware Cofactor Expansion: A Novel Preimage Computation Technique..... 280
Kameshwar Chandrasekar and Michael Hsiao

Requirements and Concepts for Transaction Level Assertions..... 286
Wolfgang Ecker, Volkan Esen, Michael Hull, Thomas Steininger and Michael Velten

Adding Debug Enhancements to Assertion Checkers for Hardware Emulation and Silicon Debug 294
Marc Boulé, Jean-Samuel Chenard and Zeljko Zilic

Simulation-based Functional Test Justification Using a Boolean Data Miner..... 300
Charles H.-P. Wen, Onur Guzey and Li-C. Wang

Session 7.2 Application Specific Processing Elements

Chair: Jamil Kawa, Synopsys

FPGA Implementation of High Speed FIR Filters Using Add and Shift Method 308
Shahnam Mirzaei, Anup Hosangadi and Ryan Kastner

FPGA-based Design of a Large Moduli Multiplier for Public-Key Cryptographic Systems 314
Osama Al-Khaleel, Chris Papachristou, Frank Wolff and Kiamal Pekmestzi

Split-Row: A Reduced Complexity, High Throughput LDPC Decoder Architecture 320
Tinoosh Mohsenin and Bevan Baas

An Efficient, Scalable Hardware Engine for Boolean SATisfiability 326
Mandar Waghmode, Kanupriya Gulati, Sunil Khatri and Weiping Shi

Session 7.3 Physical Design

Chair: Saurabh Adya, Synplicity

Power/Ground Supply Network Optimization for Power-Gating 332
Hailin Jiang and Malgorzata Marek-Sadowska

A Pattern Generation Technique for Maximizing Power Supply Currents 338
Kunal Ganeshpure, Alodeep Sanyal and Sandip Kundu

Partial Functional Manipulation Based Wirelength Minimization 344
Avijit Dutta and David Z. Pan

Iterative-Constructive Standard Cell Placer for High Speed and Low Power 350
Sungjae Kim and Eugene Shragowitz

~~~ Session 8 ~~~

Session 8.1 Design Techniques and Methods

Chair: Mauricio Breternitz Jr., Intel

Generic Architecture Description for Retargetable Compilation and Synthesis of Application-Specific Pipelined IPs 356
Bita Gorjiara, Mehrdad Reshadi and Daniel Gajski

Assertion-Based Microarchitecture Design for Improved Fault Tolerance 362
Vimal Reddy, Ahmed Al-Zawawi and Eric Rotenberg

High-Speed Factorization Architecture for Soft-Decision Reed-Solomon Decoding 370
Xinmiao Zhang

Session 8.2 System On Chip Design

Chair: Roozbeh Jafari, UC Berkeley

Guiding Architectural SRAM Models 376
Banit Agrawal and Timothy Sherwood

A System-level Network-on-Chip Simulation Framework Integrated with Low-level Analytical Models 383
Jinwen Xi and Peixin Zhong

Reliability Support for On-Chip Memories Using Networks-on-Chip 389
Federico Angiolini, David Atienza, Srinivasan Murali, Luca Benini and Giovanni De Micheli

Task Merging for Dynamic Power Management of Cyclic Applications in Real-Time Multiprocessor Systems 397
Qinru Qiu, Shaobo Liu and Qing Wu

Session 8.3 Power-Efficient Systems

Chair: Dan Sorin, Duke University

A Capacity Co-allocation Configurable Cache for Low Power Embedded Systems 405
Chuanjun Zhang

System-Level Energy Modeling for Heterogeneous Reconfigurable Chip Multiprocessors 411
Xiaofang Wang, Sotirios Ziavras and Jie Hu

Improving Power and Data Efficiency with Threaded Memory Modules 417
Frederick A. Ware and Craig Hampel

~~~ Session 9 ~~~

Session 9.1 Improving Test Quality

Chair: Yervant Zorian, Virage Logic Corp.

A New Class of Sequential Circuits with Acyclic Test Generation Complexity 425
Chia Yee Ooi and Hideo Fujiwara

Efficient Testing of RF MIMO Transceivers Used in WLAN Applications 432
Erkan Acar and Sule Ozev

A Theory of Error-Rate Testing 438
Shideh Shahidi and Sandeep Gupta

Generating Compact Robust and Non-Robust Tests for Complete Coverage of Path Delay Faults Based on Stuck-at Tests 446
Dong Xiang, Kaiwei Li, Hideo Fujiwara and Jiaguang Sun

Session 9.2 Architectural Synthesis

Chair: Anup Hosangadi, Cadence

Stochastic Dynamic Thermal Management: A Markovian Decision-based Approach 452
Hwisung Jung and Massoud Pedram

Design and Implementation of Software Objects in Hardware 458
Fu-Chiung Cheng and Hung-Chi Wu

An Accurate Energy Estimation Framework for VLIW Processor Cores 464
Sourav Roy, Rajat Bhatia and Ashish Mathur

~~~ Session 10 ~~~

Session 10.1 Design Practice

Chair: Steve Keckler, University of Texas at Austin

Design and Implementation of the TRIPS Primary Memory System 470
Simha Sethumadhavan, Robert McDonald, Rajagopalan Desikan, Doug Burger and Steve Keckler

Implementation and Evaluation of On-Chip Network Architectures 477
Paul Gratz, Changkyu Kim, Robert McDonald, Steve Keckler and Doug Burger

Microarchitecture and Performance Analysis of Godson-2 SMT Processor 485
Zusong Li, Xianchao Xu, Weiwu Hu and Zhimin Tang

Patching Processor Design Errors 491
Satish Narayanasamy, Bruce Carneal and Brad Calder

Session 10.2 Architectural Support for Error Protection

Chair: Eric Rotenberg, NC State University

Choosing an Error Protection Scheme for a Microprocessor's L1 Data Cache 499
Nathan Sadler and Daniel Sorin

Architectural Support for Run-Time Validation of Control Flow Transfer 506
Yixin Shi, Sean Dempsey and Gyungho Lee

Pesticide: Using SMT Processors to Improve Performance of Pointer-Bug Detection 514
Jin-Yi Wang, Yen-Shiang Shue, T N Vijaykumar and Saurabh Bagchi

~~~ Session 11 ~~~

Session 11 Special Session on Nanotechnology (II)

Chair: Pranav Ashar, Real Intent Inc.

Trends and Future Directions in Nano Structure Based Computing and Fabrication 522
R. Iris Bahar

Author Index 528

This material may be protected by Copyright law (Title 17 U.S. Code)

Power/Ground Supply Network Optimization for Power-Gating

Hailin Jiang
ECE Department, UCSB
hailin@ece.ucsb.edu

Malgorzata Marek-Sadowska
ECE Department, UCSB
mms@ece.ucsb.edu

***Abstract* -- Power-gating is a technique for efficiently reducing leakage power by shutting off the idle blocks. However, the presence of power-gating may also introduce negative effects on power supply network, which have not been considered in the earlier design stages. Ignoring those effects may result in suboptimal power supply network designs and could potentially even nullify the intended power savings. In this paper, we analyze mutual dependencies between the sleep transistors and the P/G network, and we present a general flow to optimize the P/G supply network for power-gating. Experimental results show that sizing sleep transistor and power network separately cannot achieve optimal solution in terms of power. By compromising only 1% of the total area, our optimization method allows us to save 10% of power dissipated on decaps and sleep transistors, which is a practical solution for a power-gated system. We also report results of a study on optimal solutions for various gated areas and current densities.**

***Index Terms* -- Power gating, power/ground network, decap, sleep transistor, optimization.**

I. INTRODUCTION

Due to continuous shrinking of the minimal feature size, lowering of supply voltages, and lowering of threshold voltages, leakage power is emerging as a major challenge for current and future CMOS designs. Power-gating is an efficient technique for reducing leakage power by shutting off the idle blocks. Implementation of power-gating requires a multi-threshold CMOS process. Logic blocks are implemented using low-V_t, high-performance transistors, whereas high-V_t transistors (also called sleep transistors) connect the gated blocks to the power supply [6].

However, the power-gating is not without cost. In [4], the authors discuss and quantify the negative effects of power gating, which include noise, performance penalty, area and power overhead, etc. Recently, research efforts have been made in the physical design stage to reduce some of these negative effects. In [1], the authors propose a novel gating structure in which the sleep transistors are turned on in a non-uniform, step-wise manner to reduce the magnitude of the voltage fluctuations. In [5], the authors propose two clustering algorithms based on bin-packing and set-partitioning techniques for centralized sleep-transistor sizing, which improve the chip area and performance.

However, all those works have been done assuming that the power supply network had already been designed. There is no mention that the global power supply grid requires any special considerations related to power gating. Designing the global grid giving no consideration to power gating causes two problems. First, introducing power-gating to an existing grid causes a new power grid noise originating from the switching of sleep transistors. At the same time, gated macros shield the decap effect from the gated circuit and hinder the decap insertion in that area. Thus the power supply network should be appropriately redesigned to be immune to the gating noise. Second, the traditional P/G network optimization performs wire sizing and decoupling capacitor insertion [7][9] targeting at minimizing the total area. However, when power-gating is implemented, sleep transistors will consume power and more decaps will cause more dissipated leakage power, especially in more advanced technologies. If the power delivery network and sleep transistors are designed in such a way that their extra costs nullify the power savings, the power-gating technique becomes useless. Because of the mutual dependencies between the sleep transistors and the P/G network, we have to consider them together to achieve an optimal solution in terms of power. In this work, we present a general algorithm to optimize the power/ground supply network for power-gating. To the best of our knowledge, our work is the first one that addresses this problem.

The remainder of the paper is organized as follows. In section II, we point out the problems introduced by power-gating in the context of P/G network. In section III, we address the co-design of the sleep transistors and of the P/G network. In section IV, we present our method for optimizing the P/G network for power-gating. In section V we show the experimental results. Section VI summarizes our conclusions and suggests practical uses for the results.

II. ANALYSIS OF P/G NETWORK DESIGN WITH POWER-GATING

Traditionally, the on-chip power distribution network is constructed hierarchically. Power is delivered from the top-level metal layer (which is connected to the package), down through the internal layers, and finally to the active device. The entire chip is fully powered at all times. In a power-gating system, a circuit is divided into several power domains. Each domain is independently controlled by a sleep-transistor. The sleep transistors are turned off to reduce the dynamic power and leakage power in a standby mode, and turned on in an active mode for normal operation.

Power/ground network is traditionally optimized by wire width sizing and decap insertion, with an objective of minimizing the total area under the IR drop and electrical migration constraints. However, when power-gating is applied on a power supply network, the new technique will introduce extra effects which did not exist before but which should be considered now.

1-4244-9707-X/06/$20.00 ©2006 IEEE

First, the sleep transistor needs to be carefully designed. Its size must be sufficient to guarantee that the current drawn by a macro does not cause an excessive voltage drop on a sleep transistor which is turned on. However, when large-size sleep transistors are turned on and off, considerable power supply currents are drawn in a short period of time, which may result in large voltage fluctuations on the power grid. This *power-gating noise (PGN)* affects the reliability of systems-on-chips (SoCs), especially for advanced CMOS technologies with narrow noise margins. We need to add extra decap to reduce the *PGN* and take into account the additional leakage currents associated with the intentionally introduced capacitors.

Second, in the power-gating system, the gated macros are disconnected from the power supply in their idle state, which prevents them from acting as decaps for the active circuits. Thus the non-gated macros adjacent to the gated circuitry may need extra decap to guarantee that power grid noise remains within tolerable margins. The gated macros not only stop providing decap to other macros, but also act as an obstacle for decap insertion. Extra decap will enlarge the chip size and again consume more leakage power.

So without taking these effects into account, the power supply network will not be robust enough to tolerate noise and needs to be redesigned. Now, the question is, should we design a P/G network with power-gating in one shot? Is the co-design of sleep transistors and P/G network necessary? In the following section, we will discuss the mutual dependencies between the sleep transistor design and P/G network design to answer these questions.

III. CAN THE SLEEP TRANSISTOR AND P/G NETWORK DESIGN BE DECOUPLED?

The most straightforward approach to design a robust P/G network with power-gating is to size the sleep transistors first, and then optimize the P/G network. This approach works to achieve the minimal total area consumed by the sleep transistors, decaps, and power mesh. This is so because the smaller sleep transistors will cause less noise, thus requiring fewer resources to counteract it. All the sizings go in the same direction. We can first minimize the total area of sleep transistor under the performance constraint (i.e. the maximal voltage drop across on the sleep transistor), then optimize the P/G network by wire-sizing and insert decap based on the given size of sleep transistors.

However, the purpose of introducing power-gating is to save power. If the cost of power overhead caused by power gating is greater than the savings it provides, power-gating is useless. So the task we face is how to minimize the power consumption caused by power-gating. We have observed a mutual dependency in terms of power between the sleep transistors' sizes and decap. When we decrease the sleep transistors' sizes, the switching noise on the power grid decreases, which calls for less decap and in turn less dissipated leakage power. However, smaller size transistors have larger resistance, which increases the IR drop across them, which increases the power consumed. So the simple approach outlined at the beginning of this section cannot guarantee the minimal power consumption. Optimizing the area would make no sense because it could erode the potential power saving. Moreover, because of the mutual dependency, the designs of sleep transistors and P/G networks cannot be decoupled. We need to find the trade-off between sleep transistors and decap to achieve the optimal solution in terms of power.

In this work, we present a general flow to optimize a P/G network with power-gating. Through this flow, we can achieve an optimal solution in terms of either area or power consumption. More generally, by adjusting the weighting parameters, we can determine the best trade-off between area and power, depending on design requirements.

IV. P/G NETWORK OPTIMIZATION CONSIDERING POWER-GATING

A. Modeling

a) Power-gating.

The power-gating model is shown in Fig.1. The upper power mesh can be modeled as a linear resistive network excited by constant voltage sources (we ignore the package inductance in this work). The lower power mesh is composed of a linear RC network excited by time-varying current sources which represent the switching currents drawn by the logic circuits. We use a simple triangular waveform to model the current profiles. C denotes decap from the on-chip non-switching capacitors C_{ckt} and/or purposely inserted oxide capacitors C_{ox}.

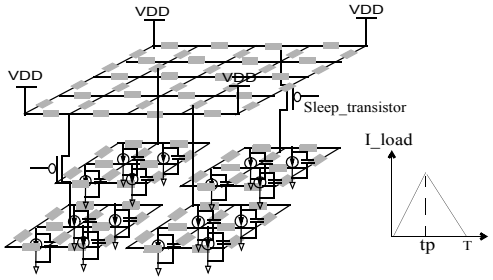


Fig. 1. Power gating modeling

b) Sleep transistor.

The model we use for the sleep transistor depends on its region of operation, see Fig.2. When the sleep transistor is switching, it works in the saturation region. In the saturation stage, the sleep transistor can be modeled as a current source with a triangle waveform. The peak current is expressed by Sakurai's alpha-power-law [8] formula:

$$I_D = \frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS}-V_{th})^{\alpha} \quad (1)$$

where α is the velocity saturation index for modeling the short channel effects. It is close to one in modern deep submicron devices. We define the switching period as twice the falling time of the signal V_G: $t_2 - t_1 = t_1 - t_0$. (Refer to Fig.2 for definitions of t_0, t_1 and t_2.) When a gated macro is active, the sleep transistor which controls it works in the linear region and can be modeled as a resistor:

$$I_{ST} \approx \mu_p C_{ox}\left(\frac{W}{L}\right)(V_{dd} - V_{tH})V_{DS} \quad (2)$$

$$R_{ST} = \frac{1}{\mu_p C_{ox}(V_{dd} - V_{tH})}\left(\frac{L}{W}\right) \quad (3)$$

where I_{ST} is the switching current of the logic block, V_{tH} is the threshold voltage of the sleep transistor, and R_{ST} is the channel resistance of the sleep transistor in the linear operation region.

We know that voltage drop on a sleep transistor will degrade the chip's performance. We define the allowable performance loss (PL) as:

$$\delta = 1 - T_d / T_d^{ST} \quad (4)$$

where T_d is the delay of the circuit when sleep transistors are absent, and T_d^{ST} is the delay of the circuit when sleep transistors are present. From [5] we know that:

$$MAX(V_{ST}) = \delta(V_{dd} - V_{tL}) \quad (5)$$

$$MIN\left(\frac{W}{L}\right)_{ST} = \frac{I_{MAX}}{\delta\mu_p C_{ox}(V_{dd} - V_{tL})(V_{dd} - V_{tH})} \quad (6)$$

where I_{MAX} is the peak current of I_{ST} and V_{tL} is the threshold voltage of the gate in logic blocks. This formula indicates the lower bound of sleep transistor size.

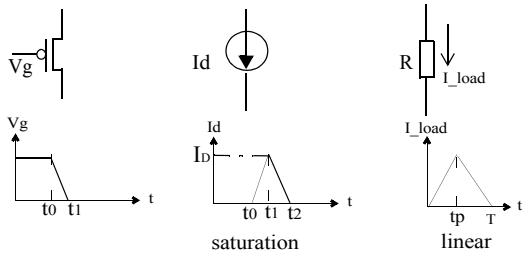


Fig. 2. Sleep transistor modeling

The model of sleep transistor in a saturation region will be used for noise analysis, and the model of sleep transistor in a linear region will be used for power estimation in our objective function. Note that the power consumption should also include the dynamic power consumed by the sleep transistors during the switching period. However, if the gating period is long enough, that part of power is relatively small and can be ignored in the objective function.

c) Power grid noise

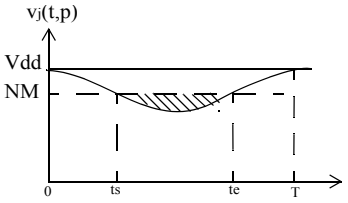


Fig. 3. Noise at typical grid node

To estimate the power grid induced noise at a node, we use the following efficient formulation [7]:

$$z_j(p) = \int_0^T max\{NM - v_j(t,p), 0\}\,dt = \int_{t_s}^{t_e} \{NM - v_j(t,p)\}\,dt \quad (7)$$

where p is the tunable circuit parameter and NM is the noise margin. This integral expression represents the shaded area in Fig.3. For the whole circuit, we have

$$Z = \sum_{j=1}^{N} z_j(p) \quad (8)$$

where N is the number of nodes whose noise goes beyond the margin. This metric is a summation of the integrals of the noise violations, which is zero if all constraints are satisfied.

B. Problem formulation

The optimization of P/G network with power-gating can be formulated as:

Objective: $MIN[\alpha \cdot Area + (1-\alpha)\cdot\beta\cdot Power]$

where

$$Area = \sum_{i=1}^{I} l_{Ti} w_{Ti} + \sum_{j=1}^{J} A_{Cj} + \sum_{k=1}^{K} l_{Rk} w_{Rk}$$

$$Power = \sum_{i=1}^{I} (I_i^{max})^2 \cdot R_{Ti} + \sum_{j=1}^{J} P_{unit} \cdot A_{Cj}$$

Subject to:

$$w_{Ti}^{min} \le w_{Ti} \le w_{Ti}^{max} \qquad i = 1, 2 \ldots I$$

$$0 \le A_{Cj} \le A_{Cj}^{max} \qquad j = 1, 2 \ldots J$$

$$w_{Rk}^{min} \le w_{Rk} \le w_{Rk}^{max} \qquad k = 1, 2 \ldots K$$

$$\text{and} \quad Z(w) < \varepsilon \quad (9)$$

where β is a scaling factor to make the two terms in the objective function of the same magnitude. w_{Ti} denotes width of the i-th transistor, w_{Rk} is the width of the k-th wire in the grid, and A_{Cj} is the area of the j-th inserted decap C_{ox}. These are the variables we need to adjust. l_T is the length of a sleep transistor and l_R denotes the length of a wire segment. w_{Ti}^{min} is the lower bound of the size on an i-th sleep transistor, which is determined based on Eq.(6). Other bounds are determined by the design. r_T is the resistance of a sleep transistor, which is defined in Eq.(3). I^{max} is the peak current of the current drawn from the gated blocks and P_{unit} is the leakage power per unit area of decap. Z is defined in Eq.(8) and ε is a very small number.

α is a weight factor to trade off between area and power; its range is between 0 and 1. If we set $\alpha = 1$, we simultaneously size the wire segments, decap, and sleep transistors to achieve the minimal area under noise constraint. As we discussed in section III, the result should be the same as that obtained from sizing the sleep transistor first, followed by P/G network optimization. If we set $\alpha = 0$, we can size the sleep transistor and decap to achieve the optimal power for the initial power mesh. α can be adjusted depending on design requirement. Experiments show that the grid power consumption constitutes only 5% of the combined decaps and sleep transistors power consumption, so we do not include the grid power in the formula.

This is a non-linear problem with non-linear objective and constraint functions. We can apply a standard sequence-of-quadratic-programs (SQP) [3] to solve this optimization problem. The calculation of objective function and its derivatives with respect to each decision variable is straightforward. The evaluation of constraint function Z can be done by HSPICE simulation. We use adjoint sensitivity analysis [2] to calculate the derivatives of Z with respect to varying parameters. In the following sub-section we discuss this point in more detail.

C. Sensitivity calculation

The adjoint-network-based sensitivity analysis is a standard technique for circuit optimization used when sensitivities of the cost function with respect to many parameter values are required. In [7] the authors use this method to find the optimal solution for decap sizing and placement.

The basic idea of the adjoint sensitivity analysis is as follows. By applying Tellegen's theorem, we have

$$\int_0^T \sum_V [\hat{v}_V\, \delta i_V - \hat{i}_V\, \delta v_V]\, dt + \int_0^T \sum_I [\hat{v}_I\, \delta i_I - \hat{i}_I\, \delta v_I]\, dt = \int_0^T \sum_{NS} [\hat{i}_{NS}\, \delta v_{NS} - \hat{v}_{NS}\, \delta i_{NS}]\, dt \tag{10}$$

where v and i represent the vectors of branch voltages and currents in the original network N, and where $\hat{v}$ and $\hat{i}$ represent the branch voltages and currents in the adjoint network $\hat{N}$. The networks N and $\hat{N}$ have the same topology; both satisfy the Kirhchoff's current (KCL) and voltage (KVL) laws. V denotes the terms corresponding to voltage sources; I denotes the terms corresponding to the current sources; NS denotes the terms corresponding to branches with no sources.

All the interesting performance metrics (power, delay, voltage, etc.) can be expressed with the following general formula:

$$\Phi = \int_0^T f(v_I, i_V)\, dt \tag{11}$$

whose variation is:

$$\delta\Phi = \int_0^T \left[\sum_V \frac{\partial f}{\partial v_I} \delta v_I + \sum_I \frac{\partial f}{\partial i_V} \delta i_V \right] dt \tag{12}$$

So, for a given performance function Φ, the excitations $\hat{v}_V$ and $\hat{i}_I$ in adjoint network can be chosen so as to make the left-hand side of Eq.(10) equal to the performance variation $\delta\Phi$. Since the choice of the element types in the adjoint circuit is arbitrary, they can be chosen so as to cancel the terms depending on δi_{NS} or δv_{NS} in the right-hand side of Eq.(10) leaving only the terms depending on parameter variation.

In the original network we attach a zero valued current source to those nodes which do not tap to any source (either voltage or current). Z is then the function of v_I:

$$Z = \sum_{j=1}^{N} \int_{t_s}^{t_e} \{NM - v_I^j(t)\}\, dt \tag{13}$$

Then the variation of Z can be expressed as:

$$\delta Z = \sum_{j=1}^{N} \int_{t_s}^{t_e} \frac{\partial f}{\partial v_{Ij}} \delta v_{Ij}\, dt = \sum_{j=1}^{N} [u(t-t_e) - u(t-t_s)] \cdot \delta v_{Ij} \tag{14}$$

We assign the adjoint circuit excitations such that:

$$\hat{i}_I = \frac{\partial f}{\partial v_I} = u(t-t_f) - u(t-t_0), \qquad \hat{v}_V = \frac{\partial f}{\partial i_V} = 0$$

Then the Eq.(10) is rewritten as:

$$-\delta Z + \int_0^T \sum_I \hat{v}_I\, \delta i_I\, dt - \int_0^T \sum_V \hat{i}_V\, \delta v_V\, dt = \int_0^T \sum_{NS} [\hat{i}_{NS}\, \delta v_{NS} - \hat{v}_{NS}\, \delta i_{NS}]\, dt \tag{15}$$

The voltage sources are constant, so $\delta v_V = 0$. Unlike in [7], we need to adjust the sleep transistor which is modeled as a current source in the original network. That means i_I is a varying parameter and $\delta i_I \neq 0$. Eq.(15) becomes:

$$\delta Z = \int_0^T \sum_{NS} [\hat{v}_N\, \delta i_N - \hat{i}_N\, \delta v_N]\, dt + \int_0^T \sum_I \hat{v}_I\, \delta i_I\, dt \tag{16}$$

From [2], we know that if the corresponding R(C) branches of the adjoint and original networks are the same, the first term on the right-hand side of Eq.(16) depends only on parameter variation, which can be stated as:

$$\delta Z = \sum_G \left[\int_0^T \hat{v}_G(\tau)\, v_G(t)\, dt \right] \cdot \delta G + \sum_C \left[\int_0^T \hat{v}_C(\tau)\, \dot{v}_C(t)\, dt \right] \cdot \delta C + \sum_I \left[\int_0^T \hat{v}_I\, dt \right] \cdot \delta i_I \tag{17}$$

We have: $G = \frac{w_R}{\rho \cdot l_R}$, $C = C_0 + \frac{\varepsilon_{ox}}{T_{ox}} \cdot A_C$ and

$$I = \frac{\mu_p C_{ox}}{2} \left(\frac{w_T}{l_T} \right) (V_{Gs} - V_{th}) = \lambda \cdot w_T$$

where C_0 is the capacitance of the on-chip decap. By applying chain rules, we finally get:

$$\delta Z = \sum_G \left[\int_0^T \hat{v}_G(\tau)\, v_G(t)\, dt \right] \cdot \frac{1}{\rho \cdot l_R} \cdot \delta w_R + \sum_C \left[\int_0^T \hat{v}_C(\tau)\, \dot{v}_C(t)\, dt \right] \cdot \frac{\varepsilon_{ox}}{T_{ox}} \cdot \delta A_C + \sum_I \left[\int_0^T \hat{v}_I\, dt \right] \cdot \lambda \cdot \delta w_T \tag{18}$$

D. Optimization flow

The complete P/G network with power-gating optimization flow is summarized in Fig.4. First we set up a floorplanned chip with the initial power grid, define the gated

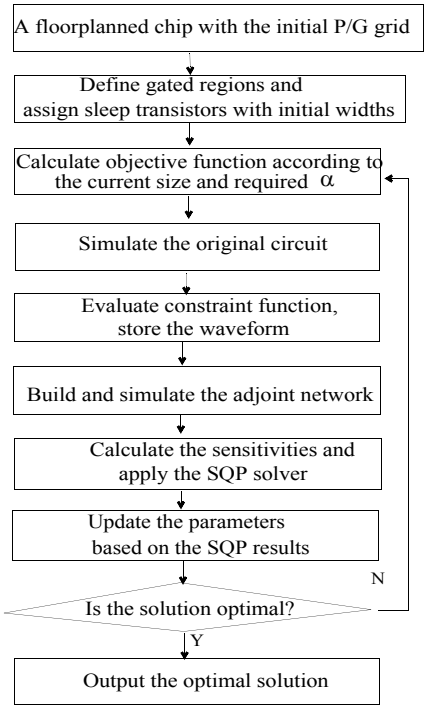


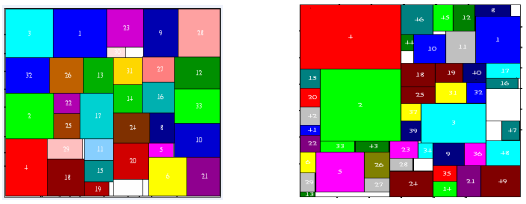
Fig. 4. Optimizing P/G network for power-gating

regions, and assign the initial sizes of sleep transistors to them. Then we apply SQP solver to size the wire segments, decap, and sleep transistor simultaneously to achieve the optimal solution according to the objective function. The sensitivity calculation is done by the adjoint method described in section IV. It must be repeated in every iteration.

V. EXPERIMENTS

We integrated C++ with TCL to develop our optimization flow. HSPICE was used to simulate the circuit and SOL/QPSOL[3] was evoked to solve SQP. We ran all the experiments on a P4 2.4GHz PC with Linux. The test circuits were implemented in $0.13\mu m$ technology with $Vdd = 1.2$. The temperature was $25^\circ C$.

We used circuits from MCNC and ISCAS benchmarks as the basic logic blocks. The switching current profiles and on-chip decap are extracted by simulating each circuit. We mapped those blocks to MCNC floorplan benchmarks *ami33* and *ami49*, respectively. The initial floorplanned chips are shown in Fig.5.



(a) ami33 (b) ami49

Fig. 5. Initial floorplanned chips

We first optimized the power network without power-gating and then applied the power-gating on the circuits in such a way that the gated area occupied half of the chip, consisting of the top-left and bottom-right quadrants. Table.1 shows the effect of power-gating. The first two columns list the data of chip and grid size, respectively. Power mesh reported in this experiment is global power mesh which is mainly affected by power-gating, because sleep transistors are connected to global power mesh. After applying power-gating, there were 96(219) violated nodes in non-gated region which would affect the non-gated circuits. The worst case voltage V_{min} was 0.93(0.72). So we concluded that not considering power-gating could lead to a wrong decision in designing a power supply network.

Table 1. Effect of power-gating

	chip_size (um^2)	grid_size	# of violated nodes	Z (v.ns)	V_{min} (v)
ami33	1232x936	30x30	96	0.58	0.93
ami49	1723x1748	40x40	219	10.07	0.72

Then we applied our flow to optimize the power network with power-gating. We first set $\alpha = 1$, which implies that we target the optimal solution only in terms of area(OptA). Then, based on this optimal solution, we set $\alpha = 0$ to determine the optimized solution in terms of power(OptP). We compared our results with the traditional two-step method (sleep transistor sized first, followed by power network optimization).

Table 2. Comparison of optimizations

		power mesh area	decap&sleep-trans.		V_{min}	# of iters	run time(s)
			area	power (mw)			
ami33	Trad	98739	16476	15.8	1.082	23	581
	OptA	98739	16476	15.8	1.080	26	625
	OptP	98862	22647	14.0	1.081	27	627
ami49	Trad	210631	62323	39.2	1.078	33	2139
	OptA	210631	62323	39.2	1.081	39	2725
	OptP	211064	78389	35.7	1.079	39	2869
cost & saving			0.6%	10%			

The comparison results are shown in Table.2. The area of power-mesh, the area of decaps and sleep transistors, as well as the power consumed by decap and sleep transistor, are reported. From this table, we note that we achieve the same results by applying the traditional method and by applying OptA, which confirms that separately optimizing sleep transistor and power networks will achieve the optimal solution in terms of area. However, it's not the optimal solution in terms of power. Comparing the data in the fifth column, we note that around 10% power saving from decaps and sleep transistors achieved by applying our optimization flow. Because the leakage power is dominant in advanced technologies, the power saving from decap has a significant impact on the total chip power consumption. The area overhead is about 0.6% in chip area, which is negligible. We also notice that the power mesh does not change much comparing OptP with OptA. After the power network with power-gating is re-optimized, worst case voltage is within or close to margin, as shown in the sixth column. Column seven lists the iterations to achieve the optimal solution. The last column lists run time. Although we employed HSPICE inside the optimization flow, run time is still affordable because the global power mesh has relative coarse grids and few nodes.

In the second experiment, we studied the impact of various power-gating schedules on optimization results. We applied four power-gating schedules on each benchmark:

- *g1*: gated area occupied 30% of the chip;
- *g2*: gated area occupied 70% of the chip;
- *g3*: gated area occupied half of the chip and gated blocks have higher current density;
- *g4*: gated area occupied half of the chip and gated blocks have lower current density.



Fig. 6. Different gating schedules

Fig.6 illustrates the gating schedules respectively. Gated circuits are marked grey. In *g3* and *g4*, we purposely re-floorplanned the chip in such a way that circuits with

Table 3. Optimizations vs. power-gating schedules

		before opt V_{min}	OptA			OptP				
			area (um^2)	power (mw)	run_time (s)	area (um^2)	power (mw)	run_time (s)	power saving%	area cost (%)
ami33	g1	1.03	13835	11.2	476	18447	10.3	497	8	0.4
	g2	0.89	26675	20.7	997	37052	19.2	1020	7	0.9
	g3	0.80	37225	28.2	1023	48756	26.0	1151	8	1.0
	g4	0.96	15108	13.8	798	23180	12.3	786	11	0.7
ami49	g1	0.72	59107	33.2	2070	74166	30.5	2113	8	0.5
	g2	0.58	98136	47.5	3070	128254	44.2	3127	7	1.0
	g3	0.51	112790	55.2	3154	145919	51.3	3018	7	1.1
	g4	0.70	51764	31.7	2349	69836	28.8	2413	9	0.6

higher current density are placed in the left half of the chip and circuits with lower current density are placed in the right half of the chip.

We applied our optimization flow on each chip with various power-gating schedules and compared OptA with OptP, in terms of area and power consumed by decap and sleep transistors. Table.3 shows the results. From the table, we note that in both gating schedules *g1* and *g2*, our optimization flow did not save as much power as in the first experiment (refer to Table.1). We explain that result as follows: If the gated area is small, the sleep transistor is small, so adjusting its area does not save much power. When the gated area is large, the sleep transistor is also large, and so the cost of power on the large amount of extra decap nullifies the saving on the sleep transistor. So, our optimization flow favors power-gating with comparable areas of gated and non-gated circuits. However, we note that for the two corner cases, the power consumed by sleep transistor and decap might be equal or exceed the power saving from power-gating, in which case power-gating is not practical.

Comparing the data for *g3* and *g4*, we notice that the advantage of OptP is diminished when gated circuits have higher current densities. This behavior is consistent with the sleep transistor's size increase when current density increases. A small change of sleep transistor will require a large amount of decap to ameliorate the noise. More decap consumes more leakage power, which makes the power saving on sleep transistor relatively smaller. So our optimization flow is more effective when power-gating is applied on circuits with smaller current densities. Again, we note that in case of large current density of the gated circuits, the amount of power consumed by the sleep transistor and decap will be larger, which may nullify the saving from power-gating. In such a case, we would not choose to apply the power-gating technique.

VI. CONCLUSION

In this paper, we have studied the effects on P/G network introduced by a power-gating technique and analyzed mutual dependencies between the sleep transistor and the P/G network. We presented a general flow to optimize the P/G supply network for power-gating in terms of both power and area. Experimental results show that sizing a sleep transistor and a power network separately cannot achieve an optimal solution in terms of power. By compromising only 1% of the total area, our optimization method allows us to save 10% of power dissipated on decaps and sleep transistors. This offers a practical solution for a power-gated system. Our optimization flow is more effective when gated circuits are of smaller current density, and when the areas of gated and non-gated circuit are comparable. We believe that our results could be used as reference by designers working on power-gating systems.

ACKNOWLEDGEMENT

This work was supported in part by SRC grant # 1069 and in part by MICRO through IBM. We gratefully acknowledge equipment grant from Intel.

REFERENCES

[1] K.Choi, Y.Xu and T.Sakura, "An effective yet feasible power-gating scheme achieving two orders of magnitude lower standby leakage", *Symposium on VLSI Circuits*, pp. 312-315, 2005.

[2] P.Feldmann, T.V.Nguyen and et al, "Sensitivity computation in piecewise approximate circuit simulation", *IEEE Trans on Computer Aided Design*, pp. 171-183, 1991.

[3] P.E.Grill, W.Murray, and et al, User's Guide for SOL/OPSOL: A Fortran Package for Quadratic Programming. Stanford, CA. Dept. Oper. Res.

[4] H.Jiang, M.Marek-Sadowsks and S.R.Nassif, "Benefits and costs of power-gating technique", *International Conference on Computer Design,* pp 559-566, 2005

[5] C.Long and L.He, "Distributed Sleep Transistor Network for Power Reduction", IEEE Trans of VLSI, pp. 937-946, 2004

[6] S.Mutoh and et al, "A 1V power supply high-speed digital circuit technology with multi threshold voltage CMOS", *IEEE Journal of Solid-State Circuit,* pp. 847-854, 1995.

[7] H.Su, S.S.Sapatnekar, and S.R.Nassif, "Optimal decoupling capacitor sizing and placement for standard-cell layout designs", *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems,* pp. 428-436, April 2003.

[8] T.Sakurai and A.Newton, "Alpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas" *IEEE Journal of Solid-State Circuits,* vol25, pp. 584-594, 1990.

[9] K.Wang and M.Marek-Sadowska, "On-chip power-supply network optimization using multigrid-based technique", *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems,* pp 407-417, 2005.

ATTACHMENT 3A

MARC Bibliographic Record

```
LEADER     -----nas--2200817-i-4500
001        991023072665202122
005        20230402213018.0
006        m-----o--d--------
007        cr-bn||||||abp
007        cr-bn||||||ada
008        100325c198u9999njuar---o-----1---a0eng--
010            $a 2018200078
022            $a1063-6404
035            $a(OCoLC)576979754
035            $a(CKB)5280000000213320
035            $a(CONSER)--2018200078
035            $a(EXLCZ)995280000000213320
042            $apcc$adlr$ansdp
050    00      $aTK7888.4
082    10      $a621$223
082    04      $a621.395/05$219
111    2_      $aIEEE International Conference on Computer Design,$jissuing
               body.
```

```
210         $aIEEE INTERNATIONAL CONFERENCE ON COMPUTER DESIGN VLSI IN
            COMPUTERS AND PROCESSOR

210         $aIEEE INTERNATIONAL CONFERENCE ON COMPUTER DESIGN

210    0_   $aProc. IEEE Int. Conf. Comput. Des.$b(Online)

222    _0   $aProceedings, IEEE International Conference on Computer
            Design$b(Online)

245    10   $aProceedings, IEEE International Conference on Computer
            Design :$bVLSI in Computers /$csponsored by IEEE Computer
            Society and IEEE Circuits and Systems Society technical
            committees on Large Scale Systems [and others].

246    1_   $iVols. for 1995- have title:$aProceedings, International
            Conference on Computer Design

246    1_   $aVLSI in computers

246    1_   $aVLSI in computers and processors

246    1_   $aProceedings of the ... IEEE International Conference on
            Computer Design

264    _1   $aSilver Spring, Md. :$bIEEE Computer Society Press

264    31   $3<2011->:$aPiscataway, NJ :$bIEEE

310         $aAnnual

336         $atext$btxt$2rdacontent

337         $acomputer$bc$2rdamedia

338         $aonline resource$bcr$2rdacarrier

500         $aPlace of publication varies: Washington, D.C., 1985- ; Los
            Alamitos, Calif., <'91->
```

500 $aSubtitle varies.

538 $aMaster and use copy. Digital master created according to Benchmark for Faithful Digital Reproductions of Monographs and Serials, Version 1. Digital Library Federation, December 2002.$uhttp://purl.oclc.org/DLF/benchrepro0212$5MiAaHDL

550 $aSponsored 1986- by IEEE Computer Society (its Technical Committee on Design Automation, 1995-), IEEE Circuits and Systems Society, and IEEE Electron Devices Society.

583 1_ $adigitized$c2010$hHathiTrust Digital Library$lcommitted to preserve$2pda$5MiAaHDL

588 $aDescription based on print version record.

588 $aLatest issue consulted: 38th (2020) (IEEE Xplore, viewed Feb. 9, 2020).

650 _0 $aElectronic digital computers$xCircuits$vCongresses.

650 _0 $aIntegrated circuits$xVery large scale integration$vCongresses.

650 _7 $aElectronic digital computers$xCircuits.$2fast$0(OCoLC)fst00907124

650 _7 $aIntegrated circuits$xVery large scale integration.$2fast$0(OCoLC)fst00975602

655 _7 $aPeriodicals.$2fast$0(OCoLC)fst01411641

655 _7 $aConference papers and proceedings.$2fast$0(OCoLC)fst01423772

655 _7 $aPeriodicals.$2lcgft

655 _7 $aConference papers and proceedings.$2lcgft

762 0_ $t2008 IEEE International Conference on Computer

Design$w(CKB)1000000000710600$z1-5090-7851-7

762 0_ $tComputer Design: VLSI in Computers and Processors, 1995. ICCD '95. Proceedings., 1995 IEEE International Conference on$w(CKB)111055184265066

762 0_ $tProceedings International Conference on Computer Design. VLSI in Computers and Processors$w(CKB)111026746743082

762 0_ $t2012 IEEE 30th International Conference on Computer Design (ICCD)$w(CKB)2670000000319048$z1-4673-3052-3

762 0_ $tProceedings International Conference on Computer Design VLSI in Computers and Processors$w(CKB)111026746746432

762 0_ $t2009 IEEE International Conference on Computer Design$w(CKB)2400000000001735$z1-4244-5028-4

762 0_ $tProceedings International Conference on Computer Design. VLSI in Computers and Processors (Cat. No.98CB36273)$w(CKB)111026746748720

762 0_ $tProceedings 1999 IEEE International Conference on Computer Design: VLSI in Computers and Processors (Cat. No.99CB37040)$w(CKB)111055184221008

762 0_ $tProceedings 2000 International Conference on Computer Design$w(CKB)111026746702506

762 0_ $tProceedings. IEEE International Conference on Computer Design: VLSI in Computers and Processors$w(CKB)111055184228484

774 0_ $tProceedings 2001 IEEE International Conference on Computer Design: VLSI in Computers and Processors. ICCD 2001$w(CKB)111055184225184

762 0_ $t2010 IEEE International Conference on Computer Design$w(CKB)2670000000058820$z1-4244-8937-7

762 0_ $tProceedings 21st International Conference on Computer Design$w(CKB)111085500343044

762 0_ $tIEEE International Conference on Computer Design: VLSI in Computers and Processors, 2004. ICCD 2004. Proceedings$w(CKB)1000000000021898

762 0_ $tComputer Design, 2006. ICCD 2006. International Conference on$w(CKB)1000000000331701$z1-5090-9163-7

762 0_ $t2011 IEEE 29th International Conference on Computer Design (ICCD)$w(CKB)267000000131581$z1-4577-1954-1

762 0_ $t2007 25th International Conference on Computer Design$w(CKB)1000000000711109$z1-5090-8607-2

776 $x2576-6996

710 2_ $aIEEE Computer Society,$esponsoring body.

710 2_ $aIEEE Circuits and Systems Society,$esponsoring body.

710 2_ $aInstitute of Electrical and Electronics Engineers,$epublisher.

710 2_ $aIEEE Electron Devices Society,$esponsoring body.

710 2_ $aIEEE Computer Society.$bDesign Automation Technical Committee,$esponsoring body.

906 $aCONFERENCE

MMS IDs

Document ID:

9911027862502121

Network Electronic IDs:

9913405518502121, 9911027862502121

Network Physical IDs:

mms_plt_ids:

991013509061902128

mms_mad_ids:

991023072665202122

mms_rf_ids:

991014138862802129

ATTACHMENT 3B

OCLC 613544548 **No holdings in XXX - 30 other holdings**

Books

						Rec Stat		**Entered**	20051118	**Replaced**	20220428105945.3
Type	a	**ELvl**	M	**Srce**	d	**Audn**		**Ctrl**		**Lang**	eng
BLvl	m	**Form**	o	**Conf**	1	**Biog**		**MRec**		**Ctry**	nju
		Cont	b	**GPub**		**LitF**	0	**Indx**	1		
Desc	a	**Ills**	a	**Fest**	0	**DtSt**	s	**Dates**	2006,		

007 c $b r $d c $e n $g ---
040 W2U $b eng $c W2U $d OCLCQ $d OCLCF $d OCLCO $d OCL $d OCLCO $d OCLCA $d OCLCQ $d OCLCO
020 9780780397071
020 078039707X
020 $z 142449707X
050 4 TK7888.3
090 $b
111 2 IEEE International Conference on Computer Design $d (2006 : $c San Jose, Calif.)
245 10 International Conference on Computer Design, 2006 : $b ICCD 2006 : 1-4 October, 2006, [San Jose, California / $c sponsored by IEEE Computer Society, IEEE Circuits and Systems Society, IEEE Electron Devices Society].
246 3 Proceedings of the 2006 International Conference on Computer Design
246 30 Computer design
246 30 ICCD 2006
260 [Piscataway, N.J.] : $b IEEE, $c ©2006.
336 text $b txt $2 rdacontent
337 computer $b c $2 rdamedia
338 online resource $b cr $2 rdacarrier
500 Title from title screen (viewed Nov. 20, 2007).
500 "IEEE Catalog Number: 06CH37820C."
504 Includes bibliographical references and author index.
506 Subscription to IEEE Xplore (Online service) required to access full text.
538 Mode of access: World Wide Web.
650 0 Computer engineering $v Congresses.
650 0 Embedded computer systems $v Congresses.
650 0 Integrated circuits $x Very large scale integration $v Congresses.
650 0 Electronic digital computers $x Circuits $v Congresses.
650 0 Microcomputers $x Design and construction $v Congresses.
650 6 Ordinateurs $0 (CaQQLa)201-0015833 $x Conception et construction $0 (CaQQLa)201-0015833 $v Congrès. $0 (CaQQLa)201-0378219
650 6 Systèmes enfouis (Informatique) $0 (CaQQLa)201-0171574 $v Congrès. $0 (CaQQLa)201-0378219
650 6 Circuits intégrés à très grande échelle $0 (CaQQLa)201-0117255 $v Congrès. $0 (CaQQLa)201-0378219
650 6 Ordinateurs $0 (CaQQLa)201-0035980 $x Circuits $0 (CaQQLa)201-0035980 $v Congrès. $0 (CaQQLa)201-0378219
650 7 Computer engineering. $2 fast $0 (OCoLC)fst00872078

650 7 Electronic digital computers $x Circuits. $2 fast $0 (OCoLC)fst00907124
650 7 Embedded computer systems. $2 fast $0 (OCoLC)fst00908298
650 7 Integrated circuits $x Very large scale integration. $2 fast $0 (OCoLC)fst00975602
650 7 Microcomputers $x Design and construction. $2 fast $0 (OCoLC)fst01019653
655 7 Conference papers and proceedings. $2 fast $0 (OCoLC)fst01423772
710 2 IEEE Xplore (Online service)
710 2 IEEE Electron Devices Society.
710 2 IEEE Circuits and Systems Society.
710 2 IEEE Computer Society.

ATTACHMENT 3C

LIBRARY OF CONGRESS AUTHORITIES

LC control no.: sh2008102939
LCCN Permalink: https://lccn.loc.gov/sh2008102939
HEADING: Embedded computer systems Congresses

000 00502cz a2200169n 450
001 7440885
005 20110729160214.0
008 080208|| anannbabn |n ana
010 __ |**a** sh2008102939
035 __ |**a** (DLC)378505
035 __ |**a** (DLC)sh2008102939
040 __ |**a** DLC |**b** eng |**c** DLC
150 __ |**a** Embedded computer systems |**v** Congresses
667 __ |**a** Record generated for validation purposes.
670 __ |**a** Work cat.: Architecture and design of distributed embedded systems, c2001
906 __ |**t** 8888 |**u** te00 |**v** 0
953 __ |**a** te00

◀ Previous Next ▶

Save, Print or Email Records (View Help)

Select Download Format: Text (Labelled Display) Press to SAVE or PRINT

Email Text (Labelled Display) to: Press to SEND EMAIL

Library of Congress
URL: https://www.loc.gov/

Mailing Address:
101 Independence Ave, S.E.
Washington, DC 20540

Library of Congress Authorities
URL: http://authorities.loc.gov/
Library of Congress Online Catalog
URL: https://catalog.loc.gov/

Questions, comments, error reports: Contact Us

AMD EX1021
AMD v. Realtek - Page 184

ATTACHMENT 4

ISQED 2007

Proceedings of the

2007
8th International Symposium on

Quality Electronic Design

March 26-28, 2007
San Jose, California

ISQED 2007 is held with technical sponsorship from the IEEE Electron Devices Society (EDS), IEEE Reliability Society, and In cooperation with IEEE Circuits and Systems Society (CASS), ACM Special Interest Group on Design Automation (ACM/sigDA). ISQED 2007 is produced and sponsored by the International Society for Quality Electronic Design (http://www.isqed.org). All rights reserved by ISQED.

Proceedings

Eighth International Symposium on Quality Electronic Design

ISQED 2007

San Jose, California
26-28 March 2007

IEEE COMPUTER SOCIETY
IEEE

Los Alamitos, California

Washington • Tokyo

CPS Conference Publishing Services

AMD EX1021
AMD v. Realtek - Page 187

TK7874.15
.I565
2007

Copyright © 2007 by The Institute of Electrical and Electronics Engineers, Inc.

All rights reserved.

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries may photocopy beyond the limits of US copyright law, for private use of patrons, those articles in this volume that carry a code at the bottom of the first page, provided that the per-copy fee indicated in the code is paid through the Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

Other copying, reprint, or republication requests should be addressed to: IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, P.O. Box 133, Piscataway, NJ 08855-1331.

The papers in this book comprise the proceedings of the meeting mentioned on the cover and title page. They reflect the authors' opinions and, in the interests of timely dissemination, are published as presented and without change. Their inclusion in this publication does not necessarily constitute endorsement by the editors, the IEEE Computer Society, or the Institute of Electrical and Electronics Engineers, Inc.

IEEE Computer Society Order Number P2795
ISBN 0-7695-2795-7
ISBN 978-0-7695-2795-6
Library of Congress Number 2006939397

Additional copies may be ordered from:

IEEE Computer Society
Customer Service Center
10662 Los Vaqueros Circle
P.O. Box 3014
Los Alamitos, CA 90720-1314
Tel: + 1 800 272 6657
Fax: + 1 714 821 4641
http://computer.org/cspress
csbooks@computer.org

IEEE Service Center
445 Hoes Lane
P.O. Box 1331
Piscataway, NJ 08855-1331
Tel: + 1 732 981 0060
Fax: + 1 732 981 9667
http://shop.ieee.org/store/
customer-service@ieee.org

IEEE Computer Society
Asia/Pacific Office
Watanabe Bldg., 1-4-2
Minami-Aoyama
Minato-ku, Tokyo 107-0062
JAPAN
Tel: + 81 3 3408 3118
Fax: + 81 3 3408 3553
tokyo.ofc@computer.org

Individual paper REPRINTS may be ordered at: <reprints@computer.org>

Editorial production by Lisa O'Conner
Cover art production by Joe Daigle/Studio Productions
Printed in the United States of America by The Printing House





Conference Publishing Services
http://www.computer.org/proceedings/

AMD EX1021
AMD v. Realtek - Page 188

Eighth International Symposium on

Quality Electronic Design

Table of Contents

Welcome Notes xvii
Organizing Committee xix
Technical Sub-Committees xx
Steering Committee xxiii
Advisory Committee xxiii
Best Paper Selection Committee xxiv
Conference at a Glance xxv

Tutorials

Chair and Moderator: **Rajiv Joshi**, *IBM T.J. Watson Research Center*

Tutorial I

SUB 45nm Technology and Design Challenges 3
Presenters: ***Gerhard Knoblinger***, *Infineon Technologies*
James W. Tschanz, *Intel*
Marcal Pol, *IMEC*

Multi-Gate MOSFET Design 3
Presenter: ***Gerhard Knoblinger***, *Infineon Technologies*

SUB 45nm Low Power Design Challenges 4
Presenter: ***James W. Tschanz***, *Intel*

Self-Adaptive Systems to Drive out the Nano-Scale Devil 4
Presenter: ***Marcal Pol***, *IMEC*

Tutorial II

Quality Driven Manufacturing and SOC Designs 5
Presenters: ***Srikanth Venkataraman***, *Intel*
Nagesh Nagapalli, *AMD*
Lech Jozwiak, *Eindhoven University of Technology*

DFM, DFY, Debug and Diagnosis: The Loop to Ensure Yield 5
Presenter: ***Srikanth Venkataraman***, *Intel*

LINDA HALL LIBRARY
KANSAS CITY, MO

AMD EX1021
AMD v. Realtek - Page 189

DFT and Test: Ensuring Product Quality 5
Presenter: ***Nagesh Nagapalli**, AMD*

Quality-Driven Architecture Synthesis and Power Aware Design of Embedded SoCs 6
Presenter: ***Lech Jozwiak**, Eindhoven University of Technology*

Evening Panel Discussion EP1

DFM—EDA's Salvation or its Excuse for Being Out of Touch with Engineering? 7
Moderator: ***Resve Saleh**, UBC Vancouver*
Organizer: ***Pallab Chatterjee**, SilicaonMap*
Panelists: ***Ivan Pesic**, President, Silvaco/Simucad*
***Robbert Dobkins**, CTO, Linear Technologies*
***Mike Smayling**, CTO Applied Materials*
***Joe Sawicki**, VP Design to Silicon Div Mentor Graphics*

Plenary Session 1P

Co-Chairs: **Kris Verma**, *Silicon Valley Technical Institute*
Massoud Pedram, *University of Southern California*

Plenary Speech

Tipping Point for New Design Technologies: DFM, Low Power and ESL 10
Jeong-Taek Kong

Session 1A: Design for Manufacturing

Chair: **Kevin Brelsford**, *Synopsys*
Co-Chair: **Praveen Elakkumanan**, *IBM*

Variation (Invited Paper) 15
Duane Boning, Karthik Balakrishnan, Hong Cai, Nigel Drego, Ali Farahanchi, Karen Gettings, Daihyun Lim, Ajay Somani, Hayden Taylor, Daniel Truque, and Xiaolin Xie

A MOS Transistor-Array for Accurate Measurement of Subthreshold Leakage Variation 21
Takashi Sato, Takumi Uezono, Shiho Hagiwara, Kenichi Okada, Shuhei Amakawa, Noriaki Nakayama, and Kazuya Masu

Strain Silicon Optimization for Memory and Logic in Nano-Scale CMOS 27
Rajani Kuchipudi and Hamid Mahmoodi

Gate Leakage Effects on Yield and Design Considerations of PD/SOI SRAM Designs 33
Rouwaida Kanj, Rajiv Joshi, Jayakumaran Sivagnaname, J.B. Kuang, Dhruva Acharayya, Tuyet Nguyen, Chandler McDowell, and Sani Nassif

Session 1B: Device and Circuit Reliability

Chair: **Samar Saha**, *Synopsys*
Co-Chair: **Nicos Konofaos**, *University of the Aegean, Greece*

A New Simulation Method for NBTI Analysis in SPICE Environment 41
Rakesh Vattikonda, Yansheng Luo, Alex Gyure, Xiaoning Qi, Sam Lo, Mahmoud Shahram, Yu Cao, Kishore Singhal, and Dino Toffolon

Combating NBTI Degradation via Gate Sizing 47
Xiangning Yang and Kewal Saluja

AMD EX1021
AMD v. Realtek - Page 190

Analytical Modeling of Hot-Carrier Induced Gegradation of MOS Transistors for Analog Design for Reliability 53
Benoît Dubois, Jean-Baptiste Kammerer, Luc Hébrard, and Francis Braun

A New Organic Thin-Film Transistor Based Current-Driving Pixel Circuit for Active-Matrix Organic Light-Emitting Displays 59
Aram Shin, Sang Jun Hwang, Seung Woo Yu, and Man Young Sung

Session 1C: Power and Thermal Management

Chair: **Dinesh Somasekhar**, *Intel*
Co-Chair: **Praveen Bhojwani**, *Texas A&M*

Mitigating Thermal Effects on Clock Skew with Dynamically Adaptive Drivers 67
Mosin Mondal, Andrew Ricketts, Sami Kirolos, Tamer Ragheb, Greg Link, Vijaykrishnan Narayanan, and Yehia Massoud

Dual-V_{DD} Clock Distribution for Low Power and Minimum Temperature Fluctuations Induced Skew 73
Sherif A. Tawfik and Volkan Kursun

Speculative Energy Scheduling for LDPC Decoding 79
Weihuang Wang and Gwan Choi

Dynamic Power Management by Combination of Dual Static Supply Voltages 85
Kanak Agarwal and Kevin Nowka

Session 1D: Analog and Mixed Signal Design

Chair: **George Alexiou**, *University of Patras*
Co-Chair: **Haibo Wang**, *Southern Illinois University Carbondale*

Low Voltage Buffered Bandgap Reference 93
Peter Hazucha, Fabrice Paillet, Sung Tae Moon, David J. Rennie, Gerhard Schrom, Donald S. Gardner, Kenneth Ikeda, Gell Gellman, and Tanay Karnik

A DLL Based Multiphase Hysteretic DC-DC Converter 98
Pengfei Li and Rizwan Bashirullah

Statistical Timing Analysis Considering Spatial Correlations 102
Hong Li, Cheng-Kok Koh, Venkataramanan Balakrishnan, and Yiran Chen

Systematic Design of a Flash ADC for UWB Applications 108
Liang Rong, E. Martin I. Gustafsson, Ana Rusu, and Mohammed Ismail

Luncheon Speech

EDA to the Rescue of the Silicon Roadmap 115
Thomas W. Williams, Synopsis

AMD EX1021
AMD v. Realtek - Page 191

Session 2A: Quality and Reliability
Chair: **Paul Tong**, *Pericom Inc.*
Co-Chair: **Bao Liu**, *UCSD*

Assessing the Implications of Process Variations on Future Carbon Nanotube Bundle Interconnect Solutions 119
Arthur Nieuwoudt and Yehia Massoud

FinFET Based SRAM Design for Low Standby Power Applications 127
Tamer Cakici, Keejong Kim, and Kaushik Roy

Compact Modeling of a PD SOI MESFET for Wide Temperature Designs 133
Asha Balijepalli, Joseph Ervin, Yu Cao, and Trevor Thornton

Modeling of PMOS NBTI Effect Considering Temperature Variation 139
Hong Luo, Yu Wang, Ku He, Rong Luo, Huazhong Yang, and Yuan Xie

Device Footprint Scaling for Ultra Thin Body Fully Depleted SOI 145
Jie Deng, Keunwoo Kim, Ching-Te Chuang, and H.-S. Philip Wong

Session 2B: Advances in Timing and Power in Physical Design
Chair: **Martin Wang**, *UIUC*
Co-Chair: **Shahin Nazarian**, *University of Southern California*

A Low-Power Multi-Pin Maze Routing Methodology 153
Ahmed Youssef, Tor Myklebust, Mohab Anis, and Mohamed Elmasry

An Aggregation-Based Algebraic Multigrid Method for Power Grid Analysis 159
Pei-Yu Huang, Huan-Yu Chou, and Yu-Min Lee

Design and Analysis of "Tree + Local Meshes" Clock Architecture 165
Gustavo R. Wilke and Rajeev Murgai

An Efficient Algorithm for RLC Buffer Insertion 171
Zhanyuan Jiang, Shiyan Hu, Jiang Hu, and Weiping Shi

Fast Crosstalk Repair by Quick Timing Change Estimation 176
Nahmsuk Oh, Alireza Kasnavi, and Peivand Tehrani

Session 2C: Power-Aware System Design Methodologies
Chair: **Lech Jozwiak**, *Eindhoven University of Technology*
Co-Chair: **Tohru Ishihara**, *Kyushu University*

Leakage-Conscious Architecture-Level Power Estimation for Partitioned and Power-Gated SRAM Arrays 185
Minh Q. Do, Mindaugas Dražd̄iulis, Per Larsson-Edefors, and Lars Bengtsson

Cross Layer Error Exploitation for Aggressive Voltage Scaling 192
Amin Khajeh Djahromi, Ahmed M. Eltawil, Fadi J. Kurdahi, and Rouwaida Kanj

A Unified Framework for System-Level Design: Modeling and Performance Optimization of Scalable Networking Systems 198
Hwisung Jung and Massoud Pedram

Thermal vs Energy Optimization for DVFS-Enabled Processors in Embedded Systems 204
Yongpan Liu, Huazhong Yang, Robert P. Dick, Hui Wang, and Li Shang

A Unified Optimal Voltage Selection Methodology for Low-Power Systems 210
Foad Dabiri, Roozbeh Jafari, Ani Nahapetian, and Majid Sarrafzadeh

AMD EX1021
AMD v. Realtek - Page 192

Session 2D: Poster Papers

Chair: Syed M. Alam, *Freescale Semiconductor*
Co-Chair: Zhen Guo, *Conexant Systems*

Reducing Delay Uncertainty of On-Chip Interconnects by Combining Inverting and Non-Inverting Repeaters Insertion 219
Charbel J. Akl and Magdy A. Bayoumi

A 8b 10Ms/s Low Power Pipelined A/D Converter 225
Bi Yuan, Yi Zhang, and Lili He

First-Order Continuous-Time Sigma-Delta Modulator 229
Yamei Li and Lili He

Reducing EPL Alignment Errors for Large VLSI Layouts 233
Yokesh Kumar and Prosenjit Gupta

Charge Recycling Between Virtual Power and Ground Lines for Low Energy MTCMOS 239
Zhiyu Liu and Volkan Kursun

Efficient Signal Integrity Verification of Multi-Coupled Transmission Lines with Asynchronously Switching Non-Linear Drivers 245
Taeyong Je and Yungseon Eo

Repeated On-Chip Interconnect Analysis and Evaluation of Delay, Power, and Bandwidth Metrics under Different Design Goals 251
Ling Zhang, Hongyu Chen, Bo Yao, Kevin Hamilton, and Chung-Kuan Cheng

Gate Level Statistical Simulation Based on Parameterized Models for Process and Signal Variations 257
Bao Liu

Tests on Symmetry and Continuity between BSIM4 and BSIM5 263
Xudong Niu, Yan Song, Bo Li, Wei Bian, Yadong Tao, Feng Liu, Jinhua Hu, Yu Chen, and Frank He

Interface Specification Assurance Methods 269
Naiyong Jin and Taoyong Ni

Multi-Dimensional Circuit and Micro-Architecture Level Optimization 275
Zhenyu (Jerry) Qi, Matthew Ziegler, Stephen V. Kosonocky, Jan M. Rabaey, and Mircea R. Stan

A Test-Structure to Efficiently Study Threshold-Voltage Variation in Large MOSFET Arrays 281
Nigel Drego, Anantha Chandrakasan, and Duane Boning

Novel and Efficient IR-Drop Models for Designing Power Distribution Network for Sub-100nm Integrated Circuits 287
Rishi Bhooshan

Processing High Volume Scan Test Results for Yield Learning 293
Alfred L. Crouch, Phil Burlison, and Dennis Ciplickas

Planar-CRX: A Single-Layer Zero Skew Clock Routing in X-Architecture 299
Weixiang Shen, Yici Cai, Xianlong Hong, Jiang Hu, and Bing Lu

Comparative Robustness of CML Phase Detectors for Clock and Data Recovery Circuits 305
David Rennie and Manoj Sachdev

Inductive Fault Analysis for Test and Diagnosis of DNA Sensor Arrays 311
Daniela De Venuto and Bruno Riccò

Fine-Grained Redundancy in Adders 317
Patrick Ndai, Shih-Lien Lu, Dinesh Somesekhar, and Kaushik Roy

MEMS Failure Probability Prediction and Quality Enhancement Using Neural Networks 322
A. Ilumoka and Hong Lang Tan

AMD EX1021
AMD v. Realtek - Page 193

Variation Aware Timing Based Placement Using Fuzzy Programming 327
V. Mahalingam and N. Ranganathan

Variation Analysis of CAM Cells 333
Amol Mupid, Madhu Mutyam, N. Vijaykrishnan, Y. Xie, and M.J. Irwin

Design-for-Manufacture for Multi Gate Oxide CMOS Process 339
Qi Lin, Mei Ma, Tony Vo, Jenny Fan, Xin Wu, Richard Li, and Xiao-Yu Li

Intelligent Random Vector Generator Based on Probability Analysis of Circuit Structure 344
Yu-Min Kuo, Cheng-Hung Lin, Chun-Yao Wang, Shih-Chieh Chang, and Pei-Hsin Ho

Power Delivery Aware Floorplanning for Voltage Island Designs 350
Yici Cai, Bin Liu, Jin Shi, Qiang Zhou, and Xianlong Hong

Passive Modeling of Interconnects by Waveform Shaping 356
Boyuan Yan, Pu Liu, Sheldon X.-D. Tan, and Bruce McGaughy

A Power Network Synthesis Method for Industrial Power Gating Designs 362
Kaijian Shi, Zhian Lin, and Yi-Min Jiang

Reducing the Energy Consumption in Fault-Tolerant Distributed Embedded Systems with Time-Constraint 368
Yuan Cai, Sudhakar M. Reddy, and Bashir M. Al-Hashimi

Challenges in Evaluations for a Typical-Case Design Methodology 374
Yuji Kunitake, Akihiro Chiyonobu, Koichiro Tanaka, and Toshinori Sato

SEU-Mitigation Placement and Routing Algorithms and Their Impact in SRAM-based FPGAs 380
Hamid R. Zarandi, Seyed G. Miremadi, Dhiraj K. Pradhan, and Jimson Mathew

Performance-Energy Tradeoffs for Matrix Multiplication on FPGA-Based Mixed-Mode Chip Multiprocessors 386
Xiaofang Wang and Sotirios G. Ziavras

A High Frequency PWM Controller in HV Bi-CMOS Process Considering SOI Self-Heating 392
Gautam Kumar Singh and Santosh Kumar Panigrahi

Sensitivity Based Link Insertion for Variation Tolerant Clock Network Synthesis 398
Joon-Sung Yang, Anand Rajaram, Ninghy Shi, Jian Chen, and David Z. Pan

Built-In Test of RF Mixers Using RF Amplitude Detectors 404
Chaoming Zhang, Ranjit Gharpurey, and Jacob A. Abraham

Glitch Control with Dynamic Receiver Threshold Adjustment 410
Michael N. Skoufis, Haibo Wang, Themistoklis Haniotakis, and Spyros Tragoudas

Programmable High Speed Multi-Level Simultaneous Bidirectional I/O 416
Yong Sin Kim and Sung-Mo Kang

A Fault Tolerant Design Methodology for Threshold Logic Gates and its Optimizations 420
Manoj Kumar Goparaju and Spyros Tragoudas

Transistor Sizing for Load Balance of Multiple Paths in Dynamic CMOS for Timing Optimization 426
Kumar Yelamarthi and Chien-In Henry Chen

Wavelet-Based Passivity Preserving Model Order Reduction for Wideband Interconnect Characterization 432
Mehboob Alam, Arthur Nieuwoudt, and Yehia Massoud

System Level Estimation of Interconnect Length in the Presence of IP Blocks 438
Taraneh Taghavi, Ani Nahapetian, and Majid Sarrafzadeh

Energy-Minimization Model for Fill Synthesis 444
Rasit Onur Topaloglu

On-Chip Inductance in X Architecture Enabled Designs 452
Santosh Shah, Arani Sinha, Li Song, and Narain D. Arora

AMD EX1021
AMD v. Realtek - Page 194

Impact of Variability on Clock Skew in H-tree Clock Networks 458
Ashok Narasimhan and Ramalingam Sridhar

Session 3A: Electrical Quality
Chair: Tom Jackson, *Cadence Design*
Co-Chair: Antonio Nunez, *University of Las Palmas*

A DOE Set for Normalization-Based Extraction of Fill Impact on Capacitances 467
Andrew B. Kahng and Rasit Onur Topaloglu

SilcVerify: An Efficient Substrate Coupling Noise Simulation Tool for High-Speed & Nano-Scaled Memory Design 475
Jeong-Yeol Kim, Ho-Soon Shin, Jong-Bae Lee, Moon-Hyun Yoo, and Jeong-Taek Kong

Pareto-Front Computation and Automatic Sizing of CPPLLs 481
Jun Zou, Daniel Mueller, Helmut Graeb, and Ulf Schlichtmann

InVerS: An Incremental Verification System with Circuit Similarity Metrics and Error Visualization 487
Kai-Hui Chang, David A. Papa, Igor L. Markov, and Valeria Bertacco

Session 3B: Analog and RF Testing
Chair: Spyros Tragoudas, *Southern Illinois University*
Co-Chair: Li-C Wang, *University of California, Santa Barbara*

Pseudorandom Test for Nonlinear Circuits Based on a Simplified Volterra Series Model 495
Joonsung Park, Hongjoong Shin, and Jacob A. Abraham

Design of a Window Comparator with Adaptive Error Threshold for Online Testing Applications 501
Amit Laknaur, Rui Xiao, Sai Durbha, and Haibo Wang

High-Frequency-Measurement-Based Frequency-Variant Transmission Line Characterization and Circuit Modeling for Accurate Signal Integrity Verification 507
Hyunsik Kim and Yungseon Eo

Achieving Low-Cost Linearity Test and Diagnosis of ΣΔ ADCs via Frequency-Domain Nonlinear Analysis and Macromodeling 513
Guo Yu, Peng Li, and Wei Dong

Fully Digital Optimized Testing and Calibration Technique for EΔ ADC's 519
Daniela De Venuto and Leonardo Reyneri

Session 3C: Low Power Circuits
Chair: Mark Budnik, *Valparaiso University*
Co-Chair: Praveen Elakkumanan, *IBM Semiconductor R & D Center*

Cell-Based Semicustom Design of Zigzag Power Gating Circuits 527
Youngsoo Shin and Hyung-Ock Kim

Lookup Table-Based Adaptive Body Biasing of Multiple Macros 533
Byunghee Choi and Youngsoo Shin

A Simple Flip-Flop Circuit for Typical-Case Designs for DFM 539
Toshinori Sato and Yuji Kunitake

A High Performance, Scalable Multiplexed Keeper Technique 545
Jaydeep P. Kulkarni and Kaushik Roy

AMD EX1021
AMD v. Realtek - Page 195

On-Line Adjustable Buffering for Runtime Power Reduction 550
Andrew B. Kahng, Sherief Reda, and Puneet Sharma

Plenary Session 2P

Co-Chairs: **Lech Jozwiak, Bindhoven** *University of Technology*
George Alexiou, *University of Patras and Computer Technology Institute, Patras, Greece*

Plenary Speechs

Programmable Engines for Embedded Systesm: The New Challenges 558
Marc Duranton

Soft-Errors Phenomenon Impacts on Design for Reliability Technologies 560
Marc Derbey

Forging Tighter Connections Between Design and Manufacturing in the Nanometer Age 562
Joseph Sawicki

Session 4A: Package Circuit Co-Design

Chair: **Kris Verman,** *Silicon Valley Technical Institute*
Co-Chair: **Lalitha Immaneni,** *Intel*

3DFFT: Thermal Analysis of Non-Homogeneous IC Using 3D FFT Green Function Method 567
Dongkeun Oh, Charlie Chung-Ping Chen, and Yu Hen Hu

Upper/Lower Boundary Estimation of Package Interconnect Parasitics for Chip-Package Co-Design 573
Eunseok Song, Heeseok Lee, Jungtae Lee, Woojin Jin, Kiwon Choi, and Sa-Yoon Kang

Inter-Strata Connection Characteristics and Signal Transmission in Three-Dimensional (3D) Integration Technology 580
Syed M. Alam, Robert E. Jones, Shahid Rauf, and Ritwik Chatterjee

A Design Methodology for Matching Improvement in Bandgap References 586
Juan Pablo Martinez Brito, Hamilton Klimach, and Sergio Bampi

Session 4B: High Level Optimization

Chair: **Anand Iyer,** *Cadence Design*
Co-Chair: **Masahiro Fujita,** *University of Tokyo*

Balanced Scheduling and Operation Chaining in High-Level Synthesis for FPGA Designs 595
David C. Zaretsky, Gaurav Mittal, Robert P. Dick, and Prith Banerjee

Efficient Transition-Mode Boolean Characteristic Function with its Application to Maximum Instantaneous Current Analysis 602
Cheng-Tao Hsieh, Jian-Cheng Lin, and Shih-Chieh Chang

Transistor-Level Synthesis for Low-Power Applications 607
Dimitri Kagaris and Themistoklis Haniotakis

Assertion Checkers in Verification, Silicon Debug and In-Field Diagnosis 613
Marc Boulé, Jean-Samuel Chenard, and Zeljko Zilic

AMD EX1021
AMD v. Realtek - Page 196

Session 4C: Interconnects and Power Grids

Chair: **Murat Becer**, *CLK Design Automation*
Co-Chair: **Jeffrey Fan**, *West Virginia Univeristy Institute of Technology*

Self-Timed Regenerators for High-Speed and Low-Power Interconnect 621
Jae-Sun Seo, Prashant Singh, Dennis Sylvester, and David Blaauw

Efficient Analysis of Large-Scale Power Grids based on a Compact Cholesky Factorization 627
Hong Li, Jitesh Jain, Venkataramanan Balakrishnan, and Cheng-Kok Koh

General Block Structure-Preserving Reduced Order Modeling of Linear Dynamic Circuits 633
Ning Mi, Boyuan Yan, Sheldon X.-D. Tan, Jeffrey Fan, and Hao Yu

Investigating Crosstalk in Sub-Threshold Circuits 639
Mini Nanua and David Blaauw

Session 4D: Parametric Variations in Design

Chair: **David Pan**, *University of Texas*
Co-Chair: **Kiran Puttaswamy**, *Georgia Tech*

A Model for Timing Errors in Processors with Parameter Variation 647
Smruti R. Sarangi, Brian Greskamp, and Josep Torrellas

Parameter-Variation-Aware Analysis for Noise Robustness 655
Mosin Mondal, Kartik Mohanram, and Yehia Massoud

Future Prediction of Self-Heating in Short Intra-block Wires 660
Kenichi Shinkai, Masanori Hashimoto, and Takao Onoye

Thermal-Aware Placement for FPGAs Using Electrostatic Charge Model 666
Javid Jaffari and Mohab Anis

Luncheon Panel Discussion LP2

Do Digital Design and Variablity Mix Like Oil and Water? 672

Moderator: *Jacques Benkoski, USVP*
Organizer: *Michelle Clancy, Cayenne Communications*
Panelists: *Shankar Krishnamoorthy, Sierra Design Automation*
David Holt, Lightspeed Logic, Inc.
Ravi Subramanian, Berkeley Design Automation
Clive Bittlestone, Texas Instruments
Tsuyoshi Yamamoto, Fujitsu Microelectronics America
Andrew Kahng, Blaze DFM

Session 5A: DFM Statistics

Chair: **Jay Sivagnaname**, *IBM*
Co-Chair: **Scott Hector**, *Freescale Semiconductor*

An Exploratory Study on Statistical Timing Analysis and Parametric Yield Optimization 677
Ayhan Mutlu, Kelvin J. Le, Mustafa Celik, Dar-Sun Tsien, Garry Shyu, and Long-Ching Yeh

From Finance to Flip Flops: A Study of Fast Quasi-Monte Carlo Methods from Computational Finance Applied to Statistical Circuit Analysis 685
Amith Singhee and Rob A. Rutenbar

AMD EX1021
AMD v. Realtek - Page 197

Defect or Variation? Characterizing Standard Cell Behavior at 90nm and Below 693
Robert Aitken

A Data-Driven Statistical Approach to Analyzing Process Variation in 65nm SOI Technology 699
Choongyeun Cho, Daeik Kim, Jonghae Kim, Jean-Olivier Plouchart, Daihyun Lim, Sangyeun Cho, and Robert Trzcinski

Power, Delay and Yield Analysis of BIST/BISR PLAs Using Column Redundancy 703
Uthman Alsaiari and Resve Saleh

Session 5B: Timing Test and Reliability
Chair: **Sreejit Chakravarty**, *CSWITCH, Inc*
Co-Chair: **George Alexiou**, *University of Patras*

Small-Delay Defect Detection in the Presence of Process Variations 711
Rajeshwary Tayade, Savithri Sundareswaran, and Jacob Abraham

Function-Based Test Generation for (Non-Robust) Path Delay Faults Using the Launch-Off-Capture Scan Architecture 717
Rajsekhar Adapa, Edward Flanigan, Spyros Tragoudas, Michael Laisne, Hailong Cui, and Tsvetomir Petrov

On Accelerating Soft-Error Detection by Targeted Pattern Generation 723
Alodeep Sanyal, Kunal Ganeshpure, and Sandip Kundu

Enhanced Identification of Strong Robustly Testable Paths 729
Edward Flanigan and Spyros Tragoudas

Session 5C: Variation Analysis and Design
Chair: **Sarvesh H Bharadwaj**
Co-Chair: **Tom Jackson**, *Cadence Design*

Reducing the Complexity of VLSI Performance Variation Modeling Via Parameter Dimension Reduction 737
Zhuo Feng, Guo Yu, and Peng Li

Enablement of Variation-Aware Timing: Treatment of Parasitic Resistance and Capacitance 743
Ning Lu and Judy H. McCullen

Soft Clock Skew Scheduling for Variation-Tolerant Signal Processing Circuits: A Case Study of Viterbi Decoders 749
Yang Liu, Tong Zhang, and Jiang Hu

Adaptation to Temperature-Induced Delay Variations in Logic Circuits Using Low-Overhead Online Delay Calibration 755
Sivasubramaniam Krishnamurthy, Somnath Paul, and Swarup Bhunia

Designing and Validating Process-Variation-Aware Cell Libraries 761
Ali Dasdan, Jinfeng Liu, Sridhar Tirumala, and Kayhan Küçükçakar

Session 5D: Lithography and OPC
Chair: **Charlie Zhang**, *Synopsys*
Co-Chair: **Sheldon Tan**, *University of California, Riverside*

Transferring Optical Proximity Correction (OPC) Effect into Optical Mode 771
Jianliang Li, Qiliang Yan, and Lawrence S. Melvin

AMD EX1021
AMD v. Realtek - Page 198

OPC-Friendly De-Compaction with Timing Constraints for Standard Cell Layouts 776
Tetsuya Iizuka, Makoto Ikeda, and Kunihiro Asada

An Automated and Fast OPC Algorithm for OPC-Aware Layout Design 782
Ye Chen, Zheng Shi, and Xiaolang Yan

A New Method of Implementing Hierarchical OPC 788
Yufu Zhang and Zheng Shi

Session 6A: DFM Process

Chair: Larry Melvin, *Synopsys*
Co-Chair: Valeriy Sukharev, *Ponte*

A New Flexible Algorithm for Random Yield Improvement 795
Subarna Sinha, Qing Su, Linni Wen, Frank Lee, Charles Chiang, Yi-Kan Cheng, Jin-Lien Lin, and Yu-Chyi Harn

Increasing Manufacturing Yield for Wideband RF CMOS LNAs in the Presence of Process Variations 801
Arthur Nieuwoudt, Tamer Ragheb, Hamid Nejati, and Yehia Massoud

Defect Tolerance in Nanotechnology Switches Using a Greedy Reconfiguration Algorithm 807
S Ramsundar, Ahmad Al-Yamani, and Dhiraj K. Pradhan

Process Variation Tolerant Standard Cell Library Development Using Reduced Dimension Statistical Modeling and Optimization Techniques 814
Shubhankar Basu, Priyanka Thakore, and Ranga Vemuri

Redundant Via Insertion in Restricted Topology Layouts 821
Kevin McCullen

Session 6B: PDM Physical Planning

Chair: Rajeev Murgai, *Fujitsu Laboratories of America*
Co-Chair: Weiping Shi, *Texas A & M University*

Recursive Function Smoothing of Half-Perimeter Wirelength for Analytical Placement 829
Chen Li and Cheng-Kok Koh

Congestion Driven Buffer Planning for X-Architecture 835
Hongjie Bai, Sheqin Dong, and Xianlong Hong

Probabilistic Congestion Prediction with Partial Blockages 841
Zhuo Li, Charles J. Alpert, Stephen T. Quay, Sachin Sapatnekar, and Weiping Shi

OPC-Friendly Bus Driven Floorplanning 847
Hua Xiang, Liang Deng, Li-Da Huang, and Martin D.F. Wong

Power-Gating Aware Floorplanning 853
Hailin Jiang and Malgorzata Marek-Sadowska

Session 6C: Reliability and Interconnect at the System Level

Chair: Ahmed Eltawil, *University of California – Irvine*
Co-Chair: Artur Chojnacki, *PDF Solutions*

Optimizing Checking-Logic for Reliability-Agnostic Control of Self-Calibrating Designs 861
Frédéric Worm, Patrick Thiran, and Paolo Ienne

AMD EX1021
AMD v. Realtek - Page 199

An Infrastructure IP for Online Testing of Network-on-Chip Based SoCs 867
Praveen Bhojwani and Rabi N. Mahapatra

Provisioning On-Chip Networks under Buffered RC Interconnect Delay Variations 873
Mosin Mondal, Tamer Ragheb, Xiang Wu, Adnan Aziz, and Yehia Massoud

Virtual Channels Planning for Networks-on-Chip 879
Ting-Chun Huang, Umit Y. Ogras, and Radu Marculescu

A 3D-Layout Aware Binding Algorithm for High-Level Synthesis of Three-Dimensional Integrated Circuits 885
Vyas Krishnan and Srinivas Katkoori

Session 6D: Design and Modeling for Soft Error Reliabilty

Chair: **Keith Bowman**, *Intel*
Co-Chair: **Hamid Mahmoodi**, *San Francisco State University*

MARS-S: Modeling and Reduction of Soft Errors in Sequential Circuits 893
Natasa Miskov-Zivanov and Diana Marculescu

An SEU-Tolerant Programmable Frequency Divider 899
Liang Wang, Suge Yue, Yuanfu Zhao, and Long Fan

A TMR Scheme for SEU Mitigation in Scan Flip-Flops 905
Roystein Oliveira, Aditya Jagirdar, and Tapan J. Chakraborty

Variation Impact on SER of Combinational Circuits 911
K. Ramakrishnan, R. Rajaraman, S. Suresh, N. Vijaykrishnan, Y. Xie, and M.J. Irwin

MEMESTAR: A Simulation Framework for Reliability Evaluation over Multiple Environments 917
Christian J. Hescott, Drew C. Ness, and David J. Lilja

Author Index 923
Participating Organizations 928
Best Paper Award 929
ISQED 2008 Call for Papers 930

AMD EX1021
AMD v. Realtek - Page 200

This material may be protected by Copyright law (Title 17 U.S. Code)

Power-Gating Aware Floorplanning

Hailin Jiang
ECE Department, UCSB
hailin@ece.ucsb.edu

Malgorzata Marek-Sadowska
ECE Department, UCSB
mms@ece.ucsb.edu

Abstract

Power-gating is a technique for efficiently reducing leakage power by shutting off the idle blocks. However, the presence of power-gating may also introduce negative effects, which are not considered in the earlier design stages. Ignoring those effects may result in suboptimal designs and potentially even nullify the intended power savings. In this paper, we propose a novel measure to efficiently capture the power-gating effects. We apply this measure in a floorplanner for power-gated chips. Experimental results show that the power-gating aware floorplanner can achieve 50% decap saving compared to a floorplanner unaware of power gating. Leakage power can be saved by inserting less decap, especially when thin-oxide decap are used due to the area constraint. Our approach can reduce leakage power consumed by decap from 36mW to 9mW when area overhead is limited to about 19% of the total chip area.

1. Introduction

With continuous shrinking of the minimal feature size accompanied by lowering of supply and threshold voltages, leakage power is emerging as a major challenge for present and future CMOS designs. Power-gating is an efficient technique for reducing leakage power by shutting off the idle blocks. Implementation of power-gating requires a multi-threshold CMOS process. Logic blocks are implemented using low-V_t, high-performance transistors whereas high-V_t transistors (so called sleep transistors) connect the gated blocks to the power supply [5].

Power-gating is not a cost-free technique. In [3], the authors discuss and quantify the negative effects of power gating which include noise, performance penalty, area, and power overhead. Recently, physical design-level techniques have been developed to eliminate some of these negative effects. In [1], to reduce the magnitude of the voltage fluctuations, the authors propose to turn on the sleep transistors in a non-uniform, step-wise manner. In [4], the authors present an efficient algorithm for placing power gating switches in the voltage islands. Their objective is to meet the electrical requirements of a design while guaranteeing the design specifications of the switches and minimizing the area overhead.

However, all these works focus on designing the components of power-gating circuitry, such as sleep transistors. In other words, there is no mention whether the earlier design stages require any special considerations related to power gating. Floorplanning is an early stage of physical design deciding relative placement and physical dimensions of macros. Power-gating also works on the macro level. The candidate gated blocks are decided before floorpanning based on the functionality and performance of the circuits. However, there are several factors determined at the floorplanning (or placement) stage which affect the area and power of a gated circuit. They are the locations and neighbors of the gated blocks, the distances between gated- and non-gated blocks, placement of gated- and non-gated regions. Without considering the power-gating effects in floorplan, the negative aspects of power gating may overwhelm the potential gain and may make the technique not worth the effort. In this work, we present an efficient measure which captures power-gating effects in floorplan stage. We develop a power-gating driven floorplanner (PGFP) for designing power-gated chips. To the best of our knowledge, our work is the first addressing this problem.

The rest of this paper is organized as follows. In Section 2, we analyze the problems introduced by power-gating in the context of floorplanning and present a new metric to measure these effects. In Section 3, we describe our power-gating driven floorplanner. In Section 4, we show the experimental results. Section 5 concludes the paper.

2. Analysis of the problem

2.1. Power-gating

Traditionally, the on-chip power distribution network is constructed hierarchically. Power is delivered from the top-level metal layer, which is connected to the package, down through the internal layers, and finally to the active devices. The entire chip is fully powered at all times. In a power-gated system, the chip is divided into several domains and local power meshes are constructed for each of them. The local mesh for gated circuit is connected to the global mesh via sleep transistors. The sleep transistors are turned off to reduce the leakage power in a standby mode, and turned on in an active mode for normal operation.

When a block is active, the sleep transistor is turned on. Its size must be large enough to guarantee that the current drawn by the block does not cause excessive voltage drop. However, when large size sleep transistors are turned on and off, considerable power supply currents are drawn in a short period of time, which may result in large voltage fluctuations on the power grid. This *power-gating noise (PGN)* affects reliability of system-on-chips (SoCs), especially those manufactured in advanced CMOS tech-

0-7695-2795-7/07 $25.00 © 2007 IEEE

AMD EX1021
AMD v. Realtek - Page 201

nologies with narrow noise margins. We need to add extra decap to reduce the *PGN* and take into account additional leakage currents associated with the intentionally introduced capacitors.

In idle state, gated blocks are disconnected from the power supply, which prevents them from acting as decaps for the active circuits. Thus the non-gated blocks adjacent to the gated circuitry may need extra decap to guarantee that power grid noise remains within tolerable margins. The gated blocks not only stop providing decap to other blocks, but also act as obstacles for decap insertion. To eliminate the *PGN* in a gated chip, extra decap must be inserted which will enlarge the chip size and consume more leakage power.

The purpose of introducing power-gating is to save power. If the cost of power overhead caused by power gating is greater than the savings it provides, power-gating is useless. So our task is to reduce those negative effects as much as possible during each design stage to maximize the final power saving gained from the power-gating technique.

2.2. Floorplan effects on power-gating

To analyze the effect of a floorplan on power saving in a power-gated chip we use the example shown in Fig.1. The shaded area represents a gated-region with two blocks. We assume that each block has one sleep transistor. The block *B* has a higher current density (dark grey) than *A* (light grey). With the same distance of a gated-block to the gated-region boundary, upon wake-up, the higher current block (which has a larger sleep transistor) will cause a larger grid-current fluctuation for its neighbor non-gated circuits. With no other constraints, the floorplan in Fig.1(b) is better than the one in Fig.1(a) because it requires less extra decap. The locations of non-gated blocks also affect the power-gating result. With the same distance of non-gated blocks to the gated region boundary, during the wake-up period a higher current density block will be affected more. So we prefer a floorplan with block current densities decreasing towards the gated region boundary, from both gated and non-gated sides.

The shape of a gated region also affects the efficiency of power-gating. Suppose we have two gated regions of the same area but of different shapes as shown in Fig.1(c) and Fig1.(d). The floorplan in Fig.1(d) has a longer boundary between the gated and non-gated regions, which implies more boundary effects during the wake-up time. So without other constrains, we prefer a chip with gated-circuits placed close together.

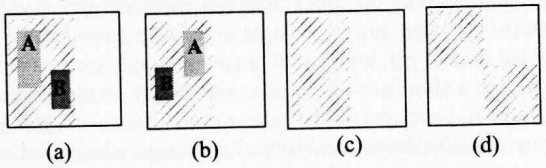


Figure 1. Floorplan effects on power-gating

2.3. Estimating decap in floorplan stage

Based on the observations discussed in Section 2.2, we propose a metric to predict the extra decap required by power-gating. For a given floorplan, we divide the chip into $M \times N$ bins. The bins occupied by gated blocks are labeled *gb*, and the bins occupied by non-gated blocks are labeled *ngb*. cd_i is the current density of a bin i, which is calculated as:

$$cd_i = \frac{\sum_{j=1}^{K_i} cd_{ij} \cdot a_{ij}}{A_i}$$

where cd_{ij} denotes current density of the jth block in the ith bin, and a_{ij} is the overlap area of the jth block and the ith bin. A_j is the bin area. K_i is the number of blocks in the ith bin. We also record the distances between the center of a gated (non-gated) bin and the nearest bins facing it on the north, south, west or east occupied by non-gated (gated) blocks. For example, in Fig.2, bin i is occupied by a gated block A. d_e and d_s are the distances between the center of i and the closet *ngb* on the east and south, respectively. We use the following formula to measure the extra decap required by introducing power-gating:

$$decapCost = \frac{gbinCost}{|totalBins|} + \frac{ngbinCost}{|ngBins|} \quad \text{(EQ 1)}$$

$$gbinCost = \sum_{i \in gbins} \sum_{k \in \{e, s, w, n\}} \sqrt{\frac{cd_i}{d_{ik}}}$$

$$ngbinCost = \sum_{i \in ngbins} \sum_{k \in \{e, s, w, n\}} \sqrt{\frac{cd_i}{d_{ik}}}$$

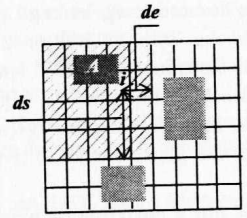


Figure 2. Measurement of extra decap

EQ1 is constructed such that if the higher current density blocks are placed closer to the boundary, the cost of extra power-gating decap is higher. The gated bin cost is divided by the total number of bins, and the cost of non-gated bins is divided by the number of non-gated bins, which implies that a smaller area of non-gated region requires larger decap area.

We test our metric on 100 power gated chips. The test chips are built in such a way that for a given floorplan, we choose randomly the locations and areas of gated circuits. The maximal number of gated regions is two. For each chip, we power gate the blocks in the gated regions and find the extra decap required to nullify the noise caused by power-gating. Then we compare the actual decap value with our metric. Fig.3 shows good correlation between the real decap insertion and our metric. We conclude that our metric can accurately capture the decap cost of

AMD EX1021
AMD v. Realtek - Page 202

power-gating and can be used to guide a floorplanner for power-gated chips.

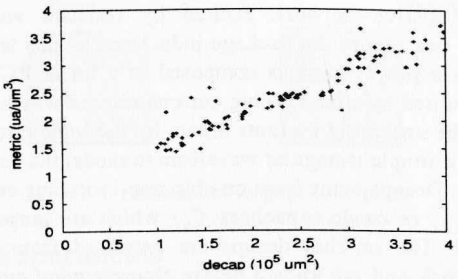


Figure 3. Correlation between our metric and real decap insertion

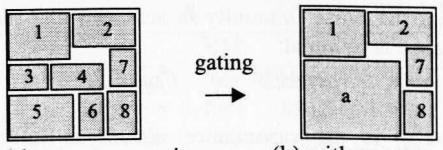
3. Power-gating driven floorplan

3.1. Sequence-pair

We use the sequence-pair representation of the floorplan topology. A sequence-pair (SP) of a module set M is a pair of sequences of the names of the modules in M. For example, $SP = (abc, bca)$ is a sequence-pair of $M = \{a, b, c\}$. An SP of M specifies the placement topology by the following rules:

- Horizontal constraint: $SP = (\ldots a \ldots b \ldots, \ldots a \ldots b \ldots)$, module a is on the left side of module b;
- Vertical constraint: $SP = (\ldots a \ldots b \ldots, \ldots b \ldots a \ldots)$, module a is above module b.

The gated blocks should be placed together. Those blocks are a subset of M and can be represented as a superinduce. We need two types of sequence-pairs to represent a power-gated floorplan: SupSP for all the non-gated modules and gated supermodules, and SubSP for the subset of modules in each supermodule. Fig.4 shows an example. If blocks 3, 4, 5, 6 are gated blocks, we group them together as a supermodule a. *SupSP* and *SubSP* are used to represent the floorplan in Fig.4(b).



(a) without power-gating (b) with power-gating

$SP = (12347568, 56834172)$ $SupSP = (12a78, a8172)$

$SubSP = (3456, 5634)$

Figure 4. floorplan represented by sequence-pair

In this paper we discuss the case of one gated supermodule, but our method can be extended to the case of many supermodules.

3.2. Simulated annealing

The problem of power-gating aware floorplan can be formulated as follows. Given a set of modules (soft/hard) with gating and connection information, find a floorplan which optimizes the following objective:

$$MIN\left[\sum_{i=1}^{M} area_i + totalWirelength + \alpha \cdot totalDecap\right] \quad \text{(EQ 2)}$$

where M is the number of modules and α is a scaling factor to make the third and the first two terms of the same magnitude. *totalDecap* can be estimated by EQ1. *totalWirelength* is measured as a summation of bounding boxes of all connections.

We implement simulated annealing process to solve the floorplan problem. Given $SP = (S1, S2)$, we allow the following moves:

- *Move1*: switch two modules in *S1*, which implies that *a-b* pair rotates by 90 degrees;
- *Move2*: switch two modules both in *S1* or both in *S2*, which implies that *a-b* pair rotates by 180 degrees;
- *Move3*: rotate an individual module.

Considering the supermodules included in a sequence-pair, we add the following rules:

- *Move1* or *Move2* can be applied on two non-gated modules;
- *Move1* or *Move2* can be applied on two suppermodules;
- *Move1* or *Move2* can be applied on a non-gated module and a suppermodule;
- *Move1* or *Move2* can be applied on two gated modules in the same supermodule;
- *Move2* can be applied on two gated modules in different supermodules with compatible gating schedules.

3.3. Sizing problem

Given a sequence-pair, we can determine the topology of a floorplan. Our objective is to find a geometric shape of each module minimizing the total area. The problem can be formulated as a geometric programming primal problem (PP):

$$\text{minimize:} \quad W \cdot H$$

$$\text{subject to:} \quad x_i + w_i \le x_j \qquad \forall e(i,j) \in G_H$$

$$y_i + \frac{A_i}{w_i} \le y_j \qquad \forall e(i,j) \in G_V$$

$$L_i \le w_i \le U_i \qquad i = 1, 2 \ldots N$$

where W and H are the chip width and height, respectively. A_i and w_i are the area and the width of a module i. x_i, y_i are the coordinates of a module i. L_i, U_i are the lower and upper bounds of the width w_i. $e(i,j)$ is an edge in the corresponding constraint graph (horizontal or vertical) for the sequence-pair.

We apply the Lagrangian Relaxation approach in [7] to solve this problem. We introduce Lagrange multipliers $\lambda_{i,j}$ and $\mu_{i,j}$ to incorporate constraints into the objective function. The following equations are repeatedly applied until w_i's converge.

$$w_i^* = sqrt\left(A_i \cdot \left(\sum_{e(i,j) \in G_V} \mu_{i,j}^k\right) \Big/ \left(\sum_{e(i,j) \in G_H} \lambda_{i,j}^k\right)\right)$$

AMD EX1021
AMD v. Realtek - Page 203

$$w^k = min\{U_i, max\{L_i, w^*\}\}$$
$$\lambda_{i,j}^{k+1} = max\{0, \lambda_{i,j}^k + \rho(x_i + w_i^k - x_j)\}$$
$$\mu_{i,j}^{k+1} = max\{0, \mu_{i,j}^k + \rho(y_i + A_i / w_i^k - y_j)\}$$

We assume that when power-gating is applied, the gated-blocks are individually power supplied. To maintain regularity of power mesh, the gated-blocks should be confined within a rectangular region. Fig.5 shows an example. For gated blocks 3,4,5,6 the floorplan of Fig.5(b) is better than the floorplan in Fig.5(a), even if the floorplan (a) is more compact.

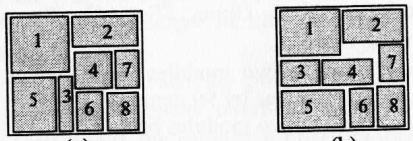


Figure 5. floorplan considering power-gating

3.4. Power-gating driven floorplanning algorithm

Our power-gating driven floorplan can be summarized as a two-step procedure embedded in simulated annealing process:

- Given a set of blocks of known areas, switching current profiles, aspect ratios, and gating status,
- Perform simulated annealing:
  - Random select a move; modules and supermodules are moved abiding to moving rules listed in Section 3.1;
  - **sizing-step1**: Calculate the shapes and relative locations of gated modules in a supermodule based on the approach discussed in Section 3.3;
  - **sizing-step2**: Calculate the shapes and locations of non-gated modules, and locations of supermoduls on the entire chip; supermodules are treated as hard modules;
  - Estimate the cost of the floorplan considering the power-gating effects quantified by EQ2;
  - Decide the acceptance of a move;
- Until the temperature has cooled down.

Experimental results reported in [7] show that applying sizing procedure only once at the end of the annealing process yields good result while running 50x faster as compared to sizing-with-annealing process. We apply the same idea in our floorplanner. We perform the two-step-planning in each iteration treating the modules as hard objects whose locations are updated. At the end of the annealing process we size the blocks. This strategy improves the run time dramatically whereas it still maintains the floorplan quality.

3.5. Decap insertion

To verify our floorplanning approach considering power-gating, we develop a tool to optimally insert decap to reduce power-gating noise. The model of a mesh is shown in Fig.6. The upper power mesh is modeled as a linear resistive network excited by constant voltage sources (we ignore the package inductance in this work). The lower power mesh is composed of a linear RC network excited by time-varying current sources which represent the switching currents drawn by the logic circuits. We use a simple triangular waveform to model the current profiles. Decaps come from on-chip non-switching capacitors C_{ckt} or oxide capacitors C_{ox} which are purposely inserted. The on-chip decaps are extracted from each logic block and are known before floorplanning and we assume that they are evenly distributed in each block. If C_{ckt} is not sufficient for noise immunity, more C_{ox} is added. In this work, we use both the thin oxide (9 $\mathring{A}$) and the thick oxide (13 $\mathring{A}$) C_{ox} modules. The thin-decap provides 44% more capacitance than the thick decap of the same area [2], but leaks more by an order of magnitude.

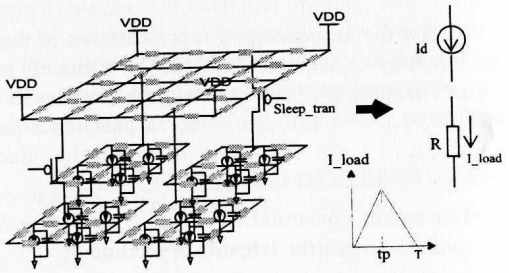


Figure 6. Power gating modeling

The model of sleep transistor depends on its mode of operation. When the sleep transistor is switching, it works in saturation mode and can be modeled as a current source with a triangle waveform. When a gated block is active, the sleep transistor which controls it works in the linear mode and can be modeled as a resistor. The optimization tool can be applied either on power-gated or non-gated chip, depending on if sleep transistor is modeled.

Given a floorplanned chip, we insert the extra decap such that the noise immunity is achieved and the total capacitance is minimal:

$$MIN \sum_{i=1}^{N} C_{OX}^i$$

where C_{OX}^i is the capacitance needed at location i, referred to as decap budget of decap i. N is the number of locations where decap can be inserted. We assume that decap can be inserted on the right and on the top of each block. So $N = 2M$, where M is the total number of blocks. We apply the algorithm described in [6] to solve this optimization problem.

Post-floorplan refinement might be implemented if the existing dead space is not enough for decap insertion. For example, in Fig.7(a), the required decap area is larger than the available dead space, so we extend the dead space in y direction (because δy is smaller than δx for the same area extension in this case) by moving macro 2. In this work, decap locations and decap budgets are deter-

AMD EX1021
AMD v. Realtek - Page 204

mined during the optimization step and do not change in post-floorplan step.

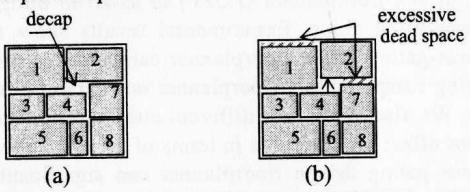


Figure 7. refinement in post-floorplan

4. Experiments

We used circuits from the MCNC and ISCAS benchmarks as basic macros and mapped them to the MCNC floorplan benchmarks. There are some floorplan benchmarks, such as *apte*, *xerox*, *hp*, which have too few macros (fewer than 11) to apply power-gating, so in this paper we show the results on *ami33* (33 macros) and *ami49* (49 macros). The switching current profiles are determined by simulating each circuit and approximating current waveforms by waveforms of triangular shape. The connections among the macros are taken from the *ami33* and *ami49* data sets.

We integrated C++ with TCL to implement our power-gating driven floorplanner. We ran all the experiments on a P4 2.4GHz PC with Linux. The test circuits were implemented in 0.13 μm technology. The temperature was 25° C.

We selected the gating status of macros in several ways to illustrate various situations. In this experiment, we applied five gating schedules: (g1) gated macros were selected randomly; (g2) high current density macros were gated; (g3) low current density macros were gated; (g4) tightly connected macros were gated, and (g5) weakly connected macros were gated. In each case, the gated macros occupied half of the chip area.

For each gating schedule, we implemented the following three floorplanning procedures:

- Regular floorplan (RFP): we applied the traditional non-slicing floorplan approach [7] on no-power-gated chips.
- Two-step-sizing floorplan (TSSFP): we implemented our two-step-sizing floorplan procedure to group the gated macros together, but we ignored the metric of gating effects in the cost function EQ2.
- Power-gating driven floorplan: (PGFP): we repeated the two-step-sizing procedure taking the gating effects into account.

Table 1 lists the comparison results in terms of dead space, run time, and decap budget, respectively. Dead space indicates the area not occupied by macros and we report it as percentage of the total area. Decap budget is the amount of capacitance required for achieving noise-immune chips. Not all dead space is used for decap insertion.

Comparing with no-power-gating floorplanning, the power-gating floorplanning (including both TSSFP and PGFP) costs more dead space. However, dead space can be utilized to insert decap, if necessary. Generally, power-gating driven floorplan saves more decap on gating high current density macros (g2) and gating tightly connected macros (g4), comparing with floorplanner unaware of power-gating. Decap increases by about 20% for power-gating without considering it at the floorplan stage. Experimental results show that our approach can decrease this number to 10%, which implies leakage power saving from inserting less decap.

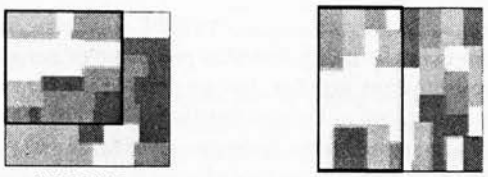
Fig.8 shows the floorplan results with and without considering power-gating. Gated macros are contained inside the marked bounding box. We use colors from light to dark to show the distribution of current densities on the chip. The area colored light implies low current density and the area colored dark implies high current density. By applying power-gating driven floorplanning, more of the lower-current-density-macros are placed close to the boundary. The floorplanner tries to reduce as much as

Table 1. Comparison among floorplanners

		RFP			TSSFP			PGFP			decap budget	
		dead space (%)	run time (s)	decap budget (pf)	dead space (%)	run time (s)	decap budget (pf)	dead space (%)	run time (s)	decap budget (pf)	TSSFP vs. RFP	PGFP vs. RFP
ami33	g1	0.4	54	579	2.1	27	667	4.2	83	620	1.15	1.07
	g2				1.9	27	689	4.2	94	642	1.19	1.11
	g3				2.2	27	648	3.9	89	614	1.12	1.06
	g4				1.3	28	677	3.3	82	619	1.17	1.07
	g5				2.5	27	671	3.8	96	625	1.16	1.08
ami49	g1	2.4	415	722	13.3	354	888	18.1	501	801	1.23	1.11
	g2				13.5	363	902	17.3	519	808	1.25	1.12
	g3				14.2	369	859	19.7	526	794	1.19	1.10
	g4				8.7	349	895	16.2	498	794	1.24	1.10
	g5				14.8	377	873	19.2	512	823	1.21	1.14
aver											1.19	1.09

AMD EX1021
AMD v. Realtek - Page 205

possible the length of the boundary between the gated and non-gated regions.



(a)TSSFP (b) PGFP

Figure 8. Current distribution of gating chip (ami33)

In the post-floorplan step, we allocate/extend the dead space for extra decap insertion. We configure our decap usage in such a way that we keep the capacitance at each location the same but we change the ratio between the thin- and thick-oxide decaps. Noise is not affected by different configurations because the capacitance does not change. Configuration of 100% thin-oxide decaps can achieve minimal area but consumes the most leakage power. Configuration of 100% thick-oxide can save the most power but also costs the most area. Given the dead space constraint, we compare our power-gating driven floorplanner with a floorplanner unaware of power-gating under different decap configurations. Table 2 reports the results. Column 1 shows the dead space constraint, Columns 2 and 4 show the leakage power consumption of decap, columns 3 and 5 show the decap configuration for the thin-oxide decap usage. We notice that if the dead space is too small, PGFP cannot provide feasible solution because it always consumes more dead space than TSSFP. However, if a design allows certain ratio of dead space, the power-gating driven floorplan may save much more power than a floorplan unaware of power-gating. For example, if the decap space constraint is 19% of the total area, the leakage power consumption is 36.1 mW by applying TSSFP whereas it is 9.2 mW by applying PGFP, which results in 26.9 mW saving of leakage power. We also notice that designs favor using thick-oxide decap as much as possible to reduce leakage power if area is not a concern.

Table 2. Leakage power with different decap configuration under dead space constraint(ami49)

dead space (%)	TSSFP		PGFP		power saving (mw)
	power (mw)	thin_oxide usage (%)	power (mw)	thin_oxide usage (%)	
13	93.2	100	N/A	N/A	N/A
17	60.0	60	39.4	40	21.6
18	49.3	50	24.3	20	25.0
19	36.1	30	9.2	0	26.9
22	10.2	0	N/A	N/A	N/A

5. Conclusions

In this work, we explore the power-gating technique and present an efficient measure for predicting power-gating effects in floorplan stage. We develop a power-gating driven floorplanner (PGFP) to assist in designing of power-gated chips. Experimental results show that the power-gating aware floorplanner can achieve 50% decap saving compared to a floorplanner unaware of power gating. We also study how different configurations of decap types affect the floorplan in terms of area and power. Our power-gating driven floorplanner can significantly save power when area constraints are imposed by the design. We believe that in future designs with technology scaling down, power-gating will become a standard technique. Considering power-gating in early design stages will become necessary.

6. Acknowledgements

This work was supported in part by SRC grant # 1069 and in part by MICRO through IBM. We gratefully acknowledge equipment grant from Intel.

7. Reference

[1] K.Choi, Y.Xu and T.Sakura, "An effective yet feasible power-gating scheme achieving two orders of magnitude lower standby leakage", *Symposium on VLSI Circuits*, pp.312-315, 2005.

[2] H.H.Chen, J.S.Neely, and M.F.Wang, "On-chip decoupling capacitor optimization for noise and leakage reduction", *Proc. Symposium on Integrated Circuits and System Design*, pp.251-255, 2003

[3] H.Jiang, M.Marek-Sadowska, S.R.Nassif, "Benefits and costs of power-gating technique", *Proc. ICCD,* pp.559-566, 2005

[4] J.N.Kozhaya, L.A.Bakir, "An electrically robust method for placing power gating switches in voltage islands", *Proc. CICC,* pp321-324, 2004

[5] S.Mutoh and et al, "A 1V power supply high-speed digital circuit technology with multi threshold voltage CMOS", *IEEE Journal of Solid-State Circuit,* pp. 847-854, 1995

[6] H.Su, S. S. Sapatnekar, and S.R.Nassif, "Optimal decoupling capacitor sizing and placement for standard-cell layout designs", *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems,* pp. 428-436, April, 2003

[7] F.Y.Young, C.N.Chu and Y.C.Wong, "Handling soft modules in general nonslicing floorplan using Lagrangian Relaxation", *IEEE Trans on Computer-Aided Design of Integrated Circuits and Systems*, vol.20, pp.687-692, 2001

[8] S.Zhao, K.Roy and C.K.Koh, "Decoupling capacitance allocation and its application to power-supply noise-aware floorplanning", *IEEE Trans on Computer-Aided Design of Integrated Circuits and Systems*, vol.21, pp.81-92, 2002

AMD EX1021
AMD v. Realtek - Page 206

ATTACHMENT 4A

```
001    995176233405961
005    20080506134200.0
008    070606s2007    caua     b    101 0 eng d
020    ##$a9780769527956
020    ##$a0769527957
035    ##$a(OCoLC)138289590
035    ##$9728127
035    ##$a(MoKL)517623-lhalldb
035    ##$a(lhalldb)517623-lhalldb
040    ##$aLHL $cLHL
049    ##$aLHLA
090    ##$aTK7874.75 $b.I565 2007
111    2#$aInternational Symposium on Quality Electronic Design
$n(8th : $d2007 : $cSan Jose, Calif.)
245    10$aEighth International Symposium on Quality Electronic
Design : $bISQED 2007 : proceedings : San Jose, California : 26-28
March, / $ctechnical sponsors, IEEE Electron Device[s] Society ;
cooperating entities, IEEE EDS ... [et al.] ; corporate & media
sponsors, Synopsys' ... [et al.]
246    30$a8th International Symposium on Quality Electronic Design
246    30$aInternational Symposium on Quality Electronic Design
246    30$aQuality Electronic Design
246    30$aISQED 2007
260    ##$aLos Alamitos, California : $bIEEE Computer Society,
$cc2007.
300    ##$axxv, 929 p. : $bill. ; $c28 cm.
500    ##$a"IEEE Computer Society Order Number P2795"--T.p. verso.
504    ##$aIncludes bibliographic references and author index.
650    #0$aIntegrated circuits $xVery large scale integration
$xReliability. $vCongresses.
650    #0$aIntegrated circuits $xVery large scale integration
$xDesign and construction $vCongresses
650    #0$aIntegrated circuits $xVery large scale integration
$xComputer-aided design $vCongresses
650    #0$aIntegrated circuits $xVery large scale integration
$xTesting $xQuality control $vCongresses.
710    2#$aIEEE Electron Devices Society
710    2#$aIEEE Circuits and Systems Society
710    2#$aSynopsys (Firm)
948    ##$aLTI 09/01/2008
```

ATTACHMENT 4B

OCLC 138289590 **No holdings in XXX - 5 other holdings**

Books

						Rec Stat		**Entered**	20070606	**Replaced**	20220610085137.4
Type	a	**ELvl**		**Srce**	d	**Audn**		**Ctrl**		**Lang**	eng
BLvl	m	**Form**		**Conf**	1	**Biog**		**MRec**		**Ctry**	cau
		Cont	b	**GPub**		**LitF**	0	**Indx**	1		
Desc	a	**Ills**	a	**Fest**	0	**DtSt**	s	**Dates**	2007 ,		

010 2006939397
040 LHL $b eng $c LHL $d DLC $d OCLCQ $d OCLCO $d OCLCQ $d OCLCA $d OCLCF $d UKMGB $d OCLCQ $d OCLCO
016 7 014543993 $2 Uk
020 0769527957
020 9780769527956
050 00 TK7874.75 $b .I586 2007
082 00 621.39/5 $2 22
090 $b
111 2 International Symposium on Quality Electronic Design $n (8th : $d 2007 : $c San Jose, Calif.)
245 10 Eighth International Symposium on Quality Electronic Design : $b ISQED 2007 : proceedings : San Jose, California : 26-28 March / $c technical sponsors, IEEE Electron Device[s] Society ; cooperating entities, IEEE EDS [and others] ; corporate & media sponsors, Synopsys' [and others].
246 30 8th Seventh International Symposium on Quality Electronic Design
246 30 International Symposium on Quality Electronic Design
246 30 Quality Electronic Design
246 30 ISQED 2007
260 Los Alamitos, Calif. : $b IEEE Computer Society, $c ©2007.
300 xxv, 929 pages : $b illustrations ; $c 28 cm
336 text $b txt $2 rdacontent
337 unmediated $b n $2 rdamedia
338 volume $b nc $2 rdacarrier
500 "IEEE Computer Society Order Number P2795"--Title page verso
504 Includes bibliographical references and author index.
540 Current copyright fee: GBP26.40 $c 32\0. $5 Uk
650 0 Integrated circuits $x Very large scale integration $x Reliability $v Congresses.
650 0 Integrated circuits $x Very large scale integration $x Design and construction $v Congresses.
650 0 Integrated circuits $x Very large scale integration $x Computer-aided design $v Congresses.
650 0 Integrated circuits $x Very large scale integration $x Testing $x Quality control $v Congresses.
650 6 Circuits intégrés à très grande échelle $0 (CaQQLa)201-0117255 $x Fiabilité $0 (CaQQLa)201-0379337 $v Congrès. $0 (CaQQLa)201-0378219
650 6 Circuits intégrés à très grande échelle $0 (CaQQLa)201-0117255 $x Conception assistée par ordinateur $0 (CaQQLa)201-0380628 $v Congrès. $0 (CaQQLa)201-0378219
650 7 Integrated circuits $x Very large scale integration $x Computer-aided design. $2 fast $0 (OCoLC)fst00975604
650 7 Integrated circuits $x Very large scale integration $x Design and construction. $2 fast $0 (OCoLC)fst00975610

650 7 Integrated circuits $x Very large scale integration $x Reliability. $2 fast $0 (OCoLC)fst00975615
653 1 Quality electronic design
653 1 ISQED
655 7 Conference papers and proceedings. $2 fast $0 (OCoLC)fst01423772
710 2 IEEE Electron Devices Society.
710 2 IEEE Circuits and Systems Society.
710 2 Synopsys (Firm)
856    $3 1850-9999 $u http://ieeexplore.ieee.org/Xplore/home.jsp $x BLDSS

ATTACHMENT 4C

LIBRARY OF CONGRESS AUTHORITIES

LC control no.: sh 85067125

LCCN Permalink: https://lccn.loc.gov/sh85067125

HEADING: Integrated circuits Very large scale integration

000 00483cz a2200181n 450
001 4718173
005 20120326100531.0
008 860211i| anannbabn |b ana
010 __ |**a** sh 85067125
035 __ |**a** (DLC)sh 85067125
035 __ |**a** (DLC)64858
040 __ |**a** DLC |**c** DLC |**d** DLC
053 _0 |**a** TK7874.75
150 __ |**a** Integrated circuits |**x** Very large scale integration
450 __ |**a** Very large scale integration of circuits
450 __ |**a** VLSI circuits
906 __ |**t** 9334 |**u** te04 |**v** 0
953 __ |**a** xx00 |**b** jg12

Previous Next

Save, Print or Email Records (View Help)

Select Download Format: Text (Labelled Display) Press to SAVE or PRINT

Email Text (Labelled Display) to:

Press to SEND EMAIL

Library of Congress
URL: https://www.loc.gov/

Mailing Address:
101 Independence Ave, S.E.
Washington, DC 20540

Library of Congress Authorities
URL: http://authorities.loc.gov/
Library of Congress Online Catalog
URL: https://catalog.loc.gov/

Questions, comments, error reports: Contact Us

AMD EX1021
AMD v. Realtek - Page 213

ATTACHMENT 4D

LIBRARY OF CONGRESS AUTHORITIES

LC control no.: sh 85112510
LCCN Permalink: https://lccn.loc.gov/sh85112510
HEADING: Reliability

000 00493cz a2200193n 450
001 4761965
005 20130830055925.0
008 860211|| anannbabn |a ana
010 __ |**a** sh 85112510
035 __ |**a** (DLC)sh 85112510
035 __ |**a** (DLC)108650
040 __ |**a** DLC |**c** DLC |**d** DLC
150 __ |**a** Reliability
450 __ |**a** Dependability
450 __ |**a** Trustworthiness
550 __ |**w** g |**a** Conduct of life
906 __ |**t** 64-- |**u** ---- |**v** 0
910 __ |**a** Record saved by tc03 on 08/29/2013 at 09:52:29
953 __ |**a** xx00 |**b** td14

Previous Next

Save, Print or Email Records (View Help)

Select Download Format: Text (Labelled Display) Press to SAVE or PRINT

Email Text (Labelled Display) to: Press to SEND EMAIL



Library of Congress
URL: https://www.loc.gov/

Mailing Address:
101 Independence Ave, S.E.

Library of Congress Authorities
URL: http://authorities.loc.gov/
Library of Congress Online Catalog
URL: https://catalog.loc.gov/

Questions, comments, error reports: Contact Us

AMD EX1021
AMD v. Realtek - Page 215

Washington, DC 20540