

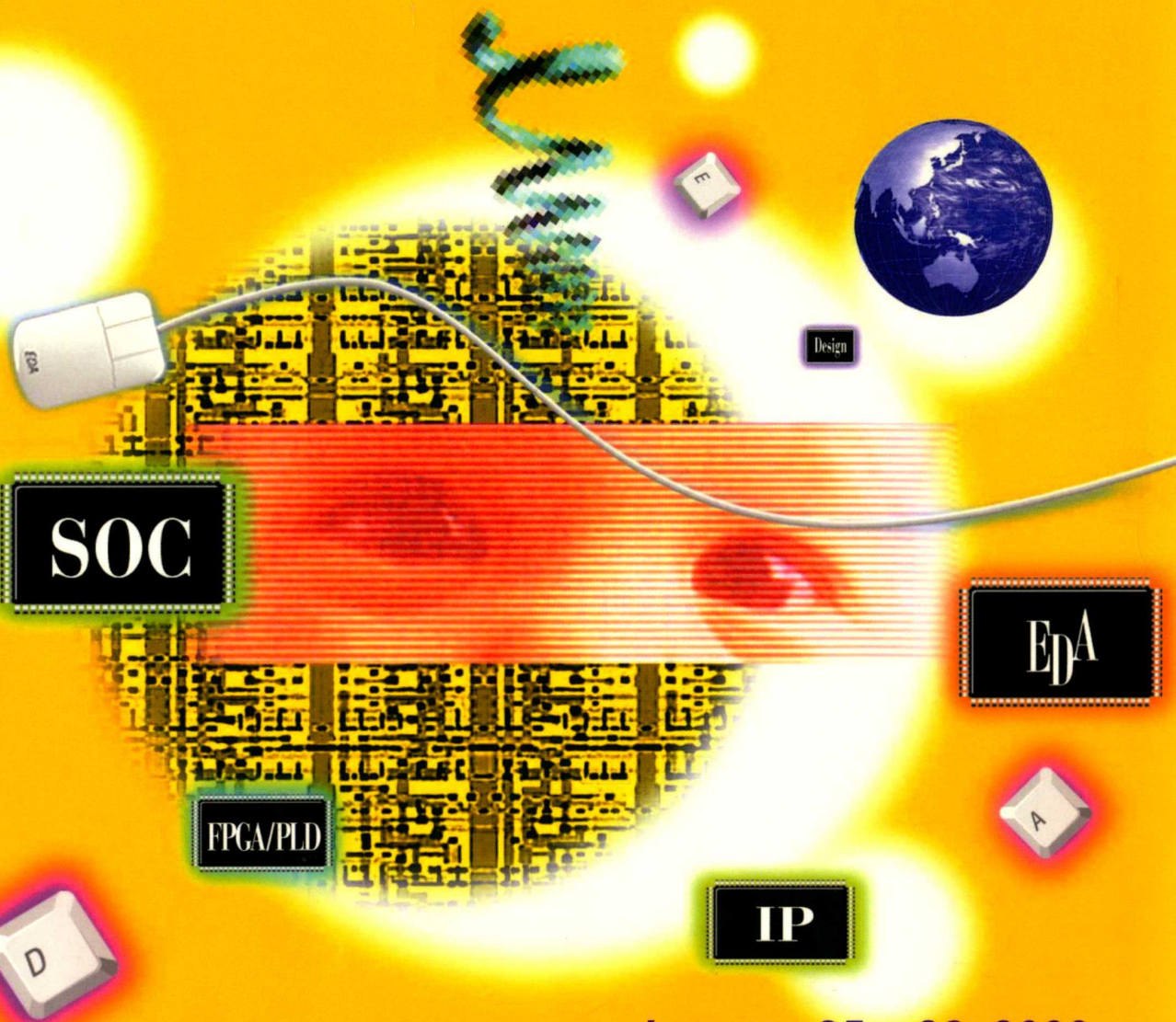
ATTACHMENT 10

ASP-DAC 2000

Asia and South Pacific Design Automation Conference 2000

with

EDA TechnoFair 2000



January 25 – 28, 2000
Pacifico Yokohama
Yokohama, Japan

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Proceedings of the ASP-DAC 2000

**Asia and South Pacific Design Automation Conference
2000**

**January 25 – 28, 2000
Pacifico Yokohama
Yokohama, Japan**

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Table of Contents

Organizing Committee	iii
Steering Committee	vi
General Chair's Message	x
Technical Program Committee	xi
Technical Program Co-Chair's Message	xv
Best Paper Award Candidates	xvi
University LSI Design Contest Committee	xvii
University LSI Design Contest Co-Chair's Message	xviii
University LSI Design Contest Summary	xix
University LSI Design Contest Awards	xx
Keynote Addresses	xxi
EDA Vendor Executive Panel	xxii

Session A1 (Special Session) University LSI Design Contest

Co-Chairs : *Ryota Kasai – NTT, Japan*
 Anantha Chandrakasan – MIT, USA

A1.1	A VLSI Implementation of the Blowfish Encryption/Decryption Algorithm	
	<i>Michael C.-J. Lin, Youn-L. Lin</i>	<i>1</i>
A1.2	VLSI Implementation of Rake Receiver for IS-95 CDMA Testbed using FPGA	
	<i>Oliver Y-h. Leung, Chi-Y.Tsui, Roger S. Cheng</i>	<i>3</i>
A1.3	VLSI Implementation of a Switch Fabric for Mixed ATM and IP Traffic	
	<i>Chi-Y. Tsui, Louis Chung-Y. Kwan, Chin-T. Lea</i>	<i>5</i>
A1.4	Design of Digital Neural Cell Scheduler for Intelligent IB-ATM Switch	
	<i>J.Lee, S. Lee, M.Lee, D.Lee, Y.Kim, S.Jeong</i>	<i>7</i>
A1.5	Genetic Algorithm Accelerator GAA-II	
	<i>Shin'ichi Wakabayashi, Tetsuhi Koide, Nayoshi Toshine, Masataka Yamane, Hajime Ueno</i>	<i>9</i>
A1.6	A Programmable Built-In Self-Test Core for Embedded Memories	
	<i>Chih-T. Huang, Jing-R. Huang, Cheng-W. Wu</i>	<i>11</i>
A1.7	An Algorithm for VLSI Implementation of Highly Efficient Cubic-Polynomial Evaluation	
	<i>Fan Mo, Yiha Zhang, Jun Yu, Qianling Zhang</i>	<i>13</i>

A1.8	Design of Self-timed Asynchronous Booth's multiplier	
	<i>Tin-Y. Tang, Chin-S. Choy, Pui-L. Siu, Cheong-F. Chan</i>	15
A1.9	High Speed and Ultra-Low Power 16x16 MAC Design using TG for Web-based Multimedia System	
	<i>Seung-M. Lee, Jin-H. Chung, Hyung-S. Yoon, Mike M-O. Lee</i>	17
A1.10	A Smart Imager for the Vision Processing Front-END	
	<i>Naoki Takeda, Mitsuru Homma, Makoto Nagata, Takashi Morie, Atsushi Iwata</i>	19
A1.11	A Binary Image Sensor with Flexible Motion Vector Detection using Block Matching Method	
	<i>Tomohiro Nezuka, Takafumi Fujita, Makoto Ikeda, Kunihiro Asada</i>	21
A1.12	An Arbitrary Chaos Generator Core Circuit Using PWM/PPM Signals	
	<i>Kenichi Murakoshi, Takashi Morie, Makoto Nagata, Atushi Iwata</i>	23
A1.13	An Application Specific Java Processor with Reconfigurabilities	
	<i>Shinji Kimura, Hiroyuki Kida, Kazuyoshi Takagi, Tatsumori Abematsu, Katsumasa Watanabe</i>	25
A1.14	Reconfigurable Synchronized Dataflow Processor	
	<i>Hiroshi Sasaki, Hitoshi Maruyama, Hideaki Tsukioka, Nobuyoshi Shoji, Hiroaki Kobayashi, Tadao Nakamura</i>	27
A1.15	Prototype Microprocessor LSI with Scheduling Support Hardware for Operating System on Multiprocessor System	
	<i>Naoki Nishimura, Takahiro Sasaki, Tetsuo Hironaka</i>	29
A1.16	A Floating Point Arithmetic Unit for a Static Scheduling and Compiler Oriented Multiprocessor System ASCA	
	<i>Takahiro Kawaguti, Takayuki Suzuki, Hideharu Amano</i>	31
A1.17	A 16bit redundant binary multiplier using low-power pass-transistor logic SPL	
	<i>Hirofumi Sakamoto, Ken'ichiro Uda, Bu-Y. Lee, Hiroyuki Ochi, Kazuo Taki, Takao Tsuda</i>	33
A1.18	An 8x8 nRERL Serial Multiplier for Ultra-Low-Power Applications	
	<i>Joonho Lim, Dong-G. Kim, Sang-C. Kang, Soo-I. Chae</i>	35

Session B1 IP Reuse and Protection Methods

Co-Chairs : *Graham R. Hellestrand – VaST Systems Technology Corp., USA*
Minoru Yamamoto – Fujitsu Ltd., Japan

B1.1	Embedded Tutorial: Essential Issues for IP Reuse	
	<i>Daniel D. Gajski, Viraphol Chaiyakul, Allen C.-H. Wu, Shojiro Mori, Tom Nukiyama, Larry Rosenberg</i>	37
B1.2	Usage-Based Characterization of Complex Functional Blocks for Reuse in Behavioral Synthesis	
	<i>Nong Fan, Viraphol Chaiyakul, Daniel D. Gajski</i>	43
B1.3	Reuse and Protection of Intellectual Property in the SpecC System	
	<i>Rainer Doemer, Daniel D. Gajski</i>	49
B1.4	Fair Watermarking Techniques	
	<i>Gang Qu, Jennifer L. Wong, Miodrag Potkonjak</i>	55

Session C1 Decision Diagrams and Verification Methods

Co-Chairs : *Yirng-An Chen – National Chiao Tung Univ., Taiwan*
 Kiyoharu Hamaguchi – Osaka Univ., Japan

C1.1	An Efficient Heuristic for State Encoding Minimizing the BDD Representations of the Transition Relations of Finite State Machines	
	<i>Riccardo Forth, Paul Molitor</i>	61
C1.2	Automatic Partitioning for Efficient Combinational Verification	
	<i>Rajarshi Mukherjee, Jawahar Jain, Koichiro Takayama, Masahiro Fujita</i>	67
C1.3	A Hardware Simulation Engine Based on Decision Diagrams (Short Paper)	
	<i>Yukihiro Iguchi, Tsutomu Sasao, Munehiro Matsuura, Atsumu Iseno</i>	73
C1.4	Formal Verification based on Assume and Guarantee Approach - A Case Study (Short Paper)	
	<i>Subir K. Roy, Hiroaki Iwashita, Tsuneo Nakata</i>	77
C1.5	Multi-Clock Path Analysis Using Propositional Satisfiability	
	<i>Kazuhiro Nakamura, Shinji Maruoka, Shinji Kimura, Katsumasa Watanabe</i>	81

Session D1 Routing in Deep-Submicron

Co-Chairs : *Jason Cong – Univ. of California, Los Angeles, USA*
 Takumi Okamoto – NEC Corp., Japan

D1.1	Self-Reforming Routing for Stochastic Search in VLSI Interconnection Layout	
	<i>Yukiko Kubo, Yasuhiro Takashima, Shigetoshi Nakatake, Yoji Kajitani</i>	87
D1.2	An Interconnect Topology Optimization by a Tree Transformation	
	<i>Naofumi Tsujii, Katsutoshi Baba, Shuji Tsukiyama</i>	93
D1.3	Timing-Driven Hierarchical Global Routing with Wire-Sizing and Buffer-Insertion for VLSI with Multi-Routing-Layer	
	<i>Takahiro Deguchi, Tetsushi Koide, Shin'ichi Wakabayashi</i>	99
D1.4	Area Routing Oriented Hierarchical Corner Stitching with Partial Bin	
	<i>Zhang Yan, Wang Baohua, Cai Yici, Hong Xianlong</i>	105

Session A2 (Special Session) CAD for Embedded Systems

Chair : *Miodrag Potkonjak – Univ. of California, Los Angeles, USA*

A2.1	Offline Program Re-mapping to Improve Branch Prediction Efficiency in Embedded Systems	
	<i>Stephen S. Brown, Jeet Asher, William H. Mangione-Smith</i>	111
A2.2	Timing Driven Co-design of Networked Embedded Systems	
	<i>Dinesh Ramanathan, Ravindra Jejurikar, Rajesh K. Gupta</i>	117
A2.3	Low-power Design Methodology and Applications utilizing Dual Supply Voltages	
	<i>Kimiyoshi Usami, Mutsunori Igarashi</i>	123
A2.4	Co-Synthesis with custom ASICs	
	<i>Yuan Xie, Wayne Wolf</i>	129

Session B2 System-Level Power Optimization & Estimation

Co-Chairs : Akira Matsuzawa – Matsushita Electrical Industrial, Co. Ltd., Japan
Masato Edahiro – NEC Corp., Japan

B2.1	A New Method for Constructing IP Level Power Model Based on Power Sensitivity	
	<i>Heng-Liang Huang, Jiing-Yuan Lin, Wen-Zen Shen, Jing-Yang Jou</i>	135
B2.2	A hybrid approach for core-based system-level power modeling	
	<i>Tony Givargis, Frank Vahid, Joerg Henkel</i>	141
B2.3	Voltage Reduction of Application-Specific Heterogeneous Multiprocessor Systems for Power Minimisation	
	<i>Allan Rae, Sri Parameswaran</i>	147
B2.4	Withdrawn	
B2.5	Synthesis of Low Power Folded Programmable Coefficient FIR Digital Filters (Short Paper)	
	<i>Vijay Sundararajan, Keshab K. Parhi</i>	153

Session C2 Design Environment for FPGA

Co-Chairs : Shinji Kimura – Nara Inst. of Science and Technology, Japan
Kazutoshi Wakabayashi – NEC Corp., Japan

C2.1	Invited Talk : Synthesis Challenges for Next-Generation High-Performance and High-Density PLDs	
	<i>Jason Cong, Songjie Xu</i>	157
C2.2	KressArray Xplorer: A New CAD Environment to Optimize Reconfigurable Datapath Array Architectures	
	<i>Reiner Hartenstein, Michael Herz, Thomas Hoffmann, Ulrich Nageldinger</i>	163
C2.3	Hardware-Software Cosynthesis for Run-time Incrementally Reconfigurable FPGAs	
	<i>Byungil Jeong, Sungjoo Yoo, Sunghyun Lee, Kiyoun Choi</i>	169

Session D2 Placement Consistent with Routing

Co-Chairs : Yu-Liang Wu – Chinese University of Hong Kong, China
Hiroshi Murata – Microark, Japan

D2.1	A New Encoding Scheme for Rectangle Packing Problem	
	<i>Toshihiko Takahashi</i>	175
D2.2	Analytical Minimization of Half-Perimeter Wirelength	
	<i>Andrew A. Kennings, Igor L. Markov</i>	179
D2.3	Modeling and Minimization of Routing Congestion	
	<i>Maogang Wang, Majid Sarrafzadeh</i>	185

Session E2 (Special Session) System-In-Package (SIP)

Chair : Wayne W.-M. Dai – Univ. of California, Santa Cruz, USA

E2.1	System-In-Package (SIP): Challenges and Opportunities	
	<i>King L. Tai</i>	191
E2.2	Taiwan Foundry for System-In-Package (SIP)	
	<i>Albert Lin</i>	197
E2.3	Integration of Large-Scale FPGA and DRAM in a Package Using Chip-On-Chip Technology	
	<i>Michael X. Wang, Katsuharu Suzuki, Wayne W.-M. Dai, Yee L. Low, Kevin J. O'conner, King L. Tai</i>	205
E2.4	Modeling and Analysis of Integrated Spiral Inductors for RF System-In-Package	
	<i>Minqing Liu, Wayne W.-M. Dai</i>	211

Session A3 Low Power Design : Implementation

Co-Chairs : Shoji Kawahito – Toyohashi Univ. of Technology, Japan
Jan M. Rabaey – Univ. of California, Berkeley, USA

A3.1	Narrow Bus Encoding for Low Power Systems	
	<i>Youngsoo Shin, Kiyoun Choi</i>	217
A3.2	Data Transmission over a Bus with Peak-Limited Transition Activity	
	<i>Vijay Sundararajan, Keshab K. Parhi</i>	221
A3.3	Power Analysis and Implementation of a Low-Power 300 MHz 8-b x 8-b Pipelined Multiplier	
	<i>Jinn-Shyan Wang, Po-Hui Yang</i>	225

Session B3 Embedded Software

Co-Chairs : Peter Marwedel – Univ. of Dortmund, Germany
Hiroaki Takada – Toyohashi University of Technology, Japan

B3.1	A New Approach to Assembly Software Retargeting for Microcontrollers	
	<i>Ing-Jer Huang, Dao-Zhen Chen</i>	229
B3.2	Register Allocation for Common Subexpressions in DSP Data Paths	
	<i>Rainer Leupers</i>	235
B3.3	A Technique for QoS-based System Partitioning	
	<i>Johnson S. Kin, Chunho Lee, William H. Mangione-Smith, Miodrag Potkonjak</i>	241
B3.4	FSM Decomposition by Direct Circuit Manipulation Applied to Low Power Design	
	<i>Samuel Wu, Jian Wei, Maximal Peurum, Qing Wu</i>	345
B3.5	Low Power Design of Sequential Circuits Using A Quad-Synchronous Design	
	<i>Joao C. Monteiro, Arlindo L. Oliveira</i>	351

Session C3 Implementation of Boolean Functions

Co-Chairs : Yusuke Matsunaga – Fujitsu Laboratories, Ltd., Japan
Hiroyuki Ochi – Hiroshima City Univ., Japan

C3.1	Exact minimization of fixed polarity Reed-Muller expressions for incompletely specified functions	
	<i>Debatosh Debnath, Tsutomu Sasao</i>	247
C3.2	An Efficient Framework of Using Various Decomposition Methods to Synthesize LUT Networks and Its Evaluation	
	<i>Shigeru Yamashita, Hiroshi Sawada, Akira Nagoya</i>	253
C3.3	Three Parameters to Find Functional Decompositions	
	<i>Tsutomu Sasao, Ken-ichi Kurimoto</i>	259

Session D3 Physical Design Planning

Co-Chairs : Wayne W.-M. Dai – Univ. of California, Santa Cruz, USA
Shuji Tsukiyama – Chuo Univ., Japan

D3.1	Delay-Optimal Wiring Plan for the Microprocessor of High Performance Computing Machines	
	<i>Jun Kikuchi, Tetsuo Sasaki, Tohru Hashimoto, Kazuhisa Miyamoto</i>	265
D3.2	MMP : A Novel Placement Algorithm for Combined Macro Block and Standard Cell Layout Design	
	<i>Hong Yu, Xianlong Hong, Yici Cai</i>	271
D3.3	Dynamic Weighting Monte Carlo for Constrained Floorplan Designs in Mixed Signal Application	
	<i>Jason Cong, Tianming Kong, Dongmin Xu, Faming Liang, Jun S. Liu, Wing Hung Wong</i>	277

Session E3 Methodologies for Reliable Design

Co-Chairs : Mitiko Miura-Mattausch – Hiroshima Univ., Japan
Andrzej J. Strojwas – Carnegie Mellon Univ., USA

E3.1	Symbolic Circuit-Noise Analysis and Modeling with Determinant Decision Diagrams	
	<i>XiangDong Tan, C.-J. Richard Shi</i>	283
E3.2	Gate-Level Aged Timing Simulation Methodology for Hot-Carrier Reliability Assurance	
	<i>Yoshiyuki Kawakami, Jingkun Fang, Hirokazu Yonezawa, Nobufusa Iwanishi, Lifeng Wu, Alvin I-Hsien Chen, Norio Koike, Ping Chen, Chune-Sin Yeh, Zhihong Liu</i>	289
E3.3	Embedded Tutorial : Subwavelength Lithography Technologies (PSM, OPC)	
	<i>Tsuneo Terasawa</i>	295

Session A4 Synthesis for System-On-A-Chip

Co-Chairs : *Rolf Ernst – Technical Univ. Braunschweig, Germany*
Ahmed A. Jerraya – TIMA Laboratory, France

A4.1	Embedded Tutorial : IC Design Technology for Building System-On-A-Chip	
	<i>Rajesh Gupta</i>	301
A4.2	Thread Partitioning Method for Hardware Compiler Bach	
	<i>Mizuki Takahashi, Nagisa Ishiura, Akihisa Yamada, Takashi Kambe</i>	303
A4.3	An Area/Time Optimizing Algorithm in High-Level Synthesis for Control-Based Hardwares (Short Paper)	
	<i>Nozomu Togawa, Masayuki Ienaga, Masao Yanagisawa, Tatsuo Ohtsuki</i>	309
A4.4	A Timing-Driven Synthesis of Arithmetic Circuits using Carry-Save-Adders (Short Paper)	
	<i>Taewhan Kim, Junhyung Um</i>	313

Session B4 Reconfigurable Computation

Co-Chairs : *Toshiaki Miyazaki – NTT Network Innovation Laboratories, Japan*
Tetsuo Hironaka – Hiroshima City Univ., Japan

B4.1	Communicating Logic : An Alternative Embedded Stream Processing Paradigm	
	<i>Norbert Imlig, Ryusuke Konishi, Tsunemichi Shiozawa, Kiyoshi Oguri, Kouichi Nagami, Hideyuki Ito, Minoru Inamori, Hiroshi Nakada</i>	317
B4.2	A Scheduling and Allocation Method to Reduce Data Transfer Time by Dynamic Re-configuration	
	<i>Kazuhito Ito</i>	323
B4.3	Invited Talk : Reconfigurable Computing: Its Concept and a Practical Embodiment using Newly Developed Dynamically Reconfigurable Logic (DRL) LSI	
	<i>Masakazu Yamashina, Masato Motomura</i>	329

Session C4 Synthesis for Low Power

Co-Chairs : *Akira Nagoya – NTT Communication Science Laboratories, Japan*
Manish Pandey – Cadence Design Systems, Inc., USA

C4.1	Power Reduction by Simultaneous Voltage Scaling and Gate Sizing	
	<i>Chunhong Chen, Majid Sarrafzadeh</i>	333
C4.2	Analysis of Power-Clocked CMOS with Application to the Design of Energy-Recovery Circuits	
	<i>Massoud Pedram, Xunwei Wu</i>	339
C4.3	Low-Power Design of Sequential Circuits Using a Quasi-Synchronous Derived Clock	
	<i>Xunwei Wu, Jian Wei, Massoud Pedram, Qing Wu</i>	345
C4.4	FSM Decomposition by Direct Circuit Manipulation Applied to Low Power Design	
	<i>Jose C. Monteiro, Arlindo L. Oliveira</i>	351

Session D4 (Panel Discussion)
Timing Closure : The Solution and Its Problems

Organizer: *Ralph H.J.M. Otten – Delft University of Technology, The Netherlands*
Moderator: *Ralph H.J.M. Otten – Delft University of Technology, The Netherlands*
Panelists: *Raul Camposano (Synopsys, Inc., USA), Oliver Coudert (Monterey Design Systems, Inc., USA), Patrick Groeneveld (Magma Design Automation, USA), Leon Stok (Thomas J. Watson Research Center, IBM, USA) 359*

Session E4
MOSFET Device Optimization

- Co-Chairs : *Naoyuki Shigyo – Toshiba Corp., Japan*
C.-J. Richard Shi – Univ. of Washington, USA
- E4.1 High Performance of Short-Channel MOSFETs due to an Elevated Central-Channel Doping**
M. Tanaka, N. Tokida, T. Okagaki, M. Miura-Mattausch, W. Hansch, H. J. Mattausch 365
- E4.2 Circuit Performance Oriented Device Optimization using BSIM3 Pre-Silicon Model Parameters**
Mikako Miyama, Shiro Kamohara 371
- E4.3 Embedded Tutorial : Design for Manufacturability**
Andrzej J. Strojwas 375

Session A5
Low Power Design : System Approach

- Co-Chairs : *Keshab K. Parhi – Univ. of Minnesota, USA*
Koji Kotani – Tohoku Univ., Japan
- A5.1 Embedded Tutorial : Low-Power Silicon Architectures for Wireless Communications**
Jan Rabaey 377
- A5.2 Run-time Power Control Scheme using Software Feedback Loop for Low-power Real-time Application**
Seongsoo Lee, Takayasu Sakurai 381
- A5.3 An Interleaved Dual-Battery Power Supply for Battery-Operated Electronics**
Qing Wu, Qinru Qiu, Massoud Pedram 387

Session B5 System Design and Debugging

Co-Chairs : *Rajesh Gupta – Univ. of California, Irvine, USA*
Takashi Kambe – Sharp Corp., Japan

B5.1	Embedded Tutorial : Multilanguage System Design	
	<i>Rolf Ernst, Ahmed A. Jerraya</i>	391
B5.2	Symbolic Debugging of Globally Behavioral Specifications	
	<i>Darko Kirovski, Inki Hong, Miodrag Potkonjak, Marios C. Papaefthymiou</i>	397
B5.3	Fast Development of Source-level Debugging System Using Hardware Emulation (Short Paper)	
	<i>Sang-Joon Nam, Jun-Hee Lee, Byoung-Woon Kim, Yeon-Ho Im, Young-Su Kwon, Kyong-Gu Kang, Chong-Min Kyung</i>	401
B5.4	Methodology for Hardware/Software Co-verification in C/C++ (Short Paper)	
	<i>Luc Semeria, Abhijit Ghosh</i>	405

Session C5 Optimization Issues in Logic Synthesis

Co-Chairs : *Tsutomu Sasao – Kyushu Inst. of Technology, Japan*
Shin'ichi Minato – NTT Network Innovation Laboratories, Japan

C5.1	Performance-Optimal Clustering with Retiming for Sequential Circuits	
	<i>Tzu-Chieh Tien, Youn-Long Lin</i>	409
C5.2	IBAW: An Implication-Tree Based Alternative-Wiring Logic Transformation Algorithm	
	<i>Wangning Long, Yu-Liang Wu, Jinian Bian</i>	415
C5.3	On Mixture Density and Maximum Likelihood Power Estimation via Expectation-Maximization	
	<i>R. Chandramouli, Vamsi K. Srikantam</i>	423

Session D5 Novel Techniques in Advanced Partitioning

Co-Chairs : *Shin'ichi Wakabayashi – Hiroshima Univ., Japan*
Tetsushi Koide – Univ. of Tokyo, Japan

D5.1	Edge Seperability Based Circuit Clustering with Application to Circuit Partitioning	
	<i>Jason Cong, Sung Kyu Lim</i>	429
D5.2	Feasible Two-Way Circuit Partitioning with Complex Resource Constraints	
	<i>Hsun-Cheng Lee, Ting-Chi Wang</i>	435
D5.3	Performance Driven Multiway Partitioning	
	<i>Jason Cong, Sung Kyu Lim</i>	441

Session E5 Efficient Estimation for Interconnection

Co-Chairs : *Hiroshi Matsumoto – NEC Corp., Japan*
Xianlong Hong – Tsinghua Univ., China

E5.1	Hierarchical Computation of 3-D Interconnect Capacitance using Direct Boundary Element Method	
	<i>Jiangchun Gu, Zeyi Wang, Xianlong Hong</i>	447
E5.2	A Simplified Hybrid Method for Calculating the Frequency-dependent Inductances of Transmission Lines with Rectangular Cross Section	
	<i>Shuzhou Fang, Xiaobo Tang, Zeyi Wang, Xianlong Hong</i>	453
E5.3	An Analytic Calculation Method for Delay Time of RC-class Interconnects	
	<i>W. K. Kal, S. Y. Kim</i>	457
E5.4	A New Efficient Waveform Simulation Method for RLC Interconnect via Amplitude and Phase Approximation	
	<i>Xiaodong Yang, Walter H. Ku, Chung-Kuan Cheng</i>	463

Session A6 Optimized LSI Design

Co-Chairs : *Chong-Min Kyung – Korea Advanced Inst. of Science and Technology, Korea*
Takashi Morie – Hiroshima Univ., Japan

A6.1	Optimization of VDD and VTH for Low-Power and High Speed Applications	
	<i>Koichi Nose, Takayasu Sakurai</i>	469
A6.2	Compact yet High Performance (CyHP) Library for Short Time-to-Market with New Technologies	
	<i>Nguyen Minh Duc, Takayasu Sakurai</i>	475
A6.3	A New CMAC Neural Network Architecture and Its ASIC Realization	
	<i>Yuan-Bao Hsu, Kao-Shing Hwang, Chien-Yuan Pao, Jinn-Shyan Wang</i>	481

Session B6 DSP and Memory Architecture

Co-Chairs : *Ichiro Kuroda – NEC Corp., Japan*
Keshab K. Parhi – Univ. of Minnesota, USA

B6.1	Retargetable Estimation Scheme for DSP Architecture Selection	
	<i>Naji Ghazal, Richard Newton, Jan Rabaey</i>	485
B6.2	Data Memory Minimization by Sharing Large Size Buffers	
	<i>Hyunok Oh, Soonhoi Ha</i>	491
B6.3	Array Allocation Taking into Account SDRAM Characteristics	
	<i>Hong-Kai Chang, Youn-Long Lin</i>	497

Session C6 Validation and Test

Co-Chairs : *Cheng-Wen Wu – Univ. of California, Santa Barbara, USA*
Tomoo Inoue – Hiroshima City Univ., Japan

C6.1	Causality Based Generation Of Directed Test Cases	
	<i>Nina Saxena, Jacob Abraham, Avijit Saha</i>	503
C6.2	Embedded Tutorial : Fault models and test generation for IDDQ Testing	
	<i>Yoshinobu Higami, Kewal K. Saluja, Yuzo Takamatsu, Kozo Kinoshita</i>	509
C6.3	Embedded Tutorial : Issues on SOC Testing in DSM Era	
	<i>Takashi Aikyo</i>	515

Session D6 Cell Generation & Process Dependent Issues

Co-Chairs : *Jun-Dong Cho – Sungkyunkwan Univ., Korea*
Yoichi Shiraishi – Gunma Univ., Japan

D6.1	A Cell Synthesis Method for Salicide Process	
	<i>Kazuhisa Okada, Takayuki Yamanouchi, Takashi Kambe</i>	517
D6.2	Monte-Carlo Algorithms for Layout Density Control	
	<i>Yu Chen, Andrew B. Kahng, Gabriel Robins, Alex Zelikovsky</i>	523
D6.3	Layout Generation of Array Cell for NMOS 4-phase Dynamic Logic (Short Paper)	
	<i>Makoto Furuie, Bao-Yu Song, Yukihiro Yoshida, Takao Onoye, Isao Shirakawa</i>	529
D6.4	A New Efficient Method for Substrate-Aware Device-Level Placement (Short Paper)	
	<i>C. Lin, D. M. W. Leenaerts</i>	533

Session E6 Analysis Techniques for Analog Circuits

Co-Chairs : *Mineo Kaneko – Japan Advanced Inst. of Science and Technology, Japan*
Peter M. Lee – Hitachi Ltd., Japan

E6.1	The Enhancing of Efficiency of the Harmonic Balance Analysis by Adaptation of Pre-conditioner to Circuit Nonlinearity	
	<i>M. M. Gourary, S. G. Rusakov, S. L. Ulyanov, M. M. Zharov, K. K. Gullapalli, B. J. Mulvaney</i>	537
E6.2	Analog-Testability Analysis by Determinant-Decision-Diagrams based Symbolic Analysis	
	<i>Tao Pi, C.-J. Richard Shi</i>	541
E6.3	A Method for Linking Process-level Variability to System Performances	
	<i>Tomohiro Fujita, Ken-ichi Okada, Hiroaki Fujita, Hidetoshi Onodera, Keikichi Tamaru</i>	547

Session A7 Advanced Design Techniques for Deep-Submicron System-On-A-Chip

Co-Chairs : Kazuo Yano – Hitachi, Ltd., Japan
Takao Onoye – Kyoto Univ., Japan

A7.1	Embedded Tutorial : Design Challenges for 0.1um and Beyond	
	<i>Takayasu Sakurai</i>	553
A7.2	A Hardware Accelerator for the Specular Intensity of Phong Illumination Model in 3-Dimensional Graphics	
	<i>Young-Su Kwon, In-Cheol Park, Chong-Min Kyung</i>	559
A7.3	Radix-4 Modular Multiplication and Exponentiation Algorithms for the RSA Public-Key Cryptosystem	
	<i>Jin-Hua Hong, Cheng-Wen Wu</i>	565

Session B7 (Special Session) Future of System Level Design Languages

Chair : Masaharu Imai – Osaka Univ., Japan

B7.1	SLDL and Rosetta	
	<i>Steven Schulz – Texas Instruments, Inc., USA</i>	571
B7.2	SystemC Standard	
	<i>Guido Arnout</i>	573
B7.3	Java based object oriented hardware specification and synthesis,	
	<i>Tommy Kuhn, Wolfgang Rosenstiel</i>	579
B7.4	Superlog, A Unified Design Language for System-on-chip	
	<i>Peter Flake, Simon J. Davidmann</i>	583

Session C7 Delay Testing and Design-For-Testability

Co-Chairs : Yukiya Miura – Tokyo Metropolitan Univ., Japan
Hiroshi Date – Inst. of Systems & Information Technologies Kyushu, Japan

C7.1	Performance Sensitivity Analysis Using Statistical Method and Its Applications to Delay Testing	
	<i>Jing-Jia Liou, Angela Krstic, Kwang-Ting Cheng, Deb Aditya Mukherjee, Sandip Kundu</i>	587
C7.2	A Testability Metric for Path Delay Faults and Its Application	
	<i>Huan-Chih Tsai, Kwang-Ting Cheng, Vishwani D. Agrawal</i>	593
C7.3	A Non-Scan DFT Method at Register-Transfer Level to Achieve Complete Fault Efficiency	
	<i>Satoshi Ohtake, Hiroki Wada, Toshimitsu Masuzawa, Hideo Fujiwara</i>	599
C7.4	A Sigma-Delta Modulation Based BIST Scheme for Mixed-Signal Circuits	
	<i>Jiun-Lang Huang, Kwang-Ting Cheng</i>	605

Session D7 (Panel Discussion) Industry-Academia Cooperation

Organizer: Tokinori Kozawa – STARC, Japan
 Moderator: Hiroto Yasuura – Kyushu Univ., Japan
 Panelists: Bill Joyner (SRC, USA), Jan Rabaey (Univ. of California, Berkeley, USA), Ivo
 Bolson (IMEC, Belgium), Yoshiaki Masuhara (Hitachi Ltd., Japan) 611

Session E7 Signal Integrity / Noise Issues in Deep-Submicron

- Co-Chairs : Hidetoshi Onodera – Kyoto Univ., Japan
 Nobuo Fujii – Tokyo Inst. of Technology, Japan
- E7.1 A 12b 50 MHz 3.3V CMOS Acquisition Time Minimized A/D Converter**
 Young-Deuk Jeon, Byeong-Lyeol Jeon, Seung-Chul Lee, Sang-Min Yoo, Seung-Hoon
 Lee 613
- E7.2 A Benchmark Suite for Substrate Analysis**
 Edoardo Charbon, Luis Miguel Silveira, Paolo Miliozzi 617
- E7.3 Embedded Tutorial : Substrate Crosstalk Analysis in Mixed Signal CMOS Integrated
 Circuits**
 Makoto Nagata, Atsushi Iwata 623

Session A8 High Speed LSI Design for Entertainment Application

- Co-Chairs : Takayasu Sakurai – Univ. of Tokyo, Japan
 Makoto Ikeda – Univ. of Tokyo, Japan
- A8.1 Invited Talk : Importance of CAD Tools and Methodology in High Speed CPU Design**
 Haruyuki Tago, Kazuhiro Hashimoto, Nobuyuki Ikumi, Masato Nagamatsu, Yasuyuki
 Yamamoto, Masakazu Suzuoki 631
- A8.2 300MHz design methodology of VU for Emotion Synthesis**
 Takayuki Kamei, Hideki Takeda, Yukio Ootaguro, Takayoshi Shimazawa, Kazuhiko
 Tachibana, Shin'ichi Kawakami, Seiji Norimatsu, Fujio Ishihara, Toshinori Sato,
 Hiroaki Murakami, Nobuhiro Ide, Yukio Endo, Akira Aono, Atsushi Kunitatsu 635
- A8.3 Repeater Insertion Method and its application to a 300MHz 128-bit 2-way Super-
 scalar Microprocessor**
 Norman Kojima, Yukiko Parameswar, Christian Klingner, Yukio Ohtaguro, Masataka
 Matsui, Shigeaki Iwasa, Tatsuo Teruyama, Takayoshi Shimazawa, Hideki Takeda,
 Kouji Hashizume, Haruyuki Tago, Masaaki Yamada 641
- A8.4 Clock Design of 300MHz 128-bit 2-way Superscalar Microprocessor**
 Fujio Ishihara, Christian Klingner, Ken-ichi Agawa 647

Session B8 (Panel Discussion)

One Language or More? (How Can We Design an SoC at a System Level?)

Organizer: Masaharu Imai – Osaka Univ., Japan

Moderator: Gary Smith – Dataquest, USA

Panelists: Steven Schulz [SLDL] (Texas Instruments, Inc., USA), Karen Bartleson [SystemC] (Synopsys, Inc., USA), Daniel D. Gajski [SpecC] (Univ. of California, Irvine, USA), Peter Flake [Superlog] (Co-Design Automation, Inc., USA), Wolfgang Rosenstiel [Java] (Univ. of Tuebingen, Germany), Hiroto Yasuura [C/C++] (Kyushu Univ., Japan), Masaharu Imai [VHDL] (Osaka Univ., Japan) 653

Session D8

High Performance Partitioning

Co-Chairs : Chung-Kuan Cheng – Univ. of California, San Diego, USA
Toshiyuki Shibuya – Fujitsu Laboratories, Ltd., Japan

- D8.1 Circuit Partitioning with Coupled Logic Restructuring Techniques**
Yu-Liang Wu, Xiao-Long Yuan, David Ihsin Cheng 655
- D8.2 Improved Algorithms for Hypergraph Bipartitioning**
Andrew E. Caldwell, Andrew B. Kahng, Igor L. Markov 661
- D8.3 Multi-way Partitioning Using Bi-partition Heuristics**
Maogang Wang, Sung Lim, Jason Cong, Majid Sarrafzadeh 667

Low-power Design Methodology and Applications utilizing Dual Supply Voltages

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Abstract - This paper describes a gate-level power minimization methodology using dual supply voltages. Gates and flip-flops off the critical paths are made to operate at the reduced supply voltage to save power. Core technologies are dual- V_{DD} circuit synthesis and P&R. We give a brief overview on existing low-power EDA technologies as background and discuss advantages and challenges of the dual-VDD approach. Through real design examples, we will show that the approach reduces power effectively while keeping the performance at negligible area overhead.

I. Introduction

Power minimization is one of the key technologies in modern VLSI design. Research and development in this field are motivated by growing markets of portable information devices, such as PDA's, cellular phones, digital camcorders and digital cameras. For VLSI's in those applications, high performance and low power are required simultaneously. High performance is required for data processing such as real-time encoding and decoding of picture/audio data, while low power for prolonging battery life.

Requirement for power minimization is not limited to portable applications. In consumer applications in which cost competition is extremely serious, low power is needed for reducing package cost. Power must be low if one uses cheap plastic packages instead of expensive ceramic ones.

Power minimization is also required for improving reliability of high-end microprocessors. Operation frequencies are raised for improving performance in those VLSI's, resulting in increasing power (current) dissipation. This tends to cause reliability problems such as electromigration in wires, hot electron effects in MOS transistors, IR-drop in power lines and ground bounce. Power reduction technologies keeping high performance are strongly required.

In this paper, we present design methodology that enables us to reduce power while keeping performance. First we will

give a brief overview on low-power EDA technologies as background. Next we will describe low-power techniques using multiple supply voltages in a core, especially focusing on a gate-level design methodology using dual- V_{DD} 's. We will discuss effectiveness and challenges of the methodology through experimental results at real chips.

II. Background

Average power dissipation in CMOS circuit consists of four components; dynamic power consumed in charging and discharging of load capacitances, short-circuit power arising from switching transient current, leakage power due to leakage current, and static power due to static current drawn continuously from the power supply [1]. Dominant fraction of average power is attributed to the dynamic power [2]. In this paper, we discuss low-power design methodology by focusing on the techniques of minimizing dynamic power.

The dynamic power is given by $P = CV^2f\alpha$, where C is the load capacitance, V is the supply voltage, f is the clock frequency, and α is the switching activity. Hence, for minimizing the dynamic power, we need to minimize the parameters of C , V , f and α . Papers have been reported on the technologies that minimize these parameters while keeping the performance. Fig.1 summarizes power minimization technologies, in which parameters to be minimized and design levels are shown two-dimensionally. Currently the most popular techniques are the ones that minimize C and α . These techniques can be classified into two categories: (i) techniques which minimize $C \times \alpha$ on average and (ii) techniques which stop switching selectively. Techniques such as low-power logic synthesis, power-driven placement and transistor sizing are examples of (i), while techniques such as gated clock and operand isolation are those of (ii). Low-power technology mapping [3] is an effective technique in low-power logic synthesis. Cells are mapped so nodes with high switching activity be hidden inside the cells.

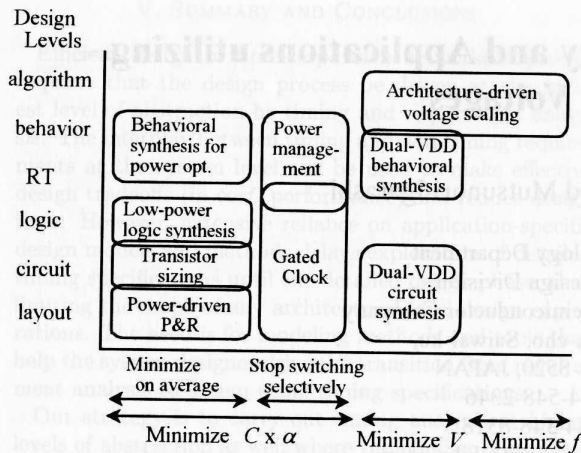


Fig.1. Power Minimization Technologies.

Load capacitances inside the cells are smaller, resulting in minimizing $C \times \alpha$ on average. Power-driven placement is a layout technique in which placement is performed so wire length weighted by switching activity be minimized [4]. As transistor-sizing techniques for low power, gate resizing [5] and gate/wire sizing [6] have been reported. Techniques categorized in (ii) focus on disabling signal transitions when they are unnecessary. Gated clock is the most well-known technique in which switching of clock signals is stopped when register-loading is not needed. Operand isolation is an approach in which transitions of inputs are disabled at circuit blocks when they are idle [7].

Another parameter to be targeted at for power optimization is the supply voltage V . Reduction of supply voltage is very effective because power is reduced quadratically. However, the performance of MOS transistors is degraded with reducing V , leading to increasing the delay. Techniques are required which enable us to reduce supply voltage while keeping the performance of the entire chip. Architecture-driven voltage scaling [8] is an approach to save power by reducing V and f . A parallel architecture is built for keeping the throughput of the entire circuit. This approach is quite effective at DSP applications, although it comes with area penalty resulting from parallel datapaths.

Another approach is to make use of dual supply voltages in a core. Only the circuit part requiring high performance is made to operate at the original voltage V_{DDH} , while the rest of the circuit is made to operate at the reduced voltage V_{DDL} . This results in reducing power without degrading the entire circuit performance. This approach can be classified by the level of granularity into (i) module level, (ii) functional-unit level, and (iii) gate level. In a module-level approach reported in [9], V_{DDL} is used in potentially power-hungry modules, while V_{DDH} is used in other ones. A designer must perform RTL design and logic synthesis taking into account the delay at V_{DDL} . As approaches for (ii), papers have been reported on scheduling and optimal voltage selection for operations in behavioral synthesis [10][11]. A gate-level approach reported in [12] is to synthesize dual- V_{DD} structure at gate level from the netlist originally designed with single supply volt-

age. No extra burden is imposed on a designer. He/she can perform RTL design and logic synthesis in the conventional way. Implementation with dual supply voltages is automatically done using dual- V_{DD} circuit synthesis and P&R [13].

III. Gate-level Dual- V_{DD} Approach for Low Power

A. Basic Concept and Problem Definition

The basic idea of the gate-level dual- V_{DD} approach is to run the gates off the critical paths at the reduced supply voltage V_{DDL} , while those on the critical paths at V_{DDH} . This results in reducing the power without degrading the entire circuit performance. This idea can be realized by performing static timing analysis for a given circuit designed with single V_{DD} , extracting the gates off the critical paths, and assigning V_{DDL} to them. If netlist and timing constraints are given along with the V_{DDL} voltage, one could generate a dual- V_{DD} circuit using conventional algorithm such as gate resizing. Fig.2 shows a possible circuit example generated in this manner. However, this circuit has a problem when implementing in CMOS LSI's. Static current flows at a V_{DDH} gate if it is directly driven by a V_{DDL} gate. This is because the PMOS at the V_{DDH} gate cannot be cut-off at the input level "High". A typical way of blocking the static current is to insert a level converter (level shifter) circuit into the interface of a V_{DDL} gate to a V_{DDH} gate. In Fig.2, level converters should be inserted into the portions marked as A to D. Level converters become an overhead of area and power. Thus the problem we need to solve is finally defined as follows: For a given circuit, choose gates and/or flip-flops to which we should apply V_{DDL} such that we minimize the number of level converters and the entire power while meeting the timing constraints.

B. Dual- V_{DD} Circuit Synthesis

Minimizing connections from V_{DDL} gates to V_{DDH} ones is a most effective way to minimize the number of level-converters needed. The Clustered-Voltage-Scaling (CVS) structure proposed in [12] is the simplest one that does it. As

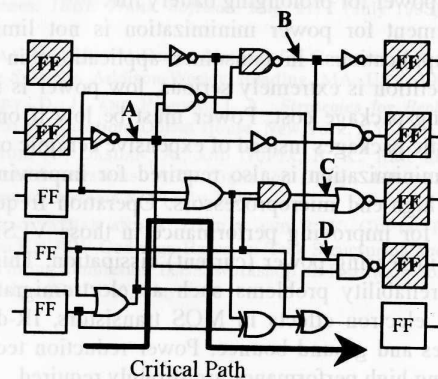


Fig.2. Circuit with portions operating at V_{DDL} (shown as shaded) and those operating at V_{DDH} .

shown in Fig.3, clustered structure is built such that logic gates on the output side of the combinational network (i.e. logic gates closer to the D-inputs of flip-flops) become V_{DDL} gates. In the CVS structure the connection pattern of a V_{DDL} gate to a V_{DDH} gate does not exist. The only portions requiring level converters are the interface between the output of a V_{DDL} flip-flop and the input of a V_{DDH} gate. Therefore, the number of needed level converters is at most the same as the number of flip-flops. Because no level converters are needed between logic gates, the CVS structure minimizes the number of level converters needed.

An extended CVS (ECVS) structure has been reported in [14]. The limitation in the CVS is somewhat relaxed so the number of gates becoming V_{DDL} be increased. In the ECVS, insertion of level converters is allowed even between logic gates. This is effective at a gate with multiple inputs when one input is on the critical path, while others are not. In the CVS, not only this gate but also its transitive fan-ins must be V_{DDH} . In the ECVS, however, we give opportunities to the transitive fan-ins to become V_{DDL} by inserting level converters at the input of the gate. In practice, it is checked if the level-converter insertion is worth performing in reducing power. If it is, the insertion is performed.

Because the CVS or ECVS structure could not be synthesized with available EDA tools, we developed a dual- V_{DD} circuit synthesizer that generates them. The synthesizer takes a gate-level netlist designed with a single supply voltage V_{DDH} as input, identifies non-critical paths by invoking an internal static-timing-analysis engine, and replaces as many V_{DDH} cells with V_{DDL} ones under the given timing constraints. Level converters are automatically inserted into needed portions. A netlist with the CVS or ECVS structure is generated as output.

C. Dual- V_{DD} Place and Route

One of the most important issues in the dual- V_{DD} layout is the voltage separation between V_{DDH} cells and V_{DDL} cells. V_{DDH} and V_{DDL} cells have to be isolated because their N-well voltages are different. Voltage separation at row-by-row has been addressed in [14][15], while the voltage separation within a row has been presented in [16]. We chose the row-by-row voltage separation shown in Fig.4 because of (i)

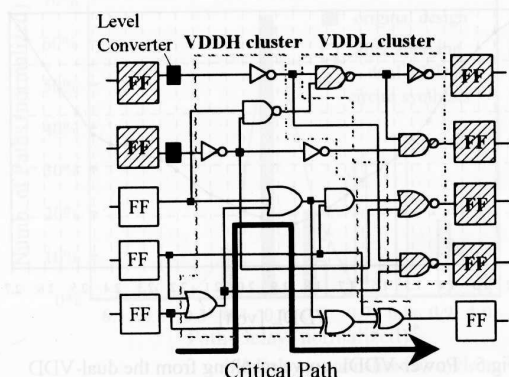


Fig.3. Clustered-voltage-scaling (CVS) structure.

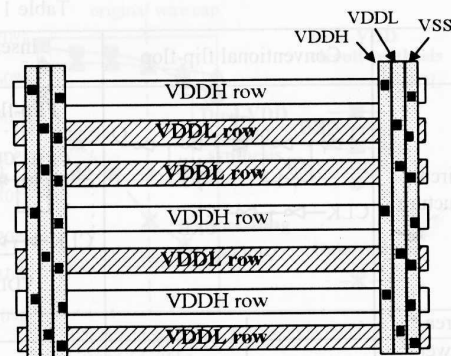


Fig.4. Row-by-row voltage separation for dual-VDD layout.

high-performance and (ii) applicability to gate arrays as well as standard-cell-based designs.

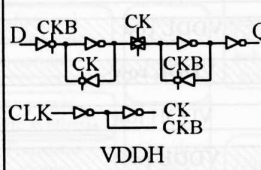
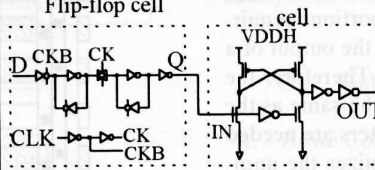
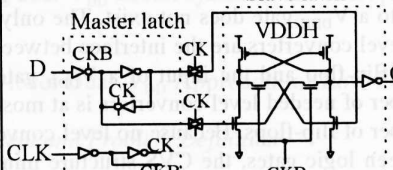
We developed automated techniques to generate the row-by-row dual- V_{DD} layout and realized on our internal P&R platform. A couple of new technologies were required. One is the optimal voltage assignment to rows. We developed voltage assignment algorithms minimizing area overhead while taking into account wire congestion and timing constraints [15][17]. The other key technology is the cell placement under the voltage constraint. In the row-by-row architecture a V_{DDH} cell must be placed in a V_{DDH} row, while a V_{DDL} cell in a V_{DDL} row. In other words, cells must be placed taking into account the voltage. Since this could not be achieved with available P&R tools, we enhanced the capability of our internal placement tool to achieve this.

D. Flip-Flop Circuit with Level-Conversion Function

The CVS and ECVS structure described above minimizes the number of level converters. The number is at most the number of flip-flops because a level converter is basically inserted at the output of a flip-flop. However, in the case of a circuit with a lot of flip-flops, inserted level converters cause a significant area penalty. We proposed an approach reducing the penalty by using a flip-flop circuit with a level-conversion function (FFLC) [17]. The circuit is depicted at the right-most column in Table 1. A master latch of the FFLC is the same as a conventional flip-flop, while a slave latch has a level-conversion function. Signals with V_{DDL} -swing at D and CLK are converted to V_{DDH} -swing at Q. Area penalty gets less by using FFLC compared to the case of inserting a level-converter cell at the output of a flip-flop (shown in column 2). Power is smaller than the conventional flip-flop operating at V_{DDH} resulting from the fact that the master latch of the FFLC operates at V_{DDL} . CLK-to-Q delay of the FFLC is larger only by 0.18ns than that of the conventional flip-flop. We chose to use the FFLC in the design because of its advantages.

The use of the FFLC allows us to shorten the turn-around-time (TAT) of the design. We developed a design flow to use the FFLC as a default flip-flop in logic synthesis. Register elements in RTL description are mapped into the FFLC's even in the single-voltage netlist. The use of the FFLC is

Table 1. Comparisons on flip-flops.

	Conventional flip-flop	Insertion of level-converter cell at output of flip-flop	Flip-flop with level-conversion function (FFLC)
Circuit structure			
Area *	1	1.64	1.21
Power *	1	0.74	0.63
Delay *	0.24 ns **	0.59 ns ***	0.42 ns **

* Results on area and power are normalized by those on the conventional flip-flop.

Power and delay were simulated at $V_{DDH} = 2.5V$, $V_{DDL} = 1.75V$, $|V_{th}| = 0.2V$.

** CLK-to-Q delay *** CLK-to-OUT delay

very helpful for minimizing the change between the single-voltage netlist and the dual- V_{DD} netlist. This is because there is no need to insert level converters at the outputs of the FFLC's, resulting in minimizing the change in gate count and path delay. This allows us to utilize the placement result of the single- V_{DD} layout as initial floorplanning information at Dual- V_{DD} layout. This leads to shortening the TAT.

E. Supply Voltage Reduction in Clock Tree

We applied the dual- V_{DD} approach also to a clock tree [13]. A root driver is made to operate at V_{DDH} , while clock buffers in the clock tree are made to operate at V_{DDL} . Since the output voltage swing of the leaf buffers is V_{DDL} , flip-flops driven by the leaf buffers must be able to receive the clock signal with the V_{DDL} swing. By using the FFLC circuits as flip-flops, this constraint is automatically satisfied. The dual- V_{DD} clock tree is generated at the layout phase using a Clock-Tree-Synthesis (CTS) technique.

IV. Application Examples of Dual- V_{DD} Approach

A. Media Processor

We applied the dual- V_{DD} circuit synthesis and dual- V_{DD} P&R to a media processor [13].

In applying this approach, the first thing we had to do was to find the optimal V_{DDL} voltage. We repeated dual- V_{DD} circuit synthesis and monitoring the power while changing V_{DDL} voltage under V_{DDH} of 2.7V. The result is shown in Fig.5. The power versus V_{DDL} curve is U-shaped, showing that the power gets the minimum at V_{DDL} of 1.9V. Intuitively we can see that the power can not be reduced at higher V_{DDL} . However, the power is not reduced either when V_{DDL} is too low. The reason is as follows: In the dual- V_{DD} approach, power reduction is determined by a couple of factors: the power reduction at a single cell by scaling the supply voltage from V_{DDH} to V_{DDL} , and the number of cells replaced with V_{DDL} ones. At lower V_{DDL} , the power at a V_{DDL} cell gets

smaller, while the number of the cells replaced with V_{DDL} ones gets fewer. This is because the performance of V_{DDL} cells gets poorer at lower V_{DDL} . In other words, to replace cells with V_{DDL} ones gets harder while meeting the timing constraints. Hence the power is not reduced when V_{DDL} is too low.

Determining the optimal V_{DDL} voltage is an important step in the dual- V_{DD} design. However, if we need to repeat the procedure described above to find the optimal V_{DDL} at each design, it would take a lot of time. Instead, if there is an approach to give us the optimal V_{DDL} in a top-down fashion, it will be more efficient. The research on this issue has been reported in [18]. The authors built a theoretical model relating the V_{DDL} / V_{DDH} value and the path-delay distribution of circuits to the power reduction. By using the model, they analyzed the V_{DDL} / V_{DDH} value maximizing the power reduction. They showed that the optimal V_{DDL} / V_{DDH} value exists between 0.6 and 0.7 irrespective of the path-delay distribution of a circuit. In the application to the media processor, the optimal V_{DDL} was empirically obtained as 1.9V under V_{DDH} of 2.7V, leading to $V_{DDL} / V_{DDH} = 0.70$. This shows a good agreement with the claim from the theory.

We performed the dual- V_{DD} circuit synthesis to random-logic modules including 2.5K through 14K cells. The per-

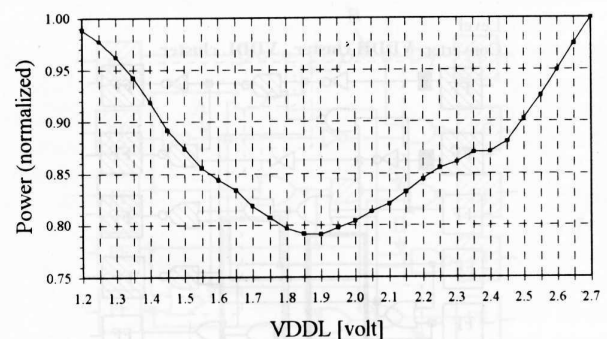


Fig.5. Power-VDDL curve resulting from the dual-VDD circuit synthesis.

centage of the cells replaced with V_{DDL} ones was 76%. To investigate the reason of the rich replacement, we analyzed the distribution of path-delays in the design. Results are shown in Fig.6. The X-axis shows the path-delay normalized by the cycle-time. Hence the normalized delay of 1.0 indicates the path-delay is the same as the cycle-time, meaning it is a critical path. Moving toward the left along the X-axis, the path-delay decreases and the slack increases. The Y-axis shows the number of paths normalized by the total number. We investigated 5.8M paths using static path analysis. In the original design, although as many as 15K critical paths exist, they occupy only 0.3% in the total paths. More than 60% of the paths have delays of half of the cycle-time. By applying the dual- V_{DD} circuit synthesis, the center of the distribution was moved toward the right. Thus the dual- V_{DD} circuit synthesis effectively spends the excessive slack remaining in the non-critical paths to build the dual- V_{DDL} structure.

We analyzed the power using the PowerMill simulation. Power was reduced by 47% in the random-logic modules while keeping the performance of 75MHz.

B. Graphic Controller LSI

We applied the dual- V_{DD} circuit synthesis to three function modules in a graphic controller LSI [19]. Power reduction was compared with that of the conventional gate-resizing technique. We investigated how the power reduction is affected by the wire capacitance. We performed dual- V_{DD} circuit synthesis and gate-resizing while changing the wire capacitance. Results are shown in Fig.7. As the wire capacitance gets dominant, power reduction in the gate-resizing significantly decreases, while that in the dual- V_{DD} circuit synthesis does not change so much.

Possible reasons are as follows: when the wire capacitance is not dominant over the gate capacitance, each gate could be down-sized without increasing the total delay. In other words, down-sizing a certain gate reduces the output load capacitance of the parent gate, allowing to down-size the parent gate itself without increasing the delay. This down-sizing chain results in reducing the total power. However, when the wire capacitance is dominant, the down-sizing chain becomes less possible because the down-sizing

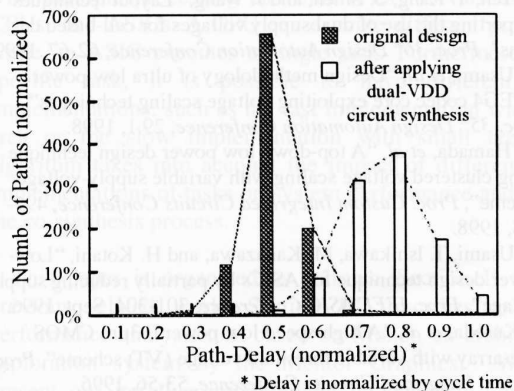


Fig.6. Distribution of path-delays

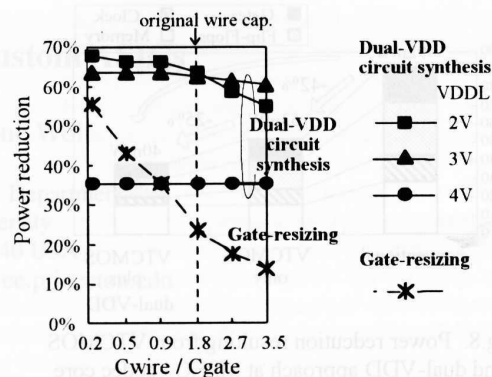


Fig.7. Affect of wire capacitance on power reduction at dual- V_{DD} circuit synthesis and gate resizing

of a gate affects less to the load capacitance. Another reason is that reducing gate capacitance does not contribute so much to the total power when wire capacitance is dominant.

Meanwhile, power reduction in the dual- V_{DD} approach does not depend upon whether the wire capacitance is dominant or not. This is because the dual- V_{DD} approach reduces the power dissipated in charging and discharging of wire capacitance as well as that for the gate capacitance.

Both of dual- V_{DD} circuit synthesis and gate-resizing are the techniques that reduce power by utilizing excessive slack in the circuit. However, they show very different sensitivity to the wire capacitance in power reduction. The dual- V_{DD} approach shows effectiveness in power savings even in the case that the wire capacitance is dominant.

C. MPEG4 Codec Core

To an MPEG4 codec core, we applied both the dual- V_{DD} approach and a VTCMOS technique to reduce power. VTCMOS is a technique to control the effective threshold voltage by applying substrate bias to MOS transistors [20]. At the active mode, transistors are made to operate at low V_{DD} with low V_{th} . At the standby mode, the effective threshold voltage is made to be larger by applying substrate bias to block the leakage current. Hence the VTCMOS technique allows us to reduce supply voltage at the active mode at the entire chip while keeping the performance.

Meanwhile, since VTCMOS does not care about excessive slack in non-critical paths, there is room for further power reduction at the gates in non-critical paths. By applying the dual- V_{DD} approach, we further reduce the supply voltage in non-critical paths to reduce power.

We analyzed the power of an MPEG4 codec core designed in 0.3 μ m CMOS technology. Results from the power simulation using PowerMill are shown in Fig.8. Operation frequency is 30MHz. VTCMOS using V_{DD} =2.5V and V_{th} =0.2V reduced power by 42% compared to the conventional design using V_{DD} =3.3V and V_{th} =0.55V. In addition, applying the dual- V_{DD} approach with V_{DDL} =1.75V reduced power further by 25% at the entire chip. We applied the dual- V_{DD} approach to the portions except memory macros.

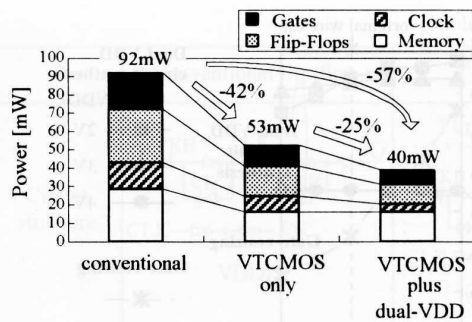


Fig.8. Power reduction resulting from VTCMOS and dual-VDD approach at MPEG4 codec core

Power was reduced at logic gates by 30%, at flip-flops by 37%, and at the clock tree by 49%, respectively. At the portions to which we applied the dual- V_{DD} approach, power was reduced by 35% even after applying VTCMOS. Thus the power in the conventional design was reduced by 57% by combining both techniques together.

To verify at real silicon, we fabricate test chips and measured average power dissipation. The chip to which we applied both the dual- V_{DD} approach and VTCMOS dissipated 45mW, leading to power reduction by 58% from the conventional design. The number of power reduction shows a good agreement with the above-mentioned results from the power simulation. The area overhead was 5% at the portions to which we applied the dual- V_{DD} approach, being almost negligible at the entire chip.

V. Conclusions and Future Work

We have described power minimization techniques reducing load capacitance, supply voltage, clock frequency, and switching activity. Currently the most popular techniques are those to reduce capacitance and switching activity. Techniques to reduce voltage, however, are very attractive because power dissipation is reduced quadratically. The dual- V_{DD} approach using two different supply voltages in a core enables us to save power while keeping the entire performance. We presented dual- V_{DD} circuit synthesis, P&R techniques and dual- V_{DD} clock tree generation. Through application examples, we showed the effectiveness of the dual- V_{DD} approach.

For future work, research efforts will be needed on noise analysis and avoidance scheme for the design with dual- V_{DD} . In particular, coupling noise should be carefully analyzed where an interconnect driven by V_{DDL} is located between two interconnects driven by V_{DDH} . We performed a design by paying special attention to inter-module wires and a clock net with V_{DDL} swing [13]. Research on systematic noise analysis and avoidance methodology will be required.

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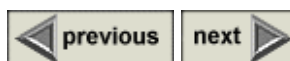
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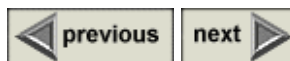
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