

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES INC.,
Petitioner,

v.

REALTEK SEMICONDUCTOR CORPORATION,
Patent Owner.

IPR2023-00920
Patent 8,006,218 B2

Before KRISTINA M. KALAN, KIMBERLY McGRAW, and
BRIAN D. RANGE, *Administrative Patent Judges*.

McGRAW, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Advanced Micro Devices, Inc. (“Petitioner”) filed a Petition (Paper 2, “Pet.”) requesting an *inter partes* review of claims 1–5, 8, and 9 of U.S. Patent No. 8,006,218 B2 (Ex. 1001, “the ’218 patent”). Realtek Semiconductor Corporation (“Patent Owner”) filed a Preliminary Response to the Petition (Paper 6, “Prelim. Resp.”). Thereafter, Petitioner filed a Brief Addressing an ITC order in a related proceeding (Paper 8, “Brief” or “Br.”) and Patent Owner filed a Reply to the Brief (Paper 9, “Reply Br.”).

To institute an *inter partes* review, we must determine that the information presented in the Petition shows “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). For the reasons discussed below, after considering the parties’ submissions and the evidence of record, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing with respect to at least one claim of the ’218 patent. Thus, we institute an *inter partes* review.

A. *Real Parties-In-Interest*

The parties identify themselves as the real parties-in-interest. Pet. 8; Paper 5, 1.

B. *Related Proceedings*

The parties identify *Realtek Semiconductor Corp. v. Advanced Micro Devices, Inc.*, Case No. 4:22-cv-04769-JSW (N.D. Cal.) and *Certain Integrated Circuits, Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1350 (U.S. International Trade Commission) (“the ITC investigation”) as related matters. Pet. 79; Prelim. Resp. 1. Patent Owner states that the ’218 patent, U.S. Patent No. 9,590,582 B2 (“the ’582 patent”),

and U.S. Patent No. 7,936,245 B2 (“the ’245 patent”) are asserted in these matters. Prelim. Resp. 1. Petitioner also challenges the ’582 patent in IPR2023-00788 and the ’245 patent in IPR2023-00789; the Board instituted *inter partes* review in both of those proceedings. *See Advanced Micro Devices, Inc. v. Realtek Semiconductor Corp.*, IPR2023-00788, Paper 9 (PTAB Oct. 26, 2023) (granting institution); *Advanced Micro Devices, Inc. v. Realtek Semiconductor Corp.*, IPR2023-00789, Paper 9 (PTAB Oct. 26, 2023) (granting institution).

C. The ’218 Patent

The ’218 patent is titled “Power Mesh Arrangement Method Utilized in an Integrated Circuit Having Multiple Power Domains.” Ex. 1001, code (54), 1:8–11. The ’218 patent issued on August 23, 2011, based on an application filed November 14, 2008, and claims priority to an application filed in Taiwan on November 15, 2007. *Id.* at codes (22), (30), (45).

The ’218 patent explains that different portions of a chip need different voltages or powers at the same time. *Id.* at 1:13–25. For example, if the chip circuitry has a normal operating mode and a sleeping mode, during the normal operating mode, the entire chip circuitry uses an operating voltage in order to conduct its normal operation. *Id.* However, during the sleeping mode, only part of the chip circuitry needs to be maintained in the normal operating mode while other circuitry can be provided with a lower voltage to maintain such other circuitry in sleeping mode. *Id.*

The ’218 patent further explains that traditional circuit design approaches do not provide a simple technique for the circuit designer to design power routing for a circuit having multiple power or voltage domains. *Id.* at 1:34–43.

Figure 1, reproduced below, is a schematic diagram illustrating a chip having multiple power domains. *Id.* at 2:45–46.

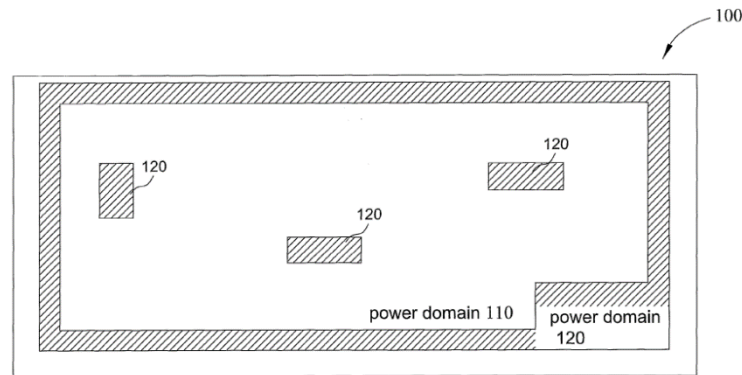


Figure 1 illustrates a chip 100 having two different kinds of power domains 110, 120, where power domain 110 is illustrated by the blank area and power domain 120 is illustrated by the oblique line area. *Id.* at 2:63–3:7. Power domains 110, 120 supply different voltages to different circuits. *Id.*

Figure 3, reproduced below, is a schematic diagram illustrating a local power mesh according to an embodiment for the chip in Figure 1. *Id.* at 2:49–51.

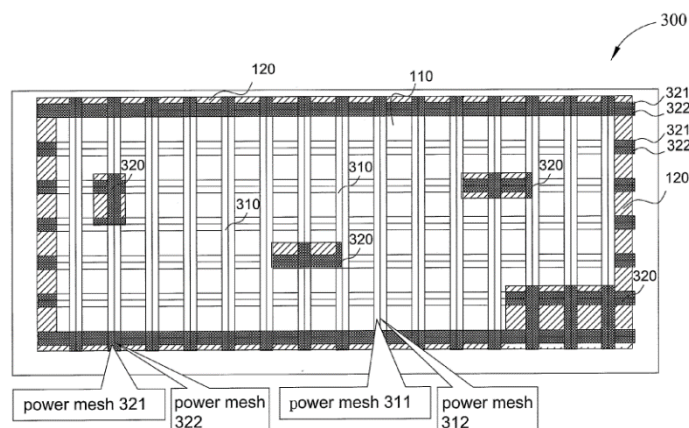


Figure 3 above illustrates local power mesh 300 partitioned into two different partial local power meshes 310, 320, at positions corresponding to the positions of power domains 110, 120 of Figure 1. *Id.* at 3:33–43.

In one embodiment, partial local power mesh 310 is placed on top of power domain 110 and partial local power mesh 320 is placed on top of power domain 120. *Id.* Partial local power meshes 310, 320 couple to power domains 110, 120 positioned below by way of via holes. *Id.* Partial local power meshes 310 comprise power wire 311 to supply a first working voltage needed by power domain 110 and ground wire 312 to supply ground potential for power domain 110. *Id.* at 3:44–64. Partial local power meshes 320 comprise power wire 321 to supply a second working voltage needed by power domain 120 and ground wire 322 to supply ground potential for power domain 120. *Id.*

Figure 4, reproduced below, illustrates a global power mesh according to an embodiment. *Id.* at 2:52–53.

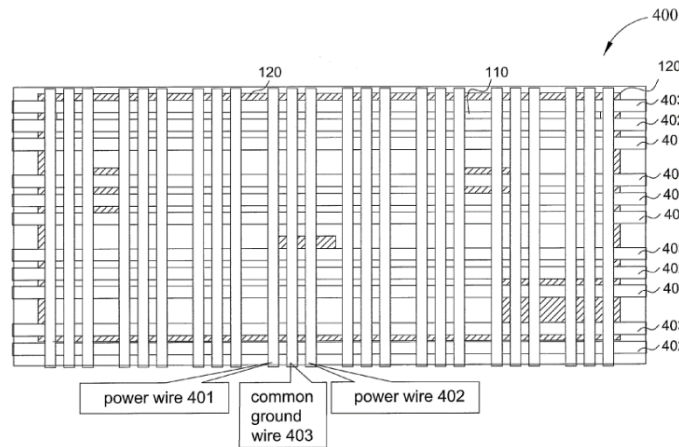


Figure 4 is a schematic diagram illustrating global power mesh 400 comprising a web-like structure with a plurality of horizontal power supply wires and a plurality of vertical power supply wires. *Id.* at 4:19–38.

Global power mesh 400 is distributed just above local power mesh 300 so that global power mesh 400 can conduct external power into the chip. *Id.* Each of the horizontal and the vertical power supply wires comprises one common ground wire 403 and two power wires 401, 402. *Id.* Common

ground wire 403 supplies ground potential V_{GND} for local power meshes 310, 320 and the two power wires 401, 402 supply working voltages V_{DD1} , V_{DD2} for local power meshes 310, 320. *Id.*

Figure 5, reproduced below, is a schematic diagram illustrating relative positions of local power mesh 300 of Figure 3 and global power mesh 400 of Figure 4, according to one embodiment. *Id.* at 2:54–56.

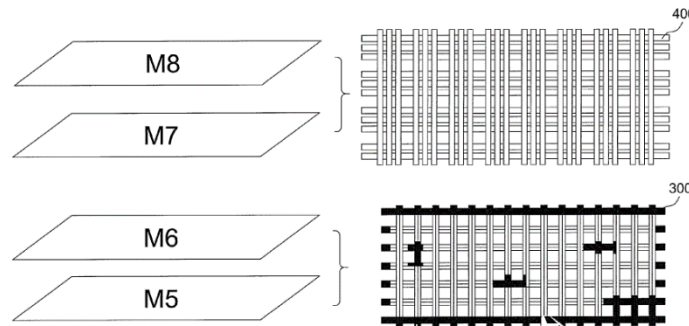


Figure 5 illustrates local power mesh 300 implemented on lower metal layers M5 and M6, with the horizontal power supply wire placed on metal layer M5 and the vertical power supply wire placed on the metal layer M6. *Id.* at 4:53–5:7. Global power mesh 400 is implemented on metal layer M7 and M8, with the horizontal power supply wire placed on metal layer M7 and the vertical power supply wire placed on metal layer M8. *Id.*

D. Illustrative Claims

Of the challenged claims, only claims 1, 12, and 19 are independent.

Independent claims 1 and 19 are method claims. Claim 1 is reproduced below with bracketing and formatting added for consistency with party usage and clarity.

1. A power routing arrangement method applied in an integrated circuit having multiple power domains, the arrangement method comprising:

- [a] forming a first partial local power mesh according to the position of a first power domain of the integrated circuit by an automatic placement and routing (APR) tool;
- [b] forming a second partial local power mesh according to the position of a second power domain of the integrated circuit by the APR tool;
- [c] forming a global power mesh that is utilized to provide the power needed by the first and the second power domains by the APR tool;
- [d] coupling the first partial local power mesh to the global power mesh and the first power domain by the APR tool; and
- [e] coupling the second partial local power mesh to the global power mesh and the second power domain by the APR tool;
- [f] wherein the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer, and
- [g] wherein the first metal layer and the second metal layer are different layers.

Ex. 1001, 6:59–7:15.

Claim 12, directed to a power routing structure, is reproduced below with formatting and bracketed material added for clarity and consistency with party usage.

12. A power routing structure applied in an integrated circuit having multiple power domains, comprising:

- [a] a first partial local power mesh having its position corresponding to the position of a first power domain and coupling to the first power domain;
- [b] a second partial local power mesh having its position corresponding to the position of a second power domain and coupling to the second power domain; and

- [c] a global power mesh, coupling to the first local power mesh and the second local power mesh, to provide the power needed by the first power domain and the second domain separately;
- [d] wherein the first partial local power mesh and the second partial local power mesh are positioned on the same metal layer while the global power mesh and the first local power mesh are positioned on different metal layers;
- [e] wherein the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer, and
- [f] wherein the first metal layer and the second metal layer are different layers.

Ex. 1001, 7:56–8:11.

E. The Asserted Grounds of Unpatentability

Petitioner contends claims 1–20 of the ’218 patent are unpatentable on the following grounds. Pet. 3–4.

Ground	Reference(s)	Basis ¹	Claim(s) Challenged
1	Jiang ² , Jiang2 ³ , Jiang3 ⁴	§ 103	12–18

¹ The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), amended 35 U.S.C. §§ 102 and 103. Because the ’218 patent has an effective filing date before the effective date of the applicable AIA amendments, we refer to the pre-AIA versions of §§ 102 and 103.

² Hailin Jiang et al., *Benefits and Costs of Power-Gating Technique*, Proceedings of the 2005 International Conference on Computer Design (ICCD 2005) (Ex. 1004, “Jiang”).

³ Hailin Jiang et al., *Power/Ground Supply Network Optimization for Power-Gating*, Proceedings of the 2006 International Conference on Computer Design (ICCD 2006) (Ex. 1007, “Jiang2”).

⁴ Hailin Jiang et al., *Power-Gating Aware Floorplanning*, Proceedings of the 8th International Symposium on Quality Electronic Design (ISQED 2007) (Ex. 1008, “Jiang3”).

Ground	Reference(s)	Basis ¹	Claim(s) Challenged
2	Jiang, Jiang2, Jiang3, Li ⁵ , Chiu ⁶	§ 103	12–18
3a ⁷	Jiang, Jiang2, Jiang3, Bertolet ⁸ , LPMM ⁹	§ 103	1–11, 19–20
3b	Jiang, Jiang2, Jiang3, Li, Chiu Bertolet, LPMM	§ 103	1–11, 19–20
4	Li, Jiang	§ 103	12–18
5	Li, Jiang, Bertolet, LPMM	§ 103	1–11, 19–20

In support of its unpatentability arguments, Petitioner relies on, *inter alia*, the declaration of Vivek Subramanian, Ph.D. (Ex. 1003, “Subramanian Dec.”).

⁵ Wei Li et al., *LVS Verification across Multiple Power Domains for a Quad-Core Microprocessor*, ACM Transactions on Design Automation of Electronic Systems, Vol. 11, No. 2, pp. 490-500, (April 2006) (Ex. 1005, “Li”).

⁶ U.S. Patent No. 7,948,292 (Ex. 1006, “Chiu”), filed June 5, 2008, claims priority to U.S. App. No. 60/976,181 (Ex. 1011, “Chiu Provisional Application”), filed Sept. 28, 2007.

⁷ For clarity, Petitioner’s alternative “Ground 3” arguments have been divided into Ground 3a and Ground 3b.

⁸ A. Bertolet et al., *A Pseudo-Hierarchical Methodology for High Performance Microprocessor Design*, Proceedings of the 1997 International Symposium on Physical Design, pp. 124–129 (April 1997) (Ex. 1013, “Bertolet”).

⁹ Michael Keating et al., *Low Power Methodology Manual*, Springer (2007) (excerpts) (Ex. 1012, “LPMM”).

II. ANALYSIS

A. Principles of Law

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). This burden of persuasion never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (discussing the burden of proof in *inter partes* review).

A claim is unpatentable as obvious under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence,¹⁰ objective indicia of non-obviousness (i.e., secondary considerations). *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). “To satisfy its burden of proving obviousness, a petitioner cannot employ mere conclusory statements. The petitioner must instead articulate specific reasoning, based on evidence of

¹⁰ At this stage of the proceeding, neither party has provided any evidence or argument regarding objective indicia of non-obviousness.

record, to support the legal conclusion of obviousness.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

We analyze the asserted grounds of unpatentability in accordance with these principles to determine whether Petitioner has met its burden to establish a reasonable likelihood of success at trial.

B. Level of Ordinary Skill in the Art

We consider the grounds of unpatentability in view of the understanding of a person of ordinary skill in the art (sometimes abbreviated herein as “POSITA”). *Graham*, 383 U.S. at 17–18. Petitioner argues that a

POSITA as of November 14, 2008, or November 15, 2007,^[11] would have had a bachelor’s degree in computer science, electrical engineering, computer engineering, or a related field, and approximately two years of experience in the design, development, and/or testing of power distribution networks related to integrated circuits with multiple power domains, or the equivalent, with additional education and/or research substituting for experience and vice versa.

Pet. 16 (citing Ex. 1003 ¶¶ 33–34). Patent Owner does not dispute Petitioner’s definition. Prelim. Resp. 7.

We adopt Petitioner’s proposed definition. We also note that this definition of a POSITA appears to be consistent with the level of ordinary skill in the art that is reflected by the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

¹¹ The application giving rise to the ’218 patent was filed November 14, 2008 and claims a foreign priority date of November 15, 2007. Ex. 1001, code (22), (30).

C. Claim Construction

We interpret a claim “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b).” 37 C.F.R. § 42.100(b). Under this standard, we construe the claim “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” *Id.*; *see also Phillips v. AWH Corp.*, 415 F.3d 1303, 1313, 1321 (Fed. Cir. 2005) (en banc) (stating “the ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention” and “after reading the entire patent” and its prosecution history). Only terms that are in controversy need to be construed, and then only to the extent necessary to resolve the controversy. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999); *see also Nidec Motor Corp. v. Zhongshan Board Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (applying *Vivid Techs.* in the context of an *inter partes* review).

Claim element 12[c] requires “a global power mesh, coupling to the first local power mesh and the second local power mesh, to provide the power needed by the first power domain and the second power domain.” Although neither party provides any particular claim construction analysis for this claim element, the parties’ arguments as to whether the asserted art teaches this claim element turn on claim construction. *See, e.g., See Pet.* 21–27; *Prelim. Resp.* 33–38, 54; *Br.* 1–2 (citing to ITC Order (Ex. 1031)); *Reply Br.* 2. For efficiency and completeness, we address construction of this claim element in the context of the patentability discussion below. No other terms require express construction to resolve any issue in dispute at this

stage of the proceeding.

D. Asserted Obviousness over Jiang, Jiang2, and Jiang3 (Ground 1)

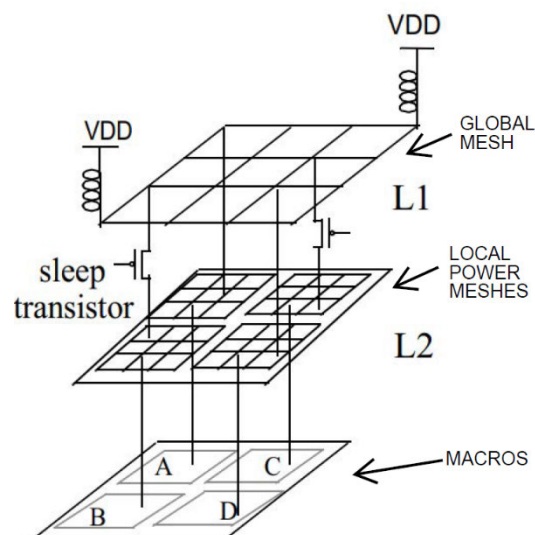
Petitioner argues that claims 12–18 are unpatentable under 35 U.S.C. § 103 over Jiang, Jiang2, and Jiang3. Pet. 17–43.

1. Jiang (Ex. 1004)

Jiang, an article titled “Benefits and Costs of Power-Gating Technique,” reports results of a study of benefits and costs of power-gating techniques in terms of power, area, and performance. Ex. 1004, Abstr. Petitioner contends, and Patent Owner does not dispute, that Jiang was published at least as early as November 8, 2005. Pet. 4.

Jiang states that power-gating is a technique for saving leakage power by shutting off idle blocks using sleep transistors that connect gated blocks to a power supply. Ex. 1004, 1, Abstr.

Figure 1(b), reproduced below (with Petitioner’s annotations at right side added), illustrates a power-gated chip. *Id.* at 1.



Jiang Figure 1(b) illustrates a global mesh connected to a voltage V_{DD} , local power meshes below the global mesh, and macros A, B, C, and D below the local power meshes. *Id.* at 1, 2.

As shown, a local power mesh is provided for each of macros A, B, C, and D. *Id.* The local power meshes for macros A and D are connected directly to the global mesh and, accordingly, macros A and D are ungated. *Id.* at 1, 2, Fig. 1(b). The local power meshes for macros B and C are connected to the global mesh via a respective sleep transistor and, accordingly, each of the macros B and C is gated by its respective sleep transistor and the respective sleep transistor is turned on in order for the corresponding macro to be active. *Id.*

Figure 10 is reproduced below. *Id.* at 7.

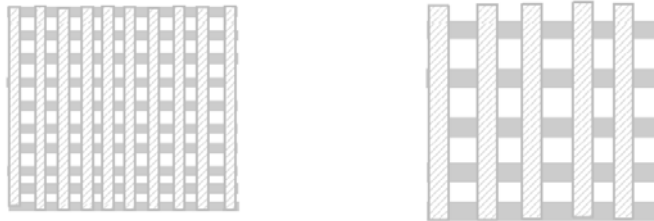


Figure 10 shows power meshes of various granularity. *Id.* The authors “studied the impact of the power mesh granularity on power-gating result [and] kept the area of power mesh constant and changed the width of horizontal and vertical segments.” *Id.*

2. *Jiang2*

Jiang2, an article titled “Power/Ground Supply Network Optimization for Power-Gating,” reports techniques for optimizing power-gating design. Ex. 1007, Abstr. Petitioner contends, and Patent Owner does not dispute, that Jiang2 was published at least as early as November 18, 2005. Pet. 4 (citing Ex. 1021).

Jiang2 describes:

In a power-gating system, a circuit is divided into several power domains. Each domain is *independently* controlled by a sleep-transistor. The sleep transistors are turned off to reduce the dynamic power and leakage power in a standby mode, and turned on in an active mode for normal operation.

Ex. 1007, 1 (emphasis added).

3. *Jiang3*

Jiang3, an article titled “Power-Gating Aware Floorplanning,” reports techniques for evaluating and improving power-gating design. Ex. 1008, Abstr. Petitioner contends, and Patent Owner does not dispute, that Jiang3 was published at least as early as March 26, 2007. Pet. 4 (citing Ex. 1021).

Jiang3 describes:

In a power-gated system, the chip is divided into several domains and local power meshes are constructed for each of them. The local mesh for gated circuit is connected to the global mesh via sleep transistors. The sleep transistors are turned off to reduce the leakage power in a standby mode, and turned on in an active mode for normal operation.

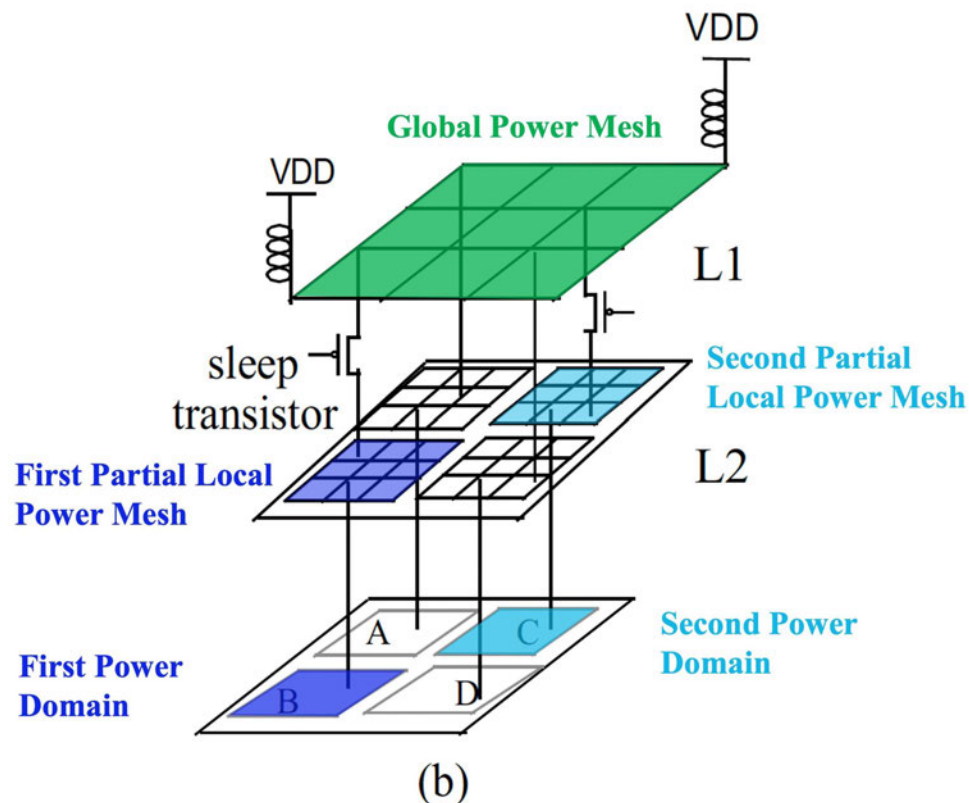
Ex. 1008, 1. Jiang3 further describes, in the context of evaluating designs, “[w]e assume that when power-gating is applied, the gated-blocks are individually power supplied.” *Id.* at 4.

4. *Analysis of Claim 12*

a) *Preamble and Elements 12[a]–[b]*

Petitioner asserts that Jiang discloses a power routing structure having a first and second partial local power mesh that each have a position corresponding to the position of a first and second power domain (e.g., two of the power meshes on L2 in Jiang Figure 1(b) that are coupled to macro A and B), as recited in the preamble and claim elements 1[b]–[c]. Pet. 17–18

(citing Ex. 1003 ¶¶ 71–73; Ex. 1004, 1–2, Fig. 1(b)). Petitioner asserts that this power routing structure is shown in its annotation of Jiang Figure 1(b), reproduced below:



Petitioner’s annotated Jiang Figure 1(b) depicts a power-gating system with colored annotations added to identify first power domain (macro B) and second power domain (macro C), each coupled to and directly below their corresponding partial local mesh. Pet. 22; Ex. 1003 ¶¶ 77–79; Ex. 1004, 2.

Petitioner further asserts that because Jiang2 and Jiang3 specifically reference Jiang, and all three references have the same first named author, a POSITA working on power routing for power-gated chips would readily look to these two references to understand terminology in Jiang. Pet. 18 (citing Ex. 1003 ¶ 73). Patent Owner does not dispute Petitioner’s

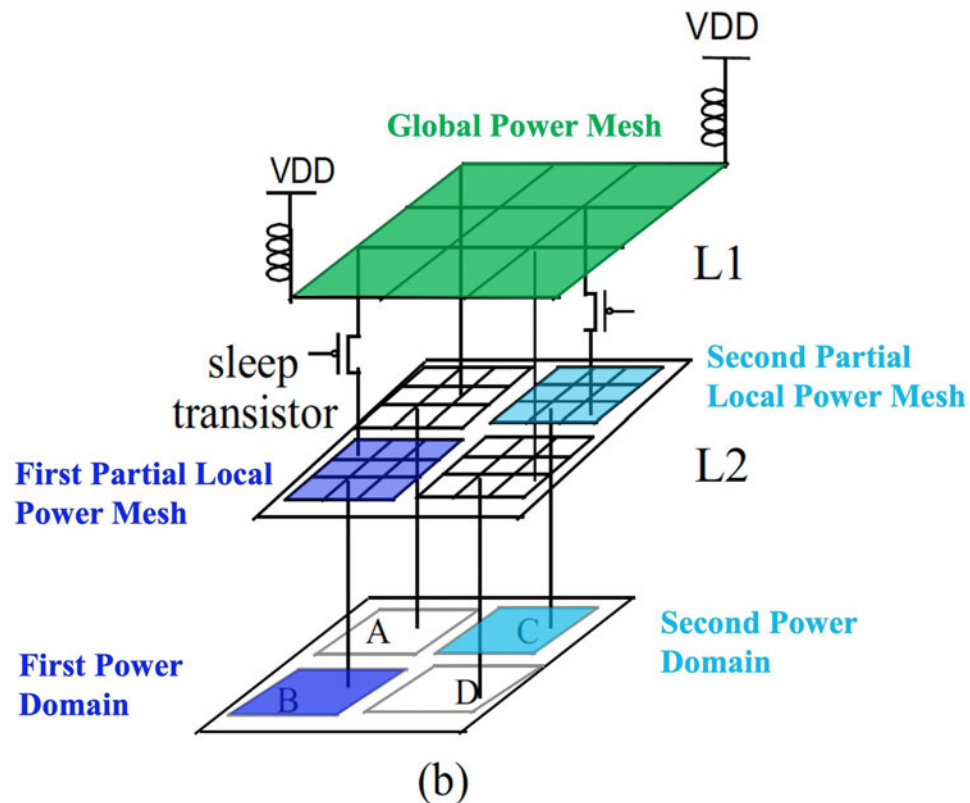
assertions.¹² We have reviewed Petitioner’s argument and evidence and determine Petitioner has shown sufficiently that Jiang discloses the preamble¹³ and the limitations recited in claim elements 12[a]–[b].

b) Claim element 12[c]

Claim element 12[c] recites “a global power mesh, coupling to the first local power mesh and the second local power mesh, to provide the power needed by the first power domain and the second domain separately.” Ex. 1001, 7:63–66. Petitioner contends that Jiang discloses this claim element because Jiang’s “global mesh” is coupled to the first and second partial local meshes via sleep transistors, as shown in annotated Jiang Figure 1(b) below. Pet. 21–22 (citing Ex. 1004, 1, Fig. 1(b)).

¹² Although Patent Owner states that it does not concede that Jiang discloses the other elements of the claim, including for example, a first and second power domain, Patent Owner does not provide any particularized argument that Jiang does not disclose the recited power domains. Prelim. Resp. 31 n.4.

¹³ Because we determine Petitioner sufficiently shows that Jiang discloses the material recited in the preamble, we need not determine whether the preamble is limiting.



Petitioner asserts that by gating the first and second partial local power meshes (and power domains) with sleep transistors, Jiang is able to provide power (VDD) to each power domain separately by switching its respective sleep transistor. Pet. 22 (citing Ex. 1004, Abstract, 1–2, 6; Ex. 1003 ¶¶ 80–81). Petitioner further asserts, to the extent not expressly disclosed, it would have been obvious for Jiang’s sleep transistors to be independently operable to reduce leakage power consumption and also because both Jiang2 and Jiang3 disclose independently operable sleep transistors. Pet. 23 (citing Ex. 1003 ¶¶ 81–85; Ex. 1007, 1; Ex. 1008, 4; Ex. 1009, 1; Ex. 1010, 1:37–43).

Patent Owner first argues that Jiang does not teach claim element 12[c] because Jiang’s sleep transistors are not part of the global power mesh, and therefore Jiang’s global power mesh lacks the structure allowing it to

provide the power “separately” as the required by the claims. Prelim. Resp. 29–32; Paper 9. Patent Owner also asserts that because Jiang’s global mesh has only one power supply, Jiang must deliver either (1) the same power through the same wiring of the global power mesh to the chip circuitry or (2) no power, which cannot satisfy the claim element of providing the power needed by the second power domain. Prelim. Res. 31.

We disagree with Patent Owner. As noted above, claim element 12[c] recites “a global power mesh, coupling to the first local power mesh and the second local power mesh, to provide the power needed by the first power domain and the second domain separately.” Neither party has provided an express or detailed claim construction analysis of this claim language. Nor does the ’218 patent appear to indicate that the phrase recited in claim element 12[c] should be afforded any special definition. *See* Ex. 1001. A plain and ordinary reading of this phrase, however, indicates that the global power mesh must be able to provide power needed by the first and second power domains separately. Pet. 21–22; Ex. 1004, Abstract, 1–2, Fig. 1(b); Ex. 1003 ¶¶ 78–85. Petitioner sufficiently shows that Jiang’s global power mesh is able to provide power separately to the first and second power domains by selectively turning off and on each domain’s sleep transistors, each of which is provided power by the global mesh.¹⁴ Pet. 22–23 (citing Ex. 1003 ¶ 81). Dr. Subramanian explains that the use of sleep transistors between the global power mesh and the first and second local power meshes enables the global power mesh to power each domain “separately” by

¹⁴ Petitioner has sufficiently shown, and Patent Owner does not dispute, that Jiang teaches sleep transistors are independently operable. Pet. 22–23; Ex. 1004, Abstract, 1–2, Fig. 1(b); Ex. 1003 ¶¶ 81–85.

selectively turning off each domain's sleep transistor when desired. Ex. 1003 ¶ 81 (citing Ex. 1004, Abstract, 1, 2). Dr. Subramanian further explains that turning off the power to the local power mesh, through use of the sleep transistors, will necessarily turn off the power to the macro (power domain) underlying the partial local power mesh. Ex. 1003 ¶ 81. Thus, Petitioner's argument and evidence that Jiang discloses connecting global power mesh power VDD to the gated macros (power domains) through the sleep transistors and the local meshes provides a sufficient showing that Jiang discloses a global power mesh that provides power to the power domains through the sleep transistors and local power meshes.

Additionally, the claim language requires the global power mesh to provide "the power needed" by the domains. Ex. 1001, 7:65–66. If no power is needed, turning off the power appears to satisfy this requirement. As such, Petitioner sufficiently shows that Jiang's global power mesh is able to provide power separately to the first and second power domains by selectively turning off and on each domain's sleep transistors.¹⁵

Our preliminary interpretation of the claim term is consistent with that of the ITC, which stated that the plain and ordinary meaning of "provide the power . . . separately" would likely include "provid[ing] the power through separate circuitry and would not require "provid[ing] different voltages through different wiring to different power domains." Ex. 1031 (ITC Order), 9; *see also* Papers 8, 9 (briefing by Petitioner and Patent Owner respectively addressing the ITC Order). The ITC further states that a

¹⁵ Petitioner has sufficiently shown, and Patent Owner does not dispute, that Jiang teaches sleep transistors are independently operable. *See* Pet. 22–23; Ex. 1004, Abstract, 1–2, Fig. 1(b); Ex. 1003 ¶¶ 81–85.

coupling that allows selective distribution of power, such as that provided by Jiang, would seem to meet this limitation. Ex. 1031, 9.

Like the ITC, we also recognize that the '218 patent discloses an embodiment in which a two-layer global power mesh has separate wiring from separate power supplies so that the power needed by any single power domain is supplied separately from that of other domains. *See* Prelim. Resp. 1 (citing Ex. 1001, 5:10–20); Ex. 1031, 9. We do not, however, read this disclosure as a limitation that must be read into the claim. The '218 patent identifies this embodiment as “one embodiment of the invention.” Ex. 1001, 5:10–14. A particular embodiment appearing in the written description, “may not be read into a claim when the claim language is broader than the embodiment.” *Superguide Corp. v. DirecTV Enterprises, Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004).

Thus, we decline to limit the scope of the claim as urged by Patent Owner. The parties are invited to address this claim construction issue during trial. *See* Consolidated Trial Practice Guide, 44–45, available at www.uspto.gov/TrialPracticeGuideConsolidated (discussing claim construction).

Accordingly, based on the record presented, we determine, for purposes of this Decision, Petitioner has shown sufficiently Jiang teaches the limitations recited in claim element 12[c], notwithstanding Patent Owner's counter argument.

c) Claim element 12[d]

Claim element 12[d] recites “wherein the first partial local power mesh and the second partial local power mesh are positioned on the same metal layer while the global power mesh and the first local power mesh are

positioned on different metal layers.” Ex. 1001, 8:1–5. Petitioner asserts that Jiang discloses that limitation by stating that partial local power meshes are on the same metal layers L2 while the global power mesh is on metal layers L1. Pet. 28 (citing Ex. 1004, Fig. 1(b), 2; Ex. 1003 ¶ 94).

Patent Owner does not dispute Petitioner’s assertions. *See generally* Prelim. Resp. We have reviewed Petitioner’s argument and device and determine Petitioner has shown sufficiently that Jiang discloses the limitations recited in claim element 12[d].

d) Claim elements 12[e]-[f]

Claim element 12[e] recites “wherein the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer” and claim element 12[f] recites “wherein the first metal layer and the second metal layer are different layers.” Ex. 1001, 8:1–11.

Petitioner asserts Jiang teaches these limitations because a POSITA would have understood that the horizontal and vertical wires in Jiang’s global power mesh would be on different layers. Pet. 29–30, 33 (citing Ex. 1004, 7, Figs. 1(b), 10; Ex. 1003 ¶¶ 95–96, 103). Petitioner also asserts that to the extent these limitations are not expressly disclosed in Jiang, that it would have been obvious to route power grid wires horizontally and vertically on alternating metal layers as a routine application of the “normal” routing structure with a reasonable expectation of success, given its ubiquitous usage. Pet. 32–33 (citing Ex. 1003 ¶¶ 102–103).

Patent Owner responds that Jiang’s Figure 1(b) only discloses a single layer, and thus does not disclose the first and second metal layers required by claim element 12[e]. Prelim. Resp. 25–27. Patent Owner further asserts

that Jiang Figure 10 is a separate embodiment and that Petitioner has not sufficiently shown a reason to combine disparate embodiments. Prelim. Resp. 27–29.

After considering Patent Owner’s arguments, we are persuaded that Petitioner provides sufficient evidence and argument at this stage of the proceeding that a POSITA would have understood that the global power mesh of L1 of Figure 1(b), comprising both horizontal and vertical segments, is made up of multiple layers. For example, Petitioner’s argument that a POSITA would have understood that the global power mesh of Jiang Figure 1 has multiple layers is supported by Dr. Subramanian’s testimony that a POSITA would have understood that the mesh’s horizontal and vertical wires would have been on different layers. Ex. 1003 ¶ 96.

Petitioner also cites to Jiang Figure 10, as well as to meshes depicted in additional references, to support its argument that a POSITA would have understood that meshes having both horizontal and vertical wires would have the horizontal wires on one layer and the vertical wires on a second layer. *See* Pet. 29–30 (citing Ex. 1004, Fig. 10; Ex. 1003 ¶ 96); *see also id.* (identifying other references that depict horizontal and vertical wires of a mesh on different metal layers and citing Ex. 1005 (Li), Fig. 3; Ex. 1006 (Chiu), Fig. 7; Ex. 1015 (Ran), Fig. 3(a)). Pet. 29; Ex. 1003 ¶¶ 94–96).

Dr. Subramanian also testifies that using horizontal power supplies wires on one metal layer and vertical power supply wires on a second different metal layer was a well-known basic feature of integrated design. Ex. 1003 ¶ 100 (citing Ex. 1016 (US 7,671,623), 8:57–59; Ex. 1018 (US 6,925,627), 9:17–23; *see also* Ex. 1003 ¶ 96 (stating the “use of single direction wires on a single metal layer is ubiquitous in the industry and citing Ex. 1004, Figure

10). How much weight to credit Dr. Subramanian’s testimony, and whether a POSITA would have understood Jiang to disclose or suggest a global mesh having two layers, is best resolved on a full record.

Accordingly, based on the record presented, we determine, for purposes of this Decision, Petitioner has shown sufficiently Jiang teaches the limitations recited in claim element 12[e]–[f], notwithstanding Patent Owner’s counter argument

e) Conclusion Claim 12

Upon review of the parties’ arguments and evidence, we determine that Petitioner demonstrates a reasonable likelihood that claim 12 would have been obvious over Jiang, Jiang2, and Jiang3. *See* Pet. 33–43.

5. Claims 13–18

Claims 13–18 depend either directly or indirectly from claim 12. Ex 1001, 8:12–38. Petitioner asserts that claims 13–18 would have been obvious over Jiang, Jiang2, and Jiang3. Pet. 33–43. Patent Owner does not address Petitioner’s arguments with respect to these dependent claims apart from its arguments directed to independent claim 12. *See generally* Prelim. Resp. Upon review of the parties’ arguments and evidence, we determine that Petitioner demonstrates a reasonable likelihood that claims 13–18 would have been obvious over Jiang, Jiang2, and Jiang3. *See* Pet. 33–43.

Furthermore, because we determine that Petitioner has shown a reasonable likelihood of prevailing at trial in demonstrating that at least one claim is unpatentable on at least one of the stated Grounds, we institute *inter partes* review of all challenged claims of the ’218 patent based on the remaining grounds identified in the Petition. *See SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018); *PGS Geophysical AS v. Iancu*, 891 F.3d

1354, 1360 (Fed. Cir. 2018) (interpreting the statute to require “a simple yes-or-no institution choice respecting a petition, embracing all challenges included in the petition”). Nevertheless, we provide our preliminary views with respect to remaining challenges below, based upon the parties’ arguments and the evidence of record as presently developed.

E. Asserted Obviousness over Jiang, Jiang2, Jiang3 with Li or Chiu (Ground 2)

Petitioner argues that claims 12–18 would have been unpatentable under 35 U.S.C. § 103 over Jiang, Jiang2, and Jiang3 and further in view of Li or Chiu. Pet. 17–43 (incorporating Petitioner’s Ground 2 arguments within its Ground 1 arguments).

1. Li

Li is an article titled “LVS Verification across Multiple Power Domains for a Quad-Core Microprocessor” that describes a methodology for the verification of a four-core microprocessor with multiple power domains. Ex. 1005, Abstr. Petitioner contends Li was published at least as early as April 1, 2006. Pet. 4 (citing Ex. 1021).

Li describes power distribution in a BCM1280 chip. Ex. 1005, 492–95.¹⁶ Figure 1, reproduced below, illustrates the chip.

¹⁶ We cite to the page numbers in the original document.

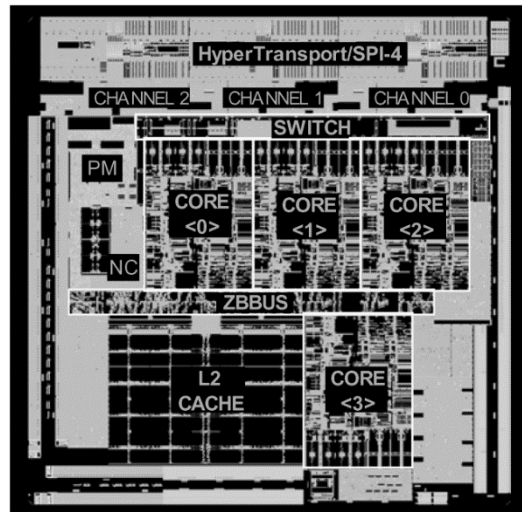


Figure 1 above illustrates a detailed floorplan of a quad-core microprocessor. *Id.* at 491.

Li explains that “[a]s a result of function and logic requirements, there are multiple voltage regions across the chip. Ex. 1005, 493. Li explains how power is applied to the chip as follows:

Power and ground are supplied to the package through two VDD inputs (VDD_switch and VDD_chip) and one GND input, respectively. Pads arrayed across the active face of the die are used to connect to I/O, power and ground. Solder bumps are attached to pads. A redistribution metal layer is designated for distributing power and ground from the bump to the chip level power grid.

Id.

Li further explains:

Metal-6 and metal-7 are extensively used in distributing power and ground across the chip. Ground (GND) and power (VDD_chip, VDD_switch) lines are routed alternately on Metal-6 in the vertical direction and Metal-7 in the horizontal direction. This forms the power grid structure at the chip top level. The power and ground lines in the local sections are grided on Metal-2 through Metal-5, on which the local power grids are formed at the block level.

Id.

Figure 3, reproduced below, illustrates the power distribution. *Id.* at 493–94.

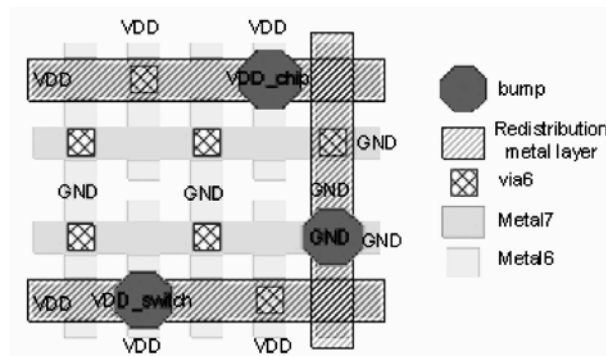


Figure 3 above illustrates power and ground distributed from bumps onto the chip-level power grid through a redistribution metal layer. *Id.* at 493–94.

2. *Chiu*

Chiu, an article titled “Method and Apparatus for Buffering Signals in Voltage Domains,” is directed to “integrated circuits having more than one voltage domain and that are capable of buffering signals in the integrated circuit, and more particularly, to buffering signals in a voltage domain of an integrated circuit that is capable of being powered down independent of another voltage domain of the integrated circuit.” Ex. 1006, code (54), 1:16–22. Chiu issued on May 24, 2011 based on an application filed June 5, 2008, and claims priority to a provisional application filed September 28, 2007. *Id.* at codes (22), (45), (60); *see also* Ex. 1011. Petitioner asserts that Chiu is prior art under § 102(e) based on its provisional application date of September 28, 2007.

Figure 1, reproduced below, is a block diagram of one example of an integrated circuit in accordance with the prior art. Ex. 1006, 7:7–8.

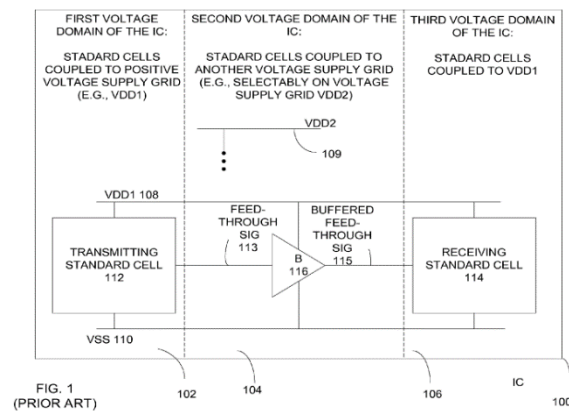


Figure 1 above illustrates integrated circuit 100, first voltage domain 102, second voltage domain 104, and third voltage domain 106. *Id.* at 1:52–2:43.

In Figure 1, first voltage domain 102 and third voltage domain 106 are associated with a positive voltage supply grid VDD1 108 while second voltage domain 104 is associated with another voltage supply grid VDD2 109. *Id.* VDD2 109 is a selectably on voltage supply grid capable of being powered up and powered down such that cells in second voltage domain 104 are also capable of being selectively powered up and powered down. *Id.*

Chiu further describes:

In prior art cell layouts where the substantially horizontal members of each of the power supply grids VDD1 108, VDD2 109 and VSS 110 are primarily used to distribute the associated voltage level of the grid throughout integrated circuit 100, the substantially vertical members of each power supply grid are primarily used to provide electrical connectivity to cells within corresponding and respective voltage domains. According[ly], *the substantially horizontal members are typically located in a higher metal layer than the corresponding substantially vertical members of the power supply grids.*

Id. at 5:8–24 (emphasis added).

3. *Analysis for Claim 12*

a) *Whether Petitioner has sufficiently shown Chiu qualifies as pre-AIA § 102(e) prior art*

A petitioner carries a burden of production to show in its petition that the asserted references qualify as prior art. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1380 (Fed. Cir. 2015) (explaining that petitioners bear the initial burden to establish that the asserted references qualify as prior art). Petitioner asserts that Chiu is prior art under pre-AIA § 102(e) based on its provisional application date of September 28, 2007.

Pet. 5. To support its argument that Chiu qualifies as pre-AIA § 102(e) prior art, Petitioner merely states that “Chiu’s provisional application contains a largely identical disclosure to the utility application that issued as Chiu and is entitled to its earliest priority date. *Compare* EX1006 *with* EX1011.”

Pet. 5.

As an initial matter, we consider whether Petitioner has sufficiently shown that Chiu qualifies as pre-AIA § 102(e) art.

A reference patent or published patent application can be entitled to the benefit of its provisional application’s filing date for pre-AIA 35 U.S.C. § 102(e) prior art purposes on two conditions. First, the provisional application must provide sufficient support for at least one claim in the reference patent or published patent application. *See Dynamic Drinkware*, 800 F.3d at 1381 (“A reference patent is only entitled to claim the benefit of the filing date of its provisional application if the disclosure of the provisional application provides support for the claims in the reference patent in compliance with § 112, ¶ 1.”).

Second, the provisional application must provide sufficient support for the subject matter relied upon for prior art purposes in the reference patent or published patent application. *See In re Giacomini*, 612 F.3d 1380, 1383 (Fed. Cir. 2010) (“[A]n applicant is not entitled to a patent if another’s patent discloses the same invention, which was carried forward from an earlier U.S. provisional application or U.S. non-provisional application.”); *Ex parte Mann*, 2016 WL 7487271, at *5 (PTAB Dec. 21, 2016) (stating that the party claiming priority also must show that the subject matter relied upon in the non-provisional is sufficiently supported in the provisional application [and that t]his subject matter test is in addition to the comparison of claims required by *Dynamic Drinkware*”);

Here, Petitioner fails to sufficiently show that Chiu’s Provisional Application (Ex. 1011) provides written description support for either (1) any claim of Chiu or (2) the subject matter that Petitioner relies upon in Chiu for prior art purposes. Petitioner provides no comparison or analysis of the material disclosed in Chiu’s Provisional Application with either Chiu’s claims or the subject matter in Chiu that Petitioner relies upon in its unpatentability argument. *See* Prelim. Resp. Petitioner’s invitation to the Board to compare the disclosure of Chiu and Chiu’s provisional application is not sufficient to meet this burden. *See Benitec Biopharma Ltd. v. Cold Spring Harbor Labs.*, IPR2016-00016, Paper 8 at 9 (PTAB Mar. 31, 2016) (stating the petitioner failed to provide sufficient evidence that the asserted reference qualified as prior art when it failed to provide expert testimony or sufficient evidence that the provisional application provides support for the claims in the asserted reference); *Comcast Cable Commc'ns, LLC v. Promptu Sys. Corp.*, IPR2018-00345, Paper 10 at 25–26 (PTAB July 2,

2018) (stating the petitioner’s “barebones analysis” was insufficient to show “how the [provisional underlying the asserted reference] provides support for the subject matter relied upon [in the asserted reference]”). Accordingly, Petitioner has not shown that Chiu is entitled to the priority date of its provisional application, and thus has not sufficiently shown that Chiu qualifies as prior art to the ’218 patent.

b) Analysis for Claim 12

In Ground 2, Petitioner relies on Li or Chiu for teaching a global mesh that provides power separately to the first and second power domains. Pet. 24–27. As noted above, Petitioner asserts Jiang’s global power mesh provides power separately to the first and second power domains through sleep transistors. Pet. 21–23. Petitioner states that, although not required by the claims, it would have been obvious to modify Jiang’s global power mesh to provide independent supply voltages to the first and second power domains because it was common practice to have different power domains coupled to different powers. Pet. 24 (citing Ex. 1003 ¶¶ 86–93; Ex. 1001, 1:28–31; Ex. 1012, 157, Figs. 11–12)). Petitioner cites to Li as teaching an integrated circuit having two power supply inputs (VDD_chip, VDD_switch) and a global power mesh having horizontal and vertical wires that carry the independent supply voltages from the separate power supply inputs. Pet. 24–25 (citing Ex. 1005, 491, 493–495, Fig. 3; Ex. 1003 ¶ 88). Petitioner also states Chiu similarly discloses a chip with multiple voltage domains where a global power mesh supplies separate voltages to different domains. Pet. 25–26 (citing Ex. 1006, Fig. 7; Ex. 1:54–60; Ex. 1003 ¶ 89).¹⁷

¹⁷ We repeat Petitioner’s contentions regarding Chiu for completeness. The Board’s analysis, however, does not rely upon Chiu.

Petitioner asserts that a POSITA would have been motivated to use separate power supplies to supply independent voltages to Jiang's power meshes to supply different power domains with different voltages in order to increase Jiang's power savings. Pet. 26–27 (citing Ex. 1003 ¶¶ 85–93; Ex. 1004, 1; Ex. 1001, 1:26–28; Ex. 1014, 3; Ex. 1012, 16–17, 177–178; Ex. 1010, 6:19–31). Petitioner asserts that applying independent supply voltages to Jiang's global power mesh would have been a routine application of a known feature with a reasonable expectation of success. Pet. 27 (citing Ex. 1001, 1:26–33; Ex. 1003 ¶ 93).

Patent Owner argues that Petitioner's "generic motivations" to "increase power savings" fail to provide sufficient motivation to modify Jiang's power gating system to supply multiple voltages. Prelim. Resp. 33–39. Patent Owner asserts that the devices in each reference operates effectively and that Petitioner has not offered any motivation to modify what Jiang has already achieved. Pet. 38–39.

On the present record, we disagree with Patent Owner. Petitioner asserts that a POSITA would have understood that different portions of a chip have different power requirements and that providing high voltages to the portions requiring high voltages and providing lower voltages (as opposed to no voltage) to the portions of the rest of the chip that require lower voltages would result in power savings. *See* Pet. 26–27; Ex. 1003 ¶¶ 90–93. Whether it would have been obvious to replace Jiang's global power mesh with a mesh having two separate power sources is an issue that is best resolved on a full record.

4. *Analysis of Claims 13–18*

Petitioner asserts dependent claims 13–18 would have been obvious over Jiang, Jiang2, Jiang3 in view of either Li or Chiu. Pet. 33–44. Patent Owner does not separately argue the patentability of these claims at this stage in the proceeding. *See generally* Prelim. Resp. Based on the preliminary record before us, we find that Petitioner’s arguments and evidence are sufficient to show a reasonable likelihood Petitioner would prevail in proving unpatentability of dependent claims 13–18 in view of Jiang, Jiang2, Jiang3, and Li. *See* Pet. 33–44.

F. Asserted Obviousness of Claims 1–11 and 19–20 over Jiang, Jiang2, and Jiang3 with Bertolet or LPMM (Ground 3a) or over Jiang, Jiang2, and Jiang3, Li, and Chiu in Combination with Bertolet or LPMM (Ground 3b)

Petitioner argues that claims 1–11 and 19–20 are unpatentable under 35 U.S.C. § 103 over the art asserted in Ground 1 (Jiang, Jiang2, and Jiang3) or in Ground 2 (Jiang, Jiang2, Jiang further in view of Li or Chiu) in further view of Bertolet and LPMM. Pet. 43–52.

1. *Bertolet*

Bertolet, titled “A Pseudo-Hierarchical Methodology for High Performance Microprocessor Design,” reports a methodology to construct complex high performance microprocessors that includes algorithmic power grid generation. Ex. 1013, Abstr. Petitioner contends Bertolet was published at least as early as April 1, 1997. Pet. 5 (citing Ex. 1021).

Bertolet describes “[a] ‘pseudo-hierarchical’ design approach [] applied to manage the floorplan, placement, and routing optimization of the

standard cell control logic.” Ex. 1013, 124.¹⁸ The method includes power routing wherein:

After custom macrocell placement, a power distribution network is algorithmically generated using a custom SKILL program. The power grid is generated on five levels of metal with multiple width wires and pitches supported on each metal level. The algorithm provides the capability to define multiple power terrains by area and level of metal. For example, two areas of the chip may have completely unique grids on all layers. Two other areas of the chip may share a common power grid on metal levels one and two, yet have different power grids on metal levels three through five.

Id. at 126.

“The final integration cycle includes a fully custom, algorithmically generated power distribution on five layers of metal that includes legal standard cell core site definition based on power analysis.” *Id.* at 125.

2. LPMM

LPMM is made up of excerpts from a manual, titled “Low Power Methodology Manual For System-on-Chip Design.” Ex. 1012, 3. Petitioner contends LPMM was published at least as early as June 4, 2007 or July 31, 2007. Pet. 5 (citing Exs. 1021, 1027).

LPMM describes projects that explored clock gating, multi-voltage, dynamic voltage scaling, and power gating. Ex. 1012, 13. LPMM describes power planning, that is, how to provide power to the various voltage areas in the design. *Id.* at 60. LPMM explains that most:

tools provide some level of automated power network synthesis (PNS) capability for the distribution of power across a design. We recommend highly that the implementation of a multi-voltage design utilize this type of PNS capability wherever

¹⁸ We cite to the page numbers in the original document.

possible. The number of concurrently changeable variables in a multi-voltage system is such that attempting to construct a power plan manually may result in a suboptimal result both in terms of routing resources consumed and the voltage drop on the rails.

Id. at 60. LPMM further describes “the sleep transistor power network can be synthesized using a power planning tool.” *Id.* at 61.

3. *Analysis for Claim 1*

Petitioner asserts that claim 1 is directed to a method of using an automatic placement and routing (APR) tool for creating a power routing structure that would be met by the routing structure in claim 12. Pet. 43 (citing Ex. 1003 ¶¶ 122–123). Petitioner asserts that it would have been obvious to use to use an APR tool, such as that taught in Bertolet or LPMM, to form the power routing structure recited in claim 12 because it was well known to use an APR tool to employ a power routing arrangement method when designing integrated circuits. Pet. 43–44 (citing Ex. 1001, 1:37; Ex. 1003 ¶¶ 124–126; Ex. 1012, 177–178; Ex. 1013, 126); *see also* Pet. 43 (stating that the first and second power domains, first and second local power meshes, and global power mesh recited in claim 1 are disclosed or rendered obvious for the reasons asserted regarding claim elements 12[a]–[c] and [e]–[f]). Pet. 43 (citing *inter alia* Ex. 1003 ¶ 124).

Petitioner further asserts Bertolet describes using a program to algorithmically generate a power distribution network, and that Bertolet’s algorithm can generate a routing structure that includes a global common power grid on two metal levels and local power grids on two additional metal levels. Pet. 44 (citing Ex. 1013, 126). Petitioner asserts that LPMM similarly teaches using an APR tool to synthesize a power network. Pet. 44–45 (citing Ex. 1003 ¶ 127; Ex. 1012, 177–178). Petitioner asserts it would

have been obvious to use an APR tool to form Jiang's power meshes and to couple the entire power routing structure because using an APR tool would save time and effort in chip design. Pet. 45 (citing Ex. 1003 ¶ 128; Ex 1024, 5:28–32; Ex. 1012, 177–178). Petitioner further asserts that a POSITA would have had a reasonable expectation of success in using an APR tool to form Jiang's meshes and to couple them to Jiang's power domains because using an APR tool to form and couple Jiang's power meshes would be no more than using well-known techniques to achieve a predictable outcome. Pet. 45–46 (citing Ex. 1003 ¶ 129). Petitioner states LPMM specifically teaches that a “power-gating design” such as a “sleep transistor network can be synthesized using a power planning tool,” and argues that Bertolet confirms that a power distribution network with global and local grids on different metal layers can be algorithmically generated. Pet. 46 (citing Ex. 1013, 126; Ex. 1004, 1–2). Finally, Petitioner asserts that the use of a commercially available APR tool to design multi-voltage power routing structures had been done before the filing of the '218 patent. Pet. 46 (asserting that the '218 patent's statement that APR tools can only support circuits having a single power domain is wrong and citing Ex. 1001, 1:37–39; Ex. 1020, 3; Ex. 1025; 1026).

Patent Owner responds that Petitioner cannot rely on its analysis of claim 12 to show unpatentability of claim 1 because claim 1 relates to use of APR tools to perform method claims while claim 12 relates to a structure and does not recite the use of APR tools to perform any method steps. Prelim. Resp. 19. Patent Owner also argues that Petitioner fails to provide a limitation by limitation analysis with respect to claim 12; Patent Owner

provides a chart to emphasize the differences between the claims 1 and 12. Prelim. Resp. 19–23.

We disagree with Patent Owner’s arguments. As Patent Owner’s own chart demonstrates, method claim 1 is essentially directed to a power routing method using an APR tool for forming and coupling the power meshes and power domains that are recited in claim 12. Prelim. Resp. 19–23. Petitioner provides sufficient argument and evidence to show a reasonable likelihood that it would have been obvious to a POSITA to use well-known APR tools, such as those taught in Bertolet and LPMM, to form the power arrangement structure of claim 12 and to couple the Jiang’s power meshes as shown in Jiang’s Figure 1(b) (thus meeting the “coupling” limitations of claim 1[d]) with a reasonable expectation of success. *See* Pet. 43–46.

To the extent Patent Owner contends that Petitioner must identify an APR tool that has, in fact, performed each of the steps recited in claim 1, we disagree. *See* Prelim. Resp. 24 (stating the prior art does not disclose use of APR tools in the manner claimed). Petitioner’s argument is based on its contention that both Bertolet and LPMM teach the use of APR tools to generate power distribution networks and that a POSITA would have found it obvious to use an APR tool to form and couple the global and partial local power meshes and power domains as recited in claim 12 in the manner recited in claim 1. Patent Owner’s argument that it would not have been obvious to use an APR tool in the method of claim 12 is a matter best resolved on a full record.

4. Analysis for Claim 2–11 and 19–20

Petitioner argues that it would have been obvious to a POSITA to use an APR tool, such as that taught in LPMM or Bertolet, in an arrangement

method to form the structures that are recited in independent claim 19 and dependent claims 2–11 and 20. Pet. 47–52. Petitioner identifies which limitations in claim 2–11 and 19–20 are found in claims 12–18. *Id.* Patent Owner’s argument for patentability for claims 2–11 and 19–20 are the same as for claim 1 (Prelim. Resp. 18–25) and are similarly unpersuasive.

G. Asserted Obviousness of Claims 12–18 over Li and Jiang (Ground 4)

Petitioner argues that claims 12–18 are unpatentable under 35 U.S.C. § 103 over Li and Jiang and provides argument and evidence as to where the art discloses or suggests each limitation and a reason to combine the references. *See* Pet. 52–70.

Patent Owner responds that Petitioner has not shown that Li or Li and Jiang disclose or suggest the first and second local power meshes recited in claim elements 12[a] and 12[b]. Prelim. Resp. 56–60. In particular, Patent Owner asserts that Li is silent as to where each of the local sections of the local power meshes are located in relation to the power domains and, thus, does not disclose or suggest first or second local power meshes having a position corresponding to their respective power domains. *Id.* Patent Owner also argues that Petitioner fails to support its argument that Li’s local power grids sit above their respective domains, fails to provide motivation to modify the placement of Li’s power grids in light of Jiang, and fails to identify any reasonable expectation of success for combining Li and Jiang. *Id.* at 58–64.

Patent Owner’s arguments raise a factual dispute best resolved on a full record. We have reviewed Petitioner’s contentions and determine that Petitioner has made a sufficient showing that Li and Jiang teach or suggest each of the limitations of claims 12–18 and has articulated a reasonable

rationale for combining the references (Pet. 52–70), notwithstanding Patent Owner’s arguments to the contrary. For example, Petitioner sufficiently shows Li discloses a first partial power domain (Cores <0>, <1>, <2>, or <3>) (Pet. 54), a second partial power domain (Li’s “switch” or the region powered by VDD_switch and encompassing the “switch”) (Pet. 58–59), and a global power mesh (the top-level power grid on metal layers 6–7) (Pet. 59–60). Petitioner also sufficiently shows that Li teaches a plurality of local power meshes (local power grids on metal layers 2–5) (Pet. 54, 59 (citing Ex. 1005, 493; Ex. 1003 ¶ 62)).

Petitioner also sufficiently shows at this stage of the proceeding that either Li, or Li and Jiang, teach or suggest claim elements 12[a]–[b]. For example, Petitioner first asserts that Li’s local power grids (first and second partial local power meshes) necessarily correspond to the position of their respective power domains, as required by claim elements 12[a]–[b] because the power grids supply power to the power domains, sit above their respective power domains, and provide power vertically downward into the circuitry Pet. 55 (citing Ex. 1005, 493; Ex. 1003 ¶¶ 152–153). Petitioner next asserts that it would have been obvious for Li’s local power grids to correspond to the positions of their respective power domains because a POSITA would understand that it is preferable to have local grids cover only the same surface area as the domains to which they supply power. Pet. 55 (stating that a local grid covering more than its underlying power domain would waste local resources and citing Ex. 1003 ¶ 155; Ex. 1006, 91:4–18; Ex. 1016, 5:14–18). Petitioner also asserts that Jiang discloses local grids that correspond to the positions of its power domains and that having Li’s local power grids correspond to their respective power domains would have

been a simple, efficient way to route power from supply inputs to power domains in Li's circuits and that doing so would merely combine prior art elements according to known methods to yield predictable results. Pet. 55–56 (citing Ex. 1003 ¶¶ 155–156).

Alternatively, Petitioner asserts that it would have been obvious to implement Li's local power grids as a web-like structure of horizontal and vertical power supply wires to be similar to Li's global power grid and because a POSITA would know that power grids are typically a meshing of horizontal and vertical metal rails on two metallization layers. Pet. 56–57 (citing Ex. 1004 ¶ 157; Ex. 1016, 8:57–59; Ex. 1019, 4:57–64, Fig. 2). Petitioner further asserts that a POSITA would have known partial local grids would not be interconnected, as taught by Jiang Figure 1(b), to save power. Pet. 57–58 (citing Ex. 1004, 1–2, Fig. 1(b); Ex. 1003 ¶¶ 157–159; Ex. 1005, 496).

These contentions are sufficient to show that Petitioner has established a reasonable likelihood of demonstrating that claim 12 would have been obvious over Li or over Li and Jiang. Patent Owner's arguments to the contrary raise issues best resolved on a full record.

H. Asserted Obviousness of Claims 1–11 and 19–20 over Li, Jiang, Bertolet or LPMM (Ground 5)

Petitioner argues that method claims 1–11 and 19–20 are unpatentable under 35 U.S.C. § 103 over Li and Jiang in combination with Bertolet or LPMM. Pet. 70–77. Petitioner asserts that it would have been obvious to form and couple the global power mesh, the partial local power meshes, and the power domains recited in claim 12 (as set forth in Ground 4) with an APR tool for the same reasons set forth in Ground 3. Patent Owner responds

that Petitioner’s arguments for Ground 5 fail for the same reasons set forth with respect to Grounds 3 and 4. Prelim. Resp. 64–66. Patent Owner’s arguments are unpersuasive at this stage of the proceeding for the same reasons set forth above with respect to Grounds 3 and 4.

I. Discretionary Denial under 35 U.S.C. § 314(a)

Patent Owner asks the Board to exercise its discretion under § 314(a) and deny the Petition. Prelim. Resp. 3–4, 10–25. Patent Owner first argues that the “Petition lacks particularity” because Ground 3 is a “catch-all” ground combining an “indeterminate number of potential references, resulting in un-defined and unbounded scope of the challenge.” *Id.* at 3, 14–16. In particular, Patent Owner notes that Ground 3 involves “any of the combinations in Grounds 1–2” in combination with either one of two other references, which would result in hundreds, if not thousands, or potential combinations. *Id.* at 14–15. Patent Owner also argues that Petitioner fails to perform an adequate *Graham* analysis. Prelim. Resp. 16–18. Patent Owner criticizes Petitioner for (1) asserting that its primary references (Jiang and Li) meet all limitations while also (2) making obviousness arguments that rely on Jiang and Li in combination with other references without explaining which limitations are missing from the primary references and which elements the other references are alleged to meet or providing any other explanation as to why an additional reference would be needed. *Id.* at 17–18. Patent Owner contends that the “Petitioner requires the Board or Patent Owner to divine the missing limitation and how Petitioner contends it is met by the combination Petitioner proposes.” *Id.* at 18. Third, Patent Owner also requests the Board to exercise its discretion to deny the Petition in its

entirety because the prior art does not disclose use of APR tools to perform the method claims challenged in Grounds 3 and 5. *Id.* at 18–25.

We disagree with Patent Owner’s first argument that the Petition is un-defined or unbounded. Rather, we understand Petitioner’s Ground 3 to more accurately present two separate and defined Grounds, which we have identified as Grounds 3a and 3b. We also disagree with Patent Owner’s second argument. A petitioner may rely upon additional references for teaching a claim element without making an admission that the primary reference fails to teach that claim element. The reason Petitioner relies upon other references in addition to the primary references was understandable to the Board. We also disagree with Petitioner’s third argument for the reasons set forth in Sections II.F and II.H. Accordingly, we decline to exercise our discretion to deny the Petition.

III. CONCLUSION

For the reasons set forth above, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing with respect to at least one challenged claim of the ’218 patent. Thus, we institute an *inter partes* review on all challenged claims and on all grounds presented.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that an *inter partes* review is instituted on each of the grounds asserted in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which shall commence on the entry date of this decision.

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Patent 8,006,218 B2

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