

UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC.,
Petitioner,

v.

REALTEK SEMICONDUCTOR CORPORATION,
Patent Owner.

Case IPR2023-00920
U.S. Patent No. 8,006,218

DECLARATION OF DR. SHUKRI SOURI

I, Dr. Shukri Sourì, declare as follows:

1. My employer, Exponent, Inc. (“Exponent”), has been retained for my services as an independent expert by Realtek Semiconductor Corporation (“Patent Owner” or “Realtek”) to offer opinions related to U.S. Patent No. 8,006,218 (the “’218 patent”) including opinions in response to the IPR petition involving the ’218 patent filed by Advanced Micro Devices, Inc. (“AMD” or “Petitioner”) and AMD’s expert, Dr. Subramanian’s papers in this proceeding.

2. I am over eighteen years of age, and I am competent to testify regarding the matters set forth in this declaration if called upon to do so.

3. I submit this declaration at the request of K&L Gates, counsel for Patent Owner Realtek in this proceeding.

4. In the preparation of this declaration, I have studied the ’218 patent (EX1001), its file history (EX1002), the Declaration of Dr. Subramanian (EX1003), and all documents cited in Dr. Subramanian’s Declaration. I also have considered the other documents or references cited in this declaration.

5. In forming the opinions expressed below, I have considered the documents listed above, the relevant legal standards as provided to me by counsel, and my own knowledge and experience.

6. I expect to continue my review, evaluation, and analysis of the information generated during discovery between the parties. I understand Dr.

Subramanian has already provided his opinions in EX1003; however, if he is permitted to offer additional opinions, I reserve my right to respond to those should I be asked.

I. Background and Qualifications

7. A summary of my experience, qualifications, and current employment are included in my CV attached as EX2003. The following is a brief summary of my relevant qualifications and professional experience.

8. I am a salaried employee of Exponent. In 2024, Exponent charges \$925 per hour for my time plus expenses for work performed in connection with this matter. I have received no additional compensation for work in this case, and my compensation does not depend upon the contents of this declaration, any testimony I may provide, or the ultimate outcome.

9. Exponent is an engineering and science consulting firm headquartered at 149 Commonwealth Drive, Menlo Park, California 94025. I am a Principal and a Corporate Vice President at Exponent. I am based in, and Director of, Exponent's New York office. I am also the Director of Exponent's Electrical Engineering and Computer Science practice.

10. I am an expert in the field of electrical engineering and integrated circuit design, including power arrangement methods and power routing structures

for circuits with multiple power domains.

11. I received my B.A. (Honors) in Engineering Science in 1992 and my MA in 2007 from Oxford University; my Master's degree in Electrical Engineering from Stanford University, California in 1994; and my Ph.D. in Electrical Engineering, also from Stanford University, California in 2003.

12. Before returning to Stanford for my Ph.D., I was a member of the staff at Raychem's Corporate Research and Development Laboratories, where I researched and built electronic systems to target reliable and safe operation of commercial and industrial equipment. My work resulted in patents awarded by the United States, European, Japanese, and World Intellectual Property Organization patent offices.

13. My Ph.D. work at Stanford was generally in the area of 3-dimensional design and fabrication of Integrated Circuits ("ICs"). I have taught several classes on IC fabrication. My contributions, as part of my Ph.D., included 3-dimensional integration of ICs. A major focus of my Ph.D. research was on the placement and routing of circuit blocks and power interconnects. This was significant in the context of moving from a 2-D to a 3-D paradigm for at least 3 reasons: 3-D offers the opportunity to have vertical interconnects; it allows for an additional degree of freedom of circuit block placement; and it also permits the integration of heterogeneous technologies that would utilize different power and voltage schemes.

14. Since joining Exponent, my professional activities have included working with industry members to understand failure modes of their products, whether such failures occur in the field after deployment, during manufacturing and quality assurance, or even earlier in the design and modeling phase. I have led complex investigations involving IC fabrication process, and I have broad experience with integrated circuit design and microprocessor architectures. For example, I have conducted several root cause analyses for ICs that failed as a result of inadequate placement of insulation barriers and protection devices in chips with multi-voltage operation schemes. Such ICs are common in power applications, such as in the operation of automotive electronics or telecom equipment.

15. I also work with government institutions to advise on technological investigations and challenges. For example, I was selected to the United States National Academy of Engineering Frontiers of Engineering Symposium to help address future technological challenges facing society; and I also advised members of the United States Congress in their Investigation into Instances of Sudden Unintended Acceleration in Toyota Made Vehicles, as instituted by the Committee on Energy and Commerce in the House of Representatives.

16. My experience with IC power structures spans over 25 years, dating back at least to my work at Raychem R&D where I researched novel techniques to control power semiconductor ICs. This involved device designs that required small

voltages to control power silicon switches capable of use in high voltage applications such as automobiles. My experience with power design in ICs continued during my doctoral research, which as I discussed earlier involved placement and routing considerations at least for integration of heterogeneous devices and technologies. I have continued to work within the industry to provide mentorship and guidance towards more reliable and robust IC designs for applications requiring multiple voltages, such as for non-volatile memories, mixed-signal ICs, and other power applications. This has involved assisting on matters pertaining to the structure and layout of ICs composed of various interconnected sub-circuits.

17. I am currently a Senior Member of the Institute of Electrical and Electronics Engineers. Additional details about my background and expertise, including publications, are further described in my professional resume, which is attached as EX2003 to this declaration. This resume includes a list of all publications I have authored within the preceding ten years. It also includes a list of cases in which I have testified as an expert at trial or by deposition within the preceding four years.

II. Understanding of the Law

18. Although I am not a lawyer, I have been advised on the relevant legal principles by Realtek's counsel and have used them as a basis for my opinions. These

are consistent with my understanding of the legal principles based on my prior experience with patent litigation matters.

19. My understanding of the legal requirements for these issues is based on communications with counsel and my prior experience with patent litigation matters. Below, I have summarized my understanding of applicable legal principles.

20. I applied the legal principles below, as necessary, in reaching my opinions. Each opinion is consistent with the claim language and the plain and ordinary meaning as understood by one of ordinary skill in the art at the time of the invention. I discuss claim construction issues further below.

21. I understand that, unlike at the district court, patents subject to *inter partes* review, such as this proceeding, are not presumed to be valid, such that a lower burden of proof is used to judge the patentability of challenged claims. Unlike the district court's "clear and convincing" burden, here a "preponderance of the evidence" burden exists.

A. Patent Claims

22. I understand that the claims within a patent set forth what the inventors have presented as their inventions.

23. I understand that patent claims, not a patent's disclosure, are what define the scope of the patented inventions.

24. I understand that a patent may include two types of claims: independent

and dependent claims. I also understand that claims can be independent or in dependent form, meaning that they depend from the identified independent claims and add requirements to those claims. An independent claim stands alone, while a dependent claim includes its own limitations, as well as the limitations of all of the claims from which it depends.

B. Level of Ordinary Skill in the Art

25. It is my understanding that when interpreting the claims of a patent, I must do so based on the perspective of one of ordinary skill in the art at the time of invention. I understand that when assessing the level of ordinary skill for a given patent, relevant factors include (1) the educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) educational level of active workers in the field.

C. Validity

26. I understand that a patent claim is invalid as “anticipated” by a single “prior art” reference if the reference discloses every single element of the claim with sufficient precision and detail to establish that the subject matter of the claim existed in the prior art. In particular, I understand that it is not sufficient to establish that all of the elements are collectively disclosed within a particular document. Instead, the operative question is whether a person of ordinary skill would have understood the

elements as being arranged as in the claim itself. I also understand that a prior art reference cannot “anticipate” a patent claim unless that reference enables one of ordinary skill in the art to make and use what is disclosed without undue experimentation. Thus, if the reference does not enable one of ordinary skill to make or use each and every claim limitation, then the claim cannot be “anticipated” by the reference.

27. I understand that an anticipation challenge to a patent claim requires a showing that each limitation of a claim, as properly interpreted, is either expressly disclosed or is inherently contained in the disclosure of a single prior art reference, arranged in the same way as in the claim. For inherency, I understand that anything not expressly disclosed must be necessarily present in the prior art.

28. I understand that Dr. Subramanian is not offering any theories of anticipation.

29. I understand that a patent claim may describe an invention that was new (*i.e.*, not anticipated by any prior art reference), but nevertheless be invalid for “obviousness” if the differences between the patented subject matter and the prior art are such that the subject matter as a whole would have been obvious to a person of ordinary skill in the art at the time the invention was made.

30. I understand that an invention is not rendered obvious simply on the basis of two or more different disclosures that collectively disclose all of the claimed

elements. In other words, an invention is not obvious just because all of the elements that comprise the invention may have been known in the prior art. Instead, a person of ordinary skill in the art must have had a reasonable expectation of success in pursuing the possibility that turns out to succeed and is claimed. In particular, I understand that knowledge of a goal does not itself render achievement of that goal obvious.

31. I also understand that determining whether or not a claimed invention would have been obvious requires assessing facts related to (1) the scope and content of the prior art, (2) the differences between the prior art and the claimed invention, (3) the level of ordinary skill in the art, and (4) any objective evidence (“secondary considerations”) of non-obviousness. I understand that this is known as consideration of the “Graham Factors.”

32. I further understand that an invention is not obvious just by demonstrating that each of its elements was, independently, known in the prior art. To prove that an invention is obvious, I understand that it can be important to point to a reason or reasons, such as a teaching, suggestion, or motivation, that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed invention does. I understand that this is because inventions in most (if not all) instances rely upon building blocks already known, and claimed discoveries almost of necessity will be combinations of what, in some sense, is

already known, therefore it can be important to point to such a reason or reasons. I understand that in identifying such a reason, the analysis need not require precise teachings in the prior art directed to the specific subject matter of the challenged claim.

33. I understand that it will often be necessary to look to interrelated teachings of multiple patents and the background knowledge possessed by a person having ordinary skill in the art in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue. I understand that any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed. I understand that when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. I understand that the combination of familiar elements according to known methods may be obvious when it does no more than yield predictable results.

34. I also understand that a claim is not invalid as obvious if it is more than the predictable use of prior art elements according to their established functions.

35. Further, I understand that while predictability is a touchstone of obviousness, the concept of a “predictable result” under the law refers not only to the expectation that prior art elements are capable of being physically combined, but

also that the combination would have worked for its intended purpose.

36. I also understand that if the prior art teaches away from combining known elements in the manner claimed by the invention at issue, discovering a successful way to combine them is less likely to be obvious. In particular, I understand that a reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant, or would understand based on the reference that the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the applicant. Likewise, I understand that similar subject matter may not be sufficient motivation for a person of skill in the art to combine references if the references have conflicting elements.

37. Further, I understand that even if a reference does not necessarily "teach away," its statements regarding preferences are relevant to a finding regarding whether a person of ordinary skill would have had reason to combine that reference with another reference.

38. I also understand that one must be cautious and resist the temptation to rely on hindsight reasoning when attempting to combine references to suggest that a claim may be obvious. It is important to analyze validity based on the perspective of one at the time of the invention, which I understand is at least as early as the effective

filing date.

39. I also understand that the burden of persuasion concerning unpatentability (in other words, the ultimate burden to prove the relevant facts to the specified degree of certainty—here, preponderance of the evidence) remains at all times on the party challenging patentability—here, the Petitioner, AMD. If the fact trier of the issue is left uncertain as to validity issues, Petitioner has thus failed to meet its burden.

III. Level of Ordinary Skill in the Art

40. For the purposes of this declaration, I have applied the level of skill in the art applied by Dr. Subramanian in paragraph 33 of his declaration.

41. My analysis and opinions below are given from the perspective of a POSITA in this technological field in the relevant time frame, unless stated otherwise.

42. I satisfied the definition of a POSITA long before the filing date of the application leading to the '218 patent. I now consider myself an expert in the relevant field of technology for the '218 patent.

43. In forming my opinions for this declaration, I have used the perspective of one of ordinary skill in the art as defined above. My opinions, however, would not be affected if a POSITA is defined as someone who has slightly more or slightly

less experience than described above.

IV. Prosecution History

44. I have reviewed the certified file wrapper or prosecution history for the '218 patent, which is EX1002.

45. I understand that the file history is intrinsic evidence that a POSITA may rely upon to understand the claims.

46. During prosecution of the '218 patent, there were office actions by the USPTO, and there were responses from the applicant. I have relied on those in my analysis.

47. Dr. Subramanian addresses the file history in paragraph 45 of his declaration (EX1003). He discusses an office action in which the claims were rejected over the combination of U.S. Patent No. 7,000,214 ("Iadanza") and U.S. Patent No. 7,234,124 ("Chen") and asserts that the rejections were not disputed. I disagree that the rejection was not disputed. While the applicants did amend the claims, the applicants also distinguished the invention of claims 1 and 12 from the prior art based on the coupling required between the global power mesh and the partial local power meshes. Applicants stated:

In the present application (see paragraph [0020], for example) the global power mesh 400 couples to the external power (such as: by way

of the I/O pin of the chip) to conduct the external power into the chip while the local power mesh 300 couples to the global power mesh 400 and the chip circuitry. In other words, the internal circuits of the chip correspond to the power domains 110, 120. Then the external power will be inputted into the chip circuitry by way of the global power mesh 400 and the local power mesh 300.

EX1002, 138. Applicants explained that “[i]n contrast, Chen has no electrical connections between the second power grid 22 and the first power grid 21.” *Id.*

V. Background of Integrated Circuits

48. 61. An integrated circuit contains electronic circuitry whose components are typically monolithically fabricated on the same piece of silicon, also referred to as a die. Each die typically contains millions, and some contain billions, of individual electronic components that are integrated onto the die. It is common to refer to each die, in totality, as an integrated circuit, or “IC,” and also as a “chip.”

49. Integrated circuits (ICs) are manufactured with high precision lithography processes in which dopants are first implanted into a silicon wafer to form electronic devices. Following this, a series of insulation and metal interconnect layers are successively added to allow interconnection of devices formed in the silicon substrate. This collective assembly of layers is called the “layer stack,” and

different manufacturing processes offer different numbers of metal layers available for routing. An etching process is used to define where interconnect should be routed through insulative material. Semiconductor materials such as silicon provide ideal foundations for the fabrication of electronic circuits because they can be doped with impurities to manipulate their conductive properties. Through selective doping or etching of targeted areas, material interfaces and gradients can be engineered with specific properties, enabling the simultaneous fabrication of billions of electronic components such as transistors, diodes, resistors, and capacitors.

50. After manufacturing is complete, a processor will generally comprise a die or dies within a package. The package, or packaging, typically comprises components that serve to mount, protect, and provide external contact points (such as wire leads, or metal pads, also called bumps) to the die or dies.

51. The integrated circuitry on each die includes mainly large numbers of transistors, along with other components such as inductors, capacitors, and resistors. These components are connected to form circuitry that can perform a wide variety of functions, such as perform digital mathematical operations on binary data or amplification and conditioning of analog signals.

52. The transistors on a silicon die are located at what engineers refer to as the “device” layer(s) or the silicon layer(s). The most common types of transistors are known as MOSFETs (metal oxide semiconductor field effect transistors), and

are formed at the silicon layer by successive patterned layers of metal, silicon dioxide, and silicon, where the silicon has been doped at certain regions of the MOSFET with other materials that change its electronic properties.

53. Above the silicon layer are metal layers. Metal layers consist primarily of wiring, which is used to connect devices together, and they frequently are made of copper. For the layers above the silicon layer, there generally is an insulating material, also called a dielectric, everywhere there is not wiring or vias, referred to as the inter-layer dielectric (ILD). Vias are used to allow an electrical connection, through the insulating material, from wires on one metal layer to those on another layer and ultimately to create electrical connections, or routing, from the top metal layer down to the device layer.

54. The electrical connections can generally be categorized into those that carry electrical power, signal, or ground, though there can be many additional categories. Power routing can be thought of as providing the energy necessary to operate connected transistors and circuitry. Signal routing can be thought of as transferring the electronic data, signals, or information between connected transistors and circuitry. And ground routing generally provides an electrical point of reference to interpret power and signal levels.

55. At the time of invention, power routing approaches required designers to consider the number of concurrently changeable variables that made

implementing power routing designs complex and unpredictable because of unintended complications that arise when power routing is designed or changed. Exemplary complications that may arise in power routing designs include dense wiring interconnects, long wire routes, parasitic capacitance, and chip area spacing penalties. EX1024, 1:44-56; EX2005, 139:19-140:12. Depending on the changes that are made, a new iterative process of testing for complications arises to ensure the change did not render the chip inoperable for its intended purpose. Furthermore, due to the space constrained nature of integrated circuits, if any components are added, other components typically must be moved, requiring additional iterative testing for complications that may arise and render the chip inoperable. Accordingly, the field of IC chip design was at the time of the invention of the '218 patent a complex and unpredictable area of technology.

VI. Overview of the '218 Patent

56. The '218 patent is directed to “a power mesh arrangement method, particular to a power mesh arrangement method applied in an integrated circuit having multiple power domains” and a related structure. EX1001, 1:7-11; 2:33-41.

57. As integrated circuit devices have become more complicated, different portions of the circuitry of a chip may need different voltages (powers) at the same time. *Id.*, 1:5-42. For example, the '218 patent recites the following:

As the circuitry of the integrated circuit becomes more and more complicate[d], there are possibilities that different portions of the circuitry of a chip need different voltages (powers) at the same time. For example, the chip circuitry may have two kinds of operating modes: the normal operating mode and the sleeping mode. During the normal operating mode, the entire chip circuitry uses the operating voltage for its normal operation. But during sleeping mode, only part of the chip needs to be maintained in the normal operating mode. Therefore, the normal operating voltage is still used by these circuits for its operation while the other circuits of the chip only need a lower voltage for maintaining the sleeping operation. Therefore, different powers need to be supplied to the different circuits inside the chip so that the circuits can perform different operations during the sleeping mode. Hence, it is common practices to arrange multiple power domains in the chip circuitry. In other words, circuits in different power domains are coupled to different powers respectively so that the circuits of different power domains use different powers to support the different operations that are just mentioned.

Id., 1:13-33.

58. At the time of the invention of the '218 patent, the traditional circuit design approach did not provide for a simple rule or step for the circuit designer to plan and design the power routing structure of a circuit having multiple power domains. *Id.*, 1:34-37.

59. For example, the automatic placement and routing (APR) tools available at the time could only support circuits having a single power domain. *Id.*, 1:34-43. The patent recites:

For example, the well-known automatic placement and routing (APR) tool can only support circuits having single power domain. Therefore, a circuit designer can only rely on the most primitive method to design the power routing of multiple power domains, such as the manual

routing. Obviously, such a design approach is not only complicated but also inefficient.

Id., 1:33-42.

60. Because APR tools were limited in their capabilities for automating the route and placement of multiple power domain chips, at the time of the invention, important portions of the power routing structure typically had to be input manually for chips that required multiple voltages. This could include, for example, inputting coordinates for each power wire, connecting some components while avoiding others, and providing properties, such as thickness, width, distance, and shape. Manually designing the power routing structure of a device without the benefits provided by the methods, structures, and arrangements of the '218 patent involved a significantly greater amount of time.

61. At the time of invention, the '218 patent also explains that a POSITA would not have known of a structure to use to easily complete the design of the integrated circuit. *Id.*, 2:33-41.

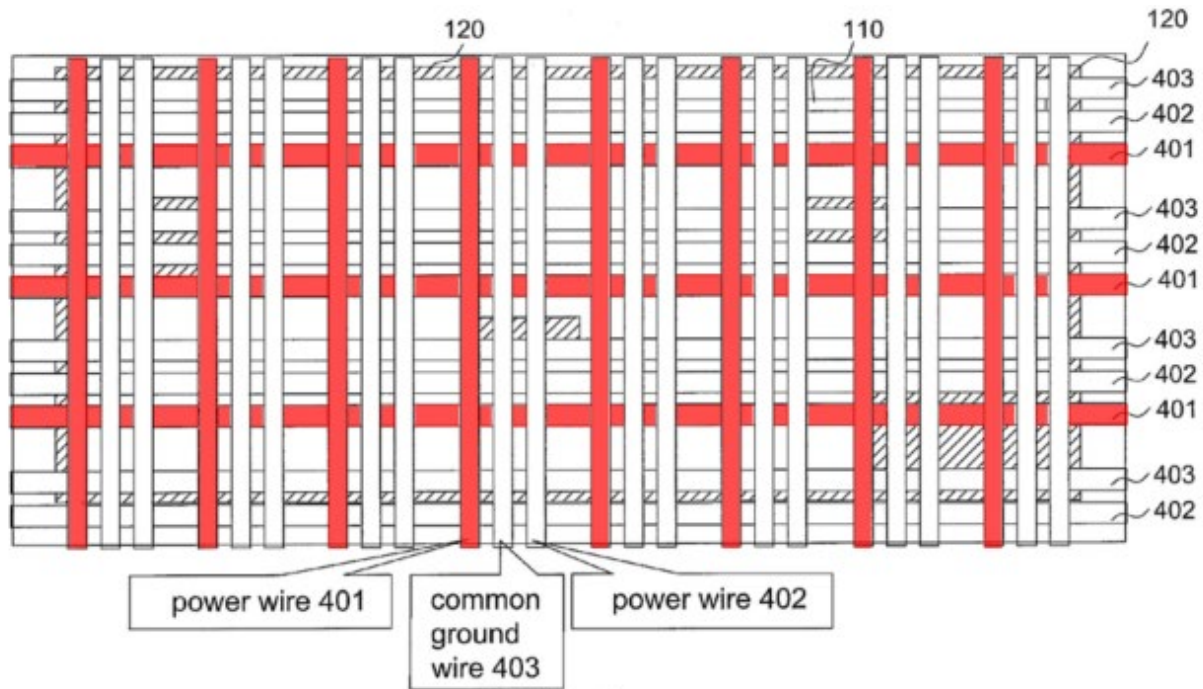
62. The '218 patent discloses an invention to overcome the problems with the prior art that “provides a power mesh arrangement method and related structure thereof for a user to easily complete the design of the power mesh of an integrated circuit having multiple power domains by following the arrangement method and its related structure.” *Id.*, 2:33-37. The method involves a power mesh arrangement that

can be implemented using an APR tool “easily so that the user can use the APR tool to automatically complete the circuit layout so as to increase the circuit design efficiency.” *Id.*, 2:37-41.

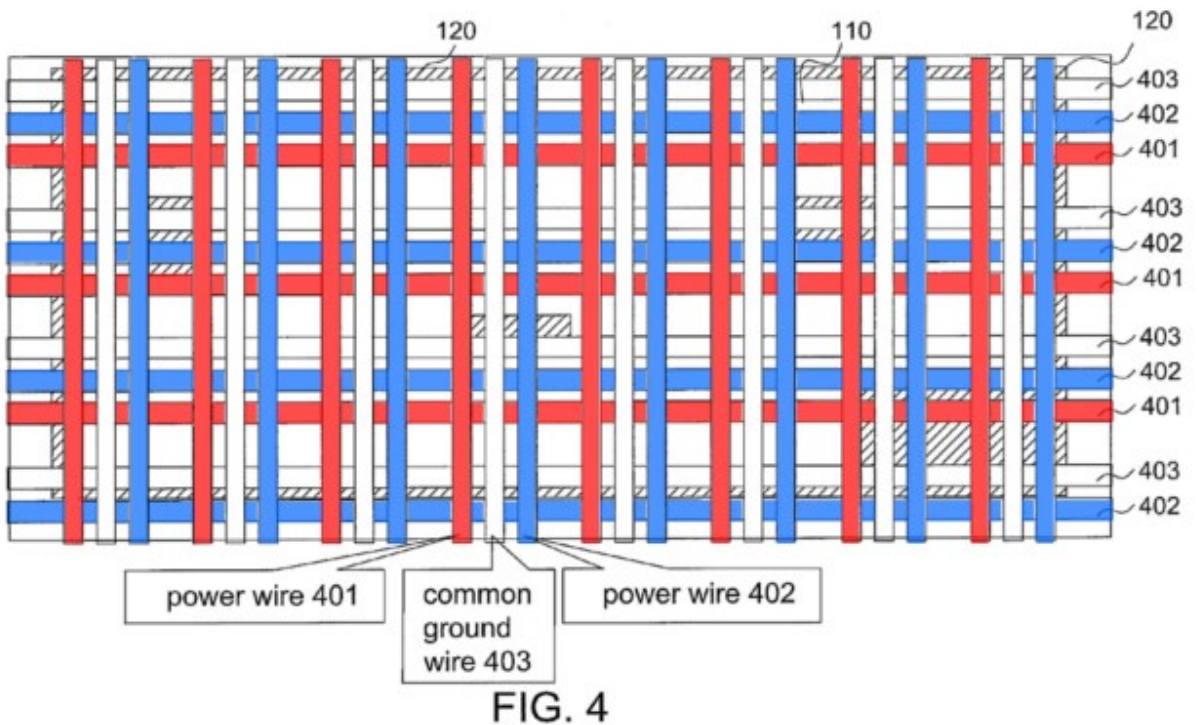
63. The '218 patent also discloses a related structure that takes into account a number of design considerations, including the efficiency of the design and creating a power routing structure that does not use undue space on the chip or adversely affect performance. *Id.*, 1:45-50; 2:33-41; 5:25-53; 6:43-40.

64. For example, the '218 patent discloses use of a global power mesh that utilizes more power supply wires in the more spacious higher metal layers so that the lower metal layers “can be released” for other uses. *Id.*, 5:25-53. The “global power mesh” is used “to provide the power needed by the first power domain and the second power domain separately.” *Id.*, 7:63-66. The global power mesh uses discrete wiring paths for each power needed for the first and second power domains and the ground. *Id.*, 4:31-38, Fig. 4.

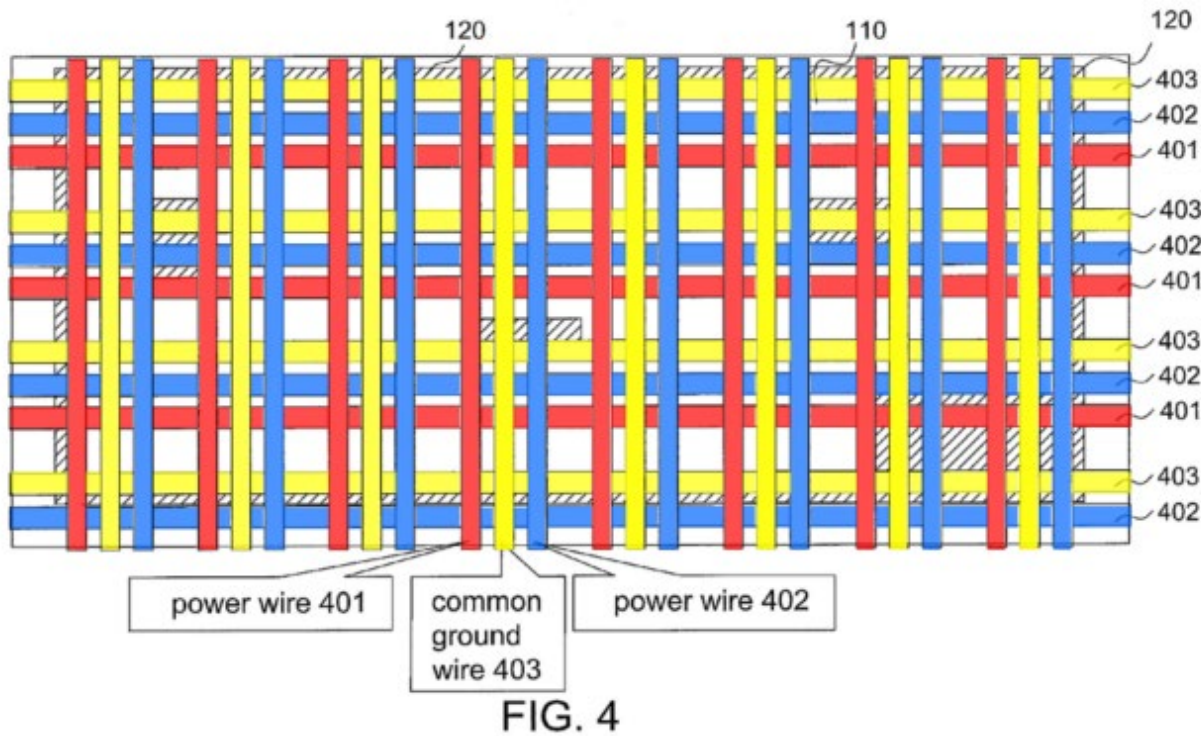
65. As I have illustrated below, the global power mesh includes power wires 401 (red) for distributing the working voltage V_{DD1} to the first power domain. *Id.*, 4:31-38.



66. The global power mesh also includes power wires 402 (blue) for distributing the working voltage V_{DD2} to the second power domain. *Id.*, 4:31-38.



67. Further, the global power mesh includes ground wires 403 (yellow) for supplying the ground potential V_{GND} to the power domains as shown below.

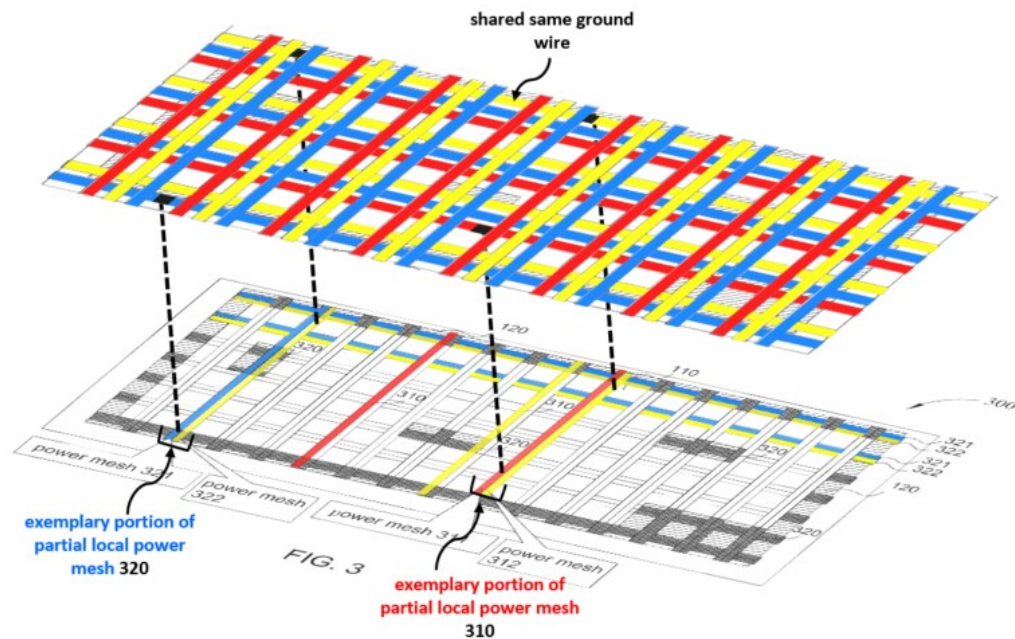


68. The wires of the global power mesh couple through a partial local power mesh to reach the power domains below. The first partial local power mesh 310 comprises a power wire 311 (red) and ground wire 312 (yellow). The second partial local power mesh comprises power wire 321 (blue) and ground wire 322 (yellow).



FIG. 3

69. The global power mesh may include “***one*** common ground wire” that is used to supply the ground potential to both of the partial local power meshes. *Id.*, 4:31-38, Fig. 4. The exemplary routing structure is illustrated below with ground shown in yellow, V_{DD1} shown in red, V_{DD2} shown in blue, and vias, connecting the wires of different metal layers depicted as black dashed lines.



70. Based on this routing structure, the patent explains that when the partial local power meshes 310 and 320 are connected to the internal circuits in each of the power domains, it is assured that the external powers V_{DD1} and V_{DD2} are definitely inputted into the chip circuitry. *Id.*, 5:21-29.

VII. Claim Constructions

A. “Power Domain”

71. The plain and ordinary meaning of “power domain” is a portion of the integrated circuit that has a different power requirement from the power requirements of another portion of the integrated circuit. I have reviewed Dr. Subramanian’s deposition transcript and it appears that he does not disagree. EX2005, 13:17-17:7.

72. It is my opinion that a POSITA would understand that a “power domain” is a portion of the integrated circuit that has a different power requirement from the power requirements of another portion of the integrated circuit. This understanding is supported by intrinsic and extrinsic evidence. EX1001, Abstract, 1:12-43; 2:24-4:52; 5:8-6:50; claims 1-20; Figs. 1-6. The embodiments of the patent describe a first portion of the integrated circuit (*e.g.*, power domain 110) that receives a power (*e.g.*, V_{DD1}) that is different from the power received from the second portion of the integrated circuit (*e.g.*, power domain 120 receiving, *e.g.*, V_{DD2}). *Id.*, Figs 1-6, 3:33-6:29, claims 1-20. In all examples, a POSITA would understand that the power domains are receiving a different power (*e.g.*, from a different power pad) through the patent’s references to V_{DD1} and V_{DD2} , indicating that a first portion of the integrated circuit (first power domain) has a different power requirement than the second portion of the integrated circuit (second power domain).

B. “First Power Domain”/ “Second Power Domain”

73. Claim 12[a] and 12[b] recite that the first and second partial local power meshes must correspond to the location of the first and second power domains. It is my opinion that a POSITA would understand that the “first power domain” must be *different* from the “second power domain.” I have reviewed Dr. Subramanian’s deposition transcript and it appears that he does not disagree. EX2005, 20:17-27:18.

74. The intrinsic evidence supports my opinion. For example, the claims

expressly identify a difference between the first and second power domain by using the terms “first” and “second” to differentiate between two different power domains. If all portions of the chip have the same power requirements, then the chip has a single power domain. A single power domain cannot satisfy the “first” and “second” power domain requirement without rendering those terms meaningless.

75. In addition, the '218 patent explains that the invention is directed to “a power mesh arrangement method utilized in an integrated circuit having *multiple power domains*.” EX1001, Abstract (emphasis added); *id.*, 1:13-33 (describing some portion of the circuitry that could operate at the “normal operating voltage” and also enter “sleeping mode” while other portions remain at “normal operating voltage”). The entire disclosure of the patent, including the examples and figures, involve providing two powers, V_{DD1} and V_{DD2} , to two different portions of chip circuitry. EX1001, 1:12-43, 3:6-64, 4:31-45, 6:16-24, Abstract, 1:57-59, 2:1-3, 2:8-13, 2:20-28, 4:25-38, 5:10-29, claims 1-20, Figs. 1-6. In practice, part of the range of voltages associated with each power may happen to have the same numerical value at some point in time, but the point of the invention is that, since they are distinct powers carried by separate paths from separate sources (*e.g.*, V_{DD1} and V_{DD2}), they do not have to.

C. “Having its position corresponding to”

76. It is my understanding that the terms “a first partial local power mesh

having its position corresponding to the position of a first power domain” and “a second partial local power mesh having its position corresponding to the position of a second power domain” were previously construed to “require only that the partial mesh overlap to some degree with its respective domain when viewed from above.”

77. It is my opinion that a POSITA would understand that “having its position corresponding to” requires that the partial local power mesh overlap to some degree with its respective domain so that the partial local power mesh can couple to the power domain positioned below by way of the via holes.

78. For example, Figure 3, discussed above, shows the partial local power mesh 310 overlaps with power domain 110 and is on top of power domain 110. Figure 3 shows that a via could be dropped from the power wires that comprise partial local power mesh 310 down to the power domain 110 to provide power. The specification further confirms that Figure 3 shows two different partial local power meshes, 310 and 320, partitioned “at the positions corresponding to the positions of the power domains 110, and 120.” EX1001, 3:33-43. According to the specification, the partial local power meshes are placed “on top” of their power domains so that they can “couple to the power domains” “positioned below by way of the via holes.” *Id.* A POSITA would therefore recognize that the partial local power meshes have at least partial mesh overlap to some degree with its respective domain when viewed from above.

D. “Power Mesh”

79. I understand that the term “power mesh” has previously been construed as “a network of intersecting wires capable of distributing power.” I have reviewed Dr. Subramanian’s deposition transcript and he agrees with this construction and applied it in his declaration. EX2005, 36:2-37:19. I will apply this construction in my declaration.

E. “Global Power Mesh”

80. I understand that the term “global power mesh” has previously been construed as a “Power mesh capable of distributing power to multiple power domains.” I have reviewed Dr. Subramanian’s deposition transcript and he agrees with this construction and applied it in his declaration. EX2005, 22:16-34:9. I will apply this construction in my declaration.

F. “To provide the power needed by the first power domain and the second domain” (Claims 1 and 12)

81. I understand that “to provide the power needed by the first power domain and the second power domain” was previously construed to mean “to provide the non-zero levels of power needed by the first power domain and second power domain.” EX2007, 99. In my opinion, a POSITA would understand that the phrase “to provide the power needed” requires some power to be provided.

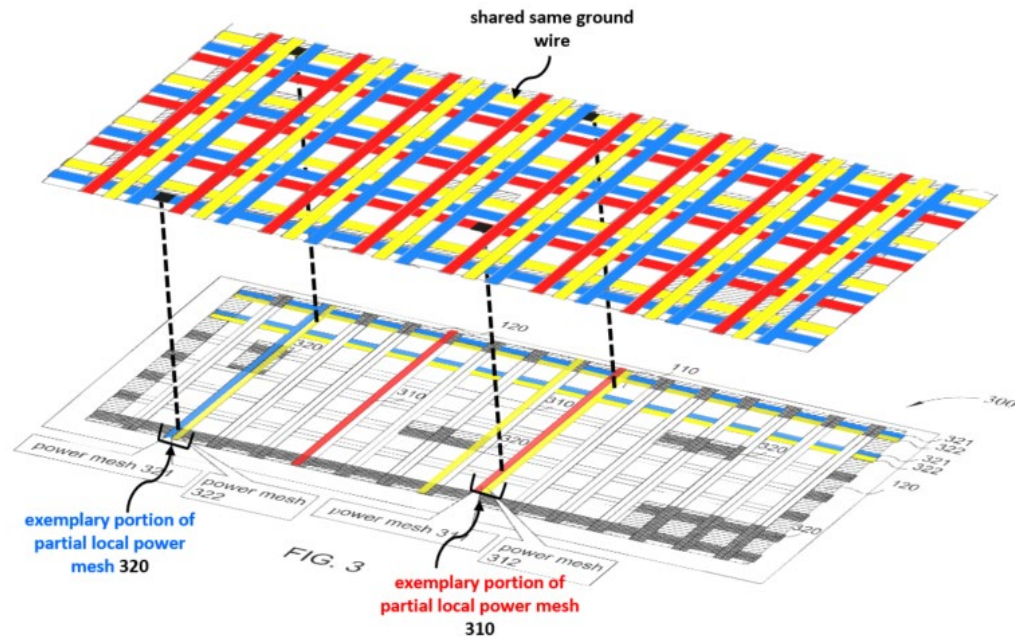
82. Based on the intrinsic record, the claims support this construction. They

recite “to provide,” which requires supplying or making power available. EX2011, 1155 (“to make available; supply”).

pro-vide (prə vīd', prō-) **vt.** --vid'ed, --vid'-ing [ME *providen* < L *providere* < *pro-*, PRO-² + *videre*, to see; see VISION] **1** [Now Rare] to get ready beforehand **2** to make available; supply **3** to supply (someone) *with* something **4** to state as a condition; stipulate —*vi.* **1** to prepare (*for or against* some probable or possible situation, occurrence, etc.) **2** to make a condition; stipulate **3** to furnish the means of support: usually with *for* —**pro-vid'er** *n.*

If no power is provided, then the term “to provide” is rendered meaningless because the opposite of what the claim recites would be within the scope. The claim does ***not*** recite “to provide the power ***if*** needed” or to “not provide power.” Had the applicants intended this meaning, they would have written the claim differently.

83. The specification further supports that the invention relates to providing ***non-zero*** levels of power. The global power mesh of the '218 patent has a wiring structure that includes two power wires to supply the working voltages V_{DD1} and V_{DD2} needed by the local power meshes and the power domains as illustrated below.



84. The patent does not describe a mechanism for the power routing structure to turn the power off or not provide power. For example, power gating is not discussed in the '218 patent.

85. Similarly, the patent describes embodiments which are in operational modes, meaning that circuitry would require power to perform its functions. For example, the patent describes a “sleep” mode of operation, in which a “lower voltage” is provided for “maintaining the sleeping mode operation.” EX1001, 1:18-34. Similarly, other portions of the specification discuss providing two powers, V_{DD1} and V_{DD2} . EX1001, 1:12-43; 3:6-64; 4:31-45; 6:16-24; Abstract; 1:57-59; 2:1-3; 2:8-13; 2:20-28; 4:25-38; 5:10-29; claims 1-20. Thus, it is my opinion that a POSITA

would understand that in all embodiments, including even during “sleep” mode, some amount of power is actually provided to the circuitry.

86. I understand that Dr. Subramanian’s position is that the “power needed” can be zero. But that argument fails to account for the “to provide” language of the patent claim. If “power needed” is zero, then there is nothing “to provide” and the claim is not met. Further, under this view, the limitation is met even if the circuitry is idle and no power is needed. Dr. Subramanian’s position renders the term meaningless.

G. “Separately” (Claim 12, 15)

87. Claim 12 recites “a global power mesh . . . to provide the power needed by the first power domain and the second domain separately.” I understand that the term “separately” was previously construed to mean “through separate electrical paths.” It is my opinion that a POSITA would understand, in the context of the ’218 patent, “separately” requires a physically distinct path for the voltages to be provided to the first power domain and second domain through the global power mesh.

88. In my opinion, a POSITA would understand that the claims require the ***global power mesh*** to have separate electrical paths. For example, claim 12 states:

“global power mesh, coupling to the first local power mesh and the second local power mesh, ***to provide the power*** needed by the first power domain and the second domain ***separately***.”

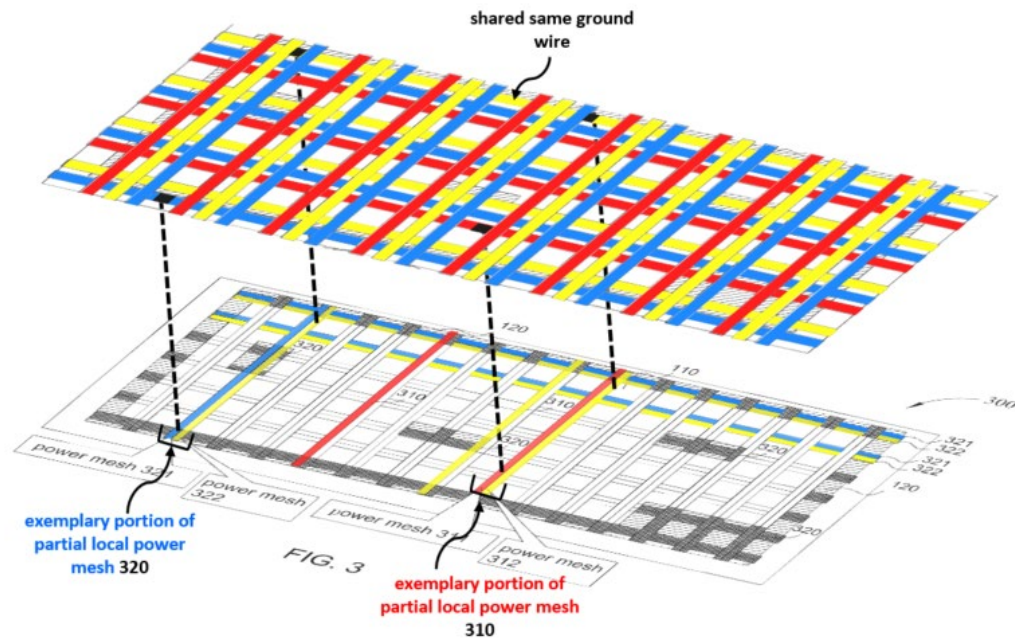
EX1001, cl. 12[c] (emphasis added); *See also id.*, cl. 15. Because of the placement

of the comma, offsetting the “coupling” limitation, a POSITA would understand that it is a separate phrase from the rest of the limitation. The commas make the phrase unambiguous that “separately” modifies “provide,” and cannot be read to modify “coupling.” EX2015, 314 (“A relative clause is said to be nonrestrictive if it could be omitted without obscuring the identity of the noun to which it refers or otherwise changing the meaning of the rest of the sentence.”). Accordingly, it is my opinion that a POSITA would understand that the global power mesh is providing the power separately to the first and second local power meshes. Because the coupling is in the nonrestrictive portion of the clause, it does not change that the “global power mesh” is what the rest of the limitation is referring to.

89. The remainder of the specification is consistent with the global power mesh providing power on separate electrical paths. In the embodiments of the '218 patent, working voltages are routed to the power domains to ensure that the exemplary powers V_{DD1} and V_{DD2} are “definitely inputted into the chip circuitry.” EX1001, 5:25-29; *see also id.*, 3:56-64; 4:31-38; 6:16-24.

90. For example, in an embodiment of Figure 4 there are “***two power wires 401, 402***” that are “used to supply the working voltages V_{DD1} , V_{DD2} needed by the local power meshes 310, 320, respectively.” EX1001, 4:31-36 (emphasis added); *see also id.*, Fig. 4. Similarly, in an embodiment of Figure 6 “***power supply wire 401***” “couples to the external power V_{DD1} ” and “uses via (not shown in the figure) to

couple to the power wire 311 located below so as to conduct the external power V_{DD1} to the chip circuitry.” *Id.*, 5:10-14 (emphasis added). “The **power supply wire 403**” “couples to the external power V_{DD2} ” and “uses via to couple to the power wire 321 located below so as to conduct the external power V_{DD2} to the chip circuitry.” *Id.*, 5:14-17 (emphasis added). Thus, it is my opinion that a POSITA would understand that the global power mesh “provide[s]” power “separately” through its discrete wiring structures. As illustrated below, the ’218 patent describes the use of separate power wires in the global power mesh to deliver the power needed by the first and second power domains separately.



91. In my opinion, Dr. Subramanian’s interpretation, that a separate via

connection from the global power mesh to the first partial local power mesh constitutes providing the power separately, cannot be correct. It ignores the grammar of limitation 12[c]. EX2015, 314. In addition, this interpretation rewrites the claims to state “separately coupling.” Had the patentee intended this meaning, it would have said so.

92. Dr. Subramanian’s interpretation also ignores the specification which explains the power needed by the first and second power domain is provided “separately” by the wires in the global power mesh, discussed above. There is no other mechanism provided for providing the power separately in the patent.

H. “Same ground wire” (Claims 9, 18, 20)

93. Claims 9 and 18 recite “wherein the first local ground wire and the second local ground wire *share the same wire* of the global power mesh.”¹ (Emphasis added.) Claim 20 recites “wherein the first power domain and the second power domain *share the same ground wire* of the global power mesh.” EX1001, cl. 20 (emphasis added).

94. In my opinion, a POSITA would understand the term “same ground wire” to mean a “single ground wire.”

¹ The first local ground wire in a ground wire in the first partial local power mesh and the second local ground wire is a ground wire in the second partial local power mesh. EX1001, claims 7-8, 16-17, 20.

95. I understand that there is a dispute over whether the “same ground wire” must be a single wire. I understand that Dr. Subramanian contends that “all of the ground wires” can be a “same ground wire.” In my opinion, Dr. Subramanian’s construction is incorrect. A POSITA would understand from the intrinsic evidence that the proper construction requires a single ground wire, rather than a collection of wires.

96. First, the claim language indicates to a POSITA that the “same ground wire” is a single wire. If there is not a single wire, then the wire is not the “same”; it would be a different wire. My understanding is based on the plain and ordinary meaning of the word “same.” Dictionaries also confirm that same means as “being the very one; identical.” EX2011, 1267.

same (sām) *adj.* [ME < ON *samr*, akin to Goth *sama*, OHG *samo*, OE *same* < IE **som-*, var. of base **sem-*, one, together, with > Sans *saṃ*, Gr *homōs*, alike, L *simul*, at the same time, *similis*, like] **1** being the very one; identical **2** alike in kind, quality, amount, or degree; corresponding: often prefixed to nouns or past participles to form adjectives **3** unchanged; not different [to look the *same* as ever] **4** before-mentioned; just spoken of Usually used with *the* — *pron.* the same person or thing: usually with *the*, *this*, or *that* — *adv.* in the same way; in like manner: usually with *the*

SYN.—*same*, in one sense, agrees with *selfsame* and *very* in implying that what is referred to is one thing and not two or more distinct things [that is the *same*, or *selfsame* or *very*, house we once lived in/ and, in another, implies reference to things that are really distinct but without any significant difference in kind, appearance, amount, etc. [I eat the *same* food every day]; *identical*, in one sense, also expresses the first idea [this is the *identical* bed where he slept/ and, in another, implies exact correspondence in all details, as of quality, appearance, etc. [the signatures are *identical*]; *equal* implies the absence of any difference in quantity, size, value, degree, etc. [equal weights, an *equal* advantage]; *equivalent* implies of things that they amount to the same thing in value, force, meaning, etc. [\$5 or its *equivalent* in merchandise] —**ANT.** *different*

Id.

97. Second, a POSITA would understand from the specification that the “same ground wire” is a single wire. As part of the routing structure, the specification explains that there can be “*one* common ground wire 403” of the global power mesh. *Id.*, 4:31-34 (emphasis added); *see also id.*, 5:17-20, 5:39-44, 6:37-40, Fig. 4. Thus, the specification contemplates that the global power mesh may contain one single ground wire that provides the ground potential to the power domains.

98. Claims 9, 18, and 20 also use the term “share.” Dr. Subramanian testified that the term “share” requires a 2:1 relationship. EX2005, 232:9-233:8. My interpretation of “share” is consistent with Dr. Subramanian’s understanding and the term “share” indicates to a POSITA that the first local ground wire and the second local ground wire connect, for example by via, to a single wire in order to “share” that same ground wire of the global power mesh. This further confirms that the “same ground wire” of the global power mesh must be a single wire so that it can be shared by the first local and second local ground wires (in a 2:1 relationship).

99. I understand Dr. Subramanian’s construction of “same ground wire” to be that all the ground wires or, effectively, a mesh of ground wires is a “same ground wire.” I disagree. The intrinsic record indicates to a POSITA that a mesh is different from a “wire.” For example, the claims use the terms “wire” and “mesh” separately and makes clear they are different by claiming that “meshes” comprise “wires.” *See, e.g.*, EX1001, cl. 15 (“The power routing structure according to claim 12, wherein

the global power mesh comprises: at least one ground wire; at least one first power wire that provides the power needed by the first power domain; and at least one second power wire that provides the power needed by the second power domain.”).

A POSITA would understand that different terms have different meanings.

100. Claim 15 further confirms my opinion. Claim 15 recites “at least one ground wire.” *See, e.g.*, EX1001, cl. 15. A POSITA would understand that “same ground wire” must be different, and narrower, from “at least one ground wire” in claim 15, so the “same ground wire” cannot be multiple wires.

101. A POSITA would also understand that Dr. Subramanian’s construction would include “vias” in the meaning of the term “same ground wire” because vias connect the wires between the two layers of the ground mesh. But the intrinsic record is also clear that a “via” connects wires and is not itself a wire. *See, e.g.*, EX1001, 4:16-18 (“Besides, the power wires and ground wires of adjacent metal layers having the same electrical property can be interconnected to each other by via”).

102. It is my opinion that Dr. Subramanian’s construction is so overbroad that it renders meaningless the requirement that the “first local ground wire” and “second local ground wire” share the ground wire of the global power mesh because it would allow ground wires of the global power mesh (not the partial local power meshes) to share “the same ground wire of the global mesh.”

I. “Global power mesh, coupling to the first local power mesh and the second local power mesh,” (claim 12[c])

103. Claim 12 recites a “global power mesh, coupling to the first local power mesh and the second local power mesh,” “a first partial local power mesh . . . coupling to the first power domain,” and “a second partial local power mesh . . . coupling to the second power domain.” In my opinion, a POSITA would understand that these claim limitations, together, require a connection from the global power mesh to the first and second partial local power meshes, and a subsequent connection to the first and second power domains. A POSITA would understand that the claim recites a specific power wiring structure in which a global power mesh provides power and ground through two partial local power meshes down to the first and second power domains.

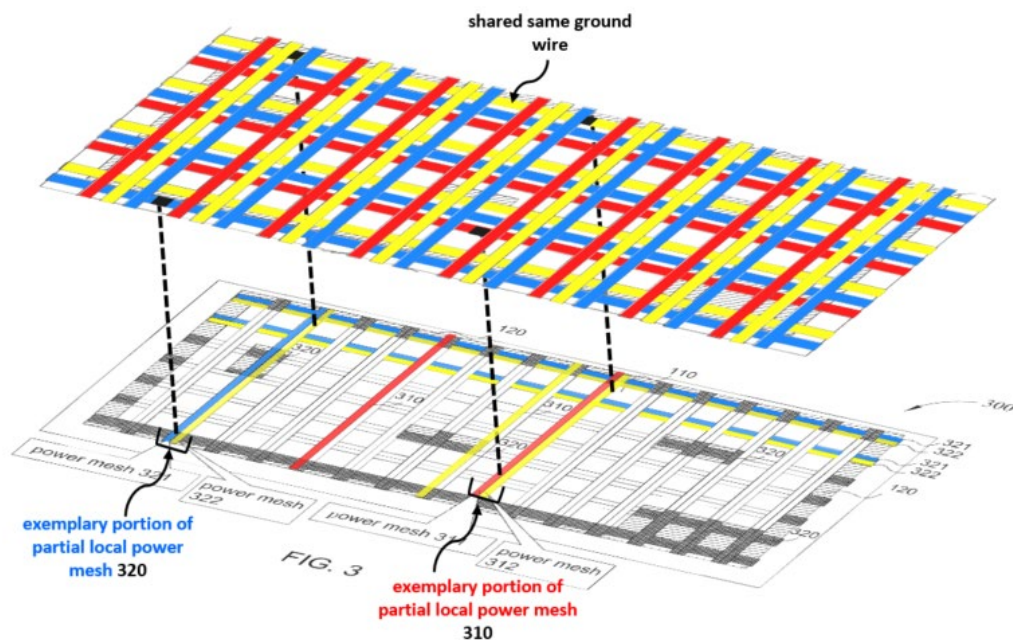
104. In contrast to claim 12, a POSITA would understand that claim 19 recites a different structure in which the global power mesh couples to the power domains without any intermediary partial local power meshes. EX1001, cl. 19 (“coupling the first power wire [of a global power mesh] . . . to the first power domain.”).

105. Based on the differences between the coupling claimed in claims 12 and 19, in my opinion, a POSITA would understand that the term “global power mesh, coupling to the first local power mesh” is different from coupling a power

wire of the global power mesh to the first power domain.

106. The intrinsic record further confirms my understanding. For example, the specification explains that the global power mesh includes two power wires, 401 and 402, and a ground wire, to supply the working voltages V_{DD1} and V_{DD2} and ground to the partial local power meshes, 310 and 320. EX1001, 4:31-45. The partial local power meshes 310 and 320 have power wires 311 and 321 and ground wires 312 and 322 to supply the ground potential needed by the power domains. *Id.*, 3:56-64. This is the structure claimed by claim 12.

107. The Figures of the patent further illustrate the intervening partial local power mesh of claim 12:



108. In another embodiment, the specification explains that the local power

mesh can be omitted in the invention and “[o]nly the global power mesh 400 is used to conduct the external power into the chip.” *Id.*, 6:9-14. In this embodiment “[i]f the density of the global power mesh is high enough as mentioned previously, it can be assured that all the circuits in the chip positioned below can be coupled to the global power mesh 400 by via to receive the ground potential V_{GND} and the working voltage V_{DD1} , V_{DD2} conducted by the global power mesh 400.” *Id.*, 14-22. The embodiment is claimed in claim 19.

109. I understand that Dr. Subramanian’s construction of the limitation in element 12[c] permits the global power mesh to connect to the power domain without an intervening connection to the first or second partial local power mesh based on his analysis of Jiang. I disagree. In my opinion, a POSITA would understand that a connection between the power wires of the global power mesh and the power domain is separately claimed in claim 19 and claim 12 must be different.

J. “Wherein the first partial local power mesh comprises: at least one first local ground wire that couples to the ground wire of the global power mesh” (claims 7, 16)

110. Claims 7 and 16 recite “wherein the first partial local power mesh comprises: at least one first local ground wire that couples to the ground wire of the require global power mesh.” In my opinion, a POSITA would understand this limitation to require ground wiring in which the ground of the global power mesh connects to a ground wire in the first partial local power mesh (and only then

provides ground to the power domain). EX1001, 3:56-60.

111. The specification supports this interpretation. With respect to the embodiment of Figure 6, the '218 patent explains that the connection between the global power mesh and the power domains occurs through the grounds of the partial local power mesh. EX1001, 5:8-10; *see also id.*, 5:21-29 (confirming that the global power mesh provides power to the chip circuitry by connecting to wires in the partial local power meshes).

112. I understand that Dr. Subramanian has admitted that Li does not disclose a ground wire in the global power mesh connecting to an intervening local power grid before reaching the power domain. I understand that he tries to construe the “coupling” element in claim element 16 as permitting “coupl[ing]” through the power domain.

113. In my opinion, a POSITA would recognize that this construction is incorrect because it reads 16 to be the same as claim 19’s limitation reciting “coupling . . . the ground wire of the global mesh to the first power domain.”

114. In my opinion, a POSITA would understand that claim 19 recites a different coupling relationship. Claim 19 recites coupling between the global power mesh and the first power domain without an intervening partial local power mesh.

115. A POSITA would not interpret “coupling . . . the ground wire of the global power mesh to the first power domain” to be the same as “wherein the first

partial local power mesh comprises: at least one first local ground wire that couples to the ground wire of the global power mesh.”

116. Dr. Subramanian has not provided any intrinsic support for an interpretation that coupling to the partial local power can occur through the power domain. A POSITA would understand that such a structure is contrary to the invention, which deliberately routes power and ground from the global power mesh to the partial local power meshes, and then to the power domains. Connecting through the power domain would use excess wiring for no reason.

VIII. THE CHALLENGED CLAIMS OF THE '218 PATENT ARE NOT OBVIOUS

A. Grounds 1 and 2: Jiang Alone and/or in View of Jiang2/Jiang3 in Further View of Li and/or Chiu Fail to Disclose Each and Every Limitation Recited in Claims 12-18

117. Dr. Subramanian provides opinions on grounds 1-2 in paragraphs 71-121 and reached a conclusion that claims 12-18 were obvious. I disagree that Dr. Subramanian has shown this.

118. In my opinion, Jiang alone or in combination does not teach or suggest the claimed invention. In my opinion, there has been no showing that Jiang teaches or suggests that: (1) macros B and C (or any macros) are “power domains” (2) a global power mesh, coupling to the first and second partial local power meshes, to provide the power needed to the first and second power domain separately (3) a two-

layer global power mesh, or (4) the ground wiring claimed in the dependent claims.

119. Jiang is fundamentally different from the claimed invention because it concerns power gating, *i.e.*, shutting power off to macros, not “providing power to the first and second power domains.”

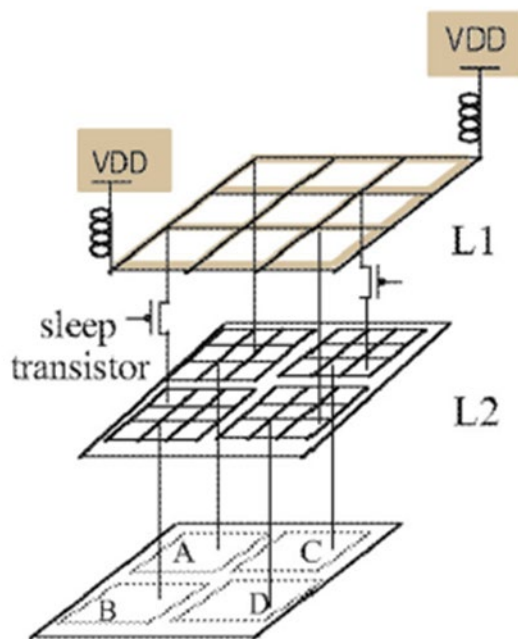
a) Elements 12[a]-[b]: Jiang in view of Jiang2/Jiang3 does not teach or suggest a first and second power domain

120. Dr. Subramanian addresses elements 12[a] and 12[b] in paragraphs 72-77. In my opinion, Dr. Subramanian cannot show these elements are met because he does not identify a first and second power domain in Jiang.

121. Dr. Subramanian maps macros B and C to the first and second power domains. EX1003, ¶74 (“I will use macro B as an example of a first power domain”), ¶77 (“I choose macro C as the second power domain”). Dr. Subramanian does not address the power requirements of macros B or C, as required under the proper construction of the term. *See* Sec. VII.A. A POSITA, however, would understand that macros B and C have the same power requirements and are, therefore in the same power domain.

122. A POSITA would understand that both macros B and C are powered by V_{DD} together. There are no other voltages provided in the Jiang Figure 1(b) embodiment. *See, e.g.*, EX1004, Fig.1(b); *id.*, 2 (“If we want to maintain the same

performance with and without power-gating, in the gated chip the V_{dd} has to be raised by ΔV to counteract the voltage drop across the sleep transistor.”). Thus, the macro’s requirements for power are the same.



123. In addition, a POSITA would understand that macros B and C are power gated together. “Power-gating is a technique for reducing leakage power by shutting off the idle blocks. EX1004, 1. In Jiang, “When a macro is active, the sleep transistor is turned on.” *Id.*, 2. When the block is idle, the sleep transistor is turned off and “the gated macros are disconnected from the power supply.” *Id.*

124. Jiang repeatedly discloses only two power gating schemes: non-power gated and power-gated. EX1004, 2, 7, Table 1. If the power gates (e.g., sleep transistors) were not operating simultaneously, Jiang would discuss a third power

gating scenario in which only one macro was gated. *Id.* That is not disclosed, confirming a POSITA's understanding that macros B and C are gated together. *Id.* Thus, a POSITA would understand that Jiang's macros B and C are idle at the same time and, therefore have no power requirements at the same time. This is further shown by Jiang's analysis in Table 1 that identifies Macros B and C as part of Region I and ungated macros A and D as part of Region II. *Id.*, 2 ("We will now consider the chip shown in Fig.1. Region I contains the gated macros B and C, whereas region II consists of ungated macros A and D.")

Table 1. Power-gating vs. non-power-gating

	non-power-gating chip region		power-gated chip region	
	I	II	I	II
P(leakage)	1	1	↓	↑
P(dyn)	1	1	↑	↑
Area(decap)	1	1	1	↑
Area(st)	N/A	N/A	↑	N/A

Id., Table 1.

125. Dr. Subramanian denies that the macros B and C are gated together and asserts that they are independently power gated. EX1003, ¶81 ("A POSITA would understand that the point of adding sleep transistors to individual power meshes and their underlying domains is to be able to turn off their power supply when the underlying macro is not needed. A POSITA would understand that Jiang's insertion

of sleep transistors between the global power mesh and the first and second partial local power meshes enables the global mesh to power each domain ‘separately’ by selectively turning off each power domain’s sleep transistor when desired.”). I disagree that Dr. Subramanian has shown this.

126. In my opinion, Dr. Subramanian is wrong because Jiang does not disclose independently operable sleep transistors, as discussed above. Jiang discloses to a POSITA that the macros B and C are power gated together.

127. The basis for the assertion appears to be in ¶82 of Dr. Subramanian’s declaration which states: “Jiang does not disclose any linkage between the individual sleep transistors, such that they would all be required to be in the same state at the same time.” But Jiang is a cartoon schematic and does not show all details, including details of the sleep transistors necessary to make assertions about all of their physical connections. For example, Dr. Subramanian agreed that the location of the sleep transistors is not shown correctly and a POSITA would understand that the sleep transistors are in the silicon device layer. EX2005, 174:16-175:12. A POSITA would not expect to see such details in the cartoon schematic of Jiang Figure 1(b) and would not infer independent power-gating, particularly because Jiang only discloses two power supply schemes.

128. Dr. Subramanian also cites to disclosures of other references in an attempt to show that Jiang teaches or suggests independent power gating. EX1003,

¶83. I disagree that these other references can change the disclosure of Jiang. A POSITA would understand the disclosure of Jiang without reference to other references.

129. Further, a POSITA would understand from the other embodiments of Jiang that there is not independent switching of the gates. The model of Figure 3, states, “We have two power supply schemes: (a) power gating and (b) no power gating. We have two regions (I) consisting of gated circuits and (II) of non-gated circuits.” EX1004, 4. If there were independent operability of each of the sleep transistors, then there would be additional power supply schemes in which there were only partial power gating. That is not disclosed.

130. Based on the disclosure of Jiang, a POSITA would understand that Macros B and C are gated on and off together and have the same power requirements. Macros B and C are, therefore, part of the same power domain.

131. Dr. Subramanian also asserts that each of Jiang’s “macros” is a power domain. EX1003, ¶72. I disagree that Dr. Subramanian has shown this. Dr. Subramanian assumes that each macro has different power requirements without providing any evidence to support this understanding.

132. Macros are simply collections of cells. For example, U.S. Pat. No. 7,219,324 explains that “Basic cells are combined into pre-designed circuit units known as ‘macro cells.’” EX2012, 1:45-57. References explain that “A designer,

with a tool such as a compiler, selects desired elements from a library of macro cells and places them in a design.” *Id.* This is consistent with how Jiang uses the term “macros” and these macros can be “commonly used elements such as NAND gates, NOR gates, and flip-flops.” *Id.* A POSITA would understand that a typical power domain would be typically comprised of many individual gates and flip-flops. Jiang states “We implement 26 circuits (from MCNC and JSCAS benchmarks respectively) as the basic logic blocks. The initial floorplan of those blocks is shown as in Fig. 7.” EX1004, 6.

133. Dr. Subramanian improperly equates macros with power domains by using Jiang2 (EX1007) and Jiang3 (EX1008). EX1003, ¶¶72-73 (“a POSITA . . . would readily look to the teachings of Jiang2 and Jiang3 to understand the terminology in Jiang”). In my opinion, this is incorrect. Jiang2 and Jiang3 disclose different systems, that unlike Jiang, do have independently power gated macros, so their “macros” are not the same structures as those in Jiang.

134. Jiang2 (EX1007) discloses a system in which “[e]ach domain is independently controlled by a sleep transistor.” EX1007. As discussed above, each macro in Jiang is not independently controlled by a sleep transistor.

135. Jiang3 (EX1008) relates primarily to power-gating aware floorplanning for designing power-gated chips. EX1008, 1. Jiang3 does not use the term “power domain,” but does refer to a “domain.” It explains that “the chip is divided into

several domains and local power meshes are constructed for each of them.” EX1008, 1. When actually discussing its gated macros, however, it states “gated macros,” not power domains or domains. EX1008, 5. Thus, a POSITA would understand within the context of Jiang3 that each gated macro was distinct from a domain.

136. Jiang3 also discloses that its macros were independently gated because it discloses various gating schedules: “(g1) gated macros were randomly selected; (g2) high current density macros were gated; (g3) low current density macros were gated; (g5) weakly connected macros were gated.” EX1008, 5. As discussed above, each macro in Jiang is not independently controlled by a sleep transistor.

137. Further, Jiang2 and Jiang3, in using the term “power domain,” are not referring to the claimed power domains. In my opinion, Jiang2 and Jiang3 are referring to *power-gated* domains because each macro is power gated. The ’218 patent refers to “power domains” differently, as domains that are receiving discrete powers. There is no mention of power-gating at all in the ’218 patent.

b) Element 12[c]: Jiang in view of Jiang2/Jiang3 does not teach or suggest a global power mesh, *coupling* to the first local power mesh and the second local power mesh, to provide the power needed by the first power domain and the second domain *separately*

138. Dr. Subramanian provides his opinions on element 12[c] in ¶¶ 78-93. In my opinion, Dr. Subramanian’s analysis of element 12[c] is incorrect for several

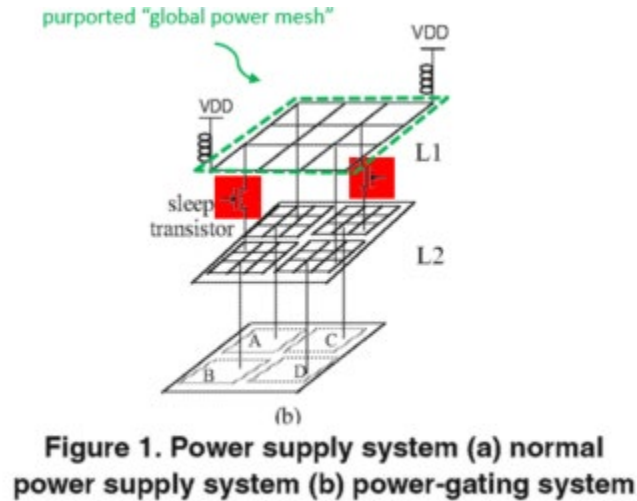
reasons, discussed further below.

(1) Jiang does not teach or suggest a global power mesh “coupling” to the first and second partial local power meshes

139. Dr. Subramanian asserts that Jiang discloses a “global mesh” that is coupled to the first and second partial local power meshes via the sleep transistors. EX1003, ¶¶78-79. I disagree that Dr. Subramanian has shown this.

140. As an initial matter, I disagree that Dr. Subramanian has shown that Jiang discloses a global power mesh. Dr. Subramanian has not shown that Jiang discloses a “global power mesh” because Dr. Subramanian has not shown it is capable of distributing power to multiple power domains. *See* Sec. VII.E. As discussed above, he has not shown that Jiang includes multiple power domains. For the remainder of my analysis, however, even though I disagree that Dr. Subramanian has shown that there is a “global power mesh” or a “first power domain” or a “second power domain,” I will assume that these limitations have been met to facilitate the remainder of the analysis.

141. I also disagree that the connection between the top layer “L1” mesh couples to the first and second partial local power meshes as required by element 12[c]. Instead, the top layer mesh in Jiang couples to the sleep transistors.



142. In the schematic of Figure 1(b), the sleep transistor is shown floating between L1 and L2, but a POSITA would understand that the sleep transistor is actually located in the silicon. EX1004, 1-2; EX2005, 174:16-175:12. The sleep transistor receives the V_{DD} voltage at all times and, therefore, has the same power requirements as the other circuitry receiving the V_{DD} voltage. A POSITA would, therefore, understand that the sleep transistor is itself part of a power domain.

143. As I have explained above, claim 12 requires a specific routing structure—coupling between the global power mesh and the first partial local power mesh. *See* Sec. VII.I. In Jiang, a POSITA would understand that the global power mesh couples to the sleep transistor in a power domain without an intervening first partial local power mesh. As a result, it is my opinion that element 12[c] is not taught or suggested by Jiang.

(2) Jiang does not teach or suggest “providing the power needed by the first and second power domains separately”

144. Dr. Subramanian asserts that the use of sleep transistors satisfies the limitation of 12[c]. EX1003, ¶¶81-82. He asserts that a POSITA would understand that the sleep transistors in Jiang allows the global power mesh to provide the power “separately” by “selectively turning off each domain’s sleep transistor when desired.” EX1003, ¶81. As discussed above, I disagree that Dr. Subramanian has shown this. First, Jiang does not disclose selective turning off of each macro’s sleep transistor independently.

145. Dr. Subramanian further asserts that “Turning *off* the power to the partial local power mesh will necessarily turn *off* the power to the macro underlying that partial local power mesh as well, thus avoiding the current drain of keeping an idle macro powered up. In this way, Jiang teaches a global power mesh that is able to power the first and second power domains separately.” EX1003, ¶82 (emphasis added). I disagree that Dr. Subramanian’s theory of selectively turning off power meets the limitation of 12[c]. A POSITA would understand that turning power off through a sleep transistor is not “providing the power needed.” It is turning the power off. A POSITA would understand that the power is turned off because the macro is “idle” and does not need power. EX1004, 2 (“the gated macros are disconnected

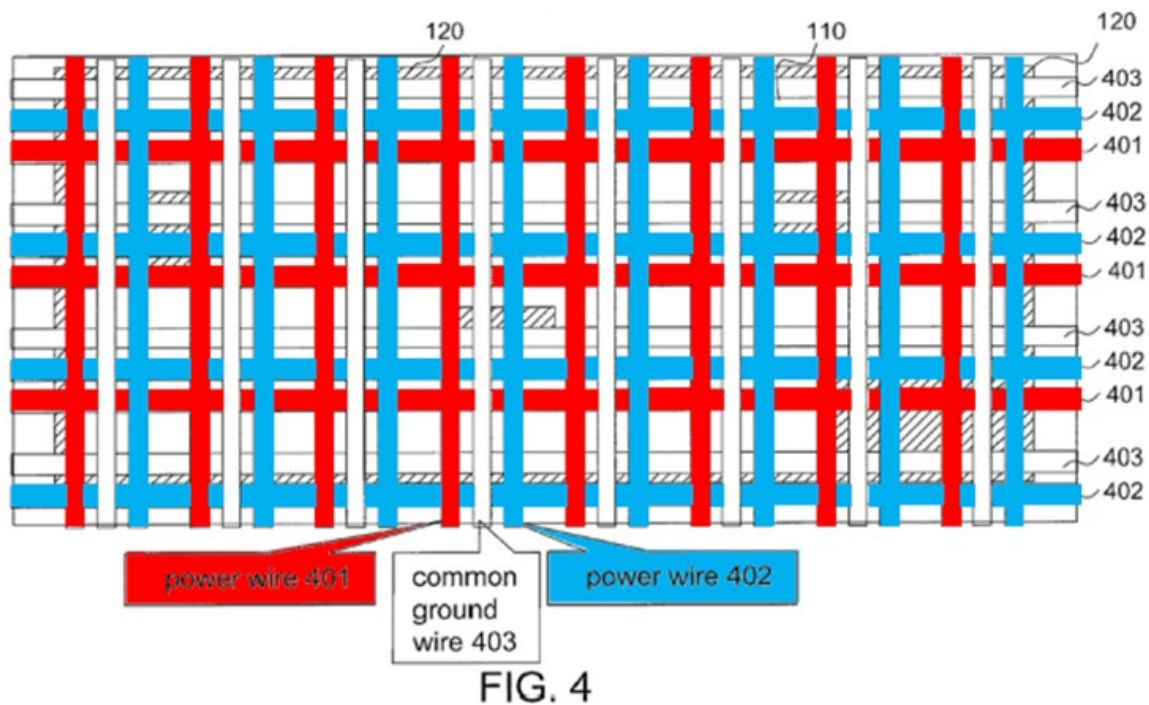
from the power supply during their idle state.”).

146. Even if Jiang taught or suggested individually controlled power-gates, the power-gating turns the power off and does not provide power needed. For example, if macro B were gated and macro C were not gated, the power needed would only be provided to macro B (the purported first power domain) *or* macro C (the purported second power domain). This does not meet the limitation of claim 12[c] which requires providing power needed to the first *and* second power domains. The only time that occurs is when both gates allow power to flow, at which point the global power mesh is not providing the V_{DD} power “separately.”

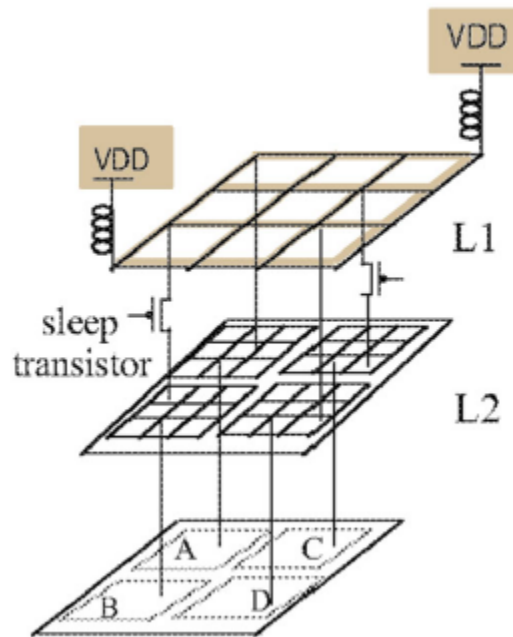
147. I have reviewed Dr. Subramanian’s deposition transcript. At his deposition, Dr. Subramanian suggested that even when a power domain is gated, the circuitry still receives some leakage power. EX2005, 83:6-88:13. But leakage power is not *power needed*. When the macro is gated, it is “idle” and does not *need* power and, therefore, does not meet element 12[c]. EX1004, Abstract (“Power-gating is a technique for saving leakage power by shutting off the idle blocks.”).

148. I also disagree that the global power mesh in Jiang is used to “provide the power needed by the first and second power domain separately” as required by claim 12. As I discussed above, a POSITA would understand that this limitation requires a global power mesh to provide non-zero powers through separate electrical paths. *See* Sec. VII.F-G. An exemplary embodiment of the global power mesh of the

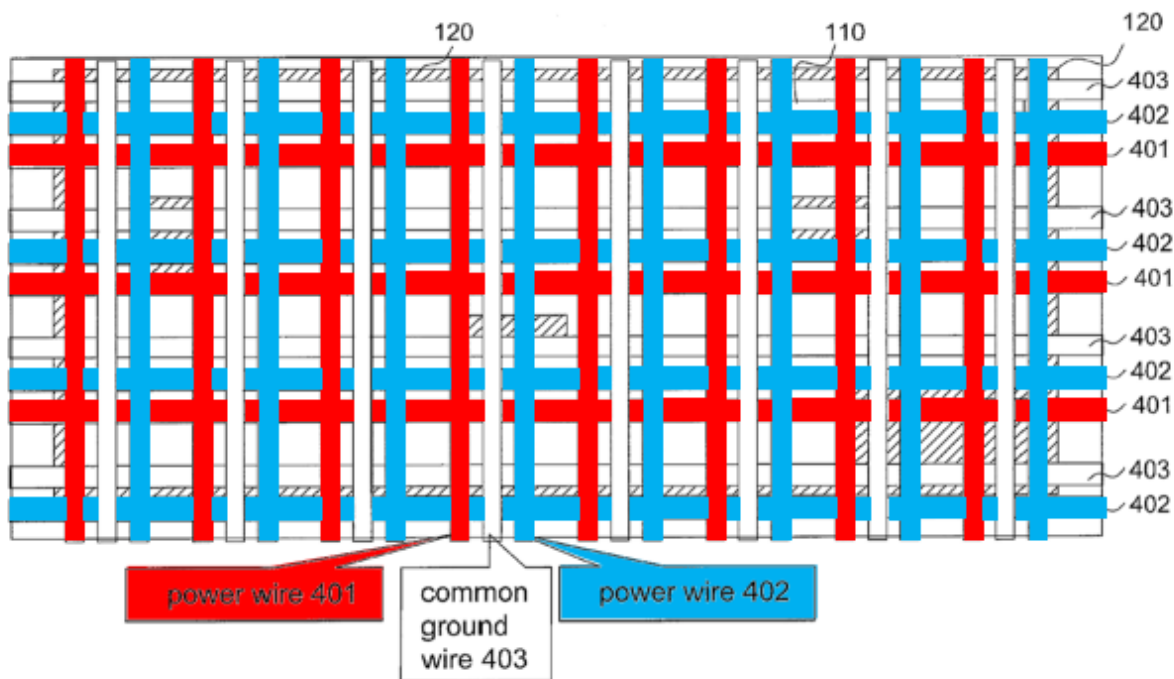
'218 patent is below:



149. In my opinion, Dr. Subramanian has not shown that Jiang's top layer "L1" mesh provides the non-zero powers needed by the first and second power domains through separate electrical paths. Jiang's mesh in "L1" instead uses wires that are electrically connected to provide the same power (V_{DD}) to both macros B and C. Thus, the paths of the global power mesh are not separate electrical paths because the current can flow through any and all of the wires within L1 of Jiang.



150. In contrast to Jiang, the invention requires separate wiring in the global power mesh to provide the power needed to the first and second power domains separately as shown below.



151. A POSITA would understand that Jiang does not disclose a global power mesh to provide the power needed by the first and second power domains “separately” as claimed in the ’218 patent.

(3) It would not be obvious to modify Jiang’s sleep transistors to be independently operable

152. Dr. Subramanian provides an obviousness analysis concerning modifying Jiang’s sleep transistors to be independently operable in paragraphs 83-85.

153. First, independently operable sleep transistors do not meet the claim limitations. *See* Sec. VIII.A.b.2. Under the proper construction for “to provide the power needed to the first and second power domains,” the global power mesh must

provide non-zero power to the first and second power domains. Independently operable sleep transistors applied to Jiang would provide power to the first *or* second power domain, not to the first *and* second power domain, as required by claim 12[c]. When power is being provided to both macros, the global power mesh is not providing the power separately because the wires are electrically connected. *Id.*

154. Second, Dr. Subramanian asserts that a POSITA would be motivated to make the Jiang sleep transistors independently operable to save power or provide more control. EX1003, ¶83 (“*independent power gating* structure is an effective means for reducing leakage power consumption in a system-on-a-chip”).

155. In my opinion, A POSITA would understand that there is no reason to modify Jiang with an additional voltage supply because Jiang configures macros B and C with the same voltage supply. EX1004, Fig. 9. As shown by Figure 9 of Jiang, the author made a strategic decision to gate the blocks in region B and keeps the blocks in region S active. EX1004, 7.

Figure 9. Circuits have different behavior in different regions

S	B
B	S

EX1004, Fig. 9. Therefore, Macros B and C receive the same power at the same time

or are shut off at the same time. Further, there is no motivation to modify the structure of Jiang because the circuit is configured to supply a single V_{DD} to Macros B and C at the same time. This is particularly true because the change would add additional complexity to Jiang's system to control the power provided to each macro independently.

156. Dr. Subramanian also asserts that a modification to Jiang's sleep transistors "would have been a routine application of a known" functionality "with a reasonable expectation of success given its ubiquitous usage." I disagree that Dr. Subramanian has shown this. Dr. Subramanian does not show why a POSITA would have modified Jiang in the first place. Dr. Subramanian merely shows that independently operable sleep transistors were known in other systems, but not that a POSITA would have been motivated to modify the operation of Jiang to include this feature.

(4) It would not be obvious to modify Jiang's "L1"
"global mesh" with Li and/or Chiu

157. Dr. Subramanian also asserts that it would be obvious to modify Jiang's top layer to supply independent voltages to the first and second power domains. EX1003, ¶¶86-93. I disagree that Dr. Subramanian has shown this.

158. Dr. Subramanian asserts that a POSITA would be motivated to supply multiple independent voltages "to power Jiang's different power domains with

different voltages” “to the extent that Jiang’s macros required different voltages to function correctly.” EX1003, ¶¶91. This analysis assumes a motivation that does not exist. It assumes that Jiang’s macros are different than disclosed. Unless Jiang’s macros needed different voltages, a POSITA would not be motivated to make the modification Dr. Subramanian proposes.

159. Jiang itself shows that all macros, Macros A-D, received the same V_{DD} supply and did not need different voltages. Therefore, it is my opinion that a POSITA would understand that Jiang’s macros are designed to receive one power, V_{DD} . A POSITA would not modify the power routing structure for no reason.

160. Dr. Subramanian also asserts that a POSITA would have known to use separate power supplies to save power or provide more control. EX1003, ¶¶86-93. But Jiang also had already “achieve[d] 47% leakage power saving while maintaining the same performance.” EX1004, 1. Without evidence that there would be additional power savings, a POSITA would not be motivated to modify Jiang. For example, a POSITA would recognize that Jiang received the voltage it was designed to receive, V_{DD} , and a different voltage would not be beneficial. And if power were supplied when the macros did not need power (*i.e.*, disabled via power-gating transistors), the independent voltage supplies AMD proposes would waste power, not save power, which is a further reason that a POSITA would not implement that change.

161. A POSITA would also recognize that adding multiple separate power

supplies to Jiang would interfere with its entire premise—to study power gating of the macros. Jiang’s macros needed one voltage, V_{DD} , and were power-gated in order to study the costs and benefits of power gating in the system. EX1004, 1 (“In this paper, we study and quantify the benefits and costs of the power-gating technique in terms of area and power”). A POSITA would not modify the power routing structure provided in Jiang to change its purpose. This is particularly true because there are other costs, such as making the routing more complicated and requiring additional wiring and/or metal layers. A POSITA would not add components without there being a benefit to doing so, which AMD has not identified. *Id.*

162. Dr. Subramanian also argues that “[a]pplying independent supply voltages to Jiang’s global power mesh would have been a routine application of a known feature to Jiang’s device with a reasonable expectation of success.” EX1003, ¶93. I disagree that Dr. Subramanian has shown that altering Jiang is “routine,” “common practice” or that a POSITA would have a “reasonable expectation of success.” Dr. Subramanian has not shown that it was “common practice” to modify Jiang to include multiple independent supply voltages. Dr. Subramanian has not provided any evidence to support the conclusion. All AMD has shown is two other systems that supply two voltages.

163. I also note that Dr. Subramanian never shows that a combination of Chiu’s routing structure or Li’s routing structure with Jiang would result in the

claimed invention. The routing structures of Li and Chiu are different from Jiang and Dr. Subramanian never explains how a combination would read on the claims or why a POSITA would be motivated to select only portions of the routing structure from any particular reference. For example, Li only discloses local power grids in “local sections” and Chiu discloses a direct connection from one grid to the circuitry. Dr. Subramanian never explains how these differences would be accounted for in a combination.

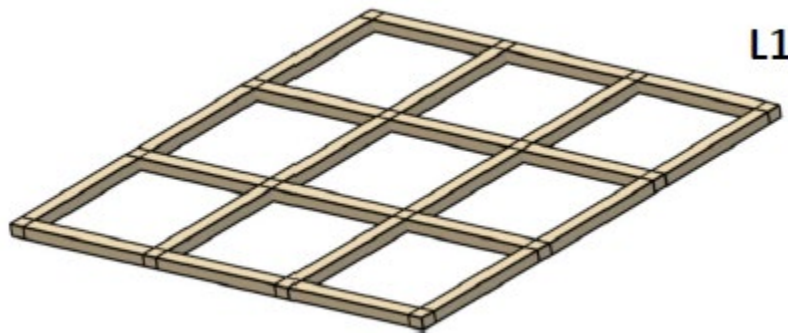
164. Dr. Subramanian asserts that Chiu teaches a global power mesh positioned above a first partial local power mesh. EX1003, ¶107 (citing EX1006, 2:55-61). However, Chiu does not disclose a first partial local power mesh and a second partial local power mesh. EX1006, 2:55-61. Chiu discloses a grid in the upper most layer that provide power to cells through a via stack. *Id.* Dr. Subramanian also mentions voltage rails, which he asserts serve the same purpose as a partial local power mesh. (EX1003, ¶¶62-63, 89, 155 (citing EX1006, 9:6-26)). I disagree that Dr. Subramanian has shown any rail in Chiu to be a “power mesh.”

165. In addition, Dr. Subramanian states that the ’218 patent “acknowledges” that certain features were “common practice” to support its modification of Jiang. EX1003, ¶93. I disagree that Dr. Subramanian has shown anything in the ’218 patent supports a modification of Jiang.

c) Elements 12[E]-[F]: Jiang in view of Jiang2/Jiang 3 fails to disclose a multi-layer global power mesh

166. Dr. Subramanian asserts that Jiang discloses Elements 12[E] and 12[F] because Figure 10 of Jiang discloses two layers. EX1003, ¶¶94-96. I disagree that Dr. Subramanian has shown this. Figure 10 is a different embodiment than Figure 1(b). A POSITA would understand that Figure 10 does not disclose mesh L1 of Jiang.

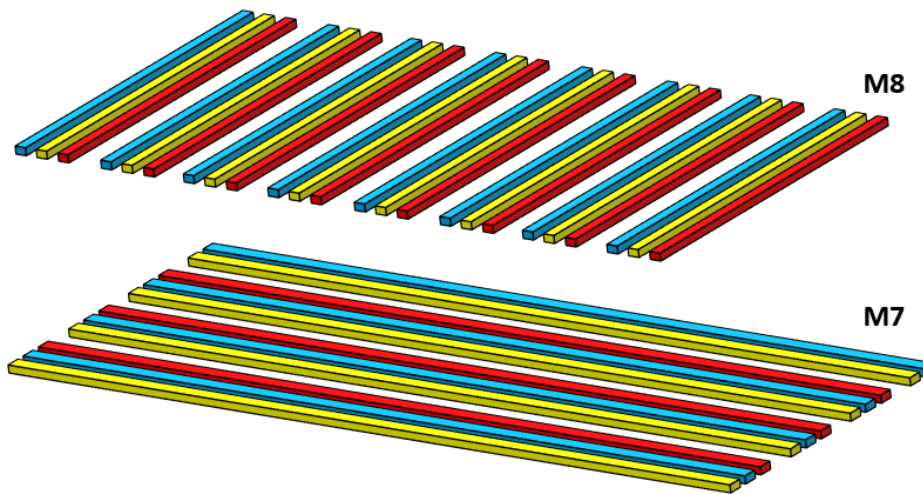
167. Jiang Figure 1(b) discloses a single layer global power mesh on one layer, identified as “L1.”



168. A POSITA would understand that, in Jiang, only one layer is disclosed because only one voltage (V_{DD}) is being provided. In the context of Jiang’s disclosure, a POSITA would not find it necessary to modify Jiang to use two layers to distribute a single V_{DD} when the disclosed single layer was sufficient. For example, in a design with multiple voltages being distributed, there might be a

concern with shorting if there were only one layer, however, there are no concerns with shorting where the mesh distributes only a single V_{DD} , as Jiang Figure 1(b) does.

169. The single layer in Jiang fails to meet the claim limitations, which requires a two-layer global power mesh, as illustrated below.



170. Dr. Subramanian also offers an obviousness analysis in which Jiang is modified by Li and/or Chiu to avoid “shorting.” EX1003, ¶¶97-102. But as discussed above, shorting is not a concern with the structure of Jiang distributing only one V_{DD} . A POSITA would recognize that avoiding shorting is not a motivation to modify Jiang. Thus, a shorting concern would not cause a POSITA to change Jiang to add complexity and metal layers to its already existing structure.

171. Dr. Subramanian identifies other references that he asserts show two-

layer power meshes. EX1003, ¶¶97-102. But without a reason to modify Jiang, these references would not cause a POSITA to change Jiang to add complexity and metal layers to its already existing structure.

172. Dr. Subramanian also relies on his analysis with respect to 12[c]. EX1003, ¶101. This combination fails for the same reasons discussed in 12[c]. *See* Sec. VIII.A.b.4.

173. At his deposition, Dr. Subramanian asserted that there would be a concern with shorting signal wires. EX2005, 209:4-210:7. But Dr. Subramanian is simply speculating that signals would be routed on L1. Jiang Figure 1(b) does not teach or suggest that signal routing is on L1.

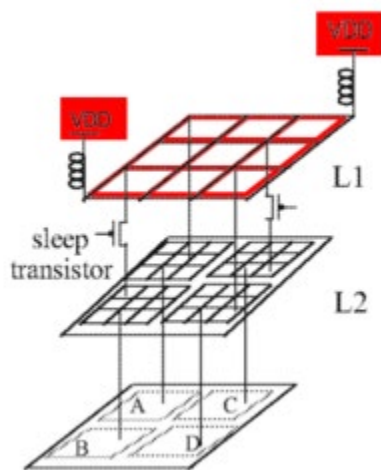
174. Dr. Subramanian states that the modification is a “routine application of a known” “routing structure . . . with a reasonable expectation of success.” EX1003, ¶102. I disagree that Dr. Subramanian has shown that any modification is routine or would have a reasonable expectation of success. Dr. Subramanian refers to two layer meshes as “ubiquitous” but in so doing, he does not appear to address whether the modification he proposes would have a reasonable expectation of success and instead focuses on other systems having multiple layers.

d) Claims 13-18: Jiang fails to disclose any ground routing structure

175. Claims 13-18 depend from claim 12. It is my opinion that the elements

of claims 13-18 are not taught or suggested, at least because the elements of claim 12 are not. As discussed below, because each of the elements of claims 15-18 are not obvious, any claims depending on those claims are also not obvious.

176. In addition, claims 15-18 require specific ground wiring that Jiang Figure 1(b) does not teach or suggest. As shown below, Jiang Figure 1(b) does not teach any ground wiring. As a result, claims 15-18 are not taught or suggested by Jiang alone or in combination.



(1) Claim 15

177. Claim 15 recites, among other things, “wherein the global power mesh comprises: at least one ground wire.” As explained above, Jiang Figure 1(b) does not disclose a ground wire in the “global mesh.”

178. Dr. Subramanian suggests that there is some inherent disclosure of a

ground wire in the global power mesh. EX1003, ¶109 (“To the extent not inherent”).

A POSITA would understand that ground need not necessarily be routed through a global power mesh. A POSITA would understand that ground can be routed in other ways. For example, ground can be provided through a via stack down to the substrate. EX1006, 2:61-63; EX2005, 132:9-11.

179. Dr. Subramanian also asserts it would be obvious to provide grounds through a global power mesh based on Li and Chiu. EX1003, ¶¶109-11. But Jiang itself teaches away from grounding in the global power mesh by showing grounding in the substrate in Figure 2. The symbol circled in red below indicates ground. Such a disclosure would lead a POSITA to a different routing configuration than that disclosed and claimed in the ’218 patent, *i.e.*, implementing a ground in the substrate.

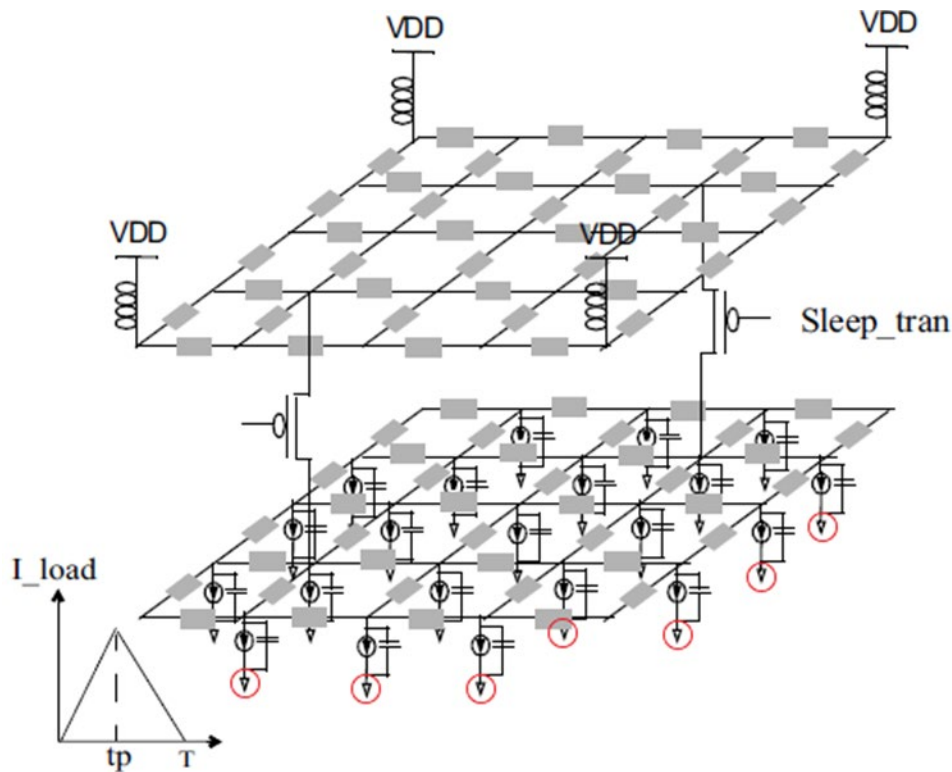


Figure 2. Power gating modeling

180. Dr. Subramanian states that a POSITA would have been motivated to provide a ground connection as part of the global power mesh because (1) ground is necessary for the circuit to function (2) routing through the global power mesh was “routine” and “efficient.” EX1003, ¶109. The modification proposed, however, would require using additional metal layers, which is not “efficient” when the circuitry in Jiang only discloses one V_{DD} . Without an expected benefit, a POSITA would not modify Jiang.

181. Dr. Subramanian also fails to show any reasonable expectation of

success simply concluding that it exists. EX1003, ¶109. There is also no showing that modifying Jiang would be expected to be successful.

182. Dr. Subramanian also cites the motivations provided with respect to 12[e] and 12[c]. EX1003, ¶¶110-11. I have explained why a POSITA would not be motivated to change Jiang above with respect to 12[c] and 12[e].

183. I, therefore, disagree that a POSITA would have a motivation to modify Jiang to include a ground in the global power mesh with a reasonable expectation of success.

(2) Claim 16

184. Claim 16 depends from claim 15 and adds the additional limitation “wherein the first partial local power mesh comprises: at least one first local ground wire that couples to the ground wire of the global power mesh.” It is my opinion that Jiang does not teach or suggest this limitation because a POSITA would understand that Jiang Figure 1(b) does not disclose a ground on the L2 layer. Dr. Subramanian again suggests that there is some inherent disclosure. EX1003, ¶113. I disagree that Dr. Subramanian has shown this. As previously discussed, there are other ways to route a ground wire and Figure 2 of Jiang suggests to a POSITA that the ground is in the substrate. Chiu also suggests using via stacks to directly route a ground from the upper most layer to the silicon layer. EX1006, 2:55-63.

185. Dr. Subramanian also asserts it would be obvious to include a first local ground wire assuming there was a ground wire as part of the global power mesh. EX1003, ¶113. But for the reasons discussed with respect to claim 15, a POSITA would not be motivated to include a ground wire in the global power mesh of Jiang to start with.

186. Dr. Subramanian relies on the purported wiring in Li, but as Dr. Subramanian admitted, even in Li, the ground connects to the substrate so that the ground switch can operate. EX2005, 174:16-175:22. Thus, Li cannot be relied on for this limitation.

187. Similarly, Dr. Subramanian relies on the combination of Jiang with Li and/or Chiu it proposes for claim limitations 12[c] and 12[e]. EX1003, ¶116. But for the reasons those modifications fail, AMD's argument with respect to claim 16 also fails. *See* Sec. VIII.A.b.4-c.

188. Even if a POSITA were motivated to include a ground wire in the global power mesh, Chiu actually teaches away from coupling grounds in the global power mesh and grounds in a partial local power mesh. A POSITA reviewing Chiu would be discouraged from using additional metal layers when grounds in the purported global power mesh can connect down to the circuitry through a via stack. EX1006, 2:55-63.

189. Dr. Subramanian also asserts that a POSITA would be motivated to add

ground lines to the local partial local power mesh because it was “known,” or because it was a “routine application of a known functionality.” EX1003, ¶115. I disagree that Dr. Subramanian has shown this. Dr. Subramanian has not shown that adding ground lines to a partial local power mesh is well-known or “routine” or would have a reasonable expectation of success. At best, he has shown that one reference, Li had ground wires in a local power grid. As I mentioned above in VIII.A.b.4. Dr. Subramanian has not shown that Chiu discloses ground in a local power mesh.

(3) Claim 17

190. Claim 17 recites “wherein the second partial local power mesh comprises: at least one second local ground wire that couples to the ground wire of the global power mesh.” Dr. Subramanian does not provide any additional reasons that claim 17 is disclosed beyond what it argued with respect to claim 16. EX1003, ¶¶118-119. Thus, for the same reasons claim 16 is not obvious, claim 17 is also not obvious, it is also my opinion that claim 17 is not taught or suggested by Jiang alone or in combination.

(4) Claim 18: Jiang fails to disclose a “Same Ground Wire”

191. Claim 18 recites that the first local ground and the second local ground

wire “share the same ground wire of the global power mesh.” In my opinion, a POSITA would understand that the specific wiring required by claim 18 is not taught or suggested by Jiang alone or in combination.

192. First, Jiang itself discloses no ground wires in Figure 1(b) and, therefore, cannot disclose the limitation of claim 18. In addition, for all the reasons discussed above with respect to claims 15-16, it is not inherent or obvious to include a ground wire in any mesh in Jiang.

193. Dr. Subramanian asserts that Jiang would have a single ground supply voltage. EX1003, ¶120. But that is not what Jiang discloses. Jiang Figure 1(b) does not disclose any ground in its meshes. Further, Jiang could have implemented ground supply voltages in a different way than the manner claimed. For example, more than one ground can be supplied in a chip and there is not necessarily only one way to do it.

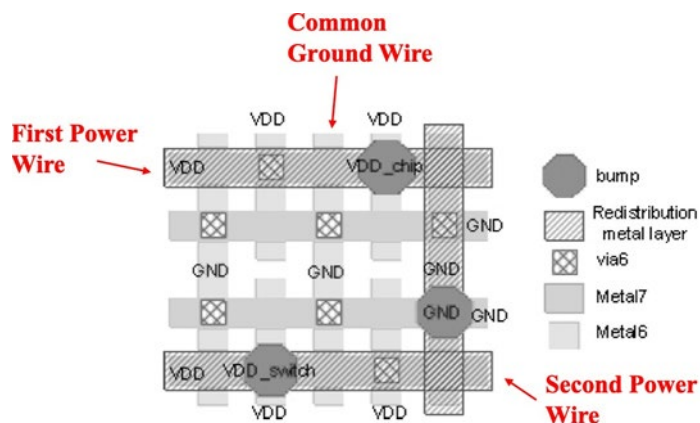
194. Dr. Subramanian appears to rely on a prior combination of Jiang with Li or Chiu for his analysis. EX1003, ¶¶120-121. For the reasons I have already discussed, I disagree that Dr. Subramanian has shown that a POSITA would modify Jiang based on Li or Chiu.

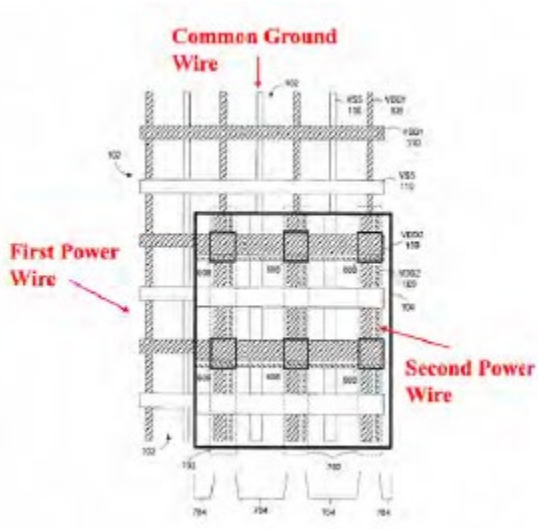
195. Even if there were a single ground supply disclosed in Jiang and Jiang were modified with Li and/or Chiu, I disagree that Dr. Subramanian has shown that the modified Jiang system would teach or suggest the limitation of claim 18 because

Dr. Subramanian cannot show a “same ground wire.”

196. Dr. Subramanian asserts that “all the ground wires in the global mesh” are the “same ground wire.” EX1003, ¶121. But a POSITA would not interpret “same ground wire” in this manner. *See* Sec. VII.H. Such an interpretation is conflating the same ground *potential* with same ground *wire* or improperly equates a ground “mesh” with a ground “wire.” A POSITA would not understand a ground mesh or wires with the same ground potential to be the “same ground wire of the global power mesh.” I address these arguments further below with respect to Li and for the same reasons Li does not teach or suggest claim 18, Jiang alone or in combination also does not. *See* Sec. VIII.C.d.2.

197. Dr. Subramanian also labels a “common ground wire” in certain figures of Li and/or Chiu. EX1003, ¶111.





198. These purported “common ground wire(s)” have not been shown to be the “same ground wire” of claim 18 because neither Li nor Chiu discloses where any ground connections to lower layers are. Thus, a POSITA would understand that these purported “common ground wire(s)” are not shared by a first and second local ground wire as required by claim 18. Further, Dr. Subramanian never even attempts to show that Chiu even discloses partial local power meshes. Thus, Chiu cannot teach or suggest claim 18.

199. For all of these reasons, it is my opinion that claims 12-18 are not unpatentable based on the Grounds 1-2 challenge.

B. Grounds 3a and 3b: Claims 1-11 and 19-20 are not obvious over Jiang/Jiang2/Jiang3/Li/Chiu and further in view of Bertolet and/or LPMM

200. Dr. Subramanian’s opinions on Ground 3 are in paragraphs 122-148. Dr. Subramanian concludes that the combination of references in Ground 3 renders

the terms obvious. I disagree for the reasons identified below.

201. Ground 3a and 3b challenges claims 1-11 and 19-20. Ground 3 is based on Grounds 1-2 in further view of Bertolet and LPMM. EX1003, ¶122. In fact, he incorporates these grounds into Ground 3. EX1003, ¶¶123-124, 131-148. In my opinion, for the same reasons Grounds 1-2 do not render claims 12-18 obvious, Ground 3 also does not render claims 1-11 and 19-20 obvious.

a) Dr. Subramanian fails to show all elements of the claims were taught or suggested by any reference

202. Independent claims 1 and 19 recite the use of an automatic placement and routing (“APR”) tool to form various power routing structures in a multi-voltage power domain design. An APR tool is a tool that can perform routing and placement for a power routing structure in an integrated circuit. As the patent explains, APR tools are used by a circuit designer to design the power routing of chips:

For example, the well-known automatic placement and routing (APR) tool can only support circuits having single power domain. Therefore, a circuit designer can only rely on the most primitive method to design the power routing of multiple power domains, such as the manual routing. Obviously, such design approach is not only complicated but also inefficient.

EX1001, 1:37-43. The patent further explains:

Besides, the power mesh arrangement method disclosed in the invention can be implemented in the APR tool easily so that the user can use the APR tool to automatically complete the circuit layout so as to increase the circuit design efficiency.

Id., 2:38-41.

203. At the time of the invention of the '218 patent, APR tools supported single-power domain integrated circuits. However, there were no well-known off-the-shelf, conventional, APR tools that could be used to automatically perform the steps in claims 1-11 or 19-20 for multiple power domain chips. Dr. Subramanian states that the '218 patent was incorrect in explaining that the well-known APR tools only supported circuits having a single power domain. EX1003, ¶¶39, 50. I disagree because Dr. Subramanian has not shown any reference to support his opinion. He also seems to assume that the statement in the patent means that there could be no automation in the context of a multi-power domain chip, which is incorrect. The context makes clear that the point being made is that there is no well-known APR tool for multiple power domain chips.

204. Regardless, the issue is whether any reference teaches or suggests the claim limitations at issue, not whether there was a tool available to support multiple power domain chips. Dr. Subramanian has not identified any references alone or in combination that teaches, suggests, or discloses the elements of claims 1 or 19. In particular, he does not identify any APR tools that perform the steps claimed in 1[a], 1[b], 1[c], 1[d], or 1[e] or 19[a]. There is simply no disclosure of the “forming” steps or the “coupling” steps by an APR tool taught or suggested in the art.

205. Dr. Subramanian repeatedly attempts to assert that there were APR tools in 2007 that *could* automatically place and route the structure of Jiang or that it “would have been the expectation.” EX1003, ¶¶125-26, 128-29. I disagree that he has shown that, as discussed further below.

206. The references Dr. Subramanian cites, Bertolet and LPMM, do not disclose any suitable tools available or that were known that could perform the claimed steps, for power routing of a multi-voltage design, alone or in combination.

207. Bertolet is an article from 1997, nearly ten years before the priority date, and relates to the use of a “custom SKILL program” in a *single power domain* chip. EX1013, 126. A POSITA would recognize that Bertolet relates only to a single power domain chip because Bertolet recites that that it was fabricated in a “2.5V CMOS n-well technology.” EX1013, 124. Bertolet discloses that the custom SKILL program can generate grids by area and level of metal, creating, what Bertolet describes as “power terrains.” EX1013, 126. A POSITA would understand that power terrains are not power domains because Bertolet receives only one voltage. Even if Dr. Subramanian were correct that power gating creates power domains (EX1003, ¶129), Bertolet also does not discuss power-gating.

208. Dr. Subramanian concedes that Bertolet only discusses a single voltage design. EX2005, 266:22-267:12 (“with respect to Bertolet I told you that it was silent on the number of voltages beside identifying the external voltage is 2.5 volts.”). This

further confirms that a POSITA would understand that Bertolet does not teach or suggest routing and placement in a multi-voltage system and would not perform the steps of claims 1-11 and 19-20.

209. LPMM further confirms that Bertolet, from 1997, was not intended or used for multi-voltage designs. LPMM explains that multi-voltage designs were new as of 2007. EX2013, 21. For example, LPMM describes that a “new approach is to partition the internal logic of the chip into multiple voltage regions or power domains, each with its own supply.” *Id.* Accordingly, a POSITA would understand that Bertolet, in 1997, was not being applied toward these new approaches described in LPMM like multi-voltage designs.

210. LPMM is a reference related to low power design. EX1012, 61. LPMM references multi-voltage designs but does not disclose any tool capable of performing the steps of the APR tool claims of the '218 patent. Rather, Dr. Subramanian cites LPMM for a power network synthesis (PNS) capability. EX1012, 177-178. The synthesis capability in LPMM does not disclose forming a global power mesh or partial local power meshes or coupling those meshes as claimed. A POSITA would understand that it does not disclose any of the claimed steps in 1-11 or 19-20.

211. The portion of LPMM cited by Dr. Subramanian confirms that it simply discloses an EDA tool that can provide “some level of automated power network

synthesis (PNS) capability for the distribution of power across a design” and recommends using such a capability “wherever possible.” EX1012, 177-78. This suggests to a POSITA that automated capabilities are not necessarily “possible” to use in multi-voltage designs. It does not teach or suggest to a POSITA any steps of the claims 1-11 and 19-20.

212. Dr. Subramanian also discussed an ARM chip of LPMM that shows a multi-voltage design. EX1003, ¶127. He asserts that LPMM recommends using an APR tool for this application. *Id.* But Dr. Subramanian never shows that LPMM discusses using any automation with the ARM chip specifically. That is not what LPMM discloses. LPMM also does not recommend using an APR tool to perform any of the steps of claims 1-11 or 19-20.

213. Dr. Subramanian also asserts that a POSITA would have found it “obvious” to form and couple Jiang’s power meshes with “an APR tool.” EX1003, ¶126. I disagree that Dr. Subramanian has shown this. Dr. Subramanian does not cite any reason to use an APR tool with Jiang, which is discussed further below.

214. Dr. Subramanian asserts that Bertolet could form a global and partial local power mesh. EX1003, ¶¶126, 129. I disagree that Dr. Subramanian has shown this. Bertolet discloses use of a custom SKILL program to form various “power grids” in a *single power domain* chip, which a POSITA would understand is inapplicable to multi-voltage chips because, for example, it does not take into

account any power domains or multiple different power wires. EX1013, 126. Further, Bertolet describes a configuration for “global” routing and a local interconnect on one level of metal. *Id.* But nothing in Bertolet teaches or suggests forming that “global” routing is the same as a global power mesh in the ’218 patent, *i.e.*, a network of intersecting wires capable of distributing power to multiple power domains.

215. Similarly, nothing in Bertolet teaches or suggests forming a first or second partial local power mesh according to the position of a first or second power domain, respectively. Bertolet never discusses power domains.

216. The other references Dr. Subramanian cites also do not disclose the steps of claims 1-11 or 19-20.

217. For example, Dr. Subramanian cites Li. EX1003, ¶128. But Li discloses an “automated procedure . . . connecting local logic to the top-level power grid.” EX1005, 493. This procedure suggests the automated procedure is related to connecting the circuitry from the chip to the top level power grid in Li. Li is silent on how any connections to these local power grids would have been made. Thus, no connection to local power grids via an APR tool (or any other specific method) has been disclosed in Li.

218. In my opinion, Li teaches away from performing the steps claimed. The chip in Li was based on a reused design. Li explains “Due to the importance of the

stringent time-to-market demand, design reuse has become a common practice in today's IC industry." EX1005, 499; *see also id.*, 491 ("The combination of continually rising complexity of chip designs, the reuse of existing IP, and the efficient verification methodologies have all helped to expedite the processor design cycle."). The purpose of Li was to prepare an LVS methodology that could be used to confirm that there were no errors in the modification of the prior design. Thus, a POSITA would be discouraged from starting from scratch based on Li and would instead be encouraged or led to also reuse old designs and implement a similar LVS methodology.

219. Dr. Subramanian also cites Jiang, Jiang2, Jiang3, Li, Chiu, LPMM, and Bertolet. EX1003, ¶¶25, 130. But Dr. Subramanian has not shown that Jiang, Jiang2, Jiang3, or Chiu even mention a power routing arrangement method or APR tools.

220. Thus, Dr. Subramanian does not cite any references that teach or suggest any of the following steps:

- 1[a]: forming a first partial local power mesh according to the position of a first power domain of the integrated circuit by an automatic placement and routing (APR) tool;
- 1[b]: forming a second partial local power mesh according to the position of a second power domain of the integrated circuit by the APR tool;

- 1[c]: forming a global power mesh that is utilized to provide the power needed by the first and the second power domains by the APR tool;
- 1[d] coupling the first partial local power mesh to the global power mesh and the first power domain by the APR tool;
- 1[e] coupling the second partial local power mesh to the global power mesh and the second power domain by the APR tool;
- 19[a]: providing a global power mesh, positioned above a first power domain and a second power domain, comprising at least one first power wire that provides the voltage needed by the first power domain, at least one second power wire that provides the voltage needed by the second power domain, and at least one ground wire that provides the ground potential needed by the first power domain and the second power domain by an automatic placement and routing (APR) tool;”
- 19[b]: “coupling the first power wire and the ground wire of the global power mesh to the first power domain by the APR tool”

221. Dr. Subramanian asserts that a POSITA would know “how to use” an APR tool with a multi-voltage chip. EX1003, ¶128. I disagree that Dr. Subramanian has shown this. There were no well-known tools for that function, so there is no basis to assume that POSITA would know how to use it.

222. Dr. Subramanian also cites the ’218 patent for the statement that “APR

tools were well-known.” EX1003, ¶126. But the ’218 patent refers to the use of APR tools that support single power domain chips. Dr. Subramanian has not shown any APR tool that performs the steps claimed.

223. Dr. Subramanian also cites a press release (EX1025), but this does not teach or suggest any elements of claims 1 or 19. EX1003, ¶129. Dr. Subramanian makes a number of assumptions about APR tools being used, but there is simply no disclosure that they were actually used, much less that they performed the claimed methods. I understand that AMD and Dr. Subramanian have not shown that the press release is prior art. But even if it were, if anything, it confirms that the use of an APR tool for multi-voltage designs was not well-known and was uniquely challenging or difficult for a POSITA. Otherwise, there would be no reason to issue a press release.

b) Dr. Subramanian fails to show a motivation to combine references to achieve the claimed invention

224. As discussed above, Dr. Subramanian fails to show that all elements of the APR tool claims are disclosed. Even if he did, it is my opinion that a POSITA would not combine the references with a reasonable expectation of success.

225. First, Dr. Subramanian relies on some combination of capabilities from various references, such as the SKILL program of Bertolet and the synthesis capabilities discussed in LPMM, to argue a POSITA would be motivated to use “an” APR tool. EX1003, ¶¶125, 128-130. I disagree that Dr. Subramanian has shown this.

Dr. Subramanian has not identified an APR tool that taught or suggested the steps of the invention and has provided no motivation for a POSITA to combine or modify existing APR tools to perform the steps of the claims 1-11 or 19-20.

226. Even if Dr. Subramanian were only citing Bertolet or LPMM alone, as discussed above, neither alone could form the structure of Jiang, let alone perform the steps of claims 1-11 and 19-20.

227. Dr. Subramanian asserts that it would be obvious to use “an APR tool” because it would save time and effort in chip design and LPMM recommends using “automated power network synthesis” “whenever possible.” EX1003, ¶¶125-26, 128. I disagree that Dr. Subramanian has shown this. Nothing in LPMM teaches or suggests using an APR tool to perform the steps of claims 1-11 and 19-20.

228. Even if there were a motivation, Dr. Subramanian fails to show that a POSITA looking for “an APR tool” to save time and effort in chip design, *would* turn to Bertolet or LPMM’s PNS capabilities. Dr. Subramanian fails to identify a motivation to use the Bertolet or LPMM capabilities.

229. In addition, Dr. Subramanian also asserts that a POSITA would be motivated to use an APR tool to implement Jiang’s Figure 1(b). EX1003, ¶¶125-26, 128-29. I disagree that Dr. Subramanian has shown this. Jiang’s cartoon schematic in Figure 1(b) does not suggest the need for APR tools. Jiang Figure 1(b) is a quantitative model used to illustrate the costs and benefits of power-gating. EX1004,

1-2. Jiang never contemplates that Figure 1(b) could be turned into a chip (the step at which APR tools are generally applied) and creating a chip would defeat the purpose of Jiang—to model power gating. EX1004, 1-2. Even Dr. Subramanian states that “A POSITA would know that the RTL-to-GDSII design steps included placement and routing of the power network.” EX1003, ¶129. But he provides no reason to generate a GDSII design for Jiang. There is none. A POSITA would effectively have to design an entirely new chip because Jiang Figure 1(b) is just a qualitative model to study costs and benefits of power gating. Thus, it is my opinion that a POSITA would not be motivated to use APR tools with Jiang’s Figure 1(b).

230. Dr. Subramanian asserts a reasonable expectation of success in arriving at the claimed invention. EX1003, ¶129. I disagree that Dr. Subramanian has shown this. Dr. Subramanian has not even shown that all elements of the claims were disclosed, or how the combination of references would work to arrive at the claimed invention. They would not. Rather, the conclusion appears to be reliance on the misstatements that Bertolet or LPMM *could* perform the method steps claimed. A POSITA would recognize that Bertolet and LPMM do not teach or suggest any of the steps claimed and, as a result, a POSITA would not expect them to be suitable for use alone, much less together or with Jiang’s Figure 1(b) alone or modified as described in Grounds 1-2, or expect success to achieve whatever combination Dr. Subramanian proposes amongst these choices.

231. Dr. Subramanian also argues expectation of success based on other documents, such as a press release (EX1025), and an article (EX1020). EX1003, ¶129. I disagree that Dr. Subramanian has demonstrated that these show a reasonable expectation of success in the combination Dr. Subramanian is proposing. Dr. Subramanian does not propose using the tools identified in these references. None of the references shed light on whether a POSITA would have a reasonable expectation of success using an existing “APR” tool combined with Jiang to reach the claimed invention. A POSITA would recognize that the press release does not inform on the state of the art and offers no details on the capabilities of the programs. It appears to simply be marketing material.

232. For all of these reasons, it is my opinion that claims 1-11 and 19-20 are not unpatentable based on the Ground 3 challenge.

C. Ground 4: Claims 12-18 are not obvious over Li in view of Jiang

- a) 12[a]-12[b]: Li alone or in combination does not suggest a local power grid that corresponds to the location of, and couples to, a first and second power domain (Core and Switch)**

233. Dr. Subramanian provides opinions on Ground 4 at paragraphs 149-181. He concludes that Li alone or in combination with Jiang teaches or suggests each limitation of claims 12-18. I disagree that Dr. Subramanian has shown this.

234. Dr. Subramanian asserts that Li discloses a local power grid that

corresponds to the location of and couples to the first and second power domains, which he identifies as the core and switch regions of the chip. EX1003, ¶¶149, 152, 155, 160-61. I disagree that Dr. Subramanian has shown this. A POSITA would understand that Li does not disclose the location of the local power grids because Li discloses that they are in the “local sections” but does not disclose where the “local sections” are. A POSITA would not interpret silence as a disclosure and would understand that there are only local power grids in specific undisclosed “local sections.”

235. More specifically, Dr. Subramanian relies on the following disclosure from Li for elements 12[a] and 12[b]: “The power and ground lines in the local sections are grided on Metal-2 through Metal-5, on which the local power grids are formed at the block level. The local power grids are left floating until final assembly at the full-chip level.” EX1005, 493. He concludes that this means there are local power grids in the core and switch sections of the chip. EX1003, ¶¶152-54. I disagree that Dr. Subramanian has shown this. A POSITA would understand that the “local power grids” of Li are only in the “local sections.” Neither Li nor Dr. Subramanian explains, teaches, or depicts where any “local sections” are actually located and thus, they are not disclosed.

236. During his deposition, Dr. Subramanian stated that “local sections” were referring to the “local layers” used for the local power grid, *i.e.*, metals layers

2-5, in contrast to the “global sections.” EX2005, 257:4-258:1. I disagree that Dr. Subramanian has shown this. A POSITA would understand that Li already discloses that the “local grid” is on metal layers 2-5. A POSITA would find it redundant to also refer to layers 2-5 as a “local section.” A POSITA would have expected Li to identify any layers used for the local power grid as “local layers” not “local sections.” I also disagree that Li is contrasting “local sections” with “global sections.” The phrase “global sections” is not used in the Li reference.

237. Dr. Subramanian relies on other disclosures of Li related to claim limitations 12[a] and 12[b]. A POSITA would not understand these other disclosures to teach or suggest placing local grids at the core or switch areas of the chip either. For example, Dr. Subramanian relies on the phrase “at the block level” in Li which he argues means that the local power grids “are formed to correspond to the underlying circuitry that they will supply.” EX1003, ¶153. However, beyond providing a cursory description, Dr. Subramanian does not provide further explanation nor does he prove that a POSITA would thus understand “at the block level” to teach placing local grids at the locations of the core or switch areas. A POSITA would understand that being formed at “block level,” does not change that at “block level” is still “in the local sections.” EX1005, 493.

238. Dr. Subramanian also states that it would have been obvious for Li’s local power grids to be partial local power meshes having their positions correspond

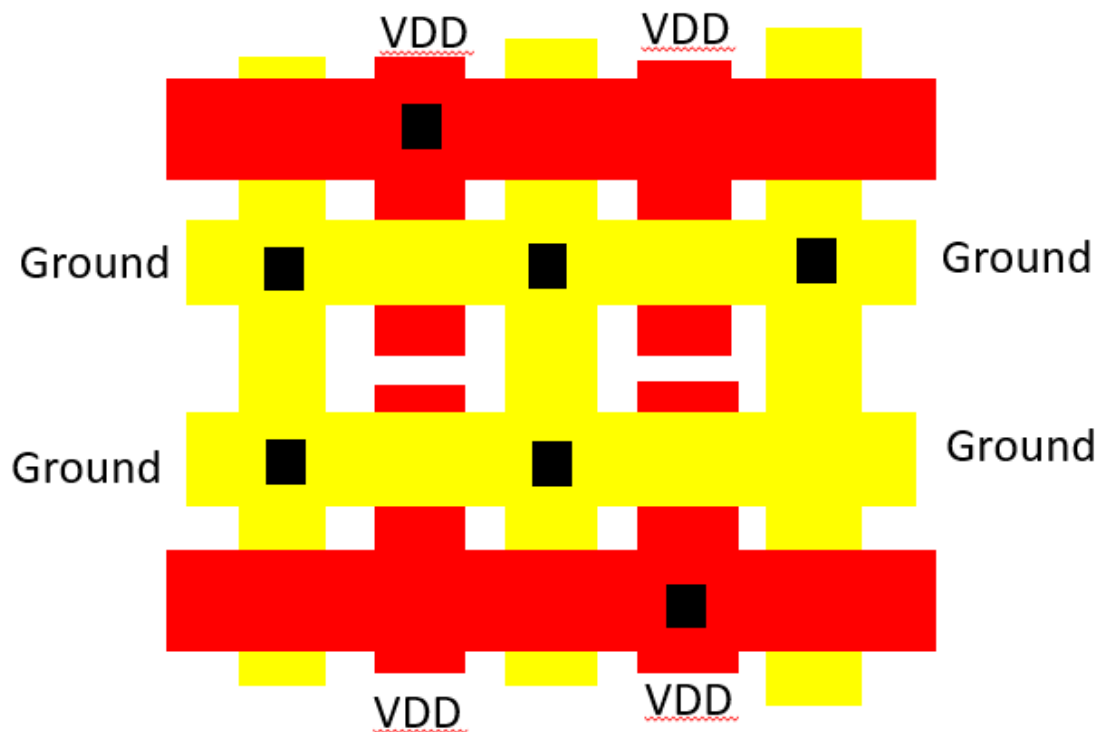
to the positions of their respective power domains based on Jiang because it would be “combining prior art methods according to known methods to yield predictable results.” EX1003, ¶155. I disagree that Dr. Subramanian has shown this. The purpose of the location of the grids on “L2” of Jiang was to illustrate the specific qualitative model discussed in Jiang. There is no such similar reason to position a local power grid in Li. I also note that POSITA would not modify Li with Jiang to add “local power grids” in locations where the “local power grids” were not needed because there is no reason to add additional wiring to a space constrained integrated circuit. *Id.* Without a benefit, a POSITA would not modify Li.

239. In my opinion a POSITA would understand that Li is silent on the location of the power grids and therefore, does not teach or suggest any of the elements that rely on a first or second partial local power mesh, including elements 12[a], 12[b], 12[c], 12[d], 14, and 16-18.

b) 12[C]: Li does not teach or suggest a global power mesh on metal layers 6 and 7

240. Dr. Subramanian asserts that there is a global power mesh on metal layers 6-7. EX1003, ¶164. I disagree that Dr. Subramanian has shown this. There is no teaching or suggestion of any network of intersecting wires capable of distributing VDD_Switch and VDD_Core to the Core and Switch power domains on metal-6 and metal-7. A POSITA would understand from Figure 3 that metals-6

and 7 disclose only one V_{DD} on metal-6 and metal-7. The wires themselves are labeled only V_{DD} , suggesting to a POSITA only one voltage. Li does not disclose if or how V_{DD} relates to either V_{DD_Switch} or V_{DD_Core} . I have created the following to illustrate the actual wiring disclosed on the metal 6 and metal 7 layers in Figure 3:



241. Figure 3 of Li shows a redistribution layer that labels some wires V_{DD_Switch} and V_{DD_Core} . But Dr. Subramanian explained that he is not relying on the redistribution layer (RDL) of Li for the “global power mesh.” EX2005, 85:3-

86:20.

242. In Li, a POSITA would understand that it makes sense to only include one V_{DD} on metals-6 and 7 in the chip disclosed in Li because only certain sections of the chip would receive V_{DD_Switch} and other sections would receive V_{DD_Chip} . Li itself explains that “ V_{DD_chip} provides power for all the internal logic except the node controller, packet manager, switch, and HT/SPI-4 ports.” EX1005, 495. Therefore, a POSITA would not use space in the chip on lower layers, such as the metal-6 or -7, unless there was some need to do so, such as providing the power to the circuitry below.

243. Dr. Subramanian also relies on the statement from Li that discloses that the metal-6 and metal-7 layers are “extensively used in distributing power and ground across the chip.” EX1003, ¶164; EX1005, 493. But this does not teach a network of intersecting wires of both powers across the entire metal-6 or metal-7 layers.

244. For the reasons discussed above, it is my opinion that neither Figure 3 nor any other disclosure in Li identifies a network of intersecting wires capable of distributing both V_{DD_Chip} and V_{DD_Switch} power wires. In my opinion, Dr. Subramanian has failed to show that there is a global power mesh disclosed in Li.

245. In my opinion, because Dr. Subramanian has not shown that there is a global power mesh, Dr. Subramanian cannot show that any claim limitation reciting

a global power mesh is met, including 12[c], 12[e]/[f], 13, 15-18.

c) 12[C]: Li does not teach or suggest coupling the first and second partial local power meshes to the global power mesh

246. Dr. Subramanian asserts that Li discloses coupling the first and second partial local power meshes to the global power mesh. EX1003, ¶¶154, 160, 164. I disagree that Dr. Subramanian has shown this. A POSITA would understand that there is no such teaching or suggestion in Li.

247. To the contrary, a POSITA would recognize that Li discloses a connection between the “top-level power grid” and the “local logic” (the chip circuitry). EX1005, 493.

248. Dr. Subramanian asserts that the top-level power grid necessarily also includes connecting the local power grids. EX1003, ¶¶152-53. I disagree that Dr. Subramanian has shown this. Other options are possible. For example, local grids in the core or switch locations are not disclosed and thus may not exist in Li, in which case there would be no connections to the local power grid possible at those locations. By way of another example, Dr. Subramanian admitted, there can be connections from the “top-level power grid” to a silicon transistor rather than a connection to a local grid. EX2005, 174:16-175:22. Li itself discloses that kind of connection to the switch in the core section of the chip so that the ground is routed

through the switch so that the core can be electrically isolated. EX1005, 494.

249. By way of yet another example, Li discloses a connection between the local logic and the top-level grid: “At the final stage of the layout design, an in-house automated procedure is applied, connecting local logic to the top-level power grid, to implement a complete full-chip power distribution network.” EX1005, 493.

d) Claims 13-18

250. It is my opinion that the elements of claims 13-18, which depend from claim 12, are not taught or disclosed by Li alone or in combination because the elements of claim 12 are not taught or suggested. In addition, it is also my opinion that certain elements of claims 16-18 are also not taught or disclosed by Li alone or in combination.

(1) Claim 16: Li Fails to disclose a first partial local power mesh that comprises at least one first local ground wire that couples to the ground wire of the global power mesh

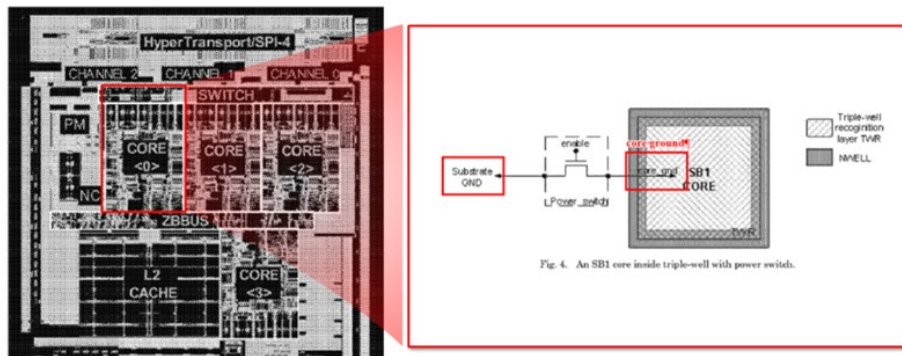
251. Claim 16 recites a “first local power mesh that comprises: at least one first local ground wire that couples to the ground wire of the global power mesh.”

252. Dr. Subramanian asserts that claim 16 is rendered obvious in view of Li alone or in combination. EX1003, ¶¶178-79. I disagree that Dr. Subramanian has shown this. Dr. Subramanian has not shown that Li teaches, suggests, or renders this

limitation obvious to a POSITA.

253. Dr. Subramanian states that the “global power grid connects to the local logic (power domains) *through* the local power grids.” EX1003, ¶178; Pet., 68. But, during his deposition he admitted that the global grid at the core actually connects to the *switch* in the power domain. EX2005, 174:16-175:22. This is what Li expressly discloses: “At the final stage of the layout design, an in-house automated procedure is applied, connecting the local logic to the top-level power grid.” EX1005, 493. This type of connection does not meet the limitation of claim 16. *See* Sec. VII.J.

254. A POSITA would understand that the ground from the global power mesh must first drop to the ground in the power domain (in the substrate) for the power switch to operate. As shown in detail below, the switch connects substrate ground to the core ground. The switch in Li operates to disable the core by cutting off the ground and a POSITA would understand that the ground for the core must be routed through the switch for the switch to operate and for the core to: (1) be “electrically isolated,” (2) be “isolated from the ground outside the core,” and (3) have a “different internal ground net.” EX1005, 494-95. Li describes the ground wiring at the core in detail and there is no disclosure of a local power grid. A POSITA would understand that there is, therefore, no local power grid disclosed at the core and that claim 16 is therefore not taught or disclosed in Li.



255. Dr. Subramanian also asserts a theory of inherency that a POSITA would understand that Li's disclosure "necessarily" requires the connection from the global power mesh through the local grids to the chip circuitry because otherwise power would not flow and the chip would be non-functional or local grids would be left floating. EX1003, ¶179. I disagree that Dr. Subramanian has shown this. Even Dr. Subramanian testified, one can have a direct connection from the top layer to the switch and a local grid is not needed. EX2005, 46:9-51:17. Further, as Li discloses, a local power grid is not present in all locations, only in the "local sections," further confirming a local power grid is not needed everywhere.

256. Because Li teaches grounding in the substrate at the core through a switch, it would discourage a POSITA from using a local power grid to route ground potential to the power domain. Further, any modification to the switching structure to route the ground through a local power mesh would undermine the principal of operation of the switch and render it inoperable. This is because another ground connection would bypass the switch.

(2) Claim 18: Li fails to disclose wherein the first local ground wire and the second local ground wire share the same ground wire of the global power mesh

257. Dr. Subramanian opines that Li alone or in combination meets the elements of claim 18. EX1003, ¶181. I disagree that Dr. Subramanian has shown this. A POSITA would recognize that Li fails to disclose a first local ground wire and a second local ground wire that share the same wire of the global power mesh.

258. First, because claim 16 is not taught or suggested by Li, there is no first local ground wire in the partial local power mesh that couples to the ground wire of the global power mesh, and thus, there is necessarily no “shared ground wire.”

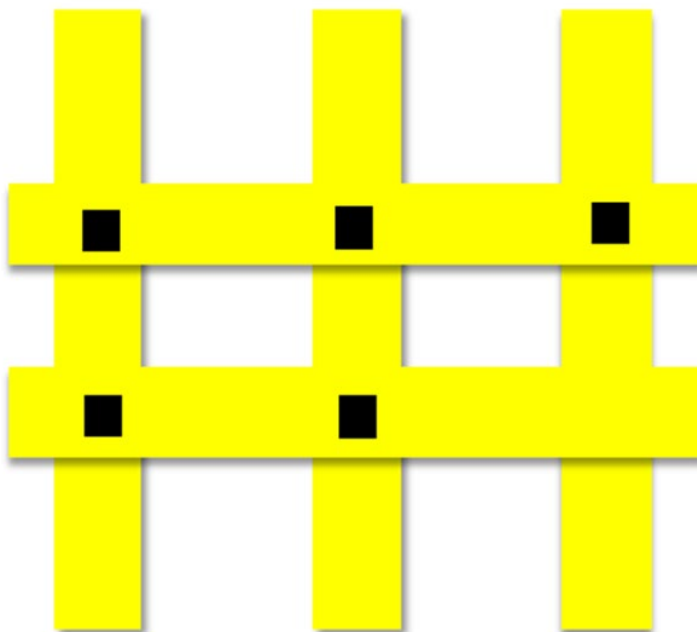
259. Further, a POSITA would recognize that Li does not disclose a single ground wire in the purported global power mesh in metals 6 and 7 that is shared by a first and second local ground wire. Indeed, Li does not identify any connections shown below metal-6. EX1005, Fig. 3 (showing only via 6, which connects metal 6 and metal 7). Dr. Subramanian agrees that Figure 3 does not show connections below metal-6. EX1005, 493-94.

260. Dr. Subramanian asserts that claim 18 is met because “all” ground wires are connected together and “all” “ground wires” are the “same ground wire.” EX1003, ¶181. I disagree with this assertion for several reasons.

261. First, a POSITA would not understand “all” the ground wires to be the “same ground wire.” A POSITA would understand that the “same ground wire”

requires a single wire that is shared by *local* ground wires in the partial local power meshes, not many ground wires that are shared by the ground wires of the *global* power mesh.

262. I have illustrated an example of “all the ground wires” as Dr. Subramanian proposes in the context of Figure 3:



263. As can be seen above, Dr. Subramanian’s construction that all ground wires of the global mesh are the “same ground wire” equates an entire mesh with a single ground wire. This is not how a POSITA would understand the term. The intrinsic record distinguishes between single “wires” and “meshes,” the latter being structures comprising multiple wires. For example, the claims use the terms “wire”

and “mesh” separately and makes clear they are different by claiming that “meshes” comprise “wires.” EX1001, cl. 15 (“The power routing structure according to claim 12, wherein the global power mesh comprises: at least one ground wire; at least one first power wire that provides the power needed by the first power domain; and at least one second power wire that provides the power needed by the second power domain.”).

264. Dr. Subramanian’s “all ground wires” interpretation is also not how a POSITA would understand the term because it requires including “vias” as wires. The intrinsic record distinguishes between vias and wires and indicates that “via” connects wires and is not itself a wire. *See, e.g.*, EX1001, 4:16-18 (“Besides, the power wires and ground wires of adjacent metal layers having the same electrical property can be interconnected to each other by via.”). That is also how a POSITA would understand the term “via.”

265. I also disagree with Dr. Subramanian’s assertion that “all” the ground wires of Li are connected together. EX1003, ¶181. Li does not disclose this. Rather, a POSITA would understand that there are numerous pads arrayed across the die, including several ground pads. EX1005, 493. A POSITA would expect that not all of these individual wires must intersect each other on metal-6 and metal-7. For example, there may be interruptions in the ground grid on those layers such that pathways between wires have to bypass “cutouts” in the grid caused by obstacles.

266. Dr. Subramanian also labels the middle vertical wire in Figure 3 as the “common ground wire.” EX1003, ¶177. A POSITA would not understand this wire to be the “same ground wire” of claim 18 because there are no connections shown to the ground wires below.

267. Dr. Subramanian also finds it relevant that a “ground reference GND” or common potential is sufficient to meet claim 18. EX1003, ¶181. But Dr. Subramanian agreed that a common ground potential does not satisfy the same ground wire limitation but could not think of an example in which a common “ground reference,” i.e., shared ground potential, would not satisfy the same ground wire limitation under his construction. EX2005, 262:17-264:18. This shows his construction is overly broad.

268. Because Dr. Subramanian is incorrect that the “same ground wire” can be “all the ground wires” or a ground mesh, and assumes all wires of the global power mesh are connected together, and constitute a single wire, Dr. Subramanian has not shown obviousness.

269. For all of these reasons, it is my opinion that claims 12-18 are not unpatentable based on the Ground 5 challenge.

D. Ground 5: Claims 1-11 and 19-20 are not obvious over Li in view of Jiang and further in view of Bertolet and/or LPMM

270. Dr. Subramanian provides opinions on Ground 5 in paragraphs 182-87

and concludes that claims 1-11 and 19-20 are obvious. I disagree that Dr. Subramanian has shown this.

271. First, Dr. Subramanian relies on Ground 4 in further view of Bertolet and/or LPMM. EX1003, ¶¶182-83. It is my opinion that Ground 5 fails for the same reasons Ground 4 fails.

272. Dr. Subramanian also relies on the analysis of Ground 3 to support the motivation to combine a primary reference with Bertolet and/or LPMM. EX1003, ¶¶182-83. It is, therefore, my opinion that Ground 5 fails for the same reasons Ground 3 fails.

273. Dr. Subramanian continues to fail to show that all limitations of claims 1-11 and 19-20 were disclosed in the references cited. As I discussed with respect to Ground 3, Dr. Subramanian again misrepresents Bertolet and LPMM and contends that a POSITA would have found it obvious “to form and couple Li’s power meshes” a POSITA was “aware of” the need to use automated tools and “would find it obvious that a similar automated procedure could be used to form Li’s grids.” EX1003, ¶186. I disagree with Dr. Subramanian’s characterizations of the prior art as discussed in Ground 3. Dr. Subramanian has not shown a teaching or suggestion to perform the specific steps of claims 1-11 or 19-20 using an APR tool.

274. Dr. Subramanian asserts that a POSITA would use APR tools to implement the structure of Li. EX1003, ¶¶185-87. I disagree that Dr. Subramanian

has shown this. Dr. Subramanian does not consider that Li's power meshes were formed through design reuse. EX1005, 491-42. Dr. Subramanian provides no motivation to modify this method of power routing to use the claimed APR tools. Dr. Subramanian combines Bertolet, LPMM, and Li, but fails to provide a motivation to combine these specific references. As I discussed with respect to Ground 3, it is my opinion that Li discourages use of additional APR tools because it was based on a design reuse and developed an LVS process to check the layout based on design reuse. A POSITA would, therefore, be encouraged to follow a design reuse method proposed in Li to get to market faster. EX1005, 490-93. Dr. Subramanian also never explains why the existing method in Li, design reuse, would be modified. A POSITA would not be motivated to change Li's existing method without a perceived benefit.

275. For all of these reasons, it is my opinion that claims 1-11 and 19-20 are not unpatentable based on the Ground 5 challenge.

IX. Reservation of Rights

276. I reserve the right to amend or supplement this declaration as this case proceeds and any additional information comes to light.

277. I understand that traditionally no live expert testimony is used at the PTAB, and I presently have no plans to testify; however, should I be asked, I reserve

my right to use exhibits to summarize or exemplify my opinions (including exhibits I have not yet created) if called to testify.

278. If it would be helpful, I am willing and able to provide additional background.

279. I further reserve the right to respond to any opinions presented by any of Petitioner's experts regarding the meaning of any claim term or limitation. I also reserve the right to provide further opinions, if requested to do so.

All of the statements made in this declaration of my own knowledge are true. All statements made based on information and belief are believed to be true. Further, these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code.

IPR2023-00920
U.S. Patent No. 8,006,218

Dated: March 1, 2024

A handwritten signature in blue ink, appearing to read "S.J. Sour", is written over a horizontal line.

Shukri J. Sour, Ph.D.