UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC.,	)	
	)	
Petitioner,	)	
	)	Case IPR2023-00920
-vs-	)	
	)	U.S. Patent No.
REALTEK SEMICONDUCTOR CORPORATION,	)	8,006,218
	)	
Patent Owner.	)	

The videoconference deposition of VIVEK SUBRAMANIAN, Ph.D., taken remotely before JUNE M. STEARNS, CSR, RMR, and Notary Public, pursuant to the applicable rules, commencing at 7:54 a.m. Central Standard Time on February 16, 2024.

REALTEK EXHIBIT 2005
AMD v. Realtek
IPR2023-00920

There were present via videoconference at the taking of this deposition the following counsel:

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NOTE: Exhibits were provided for inclusion with deposition transcripts.

THE REPORTER: Before we proceed, I will ask counsel to agree on the record there is no objection to this Certified Shorthand Reporter administering a binding oath to the witness remotely.

Will all counsel state their agreement on the record, please.

MS. WEISKOPF: I agree.

MR. WILSON: And I agree also.

(Whereupon the witness was duly sworn.)

THE REPORTER: Thank you. Please proceed.

VIVEK SUBRAMANIAN, Ph.D.

witness herein, called for examination, having been first duly sworn via videoconference, was examined and testified as follows:

EXAMINATION

BY MS. WEISKOPF:

Q Good morning for me, Dr. Subramanian, but I think it may be evening for you. Thank you for coming. My name is Elizabeth. We've met before. I'm an attorney at the law firm at K&L Gates, and in this lawsuit I represent Realtek.

You've done this many times before I know. I'm just going to ask you some questions, and if you don't hear the question or you don't understand the question just let me know and I'll try to clarify.

Is that okay?

A Good morning, and, yes, that is fine.

Q Thank you. And you know all the rules. You'll have to verbalize your answers so that we can hear them and they can be transcribed by the court reporter.

Is that okay?

A Yes, that's fine.

Q Is there any reason that you can't give truthful and complete testimony today?

A No, not that I'm aware of.

Q All right. And, of course, if you want to take a break just let me know. It's best to do that while a question is not pending.

Is that okay?

A Yes, that's fine.

Q All right. So just because you're appearing remotely I'm just going to ask you a few kind of preliminary questions so that we're all on

the same page. It doesn't look like it, but is anyone in the room there with you?

A No.

Q And do you have any documents or any papers in front of you?

A No.

Q Okay. Do you have a pen and paper if we need to draw anything accessible?

A Yes, I have -- yes. Yes, I can manage.

Q You'll be able to find something? Okay.

A I will.

Q Thank you. And is the phone, your phone, or, you know, your iPhone or Android accessible or any other way of communicating with people available to you?

A It is, but I'm going to put it in airplane mode right now.

I just did, so, therefore, I no longer have external access.

Q Okay; great. Please don't consult your e-mails or text messages while we're taking the deposition today.

Is that okay?

A That's fine.

Q All right. So just some preliminaries on your deposition prep. Did you do anything to prepare for your testimony today?

A Yes.

Q Did you speak with anyone besides your attorney?

A In relation to preparation, no.

Q Did you review any documents?

A Yes.

Q Which documents did you review?

A I reviewed my declarations that I submitted in this matter. I reviewed some of the exhibits that are associated with this IPR. I reviewed related documents from -- that are related to this patent but from another matter, specifically the matter at the International Trade Commission.

Yes, and I guess that covers it.

Q Okay. Did you do anything else to prepare for your deposition today?

A Yes. I had some meetings with counsel.

Q Okay. And then how much time do you think you spent preparing for the deposition today?

A Oh, several hours.

Q Okay. You mentioned that up reviewed your declaration that was submitted in this IPR; is that right?

A Yes.

Q Is there anything in there that you'd like to change?

A Yes, I believe there is a typo that I found. It was on paragraph one twenty -- let's see where was it. One second. I'll tell you where it was.

Paragraph 129. If you look at the bottom of page 83, there's a missing word. It says "Further supporting a POSITA's reasonable expectation of success is the fact that prior to the '218 patent in," and then there's nothing there and there's a comma, and I think that should be 2006 because that's when the document was dated.

Q Okay. Good. I've made that correction on my version.

Anything else that you'd like to change?

A That's all I'm aware of as of right now.

Q Okay. It seems as if you have your declaration open on your computer, is that right,

you have a version open?

A That's right. I have clean PDFs right now. I have a directory on my computer that has clean PDFs of my declarations and also has all the exhibits associated with this matter, and that's all I have open.

Q Okay.

A I don't have all the exhibits open, but I have a directory in which the exhibits are there.

Q Okay. That's largely what we're going to talk about today so that's great, I'll introduce those, but you should feel free to either download the version that I give you or use your own versions to search or whatever it is you need to do to answer the questions.

Is that okay?

A Yes, that's fine. Thank you.

Q Okay. All right. Well, let's start by talking about the '218 patent. I'm going to try to introduce this, and I apologize ahead of time. I usually have some help doing this so today I'm going to try to do it myself, and I apologize if this is a little bit slow to start with.

I apologize. We may have to get off

the record for me to get some help on how to introduce this. I've moved it to the Marked Exhibits folder, but it's not allowing me to stamp it or anything.

Are you able to see it, Dr. Subramanian, in the Marked Exhibits folder?

A One second. I haven't actually opened that folder. Let me check.

MR. WILSON: What is it you're trying to put in there? I see Exhibit 1003.

MS. WEISKOPF: Oh, yeah. Well, that's not even the right one, but I'm going to do that one next.

MR. WILSON: Okay.

MS. WEISKOPF: Let's try to get 1001.

MR. WILSON: Yeah, 1001 is there now.

MS. WEISKOPF: Okay; good. That's the one I want to use.

THE WITNESS: For me it's telling me I don't have permission to access any folder, but it's okay. I mean, I don't need the folders. If you're using all the exhibits that are already available in this matter I have them all locally, so it's up to you.

MR. WILSON: Did you try the view only option?

THE WITNESS: No.

MR. WILSON: Try that option.

BY MS. WEISKOPF:

Q Seems as though I need to introduce it, and that's what I think the problem here is is that I don't know how to do that right now. So --

A With the view only option -- I apologize, I didn't mean to speak over you, but with the view only option I am able to see the folders. I am able to see the documents.

MR. WILSON: Okay.

MS. WEISKOPF: Do you mind if we go off the record for one second while I speak with June and see if we can figure out how to do this? I'm really sorry about that.

MR. WILSON: Yeah, no problem.

(Whereupon a discussion was held outside the record.)

(Document was marked Exhibit 1001 for identification.)

MS. WEISKOPF: Can we go back on the record, please, June?

THE REPORTER: Yes.
MS. WEISKOPF: Okay; great.
BY MS. WEISKOPF:
Q All right. So, Dr. Subramanian, you can see the AMD Exhibit 1001 which I'm introducing as Exhibit 1; is that right?
A Yes.
Q And you've seen this document before?
A I have.
Q Okay; great. Let's just move to column 1. So if I move the document are you able to see it, Dr. Subramanian, or do you have to move it yourself?
A Oh, I have to move it myself.
Q Okay.
MR. WILSON: You could probably share if you wanted to.
MS. WEISKOPF: Oh, like screen share it?
MR. WILSON: Yeah.
BY MS. WEISKOPF:
Q That's probably right. Let's try it this way since we both have a copy of it and then I will screen share if I need to, or I think I have too many things open to make that a good option right

now. I'll close a few things.

Okay. Could you please just look at column 1, line 8, and confirm for me that this patent relates to a power mesh arrangement in an integrated circuit having multiple power domains; is that right?

A Column 8 of the -- sorry, column 1 of the '218 patent around line 8 it says "The invention relates to a power mesh arrangement method, particular to an power mesh arrangement method applied in an integrated circuit having multiple power domains."

Q Okay. So do you agree that this relates to an integrated circuit having multiple power domains, this patent?

A Yes I agree.

Q Okay. And for the term "power domain" in the context of the '218 patent, do you agree that a power domain is a portion of the integrated circuit that has a different power requirement from the power requirements of another portion of the integrated circuit?

A Could you repeat what -- the definition that you provided, please?

MS. WEISKOPF: Yes. Ms. Court Reporter, are you able to read that back? I don't have the real-time.

(Whereupon the question was read by the reporter as follows: "Question: Okay. And for the term 'power domain' in the context of the '218 patent, do you agree that a power domain is a portion of the integrated circuit that has a different power requirement from the power requirements of another portion of the integrated circuit?")

THE WITNESS: Yes, that could certainly be an applicable way of interpreting that language for a power domain.

BY MS. WEISKOPF:

Q Is that the meaning of power domain that you applied in your declaration?

A Yes, in that it's consistent with what I would view as the plain meaning or at least it's one way of describing what falls within the plain

meaning of the term, that would fall within the analysis that I provided because I use plain meaning in my analysis.

Q Okay. And you agree that the plain meaning of a power domain is a portion of the integrated circuit that has a different power requirement from the power requirements of another portion of the integrated circuit?

MR. WILSON: Objection; form.

THE WITNESS: That falls within the scope of what would be the plain meaning. In other words, I believe that a POSITA looking at the term "power domain" would say that were there a portion of an integrated circuit that had a different power requirement than other portions of said integrated circuits they would, for example, constitute two separate power domains.

BY MS. WEISKOPF:

Q Okay. You said it falls within the scope, which suggests you think the plain and ordinary meaning is a little bit broader; is that right?

A No, it's actually the reason I use falls within the scope is that's one way to describe it

but it's not the only way to describe it.

Q Okay. What are the other ways to describe it?

A For example, if you define power domain and you were more specific and you said, for example, that they have different voltage requirements, it's true it would result in different power requirements, but that's another way of saying a specific case of two separate power domains.

Q Okay. So when you said "falls within the scope" you meant that there are more examples but not that it was broader in meaning; is that right?

A I'm not sure I understand what you mean by that.

Q Well, I just want to make sure that you don't have another plain and ordinary meaning of the term power domain that we haven't talked about, so I'm just trying to understand that.

MR. WILSON: Objection; form.

BY MS. WEISKOPF:

Q So do you have a different view of what power domain is other than what we just discussed?

A If by that you mean am I -- do I have a

view that something that has a different power requirement than another part of the circuit could fall within the same power domain, I think the answer is no. So I think as one way to characterize how one of skill would view a power domain that is certainly reasonable as a representation of the plain and ordinary meaning.

Q In practice different circuitry is provided with different powers depending on the needs of that circuitry; is that right?

A It could be. That's not necessarily true, but, yes, that is certainly possible.

Q Why do you say that's not necessarily true?

A Because it could be that they're provided with the same power because they don't need different powers or it could be that they're provided with the same power even though their power needs are different just because it simplifies the circuit architecture to provide them with the same power.

Q What are the advantages of simplifying the circuit architecture?

A Well, for example, if you don't care

about power consumption, putting aside the requirements of the patent or putting aside anything to do with the patent, if you have a hypothetical circuit where you were not constrained by the power consumption of a particular circuit or a subcircuit within said circuit and let's say that circuit could operate at, for example, a much lower voltage, you may choose not to operate it at that much lower voltage just so that you don't have to have the power supply circuitry to generate that much lower voltage.

Q Okay. Is it of benefit to avoid having additional power supply circuitry?

A It could be, yes, in some situations, yes. Additional circuitry takes more space.

Q Okay. It's space constrained in an integrated circuit; is that right?

A That's certainly one of the constraints. There's always trade-offs, but, yes, one of the things that you trade off in any circuit design is how much space the design takes. But we always make these trade-offs. It's the nature of basic engineering.

Q Okay. In practice different circuitry

may not need any power at all also; is that right?

A I'm not sure I understand what you mean by that.

Q Sure. A portion of the integrated circuit may be idle, for example, and may not need any power; is that right?

A Yeah, I think I understand. Okay. So you mean -- you're not saying all the time, you're saying there could be periods of time where a particular part of a circuit may not have a nonnegligible power event, and if that's what you're saying the answer is yes. There are times where we essentially drive a circuit to a deep sleep state and in that deep sleep state other than leakage power, which is not zero, it's small, other than leakage power there's not appreciable power consumption.

Q Okay. And power-gating is a technique to turn off power to a portion of the circuit that's not being used; is that right?

A It could be. It doesn't have to be.

Q How would you describe power-gating?

A Well, power-gating can do various things. So you can use power-gating to turn off the supply

of any appreciable power beyond leakage power to a particular circuit block, but you can also use power-gating, for example, to adjust the power that's delivered.

There is multiple ways to use power-gating, but it is true that one of the ways you can use power-gating is to largely turn off the power provided to a particular circuit block other than leakage power.

Q Okay. Do you mind just turning to claim 12 in the Exhibit 1001?

A I have it in front of me.

Q Okay. The claims here recite a first power domain and a second power domain.

Do you see that?

A Yes.

Q Okay. Do you agree that the first power domain and the second power domain have different power requirements?

A With respect to each other, if we -- if we see that the first power domain is called out as a different power domain than the second power domain, and that is true in claim 12 because claim 12 starts out by saying that there's a first power

domain and separately calls out a second power domain, and indeed in the preamble it calls out having multiple power domains, given that I agreed earlier that one way to classify what falls within the scope of the plain meaning of a power domain is that it has a different power requirement from other parts of the circuit that would be in other power domains it would follow that the power requirements of the first power domain could be different, and indeed may be different, than the power requirements of the second power domain.

Q Do you agree that the claim requires the power requirements of each power domain to be different?

MR. WILSON: Objection; form.

THE WITNESS: No, the claim states what it says. The claim says that there's a first power domain and then there's a second power domain. As we discussed previously and as I told you in a previous answer, within the scope of what one of skill would consider to be a power domain is indeed the possibility that the power requirements of circuitry within the first domain are different from the power requirements of the circuitry of

said second domain.

So to the extent that we have a first power domain and a second power domain, within what would constitute the plain meaning of said power domains it would follow then that the power requirements of the first domain could be different from that of the second domain.

BY MS. WEISKOPF:

Q Okay. Can the power requirements of the first domain be the same as the power requirements for the second power domain?

MR. WILSON: Objection; form.

THE WITNESS: At certain points in time, sure.

BY MS. WEISKOPF:

Q Can the power requirements of the first power domain be the same as the requirements of the second power domain at all times?

MR. WILSON: Objection; form.

THE WITNESS: I don't think I have enough information to answer that. Am I to assume they're on the same integrated circuit and are contiguous or could they be completely separated from each other?

BY MS. WEISKOPF:

Q Well, I'm just asking in the context of claim 12. So claim 12, however you interpret it, are the power requirements of the first power domain and the power requirements of the second power domain the same at all times?

A They certainly don't have to be, but you can have power domains that happen to coincidentally require the same voltages and the same currents, and maybe even the same duty cycles in terms of when they are on, but they may still be separate power domains because they're entirely separated from each other; so, therefore, they still have different power requirements in terms of the spatial delivery of said power.

Q Okay. Is there anything in the '218 patent that you're basing that opinion on?

MR. WILSON: Objection; form.

THE WITNESS: The specific example that is given in the '218 patent, for example, if we look at the exemplar that's provided starting at the bottom of column 2 and continuing into column 3, that example specifically has different powers that supply different voltages. So that one

certainly wouldn't fall -- that would not fall within the scope of a situation where you coincidentally have the same voltage requirements.

The -- I believe all the examples that are given specifically say -- follow that or if we look at column 1 at line 35 it says -- sorry, not line 35. I apologize. Line 28 it says "Hence, it is common practices to arrange multiple power domains in the chip circuitry. In other words, circuits in different power domains are coupled to different powers respectively so that the circuits of different power domains use different powers to support the different operations that are just mentioned."

So I think in the examples that it gives there it calls them out as different domains and it says they have different powers. The time it provides more specificity on the different powers is when it provides different voltages.

BY MS. WEISKOPF:

Q Okay. So how does that support your opinion that the first and second power domains can have the same power requirements at all times?

MR. WILSON: Objection; form.

THE WITNESS: Just to be clear, that's not what I said.

BY MS. WEISKOPF:

Q Okay.

A I said you could have a situation where you have different power domains that coincidentally have the same voltage requirements and the same current requirements and even the same duty cycle but they are still powered separately because they are geometrically spaced such that they must be powered separately.

So they still have different powers just based on the fact that they are geometrically separated and are powered separately. It's still the case that we are talking about having different powers.

Q I understand, I think. Let me clarify or ask a clarifying question. You're saying that they can have the same power requirements in the sense of having the same nominal voltages; is that right?

MR. WILSON: Objection; form.

THE WITNESS: Yes, that is one statement that I made as part of a larger statement.

BY MS. WEISKOPF:

Q But even if they have the same nominal voltages, in your opinion they would be powered separately with different power supplies; is that right?

MR. WILSON: Objection; form.

THE WITNESS: They could be. That's not necessarily true, but it is true that you could have two circuit blocks that happen to run at the same voltage but they may be powered separately. That's certainly true.

BY MS. WEISKOPF:

Q Okay. If you have two circuit blocks that are powered together and have the same power requirements at all points in time, does that satisfy the first and second power domains within the scope of claim 12?

MR. WILSON: Objection; form.

THE WITNESS: I think I understand. I think when you said "powered together" you mean they're driven by the same power supply, and if I assume that's what you meant, in other words, by powered together in your question you meant they are driven by the same power supply and they just

happen to be two different circuit blocks, those would be the same power domain because they are driven by the same power supply. So by the nature of that they are the same power domain.

BY MS. WEISKOPF:

Q Okay. Can you clarify what you mean by "power supply" in that example?

A Yes. So in my example what I meant is so if we have a circuit block that has arbitrarily a wire running into it that provides it to power and then we have another circuit block that has a wire running into it that provides it power and those two wires are tied to each other so that at all times they are driven by the same power supply above said wire, those would be one power domain because they necessarily in the physics of how these operate will always receive the same supplies because it's the same path.

Q Okay. Sometimes chips have a power supply that enters the chip through an I/O pin; is that right?

A In fact, that's almost always true. Yes, I agree.

Q Okay. Is that what you're referring to

as power supply?

A No, I was not.

Q Okay. Sometimes chips have power pads or bumps on them. Is that what you're referring to as power supply?

A No. I was using a much more granular view. Everything I said was within the chip.

Q Everything is within the chip, okay.

A Actually, I apologize, within my previous discussion that wire that I was referring to was within the chip.

Q Okay. I don't understand because usually the power pads and bumps are within the chip also, aren't they?

A The power pads and bumps are on the edge of the chip so to that extent they are within the confines of the chip, but I was even more granular. I was inside the chip in my hypothetical that I gave you a few minutes ago.

Q Okay. I'm not trying to be difficult. I really just want to understand. You're talking about like the specific wiring structure, so if you're looking granularly at the chip and you're looking at how the wires are connected that's how

you're determining whether or not they're coming from the same power supply; is that right?

A In the specific context that I gave you, yes, because that's how I defined it. In other words, in my previous answer what I said is we have one circuit block and power for that circuit block comes from some internal wire of the chip, and then I have another circuit block and power for that comes from some other internal wire of the chip, and those two wires are directly connected to each other so that the power that is provided to those two circuit blocks is the same. It's the same path.

Then in that situation those would be one power domain because there is simply no way for them to be driven other than with exactly the same supply because they are essentially two subcircuits within a singular power domain.

Q Would the same be true if you're looking at a power supply that's outside the chip that drives both circuit blocks?

A It -- I need more context to answer, but I can certainly envision a situation where that would be true. In other words, if I have a chip

and it has two or more circuit blocks but the circuit blocks are wired together such that they always have the same power delivery, in fact, they could be contiguous to each other, in that situation that entire circuit or at least the circuit blocks I was referring to in the previous part of my answer would be within the same power domain. It may just be that that particular integrated circuit happens to have a singular power domain.

Q Okay. So if power entered the chip, went to one circuit block and then was connected at a lower level by, for example, a power rail to another circuit block, that would all be one power domain; is that right?

MR. WILSON: Objection; form.

THE WITNESS: I don't have enough information to answer. Is that the only way power is provided to both of those circuit blocks or could there be multiple power rails running to said circuit blocks?

BY MS. WEISKOPF:

Q Let's just assume one for now.

A Okay.

MR. WILSON: Objection; form.
THE WITNESS: Okay. I think I understand. So if I have an external power supply that provides power to an integrated circuit inside a package, within that package there's some internal wire that provides power to circuit block -- let's call it circuit block A, and then there's a wire in the hierarchy that runs from circuit block A to circuit block B and that wire is essentially a continuation of the power supply line such that the power supply that was provided to circuit block A is also provided to circuit block B and the power requirements, therefore, of circuit block A and B are the same and indeed they are the same power domain, they're just subcircuits within a singular power domain, then it would follow that that is a singular power domain.
BY MS. WEISKOPF:
Q Okay. So based on our conversation here, power requirements are measured over time; is that right?
MR. WILSON: Objection; form.
THE WITNESS: So power is actually an instantaneous measure so I don't think that's what

you meant, but I think what you're asking me is when you are describing the power requirements for a circuit it may be that instantaneously they are the same but if they vary with time differently you still describe the power requirements differently and then the answer would be yes.

BY MS. WEISKOPF:

Q Okay. Let's turn to column 1, line 12. This is example you referred to -- are you there at this example?

A I am.

Q Okay. Here the patent is explaining that the chip circuitry may operate at a normal mode and at a sleep mode, so in the normal mode the entire chip is receiving the same nominal voltage, is that right, in this example?

A Yes, I agree.

Q Okay. But there's another point in time when a portion of the chip will go into a sleeping mode and receive a lower power; is that right?

A Actually, the language here says lower voltage, but other than that your statement was correct.

Q Okay. Do you agree this is an example

disclosing an integrated circuit with two different power domains?

MR. WILSON: Objection; form.

THE WITNESS: Putting aside any other requirements in that it looks like at least in this description there are periods in time where part of the chip will run at different powers than other parts of the chip, it would be true that those two would constitute two different power domains.

BY MS. WEISKOPF:

Q Okay. Let's go to claim 12 and talk about another term, global power mesh. Please let me know when you're at claim 12.

A I'm there.

Q Okay. Do you agree that a global power mesh is a power mesh capable of distributing power to multiple power domains?

A In the context of claim 12 where we see that that's how -- that's the relationship between the various claim elements, it's true that in that situation for a system such as that of claim 12 a global power mesh would be capable of distributing power to I think you said multiple power domains, and that's what the claim says.

Q Okay. Is this the construction of global power mesh that you applied in your declaration?

A So I applied the plain meaning. It's certainly true that that falls within the scope of it. In other words, there are other requirements imposed on the claims and the fact that there are multiple power meshes is described within the claims themselves, so to that extent that's consistent with the claims.

Q It sounded like you said there's other requirements for the global power mesh; is that right?

A Yes. For example, in claim 12 there's other limitations that impose requirements on the positioning of the global power mesh.

Q Okay. What other requirements are there for the global power mesh?

A Well, so if we look at claim 12, claim 12 tells us various requirements in the global power mesh. It says, firstly, that the global power mesh is coupled to the first local power mesh and the second local power mesh, so that's a requirement.

It also says that it uses it to provide the power needed by the first power domain

and the second power domain separately. So that's another requirement.

And then it goes on to say in the next limitation the global power mesh and the first local power mesh are positioned on different metal layers, so that's another requirement of claim 12.

And then it goes on to say that the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer.

So in the scope of claim 12 those are the requirements that are imposed on a global power mesh.

Q Okay. Are there any other requirements?

A Yes. I apologize. There is one more. It did go on to say, the very last limitation, that the first metal layer and the second metal layer are different layers, so that is another requirement since that is related to the global power mesh. And this is specific to claim 12.

Q Okay. Anything else for claim 12?

A I don't believe so. I think I read every requirement that is imposed on the global power

mesh by claim 12.

Q Okay. Do you agree that a power mesh is a network of intersecting wires capable of distributing power?

A Yes, I agree that's a reasonable characterization of the requirement -- of at least some of the requirements of being a power mesh, putting aside the other requirements imposed by the claim.

Q Is that the construction that you applied in your declaration?

A So I actually looked -- I understand that there's multiple constructions that have been proposed. I use the plain meaning. It's certainly true that the art that I cited would certainly invalidate under that construction. So that is one of the constructions that I considered, but it would even be true for a narrower construction.

So, for example, if we imposed a requirement of parallelism of the wires it would still be true that the art would invalidate.

Q Okay. Can you tell me what the plain meaning of that phrase is, "power mesh"?

A Could you repeat the question, please?

Q Sure. What is the plain meaning of the term "power mesh"?

A So I believe it's at a minimum true that a power mesh would require intersections. I understand that AMD contends that power mesh means two sets of parallel conductive wires that form a net or weblike structure.

So it is certainly true that at a minimum you must have the intersections. I believe it's correct that there should be a weblike structure. However, the art would invalidate under either view; in other words, whether you require the weblike structure or you merely just require intersections.

Q Okay. Anything else with respect to the plain meaning of power mesh you'd like to add?

A I think I've covered the various analyses that I provided within my report and that have been offered by the parties.

Q Okay. Let's turn to column 3, line 25. And let me know when you're there, please.

A I'm there.

Q Okay. So we sort of touched on this before, but it says here "The global power mesh

couples to the external power, such as by way of an I/O pin of the chip, to conduct the external power into the chip."

Do you agree with that statement?

A I don't know -- I don't know -- I mean, the statement is what it is. I believe you read it correctly. I don't know what you're asking me beyond that.

Q Okay. So there's typically an I/O pin that conducts external power into a chip; is that right?

A Yes, in any chip of this kind that's true. I mean, theoretically you can have chips that generate their power by energy harvesting internally, but these chips certainly the power is conducted through an I/O pin. I agree.

Q Okay. And so you would have an I/O pin for each power and for a ground, one or more grounds, is that right, is that how a chip would work?

MR. WILSON: Objection; form.

THE WITNESS: It depends on the chip. So, in other words, there are chips that have multiple -- for example, multiple voltage

requirements but only have one voltage I/O pin and one ground I/O pin and then internal to the chip they have a voltage regulator that is used to generate any other voltages that are required.

There are also chips where for each voltage required by the chip there's a separate I/O pin. In other words, there may not be any internal voltage generation.

BY MS. WEISKOPF:

Q Okay. And if there's multiple ground potentials provided you could have multiple I/O pins or would you -- is that correct?

A I'm sorry. I think you said ground potentials.

Q Yes, for ground potentials. How do you get ground into a chip?

A Oh. I understand. Okay. So the -- integrated circuits are put inside packages. The packages are almost always insulating, and it's really important to have a good ground.

The way we get ground to chips, this is the standard way that's pretty much used in almost -- in fact, it's used in every chip of this kind that I'm aware of, and it's pretty much the

easiest way to do it, is you have one or more ground pins that are used to provide ground because that is the access you have to the chip. The chip is in an insulating package. The only way to bring ground in is through the I/O pins.

Now you can have a singular ground pin or you can have multiple, but because they're ground they are coincidentally and nominally the same potential. It's just a way of providing a good quality ground. It's important to have low resistance, which is why, firstly, we get the metallization to get the grounds in.

Q Okay. If you have multiple ground pins what would the purpose of that be?

MR. WILSON: Objection; form.

THE WITNESS: Actually, I just answered that, but I'll answer it again.

So we use -- so it depends on the application, but in a lot of circuits, in fact, most circuits, it's important to have a robust ground connection. The reason is every voltage is referenced relative to ground. And even though the ground -- the different ground pins that we just discussed in my previous answer and in your most

recent question are nominally at the same potential, it's important that it maintains that potential even when the circuit is operating and, therefore, current is flowing to ground.

So in that situation it's important that we have a low-resistance path to ground. By having multiple ground I/Os you're essentially providing parallel conduction paths which lowers the resistance of the overall chip to ground, and that's beneficial for maintaining a robust ground potential.

BY MS. WEISKOPF:

Q Can you please explain what you mean by "a low-resistance path"?

A Sure. So in these circuits current flows -- electrical current flows through the circuit. The energy for that current starts from the positive supply, if we define it in terms of conventional current, and flows through the circuit to ground to do whatever work the circuit wants to do.

Because there is current flowing to the ground point, any time current flows through a conductor there's a small resistance of that

conductor, and if there's appreciable concurrent flow the voltage drop across that conductor can be nonnegligible. In that situation it's important to minimize the resistance so that you don't artificially raise the ground level in a way that makes the circuit operation unstable.

And that's why it's desirable to have a low-resistance path, and this is why grounds always use I/O pins. Even when you make a connection to the substrate, the substrate is connected to the I/O pin and the I/O pin provides the path to ground because everything else is in an insulating box typically and the best path, the most efficient path, for getting current in and out of a circuit is through the I/O pins, and that's true for grounds and that's true for voltage supplies.

Q How do you minimize the resistance path inside the chip?

A Are we talking specifically about ground now?

Q We can start with ground. I'd like to know the answer for both. How do you minimize the resistance path inside the chip for ground?

A Okay. So for ground the most efficient way and, in fact, pretty much the standard way, the most well-known way, to minimize the resistance is to use a network of connections such that you provide easy access to the ground wherever it's needed over the dimensionality of the chip. So what that means is, for example, you have good access to ground from the bottom left of the chip and you have good access to ground from the top right of the chip.

To ensure that you have low resistance you try to run the ground in low-resistance metal wiring. The way these chips are built, the way that's done is you have thick wires in the upper parts of the chip that provide low resistance, and then what you do is you typically have a distribution network that ensures that the ground is provided wherever you need it without having long, circuitous paths to get to the ground.

My answer would have been the same with respect to power except every time I said ground I would have replaced the word by power for the positive power supply.

Q Okay. How do you avoid long, circuitous

paths inside of a chip?

A It's done through the routing of the wiring. So what you would do is you would make sure that you make the lines as well -- as directly connected as possible and you provide -- you provide drops starting from the top of the chip down to the substrate that ideally, given the routing constraints, are as direct as possible.

It's standard technique. This is well-known.

Q Okay. What do you mean by "drops"?

A In an integrated circuit, and that's certainly true for the integrated circuits that are described in the '218 patent, there are multiple layers of metal. So when you bring in a signal from the top, whether it's power or ground or even a digital logic signal, it comes in at the top of the chip at the highest metal layer and then you have to bring it down to the active circuitry which is built in the silicon underneath.

So drops was referring to getting it from the top layer of metal down to the active circuitry underneath in my previous answer.

Q Okay. Let me see if I understand. We've

talked about there being different pads or bumps on the top layer and -- is that right?

A If we define the top layer as the layer on which the pads or bumps are, yes, that's true.

Q Okay. The power comes in through those pads or bumps; is that right?

A In my previous answer and in your previous question, yes, that's how we defined it.

Q And the ground also comes in through those bumps?

A Yes, with respect to my previous answer and with respect to your previous question, that's true.

Q Okay. So by drops you're talking about the wiring structure from each one of those pads or bumps?

A No. Drops was more specific.

Q Okay.

A When I use the word "drops" I was referring to the vertical connections that are used as a series of vias, et cetera, to bring us from the top level of metal down to the active circuitry at the level of the silicon wafer.

Q So to minimize the resistance you would

have a direct vertical connection from the pad top layer down to the circuitry; is that right?

A No. That's almost never true. You could, that is a way to get a very low resistance, but sometimes routing constraints prevent you from doing that or process rules prevent you from doing that. But the key is you try to make it as direct as you can.

Q I see. So for either the power or the ground bumps on the top you try to make it as direct as possible of a path to the circuitry below in order to minimize resistance; is that right?

A For any given circuit given the routing constraints, yes, if you want to minimize resistance the best way to do it is to provide the most direct path you can. It's not -- it's relatively straightforward, but there are constraints imposed on it so it requires some trade-offs.

Q Okay. And you could drop vias directly from a pad or bump all the way down to the circuitry; is that right?

A That's one way to do it. That may not be possible due to other constraints but it is

certainly possible to do that, and I am aware of some circuits where that is done, as in real commercial parts where that is done, but that's not always the case. Sometimes constraints prevent you from doing that.

Q Okay. But you could do that direct connection from the top to the circuitry below for both power and ground; is that right?

A If other constraints don't prevent you from doing it, yes, that's true. Conceptually you could have a chip where you have a series of vias that run from the pad level down to the active level for both power and ground. That's conceptually possible.

Q So the I/O pin, back to that, the I/O pin, is there a connection between the I/O pin and each pad or bump?

A I'm sorry. I don't understand that question at all.

Q Okay. Let me make it a broader question then. The power is coming into the chip through the I/O pin; is that right?

A Through a particular I/O pin.

Q Yeah, okay, through a particular I/O pin.

So the power and the ground are each coming into the chip through a particular power or ground I/O pin; is that right?

A I understand your hypothetical so far, yes.

Q Okay. How does the power from the I/O pin get to each power pad or bump?

A Ah. I understand. So it depends on the chip. The -- the I/O pin is on the package of the chip, and the package is insulating and the I/O pins provide a conductive path into the chip. Depending on the chip, the bump can be directly connected to the I/O pin via, for example, a flip chip connection or it could use a redistribution layer, which is sort of an intermediate circuit element that makes the connection, or it could use wire bonding.

There's multiple ways this is done. There's multiple ways. It's industry standard, but there are multiple ways of doing it and they still exist today.

Q Okay. Is the purpose of a bump to make the direct connection with the I/O pin?

A In some assembly techniques, yes. In

others, no. It depends.

Q Okay. What is the bump used for if it's not used for making a connection with the I/O pin?

A Just to be clear, you said a direct connection. So in an assembly technique where there's a redistribution layer the bump makes a connection from the chip to the redistribution layer and then the redistribution layer has a connection to the I/O pin.

Q Okay. If there's a redistribution layer is there only one bump?

A I don't understand.

Q Okay. I'm sorry. I'm trying to understand what you're saying, so my apologies.

You've made a distinction between some chips having bumps that make a direct connection to an I/O, and then there's a distinction that you made with chips that have a redistribution layer. I'm trying to understand how those are different if they all have multiple bumps.

A Okay. So in the first example that I gave you, that may be a chip scale package where you have flip-chipped the chip such that its bump is in so-called direct connection to the I/O pin

that feeds to the exterior of the package. That is the first example.

In the second example that I gave where I identified a redistribution layer, in that situation the chip might be flip-chipped to form a connection from the bump to a pad on the redistribution layer substrate. Then the redistribution substrate runs laterally and then from another pad in the redistribution layer substrate a connection is made to the package I/O pin. That could be done by a bump, so that's a second bump but it's not a bump on the chip, it's a bump on the redistribution layer substrate.

That's the most common way of doing it. In theory you could also do it by wire bonding, though I don't believe wire-bonded redistribution layers are very common anymore because it's just more complexity than is needed.

Q Okay. That was very helpful.

So when you have a redistribution layer you may have many bumps for power that are then connected indirectly to the pin through a redistribution substrate, is that right; is that what you're saying?

MR. WILSON: Objection; form.

THE WITNESS: Actually, in my answer I only mentioned one bump. It's for any arbitrary signal, be it power, ground, or a logic signal, for example. In the chain that I mentioned there's a bump from the chip that made the connection to a pad on the redistribution layer, the redistribution layer then ran laterally, and then there was a connection, for example, another bump, between the redistribution layer metallization and the I/O pin on the package.

And that answer or that description would be true for a situation where we are talking about a power line, that answer would also be true if we were talking about ground, and that answer would also be true if we were talking about a digital signal, for example.

BY MS. WEISKOPF:

Q Okay. I think I need to just go through this sort of more stepwise to make sure I understand. So for a chip with a redistribution layer you have a bump that makes contact with the I/O pin; is that right?

A On the redistribution layer in the case

where it's a flip chip redistribution layer assembly, the answer is yes.

Q Okay. Let's assume that that bump is a ground bump. Would the redistribution layer have a second ground bump?

A You mean to make a connection to a second I/O pin?

Q Just -- I'm not necessarily saying that. Just any second bump.

A I don't know. It depends on -- if you have a redistribution layer that has multiple redistribution traces to connect to multiple ground I/O pins then there could be multiple bumps, but that's not necessarily the case. You could also just have a redistribution layer that is making a connection to a singular ground I/O pin on the package.

Q Okay. If there's a singular I/O pin, would you expect there to be one bump or many bumps on the redistribution layer?

A You mean for ground?

Q Sure, for ground.

MR. WILSON: Objection; form.

THE WITNESS: No, you -- I mean, you sort

of constrained the problem for me already. You've told me that in that example there's only a single ground I/O pin, so to that extent you would just -- in that situation you would just need one bump to connect to said I/O pin.

BY MS. WEISKOPF:

Q Okay. Would there be other power pads or ground pads in that situation?

A Well, with respect to ground pads you told me in the start of your question that there was just one ground I/O pin, so on the redistribution layer, therefore, there would only be one ground pad based on the constraints you imposed on the hypothetical.

Having said that, at least with respect to power I would expect that there will be somewhere else a power I/O pin and so, therefore, there will be a bump that corresponds to said power I/O pin.

Q Okay. If you only have one bump does that cause an issue for this resistance we were talking about?

MR. WILSON: Objection; form.

THE WITNESS: No, not necessarily. It

depends on the size of the bump and it depends on the routing.

It is routine to make chips with a single -- with a single ground I/O. There's plenty of chips that have been made over the history of the semiconductor industry where that's true. There are also chips where we have multiple ground I/O pins. Both exist.

BY MS. WEISKOPF:

Q How do you minimize the -- how do you minimize the resistance when you have only one bump?

MR. WILSON: Objection; form.

THE WITNESS: I'm going to assume for the purposes of your question that you're asking me about the ground connection because that's what the previous question was. So in that situation what you do is, firstly, you make sure you're using as direct a path as you can given the constraints of routing and the fabrication process, and you make sure that the bump is a lower resistance metal, which it typically is, and you make sure the long wires are built in thick and connect, which they usually are, and that will then minimize in that

situation the resistance of that ground connection.
BY MS. WEISKOPF:
Q Okay. Can ground enter a chip through a layer that's not the top layer?
MR. WILSON: Objection; form.
THE WITNESS: I need more. Am I to assume this is sort of a standard silicon chip such as one of skill in the art would know or is it some special case?
BY MS. WEISKOPF:
Q It's not constrained in any way, just what is available at the time of the, you know, 2007 could ground enter a chip through a layer that's not the top layer?
A I understand. So the standard way of doing it, this is true for the -- if not every single chip that's made in the real world it's certainly the vast majority of them, the only I/O access is through the top layer of metallization. We do not form I/O connections to the external world through lower layers of metallization or through the substrate. The substrate is sitting in an insulating package, so the way we get in and out of the package is through the I/O pins which are

connected to the top layer of metallization.

That's pretty much the standard way of doing it, it's the most efficient way of doing it, and it's certainly true that it's the way it's done in the vast overwhelming majority of integrated circuits that are made and have been made not just since the time of the patent but even predating the patent.

Q Okay. What are some -- are there other ways of doing it that's not the standard way?

MR. WILSON: Objection; form.

THE WITNESS: What I told you was the way it's done. I said -- maybe you're imagining something else, but I haven't thought about that because everybody pretty much does it this way. This is the most obvious and straightforward and efficient way to do it.

BY MS. WEISKOPF:

Q Okay. So you're not aware of any chip where the ground enters in a manner that's not the top layer?

A With respect to the interconnect stack, no, because we almost always -- I mean, in theory I guess you could imagine a situation where you

choose to make a chip some other way, but I don't imagine you would want to do that because it's a less efficient way of doing things.

That's -- the most efficient way is to use the top layer because that's where you can make easy access to the bumps.

Q Okay. So you're not aware of any chip that does it but you can think of a chip that might do it, bring ground or power in through a layer that's not the top layer?

MR. WILSON: Objection; form.

THE WITNESS: Again, what I said was I'm not aware -- it is certainly true I am not aware of any chip that does it any other way other than through the top layer. That is certainly the most efficient way of doing it.

I don't know whether someone has made a chip that is -- uses something else. I will say I don't know why they would do it that way. It's certainly not the most efficient way to do it. The most efficient way is through the top layer. It provides a low-resistance path, it's where the bumps are, it's standard practice, and the overwhelming majority of chips are made that way.

So if you asked someone of skill in the art how they would want to do it that's how they would do it, through the top layer.

BY MS. WEISKOPF:

Q Okay. Can there be grounding through the substrate?

MR. WILSON: Objection; form.

THE WITNESS: I need more information. Do you mean is the substrate grounded or does the substrate provide a ground path to the external world?

BY MS. WEISKOPF:

Q Is the substrate grounded first.

A Okay. So, in fact, it is common practice to ground the substrate, but, to be clear, that substrate ground is also provided through the interconnect stack through the top layer. So all we do is we have a connection that ultimately makes a well contact, but it's still coming through the interconnect stack through the top layer.

The substrate itself is built -- is put inside the package, and the package is almost always a polymer package which is insulating. So you do not get access to the substrate through an

insulating package. The only access in and out is through the interconnect stack.

Q Let's go to column 4, line 31. So here this is talking about the global mesh which is used to supply voltage to the entire chip and then there's a common ground wire 403 used to supply the ground potential VGND needed by the local power meshes 310 and 320.

Do you see that?

A I do see that.

Q What does VGND stand for here?

A Here this stands for V ground, which is the ground potential.

Q Is that a common ground potential?

A In that the upper part of the sentence says one common ground wire to supply the ground potential, yes, in that context this is a common ground potential. In other words, it's providing the ground for both of the local power meshes 310 and 320, which will then ultimately provide the power to the circuit.

Q Okay. POSA would understand or person of ordinary skill in the art would understand that for power to be provided there must be both power and

ground potential; is that right?

A Just to confirm, you mean power -- to provide power to some circuit is what you mean?

Q I'm sorry. That's right, to provide power to a circuit you need both power and ground potentials; is that right?

A Ultimately, yes, because in these circuits it's electrical power we're talking about and one of the component requirements to provide electrical power is a potential difference, and so the difference is the voltage difference between the power supply line and the ground line as we typically define it.

Q Let's go to claim 12 again. Claim 12 recites a first partial local power mesh and a second partial local power mesh; is that right?

A Yes.

Q Okay. And the first partial local power mesh has its position corresponding to the position of the first power domain; is that right?

A Yes.

Q Does corresponding to you require the first and the second power domains to have the same size and shape as the first power domain and the

second power domain?

A So in my view that is the correct reading of how this should be interpreted, but for the purposes of my analysis I have not assumed that and that is not required --- it is my opinion that the art would invalidate whether that was a requirement or not, but I have not assumed that for the purposes -- that that is a requirement for the purposes of my invalidity analysis.

Q Okay. What construction did you apply for the corresponding to claim term?

A So I applied the plain meaning which doesn't impose a requirement -- so I applied the plain meaning and I -- and I assumed that there's not a requirement that falls within the plain meaning that would require a size and positional correspondence. All I effectively assumed was required is that there was the ability to provide the correspondence for the purposes of the delivery of said power. So I did not impose a size and positional requirement in my analysis for invalidity here.

But having said that, in my opinion the art would invalidate even if that requirement

were imposed.

Q Could you agree that a first partial local power mesh having its position corresponding to the position of a first power domain requires only that that partial local power mesh overlap to some degree with its respective domain when viewed from above?

A I think I already answered that. It's my view that that is not the correct reading, but I assume that that would be good enough -- or at least to cover within the scope of my invalidity analysis I assume that that could be a requirement that's imposed. In any case, my invalidity analysis would apply whether that was the only requirement or the size and positional correspondence requirement was imposed as well.

Q Okay. That's the same for the second partial local power mesh having its position corresponding to the second power domain; is that correct?

A Yes, that's correct, my answer will be the same except I would replace wherever I said first with second.

Q Okay. So claim 12 also recites the word

"separately."

Do you see that?

A Yes.

Q Is it your opinion that separately means separately in time?

A Separately in time, I don't understand what you mean by that.

Q Well, does separately require a separation in time or does separately require a separate path?

MR. WILSON: Objection; form.

THE WITNESS: In this situation, this -- so all this is saying is it provides the power separately. So, in other words, if we look at this what it requires is that there be -- that they are just separate paths. As long as they have their own paths they would meet it.

It could be coincidentally that they happen to have different timings associated with them, but that's not a requirement imposed by this separate language in this limitation.

BY MS. WEISKOPF:

Q Okay. Does separately mean through separate electrical paths?

MR. WILSON: Objection; form.

THE WITNESS: Could I have the question again, please?

BY MS. WEISKOPF:

Q Sure. Does separately in this context of claim 12 mean through separate electrical paths?

MR. WILSON: Objection; form.

THE WITNESS: Within the plain meaning I think separately here could be met by having quite simply separate paths, specifically with respect to the delivery of power for the first power domain and the second power domain.

BY MS. WEISKOPF:

Q Okay. In your response you just said separate paths. Is that meant to be different than separate electrical paths?

A No, I did not mean anything different by that.

Q Is separately met by only partially separate electrical paths?

MR. WILSON: Objection; form.

THE WITNESS: I'm sorry. I didn't understand the question.

BY MS. WEISKOPF:

Q Does separately require a separate electrical path or only a partially separate electrical path?

MR. WILSON: Objection; form.

THE WITNESS: I'm not sure -- again, I'm not sure I understand what you mean by "a partially separate electrical path." If -- I think I need more clarification as to what that means.

BY MS. WEISKOPF:

Q Does the path -- does the electrical path have to be completely separate for separately to be met?

MR. WILSON: Objection; form.

THE WITNESS: Again, I still -- you're using the word "separate" to ask me about separates. I don't know how to answer that. I think I'm going to need you to clarify what you mean by the paths being completely separate before I know how to answer that because the question is sort of circular in how it's constructed.

BY MS. WEISKOPF:

Q Okay. Can you give me an example of a separate electrical path that meets this

limitation?

A Again, that's circular. By definition a separate -- at least with respect to the separate requirement, if you're telling me the paths -- the two paths are separate it meets the requirement.

So I don't know how to answer that when your question is including -- is starting by telling me it's met the requirement.

Q I'm just asking for an example that meets the separately requirement based on the meaning that we just discussed. That's all. Could you give me an example?

A Okay. I think I understand. So if we had a path A that ran through the interconnect stack and provided power to domain A and then we had another path B that ran through the interconnect stack and provided power to domain B and the two -- the two -- the two paths had independent wiring in that the wiring for one was not entirely shared with the wiring for the other they would be separate.

Q Okay. When you say "not entirely shared," what does that mean?

A Well, let's take an example where we

happen to have arbitrarily four layers of metal, and the way I provide power is the power is provided from arbitrarily metal-4 to metal-3 to metal-2 to metal-1 to the active circuit underneath. That would be true for both the power provided to domain A and the power provided to domain B.

But the wiring, if I sort of look at it in sort of two dimensions, the wiring is set up such that domain A uses wiring that's arbitrarily on the left half of the chip and domain B uses arbitrarily wiring that's set up on the right half of the chip, that would meet my previous description.

Q Okay. If the wiring on the left and the wiring on the right were connected on the top metal-4 layer, would that be a separate electrical path?

MR. WILSON: Objection; form.

THE WITNESS: I need more information to answer. How is the wiring on the other layers?

BY MS. WEISKOPF:

Q Not connected.

MR. WILSON: Objection; form.

THE WITNESS: Okay. I think I understand. So you're asking me if I have -- coincidentally the power happens to come in from one power pin, for example, which connects to metal-4 but then I split it up and I have a path that runs on the left half of the chip to the first power domain and the right half of the chip to the second power domain could that be considered separate, and my answer would be, yes, in that situation that could be considered separate because they are still separate paths. They are still different paths.

BY MS. WEISKOPF:

Q Okay. In that scenario if the path on the left is connected to the path on the right by a wire on the metal-4 layer, the top metal-4 layer, is that a separate path?

MR. WILSON: Objection; form.

THE WITNESS: Assuming the other constraints that were imposed by my previous answer where I gave a description they would still be different paths and it just so happens that higher up they happen to share a particular layer of metal the paths are still different. So, yes, that would

still in that situation meet the requirements of being separate.

BY MS. WEISKOPF:

Q Can electricity flow through either path in that scenario where they're connected by a wire on the top layer?

MR. WILSON: Objection; form.

THE WITNESS: I'm not sure I understand what you mean by that.

BY MS. WEISKOPF:

Q Well, we're talking about a separate electrical path. I'm trying to understand how that's separate when it's all connected together.

A But they're not all connected together, just to be clear. In that situation they would have the same voltage because they are provided by supply from the same line, but because there are different paths, for example, in the example that I gave you earlier you could power-gate block A and not power-gate block B and they would be different and separate paths, they are different paths meeting the separate requirement because the power for the first domain and the second domain are provided separately.

Q Let's assume that there's no power-gating. Are they still separate paths in the scenario we talked about where there's a path on the left and a path on the right but they are interconnected on the top metal-4 layer through a wire?

A I don't have enough information to answer. Do the power domains still have different power requirements or are they one power domain?

Q Well, if they're all interconnected could they have different power requirements if there's no power-gating?

A This is your hypothetical. I don't know. I don't have enough information to answer.

Q So in our example we have a path on the left and a path on the right. There's no power-gating at all. There's no connections between the path on the left and the path on the right except one wire on the top layer connecting the path on the left and the path on the right. In that scenario is that a separate electrical path?

MR. WILSON: Objection; form.

THE WITNESS: Again, I don't have enough information to answer because it seems like as you

have set up your question it's one power domain because you told me that they're provided with the same voltages, they're provided with the same powers, you told me that I should explicitly assume that there's no power-gating, yet you seem to be setting up your question by telling me that they're different power domains.

So I don't know how to answer that. It seems contradictory in the way you set it up.

BY MS. WEISKOPF:

Q I'm not assuming anything about a power domain at all in this situation. I'm just asking about an electrical path. There's nothing -- don't worry about the power domains here. We have a wiring path on the left and a wiring path on the right that are separate, and then we have a wire on the top metal layer that's connecting the path on the left and the path on the right. Is that a separate electrical path?

A In that the path on the left is different from the path on the right, yes, they are still separate, putting aside any requirements for them being different power domains or not.

Q Okay. What makes this separate?

A They are different paths. They're not the same path. It may be -- it may be that they coincidentally happen to share the same voltage just because they were driven by the same voltage, but they are different paths.

Q And is it true that the voltage can flow through the entire left path and right path?

A I don't know how to answer that question. Voltage doesn't flow. I think you mean current.

Q I do mean current. Thank you. Can the current flow through the left and the right path in our example?

A Yes.

MR. WILSON: Objection; form.

THE WITNESS: There will be different currents that will flow into the left path and into the right path. The wire that ties them together on the top level sets them nominally to the same voltage on the top level, but based on the current needs of the circuit on the left path and the current needs of the circuit on the right path you will have different currents. That's sort of Engineering 101 that we teach our students when we teach them Kirchoff's current laws.

Kirchoff is C-i -- no, K-i-r-c-h-o-f-f.

BY MS. WEISKOPF:

Q So are those two paths electrically connected in our example?

A I believe you -- in the hypothetical you gave me the answer is yes in that they are electrically connected through that top wire, but they are still different paths in how they're connected to the circuitry underneath.

Q The basis for those being different paths is because they're different wires; is that right?

MR. WILSON: Objection; form.

THE WITNESS: Well, it is true that they are different wires, no, but they are different paths because they are different paths. You just told me one is on the left and one is on the right. So as we define the hypothetical they are different.

BY MS. WEISKOPF:

Q But they're all part of the same circuit?

A Sure, and it's certainly possible to have multiple paths in the same circuit.

Q So can you just help me understand

exactly why these are separate because I don't understand right now, so if you could tell me in another way, explain as if I'm your student why these are separate paths.

MR. WILSON: Objection; form.

THE WITNESS: Okay. In the hypothetical that you set up for me, as I understand the hypothetical, at the top layer of metallization we have a wire that connects from the left half of some wiring to the right half of some wiring. So, therefore, they are connected to the same voltage.

However, there's wiring that runs down through the interconnect stack to some circuit on the left, and there's wiring that runs down through the interconnect stack to some circuit on the right. Those are different wires from each other.

Because they are connected on the top they will be at the same voltage, but they are separate connections, one going to the left circuit and one going to the right circuit, because they are different.

BY MS. WEISKOPF:

Q How does the -- how does the current behave when it's making a decision which path on

the left or the right to take?

MR. WILSON: Objection; form.

THE WITNESS: So -- well, the current doesn't make a decision. It sort of follows the laws of physics. But the short answer is the way these circuits work is assuming -- assuming we ignore resistive drops in the top metal layer the potential at the junction of the two paths will necessarily be the same, and then what happens is the current that flows through the left path will be determined by the impedance of the circuit on the left side and the current that flows through the right path will be determined by the impedance of the circuit on the right side and the ratio of those currents is going to be determined by the impedances.

In other words, that's called current sharing where it's not that the same electron flows into the left and the right. It's the ratio of electrons that go to the left versus the ratio that go to the right. Or let me rephrase that. The ratio that go to the left versus the right depends on the relative impedance of the circuits they are driving.

BY MS. WEISKOPF:

Q Okay. Any single electron could go left or right; is that right?

A Yes. In our view of the world that we use for this analysis electrons cannot be split.

Q In our example it could take the left wiring route or the right wiring route; is that right?

A That's right.

Q So is it true that the only way to have a separate path is to have a separate wire?

MR. WILSON: Objection; form.

THE WITNESS: Again, I don't know how to answer that because you used separate on both sides. If the path we are talking about is a wiring path, then it's true that by using a separate wire you end up with a separate wiring path.

BY MS. WEISKOPF:

Q Can you use the same wire and have a separate wiring path?

MR. WILSON: Objection; form.

THE WITNESS: If the entire connection is the same, in other words, it's the same wire all

the way through, then, no, that would be -- in that situation that's a singular wiring path.

BY MS. WEISKOPF:

Q Is there any difference between an electrical path and a physical path in your mind?

A Sure.

MR. WILSON: Objection; form.

THE WITNESS: Sure. Sure, there could be, but it depends on the hypothetical.

For example, an electrical path that we are talking about could be a path that is a wiring path. A physical path could be an insulator or it could be a path on the row. Not all physical paths are electrical paths. Electrical paths, on the other hand, are physical because they are still physical connections.

BY MS. WEISKOPF:

Q So in the sense of a chip, if you have a separate physical path do you necessarily have a separate electrical path?

A I don't know how to answer that. I don't have enough information on what you mean by "a separate physical path."

Q Okay. I'm just talking about a wire

really. So -- I mean, is there another physical path you can think of in a chip?

A Again, it's your hypothetical. You used physical path. When I use physical path I use it to describe a path on a row or a stack of insulators, but in this case it seems like you're talking about wiring so I don't know how to answer that.

Q Okay. Let's just use wire then in that case. I mean, is there any way to have a different electrical path without having a different wire?

A Okay. I think I understand. So you're asking me is there any way to have a different electrical path without having a different wire, and I think the answer is, no, in that situation at least one wire must be different because there has to be some difference in the path for it to be electrically different.

Q You mentioned circuits can have many different electrical paths; is that right?

A As a general statement, yes. I mean, circuits are constructed in multiple elements typically.

Q Okay. Yeah. Can you explain that a

little bit more? What do you mean by that?

A Sure.

MR. WILSON: Objection; form.

THE WITNESS: Sure. If you take a hypothetical circuit, a hypothetical circuit is typically constructed of multiple elements, for example, multiple transistors, perhaps multiple resistors and capacitors, maybe multiple diodes. They are wired together to make a more complex structure, which is what we call a circuit.

Given that there are multiple elements, for example, transistors that are wired together, there are, as they are wired, multiple paths connecting said elements.

MS. WEISKOPF: Okay. Do you want to take a break or would you like to keep going?

THE WITNESS: I'm actually fine, but I think the court reporter has the hardest job so it depends on her.

THE REPORTER: I would love a break.

MS. WEISKOPF: Why don't we take a break then for just a minute.

THE REPORTER: Thank you.

(Whereupon, a recess was taken.)

MS. WEISKOPF: Back on the record.
BY MS. WEISKOPF:
Q Dr. Subramanian, I still want to keep speaking about claim 12. Can you look at the last couple of elements in claim 12 regarding the plurality of horizontal power supply wires and the plurality of vertical power supply wires? Do you know which limitation I'm talking about?
A Yes, I believe it's the second to last limitation of claim 12.
Q Yes. Do the last -- does the last -- Strike that.
Does the second to last require -- limitation of claim 12 require all the horizontal wires to be on one layer of the global power mesh and all of the vertical wires to be on another layer of the global power mesh?
MR. WILSON: Objection; form, outside the scope.
BY MS. WEISKOPF:
Q Well, I can rephrase that actually.
What is the construction that you applied in your declaration for this limitation?
A With respect to limitation 12, what I've

called 12[e], which is the second last limitation of claim 12, what I looked to see was with respect to my invalidity analysis whether the meaning of this limitation was met given the plain meaning imposed by said limitation.

So what I looked for here was I looked to see was there something that would meet the plain meaning, which I found. For example, in both Jiang and Li I found that the plurality of horizontal power supply wires associated with the global power mesh were in one metal level and the plurality of vertical power supply wires associated with said global mesh were on a second level.

Q Okay. What is the plain meaning of this 12[e] limitation?

A So the 12[e] limitation, firstly, it's addressing the global power mesh, and the requirements it imposes on the global mesh is that there be a plurality of horizontal power supply wires, so more than one, and that there be a plurality of vertical supply wires, so that means more than one.

It requires that for that first plurality they be horizontal and for the second

plurality they be vertical. For the horizontal wires it requires they be placed on a first metal layer and for the vertical wires they be placed on a second metal layer.

Q Okay. Do you agree that there can be vertical power wires also on the first metal layer?

MR. WILSON: Objection; form and outside the scope of his declaration.

BY MS. WEISKOPF:

Q So I'm just trying to understand what the plain meaning is, Dr. Subramanian. So does it require some, some amount of plurality of horizontal power supply wires placed on a first metal layer and there can be other wires placed in different directions on that first metal layer, is that the plain meaning?

MR. WILSON: Objection; form, outside the scope of his declaration.

This is a question that was directly addressed in the ITC. It was not addressed and is not relevant in this IPR.

MS. WEISKOPF: I disagree because I think the plain and ordinary meaning that he applied is important to understand, so I really just want to

understand the scope of the plain and ordinary meaning.

MR. WILSON: Fine, you can ask your question, but it's outside the scope of his declaration.

THE WITNESS: So with respect to my analysis here, what I looked for was something that met the plain meaning. What I found, and it clearly meets the plain meaning, is that there is -- that the horizontal wires associated with said plurality are on one layer and the vertical wires associated with said plurality are on a second layer, and I found that in the art that I use in my analysis. So that would meet the plain meaning.

BY MS. WEISKOPF:

Q I think -- I understand that that's within the scope of the plain meaning. Do you have an understanding of what the plain meaning is, the full scope of the plain meaning is?

A So I provided that in my previous answer where I said the plain meaning of this limitation is provided -- is, firstly, this limitation is associated with the global power mesh. It imposes

a requirement to fall within the scope of the plain meaning of this limitation that the global power mesh has a plurality of power supply wires that are horizontal, so there's more than one horizontal power supply wire and it's on a first metal layer, and then, correspondingly, for the second part of this limitation there's a requirement that there be more than one vertical power supply wires and that those are on a second metal layer.

(Document was marked Exhibit 1005 for identification.)

BY MS. WEISKOPF:

Q Maybe we can come back to this question in Li and you'll understand why I'm wondering the full scope of your plain and ordinary meaning when we get into the context of Li because I just want to make sure I understand what you're saying is the global mesh in Li.

So, actually, why don't we flip over to Li quickly. Let me see if I can figure out how to use this Exhibit Share.

So Li is called Exhibit 1005. Are you able to see 1005, Dr. Subramanian?

A I already have 1005 on my local folder,

so I can use that -- yeah, I see it. It just showed up on the drive as well.

Q Okay; good. Yes, let's just go to figure 3 really quickly to try to put some context onto this.

So on figure 3 we can see that there's this shaded layer called the redistribution layer. Do you see that in figure 3, it's got three wires?

A Yes.

Q Those have -- those have these things called bumps on them.

Do you see that?

A Yes.

Q Do you think that the -- or is it your position that the redistribution layer here is part of the global power mesh?

A So with respect to the global power mesh what I point to are metal-6 and metal-7, and I would refer you to -- with respect to limitation 12[e] I would refer you to paragraph 169 of my declaration where I specifically call that out and with respect to where I first identify the global power mesh in Li I would refer you to, for example, paragraph 164 where I call that out.

Q Okay. So the redistribution layer here is not part of the global power mesh; is that right?

A What I identify as the global power mesh is metal-6 and 7. The redistribution layer is another metal layer that's above metal-6 and 7.

Q Okay. And so for the purposes of your opinions here the redistribution layer is not one of the layers of the global power mesh?

A With respect to what I identify as the global power mesh I do not identify the redistribution layer that's a higher metal layer. I identify the metal layers 6 and 7.

Q Do you have any other opinions about the redistribution layer besides what you put into your declaration about it being part of the global power mesh?

A No, I point -- what I put in my declaration is what I put in -- is the opinion that I offer.

Q Okay. All right. I understand. I appreciate you are clarifying.

All right. Let's talk about -- let's go back to Exhibit 1001, which is the '218 patent,

and let's look again at claim -- go back to claim 12. Claim 12 also recites to provide the power needed by the first and second power domain; is that right?

A Yes. I believe that's towards the end of the third limitation of claim 12.

Q Yes. What meaning did you apply for that phrase in your declaration?

A Again, I applied the plain meaning. So specifically in the context of this limitation this is referring to the global power mesh, and the part that you specifically asked me about is the phrase "to provide the power needed by the first power domain and the second power domain." You didn't use the word "separately."

So all this is requiring is that the global power mesh which is coupled to the first and second local power meshes is providing power to the power domains in question; namely, the first power domain and the second power domain.

Q Okay. Do you agree that this phrase requires providing some nonzero power to both the first and second power domains?

A So I don't think that's the correct

reading. If the need is zero, I think it would be acceptable for it to be zero.

Having said that, in the art that I used they would meet even if the requirement is that it be nonzero because no matter what it will at least provide the leakage power to maintain the circuit operation even in the case where you have a transistor that's gating it, and it certainly would be obvious to provide nonzero power in both situations if that were what is required.

And when you are power-gating there will at least be periods of time where you're providing nonzero power.

Q Okay. So none of the opinions in your declaration would change if providing the power needed required nonzero power; is that right?

A In other words, it is my opinion that -- the opinions I provide, the grounds that I provide with respect to invalidity would apply whether or not nonzero power were required.

Q Let's look at claim 14. This one requires the partial local power meshes to not be electrically coupled; is that right?

A That's right. This is, of course, under

the assumption I've been asked to assume that the local power mesh is referring back to the partial local power mesh, and that is an assumption I made for this matter.

Q Thank you for clarifying that. I understand.

So let's talk about electrically coupling. Can power wires electrically couple?

A I don't understand the question. You mean with respect to each other?

Q Yes. Can you couple two power wires together?

A Conceptually, yes.

Q Okay. How do you couple two power wires together?

A For example, one way to couple two power wires together is to run a wire that connects them so you have an electrical connection between them.

Q Okay. And vias would also electrically couple two power wires and a chip; is that right?

A If you have a via that connects two wires which in this case would be on different levels together, yes, the answer is that could couple them, sure.

Q Does your answer change at all if you're talking about ground wires?

A No, the constraints that I imposed in my previous set of questions would be the same. Sorry. The constraints that I imposed in my previous set of answers would be the same.

Q Okay. So just by connecting two power wires together you can electrically couple them; is that right?

A In the specific example that I gave, yes. You asked me to give an example of how you could couple them. In that example putting the wire there coupled them.

Q Okay. And then you can also couple two ground wires by connecting two wires with a third wire for ground; is that right?

MR. WILSON: Objection; form.

THE WITNESS: If you have two ground wires, one way to couple them would certainly be by connecting them together with a third wire such that they were electrically tied to each other.

BY MS. WEISKOPF:

Q Okay. And the same applies to ground wires for a via also, if you have two ground wires

on two different metal layers that are connected together by a via they would be electrically coupled; is that right?

A Yes, I agree.

Q Okay. Let's look at claim 1. Now, you and I have spent less time talking about this one. This one requires APR tools; is that right?

A Yes.

Q What is an APR tool?

A APR stands for automatic place and route or sometimes referred to as automatic placement and routing, and it's a software tool that is used to at least partially automate the wiring that occurs during the design of a silicon integrated circuit.

Q Now I've looked at your declaration and it seems to me, but please correct me if I'm wrong, that your opinion is that if there's a structure that meets the elements of claim 12 then the method of claim 1 is performed; is that correct?

MR. WILSON: Objection; form.

THE WITNESS: That's not quite correct. It's my opinion that if one of skill knew of the structure of claim 12 and was aware of the use of APR tools, and it's my opinion that one of skill

was, one of skill would find claim 1 or the method of claim 1 to be obvious.

BY MS. WEISKOPF:

Q Okay. I understand. So let's put aside the APR tool limitation in each of these elements. Is it your opinion that if you have the structure of claim 12 you would necessarily perform the steps in claim 1 with the APR tool limitation aside?

MR. WILSON: Objection; form.

THE WITNESS: No, it's my opinion that one of skill looking at art that disclosed the structure of claim 12 would find the steps of claim 1 to be obvious, putting aside the APR tool requirement.

In other words, my -- I'm not offering an anticipation argument, for example, in ground 3 with respect to claim 1. I'm offering an obviousness argument with respect to claim 1.

BY MS. WEISKOPF:

Q Okay. I think I understand. So you have a structure of claim 12, and it's your opinion that a POSA would find it obvious to perform each step in order to get to claim 12, is that right, the claim -- excuse me.

If you have a structure of claim 12 it would be obvious to perform each of the steps in claim 1 to achieve that structure; is that correct?

MR. WILSON: Objection; form.

THE WITNESS: So if one of skill were aware of art that taught the structure of claim 12 one of skill would find it obvious to perform all the steps of claim 1, putting aside the APR argument which I also believe is obvious in light of the art.

BY MS. WEISKOPF:

Q Can the structure that meets the elements of claim 12, can that be formed in different ways?

MR. WILSON: Objection; form.

THE WITNESS: And just to be clear, your question was about claim 12? In other words, to realize a structure of claim 12 could you form it in different manners using different methods?

BY MS. WEISKOPF:

Q Yes, that's exactly the question.

A Okay. I think I understand.

And so the answer to that is, yes, in that, for example, as I say in my declaration, the claim -- if we look at, for example, claim element

12[a], which is about the first partial local power mesh, you could do it without an automatic place and routing tool but -- and so that would be doing it in a different method than doing it with the automatic place and routing tool, but to one of skill it would be obvious to do it with an automatic place and routing tool.

Q Okay. Is it your opinion that as long as you have formed a first partial local power mesh using an APR tool by the end of the process you will have performed that step, forming the partial local power mesh step?

MR. WILSON: Objection; form.

THE WITNESS: I'm not sure I understand the question, but if your question is if you perform -- I think we're talking about step 1[a], which is the forming of first partial local power mesh limitation. If you perform all the requirements of that step, including using the automatic place and routing tool, it's true that by definition, just based on the circularity of that question, you would have performed step 1[a].

BY MS. WEISKOPF:

Q Sure. So if you start with a structure

of claim 12, does that necessarily require forming a first partial local power mesh according to step 1[a]?

A Okay. I think --

MR. WILSON: Objection; form.

THE WITNESS: So if we look at step 12, if we have a piece of art that shows us that that art shows a first partial local power mesh and its position is corresponding to the position of a first power domain, so, in other words, you established the correspondence relationship, to one of skill it would be obvious that the way to get there is by forming that first partial local power mesh according to the position of a first power domain of the integrated circuit, and if we wanted to we could certainly have done it and it would be obvious to one of skill in the art to do it with an APR tool.

BY MS. WEISKOPF:

Q Okay. So it's your opinion that it's not necessarily required in order to form a structure according to claim 12 but it would be obvious to perform step 1[a]; is that right?

A My opinion on claim 1 is an obviousness

opinion. So, for example, I specifically -- I say that, and I told you this in a previous answer, that you could in theory achieve step 12[a] without using an APR tool, but it would be obvious to use an APR tool.

Q Okay. Yeah. Let's put aside the APR tools because that's where I'm trying to clarify. I understand that that's part obvious, your argument is that that's obvious to use the APR tool, but I'm most interested right now in not using an APR tool but the other portions of step 1[a], so forming a first partial local power mesh according to the position of a first power domain.

For that step, is that step necessarily formed, and performed I mean, is that step necessarily performed if there's a structure that meets the elements of claim 12?

MR. WILSON: Objection; form.

THE WITNESS: Again, I don't have enough -- I don't know how to answer that question because you're asking me about -- about -- well, actually, I'm not sure I understand what you're asking me. I guess that's the answer. I don't have an answer to that question.

BY MS. WEISKOPF:

Q Okay. Do you -- in order to achieve the structure of claim 12 do you necessarily have to form a first partial local power mesh according to the position of a first power domain?

MR. WILSON: Objection; form.

THE WITNESS: I think I understand. If one of skill were to build a structure or to look at art that ultimately delivered a structure that corresponded to element 12[a], the method they would use to get to 12[a] would follow parts of limitation 1[a] but not all of it.

BY MS. WEISKOPF:

Q Okay. That is exactly what I'm trying to ask. So in order to achieve the structure of claim 12 you would necessarily perform that step of forming a first partial local power mesh according to the position of a first power domain?

MR. WILSON: Objection; form.

THE WITNESS: Again, I'm not sure I understand the question.

So one -- again, this is all -- this is an obviousness position, so it's all through the eyes of one of skill. One of skill would say if I

were trying to build a structure that ultimately resulted in the structure of 12[a] it would be obvious to do it by forming a first partial local power mesh according to the position of a first power domain of the integrated circuit without requiring specifically the automatic place and route tool, but it is my opinion that even that would be obvious as well.

BY MS. WEISKOPF:

Q Okay. I get it. So the -- what are the other ways to achieve the structure of claim 12 that don't involve performing this forming of first partial local power mesh according to the position of a first power domain?

MR. WILSON: Objection; form.

THE WITNESS: I have -- I don't know the full universe of possibilities. I've given you the one possibility, which is you could do it without using an APR tool.

BY MS. WEISKOPF:

Q Okay. Can you create a structure of claim 12 without forming a first partial local power mesh according to the position of a first power domain?

A I don't have enough information to answer. I don't -- so I have not investigated the full universe of possibilities. It's certainly true that one of skill looking at a structure of claim 12[a] as disclosed by both Jiang and Li would find claim 1[a] obvious.

Q Okay. In rendering that opinion you didn't consider other methods that might have achieved the structure of claim 12?

MR. WILSON: Objection; form.

THE WITNESS: I don't know how to answer that. I considered the disclosures of Jiang and Li.

BY MS. WEISKOPF:

Q Okay. Jiang does not disclose how the structure of the figure 1(b) is formed; is that right?

MR. WILSON: Objection; form.

THE WITNESS: Within the disclosure of Jiang associated with figure 1(b) there's no explicit description of the fabrication process that's used. However, to one of skill looking at it, one of skill would say that the methods to get there, putting aside the APR requirement, it would

certainly be obvious to follow that of claim 1.
BY MS. WEISKOPF:
Q Okay. Why would it be obvious?
MR. WILSON: Objection; form.
THE WITNESS: It would be obvious in light of the disclosure. So if we look at figure 1(b), what figure -- if we're talking specifically about the first partial local power mesh, what we see in Jiang(b) is we have the partial local power mesh is shown on L2 and they have the correspondence that we had discussed previously with respect to their respective power domains.
So one of skill seeing that would say that it would be obvious to form a first partial local power mesh according to the position of a first power domain of the integrated circuit.
BY MS. WEISKOPF:
Q Have you performed power routing design?
A You mean personally?
Q Yeah, yeah. Personally.
A Yes, absolutely.
Q Do you form a mesh as part of the power routing design?
A Yes, I have.

MR. WILSON: Objection; form.

THE WITNESS: Yes, I have in some of my previous designs.

BY MS. WEISKOPF:

Q What are some of the other ways you've formed the power routing structure besides a mesh?

A Oh. Well, I've done simple integrated circuits where I didn't use meshes, where I used -- where I used nonmesh power routing architectures, but those were extremely simple circuits.

For more complex circuits you almost always use some sort of mesh architecture just because it's a very efficient way of performing the routing. Also, it turns out in modern design rules really starting at about 130 nanometers it turns out there are actually process requirements that require unidirectional metal during your layout process, so you end up getting a mesh when you do the routing.

Q So for the more simple ones that didn't involve a mesh how was your power routed?

A I did it by hand, and I had just individual lines that provided wiring to specific connection points in the active circuit.

Q Is it fair to call those lines rails? Is that what rails means?

A No. Not necessarily. Those were -- those were actually just arbitrarily hand drawn. In other words, they were bidirectional lines. They ran in a single layer both vertically and horizontally to deliver power to certain parts of the circuit. There were no intersections in those designs.

Q Okay. Does rail mean there's an intersection?

A No.

Q Okay. Okay. Let's just go back to claim 12 here. I mean, I'm sorry, claim 1.

It's not your opinion that claim 1 requires any order of steps; is that right?

A You mean relative -- you mean one step relative to the other?

Q Right. There's no order of steps required by claim 1; is that right?

A So I -- for the purpose of my analysis it wouldn't affect my opinion whether there is an order requirement or not because it will be obvious no matter what. But having said that, with respect

to my analysis, therefore, it doesn't matter whether there's an order requirement or not.

Q Okay. Is there an order of steps required, though, in your opinion?

A Again, for the purposes of my analysis it doesn't matter whether there's an order requirement or not. Just looking at the individual relationships between the individual steps, provided you have the position of the first power domain you could form the partial local power mesh according to that and you could do that similarly for the second power domain. Provided you had those two power domains available you could implement the individual steps either 1[a] before 1[b] or 1[b] before 1[a].

So provided the requirements of the relationships between the individual limitations are provided, in theory you could do 1[b] before 1[a] or 1[a] before 1[b] because they don't depend on each other, but, again, in my view it would be obvious no matter whether there's an ordering requirement or not.

Q Okay. Yeah. Let's look at the next one, 1[c]. Is there an ordering requirement for 1[c],

forming a global power mesh?

A You mean with respect to, for example, 1[a] and 1[b]?

Q Right. We determined already that 1[a] and 1[b] can be performed in any order. What about 1[c], does that have an ordering requirement?

A So conventionally with respect to how we often do layouts it's usually true that we start with the lower levels of metal and work our way up, but conceptually what you could do is you could do the global power mesh knowing where you plan to place the local power meshes and you know where you plan to place the local power meshes because you know where the power domains are.

So in theory, with that foreknowledge, you could do 1[c] before you do 1[a] and 1[b] in terms of the layout.

Q Okay. Now let's take the coupling steps. Is there any order required for the coupling steps?

A So with respect to the coupling steps, specifically that's 1[d] and 1[e] where you're coupling the respective local power meshes to the global power mesh, provided you know the position or the planned positions of the local and global

power meshes you could in theory lay out the vias first to perform the coupling.

In practice that's typically not what's done. The vias are defined after you've positioned the respective metal layers, but it is conceptually possible that if you have foreknowledge of their planned position you could do the vias before you do the metal layers and then define the metal layers to make sure that they are in the right positions relative to the vias.

Q Okay. So I think we've gone through each of the steps of claim 1, and it sounds like there's no ordering requirement in your opinion; is that right?

A So, again, as I said, with respect -- so with respect to my invalidity opinion it does not matter whether there's an ordering requirement or not. With respect to the individual limitations, provided you have the necessary foreknowledge you could switch the order around. I agree with that. But, again, it's only in the situation where you have that foreknowledge and follow it.

Q So let's look at claim 19, which is also an APR tool claim. So there's one big step here

that starts with "providing a global power mesh" and it's many lines long, and at the end it says "by an automatic placement and routing tool."

Do you see that?

A I do.

Q So we can go through this individually, but my question is do each of the different wires that are discussed here in the providing step, do they each need to be placed by the APR tool in your opinion?

A So the requirement imposed by this claim limitation is that you're providing a global power mesh. That's sort of the crux of this limitation. And it says -- it has various wires called out, but those wires are called out as following the comprising language and it says that the global power mesh comprises at least one first power wire, at least one second power wire, and at least one ground wire.

So as I read this limitation, given that the by an automatic placement and routing tool language appears at the end of this limitation it applies to the global power mesh. So it applies to the global power mesh. That doesn't mean every

single structure that is used in the global power mesh cannot have any manual input, but you have to use the APR tool when you're making the global power mesh. That's the requirement.

Q Okay. So at least one first power wire claimed here, does that need to be provided by an automatic placement and routing tool?

A If you meet the requirement that the global power mesh is provided by an automatic place and routing tool conceptually you could have individual wires that are not specifically provided by that provided the overall mesh is, and that would include the first power wire.

Having said that, it is my opinion that no matter what, whether it must be provided by an APR tool for that specific wire or not, it would still be obvious because it turns out sort of the global power wire routing is one of the things that APR tools are really good at. They're really good at generating meshes. So it's very straightforward to do it that way.

Q Okay. Is there any order required in claim 19?

A So if we look at claim 19, the first

limitation specifies the global power mesh. The second limitation requires coupling to the first power domain. The third limitation requires coupling to the second power domain. The fourth limitation just gives us more details about the power mesh, and specifically the global power mesh. And the fifth limitation just places a layer requirement.

So with respect to the second and third limitations, it's my opinion that -- firstly, this -- it's my opinion that this entire claim would be obvious independent of whether there is or is not a power requirement -- sorry, an ordering requirement. In other words, the prior art would invalidate this claim under both situations.

But, again, using the same analysis that I provided earlier, in theory with the foreknowledge of the positioning of the wires of the global power mesh the APR tool could place the vias to enable the coupling required by the second and third limitations prior to the power mesh wires having been placed. That's typically not how it's done. The most straightforward way to do it is to place the wires first and in the next iteration

when the APR tool goes through it it places the vias, but conceptually if the APR tool were preprogrammed with the knowledge of where the wires are going to be or where they need to be, the APR tool could reverse the order.

So in theory it would be possible then to do steps 19[b] and [c] before you did 19[a], but, again, in my opinion independent of whether there is an ordering requirement or not this claim would still be obvious in light of the prior art.

Q But as we just discussed, claim 19 does not actually have an order requirement, right?

A Again, as I said, so if we look at 1[b] -- and I guess the ordering requirement is really related to 1[a] -- sorry, 19[a], 19[b], and 19[c]. Given the specific requirements of foreknowledge that I placed, it is conceptually possible to not impose an ordering requirement and still implement the method of claim 19.

Q Okay. So as we discussed for claims 1 and 19, there's no ordering requirement; is that right?

MR. WILSON: Objection; form.

THE WITNESS: That's not what I said. I

said in the specific situation where you implement the foreknowledge that you need to eliminate the need for ordering one could practice the methods of claims 1 and 19, but it's in that specific situation.

In other words, if you didn't have the foreknowledge and you just placed the vias without making any effort to align them to the metallization you wouldn't get a functional structure meeting the requirements of the method of the claim.

BY MS. WEISKOPF:

Q Okay. So I'm just talking about claim construction here, to be honest, not sort of any of the rest of conceptually what you're talking about. I just want to know do you think that claims 1 and 19 have an order of steps requirement or not?

MR. WILSON: Objection; form.

THE WITNESS: Again, with respect to claims 1 and 19, firstly, it is my opinion that independent of whether there is an order requirement or not the prior art would still make these obvious.

Having said that, if we meet the

requirements of every limitation, and to meet said requirements of every limitation if we want to reverse the ordering we would need to have some foreknowledge, but assuming we do that and can meet the requirements of the limitations then the ordering wouldn't matter.

BY MS. WEISKOPF:

Q Okay. And would a person of ordinary skill in the art know how to meet those foreknowledge requirements?

MR. WILSON: Objection; form.

THE WITNESS: Yeah, conceptually, yes, because a person of ordinary skill in the art would be controlling the APR tool and specifying the ordering of the layers.

Having said that, the normal way to do it that is common is to do the interconnect before you do the vias. That's just the standard way of doing it. So while it would be obvious, it's often easier to do it in the order that is actually specified.

Let me rephrase that. It's more standard to do it in the order that is specified.

BY MS. WEISKOPF:

Q Okay. So I just need your opinion on what claims 1 and 19 require. Does claim 1 require an order of steps?

MR. WILSON: Objection; form.

THE WITNESS: Okay. So I think I've answered that. So if you are able to -- so, firstly, it is my opinion that claim 1 is obvious whether or not there's a step requirement for -- an order requirement for the steps.

Having said that, if we look at the individual limitations of claim 1, if we are able to carry out said limitations of claim 1 correctly you could practice the method of claim 1 without imposing a requirement on the order of steps, but you would need to actually implement that.

BY MS. WEISKOPF:

Q Okay. This is just a yes-or-no question. In your opinion does claim 1 require an order of steps?

MR. WILSON: Objection; form.

THE WITNESS: Again, it's not a yes-or-no answer because it depends on the situation. If you do not follow the order of steps of claim 1 but you

do it incorrectly it won't practice the method of claim 1, but if you do it correctly you can do it without imposing an order requirement.

BY MS. WEISKOPF:

Q I'm not talking about practicing claim 1. I'm just talking about the requirements of claim 1. Does claim 1 on its face, doing purely claim construction, require an order of steps?

MR. WILSON: Objection; form.

BY MS. WEISKOPF:

Q Just yes or no.

A Again, I'm afraid it's not a yes-or-no question -- the answer is not a yes-or-no answer, so I'm not able to give it a yes-or-no answer because of the following reason.

To do the correct claim construction whatever you're construing has to actually define the scope of the claim, which means it has to actually define the method that's being performed. If the method is -- to perform the method it is possible to perform said method without imposing an order requirement, but you still have to do the necessary things to enable the practicing of the method.

Q Is your answer the same for 19?
A Yes, with the same reasoning.
Q So a POSA would understand that you could perform claim 19 without following an order of steps?
MR. WILSON: Objection; form.
THE WITNESS: Again, it's the same answer I gave earlier, which is provided a -- so a POSA would know given the foreknowledge, which a POSA would have, that the claim 19 could be practiced given that foreknowledge without imposing a requirement of the order provided they actually followed the steps with the appropriate foreknowledge.
BY MS. WEISKOPF:
Q And the POSA would have that appropriate foreknowledge; is that right?
MR. WILSON: Objection; form.
THE WITNESS: Yeah, I believe that a POSA would certainly be -- it would be straightforward for a POSA to obtain that foreknowledge.
BY MS. WEISKOPF:
Q Okay. I just want to ask you some terminology questions to make sure that we're on

the same page. Have you heard the term PMOS switch?

A PMOS switch? Yes.

Q What is that?

A So it's a particular type of switching transistor. PMOS -- so M-O-S stands for metal-oxide-semiconductor. P is electrical engineering shorthand for holes. So PMOS just means a metal-oxide-semiconductor switch where the dominant carrier is holes.

Q Is there a connection between a PMOS switch and a power switch?

A It depends. There could be or there could not be. You can use -- you can use PMOS switches to implement power switches or you cannot. It's up to you.

Q What kind of switches are there -- let me rephrase that.

You can have a power or a ground switch; is that right?

A I don't know what --

MR. WILSON: Objection; form.

THE WITNESS: Yeah, I need more information to answer that. I don't know what you

mean by that.
BY MS. WEISKOPF:
Q There exists switches that control power and there's also switches that control the ground; is that right?
MR. WILSON: Objection; form.
THE WITNESS: Okay. So you could have a switch that sits between the power supply terminal and your circuit. You can also have a switch that sits between the ground terminal and your circuit. So if that's what you mean by a power switch and a ground switch, yes, it's true you can have both types of switches.
BY MS. WEISKOPF:
Q Okay. And can you use a PMOS switch for both power and ground switching?
A Yes. It provides -- yes. The short answer is yes. There is slight differences in the voltages that are available when you use it for pulling up or pulling down, but conceptually, yes, you can use it in both locations. There's advantages and disadvantages to doing it that way.
Q Okay. There's also something called an NMOS switch, right?

A Yes.
Q What's an NMOS switch?
MR. WILSON: Objection.
THE WITNESS: Again, M-O-S --
MR. WILSON: Hang on. Objection; form and outside the scope of his declaration.
This, again, is venturing into ITC determination territory. It's not relevant to the IPR.
MS. WEISKOPF: I think there's an NMOS switch mentioned in Li, so I disagree. I think it's part of the disclosure of Li. I'm just trying to understand the switches.
MR. WILSON: Okay. Where is the PMOS switch?
MS. WEISKOPF: I think the PMOS switch is in Jiang, but we can get into that. I think there's different switches.
MR. WILSON: Yeah, I don't think so.
MS. WEISKOPF: It's also just background.
BY MS. WEISKOPF:
Q Anyway, what is an NMOS switch, Dr. Subramanian?
A So M-O-S stands for metal-oxide-

semiconductor. N is electrical engineering shorthand for electrons. So an NMOS switch is a switching metal-oxide-semiconductor transistor where the major carrier that is used in the channel is electrons.

Q Okay. Is an NMOS switch used as a ground switch at least sometimes?

A It could be. Doesn't have to be. There's multiple possible ways of using it.

Q Okay. Do you recall if there's an NMOS switch in the Li reference mentioned?

MR. WILSON: Objection; form.

THE WITNESS: I'm sorry. I'll have to look at Li. I haven't memorized Li.

BY MS. WEISKOPF:

Q That's okay. Let's flip to Li. Let's look at that together.

A Okay. I have Li.

Q Okay. Yeah, can you turn to page 492?

A Okay.

Q Do you see under section 2 it says NMOS and PMOS?

A Yes.

Q What does that mean?

A So --

MR. WILSON: Objection; form.

THE WITNESS: So in page 492, and you're referring to the Process Technology section 2? Is that what you're referring to?

BY MS. WEISKOPF:

Q Yes.

A Okay. So in that where the words "NMOS" and "PMOS" appears are in the sentence "When a triple-well CMOS technology is used, separate voltage lines can be connected to the NMOS and PMOS bulk regions."

What that is referring to is when we build these transistors there are built-in wells. A triple-well technology, and, actually, a triple-well technology is shown on the next page, 493, what you have is you have a well inside another well, and the advantage of doing that is you can reverse bias the voltage between the inner well and the outer well so you don't have cross talk between adjacent wells.

So what that allows you to do is that allows you to apply different voltages to the well regions off the transistors which is then used to

do what's called body biasing or back biasing of the transistors and that allows you to dynamically alter the threshold voltage such that you can turn them off strongly.

Q Okay. Is there a switch in Li?

MR. WILSON: Objection; form.

THE WITNESS: Yes, we look, for example, on page 494 on figure 4 there's a device called a power switch, which is in the dashed line on figure 4.

BY MS. WEISKOPF:

Q Okay. Is that a ground switch?

A So in the -- in the device that's shown here it's connected -- it's the enable line or it's the power switch that lives between the core and the ground, specifically called substrate ground which is different from well ground, and that is, therefore -- given the definition you provided earlier where you said a power switch would be a switch between power and the circuit and a ground switch would be between the circuit and ground, under that definition this would be a ground switch because it's on the ground side of the core.

Q Okay. Do you know if this is an NMOS

switch or a PMOS switch?

A So I would expect this to be an NMOS switch so for the following reasons. Firstly, generally when we show PMOS switches we show them with a little dot on the gate side which this doesn't have, has a little bubble on the gate side.

You could do this with PMOS or NMOS. There's reasons to do it with NMOS, there's slight power advantages of doing it with NMOS, but you can conceptually do it with both.

With respect to the description, other than the fact that it shows a transistor without a bubble, it's silent at least in the description of figure 4 with respect to the power switch as to whether it's NMOS or PMOS, but it wouldn't surprise me -- actually, it looks like in the next paragraph, 4.2, it says it's an NMOS switch. So that's further validation that this is probably NMOS.

It looks like NMOS to me, and it seems like in section 4.2 it says that the different internal ground net for each core is separated from chip ground by an NMOS switch. So I would expect this to be NMOS.

Q Okay. All right. So in terms of macros, do you agree that a macro is a collection of cells?

MR. WILSON: Objection; form.

THE WITNESS: So it can be. So macro is used in multiple ways in different applications. Certainly -- I mean, one way that we can use macros is a name to describe a collection of cells. Macros are also used to describe circuit blocks because it's hierarchical. So we often use the term "a macro" when we're talking about a circuit block. It's very contextually specific.

BY MS. WEISKOPF:

Q Are circuit blocks made of macros?

MR. WILSON: Objection; form.

THE WITNESS: They don't -- so they could be or they could not. Again, it's contextually specific. A circuit block itself could be a macro, but a circuit block could also be described as having a bunch of macros that are connected together to form a bigger macro which is then a circuit block.

A macro is a hierarchical term, so it depends on the context very specifically. So, for example, if we look at Li, Li calls them macros,

but it's very clear that what Li is talking about is actually these are big circuit blocks so they're power domains.

Sorry, not Li. I meant Jiang.

BY MS. WEISKOPF:

Q So I was definitely distracted by you saying Li because I thought we were talking about Jiang. So for Jiang you're saying there's collections of cells; is that right?

MR. WILSON: Objection; form.

THE WITNESS: In fact, that's exactly not what I said. What I said is when Jiang is using the term "macro" it's using it to describe these circuit blocks A, B, C, and D, which are very clearly power domains.

BY MS. WEISKOPF:

Q Okay. But they -- I understand. So the A, B, C, and D circuit blocks in Jiang are circuit blocks made of macros?

MR. WILSON: Objection; form.

THE WITNESS: No. Again, that's not what I said, and I'm going to say it again.

Jiang uses the term "macro," so when Jiang uses the term "macro," let me see if I can

search. Yeah. Okay.

So, for example, if we look at paragraph -- the bottom of column 2 of Jiang, it says right at the bottom "In the power-gated chip, we have local power meshes for all macros, and sleep transistors are used to connect the local mesh to the global mesh."

It goes on to say at the top of column 3 "When a macro is active, the sleep transistor is turned on."

So what we see clearly here is that what it's referring to is the macros are the blocks A, B, C, and D. So those are the macros. It's not that they are -- in some other context you could say that the design of those n-wells is lower level macros, but the macros Jiang are referring to are the circuit blocks, in other words, the power domains, A, B, C, and D.

BY MS. WEISKOPF:

Q I think I understand. You're just saying A, B, C, and D are what the macros are in Jiang; is that right?

MR. WILSON: Objection; form.

THE WITNESS: In the description that I

just read, so specifically it says "In the power-gated chip," which is the 1[b] chip, it says "we have local power meshes for all macros, and sleep transistors are used to connect the local mesh to the global mesh. When a macro is active, the sleep transistor is turned on."

So using that language what we see is, for example, if we look at A, B, C, and D they are macros and they each have a local -- a local power mesh associated with them and then sleep transistors are provided. Now, in this case sleep transistors are provided associated with B and C but not with A and D.

(Document was marked Exhibit 1004 for identification.)

BY MS. WEISKOPF:

Q Okay. I understand macros in this context according to your opinion. I appreciate that.

Okay. Just for the record, the Jiang is Exhibit 1004 that we were just talking about, and we're going to introduce that as an exhibit also.

Okay. So let's -- so now we're

talking about IP blocks. Do you agree that the functions of the chips are executed by the IP blocks?

MR. WILSON: Objection; form.

THE WITNESS: I'm sorry. Could you point me to what IP blocks you're referring to?

BY MS. WEISKOPF:

Q It's a more general question. I'm not trying to use terminology -- I'm just trying to use general terminology here. You know, if you've got an SoC the functions are performed by the blocks for the circuitry of the chip; is that right?

MR. WILSON: Objection; form.

THE WITNESS: Again, I think I need more information to answer. So you also changed terminology. So first you said IP blocks and then you said circuits of the chip, so maybe you can clarify the question and then I'll know which one you want me to answer.

BY MS. WEISKOPF:

Q Okay. Yes, I didn't realize it was confusing.

So what's an IP block?

A So it's --

MR. WILSON: Objection; form.

THE WITNESS: Sorry. It's contextually specific. There's different use of the term "IP block," but generally in the chip design industry an IP block is often used to refer to sort of the layout of a circuit that is sort of self-contained.

For example, you can have an IP block for a memory, and that means that's the memory which you could drop into a larger circuit and make something more complex.

BY MS. WEISKOPF:

Q Okay. What performs the functions of a chip?

MR. WILSON: Objection; form.

THE WITNESS: I guess it depends on what you mean by "functions," but if you're asking me what allows a chip to -- or what happens when a chip is operating, once the circuitry within the chip is performing electrical operations those electrical operations may be direct electrical operations or they may be electrical operations that embody implementation of software functionality. In other words, the software is running on the hardware.

But in either case, what's happening when the chip is operating is the electrical circuits are operating.

BY MS. WEISKOPF:

Q Okay. And power is provided to those -- to the circuitry of the chip for it to function; is that right?

A For any chip that is not self-generating power, it's true that you have to provide power to the chip for it to operate.

Q And you're providing power to the chip circuitry for it to operate; is that right?

A In that situation, yes, I agree.

Q Okay. And the specific circuitry in the chip is how you determine what power to provide; is that right?

MR. WILSON: Objection; form.

THE WITNESS: Yeah, I'm sorry, I have no idea what that question means.

BY MS. WEISKOPF:

Q How do you determine what power to provide to the chip circuitry?

A So it depends. So, for example -- well, ultimately there's -- for a given circuit there is

needs imposed with respect to what voltage ranges over which the circuit will operate.

So we know when we go through our design and validation that circuits will run above a certain voltage and below a certain voltage. There's a certain range in which they'll operate. If we go above or below that we'll either damage the circuit or it won't work.

And so at least with respect to voltage we have specifications which define what are needed. We provide the voltage. The circuit sort of draws its own current based on the voltage that it is provided. We generally have an understanding of what that current draw is, we know that from the design process and we know that through validation, and so then we just make sure that the power supply is capable of providing the current that we need.

That's sort of how we set up chips to operate with respect to the power supply requirements.

Q Is it typically preferred to provide -- to provide the least amount of power the circuitry needs to operate?

A No. That might be true in some situations. In others it's categorically not true.

For example, I mean, we do this all the time, in microprocessors we routinely ramp up and ramp down the power that we provide based on our performance requirements. So if you just provided the least amount of power that it needs to operate it will tend to -- it will save you power but it will run at sort of the lower limit of what it's capable of performing at. If you can provide more power, if you're able to dynamically clock it, you might be able to run it at higher performance levels.

So it's -- it's application-specific. It is true that in some applications you want run at the minimum power that you can reliably meet, but in others that may not be what you want.

Q Okay. So you would look at the performance requirements to determine how much power to provide; is that right?

MR. WILSON: Objection; form.

THE WITNESS: No, that's not quite correct. One of the things that determines the power requirements is performance. The other thing

that determines power requirements is basic functionality; in other words, will it work. Still another thing that determines power requirements are reliability. It may be that at the minimum possible power it barely works but it doesn't guarantee to work all the time.

So there's a bunch of factors that we consider. We know how to do this. We know how to map power reliability and performance. In fact, we do this routinely during design and validation.

BY MS. WEISKOPF:

Q So power-gating is typically implemented using a switch; is that right?

A It certainly at least uses a switch. There can be others -- I mean, there usually is other circuitry associated with power-gating, but, yes, ultimately somewhere in the path some sort of switch is inserted. I agree with that.

Q Are switches typically in the substrate?

MR. WILSON: Objection; form.

THE WITNESS: So, again, so it -- in these sorts of circuits the switches that we are able to use are transistors. The transistor is built at the top of the substrate. In other words,

it's in the surface layer of the substrate. The gate of the transistor is just above the physical silicon substrate, but if by using the term "substrate" you meant as opposed to in the interconnect layers then, yes, it's true, the switches are usually in the substrate, not in the interconnect.

BY MS. WEISKOPF:

Q Okay. Are you familiar with the term "via stack"?

A Yes.

Q What is a via stack?

A A via stack is a series of individual vias. Typically the term "via stack" is referring to vias that are connected end-to-end, though sometimes a via stack is used more broadly.

But in general via stack is used to indicate a series of vias that are placed end-to-end on top of each other to allow connections from a low level of metallization to a high level of metallization without having to jog laterally during the connections.

Q Can you use a via stack for routing both power and ground?

MR. WILSON: Objection; form.
THE WITNESS: It depends on the specifics. If you don't impose any other constraints, conceptually, yes, you could.
BY MS. WEISKOPF:
Q Okay. So you could route ground using a via stack; is that right?
A Conceptually, yes, I agree. Again, it depends on other constraints, but it is certainly possible to route ground with a via stack. I agree.
Q Okay. We talked about this briefly before, but are you familiar with the term "common ground"?
A Sorry. I didn't hear you.
Q Oh. Are you familiar with the term "common ground"?
A I've certainly heard it in different contexts, yes.
Q Does that mean that there's a common ground potential?
A With respect to the specific definition of commonality, in other words, if the context for the common ground is this is the common ground for

block A, then that would indicate that that is the ground point that serves as a reference ideally for everything that's connected to it, putting aside non-idealities.

Q We talked about this before, too. Sometimes you wouldn't want to connect the ground of one circuit to the ground of another circuit because you'd want to isolate them; is that right?

MR. WILSON: Objection; form.

THE WITNESS: I don't remember talking about that before, so perhaps -- I don't recall that discussion. So maybe you can ask the question without referring to that or, if so, you're going to have to point me to what we said earlier. I just don't remember that discussion.

BY MS. WEISKOPF:

Q Okay. I'm sorry about that.

We talked about two different I/O pins for the same common ground potential previously. Do you remember that?

A Okay. That's not quite right. What we talked about was the possibility of having certain chips where you might have two different grounds as I/Os.

Q Those two different grounds could have the same ground potential; is that right?

A In an ideal world I would say yes because you like ground to be reliable and a unipotential. In practice because of ground bounce that may not be exactly the case, but, yeah, ideally they're at the same potential. Ideally ground is ground.

Q Would you refer to those as having a common ground because they're at the same ground potential?

A So it depends on the specifics. It's contextually dependent. If you're defining commonality based on the fact that they are ultimately the same potential, then you could say that's at the common ground potential.

But if, on the other hand, you're using the ground -- the commonality as defined by which circuit blocks they're connected to, then they may not be a common ground. They may be coincidentally at the same potential, but they are not a common ground.

Q Okay. So they have to be connected to the same set of circuitry to be called a common ground; is that right?

A No. In fact, I just gave you the opposite case as well. I gave you the contextually specific answer.

So in my previous answer I gave you both cases. I said if you are defining commonality based on the potential, if they happen to be at the same potential you could say they are at the common ground potential. But, on the other hand, if you are defining commonality based on what they are connected to, then you might say they're coincidentally at the same potential but they are separate grounds.

Q Okay. And either one of those is a way the term "common ground" is used in the industry?

A So, as I said, it's contextually specific. So generally when we're talking about potential, if we say a common ground potential what we mean is that is the potential of the ultimate circuit ground. So that would be the case with respect to the first example that I gave you.

If we are talking about circuit connections, then we are talking about what they're connected to and that would be the second case of what I gave you.

So it's contextually specific.

Q Okay.

A And that's not to say there aren't other contexts. Those are the two that come into my head right now.

Q If you wanted to have separate ground networks that had the same potential you could refer to those as having a common ground; is that right?

A I think it depends on the context. If you are -- it's, again, the same answer that I gave you earlier. If you are defining commonality based on the potential, then if they are at the same potential then by definition they're at the common ground potential.

On the other hand, if you're defining commonality based on the connections, then, no, you would say they coincidentally are at the same potential but it's not a common ground.

It's contextually specific.

(Document was marked Exhibit 1024 for identification.)

BY MS. WEISKOPF:

Q One of the -- I'm going to put another

exhibit in here, in your folder. It's this one called Tai, Exhibit 1024, so I'm going to introduce that exhibit.

Okay. Do you have that one up, Dr. Subramanian?

A I do.

Q And do you recognize this as one of the references that you considered in rendering your declaration?

A I do. I definitely read this before, but I'm trying to see where I cited it in my declaration. And I'm not seeing it cited, but, yes, I have seen this before. I recognize it.

Q Okay. Well, I'd just like to take you to column 1, line 44. And feel free to read the entire background section here just for context if you'd like and let me know when you're done.

A Well, but just ask me the question and then I'll read it once I've decided what I need.

Q Sure. That's no problem.

So I just want to ask some questions about what the -- what, for example, the designs described -- let me start over.

It says "The designs described above

suffer from chip area spacing penalties, in addition to complications in place and route process." I wanted to ask you what that meant and for some examples of that.

A Okay. Give me one second.

Q Of course.

A Okay. I've read it.

Q Okay. So the reference Tai starting at about line 44 says "However, the designs described above suffer from chip area spacing penalties, in addition to complications in place and route process." What is this referring to when it talks about complications in the place and route process?

A So it actually addresses this in the very next sentence. It says "Complications may include dense interconnect and long wire routes, causing antenna violations, capacitive parasitics, and other problem."

Q Let's talk about each one of those, if you don't mind. So the complications may include dense interconnect and long wire routes, can you explain why that's a complication in place and route process?

A Sure. So one of them I already

addressed, which is when you have to provide -- so this is all in reference to the voltage islands. That's what this section is referring to.

When you have to provide multiple different voltages for the different voltage islands you can end up having a lot of wiring associated with the routing associated with that. So that means you've got more wiring, you may have to make your interconnect density higher, which then increases capacitive coupling. It also can mean the wires are long, which means they have more resistance.

Q It says complications may also include causing antenna violations. What does that mean?

A So an antenna violation is a term that's used to -- so there's something called the antenna effect, which is when you have a large net surface area of a metal wire, both during the fabrication of the circuit and afterwards in the operation of the circuit that long, large metal wire, the area of the wire can act like an antenna, and, for example, during the fabrication of the circuit that can be bad because when you're performing etching during the fabrication process nonuniform fields in

the plasma etcher couple into the antenna and they cause the chip to charge up.

So there's often rules on how much wiring you can have that's exposed that's connected to, for example, a single transistor, and that's called an antenna restriction. And an antenna violation would be when you exceed that, and you've exceeded that because your wiring is so large that you ended up with a large exposed area.

Q Okay. Another complication listed here is capacitive parasitics. Can you please explain that complication?

A Sure. Actually, I already addressed this earlier where I said when you have wires that are packed densely close to each other there can be capacitive coupling between them, and that's what this is referring to.

Q Why is that a problem?

A Well, if you have signal lines it tends to slow things down, which is not desirable. It can also cause cross talk.

If you're talking about power and ground lines, it can cause -- so two things can happen. One is there's more dynamic power

consumption. As the capacitors charge and discharge they use power, which is undesirable or it can be undesirable. It's a complication. We know how to deal with it. And then also it can affect the behavior of circuits that are connected to those wires because essentially when the circuits are trying to turn on and off they have to deal with the charge associated with those capacitors.

So the good news is we're able to simulate and deal with all of these, but these are definitely known issues and have been known for decades with respect to routing.

Q Okay. It also has sort of this catchall other problems at the end of the sentence. Are there other problems that you can think of?

MR. WILSON: Objection; form.

THE WITNESS: Well, it doesn't say here, right? I mean, he just says other problem.

So I don't know specifically what Tai had in his or her head when he or she made this statement, but, I mean, the one other thing I can think of which hasn't been explicitly called out off the top of my head, the other concern that you

have is inductance, which is when you have long wires there's inductance associated with them which can have similar detrimental effects to the effects that I mentioned when I discussed capacitance.

BY MS. WEISKOPF:

Q Okay. So why are these complications in the place and route process?

MR. WILSON: Objection; form.

THE WITNESS: So they are complications because they involve trade-offs. You accept that when you make your lines a lot longer they might cause some of these problems. So you have to account for them in your place and route.

What you have to do is either you put in rules, for example, I used to do this, there's a language called SKILL, S-K-I-L-L, that we use in Cadence routing tools anyway, and in SKILL you could write code that sort of said, okay, I'm going to impose a restriction that if I calculate the antenna size to be so much it's going to trigger a violation and when you start adding these things in you have to include that in your SKILL.

We've known how to do this for decades. We've been doing variations on this since

I was a graduate student, and I was a graduate student in the mid 1990s. Probably even before that, I just don't know for sure.

But these are complications, we can deal with it, but it certainly does mean that we have to deal with it.

BY MS. WEISKOPF:

Q There's one other statement here that says there's "Restrictions in localized and global placement and routing, imposed by known dual voltage designs, impede the iterative IC timing convergence process."

Do you see that?

A Yes.

Q What is the iterative IC timing convergence process?

A Okay. So there is something that we do when we do integrated circuit design. It's a standard step. It's called STA, or static timing analysis, something we do routinely.

What you do is when you do your initial design you haven't really fully accounted for the effects of routing on the performance. In other words, let's say you have some part of a

circuit where two signals need to arrive at that circuit at about the same time and if they arrive too far apart the circuit won't work.

We do our initial design without accounting for how the routing might affect the arrival times of those signals. And then what we do is once we finished our design we do a static timing analysis, it's sort of a -- static timing analysis is we make certain assumptions, we sort of say each transistor imposes this much delay, each millimeter of wire imposes this much delay, and we kind of calculate a global delay model and then we say, okay, are we going to have any timing violations, are there any signals that should have arrived at a particular point in time that did not arrive close enough to each other.

And then if the answer is yes, then we have to go fix that and we iterate. So what we do is we say, okay, well, this signal is arriving too late, signal B is arriving too late, so I'm going to delay signal A so that they arrive within the window that I needed them to arrive. And then we iterate and we do it again, and that is what it's referring to in the iterative IC timing convergence

process.

In other words, you find these static timing errors, you modify the design to fix them, then you run it again until you pass with no violations.

Q Okay. We can put this one to the side for now and let's go back to Li, Exhibit 1005.

A Okay.

MS. WEISKOPF: I believe this one has already been introduced as an exhibit.

So I should ask before we get started on Li, does anybody need a break?

THE WITNESS: I think the court reporter would like a break.

MS. WEISKOPF: I think so, too. Do you want to take a five-minute break?

THE REPORTER: Yes, please.

MS. WEISKOPF: Okay. Let's do that then. Thank you.

(Whereupon, a recess was taken.)

MS. WEISKOPF: Let's go back on the record then.

BY MS. WEISKOPF:

Q Dr. Subramanian, we were just about to start talking about Exhibit 1005, which is the Li reference. Do you recognize this reference as one of the ones that you've relied on in your declaration?

A Yes.

Q Okay. So Li describes a BCM1280 chip; is that right?

A Yes.

Q Okay. At the very beginning here at the summary it's talking about the first sentence says "A unique LVS (layout-versus-schematic) methodology has been developed."

What is a layout-versus-schematic?

A So in the design of integrated circuits the layout is the graphical specification of the transistor and sort of component connections. the -- sorry. That's the schematic. The layout is the definition of the pattern files to make the masks that would be used then to fabricate the circuit.

Both of those involve some handwork and some computer-based work, and the computer-based -- I mean, the handwork is still

done on a computer but it's sort of manually input, and there is a risk, therefore, of errors where you make a mistake and your layout doesn't exactly match what the schematic requires. In other words, if you were to build the chip based on the layout what you'd get wouldn't match exactly what the schematic thought you would get.

So layout-versus-schematic is essentially a technique implemented in software typically where we take the layout and we back-calculate what is the schematic associated with it and then we compare that to the original schematic, and in an ideal world if there's no errors they match up.

Q So it says here next "The chip is migrated from its previous generation."

Does that mean that they reused the design of the prior chip?

A So I think the answer is no, they didn't reuse it all, but they certainly reused parts of it. I think that's what this means.

Q Okay. It says "Due to the design reuse, VDD and GND are designed as global nets but they are not globally connected across the entire chip."

Do you see that?

A Yes.

Q What does that mean?

A So what this is saying is that VDD is referring to one of the power supply lines and GND refers to ground, it says they are designed to be global nets, in other words, they are globally available across the chip, but they are not connected across the entire chip and specifically, you know, as you'll see later in this, there are local VDDs, for example.

Q Is a net a mesh?

A So it depends on the context. The term "net" is often used to describe a mesh, but, in fact, in this particular sentence what this is referring to is actually sort of the electrical description of net where when we sort of describe nets while talking about power supplies or power supply routing the net is the term used to describe the routing architecture associated with a particular power supply level.

So when it says VDD net, that's the network. In other words, the connection of interconnects that provide VDD. And ground net

would be the connection of interconnects that provide ground. And if you had a clock net, it would be the same thing for the clock signal.

Q Let's turn to the next page, 491. So starting with the full paragraph on this page, kind of towards the end of that paragraph it says "Each core is isolated from the others by a triple-well."

Do you see that?

A I think you read -- didn't read it quite right. You mean "Each single core, isolated from the others by a triple-well"?

Q Yes, that's what I mean. Yes, do you see that sentence?

A I do.

Q Okay. Does the triple-well separate each core from the rest of the chip also?

A You mean outside of the -- you mean outside of the other cores? You mean with respect to other parts of the chip?

Q Yes, exactly. Is the core isolated from all other parts of the chip?

A So it depends on the biasing of the triple-well, but the short answer is yes. What will happen is when you have a circuit within a

triple-well when you set the biasing of the intermediate and outdoor wells it will essentially reverse bias one of the well junctions so that the circuit within that well is isolated from everything around it, which would include the other cores but also the other parts of the circuit.

Q Okay. Is that why it refers in the next sentence that each core is now built in a unique voltage region?

A I'm sorry. Where are you reading?

Q Yeah, just right after that, "Each single core, isolated from the others by a triple-well," right after that sentence it says "Therefore, under the full-chip context, each core is now built in a unique voltage region."

Do you see that?

A No, when I flipped forward I lost the page. Which page are you on?

Q Oh. 491.

A Okay. Oh, I see it.

Q What does unique voltage region mean here?

A Well, here what it's referring to in this sentence where it's saying each core is now built

in a unique voltage region, what that means is each core can be addressed at its own voltage because it's in a triple-well.

In other words, since it's in a triple-well you can choose the voltages at which you operate that circuit without regard to how it might affect another circuit near it because it's in its own triple-well, and here the circuits they're referring to specifically are the cores.

Q The next paragraph says "Due to the manual nature of the layout construction." Is that referring to performing the layout manually?

A Yes, but just to be clear, that doesn't mean it's entirely manual. It just means that there's a lot of manual input. And that's certainly true.

Q Okay. Let me just see here. I think we've talked about some of this already. Let's move to 493.

A Okay.

Q Sorry. I'm looking for the place so I can refer you to it.

Okay. Starting at the paragraph that says "Due to the trend of ever increasing die

size," it says "Pads arrayed across the active face of the die."

Do you see that?

A Yes.

Q What is it referring to when it says there's pads arrayed across the active face of the die?

A Okay. So here, firstly, it tells us something about this chip because in the previous paragraph it tells us flip chip technology is chosen for packaging this chip. In flip chip technology what you do is you take the chip, you put pads, depending on the generation of flip chip technology, either arrayed across the entirety of the die or some fraction of the die. You then put solder balls on the pads and you flip the chip over and you connect it to the package.

So that's what this is referring to where it says that those pads arrayed across the active face of the die are used to connect to I/O, power, and ground, and specifically what that is saying is that's how the connections are made between the die and the package for I/O, power, and ground.

Q Are the pads, what's the purposes of the pads?

A The pads are the electrical regions on the die on which solder balls or solder bumps are placed.

Q Okay. Do you know how many pads there are in a flip chip technology?

A Oh, it depends on the specific design. There can be thousands, but there can also be tens. It's design-specific.

Q Okay. Why would you have thousands of pads?

A Well, consider a microprocessor. It has power. It has ground. It has lots of memory input/output connections. It has clocks. It has control signals. There can be thousands of signals.

Q So the pads would correspond to each signal?

A They could. In some cases they are not connected to anything, they're just there, and in other cases they are redundant.

Q What do you mean by "redundant"?

A So in some cases we have multiple pads

that are used for the same signal just because for layout reasons it's convenient to do so or there's some performance reason to do so.

Q Okay. What are those reasons to use redundant pads?

A Well, one of them we already discussed, which is if you want a lower resistance providing multiple pads lowers the overall resistance. The other reason to do it is if you are using the chip in some sort of daisy-chained architecture where there's a signal going into one chip but then it's going to come out of that chip and be fed to another chip, then sometimes having two pads associated with the same signal allows you to daisy-chain more easily on the board.

Q Would that daisy-chain reason apply to power or ground routing?

A Usually, no. I mean, daisy-chaining is used for propagating active signals such as memory input/output signals, for example.

Q Okay. Would you have redundant pads for powering ground to lower the overall resistance?

A It depends on the application but in some cases, yes.

Q Okay. And why is the overall resistance lowered when you have redundant pads?

A The reason it's lowered is you effectively have multiple bumps in parallel with each other. Each bump introduces a little bit of resistance, so by putting them in parallel the overall resistance drops.

Q Let's move to figure 3, which we've talked about briefly. Have you gotten to figure 3?

A I have.

Q So it uses a whole bunch of gray colors, so I'd just like to make sure we're both on the same page about what figure 3 is showing. We have a key to the right which has a bump which is this sort of polygon. We have a redistribution metal layer which has got these diagonal lines across it.

Do you see that?

A Yes.

Q Okay. And there are three lines on the redistribution metal layer that are shown here; is that right?

A You mean on the figure?

Q Yeah, the figure. Exactly.

A You mean not in the key. Yes, I agree,

there is two horizontal and one vertical shown in the RDL.

Q Okay. Then the next thing we see in the key is this via-6 which is a square with crosshatching. Does that -- do you agree?

A Yes.

Q Okay. And so we're seeing -- you can see one, two, three, four, five, six, seven via-6s in figure 3; is that right?

A Yes.

Q That's the only via that's being shown in figure 3; is that right?

A That's right.

Q And that via-6 connects the metal-7 and metal-6 layers; is that right?

A Yes, I agree.

Q So now here's where we get to the complicated part. There's metal-7, which is kind of a darker gray color, and there's metal-6, which is a lighter gray color in the key. Do you agree with that?

A I do.

Q Do you agree that the metal-7 wires are horizontal?

A Yes.
Q So all the metal-7 wires is a horizontal, darker gray wires; is that right?
A Yes.
Q Okay. And then the metal-6 wires are all vertical wires; is that right?
A Yes.
Q Okay. So let's put aside the redistribution layer. Besides that, the all horizontal wires in figure 3 are on metal-7; is that right?
A Yes.
Q Okay. And putting aside the redistribution layer, all vertical wires in figure 3 are on metal-6; is that right?
A Yes.
Q Okay. So I want to go back to talking about the triple-well. Actually, let me ask you another question about figure 3.
We talked about three wires here on the redistribution layer, but there would actually be more than three wires in the actual chip, right?
A You mean over the entirety of the chip?
Q Yeah, over the entirety of the chip.

A Oh, yeah, I agree.
Q And there would be more bumps across the entirety of the chip, too; is that right?
A Yes.
Q And the same for metal-6 and metal-7, there would be more wires -- I guess figure 3 isn't actually the entire top three layers of the chip, it's just a little portion of it; is that right?
A It doesn't -- it's not intended to nor does it depict the entirety of the surface area of the chip.
Q Okay. Let's go to 492. I want to ask you some questions about the triple-well technology. So right under section 2 it says "Triple-well technology allows P-wells to be placed inside a deep N-well."
Do you see that, Dr. Subramanian?
A I do.
Q What is triple-well technology?
MR. WILSON: Objection; form.
THE WITNESS: So there are different types of triple-well technology, but the specific triple-well that this section is referring to is actually shown on figure 2, which is at the top of

page 493, where you see that there is for the NMOS device in the triple-well it's got a well that's labeled -- by the way, the devices we're talking about are in the triple-well are on the right side of this figure, okay?

So the NMOS device is in the P-well, the PMOS device is in the N-well, and they are both in a deep N-well. And importantly, the deep N-well is in a P-substrate.

Now, what that means is there is a diode between the deep N-well and the P-substrate, and if you keep the substrate potential lower than -- as the lowest potential in the circuit, then that diode is always reverse biased and so that effectively isolates any transistors built within the deep N-well from interacting with anything outside that N-well.

That's the triple-well technology.

BY MS. WEISKOPF:

Q And this technology allows the core to be disabled when it's not needed; is that right?

A It is true that -- so it is true that that's one of the things you can do, but it's not the only thing you can do.

So it actually goes on to say this. What it says is this allows you to essentially put a back bias on the regions that are not operating. What that does is that effectively increases the threshold voltage of the transistors in that region and that means, A, they don't turn on in normal operating voltages, they require high voltages which we're not providing, and, B, it actually saves energy because when you increase the threshold voltage of a transistor you reduce its leakage power.

Q Figure 2 has something labeled GND2 and another area labeled GND1. Why are those labeled GND1 and GND2?

A The reason they are labeled that way is because the GND1 is in a circuit that's outside the triple-well and GND2 is for a circuit that's inside the triple-well. It's just to show that because you have the triple-well you have the possibility of preventing cross talk between those transistors.

So and specifically the transistor with the GND1 is an NMOS transistor and the transistor with the GND2 is also an NMOS transistor, but because the right one is inside the

triple-well it is electrically isolated from the transistor on the left.

Q Okay. Let's look at figure 4. So we looked at this before, and this shows you a substrate ground on the far left. What is the substrate ground?

A So the substrate ground here is referring to the ground connection that is made to the overall substrate.

So if you go back to figure 2, you see how it shows a P-substrate. Somewhere on the chip, in fact, typically in multiple points on the chip, you have vias that drop down from the interconnect stack through the various interconnects to ultimately make a connection to the substrate, and that allows you to bias the substrate.

I told you earlier when I was describing P-wells that what you do to make the P-well provide isolation is you make sure that the bias on the substrate is the lowest potential in the circuit, which in this case the lowest potential in the circuit is ground, so if you connect it to ground all the wells get isolated.

So that's what that is referring to.

The substrate ground is the connection that is provided to the substrate to -- to ensure that the substrate is at the lowest potential. That connection is still provided through the interconnect stack. It's just through an interconnect stack that ultimately has a via that drops down to the substrate.

Q Okay. Let's go back to figure 4. We talked about this power switch that's intervening between the substrate ground and the core; is that right?

A Yes.

Q Okay. And then on the other side of the switch you have something called core ground.

Do you see that?

A Yes.

Q What is the core ground?

A In this case the core ground is referring to the ground that is provided for the well of the transistors within a particular well, and in this particular case because it's told us that the cores are implemented inside wells this is the connection to the ground for the cores.

Q Okay. At the bottom of 494, the last

carryover paragraph says "A power switch structure is designed surrounding each core."

Do you see that?

A Yes.

Q What does that mean?

A So what this is basically saying is that it is possible to -- it tells us that in the next -- in two sentences down. It says "The power switch enables a single core to be turned on or off individually."

So that's what it's referring to.

Q For it to be turned on or off individually does all ground have to come through the switch?

MR. WILSON: Objection; form.

THE WITNESS: Could you repeat the question, please?

BY MS. WEISKOPF:

Q Sure. In order to turn off the ground to the core does all ground have to be routed through the switch?

A No. Specifically what has to be done is for a particular core the P-wells inside the triple-wells are connected through that ground, and

it says that specifically at the bottom of paragraph -- the first paragraph of 4.1. It says "As a result, BCM1280 has a total of four core grounds connected to the P-wells inside the four triple-wells, respectively, and one chip ground connected to the P-substrate."

So that's what it's telling us.

Q So help me understand why the ground doesn't need to be routed through the switch based on that language.

MR. WILSON: Objection; form.

THE WITNESS: Actually, that isn't what I said. Certain grounds are routed through it, just not all of them. It tells us which ones they are. It says it explicitly. It says that the four core grounds are connected to the P-wells inside the four triple-wells. So that means for each ground -- for each core its P-wells are connected to that core ground.

When we turn off that switch -- so just to be clear, when we turn on that switch what it does is it connects the P-well ground off the triple-well to the substrate. What that does is that turns off any back bias. You remember earlier

I pointed to the language on back bias. It turns off any back bias on the transistors in that well, which then means we are able to operate the transistors but, correspondingly, leakage current has gone up.

When we turn off the power switch we are turning off the P-well to substrate -- sorry, P-well ground to substrate ground connection, which means now the back bias can be applied which is used to raise the threshold of the transistors which turns them off and also suppresses leakage.

BY MS. WEISKOPF:

Q Does the core have the P-well inside of it?

A Yes, for the NMOS transistors each -- inside a core each of them has its own P-well. You can see that if you look at figure 2. If you look at figure 2, let's assume the right side is a part of a core and you'll see that there's a P-well for the NMOS transistor in there. That's what that's referring to.

Q In figure 2 where is the switch?

A It doesn't show the switch, but figure 4 tells us that the switch would be connected between

the core P-well and the chip P-well, right?

It says that -- where was it -- yes, so it says "has four core grounds connected to the P-wells inside the four triple-wells." So what we would have is the core ground is connected to the P-well that's -- actually, that has the connection GND2, okay?

And then the chip ground is actually it could either be through the connection to GND1 or it can actually be a connection that goes through a via that isn't shown onto the P-substrate, it's not visible in this figure, and then the switch connects those two together or it can connect those two together when it's on.

Q Okay. So let's look at figure 2 because I don't really understand. So inside the deep N-well is the core; is that right?

A This is a core, yes. I mean, that's -- this is a generic structure. Elsewhere it tells us that the cores are built inside triple-wells, but this is only showing two transistors so it's clearly not the entire core.

Q Okay. Let's just use it as a representation so I can understand what you're

saying. So let's assume that this core is inside the deep N-well.

Is that a fair assumption?

A Sure.

Q Okay. Where is the switch located?

A The switch will be connected -- so it's not here. The switch will be in its own triple-well, but it will be connected -- the drain of the switch will connect to GND2 and the source of the switch, if I've got that right, will be connected to the well connection, which can be done through GND1 or more likely, just for routing reasons, there will be a separate substrate connection somewhere else on the chip that isn't shown in this figure.

Q Okay. The ground that is going to be provided to the core inside the deep N-well needs to be routed through the switch; is that right?

A So if we are implementing the power switch scheme of figure 4, the ground, and it's not just any ground, it's specifically the core ground which is called out as the connection to the P-wells, off the P-wells inside the triple-well.

So that in figure 2 is GND2 because

you can see GND2 is connected to the P-well inside the triple-well. So the switch -- one side of the switch will connect to that.

Q Okay. In order to be able to turn the switch on or off and turn the core on or off, all ground going into the core needs to be routed through the switch; is that right?

MR. WILSON: Objection; form.

THE WITNESS: No. Again, I already answered this, but I'll answer it again.

Specifically, to turn this core off what you want to do is you want to prevent current flow from the core, and specifically this calls out specifically that you want to use back bias to suppress leakage current. So the way you can do that is the P-wells grounds of the core come out through GND2. Those are routed through the switch. When that switch is turned off, GND2 no longer has a ground path if there is a switch between GND2 and the substrate ground, which is what is shown in figure 4.

BY MS. WEISKOPF:

Q Okay. Is there another ground path going into the core besides the switch?

A It actually doesn't say. There could be or there could not be. It doesn't matter for the purposes of the power-gating because the power-gating is implemented using the P-wells, which is what I pointed out.

Actually, this document is silent as to whether there are other ground paths, but you still get the power-gating to work because of this one.

Q Okay. Dr. Subramanian, here's where I'm confused. If you have other ground paths going into the core then you're not able to use the back bias, are you?

A That's not true. That's categorically wrong. You absolutely can. As long as your P-wells -- the P-wells that you're back biasing are not connected to that ground, you absolutely can use back biasing.

Q So I think your point is that the ground is in the P-well and that's what's being connected to the switch; am I understanding correctly?

MR. WILSON: Objection; form.

THE WITNESS: So with respect to the ground that is used for the power switch

architecture, it is true that the grounds that are on one side of the power switch are within the P-wells inside the triple-well. That's what this document says.

BY MS. WEISKOPF:

Q I understand. That's why you were making the P-well distinction; is that right?

MR. WILSON: Objection; form.

THE WITNESS: No, I'm making that point because that's how the circuit operates.

BY MS. WEISKOPF:

Q Okay. I understand.

A It tells us that explicitly.

Q Okay. But in figure 2 there's no other ground routing disclosed; is that right?

A I agree within the wells the only -- within the triple-well the only ground that's shown is GND2. I agree with that. As I told you in my previous answer, it's silent as to whether there are other grounds.

Q Okay. So I'd like to understand how strong the global mesh and the local grids all the way down to the circuitry here in the core, I'd like to understand how you believe the connections

to ground are made, and it may be easiest to draw a picture but perhaps you could just describe in words what the ground routing structure looks like.

A Sure. I don't think we need a picture or maybe -- I'll try without a picture because I actually think the figures of Li are pretty good in this respect.

So, first, let's begin by starting at the global mesh. So if we look at figure 3 we see that there are ground lines that are provided and they are indeed routed within the global mesh which I've told you is formed using metal-6 and metal-7.

There are, of course, four -- five layers of metal below that, in other words, metal-1 through metal-5, and those are used then -- in fact, it tells us on page 493, it tells us the power and ground lines in the local sections are it says "grided" but it should be gridded on metals-2 through 5 on which the local power grids are formed at the block level.

So, in other words, we have the global mesh on 6 and 7, we have the local meshes on 2 through 5, and we've been specifically told that the local meshes also provide the relevant power

and ground lines. And the local meshes are at a block level, and so we've seen the blocks. If we look at figure 1, we see a chip detailed floor plan and we see cores and we see the switch, for example, and so those are different blocks.

And then we are told that the blocks in the specific example is for the cores, but as I told you earlier it's possible to gate anything provided it's in a triple-well, the cores are -- are -- it's possible to turn them off using the power-gating architecture that we've just been discussing.

So that's the overall routing architecture.

Q Okay. So I understand that it goes in your opinion from the global mesh there would be a ground wire, but I don't understand where that ground wire goes next. Where does the ground wire connect to next after it's -- you know, we've got a via that's dropping down from the global mesh. What's your opinion about where that wire goes next?

A Actually, Li gives us guidance on that because there's two things Li told us. I just read

you language where Li says the local meshes are gridded at the block level. We also know, now let's say specifically we are talking about a core and a core is something we want to turn off, as an example, we also know the way that the core is architected for turning it off is there is a power switch such as that shown in figure 4 that lives between the global ground, so the substrate ground, and the -- the core ground, and it's called out as the core ground on figure 4.

So where that would live is we would have routing from the global mesh through a power switch to a local mesh. The local mesh then provides ground to, for example, all the P-wells on the triple-well associated with that core.

Q Okay. So it's sort of -- I think I understand. You're saying it's global ground drops down to the switch in the substrate and then it goes back up to a local grid; is that right?

MR. WILSON: Objection; form.

THE WITNESS: So it's the global ground -- or the grounds within the global mesh to provide the power-gating for a particular core will have a sleep transistor -- as I told you earlier,

the transistors are all implemented in the silicon, so there's no transistors in the interconnect -- and then that one side of the sleep transistor is connected to a ground in the global mesh.

The other side of the sleep transistor is connected to the ground for the P-wells off the particular triple-well associated with the particular core we are talking about. Those grounds are in the relevant local mesh for the particular core we are talking about, and then those provide the ground and, of course, power for the relevant core.

BY MS. WEISKOPF:

Q Okay. Let's see if I can understand. The ground from the global drops down to the silicon transistor, it goes through the power switch, and then it goes up to a local grid on 2 through 5, metal layers 2 through 5; is that right?

A Yes, but to be clear, the global mesh side is on one side of the transistor, the local mesh side is on the other side of the transistor as shown in figure 4.

Q Okay. Does the power switch require a voltage to operate?

A You mean -- you're asking me to turn it on and off?

Q Yeah, exactly. Does the power switch need a power supply?

A Yes. To turn it on and off, yes. It tells us in -- on section 4.2 -- was it 4.2? It was somewhere where it said it was an NMOS transistor.

Well, it's somewhere where I found it earlier and I told you about it earlier, but let me find it.

Yep. Okay. In section 4.2 it says it's an NMOS switch. We also -- I told you earlier that figure 4, the diagram looks like an NMOS switch, so an NMOS switch to turn it on you apply a voltage -- a positive voltage more than the threshold voltage to the enable terminal on figure 4.

Q Okay. Do we know from the disclosure of Li whether it's receiving VDD -- which VDD it's receiving?

A We don't, but, actually, it turns out it won't matter. And the reason it won't matter is because both VDDs are higher than -- are by

definition higher than the threshold voltage so the switch will turn on.

This is being used as a switch, so it will work as long as you drive it hard enough.

Q So let's just go back to figure 2, make sure I understand. We've got our P-well inside of our deep N-well, and is the local grid covering the P-well and providing ground throughout the P-well or is it extending beyond that?

A It's both because it tells us the local grid is gridded at a block level. The block is the entire core, which includes both P-wells and N-wells within a given -- within a given triple-well.

Q Okay. So in your opinion the local grid that's over the deep N-well would be providing the ground to anything in the P-well and anything in the N-well that needed ground?

A Within said deep N-well, yes.

Q Within the deep N-well, exactly. Do we agree on that?

A Yes.

Q Okay. If there were another ground connection to that local grid through a direct

connection to the global mesh would that bypass the switch?

A I don't know how to answer that. I think -- so the switch is still in series with the P-wells. So to that extent, it's not bypassing the switch.

If you're asking me does it provide a ground potential other than that that would be passed through the switch, the answer is yes, but that doesn't matter because the P-wells still get cut off by the switch.

Q Okay. Yeah, let me try to clarify my question.

So let's just focus purely on the local grid. The ground is routed through the switch, we know that much. If there's another connection that's not up to ground that's not through the switch but is instead to it's called substrate ground, would that bypass the switch?

A Again, my answer is the same. It's a different part.

So the switch is still active, so it's not bypassing the switch in that the P-wells still get cut off by the switch but it does provide a

ground reference and it will provide that ground reference even when the switch is off. But that's okay because the switches are used for cutting off the P-wells such that you suppress leakage current, et cetera.

Q Okay. If the P-well is receiving ground through the switch and then also from a different substrate ground will the switch work?

A It can't do that. There's -- you can see there that there's a single ground connection.

Q Okay.

A So it's not set up -- for any given P-well it's telling us the P-well grounds go through the switch, but you can have other grounds that are not related to the power-gating but the power-gating is implemented through these P-well grounds.

Q Okay. I think where I'm confused is what you mean by these other grounds. Can you explain that to me? That's where I'm getting -- that's where I'm not sure what you're talking about.

A Sure. So I told you earlier that Li is silent as to whether there are other grounds inside the well. What Li says is the power-gating is

implemented through the switch that cuts off these P-wells from the substrate ground.

So it's silent as to whether there are other grounds. It is possible there are other grounds, Li doesn't say anything, but they don't interfere with the power-gating because the cutoff is still achieved using the switches that we've been discussing.

Q And that's where I'm confused, Dr. Subramanian, because if you're getting ground from a different source the cutoff wouldn't seem to matter.

A That's, unfortunately, not correct.

Q Yes. Can you explain? Can you --

A Yes. Sorry. I apologize. I spoke over you.

I'll explain it again. It tells us that the cutoff for the power-gating is through the ground connection of the P-wells. That's what figure 4 is about. If there are other grounds within the core, that does not affect that because the cutoff is still achieved using those.

For example, you can have other grounds that are used to provide reference

potentials for arithmetic logic units, et cetera, they still will get cut off because the P-well ground gets cut off.

But, again, Li is silent as to whether there are other grounds or not. We just don't know. I'm just saying there could be other grounds and it wouldn't affect the operation because the P-well cutoff still works.

Q I think my confusion maybe is that it seems as if the reason that there's disabling is because there's no ground provided. Is that an incorrect assumption?

A Well, if you're assuming that globally then, yes, it's an incorrect assumption. The reason there's disabling is when you -- it's you are removing the ground connection to the P-wells that are associated with implementing the relevant circuitry within the core affiliated with the cutoff, and what that then allows is back bias to raise the threshold voltages, et cetera.

That does not mean there cannot be other ground signals in there. They're just not associated with the cutoff operation.

Q Would the core be disabled if there were

other grounds and other operations going on in the core?

A So separate things. Yes, there can be other grounds in the core, but the basic idea is that you can turn off the core.

So there wouldn't be operations, but there can still be other grounds in there. They're just not being used.

Q Is there any reason to do that?

A Sure. I gave you one earlier where I said it can provide a reference potential, for example, for particular calculations where you need a ground.

Q For that to be disabled then you'd need to not be providing voltage; is that right?

A No, that's not true.

Q Would it still be consuming power if you provided voltage?

A Not appreciable power. That's the whole point of this back biasing scheme. What it does is when you disconnect the P-well ground it allows you to back bias those transistors so that the threshold voltage of those transistors rises, which suppresses leakage current for not just those

transistors but any transistors that are upstream of them.

Q I see. I understand what you're saying now. You're saying that it's like -- it's the -- it is a control center for the ground so that if it's cut off at the P-well it's not -- there's no ground being provided throughout the rest of the circuitry?

A No, that's not what I said.

Q Okay. I'm honestly confused. If you could just explain it again, I would appreciate it.

A Sure. I'm trying.

Again, the switch cuts off the P-well ground from the substrate ground. What that does is that allows you to then use back biasing to raise the threshold voltage of the NMOS transistors in the P-wells within the core affiliated with that triple-well such that there is no current flow through those transistors and, indeed, leakage gets suppressed because the threshold voltage rises.

There may be other ground connections inside the circuit, but they don't matter because the transistors that are switching -- or switching of the circuit is now suppressed because the NMOS

transistors are turned off due to the back biasing.

Q Okay. Well, let's move on and then I may have to come back to this because I still don't understand.

Let's go to your declaration.

A Okay.

Q So, I mean, it's pretty organized, Dr. Subramanian, and so I just want to go through the basic organization to make sure we're on the same page with that very quickly.

So with respect to grounds 1 and 2, I understand that your opinions are in paragraphs 71 through 121. Would you just confirm that for me?

MR. WILSON: Objection; form.

THE WITNESS: So the detailed claim-by-claim element analysis of grounds 1 and 2 are between the paragraphs 71 and 121, recognizing, of course, that I provide more information about the relevant art in other sections, for example, the sections that precede that.

BY MS. WEISKOPF:

Q Okay. Maybe my question is going to be related to are you relying on anything under grounds 3, 4, or 5 for your opinions on grounds 1

and 2?

A So given that grounds 3, 4, and 5 in various places, particularly ground 3, for example, discusses more details of Jiang, statements that I apply in those grounds may be equally applicable to grounds 1 and 2. And so if I'm discussing a particular aspect of Jiang or a particular reason for my opinion for Jiang and I specifically mention it in my text in ground 3, it would still be applicable to the same argumentation in grounds 1 and 2.

But in general what I've tried to do as much as possible is I tried to provide the analysis in the relevant sections, but, I mean, what's more relevant is the specific text where I say Jiang indicates this or one of skill would know this and if I make that statement about Jiang or about what one of skill would know in ground 3, if it's discussing an issue that's relevant to ground 1 and 2 it would apply to that equally.

Q Okay. Anything else from grounds -- the other grounds that I should be aware of would apply to grounds 1 and 2?

MR. WILSON: Objection; form.

THE WITNESS: Well, again, my answer is the same.

In other words, my report is -- I stand by my report except for that one correction that I gave you where there was a typo. So to that extent, if I make a particular statement and I say this is what one of skill would know, that would be true whether it applies to ground 1, 2, 3, so on and so forth.

Similarly, if I make a statement about a piece of art where I say Jiang teaches this or Li teaches this, that would be true whether it's applied to a reference that uses Li as the primary or a reference that uses Li as the secondary or vice versa.

So that's sort of my position on it. But I've tried to be clear about it and I've tried to organize things, but if I make a statement about a piece of art that's going to be true no matter which section it's in.

BY MS. WEISKOPF:

Q Okay. But you've provided the reasoning for your opinions regarding grounds 1 and 2 in the sections labeled grounds 1 and 2; is that right?

A So in terms of my element-by-element analysis, yes, I've tried to provide those reasonings there, but, to be clear, since I do use the same pieces of art in multiple grounds, statements that I make about that art would be applicable no matter which ground they're in or, correspondingly, if I make a statement about what one of skill would reasonably know or understand that would be applicable no matter which ground they're in.

Q So I'm trying to understand if like you've sort of scattered around the reasoning for grounds 1 and 2 in the other grounds. Did you do that?

MR. WILSON: Objection; form.

THE WITNESS: Okay. So as I said earlier, I've tried to provide the element-by-element analysis under each of the subheadings for each ground.

Having said that, if by "scattered" you're including the possibility that I may make a statement about what one of skill would know in the text for one ground and it would be equally applicable in another ground, the answer is

necessarily, yes, if I'm making a statement about what one of skill would know that should be true -- for consistency that should be true no matter which ground it's in.

BY MS. WEISKOPF:

Q So if I'm trying to understand your opinions related to grounds 1 and 2 I need to consult grounds 3, 4, and 5 for all of the statements that you've made about the reference and try to figure out if they apply; is that what you're saying?

MR. WILSON: Objection; form.

THE WITNESS: That's not what I said. So I told you what I just said.

I'm happy to repeat it, which is what I said was I've tried to put all my analysis for grounds 1 and 2 on the element-by-element basis within grounds 1 and 2. However, if I make a statement in another ground about a particular piece of art that is true because I'm describing a particular piece of art, that statement would be true whether it's in ground 1, 2, 3, et cetera, because I'm talking about a piece of art. So which ground it shows up in doesn't change the

characterization of the art.

Similarly, if I make a statement about what one of skill should know, that also should be the same independent of which piece of art I'm performing the analysis for because it's describing what one of skill should know or would be reasonably expected to know.

BY MS. WEISKOPF:

Q Okay. If I'm working on addressing grounds 1 and 2, and I'm trying to address grounds 1 and 2, do I need to go through grounds 3, 4, and 5 and try to determine whether or not anything you've said in those grounds supports your opinions regarding grounds 1 and 2?

MR. WILSON: Objection; form.

THE WITNESS: I don't know how to tell you how you're supposed to do your work. I'm just telling you the realities of if I make a statement about a particular ground or about what a POSITA should know, that should be a true statement independent of which ground it's being considered for. In fact, if that were not the case it means I'm being not consistent with myself.

So if I make a statement about what a

POSITA should reasonably know, that should be through independent of ground.

BY MS. WEISKOPF:

Q Okay. The reasoning that you've applied to reach your opinions on grounds 1 and 2 is contained in the paragraphs related to grounds 1 and 2; is that right?

MR. WILSON: Objection; form.

THE WITNESS: Again, with respect to the element-by-element analysis, yes, I've tried to highlight that all in the statements associated with grounds or in the sections associated with grounds 1 and 2.

Having said that, as I pointed out earlier, there are other statements in other parts, for example, there is the summary of the art that shows up before the paragraphs we talked about and then I have made statements about what one of skill would reasonably know, and those statements should stand on their own independent of which ground they are in.

In other words, if I take a position that one of skill should reasonably know how to do X, that should be true whether it's in ground 1,

ground 2, ground 3, et cetera.
BY MS. WEISKOPF:
Q So there's reasoning in grounds 3, 4, and 5 that applies to grounds 1 and 2?
MR. WILSON: Objection; mischaracterizes his testimony and asked and answered.
BY MS. WEISKOPF:
Q I don't know the answer, so if you could just be more clear about your answer. Is there reasoning in grounds 3, 4, and 5 that applies to your opinions regarding grounds 1 and 2?
MR. WILSON: Objection; asked and answered.
THE WITNESS: So, again, I will answer this again. So within -- the text for grounds 1 and 2 I've tried to provide the details of the element-by-element analysis that I've provided and I believe you said that's between paragraphs 71 and 121.
Having said that, there's certainly descriptions of the arts that appear before that, which would obviously be relevant. In addition, if I made any statements anywhere within this declaration about -- that are categorical

statements, such as this is what one of skill would reasonably be expected to know or this is what this piece of art discloses, that is a statement that is true independent of which ground it's in.

In other words, if I take a position that Jiang discloses X, I believe that to be true whether it's in ground 1, 2, or any ground that's referring to Jiang, and, correspondingly, if I make a statement that one of skill would reasonably be expected to know Y, that should also be true independent of which grounds it's in. If that were not true, that would mean that I was being internally inconsistent.

BY MS. WEISKOPF:

Q I understand that you're saying your opinions are consistent, but the answer is not responsive to the question I'm asking, which is all the reasoning that's supports your opinion regarding grounds 1 and 2 has been provided for grounds 1 and 2. I'm not understanding why we can't agree on that.

MR. WILSON: Objection; asked and answered.

THE WITNESS: Again, I can't say why --

why you're not agreeing with me, I mean, that's obviously not my job to read into your mind, but the short answer is, firstly, on its own that statement is not correct because at the very least I provided characterization of the art outside those sections, right? I provided characterization of the art in the paragraphs before paragraph 71.

And so certainly when analyzing my opinions about Jiang, for example, you would want to look not just at the sections that perform the element-by-element analysis of Jiang but also my general characterization of Jiang which shows up earlier.

And, having said that, if I'm providing opinions related to what one of skill in the art would know, when I make a statement about what one of skill in the art should know that should be and for me is true independent of which ground I put it in. So that doesn't change the facts.

BY MS. WEISKOPF:

Q I think I'm specifically asking a question about your reasoning, not necessarily your characterization of the art.

MR. WILSON: Objection; form.
BY MS. WEISKOPF:
Q So putting aside your characterization of the art, is the reasoning that supports your opinion regarding grounds 1 and 2 spelled out in the paragraphs related to grounds 1 and 2 in your declaration?
MR. WILSON: Objection; asked and answered.
THE WITNESS: Okay. So putting aside the characterization of the art, as I said, so the characterization of the art appears in various parts, which I've just discussed in my previous answer.
The other point that I made is if I make a statement about what one of skill should know or could reasonably be expected to know, that also will be true independent of the particular ground. So that's the other example that I gave you of a situation where it would be true no matter which ground you're in.
BY MS. WEISKOPF:
Q Okay. Any other pieces of reasoning that might be scattered throughout the entire

declaration that relates to grounds 1 and 2?

MR. WILSON: Objection; form.

THE WITNESS: I couldn't say specifically. As I said, I've done my best to try to keep things organized. I've given you two caveats.

I mean, the general point I'm making is if I make a statement that is independent of a particular ground, in other words, it should be true no matter what ground you're in, those statements would apply no matter what. The two examples I've given you are the ones that I can think of right now, which is any statement about the characterization of the art or any statements about what one of skill could be reasonably expected to know or would know or would think.

BY MS. WEISKOPF:

Q Okay. And those types of statements apply to all grounds; is that right?

A Yes, I would expect so. I mean -- if I make a statement saying one of skill should think this, that should not depend on the ground. If it did, it means I was being internally inconsistent.

Q Let's turn to paragraph 74 to 76.

A Okay.
Q So these appear to be paragraphs relevant to your opinions regarding element 12[a]; is that right?
A Yes, I agree. These are in relation to the limitation 12[a].
Q Okay. So in paragraph 76 you've annotated the Jiang figure 1(b).
Do you see that?
A I do.
Q Okay. Jiang figure 1(b) has got one power VDD; is that right?
A You mean on the figure?
Q Yeah, the figure shows one power VDD?
A I agree. I mean, there's two connections to it, but, yes, they're both VDD.
Q Okay. And the current can flow through any wire on L1; is that right?
A I don't know what you mean by that.
Q Is there current associated with the VDD voltage?
A Oh, you're asking me specifically about VDD?
Q Yeah.

A Okay. So the current associated with -- the current being drawn from VDD could flow through any wire in the mesh that is connected to the VDD provisioned wiring; in other words, the parts of the mesh that are providing VDD.

Q And it can also flow through any of the vias connected to the top L1 grid?

MR. WILSON: Objection; form.

THE WITNESS: Again, not just any vias, but any vias that are providing the -- that are connected to wires or interconnects that are providing VDD.

BY MS. WEISKOPF:

Q You've got this orange color that says "not interconnected."

Do you see that?

A Yes.

Q What does that mean?

A Oh. Here what I'm just showing is that you can see that the individual structures that I identify as the local power meshes are not shown with any wiring running between them. So, in other words, there's no wiring shown running from the local power mesh above B to the local power mesh

above A, so on and so forth.

Q Okay. But you would agree that the meshes on L2 are interconnected through the global mesh to one another; is that right?

A In the situation, for example, let's take the case of the mesh above D -- the local mesh above D and the local mesh above A. While the local meshes themselves are not wired to each other and have no wires that run across them, it's true that at least with respect to A and D because they connect up to the -- they connect up to the -- the global mesh and would share the same VDD voltage there will be VDD that flows to both of them through wiring that connects them in the global mesh.

Q So do you agree that those local meshes on L2 are interconnected through the global mesh?

A With respect to A and D, which do not have sleep transistors shown, if we define interconnection as being interconnection through the global mesh, in other words, we have the possibility of current -- of having an electrical conductor connecting A through D through the global mesh, I agree at least with respect to A and D that

that is true.

Q Okay. If the sleep transistors are on would they also be interconnected with the other meshes on L2 through the global mesh?

MR. WILSON: Objection; form.

THE WITNESS: I think I understand. In the situation where the sleep transistors respectively associated with B and C are in the on state there will be a conductive path running from, for example, B through the sleep transistor up to the global mesh; there will be conductive paths within the global mesh that will then run to the top of the sleep transistor associated with D -- sorry, associated with C; assuming the C sleep transistor is on there will then be a current path through that transistor to the local mesh associated with C.

BY MS. WEISKOPF:

Q And the same is true with A and D also, if the sleep transistors are on they are also -- A and D meshes on L2 are also interconnected with B and C meshes on L2?

MR. WILSON: Objection; form.

THE WITNESS: So just to be clear, I

don't think you mean they're interconnected directly. I think what you mean is there's a current path possible from A -- if the sleep transistors in B and C are on, there's a current path possible through the sleep transistors that essentially allows an equipotential induced by the fact that the sleep transistors are on such that there's a current path through the sleep transistors from the global mesh to A, to B, to C, and to D local meshes, and also because the global mesh has wiring running horizontally and vertically for at least its VDD lines that means that VDD going to the global mesh A would have a path through one sleep transistor to B, through one sleep transistor to C, through the global mesh to D, and so on for all the other local meshes.

BY MS. WEISKOPF:

Q Yes. So in the way that you just described all of the meshes on L2 are interconnected through the global mesh; is that right?

MR. WILSON: Objection; form.

THE WITNESS: So, again, as I said, interconnected to the local meshes is not the right

way to describe it because they are not interconnected through the local meshes, but there are paths through the global mesh when the sleep transistors are on that would allow an equipotential, for example, between A and B, A and C, A and D, B and C, B and D, and C and D. And I think I've covered all the combinations.

BY MS. WEISKOPF:

Q So you're drawing a distinction when I say interconnected there's some sort of direct connection between two meshes; is that right?

A So the distinction I drew was I wanted to be clear that I am not agreeing and I think it's incorrect to say that there is wiring, for example, running in the orange regions that I show on 39.

Q I see. Okay. It's all through the global mesh on L1; is that right?

A Any current flow paths that will achieve the equipotentials, for example, with respect to VDD on the local meshes associated with A, B, C, and D are caused by and exist because of the global mesh connections, and that's assuming the sleep transistors are on.

Q Okay. There are no concerns about

shorting in the L1 grid because all the wires there are the same voltage potential; is that right?

MR. WILSON: Objection; form.

THE WITNESS: I'm sorry. I have no idea what you mean by that question.

BY MS. WEISKOPF:

Q Well, the wires are crossed, do you agree with that, in L1?

A Yes, but they are in different layers. You can see that on the very next figure, figure 10.

Q Okay. Let's just look at what 1(b) shows, though, which just shows one L1 with crossed wires. If that is one layer there would be no concerns with shorting because it's all one VDD. Do you agree with that?

A It's not one layer. That's just wrong. Those are called levels, level 1 and level 2, and the specific description of them is shown in the power mesh granularity figure in Figure 10.

Q I understand that's your position. We're doing a hypothetical. That's not your position. Not your position. This is one layer. Even though they're crossed, there's no concern about shorting

because they're all the same voltage potential; is that right?

MR. WILSON: Objection; form.

THE WITNESS: That's also incorrect. The reason you know that's incorrect is if you look at Jiang, and specifically we recognize that Jiang has more -- well, firstly, Jiang is an integrated circuit, so it has more than just power and ground. It has signal lines as well.

If it was all one layer all the signal lines would be shorted to the power lines would be shorted to the ground lines, so you absolutely would have concerns.

BY MS. WEISKOPF:

Q We're looking at exactly what 1(b) shows, which is only VDD wires. Do you agree?

A I understand, but just to be clear, Jiang is not making -- I mean, Jiang is doing real circuit analysis. You can see that because if you look at the modeling, the modeling description which is on figure 2, it's specifically telling you that you have more circuitry.

So if you are treating figure 1(b) as saying that all Jiang has is just power lines,

that's just wrong. That's categorically not correct.

Q Okay. I understand that's your position, but we're looking at just literally what 1(b) shows, which is just power wires on L1.

A Okay.

Q If you're looking at just that without bringing anything else into it, if you're just looking at L1 is there any concern with shorting because the VDD wires are shorted together?

MR. WILSON: Objection; form.

THE WITNESS: If you assume that all Jiang has are just VDD wires, which in my opinion is absolute nonsense and is inconsistent with the disclosure of Jiang, at least -- if you had a system where all you had are VDD wires because they are all at the same VDD, shorting is not a problem.

However, that's not what Jiang is about, and it's categorically clear that that's the case. That's a nonsensical reading of this figure.

BY MS. WEISKOPF:

Q Okay. So we're in agreement that if you're looking at just a layer that has shorted VDD wires there's no concern about shorting against

something else?

MR. WILSON: Objection; form.

BY MS. WEISKOPF:

Q Let me strike that question. I agree that was an unclear question.

So let me actually pick up on something else you said. You brought in figure 2 of Jiang. Is it your opinion that figure 1 is the same as figure 2?

MR. WILSON: Objection; form.

THE WITNESS: Actually, Jiang tells us. So Jiang says -- so figure 1 -- well, figure 1(a) is the normal power supply system. Figure 1(b) is the power-gating system.

Figure 2 is the modeling of the system of figure 1, and the reason I brought it up is it shows you clearly that there are power draw models from circuitry, which means there's more than just power wires. That's all.

So figure 2 is not the same as power 1, but it's the description of the modeling done for figure 1(b).

BY MS. WEISKOPF:

Q Okay. I think I understand. So figure 2 is the model of figure 1(b); is that right?

A It's the power-gating model for figure 1(b), and it says that explicitly at the top of -- at the top of section 3.1 it says the power-gating model is shown as figure 2.

Q Okay. So is it your opinion that a person of ordinary skill in the art would interpret figure 1(b) with reference to figure 2?

MR. WILSON: Objection; form.

THE WITNESS: I don't know what that question means.

BY MS. WEISKOPF:

Q Well, you brought in figure 2 before, and so I'm just trying to understand how a person of ordinary skill in the art would understand figure 1(b) and whether or not the person of ordinary skill in the art would refer to figure 2 to understand 1(b).

A I understand. So the reason I brought it in was to point out the nonsensicality of your previous hypothetical. You appear to be -- well, you certainly posited in your question that L1 is a single layer that only has VDD and has no other

wires in it. I used figure 2 to point out that's nonsensical because figure 2 points out that it's a real power model that has you can see circuitry shown there, which means you cannot have a circuit that just simply has VDD, otherwise you don't have any circuitry under it. So I was just using it to point out the nonsensicality of it.

Now, one of skill would know that the power-gating model of figure 2 is for the architecture of figure 1(b) because that's what Jiang says. It says the power-gating model, the power-gating model, referring back to the power-gating system of figure 1(b), is shown in figure 2.

So the architecture is in figure 1(b), the modeling of the architecture is in figure 2, and it says so explicitly.

Q Okay. So in order to understand what figure 1(b) is showing would a person of ordinary skill in the art refer to figure 2?

MR. WILSON: Objection; form, asked and answered.

THE WITNESS: Okay. I will repeat what I said.

First, to be clear, a person of ordinary skill in the art reads the entire piece of art, and certainly with respect to understanding the modeling of the architecture of figure 1 that is provided in figure 2.

So with respect to that, to understand the architecture they look to figure 1, to understand the modeling of the architecture they look to figure 2, that's what Jiang says, and specifically for figure 1(b).

BY MS. WEISKOPF:

Q So is it incorrect to say that a person of ordinary skill in the art would look to figure 2 to understand figure 1?

MR. WILSON: Objection; form, asked and answered.

THE WITNESS: Again, I've answered that. So with respect to the modeling they would certainly look to figure 2 because figure 2 provides some of the modeling, but that's what it's for. I mean, it calls it out explicitly. Jiang says that power-gating modeling is shown in figure 2.

And the reason I pointed it out is the modeling itself shows that it's nonsensical to

treat this circuit as having interconnects that are only VDD providers. That wouldn't make sense.

BY MS. WEISKOPF:

Q I don't understand the distinction that you're drawing, which is why I'm going back to it, so maybe we can have a different conversation about this. You wanted to interpret L1 based on figure 2 and explain to me why L1 would be interpreted differently than what's shown in 1(b), so is that the correct analysis that you gave me?

MR. WILSON: Objection; form, mischaracterizes his testimony.

THE WITNESS: Well, so, actually, what you stated is wrong. That's not what I did.

So to be clear, I said figure 1(b), L1 in figure 1(b) is not a single interconnect level. I said two things. Firstly, I said when it does the detailed analysis of the interconnect Jiang actually shows that it's two levels, and you see that in Figure 10.

Then I said -- then you said, no, assume that it's all just VDD, it's all one level. I said if it's all one level then you'll short the VDD to every other signal that's on the top level.

And you said, no, assume it's only VDD. And I said that's not possible because if that were the case the modeling would not work.

So that's why I pointed to figure 2, and that is the extent to which my previous answer showed the linkage between figure 1(b), figure 2, and figure 10.

BY MS. WEISKOPF:

Q Okay. I'm just trying to get your position on these. Are you saying that figure 1(b), figure 2, and figure 10 are the same or different?

MR. WILSON: Objection; form.

THE WITNESS: Okay. By definition they are different figures, but to be clear, the relationship between them is the following. Figure 1(b) is the architecture of the power-gating system.

Figure 2 is the modeling of that power-gating system. So it's taking the architecture of figure 1(b) and performing modeling on it.

Figure 10 shows as part of the modeling what Jiang does is Jiang varies the power

mesh granularity and he looks at how it affects performance, and that granularity variation is shown in figure 10. And again, to be clear, that power mesh granularity is done for the architecture of figure 1(b) because it is related to the power-gating system. That's the analysis that Jiang does.

BY MS. WEISKOPF:

Q Let's turn to paragraph 105.

A Okay.

Q Okay. We're back to this interconnected not electrically coupled figure with the orange showing not electrically coupled in paragraph 105.

Do you see that?

A Yes.

Q Is it your position that the not electrically coupled requires a direct electrical connection?

MR. WILSON: Objection; form.

THE WITNESS: I don't know what you mean by that.

BY MS. WEISKOPF:

Q Let's talk about it then. So claim 14 says that the first local power mesh and second

local power mesh are not electrically coupled.

Do you see that?

A Yes.

Q And then you've highlighted here in orange something that says not electrically coupled.

A Yes.

Q And those look like they're not taking into account the connections through the global power mesh, and so my question is is it your opinion that not electrically coupled requires a direct connection between the first and second partial local power mesh?

A Okay. I think I understand your question. So, firstly, I think your interpretation of what I mean by this is incorrect.

So to be specific, if you look at the last statement on paragraph 105 I point out that there's no electrical coupling of one partial local power mesh to another on L2. So at least within L2 there is no partial -- there is no electrical coupling.

In the specific case where we -- if we were to say that you can have coupling through the

global power mesh to meet the requirements of claim 14, then even with respect to that at least as far as the local meshes associated with B and C are concerned, when those transistors are off they're still not electrically coupled or if even one of those transistors is off they're still not electrically coupled.

Q Okay. I understand. So the opinion here is they're not electrically coupled because the sleep transistors can be turned off, and so the dark blue and the light blue are not electrically coupled when transistors are off?

MR. WILSON: Objection; mischaracterizes his testimony.

THE WITNESS: No, that was only half of my answer. The first half of my answer is when I pointed out that there is no electrical coupling of one partial local power mesh to another on L2, so there's two reasons that I provided.

BY MS. WEISKOPF:

Q Okay. Why does the electrical coupling on L2 matter?

A Because it -- it's the facts of this -- of this piece of art. There is no electrical

coupling on L2. So I'm pointing out at least that that is the case, and if the electrical coupling between the local power -- the first and -- first and second local power meshes must be between the meshes themselves, that is not the case here.

Additionally, with respect to the meshes associated with B and C, when at least one of those transistors is off it is unequivocally clear that the first partial local power mesh is not electrically coupled to the second partial local power mesh.

Q I understand. So is it your opinion that to be electrically coupled there needs to be a connection on L2?

A I think I understand. So I actually provide three possible views of this. The first is if the -- if we construe this to require electrical coupling on L2 it's unequivocally true that that is not the case for the partial local power meshes on L2.

Second, if we allow to fall within the scope of the claim the possibility of electrical coupling between -- between the power meshes through the global mesh when at least one sleep

transistor is off, then that would not be true for the partial local power mesh associated with B and the partial local power mesh associated with C, which is what I've pointed to.

And then finally, as I also pointed out, in the case where we modify Jiang to implement a multi-voltage system, then because we have a multi-voltage system for a partial local power mesh associated with one voltage versus a partial local power mesh associated with another voltage we would not have coupling even if the sleep transistors were on because they would be at different voltages.

And so all of that is what I provide in my analysis between paragraphs 105 and 107.

Q Okay. Well, I'd like to understand what you think the plain and ordinary meaning of coupling requires. Does it require a direct connection on the same layer?

MR. WILSON: Objection; form.

THE WITNESS: So couple just means couple. It doesn't require a specific direct connection, but I provided analysis under all the possible views of it so that no matter what it is

my opinion that under -- no matter what view is taken of what electrical coupling is required Jiang discloses it or makes it obvious.

BY MS. WEISKOPF:

Q Okay. Can coupling be indirect?

MR. WILSON: Objection; form.

THE WITNESS: I need more information about what you mean by that. I don't know.

BY MS. WEISKOPF:

Q Well, do you agree that the term "coupling" is -- allows an indirect connection?

MR. WILSON: Objection; form.

THE WITNESS: Again, I need more information about what that indirect connection is. I don't know. I don't know if what you're considering indirect connection is reasonable or not, so I'm not able to answer without a specific.

BY MS. WEISKOPF:

Q I understand. At what point does an indirect connection no longer meet the coupling limitation in the patent?

MR. WILSON: Objection; form, asked and answered.

BY MS. WEISKOPF:

Q This is a claim term, Dr. Subramanian, so I'm trying to understand how you're applying this claim term. So it's the claim term in claims 14 and in other claims as well, and so I just want to understand what the plain and ordinary meaning of coupling is and the scope of what you think coupling means.

So with that background, is there a point at which an indirect connection no longer constitutes coupling within the scope of this patent?

MR. WILSON: Objection; form.

THE WITNESS: Again, I've sort of addressed this.

Firstly, to be clear, I've provided opinions under -- that under any -- I've provided three different ways under which it's still my opinion that Jiang would render this claim invalid, and those are in paragraphs 105, 106, and 107.

With respect to the specific cutoff of where at the point of indirect, I'm sorry, I don't know what you mean by indirect. You're going to have to give me a specific example for me to answer that.

It's not -- in my invalidity analysis I've provided what I believe under any reasonable view would invalidate the claim, but I don't know what you mean in your question beyond that.

BY MS. WEISKOPF:

Q So would the coupling need to be on the chip to meet the coupling limitation of claim 14?

MR. WILSON: Objection; form.

THE WITNESS: I believe so because the claim 12 starts -- if we assume the claim 12 preamble is limiting, it says "a power routing structure applied in an integrated circuit," so if we assume it's limiting then the coupling should be within the integrated circuit.

So to that extent I would say if we assume it's limiting then the answer is yes.

BY MS. WEISKOPF:

Q Okay. If the preamble is not limiting the coupling can be off chip?

A If the preamble is not limiting there's no reference to a chip whatsoever, so then I guess to that sense, yes, it's whatever has elements 12[a], 12[b], 12[c], 12[d], 12[e], 12[f], and 14, and obviously 13 since 14 depends on 13.

Q Okay. So if the preamble is not limiting then coupling could be on chip or off chip?

A If the preamble of 12 is not limiting, there is no reference to a chip whatsoever. There's no reference to an integrated circuit that shows up anywhere within claim 12, 13, and 14, so it would be incorrect for me to introduce a requirement for an integrated circuit because that would not be within a limitation of the claim.

Q I'd like to turn to the -- you mentioned there were three different possible ways that the coupling limitation is met, and you brought up the Li and Chiu modification in paragraph 107.

Do you recall that?

A Yes.

Q Okay. In paragraph 107 is it your opinion that the Jiang as modified in paragraph 107 could not be interconnected by the ground wires?

A I don't understand your question.

Q Okay. So let's look at what you've done for 107. You've brought in something about Li and Chiu's multi-voltage layout.

A Yes.

Q In that scenario it says -- I understand

you to be saying that claim 14 is still met, there's no electrical coupling between the partial local power meshes; is that right?

A In the case where you take a modified system that one of skill would form by -- or would know of by combining the teachings of Jiang with the teachings of Li or Chiu to get a multi-voltage design, that would be another reason because in that situation even if you assumed the scope of the claim covered the case where coupling could be achieved through the global power mesh because one of the local meshes would be powered by one VDD and the other local mesh would be powered by another VDD, there could not be any coupling through the VDD lines in the global mesh.

Q Okay. So let's switch to the ground lines. Is it your opinion that there would not be electrical coupling through the ground wires either through the top layer global mesh?

A So, again, one of skill could -- if one of skill -- if one of skill provided each VDD off this modified system with its own ground, then they would not be coupled provided they had their own grounds.

And specifically, if we look at the language, I believe 1006 is -- is Chiu, you see how it talks about that power and grounds as being pairs where it says power dash ground rails. So it's pairing them.

So certainly one way one of skill could make this combination is to provide separate ground rails for each of the VDDs in the combination.

Q Okay. Is that how you would make the combination if you did it with Li?

A It's certainly one way that could be done and one of skill would know how to do that, which would make it obvious.

It's not the only way that it could be done. You could invalidate claim 12 without doing that, but it would be obvious to one of skill in the art that if, for example, the PTAB finds that claim 14 requires that there be no ground connection through the global power mesh that provides some sort of interconnecting pathway, that would be obvious as well.

Q I'm asking about the specific modification to Jiang that you've made here. In

that specific modification where you modify Jiang with Li, would that specific modification have ground wires electrically coupling between the first and second partial local power meshes through the global mesh?

A I think I just answered that question, but I'll answer it again.

So this is in relation to claim 14. So in claim 14 if the PTAB, for example, finds that -- so, first, one way to do it which would be straightforward and would invalidate claim 12 is to have multiple power wires and not have multiple sets of isolated ground wires. In that situation it would certainly invalidate claim 12.

If the PTAB finds that that does not invalidate claim 14 it would certainly be obvious given that Chiu, for example, specifically teaches power ground rail pairings to say for one VDD I'll provide one set of grounds and for another VDD I'll provide another set of grounds, in which case it still invalidates claim 14, and that would be obvious as well.

Q Let's turn to paragraph 111.

MR. WILSON: If we're going to switch

topics isn't it about time for a break?

MS. WEISKOPF: That's fine with me. How long would you guys like?

THE WITNESS: At some point I'd like to eat dinner. It's like 8:00 o'clock.

MS. WEISKOPF: Yeah, I don't know what time zones anybody is on, so I'm glad you mentioned that. I also don't want to keep you super late, if at all possible, so, Dr. Subramanian, just balance that with how long you want and just let me know what you'd like.

THE WITNESS: Well, I have no idea how long you're planning to go, so if you're planning to go for a while I'd like to eat dinner. If -- and I'm sure the court reporter needs a longer break as well. But if you're going to finish up relatively soon, I don't mind taking a short break and then continuing to go, but that's -- you know, I don't know what your plan is.

MS. WEISKOPF: I can't tell how long it's going to take either because I keep asking you extra questions, Dr. Subramanian, so I think you better eat dinner but, you know, so I think it's probably safest. I don't want to keep you from

eating dinner.

THE WITNESS: Okay.

MR. WILSON: Yeah. Just for reference, I mean, we have less than two hours on the record left, so for whatever that does for you, Dr. Subramanian.

MS. WEISKOPF: Why don't we go off the record in that case. Might need all of my time given the way this has been going.

I will try to speed up, but let's go off the record and you can just tell me how long you want.

THE REPORTER: I'm off the record.

MS. WEISKOPF: Thank you.

(Whereupon, a recess was taken.)

MS. WEISKOPF: Let's go back on the record.

BY MS. WEISKOPF:

Q I'd like to turn to paragraph 111. So in this paragraph, Dr. Subramanian, there is an arrow and a wire pointing at Li figure 3 that says common ground wire.

Do you see that?

A Yes.

Q And there's also one in Chiu that the lower figure is annotated as a common ground wire. When you wrote common ground wire there do you mean that the wire has a common ground potential as other wires?

A You mean as other ground wires?

Q Yes. When you wrote common ground wire in paragraph 111, does that mean that it has a common ground potential as other ground wires?

A Yes.

Q Was it intended to have other meaning also?

A What I'm pointing out here, for example, these are the annotated versions of the figures from the two secondary references, so they're in Chiu, and what you see is that when I point to a common ground wire what that's pointing out is various things. Firstly, it's pointing out that it's grounded and, secondly, it's pointing out that you'll notice, for example, if you look at the vias in Li that the same ground wire is connected to other ground wires.

So that's why I called it a common ground wire.

Q Okay. There are ground wires on metal-7 and metal-6 and there's a via-6 connection in figure 3; is that right?

A Yes.

Q And so your point is there's a common ground wire that's connected to other ground wires through those via-6 connections in figure 3; is that right?

A That's right.

Q Okay. Now, claim 18 uses the term "same ground wire"?

A Yes.

Q Is that right?

A Yes. I believe you read it correctly.

Q Is your labeling in paragraph 111 related at all to claim 18?

MR. WILSON: Objection; form.

THE WITNESS: So I actually address claim 18 specifically in paragraphs 120 and 21. I do call out to the same figures off Li and Chiu, but so the section that you're pointing to is actually in relation to claim 15. I address claim 18 later, though I do point to the same figures in my analysis.

BY MS. WEISKOPF:

Q Okay. Is it your opinion that the common ground wire that you labeled right here in paragraph 111 is also the same ground wire required by claim 18?

MR. WILSON: Objection; form.

THE WITNESS: Could you repeat the question, please?

BY MS. WEISKOPF:

Q Yeah. Is it your opinion that the common ground wire labeled in paragraph 111 is also the same ground wire required by claim 18?

MR. WILSON: Objection; form.

THE WITNESS: So I actually address that in paragraphs 120 and 121, and just to be clear, the point that I make is to achieve a good ground everything is -- all those ground wires are connected together as shown in the annotated figure 3.

The net consequence of that is that if we look at the language of claim 18 which specifically requires the first local ground wire and the second local ground wire share the same ground wire of the global power mesh, the nature of

it producing an equipotential means that they would share at least one of those wires in terms of them having -- in terms of the provisioning of the ground.

BY MS. WEISKOPF:

Q Is it your opinion that claim 18 requires a single ground wire?

A So the claim, it says what it says. In other words, it says specifically "the first local ground wire and the second local ground wire share the same ground wire of the global power mesh." There can be other ground wires in the global power mesh, but they have to share the same ground wire.

And in my opinion it does because the nature of the mesh network of the ground connections results in there being an equipotential, which means that the same ground wire can support or, in fact, does support or provide equipotential support for the first local ground wire and the second local ground wire in their respective local meshes.

Q If the construction of same ground wire requires one same ground wire is claim 18 met under grounds 1 and 2?

MR. WILSON: Objection; form.

THE WITNESS: I need more clarification. You mean there's no other ground wires allowed, there's a single ground wire in the entire global mesh?

BY MS. WEISKOPF:

Q That is shared by the first and second local ground wires, yes.

A But there can be other ground wires in the global mesh, correct, which could also be shared?

Q Well, is that your understanding of the claim 18?

A I'm sorry. It's your hypothetical, so I'm asking you for clarification of your hypothetical.

Q Yeah, if you need to identify one same ground wire that is shared by the first local ground wire and the second local ground wire, is there one same ground wire?

A Yes, there's one and there's more than one. It's an equipotential, which means that the nature of how these ground wires are set up is such that all the ground wires will create a mesh that

provides an equipotential across that mesh. So any one of those wires would meet the requirements because it is providing the equipotential that provides the ground for the first local ground wire and the second local ground wire.

Q So is it your opinion that all ground wires in the global power mesh would share the same electrical properties?

MR. WILSON: Objection; form.

THE WITNESS: I don't know what you mean by that.

BY MS. WEISKOPF:

Q Well, you're talking about an equipotential. I'm just trying to understand is it your opinion that if all the ground wires are connected together they're all sharing the same potential?

A Approximately, yes. I mean, it's not -- in reality that's not exactly true, but in a good ground ideally and the reason to use this mesh is it will hold them all at approximately the same ground potential.

Q Okay. Claim 18 uses the word "share." Do you agree that share means something different

from coupling?

A Yes.

Q How is share different from coupling?

A Share means share. In other words, it's something that is shared. Coupling mean couple. I mean, they're different words. I don't know what else you want me to say.

Q Well, in application in a chip is shared the same as coupling, is there any difference?

MR. WILSON: Objection; form.

THE WITNESS: So it depends on the context. Again, even on a chip it depends on the context. I don't know how to answer that.

BY MS. WEISKOPF:

Q We're talking about sharing a ground wire, we're talking about the context of claim 18, so in the context of claim 18 is shared any different from coupling?

MR. WILSON: Objection; form.

THE WITNESS: So the word "coupling" doesn't appear in claim 18, so I don't know how to answer that.

BY MS. WEISKOPF:

Q Okay. Claim 12 has coupling, right?
A That's true.
Q So in the -- and claim 18 depends from claim 12; is that right?
A Yes, it does.
Q So claim 18 shares all the limitations of claim 12; is that right?
A That's right.
Q Okay. So in the context of claim 18 depending from claim 12 how is shared different from coupling?
A They're different words. Shared in this case is specifically in the reference of the relationship between the first local ground wire and the second local ground wire and how they are related to the same ground wire of the global power mesh.

Coupling appears in claim 12, for example, in the relationship between the global power mesh and the first and second local power meshes. So specifically there the relationship is a -- it says the global power mesh is coupled to the first local power mesh, so it's establishing a one-to-one relationship across those, and then the

global power mesh is coupled to the second local power mesh, so that's establishing a one-to-one relationship across those.

The shared language has a two-to-one relationship in that it's saying that the first local ground wire and the second local ground wire share the same ground wire of the global power mesh.

Q Okay. How is the sharing accomplished in claim 18, is it through coupling?

A Yes, in that the first local ground wire is in the first local power mesh, the second local ground wire is in the second local power mesh, and the same ground wire is in the global power mesh, and claim 12 tells us that the global power mesh is coupled to the first and second local power meshes.

Q In your opinion is coupling met as long as wires have a common potential?

A No, that doesn't necessarily follow. I could have two wires that are on different ends of the world and are not in any way related to each other and they could incidentally have the same potential.

Q Okay. On a chip is coupling met as long

as the wires have a common potential?

A No. My answer would be the same for the same reason.

Q Okay. Is sharing met as long as wires have a common potential on a chip?

A No. My answer would be the same for the same reason. They could coincidentally have the same potential, but that doesn't mean they're shared.

Q Sharing can mean that by coupling by via, for example?

A I don't know how to answer that. That's not enough information for me to know what you're saying.

Q So if a first local ground wire and a second local ground wire each had a via connecting to the same ground wire of the global mesh, would that meet the sharing limitation of claim 18?

MR. WILSON: Objection; form.

THE WITNESS: I guess. It depends -- I mean, I'm not sure if I have the full extent of your hypothetical, but if I understand what you're saying the global -- there's a wire -- a singular wire within the global power mesh that happens to

have a via that connects to the first local power mesh to a particular wire there and to the second local power mesh to a particular wire there; and you're asking me if those two then would share the same ground wire on the global power mesh, and I guess the answer in that situation would be yes.

BY MS. WEISKOPF:

Q Okay. If there's a switch between the ground wire of the first local power mesh and the second local power mesh -- I'm sorry. This hypothetical is going to be too complicated. Let me just skip it. So let's strike that.

Let's move to ground 3. Claim 3 depends on -- I mean ground 3. Strike that.

Ground 3 depends on your analysis for grounds 1 and 2; is that right?

A In the sense that at various points within my analysis for ground 3 I point to analysis that I've done previously for grounds 1 and 2 and indicate that it's equally applicable here.

Q Okay. If the PTAB finds that your reasoning for grounds 1 and 2 is insufficient to meet the limitations of claim 12, do you agree that the same result should happen for ground 3?

MR. WILSON: Objection; form.
THE WITNESS: I couldn't say. I would need to know the basis for the PTAB's opinion.
So as a general statement, no, I don't think I can agree without knowing the specifics.
BY MS. WEISKOPF:
Q Okay. Well, if the PTAB finds that the five references in grounds 1 and 2 of your declaration here don't disclose structure of claims 12 through 18, does ground 3 fail?
MR. WILSON: Objection; form.
THE WITNESS: Again, I'd need to know the basics -- the basis of that. Without knowing exactly what the PTAB has said, I cannot answer one way or another.
BY MS. WEISKOPF:
Q In this hypothetical they found that the structure of Jiang and all of the rest of the references in grounds 1 and 2 don't meet claims 12 through 18, in other words, grounds 1 and 2 do not invalidate those claims, if the PTAB finds that do you agree that ground 3 also wouldn't invalidate the claims?
MR. WILSON: Objection; form.

THE WITNESS: Again, I couldn't say without knowing the specifics of the basis for their finding.

BY MS. WEISKOPF:

Q What would save ground 3 in that instance?

MR. WILSON: Objection; form.

THE WITNESS: If the PTAB found that while they found that the relevant art didn't invalidate claim 12, for whatever reason they found it invalidated the relevant limitations of claim 1, then they could still arrive at a conclusion of invalidity. I don't know because you're putting me in a hypothetical that I haven't seen.

BY MS. WEISKOPF:

Q Well, for claim 1 do you identify any additional art that meets the limitations of claim 12?

A You mean other than the art that I identified versus claim 12?

Q Yes, exactly. Is there something new added in claim 1 that you are asserting meets the elements of claim 12?

A Okay. Just so I understand, you mean

other than the APR-related art?

Q Okay. Well, why don't we do this a different way. We'll go through that.

You've identified the LPMM and the, I don't know how to say it, Bertolet as two additional references for ground 3; is that right?

A That's right.

Q Okay. So I think my question is Bertolet and LPMM, is it your opinion that either one of those references discloses the structure claimed in claim 12?

A I have not offered an opinion with respect to claim 12 on the basis of Bertolet or LPMM on their own.

Q Right. So then that goes back to my question of if Jiang and all the rest of the references in grounds 1 and 2 don't disclose the structure of claim 12, isn't that necessary for ground 3?

MR. WILSON: Objection; calls for a legal conclusion and form.

THE WITNESS: Again, my answer is the same. In other words, without knowing the basis for -- without knowing more details of this

hypothetical world in which the PTAB finds that the references that I cited against claim 12 don't invalidate claim 12, without knowing the basis for that I couldn't say what conclusion they would draw with respect to whether those references invalidate the corresponding limitations of claim 1. I just don't have the information to answer that.

BY MS. WEISKOPF:

Q Let's look at your opinions for claim 1 because perhaps I'm misunderstanding, Dr. Subramanian.

It was my understanding, so please show me where I'm wrong, that what you offer for ground 3 in addition to grounds 1 and 2 are references that are disclosing something about APR tools; is that right?

A At a high level, yes, that's fair, in addition to what I provide for the references that I cited with respect to claim 12.

Q Okay. So let's go through them. Paragraph 125 I see you're citing the Bertolet reference.

A And also LPMM. They're both called out there.

Q Okay. Yeah, I actually was going to go through Bertolet first and then LPMM, so I'm not trying to be exclusive on 125. I'm just saying Bertolet is mentioned there, so I want to go through what you're citing Bertolet for in 125 and the rest of ground 3.

So here I see Bertolet being cited for a statement "after custom macro placement, a power distribution network is algorithmically generated using a custom SKILL program."

Is that right?

A That is the cite that I quote from Bertolet on the bottom of paragraph 125.

Q And that's sort of generally for the proposition that APR tools were known; is that right?

MR. WILSON: Objection; form.

THE WITNESS: Well, that's to point out that Bertolet specifically discusses how to do algorithmic generation. It's true that one of the things that this would make clear, therefore, is that these sorts of tools were known.

BY MS. WEISKOPF:

Q In 126 there's a quote that refers -- let me see if I can find it here. It's right in the middle of 126. It says "power terrains."

Do you see that?

A Yes.

Q What is a power terrain in Bertolet?

A One second. I'll need to look at Bertolet.

(Document was marked Exhibit 1013 for identification.)

BY MS. WEISKOPF:

Q Here. Let me introduce that, too, so we have a clean record.

So Bertolet is marked Exhibit 1013, and it's in the Marked Exhibits folder, too.

A Okay. So the language on power terrains appears generally in the discussion related to power routing, so it's related to the distribution of the power distribution network. And essentially what the power terrains are describing is how in an area-specific way on the chip different areas of the chip may have different gridding structures to provide power therein, so it's essentially defining islands on the chip that have different power

requirements and how those are provided.

Q Okay. You might just want to leave Bertolet open because I'm going to try to speed through this so we can all go home and you can go to sleep, Dr. Subramanian.

So is it your opinion that Bertolet discloses the structure claimed in claim 12?

MR. WILSON: Objection; form.

THE WITNESS: I have not offered an opinion of invalidity where I use Bertolet as a primary reference to invalidate claim 12.

BY MS. WEISKOPF:

Q Okay. And you're not offering any opinions that Bertolet discloses a multiple power domainship, are you?

A So with respect to my analysis of the power domain limitations of claim 12 or, correspondingly, the power domain limitations in claim 1 on their own, not counting any APR language, I'm not using Bertolet to specifically cite for evidence disclosing the power domain itself.

Q Okay. Do you have an opinion about whether Bertolet discloses a multiple power

domainship?

MR. WILSON: Objection; form.

THE WITNESS: Bertolet calls out the use of power terrains but doesn't specifically call out the relationship between that and the power structures of the chip underneath and is silent as to the voltage requirements.

Beyond calling out the fact that the chip has a -- I think a 2.5-volt supply, yes, it's a 2.5-volt supply, it doesn't call out whether there are multiple power domains specifically. So it's silent on that. It does teach the use of power terrains but doesn't relate it to the underlying circuitry.

BY MS. WEISKOPF:

Q Okay. And there's only one voltage supply; is that right?

A There's only one external voltage supply. It doesn't say whether there's internal supplies.

Q So do you agree that Bertolet does not disclose a multiple power domainship?

MR. WILSON: Objection; form.

THE WITNESS: I have not cited Bertolet as evidence for disclosing the first and second

power domains on their own, not counting the APR requirement, of claim 12 and claim 1.

BY MS. WEISKOPF:

Q Okay. Are you offering an opinion one way or the other whether Bertolet discloses multiple power domains?

A I think I just answered that question, but I'll answer it again, which is I have not offered an opinion that -- I have not taken a position that Bertolet -- that I'm using Bertolet on its own, not counting the APR tool requirement, to teach or disclose the first and second power domain requirements.

Q Okay. That only answers sort of part of the question. Are you offering any opinions at all that it discloses multiple power domains in Bertolet?

MR. WILSON: Objection; form, asked and answered.

THE WITNESS: Again, I think I just did answer the entirety of that question, but I'll say it again, which is I'm not offering an opinion that -- I have not used Bertolet to offer an opinion that Bertolet on its own, putting aside any

APR disclosures, discloses the first and second power domains of the relevant claims, for example, claim 12 and claim 1, in the limitations related to said power domains.

BY MS. WEISKOPF:

Q Okay. Does Bertolet disclose sleep transistors or switches?

MR. WILSON: Objection; form.

THE WITNESS: So it certainly discloses switches because it talks about CMOS, but I don't think it talks about sleep transistors.

BY MS. WEISKOPF:

Q Okay. Let's talk about LPMM. So you mention LPMM in ground 3, and I'm just going to try to skip here. We can go through these if you want. I'm just trying to speed up, Dr. Subramanian.

Again, you're not offering the opinion that LPMM discloses the structure claimed in claim 12; is that right?

MR. WILSON: Objection; form.

THE WITNESS: With respect to my invalidity analysis, I do not offer a ground on the basis of LPMM as the primary reference for the limitations of claim 12.

BY MS. WEISKOPF:

Q Okay. So is there any opinion whatsoever that LPMM discloses the structure of claim 12 even if it's not a primary reference?

MR. WILSON: Objection; form.

THE WITNESS: Can I have the question again, please?

BY MS. WEISKOPF:

Q Yeah. Is there any opinion whatsoever that LPMM meets the limitations of claim 12 even if LPMM is not being used as a primary reference?

MR. WILSON: Objection; form.

THE WITNESS: So I am not using -- I have not asserted an invalidity basis in which I use LPMM against claim 12 on its own. In other words, what I mean is I have used LPMM in references other than claim 12.

BY MS. WEISKOPF:

Q Okay. You're not offering the opinion that LPMM discloses forming a global power mesh using an APR tool, right?

MR. WILSON: Objection; form.

THE WITNESS: With respect to LPMM, I'm using it for the APR tool and specifically teaching

related to the APR tool.

With respect to the details of the global power mesh, for that I am not depending on LPMM on its own. I use it in combination with other references, for example, Jiang, Li, et cetera, depending on which ground we're talking about.

BY MS. WEISKOPF:

Q Okay. And you're not offering an opinion that LPMM discloses forming partial local power meshes corresponding to the location of a power domain using an APR tool; is that right?

MR. WILSON: Objection; form.

THE WITNESS: Again, with respect to -- I believe you're asking about limitations 1[a] and 1[b]. With respect to those limitations, I point to LPMM in my combinations for the use of an APR tool. For the other parts of those limitations I point to other references depending on the combination, either Li, Jiang, et cetera, and, therefore, I believe claims 1[a] and 1[b] are invalid as being obvious in light of those combinations, not based on LPMM on its own.

BY MS. WEISKOPF:

Q So you're not offering any opinion that LPMM discloses coupling power meshes using an APR tool; is that right?

MR. WILSON: Objection; form.

THE WITNESS: So I assume in this question you're referring to claim elements 1[d] and 1[e]; namely, coupling the first and second local power meshes to the global power mesh and the first power domain and second power domain using the APR tool. In those references I point to LPMM for the knowledge of one of skill in the art would have with respect to the APR tool, but with respect to the other parts of those limitations I point to other references that one of skill would use in combination and depending on the ground the references Jiang, Li, et cetera.

BY MS. WEISKOPF:

Q Okay. Let's turn to paragraph 151 of your declaration, which is Exhibit 1003.

A Okay.

Q It will take me a second to get there. I'm sorry.

Okay. 151 contains your opinion that the first power domain in the Li reference is Core

‹0›; is that right?

A That's not complete. In fact, in the very last sentence I say "I will use Core ‹0› as a representative first power domain, but any of the cores could be the first power domain."

Q Okay. I mean, is there any difference between any of the cores?

A Yes. They're different cores.

Q That's relevant to your knowledge, is there any difference between any of the cores that would change using Core ‹0›?

A You mean would my analysis change if I pointed to a different core?

Q Exactly. Is there something different about the cores that's relevant to your analysis?

A So if by that you mean would my analysis change in some way that would impact my opinions, the answer is no. I would do the same basic analysis except instead of pointing to Core ‹0› I would point to Core ‹1›, Core ‹2›, or Core ‹3›, but I would still reach the same opinion.

Q Okay. So it's your view that each of the cores, ‹0›, ‹1›, ‹2›, and ‹3›, all have the same power route instruction on the chip; is that right?

MR. WILSON: Objection; form.

THE WITNESS: Yeah, I'm sorry. I didn't understand the question.

BY MS. WEISKOPF:

Q I'm trying to understand why you brought that up. Does it matter that there's Core ‹1›, ‹2›, and ‹3› to your opinion or does Core ‹0› have any -- are they all power routed the same way?

A So the reason I brought that up is you said this paragraph I point to Core ‹0›, and the answer is, well, no, I point to actually all of them, I just Core ‹0› as exemplar. That's all.

So it was just your question was framed in a way that incorrectly characterized my report, so I corrected that.

Q Okay. I don't understand the relevance of that, but I see a dark blue box that has a first power domain and an arrow to it that says Core ‹0› so are we talking about Core ‹0› in your opinion or a different core?

MR. WILSON: Objection; form.

THE WITNESS: I'm going to repeat what I said. So I used Core ‹0› as a representative first power domain, but any of the cores could be the

first power domain.

BY MS. WEISKOPF:

Q Okay. I understand you have that written here. Could you explain to me how changing the cores would affect your analysis?

A Sure. So instead of pointing to Core ‹0›, if I were performing the analysis for Core ‹1› I would point to Core ‹1›, if I were performing the analysis for Core ‹2› I would point to Core ‹2›, and obviously if I were performing the analysis for Core ‹3› I would point to Core ‹3›.

With respect to how the analysis would proceed, it would be the same except any time I reference something related to Core ‹0› I would now point to ‹1› through ‹3›, respectively, and I would ultimately come to exactly the same outcome. In other words, I believe that this limitation is disclosed by Li.

Q Are there any other differences between the cores that would be relevant to your analysis other than their names?

A Again, I think you asked me this and I've answered it, but I'll try again, which is I would perform the same analysis, the analysis would

proceed in the same way other than the names, and I would arrive at the same outcome.

Q Do you agree that all four of the cores have a switch, a ground switch?

A I believe so. I believe -- I believe that's right.

Yes, it says that specifically. It says that on -- if I look at Li on page 494, in the last paragraph it says "A power switch structure is designed surrounding each core," and I think that --

Q Because the power -- sorry.

A And I think that's what you're referring to when you call it a ground switch.

Q I am. And so when we talked about the routing structure that you think Li discloses that goes from the global mesh down to the silicon device layers where the switch is and then up to a local power grid, that's the same power routing structure that would apply for Core ‹0›, Core ‹1›, Core ‹2›, and Core ‹3›; is that correct?

A Hierarchically, yes. Obviously because the local power meshes are gridded at a block level there will be different local power meshes for each

of the Cores ‹0› through ‹3›, so it's not the same core for all of -- sorry, it's not the same mesh for all of them.

Q Okay. I think I understand. You're saying that's generally true that it would go from the -- Strike that.

Is the switch the same between Core ‹0›, Core ‹1›, Core ‹2›, and Core ‹3›, do they each have their own switch also?

A They each have their own switches.

Q Okay. So let's just -- the power routing structure for Core ‹0› on the ground side would be the same for each core with the caveat that they would each have their own switch and power grid; is that right?

A I'm not sure what you mean by that. If you mean architecturally they would be the same, not that they are the same switches and the same power grids, then I agree. Architecturally the structure is still -- there's the chip level power grid, then there's the power switch, then there's the local grid, then there's the core, but each of the cores has its own power switch and has its own local grid.

Q Okay. Let's go to paragraph 152.
A Okay.
Q So in the middle of 152 Li describes in local power grids -- excuse me, Li describes its local power grids in the same manner stating that power and ground lines in the local sections are gridded on metals-2 through 5 on which the local power grids are formed at the block level.
Do you see that sentence?
A Yes, I think you said local, though, and I think you meant to say global. Which one were you reading?
Oh, the second sentence. Excuse me. Yeah.
Q So I'm trying to read --
A You read it correctly. You read it correctly. I apologize. I was looking at the wrong line.
Q Okay. Well, so I'd like to just focus in on this "in the local sections." You're not offering an opinion where the local sections are in this paragraph; is that right?
A I don't know what you mean by that.
Q Well, it says "in the local sections" in

this paragraph 152. Do you agree with that?

A Yes.

Q Okay. You haven't offered an opinion where the local sections are in this paragraph, have you?

A I still don't understand what you mean by that. You just repeated the question in two parts. It hasn't changed my lack of understanding of what you mean by that.

Q Okay. There's a phrase "in the local sections," right?

A Yes.

Q Is there an opinion about what that phrase means?

A Within -- within this paragraph, no. I'm just quoting from Li directly, and then here I point out, firstly, that -- you know, in the next sentence I point out that the grids would have horizontal and vertical lines and then in the paragraph after that I point out to the relationship to the blocks.

So these are the two sections where I link the relationship between the local circuitry and the local grids.

Q Okay. So do you have an opinion about where the local sections are and what that phrase means?

A Again, I don't specifically perform an analysis within this paragraph on what local sections means, but I address the relationship between the grids and the blocks in this paragraph, which is 152, paragraph 153 where I point out that the local power grids at the block level means they are formed to correspond to the underlying circuitry that they will supply and I go on from there, and then finally in paragraph 154 and 155 I address the positional correspondence and also in 156 I bring in Jiang as an additional reference, if needed.

Q Well, are you offering an opinion about the meaning of the phrase "in the local sections"?

A Again, I think I've answered that question. So I don't specifically take this language of Li where he says power and grounds in the local sections are gridded on metals-2 through 5 and address what specifically he means by "local sections," but I point out that he's referring to the local power grids, in fact, he goes on to say

that in the very same sentence, and then I talk about what that means in the context of paragraphs 153, 154, and 155.

Q Okay. I honestly don't understand, so I'm going to just ask slightly more specific questions. Are you saying in the local sections has the same meaning as at the block level?

A No, because I point to at the block level when I'm referring to at the block level.

So when Li is talking about the local sections here, this is distinguishing it from the global sections which are on metals level 6 and 7, and here he's saying the local sections, in other words, the sections where the local grids are formed, are on metals-2 through 5. That's all he's saying for here.

Q What's the point of saying local sections there?

A Li says what he says, but here it's quite straightforward. Li uses the word "local sections" here to distinguish it from the global sections because they're on different metal levels. The global sections are on metals-6 and 7, and he's saying the local sections are on metals-2 through

5. That's the point he's making in this sentence.

Q Okay. So let's go to paragraph 161. So here I understand the second power domain is identified as the switch; is that right?

A The block labeled switch, yes.

Q Yes. Okay. Let's go to paragraph 175.

A Okay.

Q So claim 14 says "The power routing structure according to claim 13, wherein the first local power mesh and the second local power mesh are not electrically coupled," right?

A I believe you read that correctly.

Q Okay. And then the first sentence in 175 says "Li discloses this limitation." Is that right?

A Yes.

Q Okay. So if the partial -- you state "If the partial local power meshes for each core or the switch were interconnected, the cores could not be described as electrically isolated from one another as well as the rest of the chip."

Do you see that?

A Yes.

Q How does that support your opinion that

Li discloses the limitation?

MR. WILSON: Objection; form.

THE WITNESS: So, again, as I told you earlier, so in the language where Li describes the individual cores as being electrically isolated, we've talked about that before, that's because they sit in triple-wells and they have their own power requirements. Specifically, if we compare the core to the switch it has a different VDD.

So the net result is what we have is if we look at the first local power mesh, which, for example, if we're using Core ‹0› would be the local mesh associated with Core ‹0›, it is electrically not coupled to the second local power mesh, which would be the core associated with the switch block, because they have separate voltage requirements and they have separate VDDs and we have the isolation that is provided by the use of the triple-well architecture which separates the ground.

BY MS. WEISKOPF:

Q Let's go to paragraph 177.

A Okay.

Q Here we have that similar annotation for

figure 3 where you have this common ground wire identified, so I have similar questions for you here is is this related to claim 18?

MR. WILSON: Objection; form.

THE WITNESS: So this is analysis that's specific to claim 15. I provide additional analysis that does refer back to this when I discuss claim 18.

BY MS. WEISKOPF:

Q Okay. So this is called a common ground wire because it shares a common ground potential with other ground wires; is that right?

A Well, that's certainly true here. In addition, as we discussed previously in Li, we have the vias that connect the multiple ground wires to each other.

Q And when you say those vias, you mean via-6; is that right?

A I mean specific instances of via-6. Not every via-6 makes a connection to ground.

For example, if you look at the via-6 on the bottom right-hand corner of the figure 3 which is annotated on page 111, that's a VDD connection. That's not a ground connection.

Q Okay. Let's see. When you talk about the vias, you're talking about the specific via-6 vias that are connecting the ground wires; is that right?

A That's right.

Q Okay. Not other vias that aren't shown; is that right?

A No, there are vias that are shown that are not connecting the ground wires.

Q Okay. When you refer to vias, are you referring only to the relevant via-6 vias or were you referring to other vias that are not shown in figure 3?

A Well, in my point about the common ground wire I was pointing to the via-6 vias that are connecting the ground wires to each other, not via-6 wires that are shown but are not for ground, they are instead for VDD.

Q Okay. Let's move to paragraph 181. Here you say "Li discloses or renders this limitation obvious," referring to claim 18; is that right?

MR. WILSON: Objection; form.

THE WITNESS: Yes, I see the language that you're pointing to.

BY MS. WEISKOPF:

Q Yeah. And it says "Li discloses that it has a common ground reference."

Do you see that?

A Yes.

Q Why does that support your opinion that Li discloses or renders claim 18 obvious?

A Well, that's part of it. It goes on to point out, and this is a similar analysis to what we discussed previously, the point is when you have this global mesh you have tied everything to an equipotential, so, in fact, the mesh will ensure, therefore, that any one of those wires is used to provide -- is providing a ground that will serve both the first local ground wire and the second local ground wire provided the switches are on.

Q So is it your opinion that a common ground reference satisfies the same ground wire limitation?

A No --

MR. WILSON: Objection; form.

THE WITNESS: No, I didn't say that. I gave you the specific reason why in this case the ground wires of Li would do this, because they

create this equipotential net such that the individual wires within the nets are actually serving to provide the potential for the first ground wire and the second ground wire by creating this equipotential net. Of course, in the specific case of Li that's true when they're powered up, not switched off.

BY MS. WEISKOPF:

Q Is there an example when a common ground reference would not satisfy the same ground wire limitation?

A I don't -- I don't know specifically. It's not my job to think of everything that doesn't satisfy the claim. My analysis is to prove that this does disclose or render obvious the claim.

Q Okay. So sitting here today you don't have an example of when a common ground reference would not satisfy the same ground wire limitation of claim 18; is that right?

A I haven't provided one, nor is it my job to do so. My job is to show that the references invalidate the claims.

Q Okay. But you're also supposed to answer my questions, right?

A Yes, and I think I am. You asked me had I shown that, and I said no and nor is it my job to do so.

Q Sure, but my question is sitting here today do you have an example of when the common ground reference satisfies the same -- does not satisfy the same ground wire, and so I'm just wondering sitting here today do you have an example or not?

MR. WILSON: Objection; form.

THE WITNESS: Okay, and I just answered that question. The very first thing out of my mouth, I'll say it again, was no, nor is it my job to do so.

It is not the purpose of my analysis to show things that do not invalidate the claim. It's my job to show that the claims are invalid in light of the art, and I've done that.

BY MS. WEISKOPF:

Q All right. Let's move to paragraph -- to ground 5. So here again you add LPMM --

A I'm sorry. Which paragraph are you on?

Q Oh, sure. Yeah. Let's look -- let's just quickly scroll to the ground 5, which starts

at paragraph 182.

A Okay. I have it. Thank you.

Q Okay. So here you're adding Li in view of Jiang in further view of Bertolet or LPMM; is that right?

A With respect to this obvious analysis, yes. The primary reference is Li in view of -- is Li, and then it's in view of Jiang and further in view of the two references I use for APR.

Q Okay. And the LPMM and Bertolet are being used for similar reasons in ground 5 that they were being used in ground 3; is that right?

MR. WILSON: Objection; form.

THE WITNESS: If by that you mean I'm using them in -- for showing that one of skill would know that the APR limitations off the relevant claims would be obvious, then the answer is yes.

BY MS. WEISKOPF:

Q Okay. We're almost done here.

Can we just scroll to paragraph 128, please?

A Okay. I have it.

Q Here it says "A person of ordinary skill

in the art in 2007 readily understood how to use APR tools to design power distribution networks on integrated circuits."

Do you see that?

A Yes.

Q What do you mean by that?

MR. WILSON: Objection; form.

THE WITNESS: So what I mean by that is, firstly, I provide a timestamp which is with respect to 2007, and then I say it's my view that a POSITA, a person of skill in the art, in that time frame would have found it straightforward, they readily understood how to use these sorts of tools, specifically the automated place and route tools, to perform the placing and routing of the power distribution networks, in other words, the wiring, on integrated circuits. So, in other words, to do the placing and routing of -- or I should rephrase that. Doing the routing of the power distribution networks as part of the place and route process.

BY MS. WEISKOPF:

Q Okay. You're not offering an opinion that LPMM or Bertolet were actually used to perform the power routing for a multiple power domainship,

are you?

MR. WILSON: Objection; form.

THE WITNESS: So we've already discussed LPMM, and I told you -- sorry. We've already discussed Bertolet, and with respect to Bertolet I told you that it was silent on the number of voltages besides identifying the external voltage is 2.5 volts. So I agree with Bertolet, that's true on its own and doesn't teach that.

Let me confirm with respect to LPMM. And, by the way, I have LPMM open. I don't think you've --

(Document was marked Exhibit 1012 for identification.)

BY MS. WEISKOPF:

Q Oh, yeah. Thank you.

Let me introduce that also so that we have a clear record. This is Exhibit 1012, which is LPMM.

A So with respect to LPMM what I would point out is if you look at page 177 of LPMM, which is page 60 of the exhibit, it calls out specifically at the second to the last paragraph "Most EDA tools provide some level of automated

power network synthesis (PNS) capability for the distribution of power across a design. We recommend highly that the implementation of a multi-voltage design utilize this type of PNS capability wherever possible."

So it is here, unlike Bertolet, it is explicitly calling out multi-voltage design. It is, however, true that it doesn't relate that specifically to the meshes, et cetera.

So there is additional information about the use of this in a multi-voltage design, in other words, a design where you have multiple voltages, but it doesn't relate it specifically to global and local meshes. So for that, of course, I'm using the other references.

Q Okay. So LPMM does not disclose by itself performing the steps of claim 1; is that right?

A On its own, yes, I agree. That's why I'm -- at least I have not offered an opinion that on its own it anticipates or renders obvious as a single reference claim 1. I'm using it in combination with Li, Jiang, et cetera, as needed for the various grounds.

MS. WEISKOPF: I don't have any more questions right now, subject to anything from Mr. Wilson.

MR. WILSON: Let's go off the record.

(Whereupon, a recess was taken.)

MR. WILSON: Okay. We have no questions.

MS. WEISKOPF: Okay.

MR. WILSON: And we'll reserve the right to read and sign.

So with that, we can go off the record.

(Whereupon the deposition was concluded at 2:52 p.m. Central Standard Time.)

STATE OF ILLINOIS)
) SS.
COUNTY OF K A N E)

The within and foregoing videoconference deposition of the aforementioned witness was reported remotely by JUNE M. STEARNS, CSR, RMR, and Notary Public, at the date and time aforementioned.

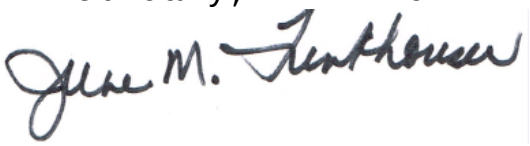
There were present via videoconference during the taking of the deposition the previously named counsel.

The said witness was first duly sworn via videoconference and was then examined upon oral interrogatories; the questions and answers were taken down in shorthand by the undersigned, acting as stenographer and Notary Public; and the within and foregoing is a true, accurate and complete record of all of the questions asked of and answers made by the aforementioned witness, at the time and place hereinabove referred to.

The signature of the witness was not waived, and the deposition was submitted, to the deponent per copy of the attached letter.

The undersigned is not interested in the within case, nor of kin or counsel to any of the parties.

Witness my official signature and seal as Notary Public in and for Kane County, Illinois, on the 19th day of February, A.D. 2024.



JUNE M. STEARNS, CSR, RMR
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February 19, 2024

To: DOUGLAS R. WILSON

Case Name: Advanced Micro Devices, Inc. v. Realtek Semiconductor Corporation
Veritext Reference Number: 6460997
Witness: Vivek Subramanian, Ph.D. Deposition Date: 2/16/2024

Dear Sir/Madam:

Enclosed please find a deposition transcript. Please have the witness review the transcript and note any changes or corrections on the included errata sheet, indicating the page, line number, change, and the reason for the change. Have the witness' signature notarized and forward the completed page(s) back to us at the Production address shown

above, or email to production-midwest@veritext.com.

If the errata is not returned within thirty days of your receipt of this letter, the reading and signing will be deemed waived.

Sincerely,

Production Department

NO NOTARY REQUIRED IN CA

DEPOSITION REVIEW
CERTIFICATION OF WITNESS

ASSIGNMENT REFERENCE NO: 6460997
CASE NAME: Advanced Micro Devices, Inc. v. Realtek Semiconductor Corporation
DATE OF DEPOSITION: 2/16/2024
WITNESS' NAME: Vivek Subramanian, Ph.D.
In accordance with the Rules of Civil Procedure, I have read the entire transcript of my testimony or it has been read to me.
I have made no changes to the testimony as transcribed by the court reporter.

_____ _____
Date Vivek Subramanian, Ph.D.

Sworn to and subscribed before me, a Notary Public in and for the State and County, the referenced witness did personally appear and acknowledge that:

They have read the transcript;
They signed the foregoing Sworn Statement; and
Their execution of this Statement is of their free act and deed.

I have affixed my name and official seal

this _____ day of_____, 20____.

_____
Notary Public

_____
Commission Expiration Date

DEPOSITION REVIEW
CERTIFICATION OF WITNESS

ASSIGNMENT REFERENCE NO: 6460997
CASE NAME: Advanced Micro Devices, Inc. v. Realtek Semiconductor Corporation
DATE OF DEPOSITION: 2/16/2024
WITNESS' NAME: Vivek Subramanian, Ph.D.

In accordance with the Rules of Civil Procedure, I have read the entire transcript of my testimony or it has been read to me.

I have listed my changes on the attached Errata Sheet, listing page and line numbers as well as the reason(s) for the change(s).

I request that these changes be entered as part of the record of my testimony.

I have executed the Errata Sheet, as well as this Certificate, and request and authorize that both be appended to the transcript of my testimony and be incorporated therein.

_____ _____
Date Vivek Subramanian, Ph.D.

Sworn to and subscribed before me, a Notary Public in and for the State and County, the referenced witness did personally appear and acknowledge that:

They have read the transcript;
They have listed all of their corrections in the appended Errata Sheet;
They signed the foregoing Sworn Statement; and
Their execution of this Statement is of their free act and deed.

I have affixed my name and official seal this _____ day of_____, 20____.

_____
Notary Public

_____
Commission Expiration Date

ERRATA SHEET

VERITEXT LEGAL SOLUTIONS MIDWEST

ASSIGNMENT NO: 6460997

PAGE/LINE(S) / CHANGE /REASON

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Date Vivek Subramanian, Ph.D.

SUBSCRIBED AND SWORN TO BEFORE ME THIS _____

DAY OF _____, 20_____ .

_____

Notary Public

_____

Commission Expiration Date

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Federal Rules of Civil Procedure

Rule 30

(e) Review By the Witness; Changes.

(1) Review; Statement of Changes. On request by the deponent or a party before the deposition is completed, the deponent must be allowed 30 days after being notified by the officer that the transcript or recording is available in which:

(A) to review the transcript or recording; and

(B) if there are changes in form or substance, to sign a statement listing the changes and the reasons for making them.

(2) Changes Indicated in the Officer's Certificate. The officer must note in the certificate prescribed by Rule 30(f)(1) whether a review was requested and, if so, must attach any changes the deponent makes during the 30-day period.

DISCLAIMER: THE FOREGOING FEDERAL PROCEDURE RULES ARE PROVIDED FOR INFORMATIONAL PURPOSES ONLY. THE ABOVE RULES ARE CURRENT AS OF APRIL 1, 2019. PLEASE REFER TO THE APPLICABLE FEDERAL RULES OF CIVIL PROCEDURE FOR UP-TO-DATE INFORMATION.

VERITEXT LEGAL SOLUTIONS

COMPANY CERTIFICATE AND DISCLOSURE STATEMENT

Veritext Legal Solutions represents that the foregoing transcript is a true, correct and complete transcript of the colloquies, questions and answers as submitted by the court reporter. Veritext Legal Solutions further represents that the attached exhibits, if any, are true, correct and complete documents as submitted by the court reporter and/or attorneys in relation to this deposition and that the documents were processed in accordance with our litigation support and production standards.

Veritext Legal Solutions is committed to maintaining the confidentiality of client and witness information, in accordance with the regulations promulgated under the Health Insurance Portability and Accountability Act (HIPAA), as amended with respect to protected health information and the Gramm-Leach-Bliley Act, as amended, with respect to Personally Identifiable Information (PII). Physical transcripts and exhibits are managed under strict facility and personnel access controls. Electronic files of documents are stored in encrypted form and are transmitted in an encrypted

fashion to authenticated parties who are permitted to access the material. Our data is hosted in a Tier 4 SSAE 16 certified facility.

Veritext Legal Solutions complies with all federal and State regulations with respect to the provision of court reporting services, and maintains its neutrality and independence regardless of relationship or the financial outcome of any litigation. Veritext requires adherence to the foregoing professional and ethical standards from all of its subcontractors in their independent contractor agreements.

Inquiries about Veritext Legal Solutions' confidentiality and security policies and practices should be directed to Veritext's Client Services Associates indicated on the cover of this document or at www.veritext.com.