UNITED STATES INTERNATIONAL TRADE COMMISSION

Washington, D.C.

In the Matter of **CERTAIN INTEGRATED CIRCUITS, COMPONENTS THEREOF, AND PRODUCTS CONTAINING THE SAME**	**Inv. No. 337-TA-1350**

ORDER NO. 21: CONSTRUING TERMS OF THE ASSERTED CLAIMS

(July 25, 2023)

REALTEK EXHIBIT 2008
AMD v. Realtek
IPR2023-00920

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I. INTRODUCTION

This investigation was instituted by the Commission on January 24, 2023 to determine whether integrated circuits—specifically, central processing units (CPUs), graphics processing units (GPUs), server processors, embedded processors, I/O processors, systems-on-chip (SoCs), Field Programmable Gate Arrays, chipsets, Accelerated Processing Units, and components of each—infringe U.S. Patent Nos. 7,936,245 ("the 245 patent"), 8,006,218 ("the 218 patent"), and 9,590,582 ("the 582 patent"). *See* 88 Fed. Reg. 4205-6 (Jan. 24, 2023). The complainant is Realtek Semiconductor Corp. ("Realtek") and the respondent is Advanced Micro Devices, Inc. ("AMD").

Pursuant to the procedural schedule, the parties filed a joint claim construction chart setting forth certain terms to be construed, and initial and rebuttal claim construction briefs. On June 5, 2023, a *Markman* hearing was held. On June 8, 2023, the parties filed a final updated joint claim chart.[1] EDIS Doc. ID 798110.

II. RELEVANT LAW

"An infringement analysis entails two steps. The first step is determining the meaning and scope of the patent claims asserted to be infringed. The second step is comparing the properly construed claims to the device accused of infringing." *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 976 (Fed. Cir. 1995) (en banc) (internal citations omitted), *aff'd*, 517 U.S. 370 (1996). Claim construction is a "matter of law exclusively for the court." *Id.* at 970-71. "The construction

[1] The briefs and amended chart submitted by the parties are hereafter referred to as:

CIMB	Realtek's Initial *Markman* Brief
CRMB	Realtek's Rebuttal *Markman* Brief
RIMB	AMD's Initial *Markman* Brief
RRMB	AMD's Rebuttal *Markman* Brief
JC	Updated Joint Claim Construction Chart
Tr.	*Markman* Hearing transcript

of claims is simply a way of elaborating the normally terse claim language in order to understand and explain, but not to change, the scope of the claims." *Embrex, Inc. v. Serv. Eng'g Corp.*, 216 F.3d 1343, 1347 (Fed. Cir. 2000).

Claim construction focuses on the intrinsic evidence, which consists of the claims themselves, the specification, and the prosecution history. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005) (en banc); *see also Markman*, 52 F.3d at 979. As the Federal Circuit in *Phillips* explained, courts must analyze each of these components to determine the "ordinary and customary meaning of a claim term" as understood by a person of ordinary skill in the art at the time of the invention. 415 F.3d at 1313. "Such intrinsic evidence is the most significant source of the legally operative meaning of disputed claim language." *Bell Atl. Network Servs., Inc. v. Covad Commc'ns Grp., Inc.*, 262 F.3d 1258, 1267 (Fed. Cir. 2001).

"It is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude.'" *Phillips*, 415 F.3d at 1312 (quoting *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). "Quite apart from the written description and the prosecution history, the claims themselves provide substantial guidance as to the meaning of particular claims terms." *Id.* at 1314; *see also Interactive Gift Express, Inc. v. Compuserve Inc.*, 256 F.3d 1323, 1331 (Fed. Cir. 2001) ("In construing claims, the analytical focus must begin and remain centered on the language of the claims themselves, for it is that language that the patentee chose to use to 'particularly point [ ] out and distinctly claim [ ] the subject matter which the patentee regards as his invention."). The context in which a term is used in an asserted claim can be "highly instructive." *Phillips*, 415 F.3d at 1314. Additionally, other claims in the same patent, asserted or unasserted, may also provide guidance as to the meaning of a

claim term. *Id*. "Courts do not rewrite claims; instead, we give effect to the terms chosen by the patentee." *K-2 Corp. v. Salomon S.A.*, 191 F.3d 1356, 1364 (Fed. Cir. 1999).

The specification "is always highly relevant to the claim construction analysis. Usually it is dispositive; it is the single best guide to the meaning of a disputed term." *Phillips*, 415 F.3d at 1315 (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)). "[T]he specification may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess. In such cases, the inventor's lexicography governs." *Id.* at 1316. "In other cases, the specification may reveal an intentional disclaimer, or disavowal, of claim scope by the inventor." *Id.* As a general rule, however, the particular examples or embodiments discussed in the specification are not to be read into the claims as limitations. *Id.* at 1323; *Kamstrup A/S v. Axioma Metering UAB*, 43 F.4th 1374, 1383-4 (Fed. Cir. 2022) (refusing to read several limitations from embodiments into claims); *Sunoco Partners Marketing & Terminals L.P. v. U.S. Venture, Inc.*, 32 F.4th 1161, 1176 (Fed. Cir. 2022) (holding plain language of claim was nonetheless broader than specification's "preferably" statement). In the end, "[t]he construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be . . . the correct construction." *Id.* at 1316 (quoting *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998)).

In addition to the claims and the specification, the prosecution history should be examined, if in evidence. *Phillips* at 1317; *see Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 913 (Fed. Cir. 2004). The prosecution history can "often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be." *Phillips*, 415 F.3d at 1317; *see Chimie v. PPG Indus. Inc.*, 402 F.3d 1371, 1384 (Fed. Cir.

2005) ("The purpose of consulting the prosecution history in construing a claim is to exclude any interpretation that was disclaimed during prosecution.").

When the intrinsic evidence does not establish the meaning of a claim, then extrinsic evidence (*i.e.*, all evidence external to the patent and the prosecution history, including dictionaries, inventor testimony, expert testimony, and learned treatises) may be considered. *Phillips*, 415 F.3d at 1317. Extrinsic evidence is generally viewed as less reliable than the patent itself and its prosecution history in determining how to define claim terms. *Id*. "The court may receive extrinsic evidence to educate itself about the invention and the relevant technology, but the court may not use extrinsic evidence to arrive at a claim construction that is clearly at odds with the construction mandated by the intrinsic evidence." *Elkay Mfg. Co. v. Ebco Mfg. Co.*, 192 F.3d 973, 977 (Fed. Cir. 1999).

If, after a review of the intrinsic and extrinsic evidence, a claim term remains ambiguous, the claim should be construed so as to maintain its validity. *Phillips*, 415 F.3d at 1327. Claims, however, cannot be judicially rewritten in order to fulfill the axiom of preserving their validity. *See Rhine v. Casio, Inc.*, 183 F.3d 1342, 1345 (Fed. Cir. 1999). Thus, "if the only claim construction that is consistent with the claim's language and the written description renders the claim invalid, then the axiom does not apply and the claim is simply invalid." *Id.*

The construction of a claim term is generally guided by its ordinary meaning. However, courts may deviate from the ordinary meaning when: (1) "the intrinsic evidence shows that the patentee distinguished that term from prior art on the basis of a particular embodiment, expressly disclaimed subject matter, or described a particular embodiment as important to the invention"; or (2) "the patentee acted as his own lexicographer and clearly set forth a definition of the disputed claim term in either the specification or prosecution history." *Edwards Lifesciences LLC v. Cook*

Inc., 582 F.3d 1322, 1329 (Fed. Cir. 2009); *see also GE Lighting Sols., LLC v. AgiLight, Inc.*, 750 F.3d 1304, 1309 (Fed. Cir. 2014) ("the specification and prosecution history only compel departure from the plain meaning in two instances: lexicography and disavowal."); *Omega Eng'g, Inc, v. Raytek Corp.*, 334 F.3d 1314, 1324 (Fed. Cir. 2003) ("[W]here the patentee has unequivocally disavowed a certain meaning to obtain his patent, the doctrine of prosecution disclaimer attaches and narrows the ordinary meaning of the claim congruent with the scope of the surrender."); *Rheox, Inc. v. Entact, Inc*., 276 F.3d 1319, 1325 (Fed. Cir. 2002) ("The prosecution history limits the interpretation of claim terms so as to exclude any interpretation that was disclaimed during prosecution."). Nevertheless, there is a "heavy presumption that a claim term carries its ordinary and customary meaning." *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002) (citations omitted). The standard for deviating from the plain and ordinary meaning is "exacting" and requires "a clear and unmistakable disclaimer." *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1366-67 (Fed. Cir. 2012); *see Epistar Corp. v. Int'l Trade Comm'n*, 566 F.3d 1321, 1334 (Fed. Cir. 2009) (requiring "expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope" to deviate from the ordinary meaning) (citation omitted). As the Federal Circuit has explained, "[w]e do not read limitations from the specification into claims; we do not redefine words. Only the patentee can do that." *Thorner*, 669 F.3d at 1366; *see Continental Circuits LLC v. Intel Corp.*, 915 F.3d 788, 797 (Fed. Cir. 2019); *Unwired Planet, LLC v. Apple Inc.*, 829 F.3d 1353, 1359 (Fed. Cir. 2016) ("[W]e have repeatedly held that it is 'not enough that the only embodiments, or all of the embodiments, contain a particular limitation' to limit claims beyond their plain meaning.").

When a patent includes claims directed to particular methods, the steps recited are not ordinarily construed to require an order unless an order is actually recited. *Interactive Gift Express,*

Inc. v. Compuserve, Inc., 256 F.3d 1323, 1342 (Fed. Cir. 2001) (citing *Loral Fairchild Corp. v. Sony Corp.*, 181 F.3d 1313, 1322 (Fed. Cir. 1999)); *see Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1345 (Fed. Cir. 2008). Alternatively, "a claim 'requires an ordering of steps when the claim language, as a matter of logic or grammar, requires that the steps be performed in the order written, or the specification directly or implicitly requires' an order of steps." *Mformation Techs., Inc. v. Research in Motion, Ltd.*, 764 F.3d 1392, 1398-99 (Fed. Cir. 2014) (citing *TALtech Ltd. v. Esquire Apparel, Inc.*, 279 Fed. Appx. 974, 978 (Fed. Cir. 2008)).

Courts are not required to construe every claim limitation of an asserted patent. *See O2 Micro Intern. Ltd. v. Beyond Innovation Technology Co.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008) (citations omitted); *Vanderlande Indus. Nederland BV v. Int'l Trade Comm'n*, 366 F.3d 1311, 1323 (Fed. Cir. 2004) (noting that the administrative law judge need only construe disputed claim terms). Rather, "claim construction is a matter of resolution of disputed meanings and technical scope, to clarify and when necessary to explain what the patentee covered by the claims." *Id.* at 1362 (quoting *U.S. Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997)); *see also Embrex*, 216 F.3d at 1347 ("The construction of claims is simply a way of elaborating the normally terse claim language in order to understand and explain, but not to change, the scope of the claims.") (citation omitted). In addition, "[a] determination that a claim term 'needs no construction' or has the 'plain and ordinary meaning' may be inadequate when a term has more than one 'ordinary' meaning or when reliance on a term's 'ordinary' meaning does not resolve the parties' dispute." *O2 Micro*, 521 F.3d at 1361. Claim construction, however, is not an "obligatory exercise in redundancy." *U.S. Surgical Corp.*, 103 F.3d at 1568. "[M]erely rephrasing or paraphrasing the plain language of a claim by substituting synonyms does not represent genuine claim construction." *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 863 (Fed. Cir. 2004). However, "there are limits to the court's

duties at the claim construction stage. For example, courts should not resolve questions that do not go to claim scope, but instead go to infringement . . . or improper attorney argument." *Eon Corp. IP Holdings v. Silver Spring Networks*, 815 F.3d 1314, 1319 (Fed. Cir. 2016).

III. TECHNICAL BACKGROUND AND LEVEL OF ORDINARY SKILL

The Asserted Patents cover methods for designing integrated circuits. The claims of the 218 patent encompass the use of "local power meshes" and a "global power mesh" to provide power to multiple power domains within the integrated circuit, where the meshes occupy different layers within a vertical stack. *See* 218 patent at cls. 1, 12, 19. The claims of the 245 patent concern another stacked structure for a "spiral inductor" with portions of layers connected to portions of other layers using vias, and with those portions having particular arrangement or dimensions relative to one another. *See* 245 patent at cls. 1, 4, 8. The claims of the 582 patent similarly concern the design of a "inductor-capacitor (LC)" circuit with a variety of layers and conductive segments within those layers having a particular arrangement and connections to one another. *See* 582 patent at cls. 1, 2, 9.

Only AMD has offered a definition for the person of ordinary skill in the art ("POSITA") for the Asserted Patents.[2] For the 245 patent, AMD argues:

> As of May 19, 2009 (the priority application filing date of the 245 patent), a POSITA pertinent to the subject matter of the 245 patent would have had at least a bachelor's degree in electrical engineering or an equivalent field, and at least 3-4 years of professional experience in the field of integrated circuit design. Prucnal Decl. at ¶ 3. Someone with additional education but less professional experience may qualify as a POSITA, such as someone with a master's degree in E.E. and 1-2 years of professional experience in the field of integrated circuit design or someone with a Ph.D. in electrical engineering. *Id.*

[2] Realtek offers a declaration from expert Dr. Joshua Phinney, which includes opinions on the subject for the 582 patent (CIMB, Ex. E), but does not mention the level of ordinary skill in the art.

RIMB at 10. For the 582 patent, AMD argues the same definition as in the 245 patent, based on a priority date of April 14, 2014. *Id.* at 31. And for the 218 patent, AMD argues, citing the declaration of an expert witness:

> One of ordinary skill in the art as of November 15, 2007 (the filing date listed for a Taiwanese application to which the 218 patent claims priority) would be someone with a bachelor of science degree in computer science, electrical engineering, computer engineering, or a related field, and approximately two years of experience in the design and development of power distribution networks related to integrated circuits, or the equivalent, with additional education and/or research substituting for experience and vice versa. Subramanian Decl. at ¶ 28.

Id. at 18.

AMD is generally persuasive. The 245 and 582 patents disclose a well understood and broadly used circuit element constructed in an allegedly novel way. The definition of a POSITA for those patents is correspondingly broad, although with several years of experience (3-4). Conversely, the 218 patent is more tailored to power delivery networks within an integrated circuit, and AMD's definition is correspondingly narrow, calling for experience directly in power distribution networks for integrated circuits with a lesser number of years' experience (~2). A degree in computer science, however, may not provide the hardware-related knowledge needed for the 218 patent without additional training or experience.

Accordingly, these definitions are accepted for the purposes of this investigation, with the qualification that the educational background for the 218 patent is electrical engineering, computer engineering, or a related field. Also, experience may substitute for education and vice versa; thus, graduate studies in electrical engineering or a related field may substitute for work experience and, likewise, additional work experience may substitute for relevant formal education.

IV. THE ASSERTED PATENTS

The 245 patent, entitled "Stacked Structure of a Spiral Inductor," issued on May 3, 2011 to Kai-Yi Huang, Yuh-Sheng Jean, and Ta-Hsuan Yeh. The 245 patent reports an assignment on its face to Realtek Semiconductor Corp. and claims priority to a foreign application filed May 19, 2009.

The 218 patent, entitled "Power Mesh Arrangement Method Utilized in an Integrated Circuit Having Multiple Power Domains," issued on August 23, 2011 to Chia-Luin Chuang. The 218 patent reports an assignment on its face to Realtek Semiconductor Corp. and claims priority to a foreign application filed November 15, 2007.

The 582 patent, entitled "Semiconductor Device with Inductor-Capacitor Resonant Circuit," issued on March 7, 2017 to Hsiao-Tsung Yen, Yuh-Sheng Jean, and Ta-Hsun Yeh. The 582 patent reports an assignment on its face to Realtek Semiconductor Corp. and claims priority to a foreign application filed April 16, 2014.

A. 245 Patent

The 245 patent has 20 claims. As of the date of this order, claims 1, 2, and 8 are asserted in this investigation. The asserted claims read as follows (with the first instance of the disputed terms highlighted in bold):

> 1. **A structure of a spiral inductor**, comprising:
>
> a first metal layer, comprising:
>
> a first segment;
>
> a second segment; and
>
> a third segment, connected to the first segment, wherein a layout direction of the third segment is different from a layout direction of the first segment and a layout direction of the second segment;
>
> a second metal layer, being positioned under the first metal layer,
>
> the second metal layer comprising:

a fourth segment;

a fifth segment; and

a sixth segment, connected to the fifth segment, wherein a layout direction of the sixth segment is different from a layout direction of the fourth segment and a layout direction of the fifth segment;

a first set of vias, for connecting the first segment with the fourth segment; and

a second set of vias, for connecting the second segment with the fifth segment;

wherein the first segment, the fourth segment and the first set of vias construct a first shunt winding; the second segment, the fifth segment and the second set of vias construct a second shunt winding; and the third segment and the sixth segment construct a crossover region.

2. The structure of the spiral inductor of claim 1, wherein the third segment is positioned between the first segment and the second segment; and the sixth segment is positioned between the fourth segment and the fifth segment.

. . . .

8. The structure of the spiral inductor of claim 1, wherein the spiral inductor is a symmetric spiral inductor.

B. 218 Patent

The 218 patent has 20 claims. As of the date of this order, claims 12-18 are asserted in this investigation. The asserted claims read as follows (with the first instance of the disputed terms highlighted in bold):

12. A power routing structure applied in an integrated circuit having multiple power domains, comprising:

a first partial local **power mesh** having its position corresponding to the position of a first power domain and coupling to the first power domain;

a second partial local power mesh having its position corresponding to the position of a second power domain and coupling to the second power domain; and

a **global power mesh**, coupling to the first local power mesh and the second local power mesh, to provide the power needed by the first power domain and the second domain separately;

wherein the first partial local power mesh and the second partial local power mesh are positioned on the same metal layer while the global power mesh and the first local power mesh are positioned on different metal layers;

wherein the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer; and

wherein the first metal layer and the second metal layer are different layers.

13. The power routing structure according to claim 12, wherein the **global power mesh** is positioned above the first local power mesh.

14. The power routing structure according to claim 13, wherein the first local **power mesh** and the second local power mesh are not electrically coupled.

15. The power routing structure according to claim 12, wherein the **global power mesh** comprises: at least one ground wire; at least one first power wire that provides the power needed by the first power domain; and at least one second power wire that provides the power needed by the second power domain.

16. The power routing structure according to claim 15, wherein the first partial local **power mesh** comprises: at least one first local ground wire that couples to the ground wire of the **global power mesh**; and at least one third power wire that couples to the first power wire and the first power domain.

17. The power routing structure according to claim 16, wherein the second partial local **power mesh** comprises: at least one second local ground wire that couples to the ground wire of the **global power mesh**; and at least one fourth power wire that couples to the second power wire and the second power domain.

18. The power routing structure according to claim 17, wherein the first local ground wire and the second local ground wire share the same ground wire of the **global power mesh**.

C. 582 Patent

The 582 patent has 9 claims. As of the date of this order, claims 1-4 and 9 are asserted in this investigation. The asserted claims read as follows (with the first instance of the disputed terms highlighted in bold):

1. A semiconductor device with an inductor-capacitor (LC) resonant circuit, comprising:

a first insulation layer;

an inductor component, comprising:

a **coil-conductor segment**, located on a surface of the first insulation layer; and

two extension-conductor segments, located on the surface of the first insulation layer, coupled to two ends of the coil-conductor segment respectively, arranged at an interval, and extending outwards relative to the coil-conductor segment, wherein a first region is defined by the two extension-conductor segments and the coil-conductor segment; and

a **capacitor component**, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer, wherein the capacitor component is correspondingly configured outwards relative to the coil-conductor segment, and the capacitor component is not substantially overlapped with the coil-conductor segment,

wherein the capacitor component comprises:

a plurality of connecting segments, extending corresponding to the two extension-conductor segments in a same direction, wherein the **plurality of connecting segments are respectively overlapped with the two extension-conductor segments in a vertical direction**; and

a plurality of electrode segments, located below the first region, wherein one end of each of the plurality of electrode segments is coupled to one of the plurality of connecting segments, and each of the plurality of electrode segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments.

2. The semiconductor device with an LC resonant circuit according to claim 1, further comprising:

a second insulation layer, wherein the **capacitor component** is sandwiched between the first insulation layer and the second insulation layer; and

an electronic component, arranged corresponding to the first region in an embedded manner on a surface, opposite to the capacitor component, of the second insulation layer.

3. The semiconductor device with an LC resonant circuit according to claim 2, wherein the electronic component is one of another **capacitor component**, a transistor component, a diode component, and a resistor component.

4. The semiconductor device with an LC resonant circuit according to claim 1, wherein the first region is defined between the **two extension-conductor segments**.

. . . .

9. A semiconductor device with an inductor-capacitor (LC) resonant circuit, comprising:

a first insulation layer;

an inductor component, comprising:

a **coil-conductor segment**, located on a surface of the first insulation layer; and

two extension-conductor segments, located on the surface of the first insulation layer, coupled to two ends of the coil-conductor segment respectively, arranged at an interval, and extending outwards relative to the coil-conductor segment, wherein a first region is defined by the two extension-conductor segments and the coil-conductor segment; and

a **capacitor component**, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer, wherein the capacitor component further comprises:

a plurality of connecting segments, extending corresponding to the two extension-conductor segments in a same direction, wherein the **plurality of connecting segments are respectively overlapped with the two extension-conductor segments in a vertical direction**; and

a plurality of electrode segments, located below the first region, wherein one end of each of the plurality of electrode segments is coupled to one of the plurality of connecting segments, and each of the plurality of electrode segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments.

V. CLAIM CONSTRUCTION

The disputed claim terms are summarized in the parties' Joint Claim Construction Chart. *See* JC. They are discussed individually below. The parties provided no agreed constructions.

A. 245 Patent – "structure of a spiral inductor"

Realtek's Construction	AMD's Construction
The "structure of a spiral inductor" in the preamble is limiting	The preamble is not limiting

JC at 1.

The only claim construction dispute involving the 245 patent is whether the preamble of claim 1 is limiting. Realtek argues it is limiting "because: (1) it provides antecedent basis for the

claims, and (2) it recites an important structural limitation—a 'spiral inductor'—that the '245 Patent identifies as critical to the invention." CIMB at 3-4 (citing *C.W. Zumbiel Co. v. Kappos*, 702 F.3d 1371, 1385 (Fed. Cir. 2012)). As for antecedent basis, Realtek points to claim 8 which recites, "[t]he structure of the spiral inductor of claim 1, wherein the spiral inductor is a symmetric spiral inductor." *Id.* at 4 (citing 245 patent at cl. 8). Realtek reasons, "[b]ecause claim 8 relies on a limitation found only in the preamble of claim 1, the preamble is limiting." *Id.* (citations omitted); CRMB at 3-4. As to the importance of "spiral inductor" to the patent's alleged invention, Realtek argues, "the specification leaves no doubt that a spiral inductor with specific structural features is the invention" and "[t]he Federal Circuit has held that the preamble is limiting when the Title, Abstract, Field of Invention, and Summary of the Invention all describe the language of the preamble as the invention." CIMB at 5-6 (citing *Deere & Co. v. Bush Hog, LLC*, 703 F.3d 1349, 1357-58 (Fed. Cir. 2012)); CRMB at 4.

In opposition, AMD suggests Realtek seeks its interpretation for the purpose of avoiding prior art transformers. RIMB at 10-11. AMD states, "the ALJ could resolve this dispute by holding that the preamble does not exclude inductors found in transformers" and then offers intrinsic evidence in support of that resolution. *Id.* at 11 ("Thus, both the inventors and the Examiner considered transformers to be relevant to the alleged invention."). Returning to the matter at hand, AMD views the preamble of claim 1 as non-limiting because the body of the claim "disclose[s] a complete 'spiral inductor'" and argues any antecedent basis issues stemming from claim 8 are inapplicable because "[c]laimed subject matter that is merely conventional and known cannot be relied on to support an argument that the preamble is limiting." *Id.* at 12-13 (citing *Cochlear Bone Anchored Sols. AB v. Oticon Med. AB*, 958 F.3d 1348, 1355 (Fed. Cir. 2020)); RRMB at 2 (citing *Am. Med. Sys. v. Biolitec, Inc.*, 618 F.3d 1354, 1359 (Fed. Cir. 2010)).

A preamble is not limiting if the body of the claim defines a structurally complete invention, and the preamble only states the invention's purpose or intended use. *See TomTom, Inc. v. Adolph*, 790 F.3d 1315, 1323 (Fed. Cir. 2015) (citations omitted). A preamble can be limiting if it recites essential structure or steps, or is necessary to give life, meaning, or vitality to the claim. *See id*. (citations omitted). A preamble can also be partially limiting; a portion that provides antecedent basis for a later claim term may be limiting, but another portion that "employs the standard pattern" of reciting a purpose or intended use need not be. *Id*. at 1323-24.

The preamble of claim 1 is limiting. The body of the claim does not recite a structurally complete invention. Most of its limitations are generic first, second, third, etc. "segment[s]" connected to each other in certain "metal layer[s]" and "layout direction[s]." 245 patent at cl. 1. Only the last limitation implies a particular apparatus when it refers to "shunt winding." *Id.* But, even then and according to AMD, "shunt" is only a synonym for "parallel," that is, "shunt" merely describes how the conductor is wound (for instance, "shunt" versus "serial") without specifying whether it is part of a spiral inductor, a generator, a transformer, or some other structure. RIMB at 9; *see* 245 patent at 6:14-17. So there is nothing in claim 1, apart from the preamble, to inform the public as to which field of art this collection of metal "segments" and "layers" pertains, or its utility. "Spiral inductor," as found in the preamble, is therefore necessary to give life, meaning, and vitality to this claim. *TomTom*, 790 F.3d at 1323.

That the body of claim 8 also recites "spiral inductor" further shows the preamble is limiting for antecedent basis reasons. AMD's contention that antecedent basis becomes inapplicable when the dependent claim merely recites well-known features is not supported in the law. *See Cochlear*, 958 F.3d at 1355 (finding antecedent basis may require terms in preamble to be limiting, but these

terms were not at issue); *Am. Med. Sys.*, 618 F.3d at 1359 (addressing term found both in the preamble and in the body of the same independent claim).

Accordingly, "[a] structure of a spiral inductor" in claim 1 of the 245 patent is limiting.

B. 218 patent – "power mesh"

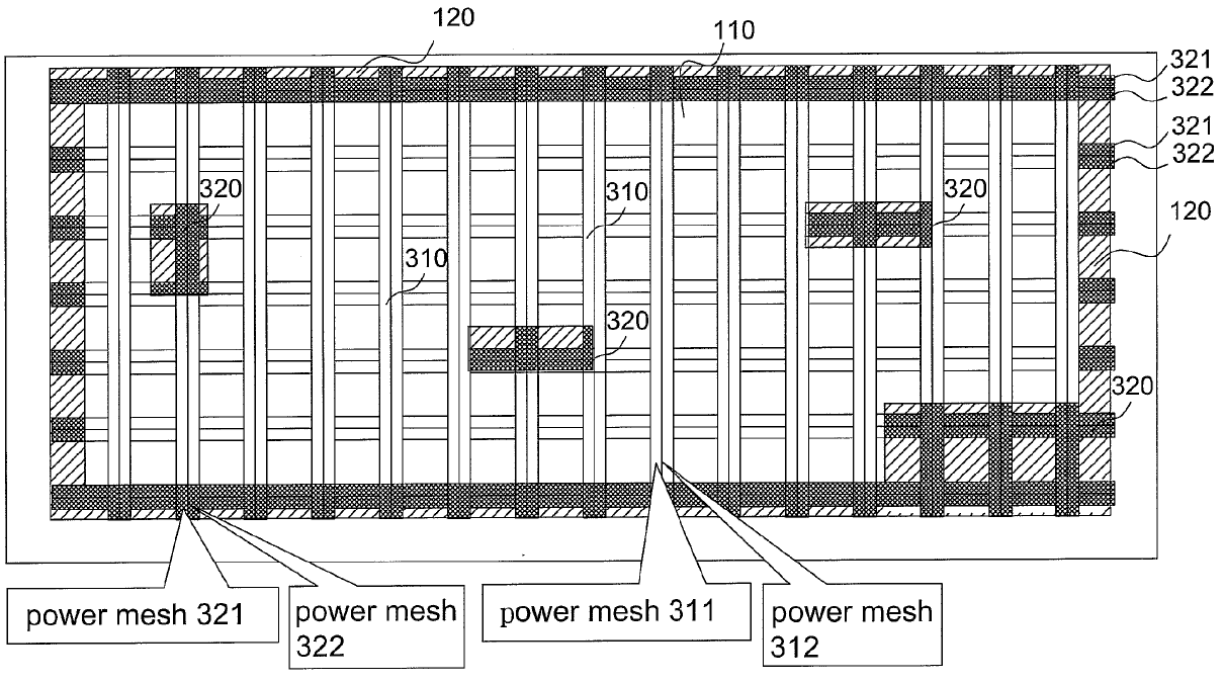
Realtek's Construction	AMD's Construction
No construction needed. A "power mesh" is a "network of wiring capable of distributing power"	Two sets of parallel conductive metal wires that form a net or web-like structure

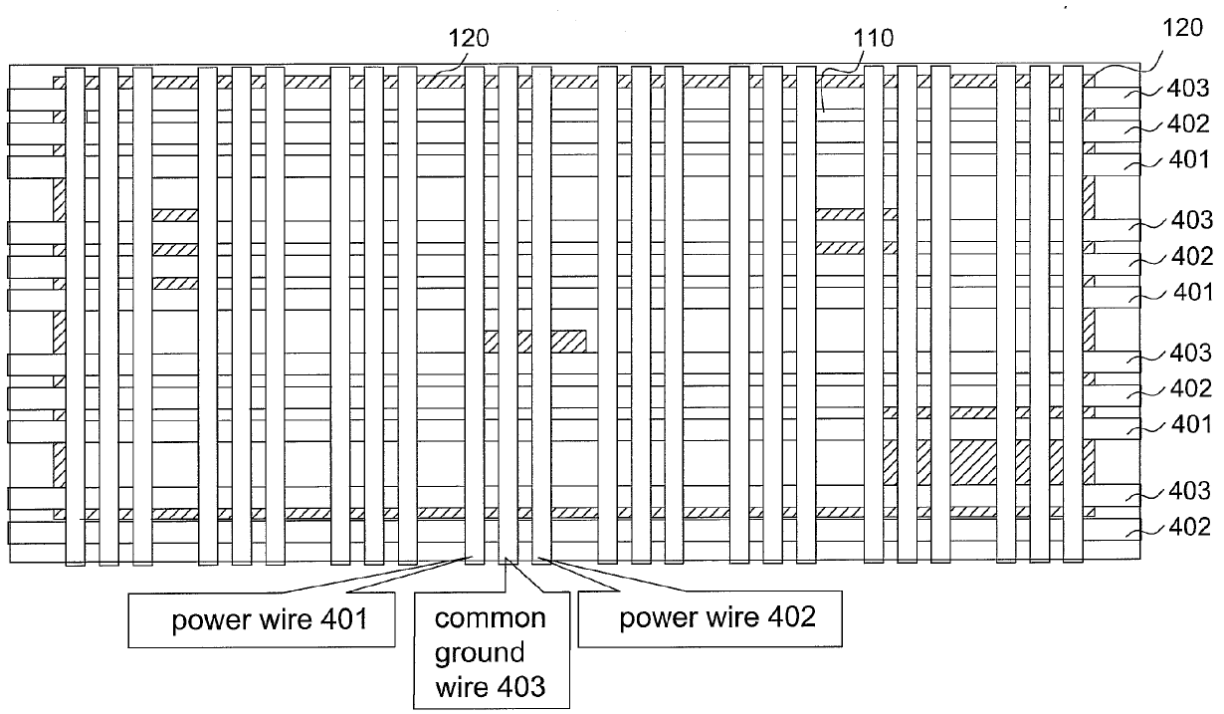
JC at 2.

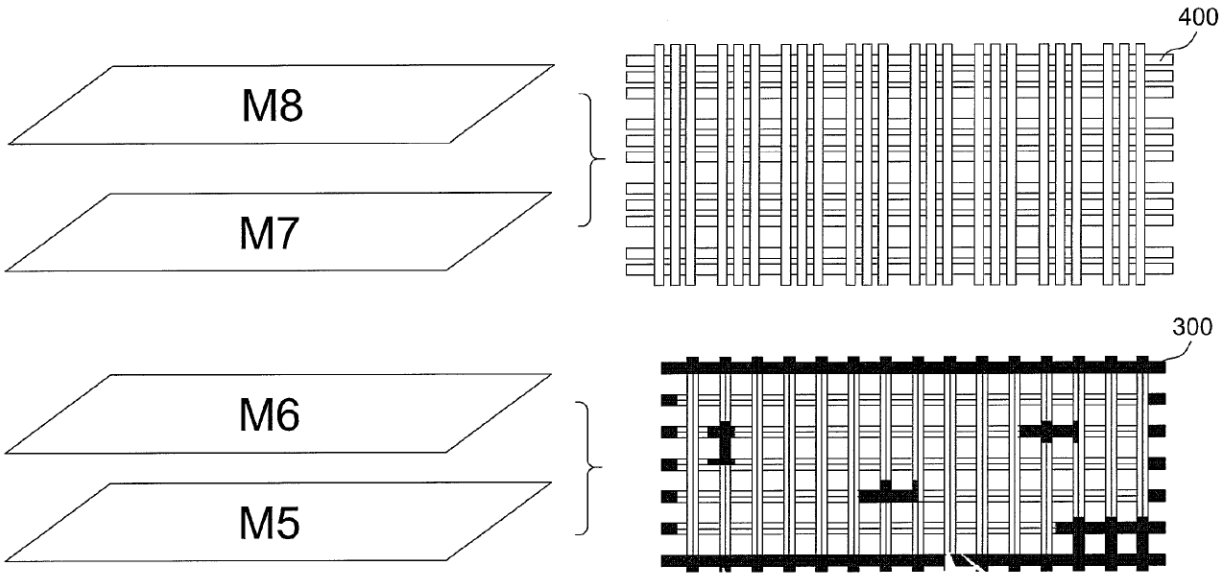
For "power mesh," AMD's construction, "two sets of parallel conductive metal wires that form a net or web-like structure," seeks to give meaning to what is meant by both "power" and "mesh." Specifically, AMD looks to the 218 patent, its expert's opinion, and other extrinsic evidence to support a definition for "mesh" as two sets of parallel wires that form a net or web-like structure. *See generally* RIMB at 18-23. And for "power," AMD proffers that the mesh must be metal and conductive, although in its reply brief, it notes, "AMD would not object to a construction omitting 'conductive metal' and only requiring 'two sets of parallel wires . . .,' and not 'two sets of parallel conductive metal wires . . .'" RRMB at 6 n.3. AMD generally complains that Realtek's briefing "fails to address the actual dispute" which is the definition of "mesh." *Id.* at 2; *see* RIMB at 19 n. 8.

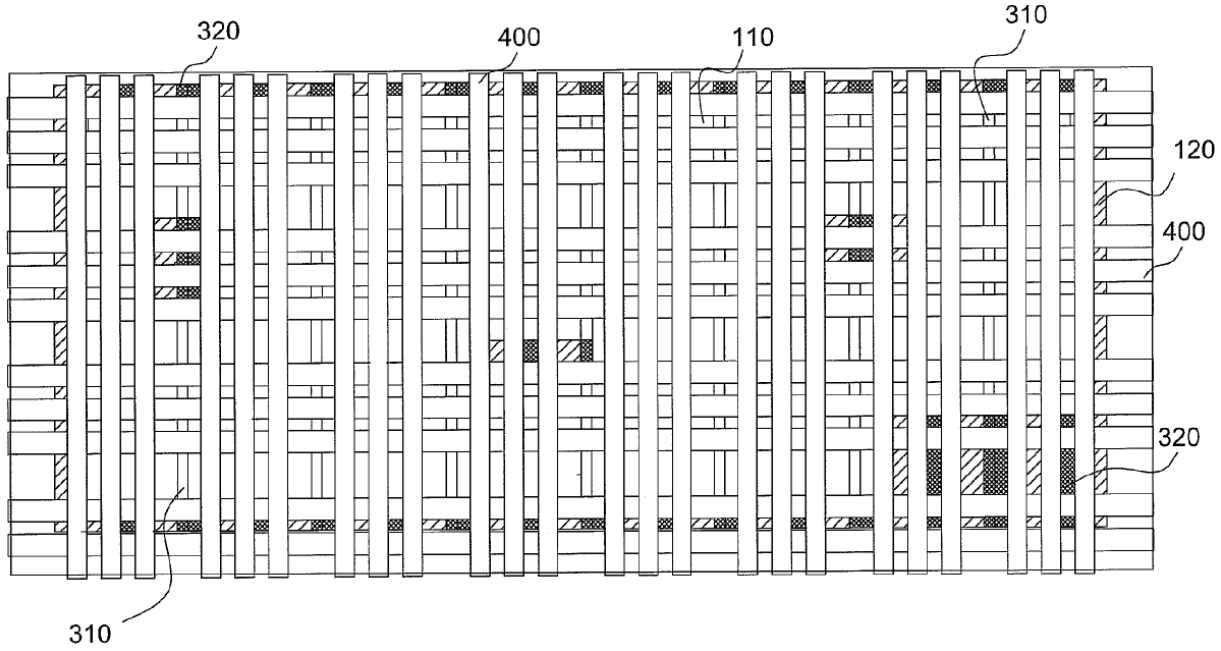
Realtek's briefing indeed criticizes AMD on various grounds without offering its own meanings for "power" or "mesh." For example, at the time of the briefing, Realtek's proposal for "power mesh" was unhelpful—"[a] mesh that comprises wires capable of distributing power." CIMB at 8. Now, as shown above, Realtek proposes "[a] network of wiring capable of distributing power." JC at 2.

Thus, the dispute, as it presently stands, is whether "mesh" should be "[a] network of wiring" or "two sets of parallel wires that form a net or web-like structure." Neither is particularly persuasive. Both parties agree "mesh" is an ordinary English word and there is no inventor lexicography or prosecution disclaimer at issue. CIMB at 8; CRMB at 5; RIMB at 20, 23; RRMB at 2. And in an ordinary sense, what makes a "mesh" a mesh is a plurality of linear members extending in different directions creating intersections. As AMD notes, the members need not intersect each other at right angles nor form negative spaces of any particular shape. *See* RRMB at 22-23. And as Realtek notes, no parallelism between members is needed either. *See* CIMB at 9. "Meshes" can include perfectly orthogonal patterns of linear members as well as asymmetric, irregular, collections—so long as there are intersections. Realtek argues that "the wires in the embodiments do not intersect" and "[t]he '218 Patent never mentions wires that 'intersect' or any other synonym, such as 'cross,' 'crisscross,' 'meet,' 'transect,' or 'traverse'" (CRMB at 6), but the patent's figures plainly show overlapping intersections in every relevant figure:




120
110
120
403
402
401
403
402
401
403
402
401
403
402
power wire 401
common ground wire 403
power wire 402


400
M8
M7
300
M6
M5



218 patent at Figs. 3-6 (assigning same element number for intersecting members in different orientations).[3]

Realtek's "network" definition does not touch upon this important feature. AMD's proposal does, but only through the vagueness of "net" or "web-like structure," which invites additional construction. It may also be helpful to hear expert evidence from Realtek on how a skilled artisan would understand the term. Accordingly, ultimate constructions for "mesh" and "power mesh" are deferred until after the evidentiary hearing, and any continued argument from the parties should take into account the above determinations.

C. 218 Patent – "global power mesh"

Realtek's Construction	AMD's Construction
Realtek would accept the ALJ's proposal: "a power mesh that need not be distributed across the full area of the chip circuitry and need	A power mesh distributed across the full area of the chip's circuitry for conducting external power into the chip

[3] The parties noted at the Markman hearing that Figure 3 contains an error in that elements labeled 312 and 322 are ground wires and not a power mesh. Tr. at 24:16-25:4.

not conduct external power directly into the chip."	

JC at 2.

For "global power mesh," the parties dispute the meaning of "global." Prior to the Markman hearing, Realtek offered the construction "a power mesh capable of distributing power to multiple power domains." CIMB at 13; CRMB at 8. Its briefing generally did not address why this definition was correct but instead criticized AMD for requiring the global mesh be distributed, in a geographic sense, across the entire chip and that it conduct external power into the chip. *See generally* CIMB at 13-17; CRMB at 8-11. Realtek contends, "[b]oth proposals are improper because they seek to import limitations that either are not in the claims or intrinsic record, or that are features of recited embodiments, which do not limit the claims." *Id.* at 13; CRMB at 8. For the distribution aspect, Realtek states, "[t]he specification makes no mention of any embodiment in which the global power mesh is distributed across the full area of the chip's circuitry. AMD's construction is based on its subjective interpretation of the embodiments in Figures 4–6." CRMB at 9. And for the external power aspect, it argues, "the Federal Circuit prohibits defining a structural claim limitation in functional terms when the claims do not include functional language" and "[o]nce the global power mesh receives external power, it already is in the chip," making AMD's construction imprecise. *Id.* at 10-11.

AMD argues that "a POSITA would have understood that 'global' imparts an additional meaning—namely, that 'global' means over the full area." RIMB at 24 (citing Subramanian Decl. at ¶¶ 73-75). AMD finds support in the intrinsic evidence:

> Every embodiment in the 218 patent shows and describes the "global" power mesh extending over the entire chip. The patent describes the "chip 100" having the multiple power domains (*see* Fig. 1). EX. 104 at 2:63-67. Fig. 6 shows the chip 100

with the "local power mesh in Fig. 3 and the global power mesh in Fig. 4." *Id*. at 2:57-59; 5:8-10. The "global power mesh 400" (*id*.) is annotated below and is plainly distributed across the full area of the chip's circuitry:

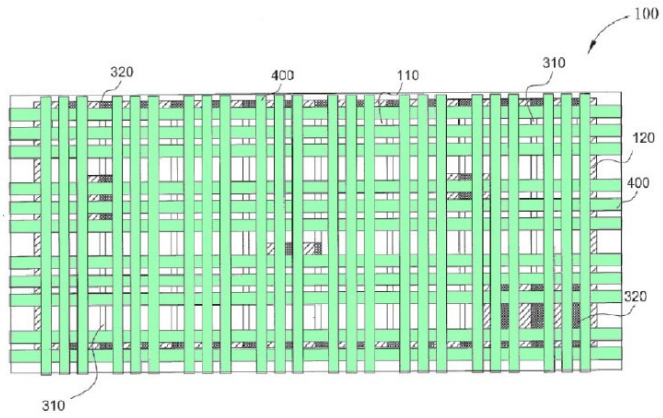


FIG. 6

Fig. 6 is consistent with the other figures in the 218 patent showing the global power mesh. In each, the global power extends over the entire chip. *See* Figs. 4 and 5. Moreover, the specification states that the "***local*** power mesh 300" (*see* Figs. 3 and 6) is "evenly distributed on top of the ***entire*** chip circuitry." *Id*. at 5:60-61. A POSITA would have understood that, with the "local" power mesh extending over the entire chip, at a minimum so must the "global" power mesh. Subramanian Decl. at ¶ 74. This is consistent with the common meaning of the terms (that is, it would be illogical for a "global" mesh to be smaller than a "local" mesh). It also conforms to the specification, which shows that the global power mesh 400 is positioned on metal layers above the local power mesh 300 and is at least co-extensive therewith (*see* Figs. 5 and 6). This is also consistent with the specification's teaching that the "partial local power meshes" only extend over the power domains and not the entirety of the chip. *See* EX. 104 at 5:61-6:1. Thus, the partial local power meshes cover sub-areas of the chip, and the local and global power meshes extend over its entirety. Subramanian Decl. at ¶ 74.

RIMB at 24-25; *see* RRMB at 7-9. AMD also points to the prosecution history, alleging the applicant had distinguished prior art based on "global power mesh" conducting external power to the chip. RIMB at 26 (citing RIMB, Ex. 107 at -2282). As for construing structural limitations with functional language, AMD argues Realtek's cited caselaw is pre-*Phillips* and otherwise not reliable. *See* RRMB at 9-10.

Realtek has the more persuasive position. The 218 patent gives no outright explanation for why a "global" mesh is "global" nor for its counterpart term, "local." For example, contrary to what

would be an ordinary understanding, a "local" mesh is disclosed in at least one embodiment as "evenly distributed on top of the *entire* chip circuitry" in the same way as a "global" mesh might be. 218 patent at 5:59-6:4 (emphasis added). And while a global mesh is shown as covering the entire circuitry in the figures of the 218 patent (*see, e.g.*, *id.* at Fig. 3), there are a variety of features that could be similarly read-in just because they appear in a patent drawing, but no party suggests doing so; *e.g.*, parallel wires must be in groups of three or must have a rectangular shape when viewed from above (*see id.*). So there is little in the specification to find that a "global" mesh is only a mesh that is "distributed across the full area of the chip's circuitry."

There is also little support for finding that "global" means conducting power directly from an external source. AMD's specification excerpts only indicate how a "global power mesh" is used by the invention of the 281 patent, not what the phrase means:

> The global power mesh couples to the external power (such as: by way of the I/O pin of the chip) to conduct the external power into the chip while the local power mesh couples to the global power mesh and the chip circuitry (that is the internal circuits of the chip corresponding to the power domains 110, 120).
>
> . . . .
>
> In one embodiment of the invention, the global power mesh 400 is distributed just above the local power mesh 300 so that the global power mesh 400 can conduct the external power into the chip by via to couple to the local power mesh 300 located below.
>
> Similarly, as the global power mesh 400 is to supply voltage to the entire chip, each of the horizontal and the vertical power supply wires must comprise one common ground wire 403 and two power wires 401, 402.
>
> . . . .
>
> It should be noted that the arrangement method and its related structure disclosed is just a preferred example of the invention and should not be construed as any limitation on the implementation of the invention. The local power mesh 300 can be omitted in the invention. Only the global power mesh 400 is used to conduct the external power into the chip. For example, the global power mesh 400 can be placed on the metal layers M5, M6 directly as shown in FIG. 4. If the density of the global

> power mesh is high enough as mentioned previously, it can be assured that all the circuits in the chip positioned below can be coupled to the global power mesh 400 by via to receive the ground potential VGND and the working voltage VDD1, VDD2 conducted by the global power mesh 400. Such equivalent changes and modifications of the present invention are considered to be within the scope of the present invention.

281 patent at 3:27-30, 4:25-34, 6:9-24; *see* RIMB at 25-26 RRMB at 10. It would be improper to treat this use of a "global power mesh" as its defintion even if so used consistently across all disclosed embodiments. *Hill-Rom Servs., Inc. v. Stryker Corp.*, 755 F.3d 1367, 1371 (Fed. Cir. 2014) ("[W]e do not read limitations from the embodiments in the specification into the claims.").

AMD's construction is also not aided by the prosecution history. In the cited excerpt, the patentee distinguished prior art U.S. Patent No. 7,234,124 ("Chen") based on the reference's failure to disclose "electrical connections" between certain grids that had been identified by the Examiner as embodying global mesh 400 and local mesh 300 of the 218 patent:

It is respectfully submitted that the combination of references cited by the Examiner fails to teach or suggest at least the above-emphasized features of independent claim 12.

As set forth above, Ladanza is silent on the structure of the chip-level connection declaration 501. In the Examiner's rejection of claim 12 (beginning on page 9 of the Office Action), the Examiner equates the global power mesh 400 and the local power mesh 300 of the present application as being comparable to the second power grid 22 and the first power grid 21 of Chen (FIG. 2). Applicant disagrees. In the present application (see paragraph [0020], for example), the global power mesh 400 couples to the external power (such as: by way of the I/O pin of the chip) to conduct the external power into the chip while the local power mesh 300 couples to the global power mesh 400 and the chip circuitry. In other words, the internal circuits of the chip correspond to the power domains 110, 120. Then, the external power will be inputted into the chip circuitry by way of the global power mesh 400 and the local power mesh 300.

In contrast, Chen has no electrical connections between the second power grid 22 and the first power grid 21 and no electrical connections between the VDD_g power network 11 and the VDD_i-VDD_n power networks 15 (see FIGS. 1 and 2). In addition, the VDD_g power network 11 and the VDD_i-VDD_n power networks 15 respectively have their own power sources.

RIMB, Ex. 107 at -2282. Despite the patentee's subsequent concluding remarks,[4] that grid 22 and grid 21 are not connected, or network 11 and networks 15 have separate power sources (as in Chen), is only relevant because of the limitation "a global power mesh, coupling to the first local power mesh and the second local power mesh, to provide power needed by the first power domain and the

---

[4] The patentee had distinguished Chen and then stated:

> It is respectfully submitted that Ladanza and Chen fail to teach or suggest that "the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layers and a plurality of vertical power supply wires placed on a second metal layer, and wherein the first metal layer and the second metal layer are different layers" as is recited in independent claim 12 of the present application. Thus, all elements of claim 12 are not taught by the combination of references utilized by the Examiner.

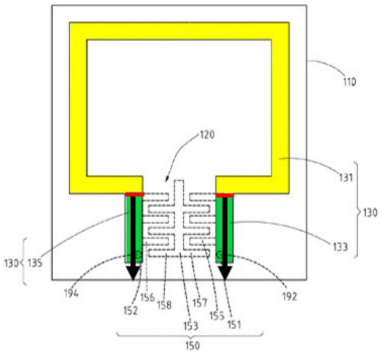
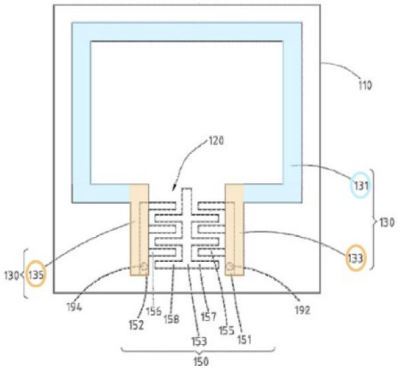
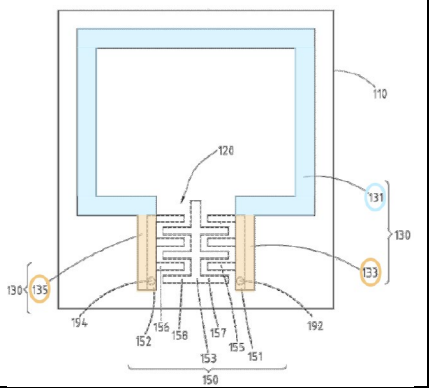
RIMB, Ex. 107 at -2282. There is no connection between this emphasized claim limitation and the patentee's remarks on Chen.

second domain separately." *Id.* at -2281-2. There is nothing, in this paper at least, to suggest that the Examiner's Section 103 rejection was overcome because of what is meant by "global," let alone clear and unmistakable disclaimer by an applicant. *Thorner*, 669 F.3d at 1366-67.

With that said, AMD is correct that "a POSITA would have understood that 'global' imparts an additional meaning—namely, that "global" means over the full area. Otherwise, the claims would have simply recited generic 'first,' 'second,' 'third,' etc. power meshes." RIMB at 24; *see* RRMB at 9; Tr. at 28:17-29:3. And Realtek's original proposed construction more closely reflects this added meaning. In ordinary terms, a "local power mesh," *inter alia*, supplies power to a local area. A "global power mesh," *inter alia*, supplies power to multiple local areas. Indeed, the invention is rooted in a solution to a problem that concerns supplying distinct power levels to distinct portions of chip circuity. *See, e.g.*, 281 patent at 1:26-28, 2:33-37, 6:41-46, cls. 1, 12, 19. Neither AMD nor Realtek point to any embodiments in which a "global power mesh" supplies power to just one "local power mesh" or less than the whole chip/circuit. And contrary to AMD's argument (RRMB at 7), this basic, broad construction does not have the exact same scope as the recited limitation "a global power mesh, coupling to the first local power mesh and the second local power mesh, to provide the power needed by the first power domain and the second domain separately" so as to render it superfluous.

Accordingly, a "global power mesh" means a "power mesh capable of distributing power to multiple power domains." Realtek's revised construction ("a power mesh that need not be distributed across the full area of the chip circuitry and need not conduct external power directly into the chip") is technically accurate as discussed above, and resolves the parties' dispute, but is a disfavored negative construction and does not actually define the term "global power mesh."

D. 582 Patent - "two extension-conductor segments"

Realtek's Construction	AMD's Construction
Ordinary and customary meaning, "portions of the inductor that extend approximately perpendicular from where each joins the coil conductor segment, as shown in green in the diagram below" 	The extension-conductor segments (highlighted in orange) may join the ends of the coil-conductor segment (highlighted in blue) as shown in the diagrams below:  Or: 

JC at 2-3.

As shown above, the parties identify "two extension-conductor segments" as requiring construction and then, according to the most recent joint chart, offer competing understandings of where the "extension-conductor segments" would begin and end within Figure 5 of the 582 patent. JC at 2-3. Neither annotated drawing relates to what the meaning of the three-word phrase, "extension-conductor segments," might be, however. *E.g., compare* RIMB at 32 (presenting plain English definitions) *with id.* at 33 (presenting annotated drawings); CRMB at 12 ("[T]he central

question being: 'where do the 'extension-conductor segments' begin and where does the 'coil-conductor segment' end?"). Thus, the "constructions" are unrelated to a *Markman* process. *Embrex*, 216 F.3d at 1347 ("The construction of claims is simply a way of elaborating the normally terse claim language in order to understand and explain, but not to change, the scope of the claims."); *SRI Int'l v. Matsushita Elec. Corp. of Am.*, 775 F.2d 1107, 1118 (Fed. Cir. 1985) ("A claim is construed in the light of the claim language, the other claims, the prior art, the prosecution history, and the specification, not in light of the accused device.").

Moreover, the parties have each furnished expert declaration supporting their respective positions. *See* CIMB at 22 (citing CIMB, Ex. E (Phinney Decl.) at ¶ 32); RIMB at 33-35 (citing RIMB, Ex. 101 (Prucnal Decl.) at ¶¶ 97-109). Inasmuch as the parties' dispute is one over claim construction, then, additional expert evidence may be helpful in resolving it.

Accordingly, this dispute is deferred until the evidentiary hearing to the extent it remains relevant.

E. 582 Patent – "coil-conductor segment"

Realtek's Construction	AMD's Construction
Realtek would accept the ALJ's proposal: "inductor coil"	No construction needed except as specified for "extension-conductor segment" above

JC at 3.

According to the updated joint chart, the parties seek a construction of "coil-conductor segment." While Realtek has proposed what might be a proper construction (Tr. at 58:3-19), AMD's illustration-based proposal suffers from the same problem identified above with "two extension-conductor segments."

Based on the parties' briefing, the dispute over this term is really over where the "coil-conductor segment" ends and the "extension-conductor segment" begins, as explained above.

Accordingly, this dispute, to the extent it requires resolution, will be resolved at the same time as "extension-conductor segment."

F. 582 Patent – "capacitor component"

Realtek's Construction	AMD's Construction
Ordinary and customary meaning, "a component that includes one or more capacitors"	One capacitor, as opposed to multiple capacitors separated by switches

JC at 3.

Next, the parties dispute the meaning of "capacitor component." Realtek contends the 582 patent specification supports its ordinary meaning of "a component that includes one or more capacitors" through disclosures such as "[a]ll the capacitors in the capacitor component 150 in these embodiments . . .." CIMB at 30 (citing 582 patent at 4:26-27). Realtek views AMD's construction as based solely on an erroneous prosecution history disclaimer. *Id.* at 32-33; CRMB at 17-20.

AMD's construction is not based on the claim language, which lacks any reference to "switches," and is instead purportedly "taken directly from the file history of the 582 patent and represent[s] the sole reason the Examiner allowed the claims." RIMB at 36; RRMB at 13 ("The file history is decisive here . . ."). AMD describes the relevant history as: the applicant facing final rejection, an unsuccessful amendment-after-final by the applicant, an examiner-initiated interview revealing an additional anticipatory reference (U.S. Pub. No. 2015/0145615 ("Jing")), a further amendment included within a Request for Continued Examination (RCE), and then allowance based on that amendment. *See generally* RIMB at 36-40 (citing RIMB, Ex. 108). AMD highlights remarks made by the Examiner in the interview summary and notice of allowance as the actual moment of the disclaimer and, correspondingly, its preferred construction:

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

The Examiner notified the Applicant that the amendment made to claim 1 (see Amended claims dated 9/16/2016) does not overcome the reference of record Daley et al. Further, a new search was conducted within the allotted time and the Examiner cites a new prior art that also reads on claim 1. Jing et al. discloses in Fig. 5 a semiconductor device with an LC circuit comprising the limitations recited within claim 1. The Examiner notified the Applicant that the amendment dated 9/16/2016 will not be entered. The Applicant acknowledged and stated that an RCE will most probably be submitted.

RIMB, Ex. 108 at -2746;

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance: As per claims 1 and 11, the closest prior art Jing et al. US Patent 9,270,247 (of record) discloses in Fig. 7 a semiconductor device with an LC resonant circuit comprising all of the limitations recited therein **EXCEPT** "wherein the plurality of connecting segments of the capacitor component are respectively overlapped with **the two extension-conductor segments**". Jing et al. discloses an inductor component 705 including legs or "extension-conductor segments" 715 and 720. The inductor 705 is connected to TWO separate finger capacitors or "capacitor components" 725 and 730. Each of the capacitor components overlaps with only a single one of the "extension-conductor segments" in a vertical direction and not both (i.e. "the two extension-conductor segments") as recited within the claims. Further, each of the finger capacitors or "capacitor components" 725 and 730 is its own separate capacitor structure separated by switches 735 as shown in Fig. 7, and thus elements 725 and 730 together cannot be interpreted as "a capacitor component".

id. at -2770-1 (emphasis in original); RIMB at 38-39. Figure 7 of the Jing reference is reproduced below, where elements 725 and 730 are capacitors separated by switches 735:

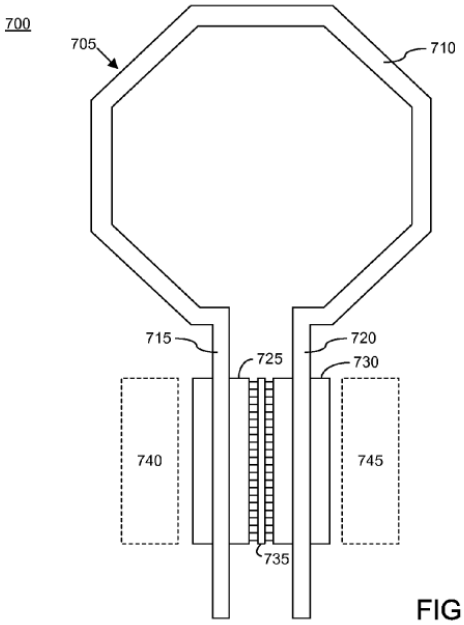


FIG. 7

See RRMB at 7. Summarizing, AMD states, "[t]here can be no doubt from the above record that while the applicants made multiple efforts to convince the Examiner to allow independent claim 1, in the end, they agreed to add the [overlapping limitation] of claims 4 and 5 into claim 1 and in doing so acquiesced to the Examiner's understanding of the claims." RRMB at 17-18 (citing, *inter alia*, *Elkay Mfg. Co. v. Ebco Mfg. Co.*, 192 F.3d 973, 978-9 (Fed. Cir. 1999)). Because of this, according to AMD, "the claim does not allow for, as Realtek urges, multiple capacitors to be lumped together as the 'capacitor component' to meet the 'respectively overlapped' limitation. *Id.* at 15.

Prosecution history disclaimer has not been shown for two reasons. First, there was no "clear and unmistakable" disclaimer with respect to "switches." *Thorner*, 669 F.3d at 1366-67. As Realtek notes, none of the cited excerpts are statements by the applicant regarding the differences between Jing and the claimed invention. They are statements by the Examiner describing their own understanding of the claims and of Jing's disclosure. Nor is it clear that the applicant acquiesced to AMD's proposed "switches" limitation, because according to the record of the interview, where the Examiner indicated they would reject the then-pending claims, there was no discussion of switches.

And acquiescence is even less clear in light of the applicant explicitly declining to "conced[e] the appropriateness of the Examiner's rejection":

> 5. (Previously Presented) The semiconductor device with an LC resonant circuit according to claim 4, wherein the plurality of connecting segments are respectively overlapped with the two extension-conductor segments in a vertical direction.
>
> . . . .
>
> Allowable Subject Matter
>
> Applicants gratefully acknowledge the Examiner's indication that claim 5 would be allowable if rewritten in independent form. Without conceding the appropriateness of the Examiner's rejection, claim 1 has been amended to include features from claims 4 and 5, and new claim 11 has been added to include the limitations of original claims 1, 4 and 5. Accordingly, claims 1 and 11 are now in condition for allowance. The pending dependent claims depend from allowable independent claims and are allowable for at least this reason.

RIMB, Ex. 108 at -2734, -2757. If the applicant did not agree claim 5 is needed to achieve patentability, then it is difficult to conclude that the applicant clearly and unmistakably limited the ordinary scope of "capacitor component" to exclude more than one capacitor separated by switches.

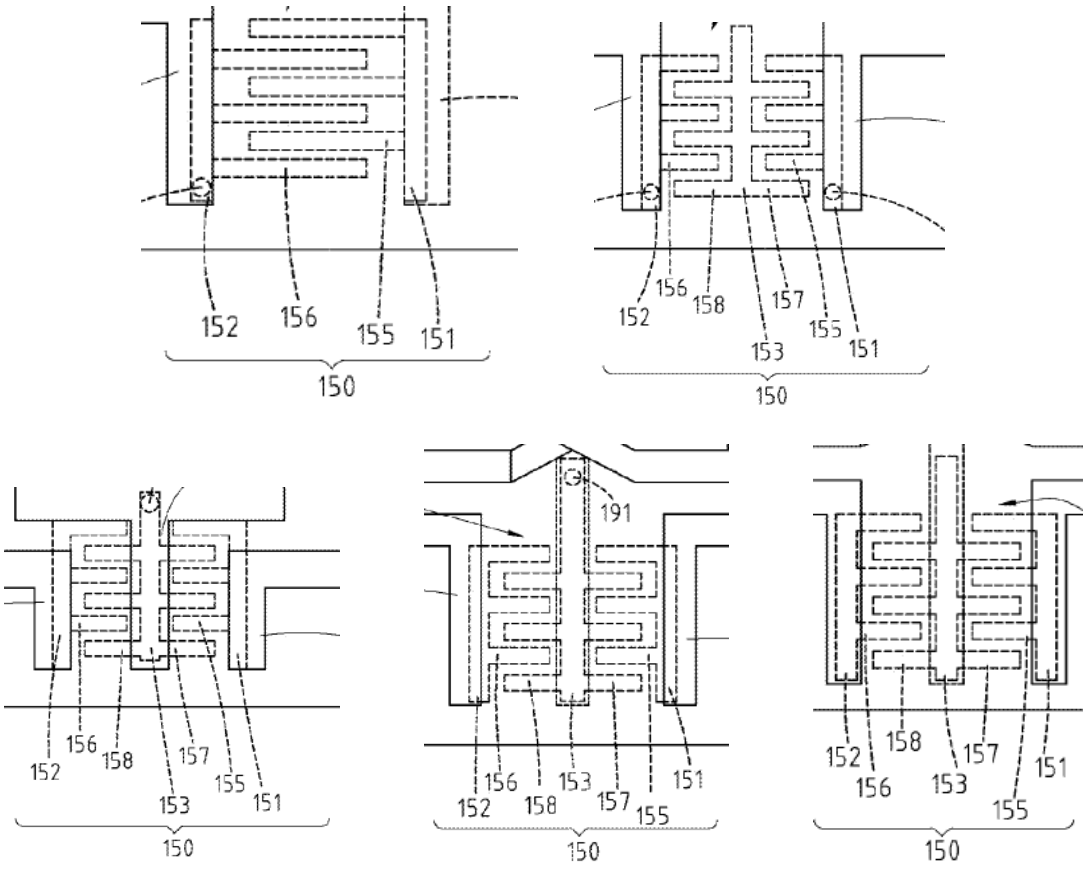
There is therefore no clear and unmistakable evidence that the applicant "adopt[ed]" the Examiner's "separated by switches" characterization "to overcome the examiner's rejection," as AMD argued at the *Markman* hearing. Tr. at 87:3-6.

This sets apart the present facts from cases like *Elkay* and *Biogen*, cited by AMD, because there the courts relied on prior art-distinguishing remarks coming from *both* the Examiner and applicant. *Elkay*, 192 F.3d at 979 ("Elkay's argument that its statement distinguishing Krug on the basis of Krug's use of separate feed tubes was insignificant is particularly unpersuasive in view of the Examiner's response to that statement."); *Biogen Idec, Inc. v. GlaxoSmithKline LLC*, 713 F.3d 1090, 1097 n.6 (Fed. Cir. 2013) ("This case deals not only with applicants letting stand an examiner's

narrow characterization of a claim term, but also their adoption of that characterization to overcome the examiner's enablement rejection. Thus, the acquiescence cases are inapposite."); *see* RIMB at 40 n. 11 ("*Elkay* is right on point"); Tr. at 86:14-22 ("But there are cases that have just addressed this specifically like *Biogen* from the Federal Circuit . . .").

Second, there was no clear and unmistakable disclaimer with respect to "one capacitor." Again, none of the cited excerpts are statements by the applicant regarding the differences between Jing and the claimed invention. And even if the applicant knew that the Examiner understood "capacitor component" to be limited to a single capacitor and intended to allow the pending claims (if rewritten) because of that construction, it is a plainly incorrect construction regardless of the prosecution history. *Elbex Video, Ltd. v. Sensormatic Electronics Corp.*, 508 F.3d 1366, 1371-3 (Fed. Cir. 2007) (citing *Biotec Biologische Naturverpackungen GmbH & Co. KG v. Biocorp, Inc.*, 249 F.3d 1341, 1348 (Fed. Cir. 2001)). "[I]ncorrect statement[s] in the prosecution history do[] not govern the meaning of the claims." *Rambus Inc. v. Infineon Techs. AG*, 318 F.3d 1081, 1090 (Fed. Cir. 2003).

To the extent the Examiner assumed that the allowed claims did not encompass "multiple capacitors . . . lumped together as the 'capacitor component,'" that assumption was incorrect. RRMB at 15. The 582 patent exclusively discloses interlaced finger structures as the "capacitor component 150" in all of its embodiments:



Id. at Figs. 2, 5, 8, 11, 15; *see id.* at Fig. 17. And the patent fairly discloses that each capacitor component 150 is made up several capacitors arranged in parallel:

> The capacitor component 150 may be in a single-ended (as shown in FIG. 1 to FIG. 3) or differential (as shown in FIG. 4 to FIG. 6) form. *All capacitors in the capacitor component 150 in these embodiments share a same metal layer*; however, the present invention is not limited thereto. Capacitors connected in parallel may be formed by using various different metal layers to increase a capacitance value, or a semiconductor transistor capacitor arranged below the capacitor component 150 may be further connected in parallel or used.

582 patent at 4:24-33 (emphasis added). AMD disputes this reading, stating that in the embodiments of Figures 1-6 there is just a single capacitor 150; but it offers only attorney argument for support. *See* RRMB at 19. AMD does not dispute, though, that a capacitor can be made by "just two slabs of metal," so that even the simplest of capacitor components disclosed in the 582 patent would arguably comprise multiple individual capacitors. Tr. at 76:4-77:14.

Thus, if "capacitor component" is limited to just one capacitor, then in none of the 582 patent's embodiments are there capacitor "connecting segments" "respectively overlapped with the two extension-conductor segements [of the inductor component]" according to independent claims 1 and 9. As shown and disclosed, each "capacitor component" (including however many "connecting segments" it may have) would only be underneath one "extension-conductor segment"—mirroring the arrangement of Jing. RIMB, Ex. 108 at -2770 (Examiner stating, "[e]ach of the capacitor components overlaps with only a single one of the 'extension-conductor segments' in a vertical direction and not both (*i.e.* 'the two extension-conductor segments') as recited within the claims."). A construction that excludes all embodiments from a patent, as this one does, is unlikely to be correct. *EPOS Technologies Ltd. v. Pegasus Technologies Ltd.*, 766 F.3d 1338, 1347 (Fed. Cir. 2014); *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996).

Accordingly, "capacitor component" is "a component that includes one or more capacitors."

G. 582 Patent – "plurality of connecting segments are respectively overlapped with the two extension-conductor segments in a vertical direction"

Realtek's Construction	AMD's Construction
Ordinary and customary meaning, "plurality of connecting segments are respectively overlapped with the two extension-conductor segments in a vertical direction"	The plurality of connecting segments of the capacitor component are overlapped with the two extension-conductor segments, wherein each connecting segment of the capacitor component overlaps with a respective extension-conductor segment in a vertical direction

JC at 3.

For "plurality of connecting segments are respectively overlapped with the two extension-conductor segments in a vertical direction," AMD contends first that both extension-conductor segments must be overlapped with members of the "plurality of connecting segments" (*see* RIMB

at 39-40), and second that "each" structure that might qualify as a "connecting segment" within an accused capacitor component must overlap with an "extension-conductor segment" (*see* RRMB at 14-15; Tr. at 90:21-91:11). Realtek apparently does not dispute AMD's first contention, but it does dispute the second. *See* Tr. at 73:1-5 ("One or more of the connecting segments has to be overlapped with one of the extension-conductor segments, and the other connecting segment, one or more connecting segments, have to be overlapped with the other extension-conductor segments. That's all the claim requires.").

AMD supports both contentions principally by arguing that there was disavowal during prosecution. *See* RRMB at 13-18. But in addition to the lack of any "clear and unmistakable" disclaimer, as explained above, there could not have been disavowal regarding the connecting segments because the Examiner did not identify any such structures in Jing. Rather, the Examiner's Reasons for Allowance only referenced whole capacitor components (finger capacitor 725 or 730) as failing to overlap with both of Jing's extension-conductors (legs 715 and 720). RIMB, Ex. 108 at -2770-1. So there was never any moment where the applicant distinguished Jing based on the nature of overlap between connecting segments and extension-conductors.

So neither of AMD's contentions regarding "respectively overlapped" is supported by the prosecution history. Nor does AMD's proposed construction capture the gist of its first contention, because it does not resolve what "respective" means. Under AMD's proposed language, if every connecting segment is overlapped with the same single extension-conductor segment, the claim language may well be satisfied. And as to AMD's second contention, there is no intrinsic evidence supporting a requirement that every structure that is arguably a connecting segment must overlap with an extension-conductor segment. Claims which use "comprising," such as claims 1 and 9 of the 582 patent, are open-ended and "do not exclude the presence in the accused apparatus or method

of factors in addition to those explicitly recited." *Vivid Techs., Inc. v. Am. Science & Engr., Inc.*, 200 F.3d 795, 811 (Fed. Cir. 1999). If at least two connecting segments (that otherwise satisfy the claim language) can be identified that overlap with the two extension-conductor segments, the claim language would seemingly be satisfied regardless if other connecting segments exist that do not overlap. So this aspect of AMD's construction cannot be correct.

By contrast, the construction Realtek articulated during the *Markman* hearing is consistent with the claim language and resolves the parties' dispute: "One or more of the connecting segments has to be overlapped with one of the extension-conductor segments, and . . . one or more [other] connecting segments, have to be overlapped with the other extension-conductor segment[]." Tr. at 73:1-5. Realtek's construction incorporates the plain and ordinary meaning of "respectively," and accounts for the various embodiments disclosed in the specification. *See* CIMB at 35-36. This construction is admittedly not what Realtek formally proposed (*see* JC at 3), but its formal proposal does not resolve the parties' dispute because it does not clarify the meaning of "respectively."

Accordingly, Realtek's informal proposal is accepted, and the term "plurality of connecting segments are respectively overlapped with the two extension-conductor segments in a vertical direction" means "at least a first connecting segment of the plurality of connecting segments overlaps one extension-conductor segment in a vertical direction, and at least a second connecting segment of the plurality of connecting segments overlaps the other extension-conductor segment in a vertical direction."

SO ORDERED.



Cameron Elliot
Administrative Law Judge