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Sherlekar et al.

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(54) **VARIOUS METHODS AND APPARATUSES TO ROUTE MULTIPLE POWER RAILS TO A CELL**

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(51) **Int. Cl.**
G06F 17/50 (2006.01)

(52) **U.S. Cl.** **716/12**; 716/13; 716/14; 716/15; 716/16

(58) **Field of Classification Search** 716/12–16
See application file for complete search history.

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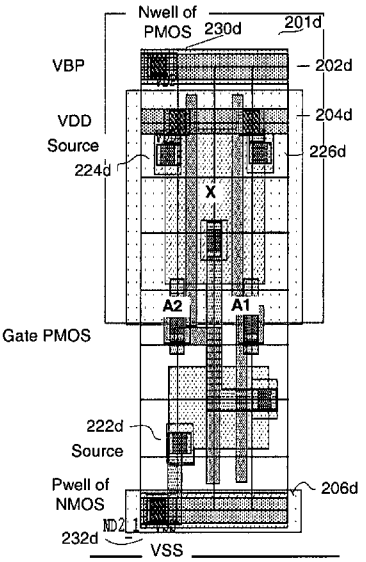
(57) **ABSTRACT**

Various methods and apparatuses are described in which an integrated circuit is organized into rows and columns of macro cells having a layout architecture that includes at least two metal layers and a plurality of traces carrying three or more different potentials of voltage routed by the metal layers. A first, a second, and a third adjacent metal layers extend across the integrated circuit. The first metal layer may be located between the second metal layer and the layer of the macro cells. The second metal layer may be located between the third metal layer and the first metal layer. The third metal layer may be orientated orthogonal to the second metal layer. The plurality of traces carry three or more different potentials of voltage and are routed in the metal layers. A first power trace supplies a VDD voltage potential. A second power trace supplies a VSS voltage potential. A third power trace supplies a third voltage potential. All three power supply traces connect to one or more transistors in a first macro cell.

21 Claims, 6 Drawing Sheets



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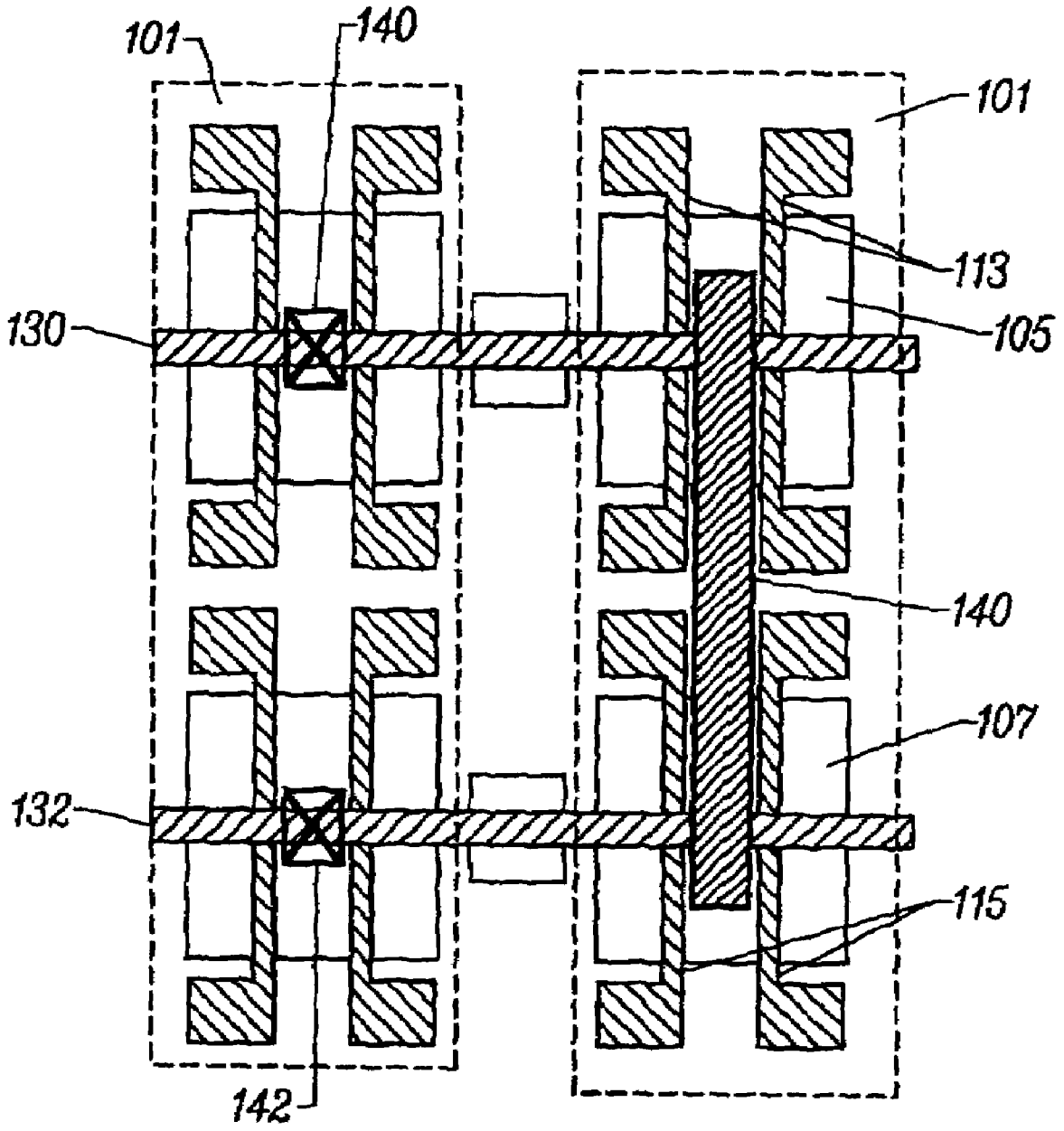
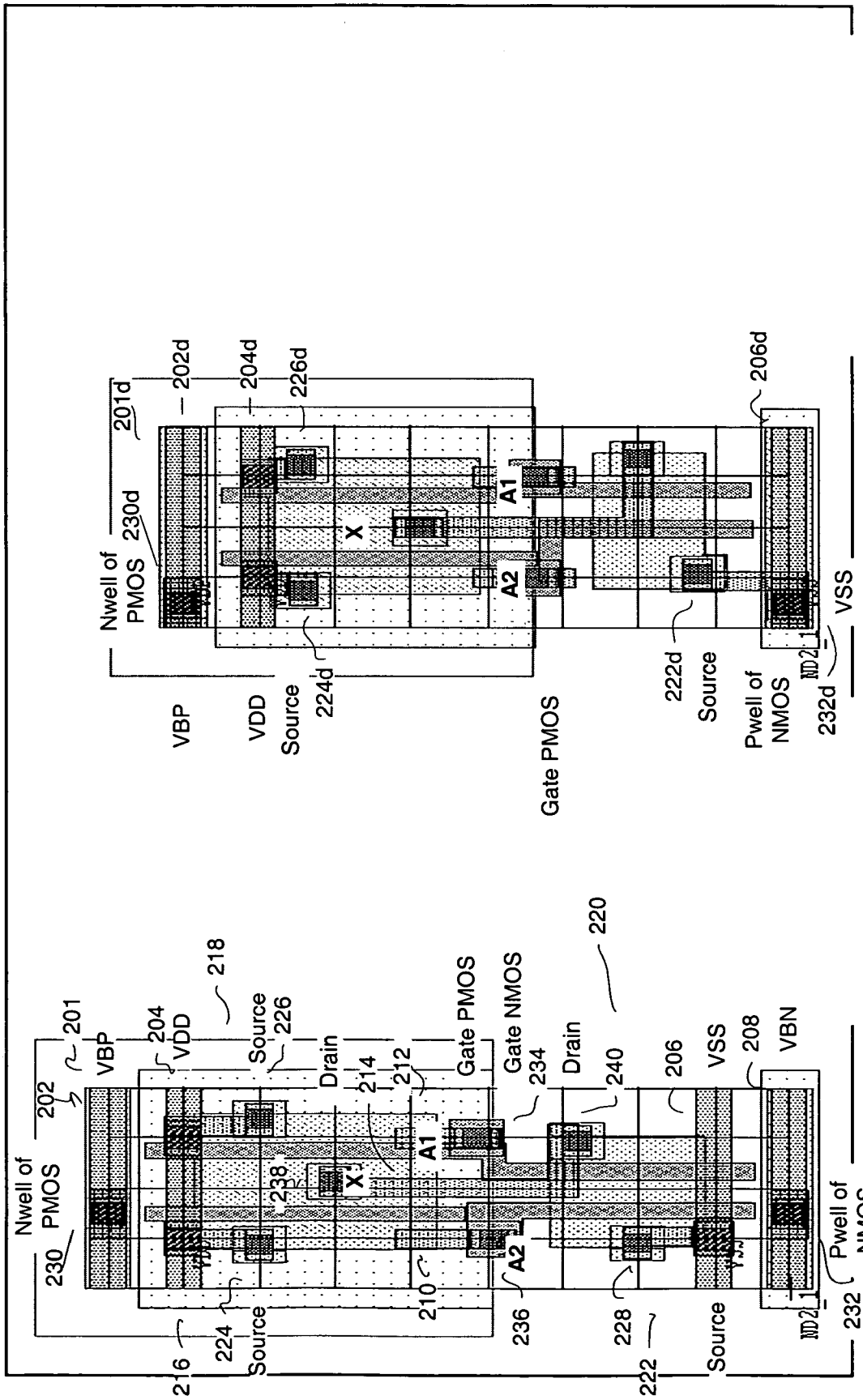


FIG. 1
(PRIOR ART)


Nwell of PMOS
230d
201d
202d
204d
226d
VBP
VDD
Source
224d
X
A1
A2
Gate PMOS
222d
Source
Pwell of NMOS
232d
206d
VSS
Figure 2D
Nwell of PMOS
230
201
202
VBP
204
VDD
218
Source
226
Drain
214
212
Gate PMOS
Gate NMOS
234
Drain
220
240
206
VSS
208
VBN
Pwell of NMOS
232
238
X
A1
A2
210
236
228
222
Source
224
Source
216
Figure 2A

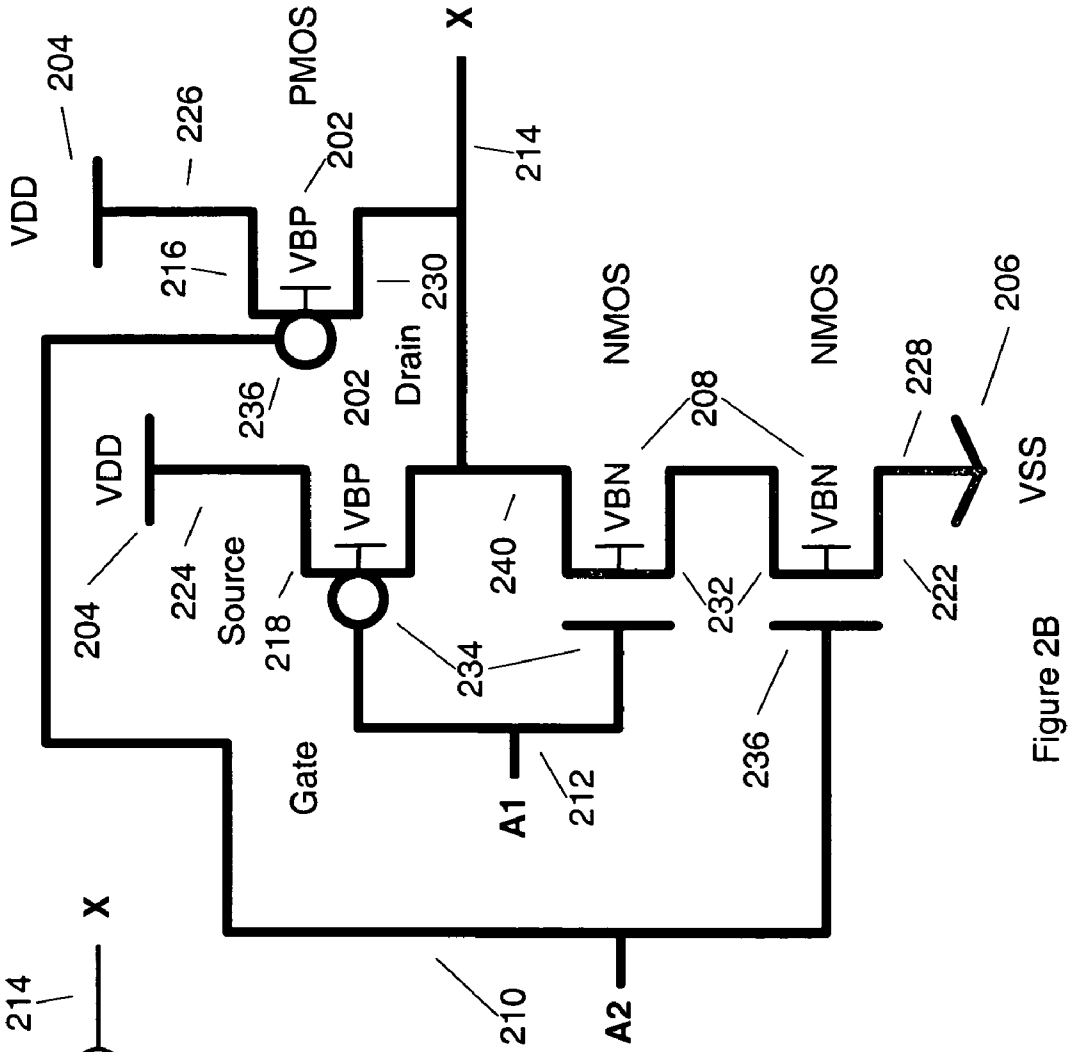
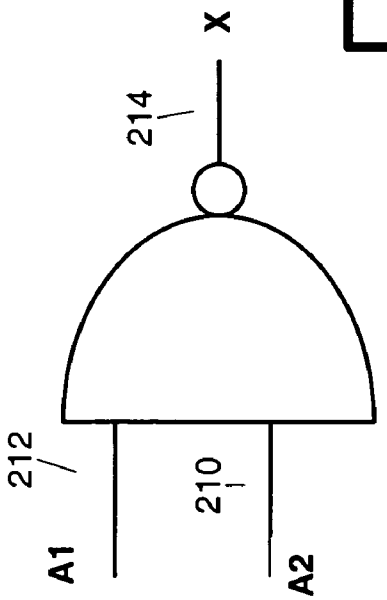


Figure 2B



NAND

Figure 2C

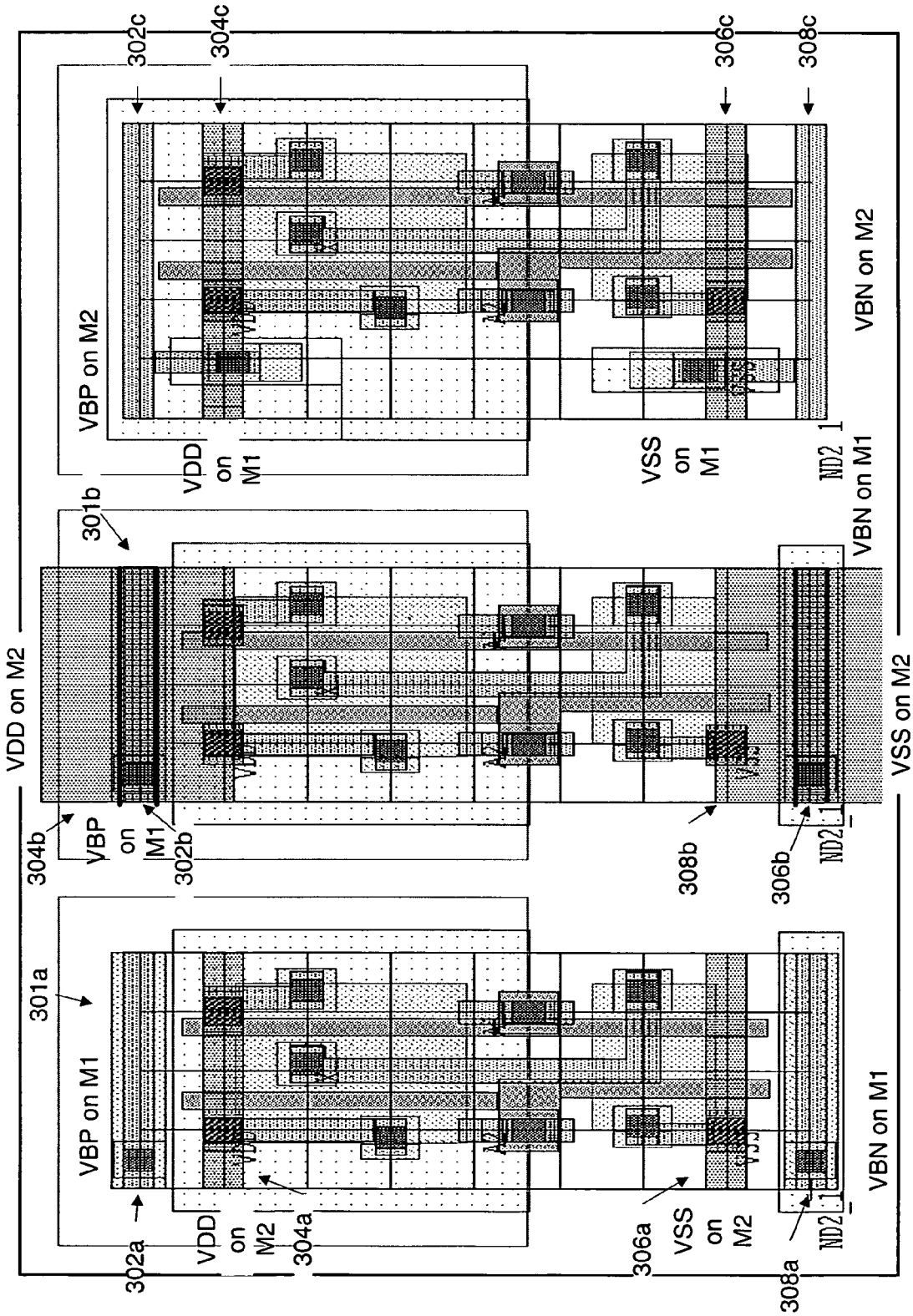


Figure 3A

Figure 3B

Figure 3C

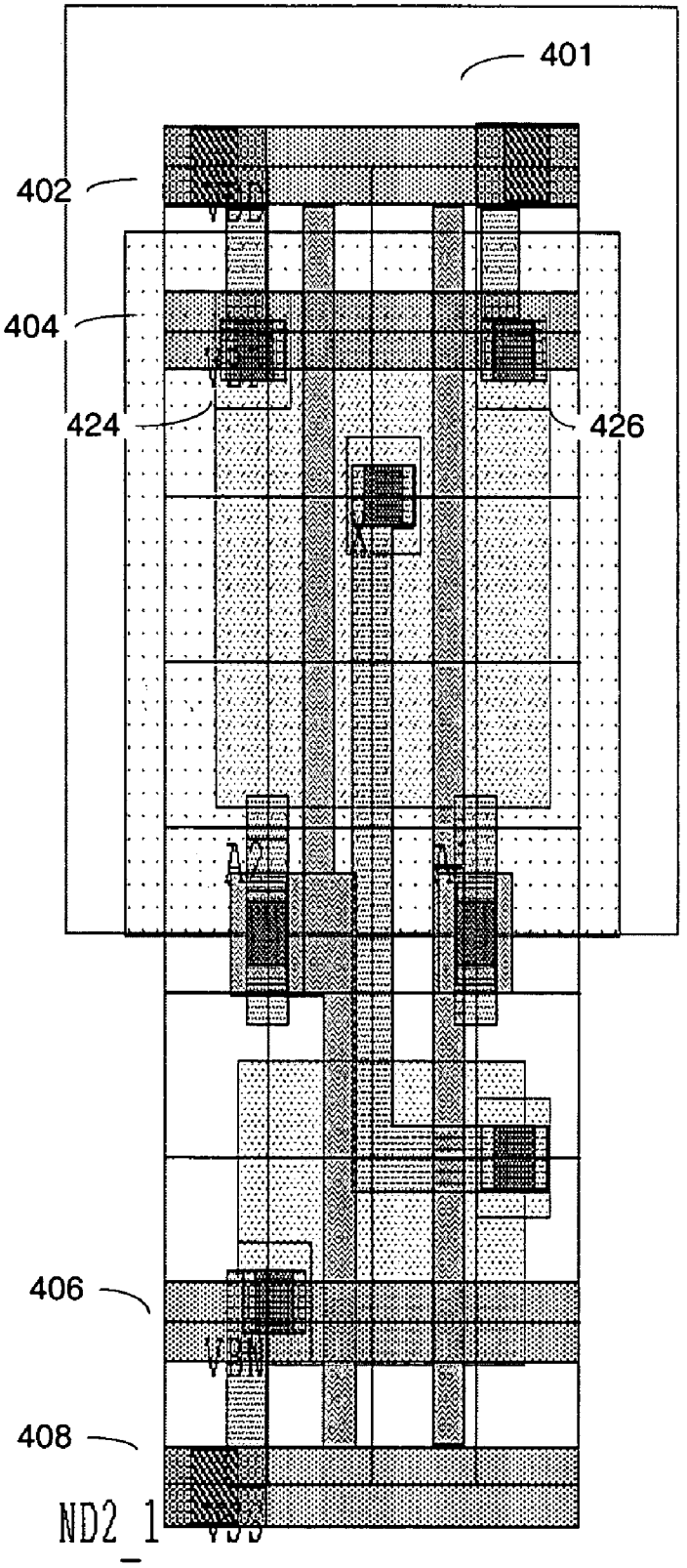


Figure 4

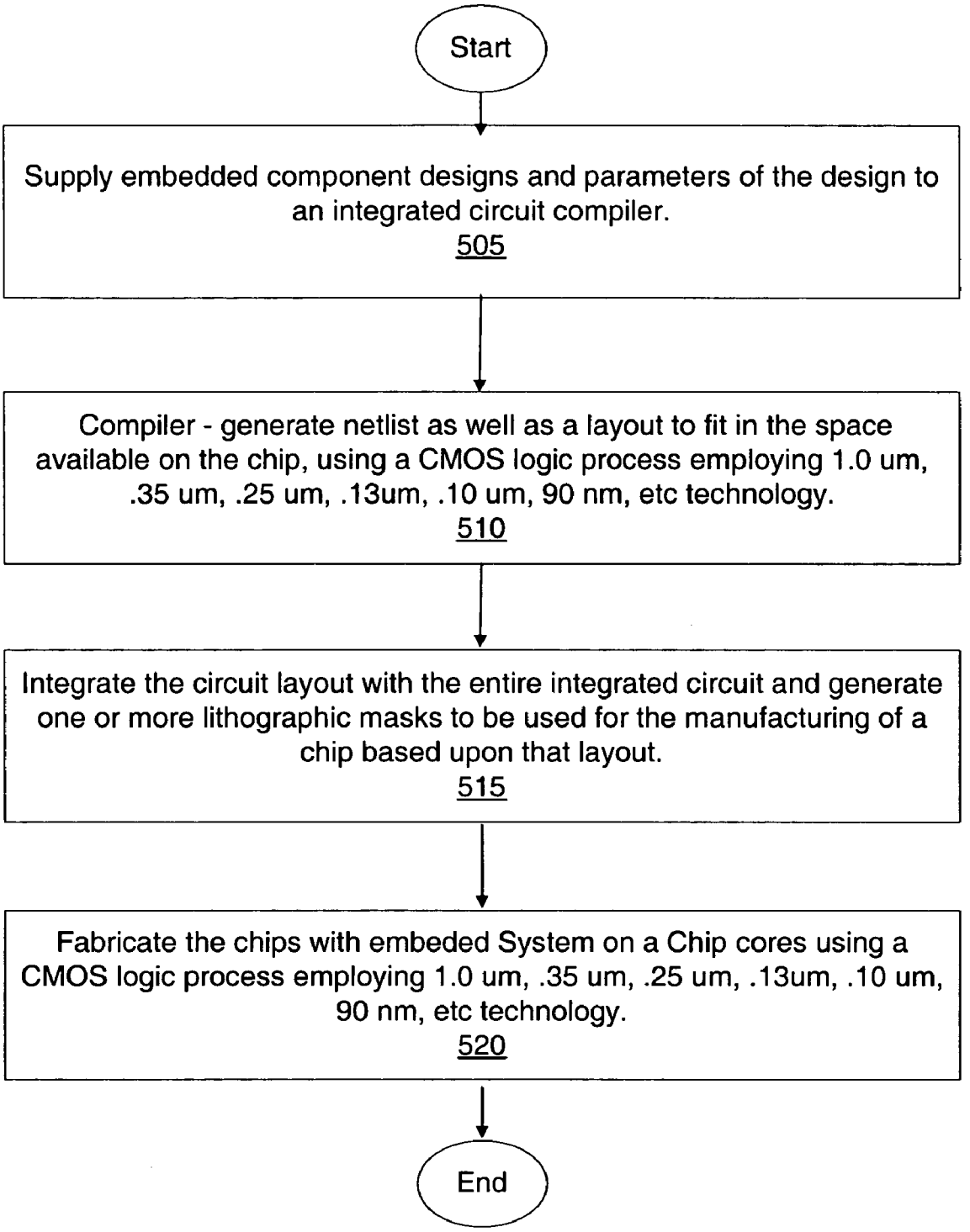

Start
Supply embedded component designs and parameters of the design to an integrated circuit compiler.
505
Compiler - generate netlist as well as a layout to fit in the space available on the chip, using a CMOS logic process employing 1.0 um, .35 um, .25 um, .13um, .10 um, 90 nm, etc technology.
510
Integrate the circuit layout with the entire integrated circuit and generate one or more lithographic masks to be used for the manufacturing of a chip based upon that layout.
515
Fabricate the chips with embeded System on a Chip cores using a CMOS logic process employing 1.0 um, .35 um, .25 um, .13um, .10 um, 90 nm, etc technology.
520
End

Figure 5

VARIOUS METHODS AND APPARATUSES TO ROUTE MULTIPLE POWER RAILS TO A CELL

RELATED APPLICATIONS

This application claims the benefit of and priority to provisional application No. 60/475,248 that was filed on Jun. 2, 2003 and is entitled, "LOW POWER MEMORY DESIGN."

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FIELD OF THE INVENTION

Embodiments of the invention generally relate to the field of routing connections in cell-based integrated circuits and gate array based integrated circuits. More particularly, an aspect of an embodiment of the invention relates to an improved power and signal routing architecture and technique to for high density and low power cell design.

BACKGROUND OF THE INVENTION

Gate array technology as well as cell-based or standard cell design, have been developed as a method of quickly designing integrated circuits.

Gate array technology is characterized by patterns of regularly placed transistors. The transistors are arranged in patterns known as basic cells. Basic cells are the smallest building block of the technology and are configured to facilitate creation of dense macro cells and efficient signal routing. Typically, the basic cells are placed on the integrated circuit in an array pattern with rows and columns. This array pattern is called a gate array.

Basic cells are combined into pre-designed circuit units known as "macro cells." Macro cells are commonly used elements such as NAND gates, NOR gates, and flip-flops. A designer, with a tool such as a compiler, selects desired elements from a library of macro cells and places them in a design. The macro cells may be interconnected in a variety of ways to perform desired functions. By being able to select macro cells from a library and place them into a design, a designer can quickly design complex functions without having to worry about the details of each individual transistor. Typically, a library of macro cells are designed from basic cells for a certain technology, and their design characteristics do not change from one design to the next.

In cell based or standard cell integrated circuits, the transistors used to construct macro cells are custom built for each macro cell, rather than from the underlying array of basic cells. However, all macro cells have the same height, and are arranged in rows similar to gate arrays.

Because a designer will use many macro cells in a particular design, it is important that the macro cells be designed as efficiently as possible. Otherwise, the inefficiencies will be multiplied, since they are replicated with every instance of the macro cell in the design.

As described above, the macro cells are made up of interconnected transistors that either belong to the underlying basic cells, or are custom crafted for the macro cell. Local interconnections are used to interconnect the transistors to form macro cells. Global interconnections are used to route signals from the input/output terminals of a macro cell to the input/output terminals of other macro cells. Clock signals, reset signals, power signals, and test signals are other examples of signals that may be routed by global interconnections. It is important that the macro cells be designed such that local and global interconnections can be made efficiently.

One concern of gate array and standard cell based designers is routing VDD and VSS (GROUND) power supply traces to the transistors of the basic cells efficiently. FIG. **1** shows a prior art design taught, for example, in U.S. Pat. Nos. 5,072,285, 4,682,201, 4,884,118, 4,783,692, and others, to route power supply traces to basic cells in a gate array.

FIG. **1** illustrates a block diagram portion of one row of a gate array design with two basic cells. Each basic cell **101** comprises a p-type diffusion region **105** and an n-type diffusion region **107**. Two gate regions **113** extend across p-type diffusion region **105** forming a pair of PMOS transistors and two gate regions **115** extend across n-type diffusion region **107**, forming a pair of NMOS transistors.

Several basic cells **101** are arranged in rows and columns on a substrate forming an array of basic cells **101**. Power supply trace **130** extends across rows of basic cells **101** in the metal one (M1) layer above p-type diffusion region **105**. Typically, power supply trace **130** is coupled to a VDD power supply source (not shown). Similarly, power supply trace **132** is formed on the M1 layer above n-type diffusion region **107**, and is typically coupled to a GROUND (VSS) power supply source (not shown). Power supply traces **130** and **132** extend across rows of the array.

Most commonly, power supply traces **130** and **132** are connected to diffusion region **105** and **107** at a common node between the two transistors by contacts **140** and **142**. An advantage of this layout is that a direct connection can be made between power supply traces **130** and **132** and diffusion regions **105** and **107**, without additional metal routing.

Traditionally, as shown in the basic cell illustrated in FIG. **1**, the M1 layer has been used to route power supply traces and other global interconnections in the direction parallel the rows (horizontal). Second layer metal (M2) has been used for global signal interconnections in the direction parallel the columns (vertical), and third layer metal (M3) for routing global signal interconnections in the direction parallel the rows (horizontal).

A disadvantage of this architectural layout is that power supply traces **130** and **132** are routed on the M1 layer. This restricts the number of local interconnections that can be made on the M1 layer, thus requiring an increased use of the M2 layer to cross over power supply traces **130** and **132**. For example, in FIG. **1**, local interconnection **140** is located on the M2 layer in order to cross over power supply traces **130** and **132**. Having local interconnections on the M2 layer causes significant blockage for M2 layer global routing, and hence lower gate density.

In CMOS cell based and gate-array integrated circuits, providing multiple supplies of different voltage potential may be needed for biasing the substrate and/or Nwell potential separately from the device source potential(s). Macro cells requiring different voltage supply potentials may be need to be intermingled, by routing on the first metal routing layer multiple supplies carrying distinctly different voltage potentials within each cell boundary. However, this

method consumes lots of area on a chip since 1) the power supply wiring, 2) the cell connection and 3) the signaling wiring all use the same routing layer. Further, the routing of the above three power supply lines entirely in the first metal layer causes cell wiring to be excluded from the regions of the cell where those power supply wiring are routed. The cell wiring is excluded from the regions of the cell regardless of whether or not that voltage supply wiring is used by the specific macro cell because the power traces on the M1 layer extend into the macro cell and occupy area that would have been available for cell and signaling routing.

SUMMARY OF THE INVENTION

Various methods and apparatuses are described in which an integrated circuit is organized in rows of macro cells having a layout architecture that includes at least two metal layers and a plurality of traces carrying three or more different potentials of voltage routed by the metal layers. A first, a second, and a third adjacent metal layers extend across the integrated circuit. The first metal layer may be located between the second metal layer and the layers of the transistors in the macro cells. The second metal layer may be located between the third metal layer and the first metal layer. The third metal layer may be orientated orthogonal to the second metal layer. The plurality of traces carry three or more different potentials of voltage and are routed in the metal layers. A first power trace supplies a VDD voltage potential. A second power trace supplies a VSS voltage potential. A third power trace supplies a third voltage potential. All three power supply traces connect to one or more transistors in a first macro cell.

BRIEF DESCRIPTION OF THE DRAWINGS

The drawings refer to embodiments of the invention in which:

FIG. **1** illustrates a block diagram portion of one row of a gate array design with two basic cells;

FIG. **2***a* illustrates an embodiment of a macro cell implementing a 2 input NAND function connecting to four power supply traces;

FIG. **2***b* illustrates an example schematic diagram of an embodiment of the transistors in the macro cell illustrated in FIG. **2***a*.

FIG. **2***c* illustrates a logic symbol corresponding to the macro cell illustrated in FIG. **2***a;*

FIG. **2***d* illustrates an embodiment of a macro cell implementing a 2 input NAND function and consisting of three power traces, each carrying a different potential of voltage to transistors in the integrated circuit;

FIGS. **3***a*–**3***c* and FIG. **4** illustrate other embodiments of power traces having different widths and routed on multiple metal layers to transistors in a 2-input NAND cell of an integrated circuit; and

FIG. **5** illustrates an example process of generating an integrated circuit with multiple power traces routed to one or more of the basic cells in a cell-based integrated circuit from designs of components with an embodiment of a compiler.

While the invention is subject to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and will herein be described in detail. The invention should be understood to not be limited to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention.

DETAILED DISCUSSION

In the following description, numerous specific details are set forth, such as examples of specific data signals, named components, connections, number of transistors, etc., in order to provide a thorough understanding of the present invention. It will be apparent, however, to one of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well known components or methods have not been described in detail but rather in a block diagram in order to avoid unnecessarily obscuring the present invention. Further specific numeric references such as first transistor, may be made. However, the specific numeric reference should not be interpreted as a literal sequential order but rather interpreted that the first transistor is different than a second transistor. An example 2 input NAND gate will be used as an example macro cell formed and connected with the various power and signaling traces. However, this is only for illustration purposes, as many other logic gates can be formed. The NAND illustrates how the power and signaling traces may be routed and connected to a macro cell. Thus, the specific details and implementations set forth are merely exemplary. The specific details and implementations may be varied from and still be contemplated to be within the spirit and scope of the present invention.

In general, various methods and apparatuses are described in which an integrated circuit is organized into rows of macro cells having a layout architecture that includes at least two metal layers and a plurality of traces carrying three or more different potentials of voltage routed by the metal layers. Three or more adjacent metal layers extend across the integrated circuit. The metal layers are stack on top of each other with insulating layers in between. The first metal layer may be located between the second metal layer and the layers of transistors in the macro cells. The second metal layer may be located between the third metal layer and the first metal layer. The third metal layer may be orientated orthogonal to the second metal layer.

The plurality of traces carry three or more different potentials of voltage and are routed in the metal layers. A first power trace supplies a VDD voltage potential. A second power trace supplies a VSS voltage potential. A third power trace supplies a third voltage potential. A fourth power trace supplies a fourth voltage potential and so on. All of the power supply traces may connect to one or more transistors in a particular macro cell.

The third voltage potential may, for example, 1) bias the well substrate of a transistor higher than the source voltage potential on that transistor to reduce power loss due to leakage, 2) enhance performance time of transistors in that macro cell, 3) provide a constant source of power to components in the macro cell when the primary source supplies, VDD/VSS, are turned off, 4) provide a switchable on/off source of power to components in the macro cell when the integrated circuit is in operation, 5) connect to some of the macro cells in a row of macro cells to allow adjacent macro cells to operate with different voltage potential requirements and different amounts of voltage supplies then a neighboring adjacent macro cell, or 6) provide other similar functions.

FIG. **2***a* illustrates a block diagram of an embodiment of transistors in a macro cell connecting to four power supply traces. The integrated circuit may organized in rows and columns of macro cells with multiple layers of metal such as a first, a second, a third, and a fourth metal layers residing above the macro cells. Each layer of metal is separated from the other by an insulating layer. The first metal layer M1 is

nearest the substrate, the second metal layer M2 is above the first metal layer, and the third metal layer M3 is above the second metal layer and is the farthest layer from the substrate. If desired, additional metal layers may also be used.

The second metal layer is above the first metal layer and has a plurality of conductive traces carrying power across the rows. The first metal layer has a plurality of conductive traces that may also carry power across the rows. In this example layout, the power traces **202**–**208** in the second metal layer M2 carry power across the rows of macro cells and the first metal layer is used for routing signaling and intraconnections **210**–**214** for transistors in the macro cells. The transistors may be, for example, n-type and p-type, Metal-Oxide-Semiconductor Field-Effect-Transistors.

FIG. **2***b* illustrates an example schematic diagram of an embodiment of the transistors in the macro cell illustrated in FIG. **2***a*. FIG. **2***c* illustrates a logic symbol corresponding to the macro cell illustrated in FIG. **2***a*.

Referring to FIGS. **2***a*–**2***c*, the macro cell may have a set of four transistors within the cell, two n-type NMOS transistors **220**, **222** and two p-type PMOS transistors **216**, **218**. A first power trace **204** in the second metal layer M2 may supply a VDD voltage potential via contacts to the source terminals **224**, **226** of the PMOS transistors. A second power trace **206** in the second metal layer M2 may supply a VSS voltage potential via contacts to a source terminal **228** of an NMOS transistor. A third power trace **202** in the second metal layer M2 may supply a third voltage potential, such as VBP, via contacts to a Nwell substrate **230** associated with the PMOS transistors to bias the wells of those transistors. The third voltage potential, VBP, of the third power trace **202** may bias the Nwell substrate **230** higher than the VDD voltage potential on the first power trace **204** to reduce power loss due to leakage. The third voltage potential, VBP, of the third power trace **202** may also bias the Nwell substrate **230** to slightly lower than the VDD voltage potential on the first power trace **204** to enhance the performance switching speed of these transistors.

Similarly, a fourth power trace **208** in the second metal layer M2 may supply a fourth voltage potential, such as VBN, via contacts to a Pwell substrate **232** associated with the NMOS transistors to bias the Pwells of those transistors. The fourth voltage potential, VBN, of the fourth power trace **208** may bias the Pwell substrate **232** lower than the VSS voltage potential on the second power trace **206** to reduce power loss due to leakage. The fourth voltage potential, VBN, of the fourth power trace **208** may also bias the Pwell substrate **232** to slightly higher than the VSS voltage potential on the second power trace to enhance the performance switching speed of these transistors.

Thus, the additional power supply traces, such as the third power trace **202** and the fourth power trace **208**, may route a voltage potential to bias the well substrate **230**, **232** of a transistor higher than a source voltage potential on that transistor to reduce power loss due to leakage or in another way alter the biasing of that transistor.

The routing technique allows easier signaling and intraconnection routing with all of the power traces routed in metal layers above the first metal layer. The first signal trace **212** on the first metal layer routed parallel to the columns of macro cells may carry a first input signal (A**1**) to the gate terminal **234** of one of the NMOS transistors as well as the gate terminal **234** of one of the PMOS transistors. The second signal trace **210** on the first metal layer routed parallel to the columns of macro cells may carry a second input signal (A**2**) to the gate terminal **236** of the second NMOS transistor as well as the gate terminal **236** of the second of the PMOS transistor. The third signal trace **214** on the first metal layer routed parallel to the columns of macro cells may connect to the drain terminals **238**, **240** of the PMOS and NMOS transistors. The third signal trace **214** on the first metal layer may carry the output signal (X) out of this configuration of transistors.

Note, the first macro cell **201** is shown only by way of example. The first macro cell **201** may be advantageously replaced with one or more different macro cells now known, or later developed. Also, although stacked via contacts couple power traces **202**–**208** with individual macro cells, other methods besides stacked via contacts may be used to make the connections.

The power traces **202**–**208** may be routed horizontal to the orientation of the macro cell **201** and with a specific relationship to the boundaries of that macro cell. The third power trace **202** carrying VBP may be routed over a first edge of a cell boundary of the first macro cell **201** to share the third power trace **202** with an adjacent cell. The second power trace **206** carrying VSS may be routed along an interior of the cell boundary. Likewise, the first power trace **202** carrying VDD may be routed along the interior of the cell boundary. The fourth power trace **208** carrying the VBN voltage potential may be routed at an opposite edge of the cell boundary. Therefore, the fourth power trace **208** may also be shared with another adjacent cell. Thus, the architectural layout of power trace lines at the edges of adjacent rows of macro cells shifted laterally with respect to each other allows sharing of power supply traces.

In this example, the power traces for the VBP/VBN voltage supplies are at the top/bottom edges of the logic cell. The power traces for VDD/VSS are routed over the logic cell. However, VDD/VSS may be routed on the edges and VBN/VBP may be routed on the interior of the macro cell. The routing of the power traces in relation to the cell boundary may be varied to maximize the density of macro cells in the integrated circuit.

The power traces **202**–**208** may be routed in metal layers that extend across the integrated circuit predominantly in a direction parallel i.e. horizontal to the rows of macro cells. The metal layers above the first metal layer M1, in this example solely M2, may route four or more different voltage supplies to the transistors in that macro cell. The parallel routing technique in combination with the varied edge and interior routing allows the power supply source connections to VDD/VSS to easily be completed with no additional cell area consumed by the supply wire for this connection.

FIG. **2***d* illustrates a block diagram of an embodiment of a plurality of three power traces, each carrying a different potential of voltage to transistors in a macro cell of an integrated circuit. Except as noted, the second macro cell is connected to the power traces in the metal layers similar to the first macro cell illustrated in FIG. **2***a*. The first power trace **204***d* supplies a VDD voltage potential via contacts to the source terminals of the PMOS transistors. The second power trace **206***d* supplies a VSS voltage potential via contacts to a source terminal **222***d* of an NMOS transistor. The second power trace **206***d* also supplies a VSS voltage potential via contacts to a Pwell substrate **232***d* associated with the NMOS transistor to bias the well of that transistor. The third power trace **202***d* in the second metal layer M2 may supply a third voltage potential, such as VBP, via contacts to a Nwell substrate **230***d* associated with the PMOS transistors to bias the wells of those transistors. Thus, the Pwell substrate **232***d* of the NMOS transistor will be the same voltage potential as the source terminal **222***d*. How-

ever, the Nwell substrate **230***d* of the PMOS transistors may be biased to a different voltage potential then the source terminals **224***d* and **226***d*.

The third power trace **202***d* being discretely separate from the primary power supply connections can provide for a wide variety of different functions. For example, the first power trace **204***d* may carry a VDD voltage potential that can be turned on and off when in operation to the second macro cell **201***d* while the third power trace **202***d* provides a constant supply of power to particular components within the macro cell during modes of operation such as a sleep mode. When VDD is turned off during a sleep mode, the second power trace can still provide a voltage potential to the well of the transistors to maintain a logic state stored by that macro cell. Also, the third power trace **202***d* can carry a voltage potential that can be continuously supplied in all operations to the second macro cell **201***d*. The third power trace **202***d* may provide a switchable on/off source of power to components in the macro cell when the integrated circuit is in operation. The different voltage potentials carried by the third power trace **202***d* can bias the transistors to enhance their performance or reduce leakage.

The routing of multiple voltage potentials and the capability to vary the power trace's specific relationship to the boundaries of macro cell in a row of macro cells allows macro cells having different voltage potential requirements and different amounts of voltage supplies to be located adjacent and intermingled with one another. Each macro cell connecting only to the power traces carries the voltage potentials needed for that macro cell.

The second macro cell **201***d* has a smaller height than the first macro cell **201**. Thus, the routing of three or more power traces across the integrated circuit allows the use of rows of macro cells with various heights. Note, the second macro cell **201***d* could easily have a smaller height than the first macro cell **201** but the same number of power rails, such as four, connected to the second macro cell **201***d*.

The first metal layer may be routed predominantly horizontal with respect to a row of macro cells, or predominantly vertical with respect to a row of macro cells, or have no predominant direction at all. The second metal layer routing the power rails may be predominantly horizontal with respect to a row of macro cells.

FIGS. **3***a*–**3***c* illustrate a block diagram of an embodiment of power traces having different widths and routed on multiple metal layers to transistors in a macro cell of an integrated circuit. FIGS. **3***a*–**3***c* illustrate three example options for routing source voltage supplies (VDD/VSS) and substrate/Nwell voltage supplies (VBN/VBP) using the Metal1 and Metal2 conductive layers. Referring to FIG. **3***a*, the first power trace **302***a* is routed on the first metal layer and supplies a VBP voltage potential to the third macro cell **301***a*. The second power trace **304***a* is routed on the second metal layer and supplies a VDD voltage potential to the third macro cell **301***a*. The third power trace **306***a* is also routed on the second metal layer and supplies a VSS voltage potential to the third macro cell **301***a*. The fourth power trace **308***a* is routed on the first metal layer and supplies a VBN voltage potential to the third macro cell **301***a*.

Referring to FIG. **3***b*, the routing connections are the same as described in FIG. **3***a*. However, the width of the second power trace **304***b* and third power trace **306***b* is much wider. The width of the second power trace **304***b* on the second metal layer extends over and past the first power trace **302***b* on the first metal layer. A macro cell adjacent to the third macro cell **301***b* may share the VDD potential on the wide second power trace **304***b* even though components on the interior portion of the third macro cell **301***b* are connecting to that power trace.

Referring to FIG. **3***c*, the routing connections are similar as described in FIG. **3***a*. However, the metal layer routings have been reversed. The first power trace **302***c* is routed on the second metal layer. The second power trace **304***c* is routed on the first metal layer. The third power trace **306***c* is routed on the first metal layer. Finally, the fourth power trace **308***c* is routed on the second metal layer. Note, any of these power traces may also be routed on the third metal layer or even higher.

Another advantage of forming power supply traces on both the first layer of metal and second layer of metal is that it frees up some of the first level of metal for routing of local interconnections as well as allows power supply traces carrying a different voltage potential to be routed on a different metal layer.

The power rails routed in the first metal layer may be routed predominantly horizontal with respect to the rows of macro cells. The power rails routed in the second metal layer may also be routed predominantly horizontal with respect to the rows of macro cells.

FIG. **4** illustrates a block diagram of an embodiment of routing the primary voltage supply traces at the edges of a cell boundary. Power supply traces **402**, **408** that carry VDD/VSS respectively are routed at the top/bottom of the macro cell **401** respectively. Power supply traces **404**, **406** that carry the Nwell and substrate voltage potential are routed over the interior of the macro cell **401**. This demonstrates the flexibility of the design as well as a feature that may not be achievable with conventional routing technology. In this configuration, using a conventional approach it might not be possible to route the source/drain connections to the VDD/VSS supply without breaking the VBN and VBP traces. The second power trace **402** is routed on, for example, a metal layer above the first metal layer and directly over the source terminals **424** **426** of the fourth macro cell **401**. Yet, the first power trace **402** is routed on, for example, the first metal layer and supplies a VDD voltage potential to the source terminals **424**, **426** without having to worry about routing around the second power trace **404***c* being directly over those components.

The routing technique of multiple power traces in multiple metal layers or even a single metal layer above the initial metal layer is also compatible with conventional NXT routing style cell libraries. The second conducting layer (typically M2) may be routed parallel to the cell rows. Further, each successive conductive layer above the second conductive layer is routed orthogonal to the conductive layer below that conductive layer.

Multiple voltage supplies can be provided on the second conducting layer alone, or in combination with the first conducting layer. One or more voltage supplies in addition to the primary supply, typically VDD/VSS (or Ground) for CMOS, are possible. The supply potentials routed on the second conducting layer or above can be easily accessed from the first conducting layer within the cell. Several supply architectures tuned to specific applications are possible.

Thus, the routing technique of multiple power traces in multiple metal layers or even a single metal layer above the initial metal layer provides improved flexibility for designing cell-based integrated circuits, such as standard cells and gate-arrays, that require multiple supplies of different voltage potential for cells in the same vicinity. Further, the routing technique eliminates any requirement that cells

requiring unique or multiple supplies at different voltage potential be grouped with like cells. The routing technique allows locally intermingled placement of cells that require common voltage supplies or non-common voltage supply potentials. The routing technique provides multiple supply connections of different voltage potential to be made available without a substantial increase in circuit area. The routing technique provides additional functionality without appreciably increasing area. The routing technique does not restrict the location of the interconnect(s) providing the substrate voltage potential or the location of the interconnect(s) providing the device source voltage potentials.

This routing technique provides an opportunity to reduce power consumption due to leakage or increase the performance of all or some portion of circuits in a design. The library/platform solution allows a chip designer the option of supplying separate N-well or substrate bias to the circuits on a chip without substantially effecting area.

FIG. **5** illustrates an example process of generating an integrated circuit with multiple power traces routed to one or more of the macro cells in a cell-based integrated circuit from designs of components with an embodiment of a compiler. The compiler may be used for making low power memory and logic platforms, high-density, high-speed and ultra-low-power logic standard cells, metal routing, as well as other applications.

In block **505**, the designs for each processor and memory component for the embedded circuit are supplied to the compiler, as well as other design parameters such as the number of columns and number of rows of the array, the available size on the chip, the number of metal layers, and other parameters. Thus, the designs for a low power memory design may be supplied to the compiler. A compiler may be a software program comprised of multiple algorithms and designs for the purpose of generating a circuit design and a layout in a space available on a target chip. The set of application-specific algorithms and interfaces of the compiler may be used by system IC integrators to rapidly create hundreds of silicon-proven System On a Chip cores. The compiler receives the component designs and utilizes those component designs in conjunction with circuit designs to optimize a circuit design and layout in the space available on a target chip.

In block **510**, the compiler generates a netlist and a layout targeted to fit in the space available on a target chip. The compiler stores the data representing the embedded circuit typically on a machine-readable medium. The compiler selects the component building blocks so that they are sized appropriately for the targeted fabrication technology. The compiler then provides the circuit layout to be used to generate one or more lithographic masks to be used in the fabrication of that embedded circuit such as a memory. The compiler also provides a netlist for verification of the embedded circuit.

In block **515**, the circuit layout generated is integrated with the rest of the layout for the chip and a machine generates the lithographic masks that contain the information necessary for the fabrication of a functional device. The machine generates one or more lithographic masks to be used to transfer that circuit design onto the chip.

In block **520**, a fabrication facility fabricates the chips with the embedded circuits using the lithographic masks generated from the compiler's circuit design and layout. Fabrication facilities may use a standard CMOS logic process having minimum line widths such as 1.0 um, 0.50 um, 0.35 um, 0.25 um, 0.18 um, 0.13 um, 0.10 um, 90 nm, or less, to fabricate the chips. The size of the CMOS logic process employed typically defines the smallest minimum lithographic dimension that can be fabricated on the chip using the lithographic masks, which in turn determines minimum component size. In an embodiment, light is transmitted through these lithographic masks onto the chip to transfer the circuit design and layout for the embedded circuit onto the chip itself. In an embodiment, the low power memory design compiler is designed for embedded applications in a standard CMOS logic process.

In block **525**, the chip may be programmed in the back end of the fabrication process using a layer physically higher than the diffusion layer. The compiler may generate instances that may be programmed by a ROM programming tool. The compiler uses routing and cell architecture that allows designers to create custom designs with just a few metal layers and via masks. The via layer and/or metal layer programmed cells may be completed in the back-end of the manufacturing process. If the programming of a ROM memory isn't made until later or a revision is needed, then the designer merely has to redesign the block, a few metal layers and via masks, thereby preserving all of the other masks.

In one embodiment, the software used to facilitate the compiler can be embodied onto a machine-readable medium. A machine-readable medium includes any mechanism that provides (e.g., stores and/or transmits) information in a form readable by a machine (e.g., a computer). For example, a machine-readable medium includes read only memory (ROM); random access memory (RAM); magnetic disk storage media; optical storage media; flash memory devices; DVD's, electrical, optical, acoustical or other form of propagated signals (e.g., carrier waves, infrared signals, digital signals, EPROMs, EEPROMs, FLASH, magnetic or optical cards, or any type of media suitable for storing electronic instructions. Slower mediums could be cached to a faster, more practical, medium.

In an embodiment, an example compiler may comprise the following. A graphic user interface, a common set of processing elements, and a library of files containing design elements such as circuits, control logic, and cell arrays that define the complier. In an embodiment, object code is compiled in a set of executable software programs.

In an embodiment, a designer chooses the specifics of a memory configuration to produce a set of files defining the requested memory instances. A memory instance may include front end views and back end files. The front end views support documentation, simulation, debugging, and testing. The back end files, such as a layout, physical LEF, etc are for layout and fabrication.

The complier outputs may include Behavioral Models and Test Benches (Verilog, VHDL), Timing Models (TLF, .Lib and STAMP), Test Models (MemBIST, FastScan), Structural Netlists (EDIF, Spice), Power Models (WattWatcher, ALF), Floorplanning and Place&Route Models, Physical LEF, FRAM, Layout (GDS), Datasheets (including power, timing, and area specifications), as well as other outputs. When programming occurs or if a revision is needed, the designer merely has to redesign the block, a few metal layers and via masks.

Some portions of the detailed descriptions above are presented in terms of algorithms and symbolic representations of operations on data bits within a computer memory. These algorithmic descriptions and representations are the means used by those skilled in the data processing arts to most effectively convey the substance of their work to others skilled in the art. An algorithm is here, and generally,

conceived to be a self-consistent sequence of steps leading to a desired result. The steps are those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers, or the like.

Although there may be some short departures from the direction of traces on each of the metal layers, the general trend is in the directions described. Departures from the general layout scheme as described may be made for solving ad hoc routing problems.

While some specific embodiments of the invention have been shown the invention is not to be limited to these embodiments. The invention is to be understood as not limited by the specific embodiments described herein, but only by scope of the appended claims.

We claim:

1. In an integrated circuit organized in rows of macro cells, a layout architecture, comprising:

first, second, and third adjacent metal layers extending across the integrated circuit, wherein the first metal layer is disposed between the second metal layer and a layer of transistors in the macro cells, and the second metal layer is disposed between the third metal layer and the first metal layer; and

a plurality of traces carrying three or more different potentials of voltage are routed in the metal layers parallel to the rows of macro cells, the plurality of traces comprising:

a first power trace to supply a VDD voltage potential,

a second power trace to supply a VSS voltage potential, and

a third power trace to supply a third voltage potential, wherein the first, second, and third power traces connect to one or more transistors in a first macro cell, and at least one of the first, second, and third power traces is shared between adjacent rows of macro cells.

2. The integrated circuit of claim **1**, wherein the third power trace to connect to a well substrate associated with the one or more transistors to bias the well of that transistor.

3. The integrated circuit of claim **2**, wherein the third voltage potential of the third power trace to bias the well substrate higher than the VDD voltage potential on the first power trace to reduce power loss due to leakage.

4. The integrated circuit of claim **2**, wherein the third voltage potential to bias the well substrate of a transistor higher than a source voltage potential on that transistor to reduce power loss due to leakage.

5. The integrated circuit of claim **1**,

wherein the first power trace is routed over a first edge of a cell boundary of the first macro cell to share the first power trace with an adjacent cell in an adjacent row of macro cells,

the second power trace routed is over an opposite edge of the cell boundary to share the second power trace with another adjacent cell in an opposite adjacent row of macro cells, and

the third power trace routed is along an interior of the cell boundary.

6. The integrated circuit of claim **1**, further comprising:

a fourth power trace routed predominantly in a direction parallel to the rows of macro cells.

7. The integrated circuit of claim **1**, wherein the first power trace is routed on the first metal layer that extends across the integrated circuit predominantly in a direction parallel to the rows of macro cells, and the second power trace is routed on the second metal layer that extends across the integrated circuit predominantly in a direction parallel to the rows of macro cells.

8. The integrated circuit of claim **1**, further comprising:

a second macro cell having different voltage potential requirements and different amounts of voltage supplies located adjacent to the first macro cell.

9. The apparatus of claim **1**, further comprising:

a switch connected to the third power trace to at least one of turn on or off a voltage potential carried by the third power trace the first macro cell.

10. The apparatus of claim **1**, further comprising:

a first transistor in the first macro cell where the second power trace connects to a well substrate associated with the first transistor.

11. The apparatus of claim **1**, further comprising:

a first transistor in the first macro cell where the first power trace connects to a well substrate associated with the first transistor.

12. The apparatus of claim **1**, wherein the second metal layer is routed horizontal with respect to a layout of the first macro cell.

13. A machine readable medium that stores data and instructions, which when executed by a machine, to cause the machine to generate a representation of the integrated circuit of claim **1**.

14. A machine readable medium that stores data representing an integrated circuit organized in rows and columns of macro cells, a layout architecture, comprising:

first, second, and third adjacent metal layers extending across the integrated circuit parallel to the rows of macro cells, wherein the first metal layer is disposed between the second metal layer and the macro cells, and the second metal layer is disposed between the third metal layer and the first metal layer;

a plurality of traces carrying three or more different potentials of voltage are routed in the metal layers parallel to the rows of macro cells, the plurality of traces comprising:

a first power trace to supply a VDD voltage potential,

a second power trace to supply a VSS voltage potential, and

a third power trace to supply a third voltage potential, wherein the first, second, and third power traces connect to one or more transistors in a first macro cell, and at least one of the first, second, and third power traces is shared between adjacent rows of macro cells.

15. The machine-readable medium of claim **14**, wherein the machine-readable medium comprises a memory compiler to provide a layout utilized to generate one or more lithographic masks used in the fabrication of the integrated circuit.

16. The machine-readable medium of claim **15**, wherein the third power trace to connect to a well substrate associated with the one or more transistors to bias the well of that transistor with respect to the VDD voltage potential to reduce power loss due to leakage.

17. The machine-readable medium of claim **15**, wherein the integrated circuit further comprises:

the first power trace routed over a first edge of a cell boundary of the first macro cell to share the first power trace with an adjacent cell of an adjacent row of macro cells,

the second power trace routed over an opposite edge of the cell boundary to share the second power trace with another adjacent cell of an opposite adjacent row of macro cells; and

the third power trace routed along an interior of the cell boundary.

18. The machine-readable medium of claim **15**, wherein the integrated circuit further comprises:

a fourth power trace routed predominantly in a direction parallel to the rows of macro cells.

19. The machine-readable medium of claim **15**, wherein the integrated circuit further comprises:

a second macro cell having different voltage potential requirements and different amounts of voltage supplies located adjacent to the first macro cell.

20. The machine-readable medium of claim **15**, wherein the third power trace to provide a constant source of power to components in the first macro cell when the VDD voltage potential is turned off during a mode of operation.

21. The machine-readable medium of claim **15**, wherein the third power trace is connected to a switch to provide a switchable on/off source of power to components in the first macro cell when the integrated circuit is in operation.

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