

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC.,	)	
Petitioner,	)	
	)	Case No.
v.	)	IPR2023-00929
REALTEK SEMICONDUCTOR	)	
	)	U.S. Patent No.
CORPORATION,	)	8,006,218
Patent Owner.	)	

DEPOSITION OF SHUKRI SOURI, PH.D.

May 7, 2024

10:01 a.m. Eastern Daylight Time

Reported by: Lori J. Goodin, RPR, CRR, RSA,
California CSR #13959

DIGITAL EVIDENCE GROUP
1730 M Street, NW, Suite 812
Washington, D.C. 20036
(202) 232-0646

1 REMOTE APPEARANCES:

2 FOR PETITIONER ADVANCED MICRO DEVICES INC.:

3 ARMOND WILSON LLP

BY: DOUGLAS R. WILSON, ESQUIRE

4 13785 Research Boulevard, Suite 125

Austin, Texas 78750

5 512-267-1663

doug.wilson@armondwilson.com

6 AND

7 ARMOND WILSON L.L.P.

8 BY: PATRICK MALONEY, ESQUIRE

4685 MacArthur Court, Suite 390

9 Newport Beach, California 92660

949-932-0778

10 patrick.maloney@armondwilson.com

11

12 FOR PATENT OWNER REALTEK SEMICONDUCTOR

13 CORPORATION AND THE WITNESS:

14 K & L GATES LLP

15 BY: ELIZABETH J. WEISKOPF, ESQUIRE

16 925 Fourth Avenue, Suite 2900

17 Seattle, Washington 98104

18 206-623-7580

19 elizabeth.weiskopf@klgates.com

20

21 Also Present:

22 Rachel Hsieh, Realtek in-house counsel

1 INDEX TO EXAMINATION

2 WITNESS: SHUKRI SOURì, PH.D.

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4 MR. WILSON 5

5

6 INDEX TO EXHIBITS

7 PREVIOUSLY MARKED EXHIBITS

8 PRIOR MARKED EXHIBITS FIRST REFERRAL

9 Exhibit 1001, U.S. Patent 8,006,218 32

10 Exhibit 1004, Jiang 138

11 Exhibit 1005, Li 140

12 Exhibit 1006, Chiu 75

13 Exhibit 1007, Jiang2 99

14 Exhibit 1012, Low Power Methodology
15 Manual 16

16 Exhibit 1013, Bertolet 171

17 Exhibit 1040, IEEE Dictionary 124

18 Exhibit 2002, Sourì Declaration 10

19

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21

22

1 TUESDAY, MAY 7, 2024, 10:01 a.m. EDT

2

3 PROCEEDINGS

4 THE VIDEOGRAPHER: We are now on the

5 record. My name is Henry Marte; I am a

6 videographer with Digital Evidence Group.

7 Today's date is May 7, 2024, and the time is

8 10:01 a.m.

9 This deposition its being held in

10 the matter of Advanced Micro Devices, Inc.

11 versus Realtek Semiconductor Corp.

12 The deponent today is Dr. Shukri

13 Sourì.

14 All parties to this deposition are

15 appearing remotely and have agreed to the

16 witness being sworn in remotely.

17 Counsel, please identify themselves

18 for the record. Afterwards, the court

19 reporter will administer the oath to the

20 witness.

21 MR. WILSON: Douglas Wilson for AMD.

22 MS. WEISKOPF: Elizabeth Weiskopf

1 for Realtek and the witness.

2 MR. WILSON: Also here is Patrick
3 Maloney from my firm, Armond Wilson LLP.

4 * * *

5 Whereupon,

6 SHUKRI SOURI, PH.D.,
7 a witness called for examination, having been
8 first duly sworn, was examined and testified as
9 follows:

10 * * *

11 EXAMINATION

12 BY MR. WILSON:

13 Q. Good morning, Dr. Sourì.

14 A. Good morning.

15 Q. Could you please state your full
16 name.

17 A. Yes, my name is Shukri Sourì.

18 Q. Okay. You understand that you are
19 testifying under oath today, correct?

20 A. I do.

21 Q. Okay. Is there anything as you sit
22 here this morning that would prevent you from

1 giving full, truthful, and accurate testimony?

2 A. No.

3 Q. Okay. If anything changes in that
4 regard, will you let me know?

5 A. Yes.

6 Q. Okay. You are physically located in
7 New York City, correct?

8 A. At this time, correct.

9 Q. Okay. And you are in a conference
10 room at K&L Gates, correct?

11 A. I am.

12 Q. Okay.

13 A. Yes.

14 Q. And Ms. Weiskopf is sitting next to
15 you. Correct?

16 A. That is correct.

17 Q. Okay. You understand that once your
18 deposition has begun, and until my questioning is
19 finished, including during breaks, you are not
20 permitted to discuss the substance of your
21 testimony with anyone, correct?

22 A. I do.

1 Q. Okay. What do you have available to
2 you as you are sitting there in the conference
3 room?

4 A. I have a printout of my declaration
5 in hard copy, unmarked, and I just have a laptop
6 where I am logged into the Box account for the
7 marked exhibits which is now empty at this time.

8 Q. Okay. So, you don't have any other
9 paper exhibits with you?

10 A. I do not.

11 Q. And you don't have any other
12 electronic communication capability with you,
13 phone or any chats or anything open on your
14 laptop there?

15 A. No chats that are open. I have my
16 mobile phone, but it is in silent mode and I have
17 no access to it at this time.

18 Q. Okay. All right. Okay. Would you
19 agree to let me know if anyone tries to contact
20 you to discuss your deposition during the course
21 of your deposition today?

22 A. Of course.

1 Q. Okay. So, if we propagate exhibits
2 to the Box account, you will be able to see them
3 and review them. Correct?

4 A. I -- hopefully. I will see the
5 exhibits, hopefully, once they are uploaded. I
6 will let you know if they are.

7 Q. Okay. And if anything stops working
8 for you, please speak up and let us know and we
9 will get it corrected as soon as possible.

10 A. I will. Thank you.

11 Q. Okay. And you have been deposed
12 before, correct?

13 A. I have, yes.

14 Q. About how many times?

15 A. In the last four years, I would say
16 on average maybe four times a year, in that
17 order.

18 Q. Okay. So, you understand how the
19 process works, understand the rules, and
20 understand how this question and answer session
21 is going to proceed.

22 Correct?

1 A. I do.

2 Q. All right. When I ask a question,
3 if you don't understand the question or the
4 question is ambiguous to you, would you please
5 ask for clarification?

6 A. I will.

7 Q. Okay. If you answer a question
8 without asking for clarification, I'm going to
9 assume that you understood it. Okay?

10 A. That is fair.

11 Q. Okay. Today we are talking about a
12 single IPR and that IPR is IPR 2023-00920.

13 Do you understand that?

14 A. That is my understanding.

15 Q. Okay. So, if I refer to the IPR,
16 you will understand that that is the IPR that I
17 am referring to?

18 A. Okay. I understand.

19 Q. Okay. You also understand that this
20 IPR involves U.S. Patent Number 8,006,218.
21 Correct?

22 A. I do.

1 Q. Okay. And so if I refer to that as
2 the '218 patent, you will know what I mean.
3 Correct?

4 A. Correct.

5 Q. Okay. Also at any time if you need
6 to take a break, as long as there is not a
7 question pending, we will take a break.

8 A. Sounds good. Thank you.

9 Q. Okay. So, you have in front of you
10 a physical copy of Exhibit 2002, which is your
11 declaration. Correct?

12 A. I do, correct.

13 MR. WILSON: Okay. And, Henry, if
14 we could, could we go ahead and push
15 Exhibit 2002 to the Box.

16 (Whereupon, previously marked
17 Exhibit 2002,
18 first referral.)

19 BY MR. WILSON:

20 Q. So, you should also have an
21 electronic copy there now to refer to.

22 Do you see it?

1 A. All right. I see it.

2 Q. Okay. If we could turn to the last
3 page of Exhibit 2002.

4 A. Just one second. I am waiting for
5 it to finish downloading. But yes, I am. I am
6 on the last page.

7 Q. And that is your signature?

8 A. That is right. It is, on Page 103.

9 Q. And it is dated March 1, 2024.
10 Correct?

11 A. That is correct.

12 Q. Did you review Exhibit 2002, your
13 declaration, prior to your deposition?

14 A. Prior to today, yes, I have.

15 Q. Yes. Okay. Did you find any
16 mistakes or errors that you believe need to be
17 corrected?

18 A. There are -- there may be some
19 typos. They don't immediately come to mind.
20 Nothing substantive. If anything comes up during
21 our discussion today, I will bring them to light.

22 Q. Okay. After reviewing your

1 declaration, Exhibit 2002, you are confident in
2 all of the opinions you expressed in your
3 declaration.

4 Correct?

5 A. I am, yes.

6 Q. Okay. Approximately how much time
7 did you spend preparing for your deposition?

8 A. I, I prepared -- how much time?
9 Several hours.

10 Q. Five hours, 10 hours, 20 hours?

11 A. Between 10 and 20.

12 Q. Okay. And did you meet with counsel
13 in preparing for your deposition?

14 A. I did.

15 Q. Who specifically?

16 A. With Ms. Weiskopf, here, next to me.

17 Q. Okay. Anyone else?

18 A. No.

19 Q. Okay. All right. Are you familiar
20 with the term "power domain"?

21 A. As used in the '218 patent, yes.

22 Q. Outside of that context, are you

1 familiar with the term "power domain"?

2 A. My opinions are based on my analysis
3 of the '218 patent, and that is what I am using
4 as a guide, as a person of ordinary skill would
5 understand that term.

6 Q. Okay. Had you -- before reading
7 the '218 patent, had you ever heard the term
8 "power domain"?

9 A. It can be used in -- depends on the
10 context, of course.

11 For the purposes of my declaration,
12 I am guided by the '218.

13 Q. Okay. You understand that power
14 domain is a claim term in the '218 patent.
15 Right?

16 A. I do.

17 Q. And you understand that claim terms,
18 generally, in patent law are given their
19 customary and ordinary meaning to a person of
20 ordinary skill in the art.

21 Correct?

22 A. I do. Guided by the specification

1 and claim construction.

2 Q. Okay. So, are you aware of a
3 customary and ordinary meaning of power domain,
4 outside the '218 patent?

5 A. Well, like I said, it depends on the
6 context.

7 Q. Okay. What, what context?

8 A. Is there a specific article or a
9 specific reference that you have in mind that you
10 would like to show me to see what the context is?

11 Q. Okay. So, without me showing you a
12 reference, you don't have any opinion on what the
13 customary and ordinary meaning of the term "power
14 domain" is in the semiconductor field.

15 Correct?

16 A. That is not what I said. I have a
17 whole section under -- in my declaration that is
18 related to claim construction discussing power
19 domain.

20 Q. Okay. In that section of your
21 declaration, do you offer an opinion on the plain
22 and ordinary meaning or ordinary and customary

1 meaning of power domain to a person of ordinary
2 skill in the art?

3 A. Let me go to that section.

4 So, this is starting Page 25 for
5 claim constructions under Subsection A, heading
6 Power Domain.

7 And in Paragraph 71, I say, "The
8 plain and ordinary meaning of power domain is a
9 portion of the integrated circuit that has a
10 different power requirement from the power
11 requirements of another portion of the integrated
12 circuit."

13 Q. Okay. And so in your opinion, that
14 is what a person of ordinary skill in the art
15 would understand the term "power domain" to mean
16 in the context of the '218 patent, correct?

17 A. That is correct.

18 Q. Okay.

19 A. And plain and ordinary meaning.

20 Q. Okay. All right.

21 MR. WILSON: So, let's take a look
22 at Exhibit 1012.

1 (Whereupon, previously marked
2 Exhibit 1012,
3 first referral.)

4 BY MR. WILSON:

5 Q. And just to refresh your memory,
6 1012 is the Low Power Methodology Manual.

7 And you have reviewed this.

8 Correct?

9 A. I have. Let me just take a look at
10 it. I'm going to download it.

11 Okay. I have it up.

12 Q. Okay. Turn to Page 40, PDF Page 40.

13 Do you see at the bottom of the page
14 where it says, "A power domain"?

15 A. I do.

16 Q. Okay. It says, "A power domain is a
17 logical entity and is a collection of design
18 elements that share a primary power supply."

19 Correct?

20 A. I see that is what it says.

21 Q. Okay. So, that is how the Low Power
22 Methodology Manual defines power domain.

1 Correct?

2 A. It introduces this as a definition
3 in this particular manual.

4 But, like I said, it depends on the
5 context.

6 Q. Okay. Do you agree with this
7 definition of power domain?

8 A. It is a way to describe what I said.
9 It is consistent with how I explain a plain and
10 ordinary meaning of power domain.

11 Q. Okay. So, you agree that the
12 definition of power domain in the Low Power
13 Methodology Manual, shown here, is an accurate
14 description of the plain and ordinary meaning of
15 power domain. Correct?

16 A. That is not what I said. I said it
17 is consistent.

18 The '218 is a little bit more
19 detailed in that it talks about multiple power
20 domains, a multi-voltage domain designs.

21 So, that is why, while the
22 definition that is introduced in the LPMM is

1 consistent with it, it is not necessarily serving
2 all of the purposes of the '218.

3 Q. Okay. Well, if we can move back up
4 the page and look at the top of the page, you
5 would agree that the Low Power Methodology Manual
6 here on the same page is describing a
7 multi-voltage design. Correct?

8 A. Where are you reading?

9 Q. I am looking at Figure 11-2 at the
10 top of the page.

11 A. All right. So, you are specifically
12 pointing to the -- which part of this, the VCPU
13 Power Down Domain?

14 Q. I am looking at the description
15 where it says, "Figure 11-2 ARM1176JZF-S
16 Multi-voltage, power gated design."

17 A. I see that. It also points to the
18 fact that this is a power gated design.

19 Q. Okay. So, but the Low Power
20 Methodology Manual is defining power domain in
21 the context of describing a multi-voltage,
22 multi-power domain design, correct?

1 A. Well, I disagree. It is also
2 describing it in the context of a power gated
3 design.

4 Q. Okay. When you say you disagree,
5 what specifically in my question did you disagree
6 with?

7 A. It was an incomplete description of
8 the context as provided by the LPMM.

9 Q. Okay. So, you would agree that,
10 that the LPMM is defining power domain in the
11 context of a multi-voltage power gated design.

12 You just also believe that it is
13 describing it in the context of what additional
14 aspect?

15 A. No. I -- that is not how I
16 understood your question.

17 Your original question was whether
18 the definition as provided by the LPMM was in the
19 context of a multi-voltage design.

20 I disagreed because that premise was
21 incomplete.

22 There were other contexts that is --

1 that are described by the LPMM, namely the power
2 gated design.

3 And so, I am just pointing to the
4 fact that the LPMM definition here is in the
5 context that extends beyond simply multi-voltage
6 designs.

7 Q. Okay. So, okay. Just so for
8 clarity.

9 You agree that LPMM is defining
10 power domain in the context of a multi-voltage,
11 multi-power domain, power gated design, correct?

12 A. Well, those are separate contexts.

13 Q. So, that is a yes, you agree?

14 A. Yes. There are a number of contexts
15 here that are provided in the LPMM that are not
16 relevant to the '218.

17 Q. Okay.

18 A. The '218, for example, doesn't say
19 anything about power gated designs.

20 Q. Okay. So, we can push Exhibit 1012
21 aside for a moment.

22 Is it possible for an integrated

1 circuit to have multiple power domains?

2 A. Is it possible based on the '218?

3 Yes. That is what the '218 is about, in part.

4 Q. Okay. But -- yeah, in fact, we just

5 saw an example of that in the Low Power

6 Methodology Manual, correct?

7 A. Not necessarily, no. Because the

8 Low Power Methodology Manual also has other

9 contexts, as I read, namely power gated designs,

10 which are not relevant to the '218.

11 Q. Okay. But it did describe an

12 integrated circuit with multiple power domains.

13 Correct?

14 A. In part, yes.

15 Q. Okay. Now, a person of ordinary

16 skill in the art would understand that in certain

17 contexts, having multiple power domains could be

18 beneficial, correct?

19 A. It depends, it depends on the

20 context.

21 Q. Right. And in certain contexts, it

22 can be beneficial. Correct?

1 A. Yeah. It depends on the
2 application. It depends on the requirements.
3 Sure. It can be beneficial.

4 Not always, though. There are times
5 when you may not want it. May not need it. So,
6 it really depends.

7 Q. Okay.

8 A. And if I could elaborate on that a
9 little bit.

10 What I mean by that is if you start
11 introducing multiple voltage designs fed or
12 provided into the chip, then you are talking
13 about increasing the level of complexity. And
14 that is why I said it depends.

15 Complexity of everything, complexity
16 of placement, complexity of interconnect
17 placement, routing.

18 So, it depends on the final goal
19 that the design is after.

20 Q. Okay. And a person of ordinary
21 skill in the art, before November 2007, would
22 have been aware of the benefits and the

1 detriments of multiple power domain designs.

2 Correct?

3 A. I would say a person of ordinary
4 skill would have known that there are issues.
5 And to decide whether or not to pursue a
6 multi-voltage design, you have to do the analysis
7 to see if you get the benefits you are looking
8 for.

9 Q. Is it possible for an integrated
10 circuit with one supply voltage, a single supply
11 voltage, to have multiple power domains?

12 A. What do you mean by a single supply
13 voltage?

14 Q. One voltage level. Let's say a
15 supply voltage is 2 volts, 2.0 volts.

16 Is it possible for a integrated
17 circuit with a single supply voltage
18 of 2.0 volts, to have multiple power domains?

19 A. So, if you've got a chip that you
20 are supplying power to, from a power supply, a
21 single power supply, at that one voltage from --

22 What matters is the single power

1 supply.

2 I would say that I, unless -- I mean
3 I would have to see it, but I don't see how you
4 would get multi -- multiple power domains from
5 that.

6 It would depend on the context, but
7 from a single power supply, I doubt it.

8 Q. Okay. So, in your opinion, in order
9 to have multiple power domains in an integrated
10 circuit, you need multiple power supplies,
11 correct?

12 A. It would be an example.

13 When I see multiple power supplies,
14 then that tells me that we are looking at a chip
15 that most likely has multiple power domains.

16 I'm not saying that that is the only
17 way that it can be done. But it certainly would
18 be a way that I would expect, therefore, results
19 in multiple power domains.

20 Q. Okay. So, when you say you are not
21 saying it is the only way, could you give me an
22 example of another way to have multiple power

1 domains in an integrated circuit without having
2 multiple power supplies?

3 A. Have I thought of a different way?
4 Well, you, I haven't thought of every possible
5 way it can be done.

6 But, you know, there can be, you
7 know, different ways of it generating power
8 internally, for example, to a chip.

9 I mean there can be different ways.

10 But if I see different external
11 power supplies, then chances are we are looking
12 at multiple power domains.

13 Q. Okay. So, as you sit here today you
14 can't give me an example of an integrated circuit
15 that has multiple power domains and does not have
16 multiple power supplies, correct?

17 A. Well, no. I just gave you an
18 example of internally generated power as an
19 example.

20 Q. Okay. But isn't that a separate
21 power supply?

22 A. Well, again, it goes back to my

1 question what you meant by power supply.

2 Are we talking about an external
3 power supply, possible internal power supplies?
4 It depends.

5 But if you are saying that they are
6 different power supplies, then yeah, they can be
7 considered different power supplies. It depends
8 on the context.

9 Q. Okay. So, let's -- when we are
10 talking about power supplies, we are talking
11 about voltage supplies to the actual operating
12 circuitry of the chip.

13 So, if they are different supplies
14 to the operating circuitry of the chip, then
15 those are different power supplies. Right? Does
16 that make sense?

17 A. No. I don't quite understand the
18 question, no.

19 Q. Okay. So, all I'm trying to do is
20 establish a baseline so we are both on the same
21 page as far as the questions that I'm asking.

22 So, if I take a 2 voltage supply

1 and, let's say, I drop it down to 1 volt, within
2 the chip for different portions of the chip, then
3 I understand that to mean there are two different
4 power supplies now, right?

5 I have created a second power
6 supply, although I used the first power supply to
7 do it.

8 Does that make sense?

9 A. No.

10 Q. I'm asking you to assume that as a
11 premise.

12 A. Okay, so, I would, so, to -- so, I
13 would disagree with that.

14 I don't think that is how a person
15 of ordinary skill would understand it.

16 When we are talking about multiple
17 voltage domains in the context of multiple power
18 supplies, I'm really looking at the layout and
19 the routing on a chip to see how power is brought
20 into the chip.

21 And I'm looking, for example, at the
22 I/O pads and look at the power pads.

1 The way that these pads are named --
2 they could have different names -- the
3 nomenclature would tell me the design of the chip
4 or inform me about the design of the chip.

5 So, I would expect to see, for
6 example, you know, if it is multi-power,
7 multi-voltage, I would expect to see a VDD1, for
8 instance, and a VDD2.

9 Some distinction between the
10 different power pads.

11 Q. Okay. Well, let's, let's -- all
12 right. Let's frame it that way then.

13 If there is a single VDD coming into
14 the chip and distributed to the active circuitry
15 in the chip, you can't think of an example where
16 that chip can have multiple power domains,
17 correct?

18 A. That would not be -- in the context
19 of the '218, that is not how a person of ordinary
20 skill would understand it.

21 Q. When you say that is not how a
22 person of ordinary skill would understand, what

1 do you mean?

2 Like, you disagree with my question?

3 Or you agree with it --

4 A. I disagree with the premise of your
5 question, because we are looking at a single
6 power coming into the chip.

7 And that single power is being used
8 to supply power to the single power domain within
9 that chip, in that case.

10 Q. So, how do you define, then, a
11 single power coming into the chip?

12 Is that one VDD? Can it be a VDD1
13 and a VDD2?

14 What, how do you define it?

15 A. Well, I mean, like I said, if you
16 are talking about a chip that has a single
17 voltage coming in from a power supply, I would
18 expect to find, you know, a VDD, for instance.
19 That would be a single voltage, a single power
20 coming in from a single power supply.

21 And in that case, if that is all
22 we've got in terms of power coming into the chip,

1 then I expect to find a single power domain in
2 that chip.

3 And again that is not in the context
4 of the '218, because the '218 is expecting
5 multiple powers coming into the chip.

6 Q. Okay. So, so, your understanding is
7 that if the there is a single power supply coming
8 into the chip, then that chip is going to have a
9 single power domain, correct?

10 A. That is my expectation, yes.

11 Q. Okay. So, when you look at the '218
12 patent claims, which recite first and second
13 power domains, your understanding is that the
14 only way that is going to happen is if you have
15 at least two power supplies coming into the chip.
16 Correct?

17 A. As an example. Like I said, I
18 provided other examples, for instance, power that
19 is internally generated by the chip,
20 independently of the supply coming in from
21 outside of the chip.

22 There can be other ways to do it.

1 But, certainly if I find a chip that has two
2 separate power supplies coming into the chip,
3 regardless of the level of voltage of those two
4 power supplies -- what I mean by that is they
5 could be of the same nominal voltage value, for
6 instance, but they are separate power supplies.

7 And of course applying the rest of
8 the requirements of the claim language, which
9 requires separate power delivery networks from
10 the global power mesh, through the partial local
11 power meshes, to the respective power domains.

12 That is how I would perform my
13 analysis to identify a power domain.

14 Q. Okay. So, so, when you look at
15 the '218 patent claims which require first and
16 second power domains, you would understand that
17 there needs to be multiple power supplies, either
18 coming in externally to the chip or generated
19 internally within the chip. Correct?

20 A. I would expect that to be the case.

21 Q. Okay. All right. Let's take a
22 look.

1 MR. WILSON: So, Henry, let's go
2 ahead and pop up Exhibit 1001, the '218
3 patent. And let's look at Figure 5.

4 (Whereupon, previously marked
5 Exhibit 1001,
6 first referral.)

7 BY MR. WILSON:

8 Q. Now, Dr. Sourì, you have --

9 A. Okay, just one second. I haven't, I
10 don't -- so, I have the two PDFs, Exhibit 1012
11 and then 2002.

12 But then there is a folder called
13 Documents. I don't see the patent.

14 Q. Okay. Give it a second. You may
15 have to refresh it for it to show up.

16 THE VIDEOGRAPHER: Yes, just refresh
17 and see if it is up.

18 THE WITNESS: Got it. Okay. Now I
19 have it.

20 BY MR. WILSON:

21 Q. Okay.

22 A. Actually just give me a sec. Let me

1 download it.

2 Q. Sure.

3 A. Okay, I've got it.

4 Q. Okay. Now, can you turn to
5 Figure 5?

6 A. Yes, I am there.

7 Q. Okay. You are familiar with
8 the '218 patent, right? You have reviewed it?

9 A. I am, yes.

10 Q. Okay. And Figure 5 shows a power
11 routing structure. Correct?

12 A. Let me see. Figure 5 is described
13 as, "a schematic diagram illustrating the
14 relative portions of the local power mesh in
15 Figure 3 and the global power mesh in Figure 4."

16 That is what Figure 5 is described
17 as, in part.

18 And, it goes on to provide more
19 detailed description starting in Column 4.

20 Q. Okay. The, in Figure 5 the grid,
21 labeled 400 on the top right, is a global power
22 mesh, correct?

1 A. In Column 4, it describes global
2 power mesh 400, that is correct.

3 Q. Okay. And global power mesh 400 is
4 on metal layers 8 and 7, correct?

5 A. So, it goes on to say in Column 5,
6 Lines 2 through 4, "Global power mesh 400 can be
7 implemented on the corresponding metal layer M7
8 to M8."

9 So, it is giving that as an example.

10 Q. Okay. And in Figure 5, each of the
11 lines or bars in the mesh in the global power
12 mesh 400 is a power or ground wire. Correct?

13 A. Each of -- so, when you say each of
14 the -- the rectangles, right? You are talking
15 about the geometric rectangles shown in 400, in
16 Figure 5, each one of those is a single wire.

17 Q. Yes.

18 A. And what it is depends of course on
19 how it is assigned and -- during the design.

20 Q. Okay. To the left of the global
21 mesh in Figure 5, there are two rectangles
22 labeled M7 and M8. Correct?

1 A. Yes. Are you referring to what look
2 like layers, M7 and M8?

3 Q. Yes.

4 A. Okay.

5 Q. Okay. M8 represents metal layer 8.
6 Correct?

7 A. Yes, corresponds to metal layer M8.

8 Q. Okay. And M7 is metal layer M7,
9 correct?

10 A. That's correct. It describes -- in
11 Column 5, it talks about corresponding metal
12 layers M7 and M8.

13 Q. Okay. And below those we have shown
14 in Figure 5 metal layers M5 and M6, correct?

15 A. At the bottom of Column 4, it
16 explains that among the layers, M5 to M8, it says
17 the local power mesh 300 can be implemented on
18 the lower -- can be implemented on the lower
19 metal layers, M5 to M6.

20 Q. Okay. So, now, Figure 5 shows the
21 relative height of metal layers M5 through M8.
22 Correct?

1 A. What do you mean by relative height?

2 Q. I mean M6 is above M5, and M7 is
3 above M6 and M8 is above M7. Correct?

4 A. Yes. And the way that it is
5 explained, for example, in the specification, it
6 says that -- above -- that M5 and M6 are lower
7 metal layers compared to M7 and M8.

8 Q. Okay. So, looking back at the
9 global mesh 400, in the top right in Figure 5.

10 And just like we have shown here on
11 the screen here, I am looking at this Figure M,
12 which is effectively landscape orientation,
13 whereas in Figure 5 the label is horizontal.

14 A. Okay.

15 Q. Does that make sense?

16 A. Yes.

17 Q. Okay. So, in that orientation, the
18 vertical wires in mesh 400 are on metal layer M8,
19 correct?

20 MS. WEISKOPF: Object to form. This
21 is outside the scope.

22 THE WITNESS: One second. If you

1 are referring to -- again, the specification
2 provides examples on Column 5, Line 5
3 through 7.

4 It says, "The horizontal power
5 supply wire is placed on the metal layer M7
6 and the vertical power supply wire is placed
7 on the metal layer M8."

8 But again, that is just an example.
9 It is an embodiment, not a requirement.

10 BY MR. WILSON:

11 Q. Okay. But that is what is shown in
12 Figure 5 as well, correct?

13 A. Figure 5, going to the bottom of
14 Column 4, says, "The horizontal power supply wire
15 is placed on the metal layer M5 and the vertical
16 power supply wire is placed on the metal layer
17 M6."

18 And again these are provided as
19 examples.

20 Q. Okay. And what you just referred to
21 is talking about the local mesh. Correct?

22 MS. WEISKOPF: Object to form.

1 THE WITNESS: The -- you are
2 referring to the local power mesh 300. That
3 is how it is referred to in the, in the
4 specification in the bottom of Column 4.

5 BY MR. WILSON:

6 Q. Okay.

7 A. You called it local mesh. It is a
8 local power mesh 300.

9 Q. Okay. Fair enough.

10 Earlier you referred to a passage in
11 the '218 patent describing the horizontal and
12 vertical wires being on metal layers M7 and M8,
13 respectively.

14 Do you recall that?

15 A. I do. Yes.

16 Q. Okay. And that is what is shown in
17 Figure 5. Correct?

18 A. As an example. Well, it -- not
19 necessarily. It is just giving this as an
20 example.

21 Q. Right. But that is the example that
22 is shown in Figure 5. Correct?

1 MS. WEISKOPF: Object to form.

2 THE WITNESS: Well, it really
3 depends on the orientation of the figure. I
4 mean you chose to put it in landscape. The
5 patent isn't showing it in landscape.

6 It is not really that important one
7 way or another.

8 Because, they are just embodiments,
9 different examples.

10 BY MR. WILSON:

11 Q. Okay. Now, Figure 5 does not show
12 anything connecting the wires on metal 7 to
13 metal 6, or metal 6 to metal 5. Correct?

14 A. I am sorry. I am not quite sure I
15 understand the question.

16 Q. So, Figure 5 does not show anything
17 connecting the wires on one metal layer to the
18 wires on a different metal layer. Correct?

19 A. When you say showing, are you asking
20 me if there is something that is annotated in the
21 figure, or based on how a person of ordinary
22 skill would understand it?

1 Q. I'm asking if there is anything
2 shown in the figure, annotated in the figure,
3 described in the figure or, or expressly depicted
4 in the figure that connects one metal layer to
5 another?

6 A. Well, I mean the figure gives us
7 some examples, right, guided by the
8 specification.

9 For example, the lower right portion
10 of Figure 5, as seen in landscape, as you show it
11 here, identifies, for example, the locations of
12 the power domains that suggests or is disclosed
13 as locations where connections can be made to
14 provide power to the respective power domains.

15 So, a person of ordinary skill would
16 understand that using this kind of mapping
17 layout, it would give guidance as to where
18 connections can be made.

19 Q. Okay. But it doesn't show the
20 connections, correct?

21 A. If you are asking does it explicitly
22 show those connections, it doesn't explicitly

1 show them in this figure.

2 But again, there is enough
3 description in the specification to guide and
4 explain to a person of ordinary skill how that
5 kind of connections or set of connections are
6 made.

7 Q. Okay. A person of ordinary skill in
8 the art would understand that there have to be
9 connections between M8 and M7, and M7 and lower
10 layers like M5 and M6, to route power and ground
11 in this design. Correct?

12 A. Not necessarily. I mean, it really
13 does depend on the architecture. A person of
14 ordinary skill would also understand that it is
15 possible to connect from the global power mesh
16 directly down to the substrate of the silicon.

17 So, it really depends on the
18 context.

19 Q. Okay. In this design, you have a
20 global power mesh that sits above the local power
21 mesh. Correct?

22 A. Well, when you say above, it is just

1 a hierarchal. So, the placement is such that it
2 is hierarchal, correct.

3 Q. But --

4 A. But, it doesn't -- but, it is not
5 telling me that there has to be connectivity
6 through M6 or an M5 from M8 and M7.

7 It really just -- these are
8 depictions that provide a general understanding.
9 But, of course, the design dictates where and how
10 those connections are made.

11 Q. Okay.

12 A. For example, in Claim 19, there is
13 no requirement that there is any connection
14 through to the local power mesh.

15 Q. Okay. So, to get power from either
16 the global power mesh or the local power mesh in
17 Figure 5 down to the power domain, there has to
18 be a vertical drop, such as a via, correct?

19 A. Vias would be a common way of
20 providing power from the global power mesh or
21 from the local power mesh. They are good
22 examples of how to do that.

1 Your question is that, does there
2 necessarily have to be a vertical connection? I
3 mean, I don't think it is necessary. It is
4 certainly a way that is contemplated in the '218,
5 but it is not necessarily the case.

6 Q. Okay. But is there another way to
7 do it?

8 A. Well, I mean in the field of
9 semiconductor devices, you know, we have various
10 ways of assembling integrated circuits into
11 packages where power or ground can be provided in
12 different ways such as through the back of the
13 substrate as an example.

14 So, it is not limited to just
15 vertical connectivity.

16 Q. Okay. But, in an example like this,
17 where ground is provided in the global mesh, the
18 customary way of getting that ground and power
19 down to the power domain would be vertically
20 through something like a via, correct?

21 A. That would be a reasonable way to do
22 it, yes.

1 Q. Okay. Now, when you see metal layer
2 M5, what do you understand as between metal layer
3 M5 and the power domains below?

4 A. One second. There is a discussion
5 about that in the specification.

6 For example, in Column 4 in
7 discussion of Figure 5, it says -- starting
8 Line 55, "In other words, the embodiments of the
9 invention need at least four metal layers to
10 implement the above global power mesh 400 and the
11 local power mesh 300."

12 So, the idea is that -- it goes on
13 to talk about, "The embodiments of this invention
14 can utilize these metal layers," these being M5
15 through M8, "to implement the global power mesh
16 400 and the local power mesh 300."

17 But it is not limiting the chip to
18 only four layers of metal. Of course, there can
19 be more.

20 And, there can be intervening.
21 There can be below M5. There is no restriction.
22 It is just using this or showing this as an

1 embodiment that four layers would be used for
2 purposes of global and local power meshes.

3 Q. Okay. And those four layers start
4 on metal layer M5, correct?

5 A. In this particular embodiment, but a
6 person of ordinary skill would understand it
7 doesn't have to.

8 Q. Okay. So, when you see metal layer
9 M5, you would see there are four metal layers
10 below metal layer M5, metal layers M1 through M4,
11 correct?

12 A. Right. It can be. It doesn't have
13 to be.

14 Q. Okay. And so, for the power to get
15 down from the global mesh or the local power mesh
16 to the power domain, if there are four layers in
17 between, M1 through M4, then the power would have
18 to go through those four layers as well, correct?

19 A. What do you mean go through? You
20 are suggesting that -- well, it has to -- the
21 power has to go down -- if we are talking about
22 vertical connectivity, yeah, it has to go down

1 from -- if it is from the global power mesh down
2 to the surface of the silicon.

3 That could be done through a via
4 stack, as an example. It doesn't have to connect
5 through any of the wiring in the lower metal
6 layers.

7 Q. Okay. But it does have to traverse
8 those lower metal layers, correct?

9 MS. WEISKOPF: Object to form.

10 THE WITNESS: Traverse meaning cross
11 the plane through which those metal layers
12 are arranged. Depending on how they are
13 arranged, yes, it can.

14 BY MR. WILSON:

15 Q. Okay.

16 A. It could also be done peripherally.
17 There are many different ways of doing it. It is
18 not limited to --

19 If you are talking about traversing
20 the plane, the horizontal plane, yes, it
21 traverses the horizontal plane, but it depends on
22 how it is constructed.

1 Q. Okay. Let's take a look at Claim 12
2 of the '218 patent.

3 Okay. So, in Claim 12, you have a
4 first partial local power mesh that is coupled to
5 the first power domain. Correct?

6 A. You are reading the first
7 limitation. You are summarizing the first
8 requirement there, the first --

9 Q. Yes, I am reading a portion of that
10 limitation, yes.

11 A. Okay, all right. So, yes, starting
12 so this is now Column 7. We are looking at
13 Claim 12. That limitation starts at Line 57 and
14 ends at Line 60.

15 Q. Okay. So you agree Claim 12
16 requires a first partial local power mesh
17 coupling to the first power domain, correct?

18 A. Yes.

19 Q. Okay. It also requires a second
20 partial local power mesh coupling to the second
21 power domain, correct?

22 A. That is correct.

1 Q. Okay. And the first and second
2 partial local power meshes are separate from each
3 other, correct?

4 MS. WEISKOPF: Object to form.

5 THE WITNESS: Well, what do you mean
6 by separate from each other? The
7 specification provides some guidance in that
8 regard.

9 BY MR. WILSON:

10 Q. So, they are not interconnected,
11 correct?

12 A. I don't know what that means. What
13 do you mean by interconnected?

14 Q. Okay. So, the first partial local
15 power mesh and the second partial local power
16 mesh are not coupled to each other. Correct?

17 MS. WEISKOPF: Object to form.

18 THE WITNESS: Now we are like three
19 different terms in. I am not quite
20 understanding precisely what the question is.

21 BY MR. WILSON:

22 Q. Okay. Do you understand there to be

1 any electrical connection between the first
2 partial local power mesh and the second partial
3 local power mesh in Claim 12?

4 A. No. So, when your question -- now
5 your question is clearer, because it is saying
6 that -- you are now talking about electrical
7 connections.

8 And there aren't any electrical
9 connections which is consistent with the
10 specification of the patent, because having
11 electrical connections between the partial
12 local -- the two different partial local power
13 meshes would result in short circuits. And that
14 would introduce electrical uncertainty.

15 So, in the context of electrical, my
16 expectation is that those two partial local power
17 meshes would not be electrically connected,
18 electrically interconnected, or whatever term
19 might be used, as long as we are talking about
20 electrical connectivity.

21 Q. Okay. Take a look at Column 4,
22 Line 49.

1 A. Yes.

2 Q. Okay. There it says, "As shown in
3 Figure 5, the global power mesh 400 is placed
4 above the local power mesh 300 and the partial
5 local power meshes 310, 320 of the local power
6 mesh are placed separately above each power
7 domain."

8 Did I read that correctly?

9 A. I'm sorry. You said Column 4,
10 Line 49.

11 Q. Yes.

12 A. I read that, yes.

13 Q. Okay. And I just read it. Did I
14 read it correctly?

15 A. I believe so, yes.

16 Q. Okay. And you see the term
17 "separately" on Line 52?

18 A. I do.

19 Q. Okay. Outside of the claims, that
20 is the only use of the term "separately" in
21 the '218 patent. Correct?

22 A. I haven't confirmed that.

1 Q. You can --

2 A. Are you asking me to check it?

3 Q. Yes, check it.

4 A. All right. Based on a search that I
5 have done, it appears that that is correct. Yes.

6 Q. Okay. So, the '218 patent provides
7 that the partial local power meshes of the local
8 power mesh are a separate -- well, first, let me
9 strike that.

10 The '218 patent provides that the
11 partial local power meshes of the local power
12 mesh are separate. Correct?

13 A. Well, in the context of the entire
14 specification, that is as correct, given the
15 understanding that a POSITA could achieve,
16 reading the spec.

17 And, for example, what I mean by
18 that is if you go back before Column 4, so going
19 to Column 3 and its discussion of partial local
20 power meshes, to provide that appropriate
21 context, starting at Line 45.

22 As an example, in Column 3 it says,

1 "It should be noted that the partial local power
2 meshes 310, 320, are not interconnected," which
3 means that the partial local power meshes 310 and
4 320 are mutually insulated to avoid mutual short
5 circuit that includes electrical uncertainty.

6 So, here the context of the local
7 power meshes being separately, as discussed
8 later, is in the context of ensuring that there
9 is no short circuiting between those partial
10 local power meshes.

11 Q. Right. The partial local power
12 meshes represent separate electrical paths,
13 correct?

14 MS. WEISKOPF: Object to form.

15 THE WITNESS: Well, you know, I
16 think that, when you are talking about
17 electrical paths, you can't just look at the
18 partial local power meshes alone. You have
19 to see how they are connected in the global.

20 So, now, I, I think now we need to
21 be guided by the entire spec, including the
22 claims, that talks about providing the power

1 separately that includes an assessment of how
2 that electrical connectivity goes up in the
3 global power mesh as well.

4 BY MR. WILSON:

5 Q. Okay. So, let's talk about that in
6 the context of ground.

7 So, are the partial local power
8 meshes 310, 320 separate paths from a ground
9 perspective?

10 MS. WEISKOPF: Object to form.

11 THE WITNESS: Separate paths from a
12 ground perspective?

13 Well, you know, it depends on the
14 design of the chip. I mean it doesn't have
15 to be. There can be a common ground. They
16 can, they can each have different grounds.

17 It really depends. And, it -- the
18 idea of Claim 12 to provide power separately
19 is to make sure that the power that is
20 delivered and provided as needed for each of
21 the first and second power domains is
22 provided separately, meaning separate

1 physical, electrical paths that are not
2 coupled for purposes of delivering power.

3 BY MR. WILSON:

4 Q. Okay. Does the '218 patent --

5 A. For the purposes of providing the
6 power needed, just to be clear.

7 Q. Does the '218 patent describe
8 anything other than a common ground?

9 MS. WEISKOPF: Object to form.

10 THE WITNESS: Does it describe
11 anything other than a common ground?

12 BY MR. WILSON:

13 Q. Yes.

14 A. I mean, I don't -- I mean there are
15 certain claims that are relevant to ground. It
16 talks about ground potential that is provided by
17 each of the power domains.

18 I'm not sure that it necessarily
19 limits it in all cases to be common. It can be,
20 but not necessarily.

21 And, so it depends on, it depends on
22 the -- it depends on the claims.

1 Q. So, let's take a look at Column 4,
2 Line 31.

3 A. Yes.

4 Q. Okay. There we are describing the
5 global power mesh 400 in Figure 4. Correct?

6 A. Yes. This is in the same discussion
7 as for Figure 4.

8 Q. Okay. And starting on Line 34, it
9 refers to the common ground wire 403 is used to
10 supply the ground potential VGND needed by the
11 local power meshes 310 and 320." Correct?

12 A. That is what it says for this
13 particular embodiment, yes.

14 Q. Okay. Do you understand Claim 12 to
15 cover this particular embodiment?

16 MS. WEISKOPF: Object to form.

17 THE WITNESS: Yeah. Claim 12, of
18 course, covers this embodiment, but Claim 12
19 isn't limited to having the same ground for
20 the power domains as yet.

21 Those are subject of further
22 dependent claims.

1 BY MR. WILSON:

2 Q. Okay. So, now I want to go back to
3 my original question which is, when we look at
4 the partial local power meshes, they do not have,
5 in your opinion, a separate path for ground.
6 Correct?

7 MS. WEISKOPF: Object to form.

8 THE WITNESS: Why do -- why do you
9 say that? Where is it that -- can you point
10 me to where I say that?

11 BY MR. WILSON:

12 Q. I'm asking you, if that is your
13 opinion.

14 A. Well, I mean my opinions are in my
15 declaration. And really to answer succinctly
16 your question, I would say it really depends on
17 the analysis that is done on a per integrated
18 circuit basis.

19 So, I'm not sure, you know, what the
20 question -- are you asking me that you cannot
21 have power delivered separately?

22 Power being delivered separately is

1 basically meaning that there can be no short
2 circuits that would result in electrical
3 uncertainty in terms of the power that is
4 delivered to the power domains.

5 Could those power domains have
6 common grounds? Yeah, they can. Could they have
7 separate grounds? Yes they can.

8 The power is delivered separately
9 regardless if, indeed, the power networks coming
10 in from the power paths through the global power
11 mesh through the respective partial local power
12 meshes are indeed electrically and physically
13 separate.

14 BY MR. WILSON:

15 Q. Okay. So, that is my point. The
16 grounds here in the global mesh and in the
17 partial local power meshes are not separate
18 paths, are they, in this example, in the '218
19 patent?

20 MS. WEISKOPF: Object to form.

21 THE WITNESS: In this example, they
22 are not separate paths, the grounds are not

1 separate paths?

2 BY MR. WILSON:

3 Q. Yes.

4 A. I'm not sure I understand that. Why
5 do you say that?

6 I mean, the specification talks
7 about wires that share the same properties can be
8 connected together.

9 So, to the extent that there are
10 grounds that are -- that have the same property,
11 they can be connected together. And that does
12 not affect the separate delivery of power as
13 needed by the respective power domains.

14 Q. Okay. So, so, it is your opinion
15 that the ground provided by the partial local
16 power meshes in this example in Figure 4 of
17 the '218 patent -- let me strike that. Let me
18 start over.

19 So, in your opinion in this example
20 in Figure 4 of the '218 patent, the partial local
21 power meshes provide ground via separate paths.
22 Is that correct?

1 MS. WEISKOPF: Object to form.

2 THE WITNESS: There is no
3 requirement to providing grounds through
4 separate paths.

5 The requirement is to provide power
6 needed separately. And, and that is not
7 affected by the ground. It depends on how
8 the ground is implemented between different
9 power domains.

10 But, as long as the, and the reason
11 is, as I quote here from Column 4, starting
12 at Line 16, it says, "Besides, the power
13 wires and ground wires of adjacent metal
14 layers having the same electrical property
15 can be interconnected to each other by via."

16 So, if there is a design where two
17 power domains share the same common ground,
18 then that can be done as explained in the, in
19 the specification without compromising the
20 ability of the different power domains being
21 provided with the power that they need
22 separately --

1 BY MR. WILSON:

2 Q. All right.

3 A. -- as required by the claim.

4 Q. Okay. You would agree that you
5 can't provide power without ground. Right?

6 A. There has to be a circuit. And
7 whether you call it a ground or not, there has
8 got to be a circuit, a way for the electricity
9 for the electrons to flow.

10 So, you could -- there has got to be
11 a potential difference. And, there has got to be
12 a circuit. And by circuit, I mean a path, a
13 closed path for electrons to flow.

14 You could name whichever terminal or
15 portion of that circuit, give it the name ground.
16 It could be a different level.

17 As long as there is a circuit that
18 has a potential difference that can drive an
19 electron flow.

20 MR. WILSON: Okay. We have been
21 going for about an hour. I'm happy to take a
22 break or keep going, whichever you prefer.

1 THE WITNESS: Sure. Can we do like
2 five minutes?

3 MR. WILSON: Sure.

4 THE WITNESS: All right.

5 THE VIDEOGRAPHER: Okay. The time
6 is 11:08 a.m. Off the record.

7 (Recess taken -- 11:08 a.m.)

8 (After recess -- 11:16 a.m.)

9 THE VIDEOGRAPHER: The time
10 is 11:16 a.m. We are back on the record.

11 BY MR. WILSON:

12 Q. Dr. Sourì, you still have Figure 4
13 in the '218 patent in front of you?

14 A. Figure 4. I do, yes.

15 Q. Okay. You have seen this figure
16 before, correct?

17 A. I have, yes.

18 Q. Okay. This figure shows the same
19 global power mesh that we were looking at in
20 Figure 5 earlier, correct?

21 A. This is identified as 400, which is
22 the embodiment of the global power mesh that is

1 also used in Figure 5.

2 Q. Now, Figure 4 labels three of the
3 wires on metal layer 8 as power wire 401, power
4 wire 402 and common ground wire 403.

5 Do you see that?

6 A. I do. You are referring -- just to
7 be clear, you are referring to the individual
8 three long rectangles, in landscape, going
9 vertically, that are annotated with the callout
10 boxes power wire 401, power wire 402 and common
11 ground wire 403.

12 Q. Okay.

13 A. And I agree, I see those as well,
14 correct.

15 Q. Okay. And the '218 patent teaches
16 that the power 401 is connected to one of the
17 partial local power meshes, correct?

18 A. Let's see. 401. So, it says
19 specifically -- or the way that it says it, one
20 way that it describes it in the specifications in
21 Column 4, Line 36.

22 It says, "The two power wires 401,

1 402, are used to supply the working voltages VDD1,
2 VDD2 needed by the local power meshes 310, 320,
3 respectively."

4 Q. Okay. So, okay.

5 So, in this passage that you are
6 referencing here, VDD1 would be power wire 401,
7 correct?

8 A. Well, VDD1 is the working voltage
9 that is supplied. And power wire 401 is used to
10 supply that VDD1 working voltage as needed by the
11 local or partial local power mesh 310.

12 Q. Okay. So, so we can say that the
13 partial local power mesh that is supplied by
14 power wire 401 is the 310 power mesh, correct?

15 A. I'm sorry. Can you repeat that
16 question again for me?

17 Q. Yes. So, if --

18 We can refer to the partial local
19 power mesh that is supplied by power wire 401 as
20 the 310 partial local power mesh, correct?

21 A. Well, I mean, that is --

22 Well, the way I would say it is that

1 power wire 401 is used to supply VDD1 to local,
2 partial local power mesh 310.

3 Q. Okay. All right. Fair enough.

4 A. That is just more -- that is more in
5 line with how the specification explains it.

6 Q. Okay. And power wire 402 is used to
7 supply working voltage VDD2 to partial local power
8 mesh 320, correct?

9 A. Needed by the local -- partial local
10 power mesh 320. That is how I would say it.

11 Q. Okay. And, the common ground wire,
12 403 is used to supply VGND, Vground, needed by the
13 local power meshes 310, 320, both of them.
14 Correct?

15 A. That is correct.

16 Q. Now could the power wire 401 also be
17 connected to partial local power mesh 320?

18 MS. WEISKOPF: Object to form.

19 THE WITNESS: I'm sorry. Your
20 question is could power wire 401 be connected
21 to partial local power mesh 320?

22 BY MR. WILSON:

1 Q. Yes. No -- sorry. Yes, that is
2 correct.

3 A. So, you are asking me if power wire
4 401 can be used to supply VDD1 to a partial local
5 power mesh 320?

6 Q. That's correct. That is my
7 question.

8 A. That would be inconsistent with
9 the '218.

10 Q. Okay. And similarly, it would be
11 inconsistent with the '218 to use power wire 402
12 to supply VDD2 to partial local power mesh 310.
13 Correct?

14 A. That is correct. In the way that it
15 is, in the way that that relationship is
16 described consistently in this specification,
17 correct.

18 Q. Okay. Now I want you to look at,
19 the same paragraph we are looking at there, but
20 the first sentence that begins "Similarly."

21 A. Yes.

22 Q. Okay. That passage says,

1 "Similarly, as the global power mesh 400 is to
2 supply voltage to the entire chip, each of the
3 horizontal and vertical power supply wires must
4 comprise one common ground wire 403 and two power
5 wires 401, 402."

6 Did I read that correctly?

7 A. You did, yes.

8 Q. Okay. So, in the global power mesh
9 400, each of the horizontal and vertical supply
10 wires comprises three wires, correct?

11 MS. WEISKOPF: Object to form.

12 THE WITNESS: I mean the way that
13 this is, I mean given the context of this
14 specification, a person of ordinary skill
15 would understand this to basically mean that
16 you've got this arrangement of power wires
17 401, 402 and common ground wire 403 present
18 in each of the arrangements of the layers, of
19 the global power mesh.

20 That is how I, that is how I and how
21 a person of ordinary skill would understand
22 it.

1 BY MR. WILSON:

2 Q. Right. But the text says is each of
3 the horizontal and vertical power supply wires
4 comprises three wires, one common ground wire and
5 two power wires. Correct?

6 MS. WEISKOPF: Object to form.

7 THE WITNESS: Well, the paragraph
8 says what it says. I'm providing you what I
9 and a person of ordinary skill would
10 understand by that text.

11 BY MR. WILSON:

12 Q. Okay.

13 A. It is -- yes, it is referring to the
14 collection of wires in each of the layers. And
15 it is saying that a person of ordinary skill
16 would expect to see a common ground wire and two
17 power wires in each of those layers.

18 Q. Well, and in each of those wires,
19 correct, that is what it says?

20 MS. WEISKOPF: Object to form.

21 THE WITNESS: Again, it says what it
22 says. I'm providing you my understanding as

1 at least from a perspective of a person of
2 ordinary skill which is, it is talking about
3 the layers on which these wires are arranged.

4 BY MR. WILSON:

5 Q. Okay. And if we look at Figure 4.
6 Now the three annotated wires, power wire 401,
7 power wire 402 and common ground wire 403, those
8 three collectively in the text that we just read
9 would represent a horizontal wire. Correct --

10 Or, sorry. A vertical wire.

11 Correct?

12 A. I'm not sure I'm understanding your
13 question. Each one of these is a wire. It is
14 annotated in Figure 4.

15 This is what I am saying is, you
16 can't just take an excerpt out of the
17 specification in isolation. It has got to be the
18 entirety of the spec including the figures to
19 understand what it is talking about.

20 And, here the figure, in Figure 4,
21 it is identifying by calling out in these boxes
22 individual wires. In this case three wires are

1 called out, power wire 401, power wire 402 and
2 the common ground wire 403 in that vertical
3 arrangement as seen in this landscape view of
4 this page.

5 So that is what it is highlighting.
6 That is what it is annotating.

7 Q. And the text describing that figure
8 says each of the horizontal and the vertical
9 power supply wires must comprise one common
10 ground wire 403 and two power wires 401, 402.
11 Correct?

12 A. That is what it says, and it is
13 consistent with what we are seeing here.

14 They are saying that it has got to
15 be at least -- one power wire 401, one power wire
16 402, a common ground wire 403 in each of the
17 arrangements of vertical and horizontal as an
18 example as shown here in Figure 4.

19 It is not limited, of course, to
20 this particular arrangement.

21 Q. Okay.

22 A. But the point is that each one of

1 these is a single wire as distinct from the
2 entire mesh.

3 So, the collection of the wires
4 makes up the mesh.

5 Q. So, let's turn over to Column 5,
6 Line 17.

7 A. Yes.

8 Q. Okay. That passage says, "On the
9 other hand, the common ground wire 402 also
10 conducts the external ground potential VGND to the
11 chip circuitry by coupling to the ground wires
12 311, 312 located by way of the via -- or, sorry,
13 located below by way of the via."

14 Correct?

15 A. That is what it says, but now this
16 is in the context of a different figure. Let me
17 go to -- this is Figure 6. Okay. So, Column 5,
18 Line 17.

19 So, yeah, it has also got the
20 numbers of the wires mixed around, because on
21 Line 14 it says the power supply wire 403.

22 Which in reference to 403, we know

1 that 403 is used to supply ground potential,
2 Vground.

3 Similarly, Column 5, Line 17, it
4 talks about a common ground wire 402, when
5 actually 402 is described earlier in the spec as
6 power wire, as well as in Figure 4.

7 So, with that, with that slight typo
8 there, it is saying that on the other hand -- I
9 understand it to say on the other hand, the
10 common ground wire, should say 403, also conducts
11 the external ground potential Vground to the chip
12 circuitry by coupling to the ground wires 311 and
13 312 located below by way of a via.

14 Q. Okay. And, so what about the ground
15 wires 311, 312?

16 As you just discussed, none of this
17 is depicted in Figure 6. Correct?

18 MS. WEISKOPF: Object to form.

19 THE WITNESS: Well, it is not -- it
20 is in a passage that is referring to
21 Figure 6, but, of course, the context is the
22 entirety of the specification.

1 I mean, the two lines before it in
2 Line 5, it is talking about Figure 4.

3 And just to be clear, 311 is, I
4 believe, it is a power wire in the partial
5 local power mesh.

6 Actually I have that in my
7 declaration.

8 Right. So, Figure 3 on my Page 24
9 of my declaration, I provide a typo
10 correction for Figure 3, as a person of
11 ordinary skill would understand it.

12 So, 311 in the partial local power
13 mesh 310 is a power wire. And 312 is a
14 ground wire in the partial local power
15 mesh 310.

16 And, so, I think that in the context
17 of Column 5, Line 20, that 311 would be -- it
18 is talking about a ground wire. It would be
19 likely to be 322.

20 BY MR. WILSON:

21 Q. So, you are saying in Column 5,
22 Line 20, the first number there ground wire 311

1 should be ground wire 322?

2 MS. WEISKOPF: Object to form.

3 THE WITNESS: Yes.

4 BY MR. WILSON:

5 Q. Okay. Now, and you are taking
6 that -- sorry. Let me strike that.

7 Okay. So, do you understand this
8 passage, as you have interpreted it with the
9 corrections to the reference numbers, to disclose
10 an example of the ground wires of the partial
11 local power meshes 322 and 312, connecting to a
12 same ground wire?

13 MS. WEISKOPF: Object to form.

14 THE WITNESS: Just give me a minute
15 to read it over again. Okay.

16 So, a couple of things. One is that
17 the paragraph which -- in Column 5, which
18 starts on Line 8, it talks about referring to
19 Figure 6, which shows a schematic diagram
20 illustrating the top view of the global power
21 mesh 400 and the local power mesh 300.

22 So, it is already giving us a

1 reference to earlier figures and examples.

2 So, Figure 6 contains all of the information
3 that is needed.

4 With respect to your question, the
5 common ground wire 402 conducts the external
6 ground potential Vground to the chip circuitry
7 by coupling to the ground wires 322 and 312
8 with the corrections located below by way of
9 the via.

10 Your question is, is this
11 identifying the single ground wire?

12 Now we are talking about Claim 18,
13 the sharing of the single ground wire -- is
14 that? Just for me to understand that
15 question better.

16 BY MR. WILSON:

17 Q. Yes, yes.

18 A. Okay. Yes. All right.

19 So, the answer is that, you know,
20 the connectivity in the vias is really not -- the
21 coupling here is really not the key to it.

22 It is identifying a single wire 402

1 that in the global power mesh that is providing
2 or being shared by the ground wires that are
3 identified in the partial local power meshes --
4 in the respective partial local power meshes.

5 So, in this case it is an example of
6 it that provides an embodiment for Claim 18.

7 MR. WILSON: Okay. I want to switch
8 to Exhibit 1006.

9 (Whereupon, previously marked
10 Exhibit 1006,
11 first referral.)

12 BY MR. WILSON:

13 Q. Now, Exhibit 1006 is the Chiu
14 reference. You are familiar with Exhibit 1006,
15 correct?

16 A. Just give me a moment to download
17 it.

18 And I have it up. And yes, I am
19 familiar with this reference.

20 Q. Okay. I want to look at a passage
21 in Column 2, Line 55.

22 So do you see the passage beginning,

1 "Generally," on Column 2, Line 55?

2 A. Yes.

3 Q. It starts out by saying, "Generally,
4 each of the voltage supply grids (positive and
5 negative) in an integrated circuit are associated
6 with the upper-most metal layers, are arranged in
7 a grid (as further discussed below) and are
8 coupled to cells and/or power-ground rails
9 associated with the middle or lower layers of the
10 integrated circuit using a piece of metal called
11 a via stack."

12 Do you see that?

13 A. I see that, yes.

14 Q. What do you understand the term
15 "cells" to mean, on Line 58 there?

16 A. Here cells are typically understood
17 to mean collection of components, electronic
18 components that may -- that generally make up a
19 circuit or a subcircuit or can be combined with
20 other cells to form circuits.

21 Generally, it is referring to
22 portions in the substrate, so circuitry formed in

1 the silicon.

2 Q. Okay. So, in this passage, Chiu
3 discloses that voltage supply grids, including
4 ground, are generally arranged in a grid.
5 Correct?

6 MS. WEISKOPF: Object to form.

7 THE WITNESS: I'm sorry. Say that
8 again.

9 BY MR. WILSON:

10 Q. Chiu discloses that voltage supply
11 grids, positive and negative, in an integrated
12 circuit are generally arranged in a grid.
13 Correct?

14 MS. WEISKOPF: Object to form.

15 THE WITNESS: It says, "each of the
16 voltage supply grids in an integrated circuit
17 are associated with the upper-most metal
18 layers are arranged in a grid." That is what
19 it says. Yes.

20 BY MR. WILSON:

21 Q. And Chiu discloses that these grids,
22 including positive and negative, are generally

1 connected to lower layers of the integrated
2 circuit using a via stack. Correct?

3 MS. WEISKOPF: Object to form.

4 THE WITNESS: I wouldn't say
5 connected to lower levels. I think what it
6 says here, they are coupled to cells, which
7 we have discussed means the silicon,
8 directly, and/or power ground rails, using a
9 piece of metal called a via stack.

10 So, it is talking about cells and
11 rails.

12 BY MR. WILSON:

13 Q. Okay. And both the cells and power
14 ground rails are lower in this example than the
15 voltage supply grids, correct?

16 A. As disclosed in Chiu, but with no
17 suggestion that the rails are in any way a mesh.

18 Q. Okay. What do you understand the
19 term "grid" to mean in this passage?

20 A. Well, that is referring to the
21 supply grid, the voltage supply grid. It is
22 referring to the upper most metal layers. That

1 is not how it is talking about the middle or
2 lower layers of the integrated circuit.

3 Q. Okay. What do you understand the
4 term "grid" to mean in this passage?

5 A. Well, I mean, you know, we talk
6 about voltage supply grids. It is just a network
7 ability to supply a voltage and power.

8 Q. It is a mesh, correct?

9 A. Not necessarily.

10 Q. It is an interconnection of wires
11 going in different directions, correct?

12 A. Not necessarily. It depends on how
13 they are designed. It is -- a grid here simply
14 is a term that we use with respect to voltage
15 supply grids or power supply grids, meaning a
16 network to supply power.

17 Q. Okay. So, it could just be wires
18 going in one direction?

19 A. In this case, as Chiu describes it,
20 it could be.

21 There is no disclosure that it has
22 to be a mesh as per the claim construction of

1 that term "mesh."

2 Q. Okay. Take a look at Column 5,
3 Line 8.

4 A. Okay.

5 Q. You see where it starts out, "In
6 prior art cell layouts"?

7 A. I do.

8 Q. It says, "Where the substantially
9 horizontal members of each of the power supply
10 grids, VDD1 108, VDD2 109, and VSS 110 are primarily
11 used to distribute the associated voltage level
12 of the grid throughout integrated circuit 100.

13 "The substantially vertical members
14 of each power supply grid are primarily used to
15 provide electrical connectivity to cells within
16 corresponding and respective voltage domains."

17 Did I read that correctly?

18 A. You did.

19 Q. It goes on to say, "According, the
20 substantially horizontal members are typically
21 located in a higher metal layer than the
22 corresponding substantially vertical members of

1 the power supply grids."

2 Did I read that correctly?

3 A. Yes. Yes.

4 Q. Okay. So, it's describing prior art
5 power supply grids as having horizontal and
6 vertical members on two different metal layers.
7 Correct?

8 MS. WEISKOPF: Object to form.

9 THE WITNESS: I -- generally that is
10 what it is describing in this passage -- in
11 this particular passage.

12 BY MR. WILSON:

13 Q. Okay. Now let's go back to
14 Column 2, and our passage beginning at Line 55.

15 Now, we talked about vertical
16 connectivity at the end of this passage in
17 Lines 60 to 61, using a piece of metal called a
18 via stack. Correct?

19 A. That is correct.

20 Q. Okay. In order for power to be
21 distributed from a grid to the cells or circuitry
22 below, using vias, the grid must be directly

1 above the circuitry. Correct?

2 MS. WEISKOPF: Object to form.

3 THE WITNESS: Well, it has -- there
4 has got to be a way to drop the vertical via
5 stack in a way where it lands somewhere on
6 the silicon such that that power can be
7 provided to the circuitry.

8 It depends on exactly where the
9 circuitry is on the substrate.

10 But, wherever it lands, it has got
11 to be able to distribute that power on the
12 surface of the silicon to the circuitry.

13 BY MR. WILSON:

14 Q. Okay. You would agree that for
15 power to drop down from a power supply grid to a
16 power domain underneath it, using a via stack,
17 there must be some overlap between the grid and
18 the power domain. Correct?

19 MS. WEISKOPF: Object to form.

20 THE WITNESS: I would think there
21 would be some way to have an overlap. It
22 doesn't have to be complete. It doesn't have

1 to be exact.

2 A way to reach vertically through
3 vias in that way.

4 BY MR. WILSON:

5 Q. Okay. Now, earlier you referred to
6 the aspect --

7 MR. WILSON: And we can push Chiu
8 aside for now.

9 BY MR. WILSON:

10 Q. Earlier you referred to the fact
11 that integrated circuits are typically
12 encapsulated in a package. Correct?

13 A. As an example.

14 Q. Okay. Insulated circuit packages
15 are -- sorry.

16 Integrated circuit packages are
17 typically insulated, correct?

18 A. What do you mean by that? I am not
19 sure I understand your question.

20 Q. So, the, the packaging that
21 surrounds a, an integrated circuit is typically
22 an insulating material. Correct?

1 A. Well, I mean the packaging is fairly
2 complex. It has got lots of different materials.

3 There can be materials typically
4 that are insulating. There can be materials that
5 are conducting. It depends on what you are
6 connecting to. There can be solder balls. There
7 can be bond wires. There can be lead frames.

8 And, certainly there is molding
9 compound that is used to protect the chip
10 against -- well, yeah, it provides some
11 electrical insulation, but it also protects
12 against environmental factors.

13 There are many materials involved in
14 packaging of an integrated circuit.

15 Q. Okay. So, the typical way for
16 power, ground and signal lines to get to the
17 integrated circuit is across the insulating
18 package, using the things that you just referred
19 to such as a solder bump, a pad, a pin, or some
20 type of lead wire. Correct?

21 A. Or a lead frame.

22 So your question is -- a typical

1 way? I mean, there are thousands of different
2 types of packages.

3 But, typically you would need
4 conductors to conduct electricity in and out of
5 the chip.

6 And so that can be done using any of
7 the mechanisms that we just listed as examples.

8 Q. Okay. And, one of the concerns of a
9 circuit designer in providing conductors that get
10 power and ground into the chip, is doing so with
11 a minimum amount of resistance, correct?

12 A. There are many concerns that a
13 designer has. Minimizing impedances, certainly
14 is a major one of them, yes.

15 Q. Okay. And --

16 A. And again it, it depends on, of
17 course, what you are --

18 Look, there are tradeoffs for
19 everything, so it depends what operating
20 frequencies we are talking about and what
21 performance expectations we have, and power
22 dissipation requirements.

1 But generally, yes, we try to
2 minimize power impedance.

3 Q. And a person of ordinary skill in
4 the art understood that in November of 2007.
5 Correct?

6 A. Yes, it is generally one of the
7 issues we are concerned about.

8 Q. Okay. One way to reduce the
9 resistance in the power supply or ground
10 conductors is to increase the cross-section of
11 metal over which the power or ground is
12 travelling. Correct?

13 A. Not necessarily. I mean there are
14 many different ways of doing it.

15 I'm not sure that that would be
16 automatically the first way that I would go for.
17 It really depends on a lot of different things.

18 Q. Okay. But it is one way, correct?

19 A. Well, it -- I mean, it is a way.
20 Whether or not it is reasonable, feasible,
21 practical, depends on wiring requirements of the
22 chip, how much real estate we've got, is

1 increasing cross.

2 So, generally speaking by increasing
3 the cross-sectional area reduces the resistance
4 per cross-section, per area provides basically
5 more surface area for electrons to flow.

6 But it depends on whether or not
7 that is a first order issue or are there other
8 bigger concerns with respect to where resistance
9 or impedance is being introduced.

10 Maybe there is a better way of
11 achieving improvement, performance improvement by
12 addressing other aspects of where resistance is
13 introduced. Such as, for example, areas where
14 conductors are joined together, soldered together
15 or how assembly is done on, say, interposer
16 boards or printed circuit boards.

17 There wouldn't -- I wouldn't
18 automatically just go with cross-sections.

19 It can be, but it depends on what
20 impact and what cost that would have on the chip
21 design.

22 Q. Okay. Another way to reduce

1 resistance in conductors providing power and
2 ground is to shorten the path that the power or
3 ground must travel over. Correct?

4 A. Generally, true. Yes.

5 Q. And, and a person of ordinary skill
6 in the art would have understand -- would have
7 understood the shortening the travel path or
8 widening the wire in November of 2007, correct?

9 MS. WEISKOPF: Object to form.

10 THE WITNESS: So, look, I didn't
11 push back too hard on you when you said
12 shortening of the wires, because generally
13 what that does is it reduces the
14 metallization requirement on a chip and
15 therefore it doesn't tax -- potentially tax
16 the chip area.

17 So, so, whereas increasing the
18 cross-sectional area may tax the chip area
19 and therefore result in larger chip. And
20 silicon real estate is really valuable.

21 So, I wouldn't automatically go with
22 increasing the cross-section.

1 I like the idea of shortening wires
2 in general. If we are able to achieve our
3 performance requirements, our timing analysis
4 requirements by shortening wires, absolutely.
5 That is a good way to do it.

6 But I wouldn't automatically go with
7 increasing the cross-section as a first line
8 of defense.

9 BY MR. WILSON:

10 Q. Okay.

11 A. It could, it could work. I'm just
12 saying that the analysis needs to be done.

13 Q. Okay, right. But, the --

14 A person of ordinary skill in the
15 art in November of 2007 understood the benefits
16 and detriments of widening a wire or shortening
17 the length of a wire in an integrated circuit
18 power supply. Correct?

19 MS. WEISKOPF: Object to form.

20 THE WITNESS: Among other
21 complexities, yes.

22 BY MR. WILSON:

1 Q. Now, you agree that designing a
2 power grid or network on two metal layers was
3 known in the prior art before November 2007.
4 Correct?

5 MS. WEISKOPF: Object to form.

6 THE WITNESS: Again, I mean a grid
7 here, even in Chiu, is used in Column 2.

8 Certainly Chiu continues to, later
9 on, as you indicated, in the disclosure
10 shows, gives example of what a grid might be
11 in that horizontal and vertical collection of
12 wires. But a grid isn't necessarily that.

13 But to your point, yeah, a network,
14 a network to supply power to a chip, yeah,
15 that is -- a person of ordinary skill would
16 understand that that is -- it is known in the
17 art.

18 BY MR. WILSON:

19 Q. Okay. So, why, as Chiu explains, is
20 it generally the case that a voltage supply grid
21 is arranged across the upper metal layers in an
22 integrated circuit?

1 MS. WEISKOPF: Object to form.

2 THE WITNESS: One second. I can --
3 the answer to your why question can be found
4 as an example in the '218. If I take you to
5 Column 5 of the '218. And let me see here.
6 Right.

7 Starting Line 30, "As was well-known
8 by those who were skilled in the art, the
9 lower metal layers are generally used for the
10 placement of metal wires that connect the
11 chip internal nodes compared to the higher
12 metal layers.

13 "Hence, the area of the lower metal
14 layers are more precious than that of the
15 higher metal layers."

16 And so, the idea is that the higher
17 metal layers would be, if it -- based on
18 the '218, if the higher metal layers are used
19 for power, that would provide for a more
20 efficient design.

21 BY MR. WILSON:

22 Q. Okay. And, more efficient in the

1 use of the metal layers, you are saying?

2 MS. WEISKOPF: Object to form.

3 THE WITNESS: Just essentially more
4 efficient in the way that power and signal
5 routing is done in a chip.

6 BY MR. WILSON:

7 Q. Okay. So, when you say more
8 efficient, is it more efficient from a space
9 perspective, from a metal usage perspective?
10 More efficient in what way?

11 A. Yeah, so, a lot of things, right.
12 So, space. You know, you are using
13 the -- if you are using the finer or lower --
14 lower layers of metal are typically a finer
15 pitch, smaller pitch, so they have lower
16 cross-section area.

17 There is more of them because you
18 are trying to keep those wires as dense as you
19 can so that you can conduct signals to all of the
20 different transistors and cells in the -- on the
21 surface of the silicon.

22 So, you really -- it is not an

1 efficient way to transfer power. You try, you
2 try to have power distributed through the thicker
3 cross-section wires in the higher tiers where
4 they are less dense.

5 And so, by trying to create or
6 design an architecture where power is distributed
7 mainly -- I'm not saying exclusively -- but more
8 of it is being distributed by the upper metal
9 layers.

10 That provides for overall better
11 performance of the chip, allowing for higher
12 density of wires in the lower layers of metal so
13 that you can send signals and connect to
14 transistors and cells, instead of having to fit
15 more and more power wires in those lower metal
16 layers.

17 Q. Okay. So, you are saying that the
18 power wires in the upper metal layers are
19 typically bigger and less dense than the power
20 wires in the lower metal layers?

21 A. Typically.

22 Q. Okay. And the density in the lower

1 metal layers is because of the need to drop power
2 down to the underlying circuitry in the substrate
3 vertically using vias, correct?

4 MS. WEISKOPF: Object to form.

5 THE WITNESS: You know, again it is
6 all driven by the requirements of the chip.

7 But, you know, generally speaking,
8 the closer you get to the transistors, the
9 finer your wires would be to be able to have
10 that resolution to drop down to your circuit
11 elements.

12 BY MR. WILSON:

13 Q. Right. Okay.

14 And, so, why then is power in the
15 upper metal layers typically arranged in a grid
16 or a network of horizontal and vertical wires?

17 A. Well, a grid isn't necessarily a
18 network of horizontal and vertical wires. It can
19 be, but not necessarily, as I have discussed
20 before.

21 So, you know, your question is --
22 well, it can be arranged in any number of ways

1 that is able to provide the power that is needed.

2 Q. Okay. So, why does Chiu describe in
3 the prior art arranging a voltage supply grid in
4 a plurality of horizontal and vertical wires?

5 I mean, that was a known concept
6 before November 2007. Correct?

7 MS. WEISKOPF: Object to form.

8 THE WITNESS: If your question is
9 are the -- it was -- the individual pieces of
10 prior art were known, but not in the way that
11 it is discussed in the '218, for purposes of
12 making it easier to design these complex
13 multi-power domain integrated circuits.

14 So, meshes -- to the extent that we
15 are talking about meshes, outside -- whether
16 within Chiu or outside, yeah, that was a
17 stand-alone concept. It was known but not in
18 the way that the '218 claims.

19 BY MR. WILSON:

20 Q. Okay. So, why would a person of
21 ordinary skill in the art use a mesh as a voltage
22 supply grid before November 2007?

1 MS. WEISKOPF: Object to form.

2 THE WITNESS: Well, again, it is
3 really dependent on the design of the chip
4 and how the designers wanted to connect to
5 the various cells and the underlying circuit
6 in the silicon or circuit elements in the
7 silicon, so it depends on where those might
8 be.

9 BY MR. WILSON:

10 Q. There must have been some efficiency
11 to the use of a mesh like that to a person of
12 ordinary skill in the art before November 2007.
13 Correct?

14 MS. WEISKOPF: Object to form.

15 THE WITNESS: There must have been a
16 reason, an efficiency?

17 I'm not sure I understand your --
18 I'm not sure I understand the question. I
19 mean --

20 We do, we do things based on --
21 again, we are trying to optimize. We are
22 trying to get the performance that we want to

1 meet performance requirements of the chips.

2 And certain designs will allow

3 for --

4 Look, there are constraints, right.

5 So, there are timing constraints. There is

6 performance constraints. There is power

7 dissipation constraints, there is power

8 capacitance and inductance constraints.

9 So, there are various constraints

10 that need to be met.

11 So, having a vertical and

12 horizontal, whether it is the same layer or

13 not, that is one way of achieving the desired

14 performance requirements.

15 BY MR. WILSON:

16 Q. Okay. So, it was at least common

17 before November 2007 to have a set of performance

18 requirements for which a power mesh with a set of

19 vertical and horizontal wires on two different

20 metal layers was a good solution. Correct?

21 MS. WEISKOPF: Object to form.

22 THE WITNESS: I, I mean the answer

1 is it depends. I mean, let me, if there is
2 something specific -- a particular article
3 about efficiency that you have in mind, I
4 would love to take a look at it.

5 But certainly having wires in -- to
6 distribute power in a mesh-like arrangement,
7 you know, one layer or more, that in itself
8 was known, but not in the way that the '218
9 claims.

10 BY MR. WILSON:

11 Q. Okay. And it was known because it
12 was an efficient solution to the collective set
13 of power distribution problems an integrated
14 circuit designer might come across, correct?

15 MS. WEISKOPF: Object to form.

16 THE WITNESS: I'm not sure I know
17 how to answer that. It depends, it depends
18 if it is the right solution or not.

19 There are many different solutions.

20 MR. WILSON: Okay. I want to
21 quickly take a look at Exhibit 1007. This is
22 Jiang2.

1 (Whereupon, previously marked
2 Exhibit 1007,
3 first referral.)

4 BY MR. WILSON:

5 Q. And you are familiar with Jiang2,
6 correct?

7 A. Yes, yes I am. One second.

8 Q. Okay.

9 A. Okay. I have it up.

10 Q. Okay. Take a look at the second
11 page at Figure 1 there.

12 A. I see that.

13 Q. Okay. You would agree that if the
14 power domain in the front left is powered down
15 and the power domain in the back right is powered
16 up, the two power domains have different power
17 requirements, correct?

18 A. No, I disagree. There are no power
19 domains here, in the context as a person of
20 ordinary skill understands power domain, and in
21 the context of the '218.

22 Q. Okay. So, take a look at Page 1.

1 Under Roman Numeral two there, middle of the
2 paragraph, do you see the line that begins, on
3 the far right, it says, "In a power gating
4 system"?

5 A. I see that, yes.

6 Q. It says, "In a power gating system,
7 a circuit is divided into several power domains.
8 Each domain is independently controlled by a
9 sleep transistor."

10 Did I read that correctly?

11 A. You did. And that is exactly my
12 point.

13 The way that Jiang -- this
14 particular Jiang reference talks about power
15 domains in the context of a power gating system.

16 So it is really a power gating
17 domain. It is not the power domain that is in
18 the context of the '218 patent.

19 Q. Okay. So, let's use your
20 terminology then. Let's look back at Page 2 in
21 Figure 1.

22 So, you would agree that if the

1 power gating domain in the front left is powered
2 down and the power gating domain in the back
3 right is powered up, the two power gating domains
4 have different power requirements, correct?

5 A. No, I disagree.

6 Q. Okay. So, they have the same power
7 requirements, when one of them is powered down?

8 A. Well, look, a power requirement is a
9 power requirement, right?

10 It is, what does that -- in this
11 case this macro or power gating, power gated
12 domain, it is what is its power requirement.

13 By simply shutting off the power to
14 it, that is not changing its power requirement.

15 You are changing whether you are
16 providing power or not providing power.

17 That says nothing about the power
18 requirement of the underlying macro.

19 So, I disagree that the requirement
20 of the power would change simply by flipping a
21 switch on or off to affect the delivery or
22 provision of power.

1 Q. Okay. Take a look at the '218
2 patent, Column 7.

3 A. Okay. I am --

4 Q. Okay. The last limitation on, in
5 this column on Claim 12, the global power mesh.
6 And in the middle of that limitation, you see the
7 language, "To provide the power needed by the
8 first power domain and the second domain
9 separately."

10 Do you see that?

11 A. I do.

12 Q. Okay. So, let's go back to the
13 example that we were referring to earlier in
14 the '218 patent, in Figure 4.

15 If you build a chip that looks like
16 this, okay, like Figure 4, but you never supply
17 power to the chip, can it meet the "to provide
18 the power needed by the first power domain and
19 the second domain separately" limitation of
20 Claim 12?

21 MS. WEISKOPF: Object to form.

22 THE WITNESS: I'm sorry. I'm not

1 quite sure I understood your question.

2 Your question is, if, your question
3 is if I never -- if I don't --

4 If I never operate this chip, does
5 it meet the requirements of Claim 12?

6 BY MR. WILSON:

7 Q. Yes.

8 A. Well, Claim 12 requires a power
9 routing structure that comprises, among other
10 things, a global power mesh to provide the power
11 needed.

12 So, if there is a global --

13 If my analysis determines of this
14 chip that there is a global power mesh, in
15 part -- assuming all of the other requirements
16 are met.

17 That there is a global power mesh in
18 there to provide the power needed, then it meets
19 the claim language.

20 Q. Okay. Regardless of whether you
21 ever powered up, correct?

22 A. Well, I, I don't -- so, I don't --

1 There is no requirement in Claim 12
2 that says you have to turn the chip on, but the
3 difference between this and a sleep transistor is
4 that the sleep transistor is not part of a, a
5 global power mesh.

6 And so, the sleep transistor in the
7 Jiang reference would be essentially turning the
8 power off, preventing any provision of power
9 needed by the -- by whatever the macro or the
10 cells are in the Jiang reference.

11 Q. Okay. What if, what if you in this
12 same example in Figure 4, you have the ability to
13 keep power wire 402 at either the voltage on
14 power wire 401 or 0 voltage, would it still meet
15 this limitation in Claim 12 to provide the power
16 needed by the first power domain and the second
17 domain separately?

18 MS. WEISKOPF: Object to form.

19 THE WITNESS: I'm not sure I follow
20 your -- you are asking me a hypothetical.

21 So, power, power wire 402, if I, if
22 I can go back to the specification is

1 described as -- yes, so again here, Column 4,
2 Line 36.

3 "The two power wires 401, 402 are
4 used to supply the working voltages VDD1, VDD2
5 needed by the local power meshes 310 and 320,
6 respectively."

7 So, those are bringing in power
8 from, whether it is from outside the chip or
9 generated somehow into the chip to deliver
10 power internally to the respective power
11 domain.

12 So, you want to change that external
13 power supply to, for, of that -- that is
14 provided --

15 So, you want to change VDD2 to VDD1.

16 Is that your question?

17 BY MR. WILSON:

18 Q. So, let's start there. Let's assume
19 that VDD1 and VDD2 are equal.

20 Does this example in the '218 patent
21 meet Claim 12?

22 A. Well, I --

1 MS. WEISKOPF: Object to form.

2 THE WITNESS: I would have to do the
3 analysis, because now you have a single --

4 Well, is it a single power supply?

5 Or is it VDD1 and VDD2 but they happen to be
6 the same nominal voltage?

7 And -- I would have several
8 questions to clarify that hypothetical.

9 BY MR. WILSON:

10 Q. Okay. Well, let's assume that they
11 are the same voltage -- they are just the same
12 voltage. It is not a single power supply. They
13 are just the same voltage.

14 MS. WEISKOPF: Object to form.

15 THE WITNESS: All right. If it is
16 the same voltage, they are two different
17 power supplies.

18 Is there anything about the power
19 domains that has changed since now we have
20 changed VDD2 to be equal to VDD1 in nominal
21 value at least?

22 BY MR. WILSON:

1 Q. No.

2 A. Okay. So, the power requirement of
3 the power domain that is associated with power
4 wire 402 hasn't changed.

5 Q. Correct. In my hypothetical, that
6 is correct.

7 A. Right. I, I have -- let's see. And
8 what else is there?

9 Yeah, I think the answer is, it
10 depends, right.

11 It depends on -- so now you still
12 have two separate power supplies, they may
13 nominally have the same voltage but they've got,
14 they've got -- it is two independent power
15 supplies.

16 And, I would still need to do the
17 analysis of the claim to make sure that the power
18 is delivered separately.

19 And then the next question would be
20 well, is the power domain -- the second power
21 domain designed in a way that it can -- its power
22 that is needed can be changed based on the

1 fluctuations or changes in the power supply
2 supplying VDD2.

3 So, the answer is, it really depends
4 on a lot of things. I'm not sure that I have
5 enough information in this hypothetical to give
6 you an answer.

7 MR. WILSON: Okay. We have been
8 going for about an hour. Are you guys ready
9 to take a break? Do you want to take a lunch
10 break? What do you want to do?

11 THE VIDEOGRAPHER: Should I go off
12 the record?

13 MR. WILSON: Yes, let's go off the
14 record.

15 THE VIDEOGRAPHER: Okay. The time
16 is 12:17 p.m. We are going off the record.

17 (Recess taken -- 12:17 p.m.)

18 (After recess -- 12:48 p.m.)

19 THE VIDEOGRAPHER: The time
20 is 12:48 p.m. Back on the record.

21 BY MR. WILSON:

22 Q. Okay. Dr. Sourì, let's look at

1 the '218 patent, and I want to look at Claim 19.

2 So, take your time, review the
3 claim. And my question is going to be, is there
4 anything in Claim 19 that precludes a local power
5 mesh between the global power mesh and the power
6 domains?

7 MS. WEISKOPF: Object to form.

8 THE WITNESS: Okay. Sorry. The
9 question again is, is there anything in
10 Claim 19 that precludes -- what was it again?

11 BY MR. WILSON:

12 Q. A local power mesh between the
13 global power mesh and the power domains.

14 MS. WEISKOPF: Object to form.

15 THE WITNESS: Okay. One second. I
16 have a section discussing this in my
17 declaration, specifically starting at
18 Paragraph 103, on my Page 39, where I talk
19 about the differences between Claim 12 and
20 Claim 19, in part.

21 And I say in Paragraph 104, "In
22 contrast to Claim 12, a POSITA would

1 understand that Claim 19 recites a different
2 structure in which the global power mesh
3 couples to the power domains without any
4 intermediary partial local power meshes."

5 Because it says, "coupling the first
6 power wire of a global power mesh to the
7 first power domain."

8 And, there -- based on the
9 differences between Claims 12 and 19, my
10 opinion is that a POSITA would understand
11 that the connection between the power wires
12 of the global power mesh and the power domain
13 is separately claimed in Claim 19 and that it
14 is different from the structure of Claim 12.

15 BY MR. WILSON:

16 Q. Right. I understand that. My
17 question is different.

18 My question is, is there anything in
19 Claim 19 that precludes an intervening local
20 power mesh between the global power mesh and the
21 first or second power domain?

22 MS. WEISKOPF: Object to form.

1 THE WITNESS: Well, I'm not sure if
2 you are asking me is there -- so, I mean I'm
3 looking at it as the totality, of course, of
4 the '218 patent and the claims.

5 So, when I look at Claim 19, I'm
6 also looking at it in the context of other
7 claims. And Claim 19 is clearly different
8 from Claim 12.

9 So, Claim 12 has that routing
10 structure that includes the partial local
11 power meshes, and that is absent in Claim 19.

12 So, a person of ordinary skill in
13 the art would understand that Claim 19 is
14 really directed towards a different type of
15 connection and supported by embodiments in
16 the specification.

17 So, I'm not sure if your question is
18 well, look you know just ignore everything
19 else and just look at the language without
20 any, without any reference to how a person of
21 ordinary skill would understand the rest of
22 the '218.

1 I'm not sure that that is your
2 question.

3 But based on my understanding of
4 Claim 19, it claims a different structure.

5 BY MR. WILSON:

6 Q. Okay. You know, either you are not
7 understanding my question or something else is
8 going wrong in the Q&A here.

9 But my question is different than
10 the question you are answering.

11 I understand you think Claim 19 is
12 directed to a different structure than Claim 12.

13 A. Okay.

14 Q. My question is whether there is
15 something within a limitation in Claim 19 that
16 precludes an intervening local power mesh between
17 the global power mesh and the first or second
18 power domains.

19 And if there is such a limitation,
20 please point it out to me.

21 MS. WEISKOPF: Object to form.

22 THE WITNESS: Well, I mean I think

1 the language of the claim itself tells me
2 that, right?

3 It says, "Coupling the first power
4 wire and the ground wire of the global power
5 mesh to the first power domain by the APR
6 tool."

7 So, that is one of them. And then
8 of course there is a similar one for the
9 second power wire and the second power
10 domain.

11 So, the language of the claim itself
12 tells me that it is a different structure
13 from Claim 12.

14 BY MR. WILSON:

15 Q. Okay. So, if there is an
16 intervening local power mesh between, for
17 example, the first power wire and the ground wire
18 of the global power mesh, and the first power
19 domain, then the first power wire and the ground
20 wire of the global power mesh is not coupled to
21 the first power domain in your opinion?

22 MS. WEISKOPF: Object to form.

1 THE WITNESS: No, that is not, that
2 is not, that is not what I am saying.

3 I'm saying just the way that the
4 language is written here, the -- there can be
5 other metal layers that are between the metal
6 layers where the global power mesh is and the
7 power domains, or the surface of the silicon,
8 for example, where the power domains are.

9 But there is nothing in this claim
10 that says you can't have intervening metal
11 layers.

12 But when it is talking about
13 coupling, it is talking about coupling to the
14 first power domain straight from the global
15 power mesh.

16 BY MR. WILSON:

17 Q. So, in your interpretation of
18 coupling in Claim 19 between the first power wire
19 and the ground wire of the global power mesh and
20 the first power domain, you think that coupling
21 has to be direct, with no intervening power
22 meshes, correct?

1 A. Well, I'm not sure what you mean by
2 no intervening.

3 I mean, there can be other layers,
4 of course, in between.

5 But, we are talking about a coupling
6 that is from the global to the respective power
7 domains.

8 Q. Right. And we all understand, as we
9 discussed earlier, that you would traverse
10 multiple metal layers to make that connection.
11 Correct?

12 A. Correct.

13 Q. Okay. So, the coupling is not
14 direct in the sense of not traversing other metal
15 layers, correct?

16 MS. WEISKOPF: Object to form.

17 THE WITNESS: It is not direct in
18 that it is not traversing. It can traverse
19 other metal layers.

20 But that vertical stack is from the
21 global power mesh to the respective power
22 domains, as an example of using a vertical

1 stack.

2 BY MR. WILSON:

3 Q. So, when you are saying a vertical
4 stack, you are saying a via stack direct from the
5 global power mesh down to the power domain?

6 A. As an example, yes. As an
7 embodiment that is also discussed in the
8 specification, specifically, I discuss it in
9 Paragraph 108 in my report, or in my declaration
10 where I can say that -- or where I do say, "In
11 another embodiment the specification explains
12 that the local power mesh can be emitted in the
13 invention."

14 And a quote from Column 6, Lines 9
15 to 14, "Only the global power mesh 400 is used to
16 conduct the external power into the chip."

17 Q. Okay. I understand that in your
18 opinion Claim 19 covers that embodiment.

19 What I'm trying to understand is if
20 it excludes other embodiments in the '218 patent
21 that use a local power mesh.

22 And I think you are testifying that

1 it does. Is that correct?

2 A. Let me just see. Yes, as I say in
3 the Paragraph 104, I say, "In contrast to
4 Claim 12, a POSITA would understand that Claim 19
5 recites a different structure in which the global
6 power mesh couples to the power domains without
7 any intermediary partial local power meshes."

8 That is how I would -- that is how I
9 am comfortable putting it in my language.

10 Q. Okay. So, I can read that language
11 one of two ways.

12 I can read that language as covering
13 a scenario in which there are no intermediary --
14 intermediary partial local power meshes.

15 Or I can read it as the -- it only
16 covers the situation without any intermediary
17 partial local power meshes.

18 In other words, Claim 19 is limited
19 to the situation in which there are not any
20 intermediary partial local power meshes.

21 I'm asking you which of those
22 positions you are taking.

1 A. So, the position that I'm taking is
2 further explained in my Paragraph 105, where I
3 say that, "A POSITA would understand that the
4 term 'global power mesh, coupling to the first
5 local power mesh,'" as used in Claim 12, "is
6 different from coupling a power wire of the
7 global power mesh to the first power domain."

8 So, I am saying here that Claim 19
9 is really talking about going straight from the
10 global power mesh to the respective power
11 domains.

12 Q. Okay. So in your opinion, Claim 19
13 is limited to the scenario in which there are no
14 intermediary partial local power meshes.
15 Correct?

16 MS. WEISKOPF: Object to form.

17 THE WITNESS: You know again, the
18 way I am comfortable saying it is exactly
19 that language between 19 and 12 are different
20 in that 19 is directed to a different
21 structure than Claim 12.

22 Where Claim 12 has a requirement for

1 that intermediary layers, 19 does not.

2 BY MR. WILSON:

3 Q. Okay. So, you don't know, as you
4 sit here today, whether or not Claim 19 is
5 limited to the scenario in which there are no
6 intermediary partial local power meshes; is that
7 correct?

8 MS. WEISKOPF: Object to form.

9 THE WITNESS: No, that is not my
10 opinion. All I'm saying is that the language
11 is different between 12 and 19, where 19 is
12 directed towards a direct connection between
13 the global and the respective power domains.

14 BY MR. WILSON:

15 Q. Right. And I'm trying to understand
16 the difference in the language that you are
17 perceiving in these claims. And I'm not hearing
18 an answer.

19 Is Claim 19 limited to the scenario
20 in which there are no intermediary partial local
21 power meshes or not?

22 MS. WEISKOPF: Object to form.

1 THE WITNESS: I mean, the best I can
2 explain to you is how I say it in my
3 declaration, which is that there is language
4 that specifies coupling to the first and
5 second local power meshes in Claim 12, that
6 does not exist in Claim 19.

7 That difference in language, as well
8 as in the context of the '218 with
9 descriptions of embodiments, Claim 19 is
10 directed towards a direct connectivity
11 between the global power mesh and the
12 respective power domains. That is how I
13 understand.

14 BY MR. WILSON:

15 Q. Okay. So, in other words you don't
16 know.

17 A. That is not -- no, that is
18 mischaracterizing what I said.

19 Q. Okay. Let me ask it a different
20 way.

21 Claim 19 recites coupling the first
22 power wire of the global power mesh to the first

1 power domain. Right?

2 A. In part, yes.

3 Q. Okay. If -- is the first power wire
4 coupled to the first power domain if there is an
5 intervening partial local power mesh?

6 MS. WEISKOPF: Object to form.

7 THE WITNESS: So, let me understand.
8 Are you asking if there exists an
9 intermediate set of layers that -- and the
10 via stack, as an example, traverses through
11 those intermediate metal layers.

12 Are you saying, okay, that is there
13 a difference between that and, say, the via
14 stack happening to connect to a wire in those
15 intermediate layers?

16 Is that a correct understanding of
17 your question?

18 Q. So, I'm not sure. I'm not sure what
19 you are asking.

20 But, let's, let me give you perhaps
21 a more detailed hypothetical.

22 A. Sure.

1 Q. If we look back at Figure 5 --

2 A. Okay.

3 Q. -- in the '218 patent.

4 A. Okay.

5 Q. And let's assume we have the
6 scenario that is shown here.

7 A. All right.

8 Q. But in my question, would Claim 19
9 read on a power wire that drops from metal 7 down
10 to metal 6, traverses a wire horizontally or --
11 well, actually in this case, traverses a wire
12 vertically on metal 6, and then traverses another
13 wire horizontally on metal 5 and then drops down
14 to the power domain, would that be coupled in the
15 sense required by Claim 19?

16 A. I see now what you are saying. And
17 in that specific hypothetical, I don't think so.
18 I don't see Claim 19 reading on that. But it
19 really does depend on the arrangement.

20 Suppose the vertical stack of vias
21 connecting from M8 or M7 down, suppose it does
22 connect to a wire on M6 and in M5 but there is no

1 traversing across horizontally or vertically,
2 just kind of dropping down to the respective
3 power domain, that is a direct coupling from the
4 global to the respective power domain.

5 Q. Okay.

6 A. And that would be within the scope
7 of Claim 19 as a person of ordinary skill would
8 understand that arrangement.

9 Q. Okay. And is it the -- is it your
10 interpretation of the word "coupling" that
11 requires that direct connection?

12 MS. WEISKOPF: Object to form.

13 THE WITNESS: Not necessarily the
14 word "coupling."

15 It is looking at the difference in
16 the language used between Claim 12 and
17 Claim 19. Where Claim 12, as I was
18 explaining earlier, talks about explicitly
19 the coupling to the first local power mesh.

20 And that is different language from
21 that used in Claim 19, as well as how the
22 embodiments are explained in the '218.

1 MR. WILSON: Okay. Henry, can we
2 pull up Tab 1 and I'm going to mark Tab 1 as
3 Exhibit 1040.

4 (Whereupon, previously marked
5 Exhibit 1040,
6 first referral.)

7 THE VIDEOGRAPHER: I will put that
8 up in just one second.

9 THE WITNESS: Okay. One second.
10 Let me just download this.

11 MS. WEISKOPF: I'm going to object
12 to this as outside the scope of his
13 declaration.

14 THE WITNESS: Okay. I have it.

15 BY MR. WILSON:

16 Q. Okay. And this is a 7th edition of
17 the IEEE Dictionary.

18 You are familiar with the IEEE
19 Dictionary, correct?

20 A. Yes. I'm familiar with -- there are
21 various IEEE Dictionaries, and this one looks
22 like it is a -- obviously not the whole thing,

1 but seven pages extracted from what appears to be
2 the 7th edition.

3 I would need to confirm that, but
4 that is at least how it appears.

5 Q. Okay. If you look at the third
6 page, you can see the copyright date of this
7 particular edition is 2000.

8 Do you see that?

9 A. I see that, yes.

10 Q. Okay. So, if we go down to the
11 sixth page, in the very bottom right, you see a
12 definition of coupling. Do you see that?

13 A. I do.

14 Q. And that definition reads, "The
15 association of two or more circuits or systems in
16 such a way that power signal information may be
17 transferred from one to another."

18 Did I read that correctly?

19 A. So far.

20 Q. Do you have any reason to agree or
21 disagree with that definition of coupling?

22 MS. WEISKOPF: Object to form.

1 THE WITNESS: Well, one, I will note
2 that you are reading a particular entry and
3 only partial with respect to ground systems.

4 There are a number of other entries
5 under coupling here. In this particular
6 dictionary set of entries, there is seven of
7 them.

8 And, again, I would say that a --
9 there -- what you are reading here is
10 consistent with my understanding, but also I
11 would say that a person of ordinary skill
12 would have to understand it in the context of
13 the patent.

14 So, it is not just simply taking
15 something out of context.

16 BY MR. WILSON:

17 Q. Okay. Okay. Let's take a look at
18 Paragraph 1 --

19 A. And just to continue with that, if
20 you look at, for example, entries for 6 and 7, 6
21 talks about various types of coupling, right, so,
22 magnetic, capacitive, conductive or resistive

1 coupling.

2 So again -- and these are all
3 relevant to the concept of coupling in an
4 integrated circuit.

5 And, so you can't just read the
6 first entry for ground systems. I mean, this may
7 or may not be completely relevant to integrated
8 systems -- integrated circuits, because it -- the
9 first entry is talking about close or loose
10 coupling versus the Entry Number 6 is talking
11 about -- is talking about propagation of energy
12 and discusses the various types of coupling.

13 And Entry Number 7 talks about
14 association of two or more circuits or systems in
15 such a way that power or signal information may
16 be transferred from one system or circuit to
17 another.

18 Again, these are -- there are a lot
19 of different definitions as provided here by the
20 IEEE Authoritative Dictionary that you have here
21 in front of me.

22 And what exactly it is that applies

1 to the '218 is guided by the disclosure of
2 the '218.

3 Q. Okay. But out of these collection
4 of definitions, you think that 1, 6, and 7 are
5 potentially relevant to the '218 patent?

6 A. I haven't spent enough time, of
7 course, on this to kind of give you an expert
8 analysis on it.

9 All I'm saying is it appears to have
10 multiple definitions. And I don't necessarily
11 agree that only one of them is relevant to the
12 one -- to the '218.

13 I would say that I would need to
14 study it in more detail. It does convey the idea
15 that there can be different types of coupling.

16 And as discussed at least in Entry
17 Number 6 for the definition of coupling, I would
18 use at least such concepts, along with the
19 guidance of the '218, as a person of ordinary
20 skill would understand.

21 Q. Okay. So, definition 6 refers to
22 the mode of propagation of disturbing energy from

1 a power system to a telecommunications system.

2 Do you understand the '218 patent to
3 disclose a telecommunications system?

4 A. Well, it depends what we mean by a
5 telecommunications system.

6 I mean, you know, to the extent
7 that -- if it is talking about a
8 telecommunication system like communicating cell
9 phones or wireless communications, then yes, you
10 know, that is different from an integrated
11 circuit.

12 But there are concepts explained in
13 Entry Number 6 for coupling that are common to
14 integrated circuits such as capacitive coupling
15 and resistive coupling, I mean, and inductive
16 coupling for that matter.

17 We even have some of the references
18 that are relied on that talk about RLC networks,
19 those are resistive, inductive and capacitive
20 networks.

21 So, clearly there are concepts here
22 that are relevant that need to be taken into

1 account.

2 Q. Okay. All right. Let's look at
3 your declaration, Paragraph 142.

4 A. Yes. I'm at 142.

5 Q. Okay. Paragraph 142 is referring to
6 the schematic in Figure 1B of Jiang, correct?

7 A. Just one second. Yes, that is
8 correct.

9 Q. Okay. If we go down to the last
10 sentence in that paragraph, you say, "A POSITA
11 would therefore understand that the sleep
12 transistor is itself part of a power domain."
13 Correct?

14 A. That is correct.

15 Q. Okay. But you do not identify which
16 power domain in Jiang it is a part of. Correct?

17 A. Jiang does not disclose power
18 domains.

19 Q. Well, but you said a person of
20 ordinary skill in the art would understand that
21 the sleep transistor is part of a power domain,
22 correct?

1 A. To the extent that there is a single
2 power domain that is -- that would be discussed,
3 that would be at best what we are discussing
4 here.

5 And Jiang does not disclose the
6 power domains as required by the '218.

7 Q. Okay. But in your opinion, a person
8 of ordinary skill in the art would understand
9 there is a power domain in Jiang, correct?

10 A. No. Jiang discloses macros. It
11 does not disclose power domains, in the plural
12 form, as required by the '218.

13 Q. Okay. So, would a POSITA then not
14 understand that the sleep transistor in Jiang is
15 part of a power domain?

16 A. Well, like I said, at best, Jiang
17 would disclose a single power domain. So, these
18 sleep transistors are part of, at best, a single
19 power domain.

20 Q. Okay. Now, the sleep transistors
21 are not powered from the local power meshes on
22 L2. Correct?

1 A. What do you mean by that question?

2 Q. The signal that controls whether the
3 sleep transistors are opened or closed does not
4 come from the local power meshes on L2. Correct?

5 A. Jiang is silent as to where -- if
6 you are talking about the signals that control
7 the gates of those sleep transistors, Jiang is
8 silent as to where they come from.

9 Q. Well, a person of ordinary skill in
10 the art would understand that the signal can't
11 come from the local power meshes or it would be
12 inoperable, correct?

13 A. I'm not sure I understand that
14 question.

15 Q. Well, if the sleep transistor is
16 open, if the gate is closed, let's say, there is
17 no power in the local power meshes above macros B
18 and C, correct?

19 MS. WEISKOPF: Object to form.

20 THE WITNESS: Yeah. No, I'm sorry.
21 I'm not sure I agree with that.

22 So, now the sleep transistor exists

1 in the surface of a silicon, right.

2 And so now you are saying -- you are
3 asking me a hypothetical where the sleep
4 transistor is on or off?

5 BY MR. WILSON:

6 Q. I'm asking you a scenario where the
7 sleep transistor is off, power is gated off.

8 A. So, there it is not -- it is turned
9 off all power to whatever macro, whether it is B
10 or C, it is turned off that power to those
11 macros?

12 Q. Yes, that is the hypothetical.

13 A. Okay. Go ahead.

14 Q. In my hypothetical where the power
15 is turned off to macros B and C, the sleep
16 transistors still can receive a signal. Right?

17 A. They can receive a signal, yes.

18 Q. Okay. So therefore that signal
19 cannot come from the local power meshes above
20 macros B and C, correct?

21 MS. WEISKOPF: Object to form.

22 THE WITNESS: They can come from

1 different -- it depends on how this is --
2 again what you are looking at in Figure 1B is
3 just a cartoon representation. It is not a
4 depiction of an actual chip.

5 And the sleep transistors would be
6 controlled in a way where the gate signals
7 can come in from a different part of the chip
8 that is able to control them.

9 But whether or not it can come in
10 through the local power meshes, I mean that
11 is -- that is something that is silent in
12 Jiang.

13 BY MR. WILSON:

14 Q. Well, if it comes in through the
15 local power mesh, once you gate off the sleep
16 transistor, it can never be turned back on,
17 correct?

18 MS. WEISKOPF: Object to form.

19 THE WITNESS: I'm not sure -- I
20 don't know why you say that.

21 Where -- what are you pointing to or
22 what are you using to assume that?

1 BY MR. WILSON:

2 Q. Well, how do you get a signal to
3 turn the sleep transistor back on from a local
4 power mesh that has no power?

5 MS. WEISKOPF: Object to form.

6 THE WITNESS: There can be, there
7 can be -- there are different wires in a
8 power mesh.

9 So, it can be coming in from a
10 different part of the chip, a different mesh,
11 or different wires.

12 There is -- I'm not understanding
13 exactly what the basis or what assumptions
14 you are making from that perspective.

15 BY MR. WILSON:

16 Q. Okay. But, I think you are agreeing
17 with me, correct me if I'm wrong, that when I
18 look at, for example, the sleep transistor above
19 macro B in Figure 1B, and it is on the left, the
20 one highlighted in red in your Paragraph 142
21 there, right? The one that actually has the word
22 "sleep transistor" next to it.

1 Do you see that?

2 A. I see that. And there is nothing in
3 Jiang that says either of those transistors are
4 operated independently. They are operated
5 together.

6 Q. Okay. So, based on your
7 understanding of Jiang, if that sleep transistor
8 is gated off, if it is turned off, there is no
9 power in the local power mesh directly underneath
10 that sleep transistor which is directly above
11 macro B. Correct?

12 MS. WEISKOPF: Object to form.

13 THE WITNESS: I disagree with that
14 set of assumptions. There is no discussion
15 of the location of the sleep transistors.

16 And you are also talking about
17 turning off just that one sleep transistor
18 which is not disclosed in Jiang.

19 There is no independent control
20 disclosed in Jiang of either of the sleep
21 transistors.

22 And there is no suggestion -- I mean

1 the way that it is drawn, it is drawn
2 incorrectly.

3 These sleep transistors would be in
4 the silicon. And it doesn't have to be in a
5 particular location, whether it is within
6 macro B or C.

7 BY MR. WILSON:

8 Q. Okay.

9 A. There is no discussion in Jiang at
10 all in that regard.

11 As a matter of fact, Jiang is
12 nothing but an analysis of the cost and benefit
13 of adding these sleep transistors.

14 Q. Okay.

15 A. Not about lay out, not about
16 routing, not about how to do it. It is silent on
17 all of that.

18 Q. Okay. So, let me ask the question,
19 assuming your interpretation of Jiang.

20 So, let's assume that both sleep
21 transistors in Figure 1B are turned off. Let's
22 assume they are located in the silicon in the

1 substrate down at the same level as the macros in
2 Figure 1B.

3 You would agree with me that when
4 those are turned off, the local power mesh above
5 macros B and C, both of those local power meshes
6 have no power. Correct?

7 A. They would, the portions of those --
8 one sec.

9 Can I have the Jiang reference to
10 look at, please?

11 Q. Sure.

12 MR. WILSON: It is Exhibit 1004.

13 Henry can we propagate that to the Box?

14 (Whereupon, previously marked
15 Exhibit 1004,
16 first referral.)

17 THE VIDEOGRAPHER: Sure, no problem.

18 It is uploaded.

19 THE WITNESS: Okay. One second.

20 So, if the sleep transistors are
21 off, they are not providing the local power
22 meshes for the macros in a way that would

1 allow for any power to be delivered to the
2 respective macros.

3 They would turn the power off. They
4 are power-gated macros.

5 BY MR. WILSON:

6 Q. So, for these sleep transistors to
7 be operable, they cannot receive their signal,
8 their switching signal from the -- their
9 respective macros, correct?

10 MS. WEISKOPF: Object to form.

11 THE WITNESS: They can receive
12 signals from any part of the chip that is
13 powered. This is a chip that does not have
14 different power domains.

15 And there are parts that are -- or
16 there are macros that have power turned off.

17 But there are other parts where
18 there exists power. So it is -- they can
19 receive power from different portions of the
20 chip.

21 BY MR. WILSON:

22 Q. Right. They can receive power,

1 their switch signal -- let me strike that.

2 They can receive a switch signal
3 from parts of the chip that are always powered,
4 but they cannot receive their switch signal from
5 macros that are switched off. Correct?

6 A. I would agree with that.

7 MR. WILSON: Okay. Let's take a
8 look at Li Exhibit 1005.

9 (Whereupon, previously marked
10 Exhibit 1005,
11 first referral.)

12 BY MR. WILSON:

13 Q. And I want to look at Page 494.

14 A. Okay. One second. I will download
15 it. Okay. Okay. I am there.

16 Q. Okay. Figure 3 in Li shows power
17 and ground distribution. Correct?

18 MS. WEISKOPF: Object to form.

19 THE WITNESS: In part. It is
20 showing a part of the chip where power and
21 ground are distributed.

22 BY MR. WILSON:

1 Q. Okay. Now, to be useful in an
2 integrated circuit, the ground supply has to be
3 provided to the substrate. Correct?

4 A. To -- sorry. To be -- say that
5 again, to be useful --

6 Q. To be useful in an integrated
7 circuit, the ground supply has to be provided to
8 the substrate. Correct?

9 A. Well, I mean it depends on the
10 design.

11 If you have a design where the
12 substrate ought to be grounded to provide a
13 reference level for the rest of the chip, you,
14 you would connect it to some reference voltage
15 that you would, you know, call a substrate
16 ground.

17 In this case -- there can be many
18 grounds in a chip, just as the case is in Li, and
19 they are not all substrate ground. Different
20 grounds are isolated from each other.

21 But there is a substrate ground and
22 that would be -- yeah, you would connect a

1 substrate ground to that.

2 Q. Okay. So, in -- well, let me back
3 up.

4 In an integrated circuit for you to
5 have for the circuitry in the substrate to
6 complete a circuit, you must supply a ground to
7 the substrate. Correct?

8 A. Well, no -- okay. The terminology
9 here is really important because in Li there is a
10 distinction made between substrate and core,
11 right? And the reason I say that is because
12 there is a disclosure in Li of something known as
13 the substrate ground versus a core ground.

14 And so, even though the core itself
15 is built in a triple well within the substrate,
16 the substrate ground is different from the core
17 ground.

18 They are electrically isolated from
19 each other. And so I just wanted to be clear
20 about that terminology.

21 Q. Okay. Li discloses a common ground.
22 Correct?

1 A. Can you show me where -- okay.

2 Q. Yeah, take a look at the previous
3 page.

4 A. Okay.

5 Q. The middle paragraph that begins,
6 "Due to the trend."

7 And the second sentence in that
8 paragraph says, "Power and ground are supplied to
9 the package through two VDD inputs (VDD switch
10 and VDD chip) and one ground input,
11 respectively."

12 Do you see that?

13 A. I see that, yes.

14 Q. Li uses a common ground. Correct?

15 MS. WEISKOPF: Object to form.

16 THE WITNESS: Well, this
17 particular -- let's see here. All right.
18 So, in paragraph -- or in Section 4.2, which
19 appears on Page 495 of Li, under the heading
20 of Multiple Power Supplies Implementation, it
21 does say that, "The ground reference GND," so
22 this is pointing to a specific ground, "is

1 common for all the power supplies."

2 So -- and that is the one that you
3 were referring to in that prior page, because
4 it was GND.

5 And so that is a common ground for
6 all of the power supplies.

7 BY MR. WILSON:

8 Q. Okay. So, Li uses a common ground,
9 correct?

10 A. For all of the power supplies, yes,
11 but that doesn't mean that it is the same ground
12 for core ground or for substrate ground.

13 Q. Okay. That common ground, GND, must
14 be provided to the substrate for the chip to
15 function, correct?

16 A. Are you asking me if the common
17 ground that is discussed in 4.2 is the same as
18 substrate ground?

19 Q. No, I'm not asking you that.

20 A. Okay.

21 Q. I'm asking you whether the common
22 ground, GND, must be provided to the circuitry in

1 the substrate, in some form, in some way, for the
2 chip to function?

3 A. Yeah, I, I --

4 MS. WEISKOPF: Object to form.

5 THE WITNESS: I'm not sure where
6 you, where it says that.

7 It discusses different grounds and
8 it discusses a substrate ground. It
9 discusses a core grounds for the various
10 cores. Not sure --

11 If your question is, is this common
12 ground equal to the substrate ground, it
13 could be.

14 But, that is -- but I understand
15 that that is not your question.

16 BY MR. WILSON:

17 Q. Yes.

18 A. So, I'm not sure how to answer that
19 question. So, I don't know how to answer your
20 question, because must it be? Well, it depends.
21 I mean the reference talks about different
22 grounds, so I'm not really sure which ground you

1 are asking about.

2 Q. Okay. So, the -- yeah, my question
3 is, you have to connect the common ground to the
4 circuitry in the substrate in some form or
5 fashion or the circuitry will not function.

6 Correct?

7 A. No, I disagree with that.

8 Q. Okay.

9 A. Because we already know that the
10 core grounds have their own core ground and they
11 can work just fine based on that core ground.

12 Because all you need, as we
13 discussed earlier, to have a circuit that
14 actually functions you need a circuit, a closed
15 loop with a potential difference and some
16 reference.

17 Now, that could be a circuit that is
18 isolated in that triple well in that core where
19 it uses the core ground as a reference. And the
20 core ground is separate from a substrate ground.

21 So, I don't agree that you must
22 bring in something. I mean, it is -- that is

1 not, that is not how the Li reference discusses
2 or teaches --

3 Q. Okay.

4 A. -- about grounds.

5 Q. What you just said is that in the
6 substrate you can have different ground
7 references.

8 For example, a core ground that is
9 not the common ground, GND, correct?

10 MS. WEISKOPF: Object to form.

11 THE WITNESS: Again, you are saying
12 that it is -- you are technically -- the
13 triple well where the core is constructed,
14 all of the cores are constructed is
15 technically in the substrate physically.

16 But there is no substrate ground in
17 those cores. It is a core ground.

18 BY MR. WILSON:

19 Q. Yes. So -- but again you are
20 answering a different question than I'm asking.

21 The -- let's talk about the
22 substrate ground. Okay. What do you understand

1 the --

2 A. Substrate.

3 Q. What do you understand supplies the
4 substrate ground, GND, in Figure 4 of Li?

5 MS. WEISKOPF: Object to form.

6 THE WITNESS: So, the -- so the
7 disclosure is not really clear. It talks
8 about ground, GND. Then in Figure 4 it talks
9 about substrate ground.

10 And then in Figure 2, it talks about
11 GND1 and GND2.

12 Now, you know, is it possible that
13 GND1 is the same as the substrate ground?
14 Yeah, I could see that. But that is
15 different from Ground 2 that is shown in
16 Figure 2, because Ground 2 is the ground that
17 is in the triple well.

18 So, that person of ordinary skill
19 would understand is most likely a core
20 ground.

21 And, now to your question is, could
22 the ground, the GND, be the same as GND1 and

1 substrate ground? It could.

2 But again there are a number of
3 grounds here that are being discussed. I'm
4 not agreeing that there has to be a specific
5 way of connecting or assigning a particular
6 ground.

7 BY MR. WILSON:

8 Q. Okay. Let's take a look at
9 Page 495.

10 A. Okay.

11 Q. Section 4.2, the section you
12 referenced earlier, about four lines up from the
13 bottom of the paragraph.

14 Do you see the sentence that begins,
15 "The different internal ground net"?

16 A. Yes.

17 Q. It says, "The different internal
18 ground net for each core is separated from chip
19 ground by an NMOS switch."

20 What do you understand a chip ground
21 to be?

22 A. I understand that to be basically in

1 reference to Figure 4.

2 So, where it is basically saying
3 that the internal grounds of -- for each core, so
4 that is, that is -- I understand that or a person
5 of ordinary skill would understand that to be the
6 core ground as shown in Figure 4 that is inside
7 the core.

8 And, when it is talking about the
9 chip ground, because it says that the core ground
10 is separated from the chip ground by an NMOS
11 switch.

12 Again, going back to Figure 4, here
13 is the NMOS switch that is identified in that
14 dashed box called Power Switch. And to the left
15 of that is substrate ground.

16 Again, a person of ordinary skill
17 would understand that it is most likely referring
18 to the chip ground as the substrate ground and
19 vice versa.

20 But it is the switch that has the
21 ability to equate the potentials of those two
22 grounds. And so the way that that would work,

1 remember that the power switch is, it has got --
2 it is in its own different location or block.

3 And it would be connected to
4 substrate ground on the drains -- on the source
5 side. On the drains side it would be connected
6 to the core ground.

7 And then the ability to turn that
8 switch on and off through the enable, enable
9 signal for the gate to result in turning on or
10 turning off that switch.

11 Q. Okay. Whether there is a substrate
12 ground in a chip design like Li says nothing
13 about how the ground connection got to the
14 substrate, correct?

15 MS. WEISKOPF: Object to form.

16 THE WITNESS: Well, I think Li talks
17 about, it talks about -- give me just one
18 sec.

19 I mean, for example, on Page 493,
20 let's see, the bottom of the second full
21 paragraph or the first full paragraph,
22 rather, it says, "At the final stage of the

1 layout design an in-house automated procedure
2 is applied, connecting local logic to the top
3 level power grid to implement a complete full
4 chip power distribution network."

5 So, the teaching in the disclosure
6 here is that you have connectivity from the
7 top level power grid down to the silicate.

8 BY MR. WILSON:

9 Q. Okay.

10 A. Through, presumably, you know, a
11 vertical stack of vias.

12 Q. Okay. Let's take a look at Jiang
13 for a second. We will look at Jiang, Figure 2.

14 A. Okay. I am there.

15 Q. Okay. So, Jiang, Figure 2, you
16 opine that that figure shows a substrate ground.
17 Correct?

18 MS. WEISKOPF: Object to form.

19 THE WITNESS: One sec. One second.
20 I'm trying to find it in my declaration.

21 BY MR. WILSON:

22 Q. Paragraph 179.

1 A. Oh, thank you. Yes. That is
2 correct.

3 Q. Okay.

4 A. Yes, and I identify it in the
5 following page, top of Page 68, where I highlight
6 where the substrate grounds are located in
7 Figure 2.

8 Q. Okay. But the fact that there is a
9 substrate ground as shown in Figure 2, does not
10 describe how the ground gets to the substrate.
11 Correct?

12 A. Well, what it does show is that I
13 agree that there are -- there can be many
14 different ways of providing a substrate ground.
15 The way that Jiang discloses it is
16 that it is not coming in from that L1 layer
17 because L1 does not have ground.

18 So, you know, there are different
19 ways in the semiconductor industry that we can
20 provide substrate grounds. I have discussed
21 earlier different type of packaging that have
22 lead frames that could provide ground to the

1 substrate directly.

2 Or there can be rails that provide
3 ground through direct via stacks, all of the way
4 down to the substrate.

5 There are a number of ways of doing
6 it.

7 Q. Okay. And one way of doing is to
8 provide ground through the global power mesh, the
9 upper metal layers, correct?

10 MS. WEISKOPF: Object to form.

11 THE WITNESS: That is not disclosed
12 in Jiang.

13 BY MR. WILSON:

14 Q. But there is a way to provide ground
15 to the substrate that a person of ordinary skill
16 in the art would have known about before
17 November 2007, correct?

18 MS. WEISKOPF: Object to form.

19 THE WITNESS: That is just not
20 disclosed in Jiang. That is not what is --
21 what is shown in Jiang instead is a, the
22 grounding of the substrate directly as shown

1 in Figure 2.

2 BY MR. WILSON:

3 Q. Okay. A person of ordinary skill in
4 the art, before November 2007, would have known
5 that you can provide ground through a global
6 power mesh at the top metal layers of an
7 integrated circuit to the substrate to provide a
8 substrate ground. Correct?

9 MS. WEISKOPF: Object to form.

10 THE WITNESS: You could if that is
11 what Jiang discloses.

12 But, it doesn't. As a matter of
13 fact, the only thing it discloses in L1 is a
14 network of VDD, a single power supply, a
15 single voltage of VDD.

16 There is no disclosure of ground
17 here whatsoever in the L1 layer or level.
18 Nor even in anything intermediate.

19 BY MR. WILSON:

20 Q. Okay.

21 A. What is shown instead is a substrate
22 ground. And as I have discussed earlier, there

1 are other ways that a person of ordinary skill
2 would understand in supplying that ground to the
3 substrate.

4 MR. WILSON: Okay. I'm going to
5 object to your answer as nonresponsive and
6 move to strike it.

7 BY MR. WILSON:

8 Q. A person of ordinary skill in the
9 art, before November 2007, knew that one way to
10 supply a substrate ground was through a global
11 power mesh at the uppermost metal layers in an
12 integrated circuit. Correct?

13 MS. WEISKOPF: Object to form.

14 THE WITNESS: Well, like I answered
15 in my exact last response is generally, yes.
16 But not as disclosed in Jiang because it is
17 missing that teaching. There is no ground in
18 the upper metal layers or any of the metal
19 layers as disclosed in Jiang.

20 Instead, it actually discloses
21 explicitly a substrate ground, and I have
22 already discussed various ways of doing that.

1 BY MR. WILSON:

2 Q. Okay. Let's look at Paragraph 203
3 of your declaration.

4 A. Yes.

5 Q. Okay. Here I want to focus on -- so
6 take a minute and review the paragraph and then I
7 want to focus on the next to the last sentence.

8 A. Okay. Yes, I have read it.

9 Q. Okay. Now, you opine that
10 Dr. Subramanian also seems to, "assume that the
11 statement in the patent means that there could be
12 no automation in the context of a multi-power
13 domain chip which is incorrect."

14 Did I read that correctly?

15 A. That is correct.

16 Q. Okay. What automation in the
17 context of a multi-power domain chip was
18 available?

19 MS. WEISKOPF: Object to form.

20 THE WITNESS: The process of
21 designing an integrated circuit is a very
22 complex process that involves many different

1 steps that go or start from creating a, for
2 example, a circuit schematic, translating
3 that schematic into various hardware
4 languages of different types, things that can
5 be synthesized, and providing net lists, and
6 then converting net lists into layouts.

7 And then from the layout, apply
8 routing of interconnects and creating -- and
9 that itself is an iterative process to meet
10 certain timing requirements and other
11 performance requirements.

12 So, it is a fair amount of trial and
13 error that is involved before generating
14 eventually a mask or what we call a tape out
15 that enables a foundry or a fabrication
16 facility to actually fabricate the chip.

17 So, it is a very involved process.
18 And yeah, there are parts of that that are
19 automated, but not in the way that
20 automatic -- or automated placement and
21 routing tools are for multiple power domains.

22 There can be other parts of it that

1 were known, or early on that were worked on,
2 for example, to create these type of hardware
3 language descriptions or net lists or
4 synthesizing what can be added to a net list,
5 for example.

6 But, he -- Dr. Subramanian has not
7 identified any reference of a well-known
8 automated place and route tool for multiple
9 power domain chips, at least.

10 BY MR. WILSON:

11 Q. Okay. And you are familiar with the
12 term "automatic placement and routing," or APR,
13 correct?

14 A. That's correct.

15 Q. Have you ever used an APR tool?

16 A. Sure, yes, I have.

17 Q. What did you use the APR tool for?

18 A. Well, you know, I -- I have --

19 My experience with place and route
20 goes back to the mid-'90's, even before, the
21 early '90's where we started off using Silvaco
22 tools to perform a place and route or automated

1 placement and route.

2 And I have used -- I have used it to
3 create integrated circuits that include, starting
4 from very early days of power circuits. These
5 were integrated circuits that were capable of
6 handling high voltage applications such as power
7 devices.

8 I have also used it to investigate
9 chips working with my, as part of my work at
10 Exponent, doing failure analysis to understand
11 ways to optimize place and route, identifying
12 root-cause analysis of failed chips.

13 I have used Cadence tools. I have
14 used Synopsis tools as well over time.

15 So, there is a variety of different
16 integrated circuits including memory and flash
17 memory chips and nonvolatile memory chips.

18 So, there are a number of
19 applications that I have used them for, in actual
20 products, manufactured, fabricated products and
21 marketed products.

22 Q. Okay. When was the last time you

1 used an automatic placement and routing tool?

2 A. Well, look, I mean, I have been
3 working at Exponent for more than 20 years now.
4 So, I have consulted with industry over the
5 years.

6 Last time I have used it was -- you
7 know, I have used Cadence tools over the last,
8 over the last year.

9 Q. Okay. Have you ever used an
10 automatic placement and routing tool for a
11 multi-power domain integrated circuit?

12 A. I have not specifically used it for
13 multiple power domain circuits.

14 There -- yeah, I have not used it
15 specifically for that purpose.

16 Some of the chips that I have looked
17 at, investigated, inspected and helped with did
18 have multiple power domains, but that wasn't
19 specifically the task that I was focused on.

20 Q. Okay. Before November 2007, a
21 person of ordinary skill in the art would have
22 known about the use of APR tools. Correct?

1 A. Generally, APR tools, yes. I mean,
2 that is, that is not, that is not -- APR tools in
3 and of themselves are well known, of course.

4 But, not in the way that is required
5 for each step of the claims in the '218 --
6 relevant claims in the '218.

7 Q. Okay. And a person of ordinary
8 skill in the art before November 2007 would have
9 known that an APR tool would allow for automatic
10 placement and routing of a power routing
11 structure in an integrated circuit. Correct?

12 MS. WEISKOPF: Object to form.

13 THE WITNESS: Your, your -- are you
14 referring -- what kind of circuit are you
15 talking about?

16 BY MR. WILSON:

17 Q. Any kind.

18 A. Well, I mean you could -- I mean APR
19 tools can be used, but we know from the '218 that
20 at the time of the invention or before the
21 invention, the APR tools that were used required
22 manual intervention and input, in order to handle

1 the additional level of complexity, as a result
2 of having multiple power domains in those
3 circuits -- in those integrated circuits.

4 Q. Okay. So when you say manual
5 intervention, is it the case that if you must
6 engage in some manual intervention when using an
7 APR tool that you are not using an APR tool to,
8 to design the power routing structure?

9 MS. WEISKOPF: Object to form.

10 THE WITNESS: I'm not sure I
11 understood that question.

12 BY MR. WILSON:

13 Q. Well, you have referred to a manual
14 intervention in the use of APR tools.

15 And I'm trying to figure out what
16 you understand the scope of use of APR tools to
17 be.

18 So, let's take a look, for example,
19 at Claim 1 of the '218 patent.

20 A. Okay.

21 Q. And the first limitation there says,
22 "Forming a first partial local power mesh

1 according to the position of a first power domain
2 of the integrated circuit by an automatic
3 placement and routing tool."

4 Do you see that?

5 A. I do.

6 Q. Okay. If you must engage in some
7 manual intervention during the use of an
8 automatic placement and routing tool to form a
9 first partial local power mesh, are you outside
10 that limitation?

11 MS. WEISKOPF: Object to form.

12 THE WITNESS: Well, you know, again,
13 I think that the way that I have read these
14 claims is the totality of the claims, right.

15 It is not just looking at each
16 limitation in isolation of the other
17 limitations in the claim.

18 It is looking at the entire set of
19 requirements. So, is a requirement of
20 forming the first partial local power mesh,
21 according, according to the position of the
22 first power domain of the IC by an APR tool.

1 Then doing the same -- not then
2 meaning that there is a particular order, but
3 rather that there is a second requirement,
4 which is doing the same for the second
5 partial local power mesh using the APR tool.

6 And then there are -- and those
7 requirements continue.

8 So, there are a set of requirements
9 throughout the entire claim that clearly show
10 the need for a design using the APR tool for
11 multiple power domain chips.

12 So, this is not about just looking
13 at each limitation in isolation. So, it is a
14 requirement that the APR tool would be used
15 for multiple power domain, power routing chip
16 design.

17 BY MR. WILSON:

18 Q. I understand. I'm just trying to
19 figure out whether you understand each of the
20 limitations of Claim 1 to require the use of an
21 APR tool without any manual intervention?

22 MS. WEISKOPF: Object to form.

1 THE WITNESS: Well, look, the manual
2 intervention that I discuss, I discuss in my
3 declaration.

4 And, for example, in Paragraph 60,
5 where I talk about how the APR tools were
6 limited in their capabilities for automating
7 route and placement of multiple power domain
8 chips.

9 Now, I'm not saying that there can't
10 be any manual operation of the APR tools. At
11 the end of the day, I need an engineer who
12 sits there and instructs the APR tool of what
13 to do.

14 But there are important portions of
15 the power routing structure that have to be
16 input manually is what I say for the chips
17 that required multiple voltages.

18 So, that is the distinction here
19 that I'm drawing. Not that any manual
20 intervention would, therefore, mean that it
21 is outside the scope of the claims.

22 It is specific to the ability, the

1 capability of automating place and route for
2 multiple power domain chips.

3 BY MR. WILSON:

4 Q. Okay. A person of ordinary skill in
5 the art before November 2007 would have known
6 that an APR tool could be used to form a power
7 routing structure that used sleep transistors,
8 correct?

9 MS. WEISKOPF: Object to form.

10 THE WITNESS: For sleep transistors,
11 yeah, for single power domain at least,
12 right.

13 So, for single -- for example, for
14 single power supply chips, yeah, I mean that
15 is, that was fairly standard.

16 BY MR. WILSON:

17 Q. Okay. Are you --

18 A. But not when you introduce multiple
19 voltages or multiple power domains.

20 Q. Okay. Are you familiar with SKILL
21 programs?

22 A. Yeah, yeah. SKILL is a known

1 language that is used typically with Cadence
2 systems for APR tools.

3 Q. Okay. And SKILL is a scripting
4 language. Correct?

5 A. That's correct. Yes.

6 Q. Okay. And a person of ordinary
7 skill in the art before November 2007 would have
8 known that a custom SKILL program could be used
9 to automatically generate a power routing
10 structure. Correct?

11 MS. WEISKOPF: Object to form.

12 THE WITNESS: Well, the SKILL
13 program can be used to indicate certain
14 constraints that are imposed on the, on the
15 chip or on the design of the chip in terms
16 of, for example, you know, dimensions of
17 wires or resistances or connectivities.

18 So, I have not -- your question was
19 that it would be programmed to automate. I
20 mean, the point of the APR tool is to
21 automate. The question is what is it
22 automating.

1 BY MR. WILSON:

2 Q. So, yes, my question is, can it be
3 used to automate?

4 A. Well, it is part of -- it is used as
5 part of an APR.

6 So, but, in and of itself is, it --
7 SKILL in and of itself without an APR tool is not
8 going to do very much.

9 Q. Well, but it was known before
10 November 2007 that SKILL is used with Cadence.
11 Correct?

12 A. That is correct.

13 Q. And, together they constitute an APR
14 tool. Correct?

15 MS. WEISKOPF: Object to form.

16 THE WITNESS: It is a capability
17 that Cadence has. But, it is not, it is not
18 there to program in an automated fashion
19 multi-powered domain place and route.

20 BY MR. WILSON:

21 Q. Okay. But, would you agree that a
22 SKILL when used with Cadence could automate the

1 generation of a power distribution network for a
2 single power domain, correct?

3 A. Well, again, your question is that
4 SKILL would do that.

5 It is SKILL as an input, providing
6 an input of constraints to the APR tool, that
7 allows the APR tool to perform the automation in
8 a manner that meets the constraints that are
9 built in or customized into the SKILL script.

10 Q. Okay. Now I think you misunderstood
11 my question.

12 My question is SKILL, in conjunction
13 with Cadence, can be used to design a power
14 distribution network for a single power domain,
15 correct?

16 A. It can.

17 Q. Okay. And, in fact, SKILL in
18 conjunction with Cadence can be used to form a
19 routing structure with two different local power
20 grids on lower metal layers for two different
21 areas of a chip. Correct?

22 MS. WEISKOPF: Object to form.

1 THE WITNESS: I'm not sure I
2 understand that question.

3 What are you referring to exactly?

4 MR. WILSON: Well, let's take a look
5 at Exhibit 1013, which is Bertolet.

6 (Whereupon, previously marked
7 Exhibit 1013,
8 first referral.)

9 BY MR. WILSON:

10 Q. And let's look at page, PDF Page 4,
11 Page 126.

12 A. One second.

13 Q. And right-hand column, under Power
14 Routing, just read that first paragraph.

15 A. I'm sorry. It just downloaded for
16 me. Where are you?

17 Q. Page 126. PDF Page 4.

18 A. Okay. All right, I'm there.

19 Q. Yes. Right-hand column, under Power
20 Routing, that first paragraph.

21 A. Okay, yes. I see that.

22 Q. Okay. So, it says, "A power

1 distribution network is algorithmically generated
2 using a custom SKILL program." First sentence,
3 correct?

4 A. Yes.

5 Q. And middle of the paragraph, it
6 says, "For example, two areas of the chip may
7 have completely unique grids on all layers. Two
8 other areas of the chip may share a common power
9 grid on metal levels one and two, yet have a
10 different power grids on metal levels three
11 through five." Correct?

12 A. Yes.

13 Q. So this is Bertolet disclosing the
14 generation of different local power meshes using
15 a custom SKILL program. Correct?

16 A. No, I disagree. It actually is
17 explicit here what it does teach. It says, "The
18 algorithm provides the capability to define
19 multiple power terrains by area and level of
20 metal."

21 And I talk about power terrains, as
22 Bertolet explains, in my declaration.

1 Q. Okay. I'm -- so, I didn't even
2 refer to that sentence.

3 The next sentence after the one you
4 referred to says, "For example, two areas of the
5 chip may have completely unique grids on all
6 layers. Two other areas of the chip may share a
7 common power grid on metal levels one and two,
8 yet have different power grids on metal levels
9 three through five."

10 So, you would agree that Bertolet
11 discloses the use of SKILL to algorithmically
12 generate unique local power grids, correct?

13 MS. WEISKOPF: Object to form.

14 THE WITNESS: Well, it -- again, by
15 describing them as power terrains. And this
16 is all in the context of a single power
17 domain chip anyway.

18 So, there is nothing here that
19 suggests that Bertolet has the capability of
20 creating or defining grids on any layers for
21 multiple-power domain chips.

22 As a matter of fact, Bertolet I

1 think is what, a 1997 reference, way before
2 multi-power domain chips were, were able to
3 be routed in any APR tools.

4 So, it is not something that I think
5 was even contemplated by Bertolet.

6 BY MR. WILSON:

7 Q. Okay. My question absolutely said
8 nothing about multi-power domain chips.

9 My question is, whether or not
10 Bertolet discloses using a custom SKILL program
11 to algorithmically generate unique power grids on
12 multiple different metal layers?

13 MS. WEISKOPF: Object to form.

14 THE WITNESS: As it discloses here,
15 I'm just providing the context of what
16 Bertolet is directed to.

17 So, it cannot be read to apply to
18 multi-power domain chips. That is all I'm
19 saying.

20 BY MR. WILSON:

21 Q. So, is the answer to my question
22 yes?

1 A. To single power domain chips, yes.

2 Q. Okay. Okay. Now let's take a look
3 at the '218 patent.

4 THE WITNESS: Is this a good time to
5 just take a break?

6 MR. WILSON: Oh, sure. Sorry.

7 THE VIDEOGRAPHER: Okay, the time is
8 2:10 p.m. Off the record.

9 (Recess taken -- 2:10 p.m.)

10 (After recess -- 2:18 p.m.)

11 THE VIDEOGRAPHER: The time
12 is 2:18 p.m. Back on the record.

13 BY MR. WILSON:

14 Q. Okay. Dr. Sourì, let's look at
15 the '218 patent. I want to look at Column 5.
16 And down at the bottom, this paragraph begins at
17 Line 54.

18 A. Yes.

19 Q. But I want to start at Line 59. And
20 you see at Line 59 it says, "Thus the following
21 will describe a simple algorithm for the APR
22 tool."

1 Do you see that?

2 A. Yes. I do.

3 Q. Okay. So, the '218 patent here
4 describes an algorithm for an APR tool. And in
5 Line 60, it says, "Firstly, the local power
6 mesh 300 is evenly distributed on top of the
7 entire chip circuitry."

8 Then, "The partial local power
9 meshes in the local power mesh 300 corresponding
10 to the power domains 110, 120 are defined such as
11 partitioning the local power mesh 300 based on
12 the positions of the power domains 110, 120 so
13 that the plurality of partitioned power meshes
14 are not electrically coupled to each other to
15 form the above mentioned partial local power
16 meshes, 310, 320."

17 Did I read that correctly?

18 A. Yes.

19 Q. Okay. So, for this algorithm, it
20 describes allocating a local power mesh 300 -- or
21 I'm sorry. Let me strike that.

22 So, for the first step in this

1 algorithm it describes defining a partial local
2 power mesh to, to be evenly distributed across
3 the circuitry of the chip and then partitioning
4 that local power mesh based on the positions of
5 the power domains into partial local power
6 meshes. Correct?

7 MS. WEISKOPF: Object to form.

8 THE WITNESS: I think you started
9 off saying that the first step was defining a
10 partial local power mesh.

11 If you meant that, I disagree.

12 BY MR. WILSON:

13 Q. Okay. Yes. Sorry. Let me try
14 again then.

15 The first step is defining a local
16 power mesh, evenly distributing that local power
17 mesh on top of the entire chip circuitry and then
18 partitioning it, based on the position of the
19 underlying power domains to form partitioned
20 partial local power meshes, correct?

21 MS. WEISKOPF: Object to form.

22 THE WITNESS: Yeah, so, you know,

1 you are using the term "partitioning." The
2 paragraph does include the word
3 "partitioning" but it uses it as an example.

4 It really does say defined, right?

5 So, it is defining the partial local
6 power meshes to form the -- you know, for
7 defining them, for example, such as
8 partitioning them based on the positions of
9 the power domains 110 and 120.

10 But in a way, of course, that the
11 partitioned partial local power meshes are
12 not electrically coupled to each other.

13 So, with that caveat, it really is
14 about definition, and the partitioning is
15 just used as an example.

16 BY MR. WILSON:

17 Q. Okay. All right. So, continuing on
18 top of Column 5 there, it says "On the other
19 hand, the approach to form the global power mesh
20 400 is much easier for the APR tool by just
21 evenly distributing the global power mesh 400 on
22 metal layers that are positioned higher."

1 Correct?

2 A. Yeah, again, I think you said on top
3 of Column 5. I think you meant Column 6, in
4 which case I agree.

5 Q. Oh, sorry. Okay.

6 So, essentially we have a two-step
7 algorithm, which first is defining a local power
8 mesh which is defined or partitioned into partial
9 local power meshes and then defining a global
10 power mesh. Correct?

11 MS. WEISKOPF: Object to form.

12 THE WITNESS: Well, I mean there
13 are -- the algorithm is encompassing of
14 defining local power mesh, partial local
15 power meshes, and global power meshes.

16 I disagree with the way that, the
17 implication of your question to suggest that
18 there is some kind of an order in saying that
19 it is a two-step process of one then followed
20 by another.

21 So, there is no indication or
22 implication that there necessarily is that

1 kind of an order.

2 There are a number of things that
3 the algorithm describes doing but not
4 necessarily in a specific order.

5 BY MR. WILSON:

6 Q. Okay. Okay. But you would agree
7 that this passage from Column 5, Line 60 through
8 Column 6, Line 4 describes an algorithm for an
9 APR tool, according to the '218 patent. Correct?

10 MS. WEISKOPF: Object to form.

11 THE WITNESS: It describes a simple
12 algorithm for an APR tool.

13 BY MR. WILSON:

14 Q. Okay. And it describes a simple
15 algorithm for an APR tool for multiple-power
16 domains. Correct?

17 MS. WEISKOPF: Object to form.

18 THE WITNESS: One second. This is
19 an algorithm that is specific to
20 multiple-power domains, as described in
21 the '218.

22 BY MR. WILSON:

1 Q. Okay. Now let's take a look at Li,
2 Exhibit 1005.

3 A. Okay.

4 Q. Okay. Now, Li describes the BCM1280
5 chip. Correct?

6 A. That is correct.

7 Q. You are familiar with Broadcom.
8 Correct?

9 A. Yes.

10 Q. Have you ever heard of the BCM1280
11 chip before this case?

12 A. Before this case, I may have.

13 Q. Okay. Do you know if it was a
14 commercially available chip?

15 MS. WEISKOPF: Object to form.

16 THE WITNESS: I, I have not -- I
17 don't recall --

18 BY MR. WILSON:

19 Q. Okay.

20 A. -- at this time.

21 Q. So, let's look at the first page of
22 Li. And looking at the abstract at the

1 beginning, about --

2 A. Yes.

3 Q. -- four lines from the bottom of the
4 first paragraph. On the right-hand side, you see
5 where it starts, "The first"?

6 A. Yes.

7 Q. Okay. It says, "The first phase
8 involves verifying LVS at the block level as well
9 as the full chip level." Correct?

10 A. That is what it says, yes.

11 Q. Okay. What does block level mean in
12 Li?

13 A. Well, I mean, you know, blocks --
14 so, when it is talking about block level, it is
15 really talking about at the level of logic
16 blocks.

17 It doesn't really provide any
18 further elaboration on it. It may later on. I
19 would have to double-check.

20 But, typically, a person of ordinary
21 skill would understand it to be at a level of
22 basically logic, logic blocks.

1 Q. Okay. And a logic block is a
2 portion of the circuitry --

3 A. Sometimes, sometimes we are refer to
4 it as IP blocks or intellectual property blocks
5 that you can purchase, acquire, and insert on
6 your chip to perform certain functions.

7 Q. It is a logical unit or entity
8 within the circuitry of the chip, correct?

9 MS. WEISKOPF: Object to form.

10 THE WITNESS: It can be. It doesn't
11 have to be in a specific physical defined
12 unique way, but it can be.

13 BY MR. WILSON:

14 Q. Okay. Let's look at Page 493 in Li.

15 A. Yes.

16 Q. Okay. Looking at the first full
17 paragraph on the BCM1280. Do you see that?

18 A. I do.

19 Q. Okay. It says, "Metal 6 and Metal 7
20 are extensively used in distributing power and
21 ground across the chip." It says, "Ground (GND)
22 and power (VDD chip, VDD switch) lines are routed

1 alternately on Metal 6 in the vertical direction
2 and Metal 7 in the horizontal direction."

3 Did I read that correctly?

4 A. You did.

5 Q. Okay. So, Li teaches that there are
6 ground and VDD chip and VDD switch wires on
7 Metal 6 and Metal 7. Correct?

8 A. Yes.

9 Q. Okay. Now, it also teaches that
10 there are local power grids on Metal 2 through
11 Metal 5. Correct?

12 MS. WEISKOPF: Object to form.

13 THE WITNESS: Well, it talks
14 about -- it talks about local sections that
15 are gridded on Metals 2 through 5 on which
16 the local power grids are formed at the block
17 level.

18 That is language that Li uses.

19 BY MR. WILSON:

20 Q. Okay. So, but you would agree that
21 the -- that Li discloses local power grids on
22 Metal 2 through Metal 5. Correct?

1 MS. WEISKOPF: Object to form.

2 THE WITNESS: That is not what it
3 says. It just simply says that there are
4 these local sections that are gridded on
5 Metals 2 -- Metal 2 through Metal 5. And on
6 these local sections or -- on which the local
7 power grids are formed on these local
8 sections at the block level, whatever the
9 local sections are.

10 BY MR. WILSON:

11 Q. Okay. So, the local sections are
12 gridded on Metal 2 through Metal 5. Correct?

13 A. Yes.

14 MS. WEISKOPF: Object to form.

15 BY MR. WILSON:

16 Q. And, the local power grids are
17 formed on either the local sections or Metal 2
18 through Metal 5, either one, both of which are
19 Metal 2 through Metal 5. Correct?

20 MS. WEISKOPF: Object to form.

21 THE WITNESS: No. I find that --
22 no, I'm not sure I -- I do not agree with

1 that. I find that confusing.

2 It says, "On which the local power
3 grids are formed at the block level."

4 So, it is talking about the local
5 sections and the local power grids are formed
6 at the block level.

7 BY MR. WILSON:

8 Q. Okay. So, your interpretation of
9 that sentence is the power and ground lines in
10 the local sections are gridded on Metal 2 through
11 Metal 5 and the local power grids are formed on
12 the local sections. Correct?

13 MS. WEISKOPF: Object to form.

14 THE WITNESS: It just says on which
15 local power grids are formed at the block
16 level. That is what it says.

17 BY MR. WILSON:

18 Q. Okay. But your interpretation of
19 that sentence is the local power grids are formed
20 at the block level on the local sections.
21 Correct?

22 MS. WEISKOPF: Object to form.

1 THE WITNESS: They are -- the power
2 and ground lines in the local sections, they
3 are gridded -- the power and ground lines in
4 the local sections are gridded on Metals 2
5 through 5.

6 On which power -- on which the local
7 power grids are formed at the block level.

8 It is not saying anything about the
9 local power grids on Metals 2 through 5. It
10 is talking about the local power grids being
11 formed at the block level.

12 BY MR. WILSON:

13 Q. Well, it says on which the local
14 power grids are formed.

15 What is that referring to? What are
16 the local power grids formed on?

17 A. I disagree with that reading. It
18 says the local power grids are formed at the
19 block level. It is not saying that they are
20 formed in the local sections or gridded on
21 Metals 2 through 5.

22 Q. Okay. Before it says local power

1 grids, it says, "on which," correct?

2 Do you see that language "on which"?

3 A. I see that language.

4 Q. What does "on which" refer back to?

5 A. One second. Okay. So, the local
6 sections are gridded on Metal 2 through Metal 5.
7 There is no disclosure of where these local
8 sections are located or positioned.

9 But it goes on to say that local
10 power grids are formed at the block level, but we
11 don't -- there is no disclosure whatsoever about
12 where the local sections are, nor exactly what or
13 where the block level is and how the local
14 sections relate to the block level.

15 Q. Okay. The sentence reads, "The
16 power and ground lines in the local sections are
17 gridded on Metal 2 through Metal 5, on which,"
18 are you with me that far?

19 A. Yes.

20 Q. What --

21 A. But it is referring to the local
22 sections.

1 Q. On which, in your opinion refers
2 back to the local sections?

3 A. Yes.

4 Q. Correct? Okay.

5 The local sections are gridded on
6 Metal 2 through Metal 5. Correct?

7 A. That is what it says.

8 Q. Okay. So, then the local power
9 grids are also on Metal 2 through Metal 5.
10 Correct?

11 A. No, I disagree. All it says is that
12 the local power grids are formed at the block
13 level.

14 Q. Well, no, that is not all it says.
15 It says, "on which the local power grids are
16 formed," which you said refers back to the local
17 sections. And you also said the local sections
18 are gridded on Metal 2 through Metal 5. Is that
19 correct?

20 MS. WEISKOPF: Object to form.

21 THE WITNESS: Well, correct. But
22 the local power grids are described as being

1 formed at the block level without any
2 indication of where those block -- where that
3 block level is, nor how it is related to the
4 local sections or even the positioning of the
5 local sections.

6 BY MR. WILSON:

7 Q. But it says explicitly, and you just
8 testified that you agree, that the local sections
9 are gridded on Metal 2 through Metal 5.

10 Why doesn't that tell you where they
11 are?

12 MS. WEISKOPF: Object to form.

13 THE WITNESS: It tells you they are
14 gridded on Metals 2 through Metal 5, but it
15 doesn't tell you where on the chip those are.

16 BY MR. WILSON:

17 Q. Okay. So, let's --

18 A. How they are related to the block
19 level or how the block level is related to where
20 on the chip they exist.

21 Q. Okay. So let's talk about two
22 different dimensions. Let's talk about the

1 vertical dimension and the horizontal dimension,
2 okay?

3 Metal 2 through Metal 5 define the
4 vertical dimension on the chip. Correct?

5 A. It -- that can be -- you can see it
6 as a relative vertical dimension, yes.

7 Q. Okay. So, we would agree that the
8 power and ground lines in the local sections
9 exist vertically on Metal 2 through Metal 5.
10 Correct?

11 A. That -- all it is saying is that the
12 local sections are gridded in Metal 2 through
13 Metal 5.

14 But that is not a disclosure of the
15 local power grids being formed on Metals 2
16 through Metal 5.

17 Q. Okay. Well, let's take it one step
18 at a time.

19 It says, "The power and ground lines
20 in the local sections are gridded on Metal 2
21 through Metal 5." Correct?

22 A. That is correct.

1 Q. So, can we agree that the power and
2 ground lines in the local sections vertically are
3 located on Metal 2 through Metal 5?

4 MS. WEISKOPF: Object to form.

5 THE WITNESS: Only in the local
6 sections. So, not necessarily -- it is just
7 saying that the local sections are gridded on
8 Metals 2 through Metal 5.

9 BY MR. WILSON:

10 Q. Well, again, that is the question I
11 asked, but that is not all that it is saying,
12 either.

13 It says, "The power and ground lines
14 in the local sections are gridded on Metal 2
15 through Metal 5."

16 Did I read that correctly?

17 A. You did. So, we are talking about
18 power and ground lines in the local sections.

19 Q. Okay. And so, can we agree that the
20 power and ground lines in the local sections in
21 the vertical dimension are located on Metal 2
22 through Metal 5?

1 MS. WEISKOPF: Object to form.

2 THE WITNESS: That's correct.

3 BY MR. WILSON:

4 Q. Okay. Now the sentence goes on to
5 say, "on which the local power grids are formed."

6 So, let's pause right there.

7 That is a reference to the fact that
8 the local power grids are formed in the vertical
9 dimension on Metal 2 through Metal 5. Correct?

10 A. I disagree.

11 Q. Okay. Why do you disagree?

12 A. Because you didn't finish reading
13 the rest of the sentence. You paused before the
14 end of the sentence.

15 Q. Okay. Didn't --

16 A. Didn't -- the sentence did not stop
17 after the word "formed." It continues to say
18 that the local power grids are formed at the
19 block level. That is when the sentence ends.

20 It is at the block level.

21 Q. Okay. So, what does on which the
22 local power grids are formed, what does "on

1 which" in that phrase modify?

2 A. It is basically telling us that the
3 local power grids, which are formed at the block
4 level, are somehow related to local sections.

5 But, there is no indication of where
6 those are located.

7 Q. But again there is an indication of
8 where they are located. In the vertical
9 dimension, they are located on Metal 2 through
10 Metal 5. Correct?

11 A. Only for local sections.

12 Q. Okay. And not --

13 A. And not -- not the local power grids
14 because the local power grids are formed at the
15 block level.

16 Q. Okay. So, you disagree that when it
17 says on "which the local power grids are formed,"
18 it is referring to the fact that the local power
19 grids are formed in the vertical dimension on
20 Metal 2 through Metal 5. Correct?

21 A. Well, it may be. It is just that
22 the disclosure is not saying it. It is not

1 telling us that the local power grids are formed
2 on Metal 2 through Metal 5.

3 It is saying that the local power
4 grids are formed at the block level.

5 Q. Okay. So, you, you think that may
6 be a proper interpretation of on which the local
7 power grids are formed, correct? Is that they
8 were formed on Metal 2 through Metal 5?

9 A. No. I didn't say that. I said it
10 may be. But, what it actually does say
11 explicitly is that they are formed at the block
12 level.

13 Q. Okay. So, we agreed earlier that
14 block in Li refers to a logic block. Correct?

15 A. Generally speaking, yes. Yes.

16 Q. Okay.

17 A. But there is no indication of, you
18 know, where that block is or how it is
19 distributed on the surface of the silicon. We
20 don't know.

21 Q. Okay. And, so, you would disagree
22 that when it says, "on which the local power

1 grids are formed at the block level," it is
2 referring there to the horizontal dimension of
3 the local power grids, correct?

4 MS. WEISKOPF: Object to form.

5 THE WITNESS: I'm sorry. I'm
6 disagreeing -- I'm disagreeing -- okay,
7 sorry.

8 Can you repeat that question again?

9 BY MR. WILSON:

10 Q. When the phrase says, "on which the
11 local power grids are formed at the block level,"
12 you disagree that at the block level is referring
13 to the horizontal extent of the local power
14 grids, correct?

15 MS. WEISKOPF: Object to form.

16 THE WITNESS: It doesn't say
17 anything about horizontal location of the
18 local power grids.

19 It is just saying on which the local
20 power grids are formed at the block level.

21 BY MR. WILSON:

22 Q. Okay.

1 A. So, there is no disclosure or
2 explanation of where that is on the chip.

3 Q. Okay. So, when it says on which --
4 sorry. Go ahead.

5 A. I just wanted to -- where the extent
6 of that is on the chip.

7 Q. Okay. So when it says, "on which
8 the local power grids are formed at the block
9 level," you don't understand that to specify any
10 location vertically or horizontally of the local
11 power grids. Correct?

12 MS. WEISKOPF: Object to form.

13 THE WITNESS: I am not, I am not
14 seeing it disclosing or teaching local power
15 grids in any specific location other than
16 saying that they are formed at the block
17 level.

18 BY MR. WILSON:

19 Q. Okay. But you, you would agree that
20 the local power grids, wherever they are, have
21 both power and ground wires. Correct?

22 A. It depends on how they are

1 implemented.

2 The disclosure goes on to say that,
3 basically the last sentence of that paragraph, it
4 says, "At the final stage of the layout design,
5 an in-house automated procedure is applied,
6 connecting local logic to the top-level power
7 grid, to implement a complete full-chip power
8 distribution network."

9 So, there is no full disclosure that
10 there is power and ground lines in the
11 intermediate metal layers.

12 Q. Okay. We can agree that there are
13 power and ground lines on Metal 2 through
14 Metal 5. Correct?

15 MS. WEISKOPF: Object to form.

16 THE WITNESS: In the local sections,
17 yes.

18 BY MR. WILSON:

19 Q. Okay. Okay. Now, looking at the
20 next sentence there it says, "The local power
21 grids are left floating until final assembly at
22 the full chip level."

1 Did I read that correctly?

2 A. You did.

3 Q. Okay. What do you understand
4 floating to mean?

5 A. It indicates that there is no
6 electrical connection.

7 Q. Okay.

8 A. So, floating voltages, for instance.

9 Q. Okay. So, the local power grids are
10 left with no electrical connections until final
11 assembly at the full chip level, correct?

12 A. That is what it says.

13 Q. Okay. So, then at final assembly,
14 there would be electrical connections to the
15 local power grids, correct?

16 A. There may be. There is no
17 disclosure of that.

18 Q. Well, the next sentence says, "At
19 the final stage of the layout design an in-house
20 automated procedure is applied, connecting local
21 logic to the top level power grid to implement a
22 complete full chip power distribution network."

1 Right?

2 A. Yes.

3 Q. Okay. That would include the local
4 power grids. Correct?

5 A. Not --

6 MS. WEISKOPF: Object to form.

7 THE WITNESS: Not necessarily. It
8 depends on how the distribution network is
9 designed. And the disclosure here is only
10 talking about connecting the local logic to
11 the top level power grid.

12 BY MR. WILSON:

13 Q. Well, it says in the sentence
14 preceding it, "The local power grids are left
15 floating until final assembly at the full chip
16 level," which is what is referred to in the next
17 sentence. Correct?

18 A. No. The -- when it talks about
19 assembly at the full chip level, so the full chip
20 level is really talking about how the, the chip
21 is assembled.

22 Whereas in the last sentence, it

1 talks about a full chip power distribution
2 network, that is specific to the inside of the
3 chip and how the distribution or the power
4 distribution network is designed.

5 Q. Okay. So, although we have local
6 power grids here explicitly in the design, in
7 your opinion they are not part of the full chip
8 power distribution network. Correct?

9 MS. WEISKOPF: Object to form.

10 THE WITNESS: I am just -- the way
11 that I am understanding the disclosure is
12 that it is talking about connecting the local
13 logic to the top level power grid.

14 To the extent that there are local
15 power grids, it is not for the purpose of
16 connecting local logic to them, as best as I
17 can tell.

18 BY MR. WILSON:

19 Q. Okay. What would they be used for?
20 What would the local power grids be used for?

21 A. There could be other things to
22 connect power that may not be logic, may not be

1 block related. It is, it is silent on that
2 front.

3 Q. Okay.

4 MR. WILSON: Okay. Tell you what.

5 Let's take a ten-minute break. We may be
6 done.

7 THE VIDEOGRAPHER: All right. Stand
8 by. The time is 2:48 p.m. Going off the
9 record.

10 (Recess taken -- 2:48 p.m.)

11 (After recess -- 2:57 p.m.)

12 THE VIDEOGRAPHER: All right. The
13 time is 2:57 p.m. We are back on the record.

14 BY MR. WILSON:

15 Q. Dr. Sourì, during the course of the
16 deposition today, have you at any time had any
17 discussion with anyone about questions, answers,
18 prospective questions or answers or the substance
19 of your testimony?

20 A. No, I have not.

21 MR. WILSON: Okay. I have no
22 further questions.

1 MS. WEISKOPF: Okay. I may have one
2 or two. Let me just have about a 5 or
3 10-minute break. Is that okay, Doug?

4 MR. WILSON: Sure.

5 THE VIDEOGRAPHER: All right. The
6 time is 2:58 p.m. Off the record.

7 (Recess taken -- 2:58 p.m.)

8 (After recess -- 3:08 p.m.)

9 THE VIDEOGRAPHER: The time
10 is 3:08 p.m. We are back on the record.

11 MS. WEISKOPF: Okay. We also have
12 no questions, but we would like to sign --
13 review and sign.

14 MR. WILSON: Okay.

15 THE VIDEOGRAPHER: Okay. This marks
16 the end of today's deposition.

17 The time is 3:08 p.m.

18 (Whereupon, signature not having been waived,
19 the deposition suspended at 3:08 p.m. EDT)

20 * * *

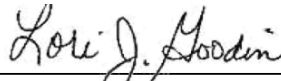
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CERTIFICATE OF NOTARY

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CA CSR # 13959 the Notary for this deposition, do
hereby certify that the witness whose testimony
appears in the foregoing deposition was sworn by
me; that I am neither counsel for, related to,
nor employed by any of the parties to the action
in which this deposition was taken; and, further, that I am
not a relative or employee of any attorney or
counsel employed by the parties hereto, or
financially or otherwise interested in the
outcome of this action.



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STATE OF CALIFORNIA, CA CSR# 13959

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1 Shukri Sourì, Ph.D., c/o
K & L GATES LLP

2 925 Fourth Avenue, Suite 2900
Seattle, Washington 98104

3

4 Case: Advanced Micro Devices, Inc. v. Realtek Semiconductor Corporation
Date of deposition: May 7, 2024

5 Deponent: Shukri Sourì, Ph.D.

6

7 Please be advised that the transcript in the above
8 referenced matter is now complete and ready for signature.
9 The deponent may come to this office to sign the transcript,
10 a copy may be purchased for the witness to review and sign,
11 or the deponent and/or counsel may waive the option of
12 signing. Please advise us of the option selected.

13 Please forward the errata sheet and the original signed
14 signature page to counsel noticing the deposition, noting the
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17 not hesitate to call our office at (202)-232-0646.

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5 Witness Name: Shukri Sourì, Ph.D.

Deposition Date: May 7, 2024

6

7 I do hereby acknowledge that I have read
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9 Witness Name: Shukri Sourì, Ph.D.

10 Deposition Date: May 7, 2024

11 Page No. Line No. Change

12

13

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Signature

Date

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