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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC.,
Petitioner,

v.

REALTEK SEMICONDUCTOR CORPORATION,
Patent Owner.

Case No. IPR2023-00920
U.S. Patent No. 8,006,218

PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE

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Exhibit No.	Description
1001	U.S. Patent No. 8,006,218 (“’218 Patent” or “’218”)
1002	File History for U.S. Patent No. 8,006,218
1003	Declaration of Dr. Vivek Subramanian (“Subramanian Decl.”)
1004	Hailin Jiang et al., <i>Benefits and Costs of Power-Gating Technique</i> , Proceedings of the 2005 International Conference on Computer Design (ICCD 2005) (“Jiang”)
1005	Wei Li et al., <i>LVS Verification across Multiple Power Domains for a Quad-Core Microprocessor</i> , ACM Transactions on Design Automation of Electronic Systems, Vol. 11, No. 2, pp. 490-500, (April 2006) (“Li”)
1006	U.S. Patent No. 7,948,292 (“Chiu”)
1007	Hailin Jiang et al., <i>Power/Ground Supply Network Optimization for Power-Gating</i> , Proceedings of the 2006 International Conference on Computer Design (ICCD 2006) (“Jiang2”)
1008	Hailin Jiang et al., <i>Power-Gating Aware Floorplanning</i> , Proceedings of the 8th International Symposium on Quality Electronic Design (ISQED 2007) (“Jiang3”)
1009	Suhwan Kim et al., <i>Minimizing Inductive Noise in System-On-a-Chip with Multiple Power Gating Structures</i> , ESSCIRC 2004 - 29th European Solid-State Circuits Conference (IEEE Cat. No.03EX705), pp. 635-638 (2003) (“Kim”)
1010	U.S. Patent No. 7,705,486 (“Lee”)
1011	U.S. Patent Application 60/976,181 (“Chiu Provisional”)
1012	Michael Keating et al., <i>Low Power Methodology Manual</i> , Springer (2007) (excerpts) (“LPMM”)
1013	A. Bertolet et al., <i>A Pseudo-Hierarchical Methodology for High Performance Microprocessor Design</i> , Proceedings of the 1997 International Symposium on Physical Design, pp. 124–129 (April 1997) (“Bertolet”)

Exhibit No.	Description
1014	Luca Benini et al., <i>Advanced power management techniques: going beyond intelligent shutdown</i> , Proceedings of the 2003 Asia and South Pacific Design Automation Conference, pp. 385–389 (January 2003) (“Benini”)
1015	Yajun Ran et al., <i>Via-Configurable Routing Architectures and Fast Design Mappability Estimation for Regular Fabrics</i> , IEEE/ACM International Conference on Computer-Aided Design (2005) (“Ran”)
1016	U.S. Patent No. 7,671,623 (“Blisson”)
1017	Screen shot of AMD Innovation Timeline, (available at https://www.amd.com/en/corporate/innovations)
1018	U.S. Patent No. 6,925,627 (“Longway”)
1019	U.S. Patent No. 7,260,805 (“Yan”)
1020	Kimiyoshi Usami et al., <i>Low-power Design Methodology and Applications utilizing Dual Supply Voltages</i> , Proceedings of the ASP-DAC 2000: Asia and South Pacific Design Automation Conference (2000) (“Usami”)
1021	Declaration of Dr. Sylvia Hall-Ellis (“Hall Ellis Decl.”)
1022	Curriculum Vitae of Sylvia Dr. Sylvia Hall-Ellis
1023	Order Granting Motion to Stay, <i>Realtek Semiconductor Corp., v. Advanced Micro Devices, Inc.</i> , Case No. 4:22-cv-04769-JSW, Dkt. 61 (N.D. Cal. Apr. 24, 2023)
1024	U.S. Patent No. 6,903,389 (“Tai”)
1025	Synopsys Press Release, <i>Synopsys Galaxy Platform Reduces Power Consumption of Industry-Leading Multi-Voltage Designs</i> , Jul. 19, 2006 (available at https://news.synopsys.com/index.php?s=20295&item=122684)
1026	Synopsys Press Release Index, July 18, 2006 through July 26, 2006 (available at https://news.synopsys.com/index.php?s=20295&l=10&year=2006&o=50)

Exhibit No.	Description
1027	Synopsys Press Release, <i>New Low Power Methodology Manual Demystifies Advanced Power Management</i> , May 29, 2007 (available at https://news.synopsys.com/index.php?s=20295&item=122821)
1028	Synopsys Press Release Index, May 24, 2007 through May 29, 2007 (available at https://news.synopsys.com/index.php?s=20295&year=2007&o=60)
1029	Complainant’s Proposed Claim Constructions, In the Matter Of Certain Integrated Circuits, Components Thereof, And Products Containing The Same, Investigation No. 337-TA-1350 (May 1, 2023)
1030	Respondent Advanced Micro Devices, Inc.’s Proposed Claim Constructions, In the Matter Of Certain Integrated Circuits, Components Thereof, And Products Containing The Same, Investigation No. 337-TA-1350 (May 2, 2023)
1031	Order No. 25 Denying Complainant Realtek Semiconductor Corp.’s Motion for Summary Determination, In the Matter of Certain Integrated Circuits, Components Thereof, and Products Containing Same, Inv. No. 337-TA-1350 (USITC Sept. 7, 2023) (excerpts)
1032	E-mail from PTAB authorizing submission of ITC Order and limited briefing in IPR2023-00920 (Sept. 14, 2023)
1033	E-mail from PTAB authorizing Petitioner’s motion to submit supplemental information in IPR2023-00920 (Dec. 27, 2023)
1034	Supplemental Declaration of Dr. Vivek Subramanian
1035	Markman Hearing Transcript, <i>In the Matter Of Certain Integrated Circuits, Components Thereof, And Products Containing The Same</i> , Investigation No. 337-TA-1350 (June 5, 2023)
1036	Realtek’s Markman Hearing Demonstratives, <i>In the Matter Of Certain Integrated Circuits, Components Thereof, And Products Containing The Same</i> , Investigation No. 337-TA-1350 (June 5, 2023)

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Exhibit No.	Description
1037	Transcript of May 7, 2024 Deposition of Dr. Shukri Sourì
1038	Reply Declaration of Dr. Vivek Subramanian
1039	Reserved.
1040	Definition of “coupling” IEEE Standard Dictionary 277 (5th ed. 1993)

I. INTRODUCTION

Realtek’s response is a scattershot of unsupported arguments that fail to demonstrate the challenged claims are patentable. The unpersuasive response rests upon untenable, mostly pointless, narrowing claim constructions and failed ITC arguments. Those arguments misrepresent the prior art’s teachings and ignore the Petition’s systematic explanations for why the challenged claims would have been obvious.

II. CLAIM CONSTRUCTION

Realtek’s brief brings to the Board the same construction arguments for “power domain,” “to provide the power needed,” “coupling,” and “at least one first local ground wire” that failed to save the challenged claims in the ITC ALJ’s Initial Determination. POR, 8-26; EX2007-EX2008. But there is no need for the Board to reach these disputes because the claims remain invalid under Realtek’s constructions. *See infra* §§III.A-B, III.D, IV.A-B.

A. “power domain” Terms

The ALJ rejected Realtek’s “power domain” construction, holding that claim 12 “permits the first and second power domains [to have] the same power requirement as one another.” EX2007, 131; *id.*, 102-05. Extrinsic evidence confirms the ALJ’s construction. *See* EX1012, 157 (“A *Power Domain* is a logical entity and is a collection of design elements that share a primary power supply.”);

EX1037, 16:5-17:10, 20:9-16 (Dr. Souri testifying LPMM is consistent with plain and ordinary meaning). Undeterred by this loss and the contrary extrinsic evidence, Realtek asks the Board to hold that the “first” and “second power domain” have different power requirements. POR, 8-11. Its arguments still come up short.

Realtek first incorrectly asserts that Dr. Subramanian agreed with Realtek’s construction. POR, 8-9. But his position was exactly the opposite:

Q Do you agree that the claim requires the power requirements of each power domain to be different?

[Objection]

THE WITNESS: **No**, the claim states what it says.

EX2005, 21:12-17¹; *id.*, 23:3-15 (power requirements of the different power domains can be “the same at all times” if “they’re entirely separated from each other”). Realtek’s lengthy citations expressly contradict its construction. *See* EX2005, 13:17-17:7, 20:17-27:18.

Realtek next points to the two voltage inputs (V_{DD1} , V_{DD2}) in the specification. POR, 10-11. But Realtek ignores that these are “just a preferred example of the invention and should not be construed as any limitation on the implementation of the invention.” EX1001, 6:9-12, 6:51-56; *Superguide v. DirecTV Enters.*, 358 F.3d 870, 875 (Fed. Cir. 2004) (“Specifications teach. Claims claim.” (citation omitted));

¹ All emphasis added unless otherwise noted.

Paper 10 (“ID”), 21 (declining “to limit the claim as urged by Patent Owner”). Nothing in the ’218 *requires* that separate power domains have different voltage levels. Indeed, the ALJ found, and Realtek concedes, the ’218’s power domains can receive “the same” voltage “at some point in time.” POR, 10-11; EX2007, 105; EX1001, 1:18-20. POSITAs would understand that different power domains can all receive the same voltage. *See e.g.*, EX1012, 156-57 (multiple domains same “1.2v” voltage); EX1007, 1-2, Fig. 1 (“circuit [] divided into several power domains” each receiving same “VDD”); *see generally* EX1004, EX1008-EX1009.

Dr. Sourì merely restates the POR with no additional analysis or support, entitling his declaration to no weight. *Compare* EX2002 ¶¶71-75 *with* POR, 8-11; 37 C.F.R. § 42.65(a); *Upjohn v. Mova Pharm.*, 225 F.3d 1306, 1311 (Fed. Cir. 2000).

B. “to provide the power needed...”

The Board has already correctly held that “turning off the power appears to satisfy [the claim’s] requirement” that the global power mesh “provide the power needed” by the power domains. *See* ID, 20. Realtek identifies no good reason for the Board to abandon its construction and follow the ALJ’s erroneous construction. Even under the erroneous construction, the ALJ found the claims invalid. EX2007, 130-31, 139-45. Thus, the Board need not reach this construction. *Nidec Motor v. Zhongshan Board Ocean Motor*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

To the extent the Board addresses the issue, Realtek’s construction (“to provide the non-zero levels of power needed by the first power domain and second power domain”) improperly eliminates “needed” from the claim. *Texas Instruments v. ITC*, 988 F.2d 1165, 1171 (Fed. Cir. 1993) (It is improper to “read an express limitation out of the claims.”). Realtek contends that if the “‘power needed’ is zero, then there is nothing ‘to provide’ and the claim is not met.” POR, 14. But that incorrectly presumes “power needed” cannot include zero power when POSITAs would recognize that if a power domain needs no power, the global mesh can provide zero voltage, which is precisely the power needed. EX2005, 87:21-88:2; EX1003 ¶¶80-81; EX1037, 104:1-2 (Dr. Souri: “There is no requirement in Claim 12 that says you have to turn the chip on....”).

Further, the intrinsic evidence does not support Realtek’s construction. Realtek argues that “all” ’218 embodiments support its construction because they provide non-zero power during “sleep” mode. POR, 14. Its sole citation to the ’218 background section doesn’t exclude or disclaim providing zero voltage when no power is needed. EX1001, 1:18-33. The specification never asserts that providing reduced power versus no power was the invention. The purported invention is “a power mesh arrangement method.” EX1001, Abstract, 1:45-2:42. Realtek provides no reason to import these limitations into the claims.

C. “separately”

AMD agrees with the ALJ’s construction of “separately” as “through separate electrical paths.” POR, 15. The ALJ found Jiang and Li both met the “separately” limitation under this construction, EX2007, 130-31, 139-45. Realtek seeks a narrower construction that “the global power mesh itself must provide power through separate electrical paths.” POR, 15. In other words, Realtek reads “separately” to require separate power supplies. Both the ALJ and the Board correctly rejected this additional requirement. ID, 21; EX2007, 99-102, 130-31.

Here Realtek argues “the global power mesh (not the coupling) provide[] the power separately, *i.e.*, by separate paths.” POR, 16-17. But it asserted the opposite at the ITC: “The ‘*coupling*’ ‘*provide[s] the power needed*’ by the first power domain and the second domain *separately*”:

1

Realtek’s Construction Reflects the Intrinsic Record – Realtek’s Construction Is Not Redundant

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Realtek’s construction: “a power mesh capable of distributing power to multiple power domains”

12. A power routing structure applied in an integrated circuit having multiple power domains, comprising:
* * *
a global power mesh, coupling to the first local power mesh and the second local power mesh, to provide the power needed by the first power domain and the second domain separately;

The “coupling” “provide[s] the power needed by the first power domain and the second domain separately”

’218 Patent at Claim 12

26

CX-1863.0026

EX1036, 26; EX1035, 14:5-7.

Realtek’s construction is improper because it would import limitations from the specification into the claim. *King Pharms. v. Eon Labs.*, 616 F.3d 1267, 1275 (Fed. Cir. 2010) (“It would be improper to limit the broad terms used in the” claims to the “specific... conditions” in the specification.). The claim language simply requires providing the power needed “separately” and does not specify how to accomplish this. As the ’218 Patent explains, a separate path extending from the global mesh could provide the power needed “separately.” EX1001, 4:46-52; EX1038 ¶¶4-6. Indeed, Dr. Souri conceded that this is the only use of “separately” in the ’218 specification apart from the claims. EX1037, 50:2-51:5.

Realtek’s argument that the ’218 Patent has “no other mechanism contemplated for providing the power separately,” POR, 16 (citing EX1001, Fig. 4, 4:31-36, 5:14-17), is contradicted by its own cited embodiment, which shows separate electrical paths coming *from the global mesh*, including separate coupling to separate partial local power meshes, *e.g.*, EX1001, 4:39-52, Figs. 4-5. Even if Realtek were correct, Realtek ultimately seeks to import a limitation into the claims, which is improper. *Superguide*, 358 F.3d at 875 (“Specifications teach. Claims claim.” (citation omitted)).

D. “coupling”

Realtek seeks a construction of “coupling” at odds with the plain language of the claims. The plain language of claim 12 requires a “first[/second] partial local power mesh... coupling to the first[/second] power domain,” and a “global power mesh, coupling to the first[/second] local power mesh.” EX1001, 7:55-66. The plain meaning of “coupling” is “[t]he association of two or more circuits or systems in such a way that power or signal information may be transferred from one to another.” EX1040, 246; EX1037, 124:16-126:15 (Dr. Souri: definition “is consistent with my understanding”). The open-ended “comprising” claims do not recite “direct” couplings or exclude additional couplings. *CIAS v. Alliance Gaming*, 504 F.3d 1356, 1360 (Fed. Cir. 2007) (“‘[C]omprising’ ... mean[s] ‘including but not limited to.’”).

Despite the claim language, Realtek argues that the “coupling” limitations of claim 12 exclude embodiments where the coupling is indirect based on claim 19. POR, 21-24 (citing EX1001, 4:31-45, 3:56-64, 6:9-22). But Realtek’s assertion that its open-ended “comprising” claim 19 excludes “intermediary partial local power meshes” is legally incorrect. POR, 21-24; *CIAS*, 504 F.3d at 1360. Its distinction between claims 12 and 19 falls apart.

E. “at least one first local ground wire that couples to the ground wire of the global power mesh”

Doubling down on its incorrect view of “coupling,” Realtek argues that claims 7 and 16 require the ground of the global power mesh connect to a ground wire in the partial local power mesh “*and only then provide[] ground to the power domain.*” POR, 24. The emphasized portion has no basis in the claim language. Realtek again invokes claim 19, but as Realtek’s own construction concedes, “couples” simply means “connects.” The claims do not preclude intervening power meshes, sleep transistors, etc. Realtek’s assertion that “[t]here is no disclosure that a coupling to the partial local power can occur through the power domain,” POR, 25, assumes that the patent must disclose an embodiment for the claim to cover it, which is not the law. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1323 (Fed. Cir. 2005) (en banc) (“confining the claims to those embodiments” improper).

F. “same ground wire”

Realtek argues that the “same ground wire” in the global mesh “share[d]” by the “first” and “second local ground wire[s]” must be a “single ground wire.” POR, 18. But this interpretation conflicts with Realtek’s infringement position, as the ALJ already found, EX2007, 149, as well as the specification, which describes a “wire” as comprising “one common ground wire 403 and two power wires 401, 402,”

EX1001, 4:31-34, such that a “wire” can comprise multiple individual wires.

EX1037, 65:22-68:3 (Dr. Souri: “it says what it says”).

G. Undisputed Constructions

For purposes of this IPR, the parties do not dispute these constructions:

Claim term	Undisputed Construction
“having its position corresponding to”	“the partial mesh overlap to some degree with its respective domain when viewed from above” POR, 11; EX2007, 94.
“power mesh”	“a network of intersecting wires capable of distributing power” POR, 11; EX2007, 91
“global power mesh”	“power mesh capable of distributing power to multiple power domains” POR, 12; EX2008, 25
“local power mesh”	refers to the “partial local power mesh” earlier in the claims POR, 12; EX2007, 105
“separately”	“through separate electrical paths” POR, 15; EX2007, 102

III. GROUNDS 1-3 (JIANG)

A. Claim 12[a]-[b]

1. Jiang's Macros Are Independently Controlled Or It Would Have Been Obvious

Realtek disputes that Jiang's "first" and "second power domain" (macros B-C) are separate power domains "because they have the same power requirements." POR, 29. This argument fails because the claimed power domains aren't "required to have different power requirements from one another." *Supra* §II.A; EX2007, 130-31. Even if they were, Jiang teaches or suggests that its macros B-C are independently power-gated, which means they have different power requirements. Pet., 17-27; EX1003 ¶¶72-93; EX1004, Abstract, 1-2, Fig. 1(b).

Realtek has no response to the Petition's explanation that Jiang's "individual sleep transistors," which are "independently switchable between on or off," showed independently power-gated power domains. EX1003 ¶¶80-82; Pet., 21-23; EX1004, Abstract, 1-2, Fig. 1(b).

Realtek speculates that the macros B-C are not independently powered because Jiang mentions "non-power-gated" and "power-gated" power supply schemes. POR, 29. Realtek identifies no reason why Jiang's disclosed power-gating mode necessarily precludes independently-gated macros. Instead, Realtek inexplicably cites Table 1. Table 1 reported on Jiang's "[g]ating-effects vs. gated-

area” experiments but said nothing about whether “the gated macros B and C” in “Region I” were independently power-gated. EX1004, 2, 7.

Even if not disclosed, independently power-gating Jiang’s power domains to “provide more granular control and help reduce power consumption” was obvious. Pet., 23; EX1003 ¶¶82-85; EX1008, 4. Realtek has no answer to AMD’s evidence supporting the “routine application” and “ubiquitous usage” of independently controlled sleep transistors. Pet., 23 (citing EX1003 ¶¶84-85; EX1008, 4); *see also* POR, 34-35.

Citing nothing in Jiang, Realtek disputes modifying Jiang “because macros B and C needed the same power... and were idle at the same time.” POR, 35 (emphasis omitted). But this assertion that the limitation was non-obvious because it was not disclosed also ignores that separately gating macros B-C permits independent control, allowing one macro to be shut down even if the other still required power. Pet., 23; EX1003 ¶¶82-85. Thus, although not required by the claims, it would be obvious to supply independent voltages to Jiang’s macros B-C, indisputably satisfying the “power domain” limitations. Pet., 24-27; EX1003 ¶¶86-93.

2. Jiang2/Jiang3 Teach Macros Are Power Domains

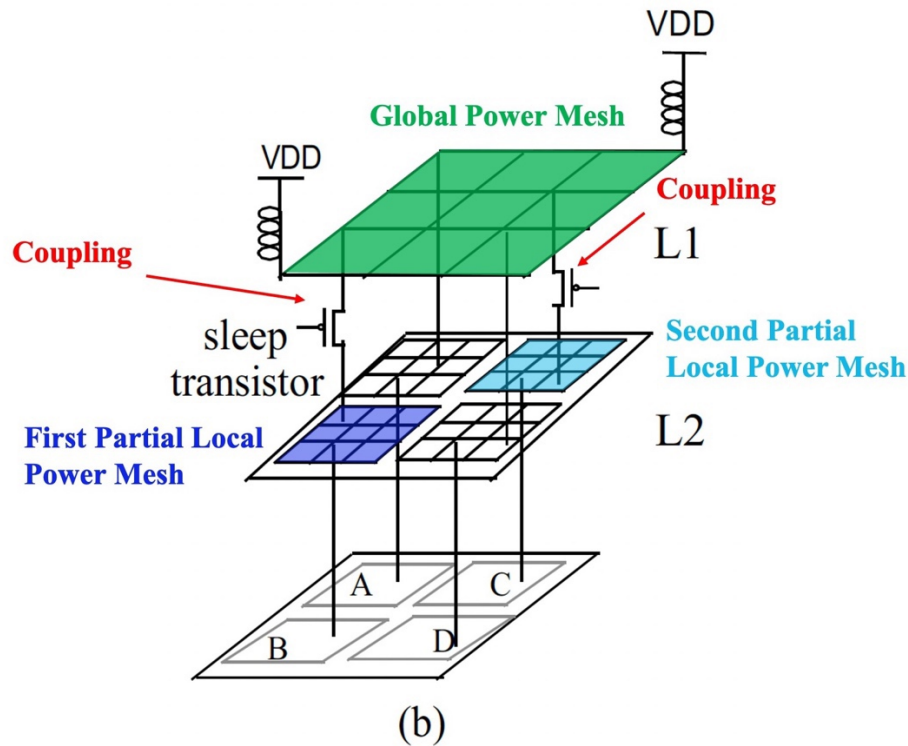
Jiang2/Jiang3 plainly taught that Jiang’s “macros” were “power domains.” Pet., 17-21 (citing EX1007, 1; EX1008, 1, 5). The ALJ agreed: “AMD rightfully points to Jiang2, a follow-on report to Jiang by the same authors, which even more

clearly associates macros with power domains....” EX2007, 130. Realtek argues the Board should entirely ignore this because Jiang2/Jiang3 “disclose different systems.” POR, 30. But Realtek never points to any differences, and its expert proffers an incorrect and flimsy position that Jiang differs because its macros are “not independently controlled by a sleep transistor.” EX2002 ¶134.

B. Claim 12[c]

1. “coupling”

Realtek argues Jiang’s inclusion of a sleep transistor precludes a global power mesh “coupling” to the partial local power meshes. POR, 31. First, this argument assumes an incorrect claim construction. *Supra* §II.D. Second, this argument ignores Jiang’s express disclosure that “sleep transistors are used *to connect the local mesh to the global mesh*”:

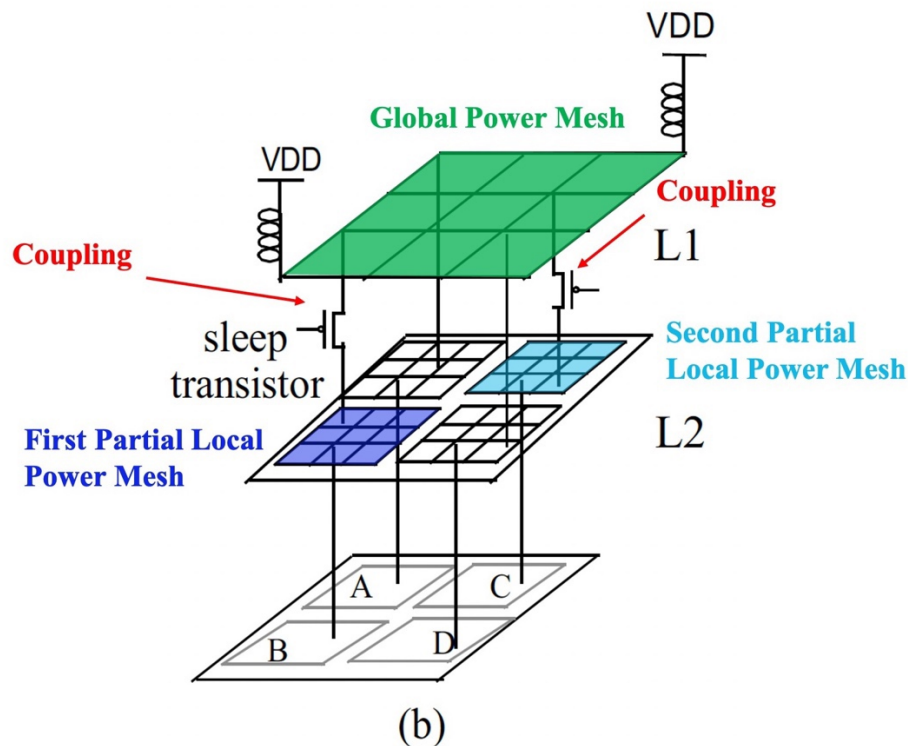


EX1004, 1, Fig. 1(b) (annotated); Pet., 17-22.

Realtek posits Jiang’s sleep transistors were in silicon and part of “the power domain,” precluding “coupling” between the global mesh and local meshes. POR, 31-32. Dr. Souri conceded Jiang’s sleep transistors cannot be part of the supplied power domain. EX1037, 137:8-140:6; EX2002 ¶142 (describing sleep transistors receiving “ V_{DD} voltage at all times,” when macros B-C do not). Even if true (it isn’t), power is transferred from global mesh to local mesh, which is “coupling.” See EX1040, 246.

2. “to provide the power needed ... separately”

Realtek contends that Jiang “does not provide the non-zero powers needed... through separate electrical paths.” POR, 33. This argument is based on two incorrect constructions. *Supra* §§II.B, II.C. Under the correct construction of “power needed” (where it can be zero), there is no dispute that Jiang teaches this limitation. *Supra* §III.A; Pet., 21-23; EX1003 ¶¶78-85. But even if Realtek’s non-zero power construction was correct (it isn’t), Jiang discloses this because the non-zero powers needed when the sleep transistors are on are provided through separate paths—the separate couplings from the global power mesh to separate partial local power meshes.



EX1004, Fig. 1(b) (annotated); EX1038 ¶7.

Despite its construction, Realtek argues that separate couplings are insufficient because “[t]he paths of the *global power mesh* are not separate.” POR, 33. The ALJ recognized “[t]his is incorrect.” EX2007, 130-31. Neither limitation 12[c] nor Realtek’s own construction requires the separate paths to be *in* the global mesh. *Supra* §II.C; EX1001, 7:64-67. Additionally, Jiang teaches separate paths through the separate local power meshes, as the ALJ found. EX2007, 130-31; EX1004, 1-2, Fig. 1(b); Pet., 21-23; EX1003 ¶¶78-85.

Even if Jiang did not teach “separately,” it would have been an obvious modification. *See* Pet., 24-27; EX1003 ¶¶86-93. Realtek doesn’t dispute that Jiang meets the claims when modified to use separate voltage supplies, as taught in Li or Chiu, or that POSITAs had a reasonable expectation of success in modifying Jiang. POR, 36-38; Pet., 24-27; EX1003 ¶¶86-93. Nor does Realtek dispute that “increas[ing] Jiang’s power savings,” Pet., 26, motivates making the modification, POR, 36-38.

Realtek argues only that Jiang already saves power and that no evidence shows separate voltage supplies yield “additional power savings.” POR, 36. Realtek is mistaken. Dr. Subramanian explained, in detail and with examples, additional power savings would be achieved by using separate supplies to power different domains at different levels, which consumes less *operating* power. EX1003 ¶¶91-

92; Pet., 26-27. This savings is *in addition to* the power savings when Jiang’s power domains were idle. EX1038 ¶¶8-9; *KSR Int’l v. Teleflex*, 550 U.S. 398, 420 (2007) (“any need or problem known in the field of endeavor” can provide a motivation to combine). This benefit answers Realtek’s argument that POSITAs would need a benefit to modify Jiang. POR, 37. Realtek’s contention that the modification supplies unneeded power to Jiang’s domains, POR, 36-37, ignores Jiang’s sleep transistors. And Jiang would not need additional metal layers, POR, 37, because its meshes are already on two different metal layers, Pet., 29-30; EX1003 ¶96.

Realtek argues adding separate power supplies would thwart Jiang’s power-gating study. POR, 37. But modifying Jiang wouldn’t remove its sleep transistors or impact power gating. Separate voltage supplies would still supply the same voltage when appropriate. EX1038 ¶10.

Realtek’s assertion that the “routine application” of independent supply voltages was generic and unsupported, POR, 38, ignores the Petition’s cited evidence, including the ’218’s admission that independent supplies were “common practice[.]” EX1001, 1:26-33; Pet., 27 (citing EX1003 ¶93).

C. Claim 12[e]-[f]

Jiang discloses the claimed global mesh routed on two metal layers. Pet., 29-33; EX1003 ¶¶95-103.

Realtek disputes this plain teaching because Jiang’s two-layer Figure 10 “is a separate embodiment” related to Figure 2, not Figure 1(b). POR, 39. But as shown below, “Figure 1(b) is the architecture of the power-gating system. Figure 2 is the modeling of *that* power-gating system.” EX2005, 210:16-22; EX1004, 2.

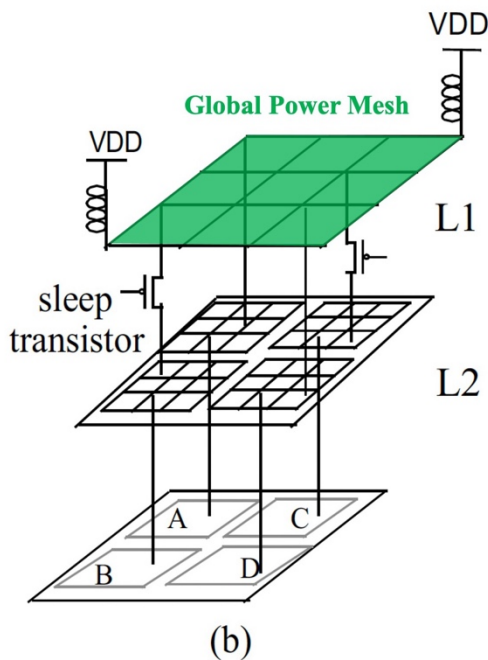


Figure 1(b)

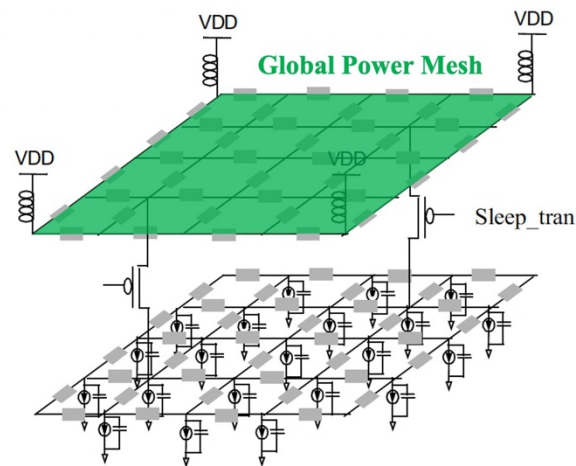


Figure 2

EX1004, Figs. 1(b)-2 (excerpted). Realtek’s admission that Figure 10 is “related to the model in Figure 2,” POR, 39, concedes it represents Jiang’s Figure 1(b) architecture, EX2005, 210:23-211:7.

With nothing from Jiang, Realtek invokes Dr. Sourì’s bare statement: “Figure 10 is a different embodiment than Figure 1(b).” POR, 39 (citing EX2002 ¶166). His unsupported testimony should be given no weight. 37 C.F.R. § 42.65(a).

Even if Jiang had not disclosed a two-layer global mesh, it would have been obvious. Pet., 31-33; EX1003 ¶¶97-103. The Petition established motivations to route Jiang’s global mesh on two layers, thus allowing the mesh to provide ground, multiple independent voltages, and/or signals on the same levels without shorting. Pet., 31-33; EX1003 ¶¶97-103; EX2005, 202:7-204:2.

Realtek avers Jiang “has only one voltage V_{DD} ” and doesn’t teach routing signals. POR, 40. But that does not address whether it would have been obvious to include them. And Dr. Subramanian explained Realtek’s assumption that Jiang only has V_{DD} wires is “nonsensical” because Jiang “is doing real circuit analysis” and has “more circuitry.” EX2005, 203:15-204:20.

D. Claim 15

The Petition established obviousness of a “ground wire” in Jiang’s global mesh. Pet., 36-38; EX1003 ¶109. Realtek neither disputes that a ground wire is necessary nor that a POSITA had a reasonable expectation of success in including the ground wire. See POR, 41-44.

Realtek instead argues Jiang “teaches away” from routing ground through the global mesh because Figure 2 “show[s] grounding in the substrate.” POR, 42. This nonsensical argument ignores how ground arrives at the substrate. EX1038 ¶¶11-12; EX1037, 156:8-22 (Dr. Souri agreeing that substrate ground can be provided

through a global mesh). Ground must enter the chip and be routed to the substrate. EX2005, 44:12-20, 55:15-58:3, 58:14-20; EX1038 ¶13; EX1006, 2:55-61.

Realtek and its expert also argue that Chiu shows “ground can be routed in other ways... such as through a via stack down to the substrate.” POR, 42 (citing EX1006, 2:61-63; EX2002 ¶178). But Chiu does not help Realtek, instead teaching routing ground *from* voltage supply “grids,” not *in lieu of* grids as even Dr. Souri acknowledged. EX1006, 2:55-61; EX1037, 77:10-78:17. And while Dr. Subramanian acknowledges that it’s “conceptually possible” to “drop vias directly from a pad or bump all the way down to the circuitry,” Realtek ignores his testimony that it “may not be possible due to other constraints.” EX2005, 46:9-47:14; *see also* EX1037, 92:7-93:16 (Dr. Souri explaining the importance of local mesh coverage of circuitry for power distribution).

Even if Jiang routed ground differently (it didn’t), that would not teach away from routing ground through the global mesh. EX1003 ¶109; *In re Mouttet*, 686 F.3d 1322, 1334 (Fed. Cir. 2012) (“mere disclosure of alternative designs does not teach away” (citation omitted)). Nothing in Jiang would have “discouraged” a POSITA from routing ground through the global mesh.

Realtek also disputes the Petition’s motivations to use the global mesh to route ground. POR, 43-44. AMD and its expert provide detailed and specific explanation and evidence supporting motivation, not generic conclusions. Pet., 36-38; EX1003

¶109 (citing exhibits); *Intel v. Qualcomm*, 21 F.4th 784, 797 (Fed. Cir. 2021) (“[A] rationale is not inherently suspect merely because it’s generic in the sense of having broad applicability or appeal.”). Dr. Sourì’s argument that routing ground in Jiang’s global mesh “would require using additional metal layers,” POR, 44, is a nonstarter because Jiang teaches or suggests meshes with two metal layers which are capable of routing ground, Pet., 29-33; EX1003 ¶¶95-103; *supra* §III.C.

E. Claims 16-17

The Petition also showed Jiang taught or suggested claims 16-17. Pet., 39-42; EX1003 ¶¶112-19. Realtek’s arguments for claim 15 should be rejected for claims 16-17 for the same reasons discussed above. POR, 44-46, *supra* §III.D. Realtek invokes Dr. Subramanian to assert a via stack from the global mesh to the substrate would “provide lower resistance” than a partial local power mesh, POR, 45, but Dr. Subramanian described “distribution network[s]” to avoid “long, circuitous paths” as would be likely if ground dropped to the substrate in only a single location, EX2005, 43:11-19. As Dr. Sourì explained, the lower metal layers (local meshes) use dense wiring of a smaller pitch “so that you can conduct signals to all of the different transistors and cells ... on the surface of the silicon.” EX1037, 92:7-93:16. Realtek also disputes the Petition’s motivation and reasonable expectation of success, POR, 45-46, but never addresses AMD’s actual argument or submitted evidence, Pet., 39-41; EX1003 ¶¶113-16.

F. Claim 18

Realtek argues Jiang does not teach or suggest local ground wires sharing the same global ground wire because “[g]round wiring can be done in many ways.” POR, 47. But Realtek never disputes the obviousness of “us[ing] a common ground in Jiang’s global and partial local power meshes.” Pet., 42-43; EX1003 ¶120; POR, 46-47. Realtek also never addresses the Petition’s point that *any* of Jiang’s global mesh ground wires could function as “the same ground wire.” Pet., 42-43; EX1003 ¶¶120-21.

Realtek mischaracterizes the Petition as relying solely on “all the ground wires” being the “same ground wire”—which was Realtek’s infringement position. POR, 47; EX2007, 149. Even under this interpretation, claim 18 is satisfied because Jiang’s partial local meshes are coupled to the global mesh, and Li meets it regardless. Pet., 21-27, 42-43; EX1003 ¶¶78-93, 120-21; EX2007, 148-50 (ALJ finding that Li disclosed limitation under this construction).

G. Claims 1-11, 19-20

Ground 3 showed claims 1 and 19 and their dependents were obvious over Jiang, optionally in view of Li or Chiu, and further in view of Bertolet or LPMM. Pet., 43-52; EX1003 ¶¶122-48. These references taught or suggested a power routing structure created with an APR tool. *Id.* Realtek’s arguments fail.

1. Ground 3’s Combination Renders Claims 1 And 19 Obvious

Realtek argues that “Petitioner cannot identify any references alone or in combination” satisfying claim 1 or 19 or how the combination would operate. POR, 48-49. Realtek ignores that Grounds 1-2 demonstrated the claimed power routing structure, and Ground 3 explained how creating that structure using APR tools would have been obvious in view of Bertolet, LPMM, and Li. POR, 48-55; Pet., 43-52.

Realtek’s strawman that no “known” APR tools “could be used to perform the steps of claim 1,” POR, 48-49, is not supported by the ’218 Patent itself which describes only a “simple algorithm for the APR tool” that evenly distributes the power meshes across the chip before subdividing the local mesh into partial local meshes. EX1001, 5:59-6:4; EX1037, 180:6-21 (Dr. Souri agreeing). The Petition established that Jiang taught both for claims 11 and 14, Pet., 34-35 (claim 14: subdivided local mesh), 49-50 (claim 11: evenly distributing power meshes), and Realtek’s POR had no response, POR, 48-55. The claimed steps were obvious to implement using existing APR tools. Indeed, Dr. Souri admitted (1) it “was fairly standard” to use an APR tool to form a single-power supply routing structure including sleep transistors (such as Jiang), and (2) APR tools *could be used* to design multiple power domain chips with some manual intervention. EX1037, 167:4-15, 161:20-163:3; *id.*, 165:18-167:2 (Dr. Souri: ’218 covers some manual intervention).

Realtek asserts Bertolet's tool was limited to a "single power domain," POR, 49-50, ignoring Bertolet's express teachings that its tool could "define *multiple* power terrains by area and level of metal" and "generate a routing structure including a global 'common power grid on metal levels one and two' and multiple local 'power grids on metal levels three through five.'" Pet., 44 (quoting EX1013, 126); *see also* EX1037, 174:7-175:1 (Dr. Souri agreeing Bertolet algorithmically generates unique power grids on multiple layers).

Realtek attacks LPMM's tool as unable to create global and partial local meshes. POR, 50. But Realtek and its expert never refute that LPMM's "power network" conventionally used a "grid design." EX1012, 175; *see also* Pet., 44-45; POR, 50; EX2002 ¶¶210. Nor do they counter expert testimony that a POSITA would understand how to use an APR tool like LPMM's to create the power routing structures from Grounds 1-2. EX1003 ¶¶124-130.

Realtek's arguments for Li are similarly unavailing. POR, 51. Li expressly teaches using its in-house APR tool "to implement a complete full-chip power distribution network," EX1005, 493, that includes the claimed power domains and meshes, *infra* §IV.A.

Realtek's final argument that the Petition omits any analysis or evidence of how the combination would read on the claims, POR, 52-53, withstands no scrutiny, *see* Pet., 43-52; EX1003 ¶¶122-48.

2. Motivation To Combine

The Petition cited extensive prior art and evidence expressly recommending APR tools. Pet., 44-46; EX1003 ¶¶125-130 (citing EX1012-EX1013; EX1001; EX1024-EX1025; EX1020). Realtek inexplicably attacks this motivation to combine as “generic,” POR, 53-55, while acknowledging AMD’s evidence that APR tools “would save time and effort in chip design” and that LPMM specifically recommends using “automated power network synthesis” “whe[r]ever possible.” POR, 54 (citing Pet., 45); *Intel*, 21 F.4th at 797 (distinguishing Realtek’s *ActiveVideo* decision where “expert indicated precisely how and why a skilled artisan would have combined the references”).

Realtek argues the Petition does not show why a POSITA would use Bertolet or LPMM, as opposed to other APR tools. POR, 54. The availability of alternatives does not defeat obviousness. *Moultet*, 686 F.3d at 1334. Realtek’s argument that “Jiang’s cartoon schematic in Figure 1(b) does not need APR tools,” POR 54, is contradicted by the ’218 Patent’s teaching to use APR tools on chips like Jiang, EX1001, 5:59-6:4; EX1038 ¶¶14-15, and Jiang’s teaching that its power meshes were used in chip design, EX1004, 6-7 (“We implement 26 circuits (from MCNC and ISCAS benchmarks respectively) as the basic logic blocks.”), Fig. 7, Table 3, 1 (Jiang: recommending “the power-gating technique in future technology nodes”);

EX2005, 203:18-19 (Dr. Subramanian: “Jiang is doing real circuit analysis”);
EX1038 ¶16.

Realtek’s argument disputing a reasonable expectation of success is a rehash of its already-disproved assertion that Bertolet and LPMM were unable to perform the claimed steps and ignores the Petition’s explanation and evidence. *Supra* §III.G.1; Pet., 43-46; EX1003 ¶¶122-30.

IV. GROUNDS 4-5 (LI)

A. Limitations 12[a]-[b]

Li taught multiple “power domains” and local power grids satisfying the claimed “first” and “second partial local power mesh.” Pet., 54-59; EX1003 ¶¶151-63. Realtek does not dispute this, POR, 56-58, instead arguing that Li’s partial local meshes are not located at their corresponding power domains. POR, 56. It concedes Li’s local meshes are in “the local sections,” yet asserts Li is silent about “where those local sections are.” *Id.* Dr. Subramanian explained that “at the block level” means Li’s local grids correspond to the position of their power domains. EX1003 ¶153. Dr. Souri agreed that “blocks” were underlying circuitry but feigned ignorance of “at the block level.” EX1037, 182:11-183:12, 189:14-190:5.

The ALJ disagreed with Realtek, finding the limitation “clearly disclosed.” EX2007, 142 (“This is why they are described as ‘local.’”). Realtek has no answer for Li’s explanation that local power grids are “formed at the block level,” EX1005,

493, which the ALJ said “strongly suggests those grids... are created in the region of the underlying logical circuitry.” EX2007, 142; *see also* EX1037, 82:14-83:3 (Dr. Souri agreeing that for a power supply grid to supply a power domain he “would think there would be some way to have an overlap”).

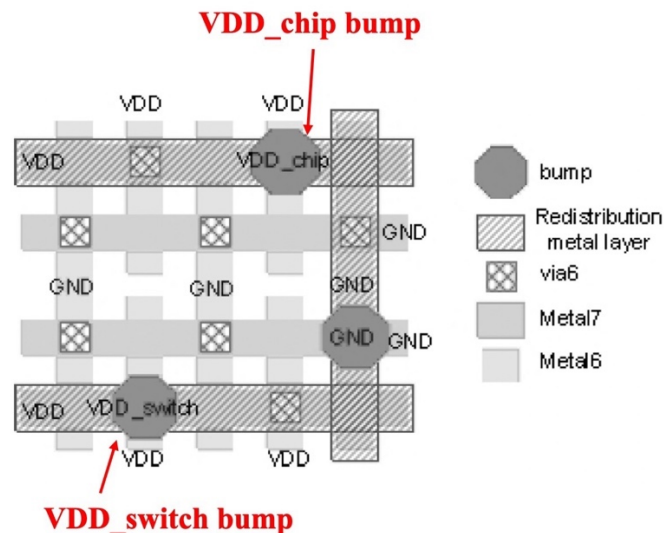
The Petition also established the obviousness of positioning Li’s local meshes over Li’s power domains as taught by Jiang. Pet., 55-56; EX1003 ¶¶154-56; *see also* EX1037, 82:14-83:3. Realtek did not dispute that POSITAs recognized this “would be a simple, straightforward, and efficient” solution. Pet., 56; EX1003 ¶¶154-56. The ALJ found these limitations were “obvious given Li’s teachings and Figure 1 of Jiang which visually demonstrates the concept,” EX2007, 142, which Realtek never addresses.

Realtek argues the “predictable” modification was generic, yet never addresses the Petition’s supporting evidence. POR, 57; Pet., 55-56; EX1003 ¶¶154-56; EX1006, 9:14-18; EX1016, 5:14-18; EX1004, Fig. 1(b)). Realtek contests whether Li and Jiang shared the same “purpose,” yet never disputes that Li would benefit from the modification. POR, 57; EX1003 ¶¶154-56. Dr. Souri’s testimony that Li’s local power grids with additional wiring “were not needed” is unexplained, EX2002 ¶238; POR, 57, and he never addresses Li’s teaching that they are part of the “complete full-chip power distribution network,” EX1005, 493.

B. Claim 12[c]

1. “global power mesh”

Realtek disputes that Li’s top-level grid satisfies the claimed “global power mesh,” arguing Li distributes only one voltage “VDD on metal-6 and metal-7.” POR, 58. Li plainly taught that its two voltages “*VDD_chip*” and “*VDD_switch*” “are routed alternately on Metal-6 in the vertical direction and Metal-7 in the horizontal direction,” as Dr. Souri readily conceded at his deposition. EX1005, 493; Pet., 59-60; EX1003 ¶¶164-65; EX1037, 183:14-184:8. Figure 3’s “bumps” illustrate the lines receiving “*VDD_chip*” or “*VDD_switch*”:



EX1005, Fig. 3 (annotated), 493. Arguing that using one voltage “makes sense” doesn’t override Li’s actual teaching of using two. *Id.*; POR, 59-60. Even had Li’s

global mesh distributed one VDD, the ALJ held the claims do not require distributing different voltages. EX2007, 130-31.

2. “coupling”

Realtek disputes Li’s disclosure of coupling its partial local power meshes to the global mesh. POR, 60. Li instructs that “local power grids are left floating *until* final assembly” when “complete full-chip power distribution network” is built by “connecting local logic to the top-level power grid.” EX1005, 493; Pet., 59-60. This requires “connecting the local power grids to the top-level power grid and the local logic,” otherwise the local grids stay “floating.” EX1003 ¶164. The ALJ agreed, and Realtek again has no answer. EX2007, 143-44 (citing EX1005, 493); POR, 60.

Realtek argues again that Li “discloses a connection between the ‘top-level power grid’ and the ‘local logic.’” POR, 60. The ALJ rejected Realtek’s argument as both “unreasonable” and “mischaracteriz[ing] the reference.” EX2007, 144. Realtek’s claim that Dr. Subramanian conceded “there can be connections from the ‘top-level power grid’ to the substrate,” POR, 60, ignores his actual testimony that Li’s global ground is coupled to a local ground via a sleep transistor. EX2005, 175:14-22.

C. Claim 16

Realtek doesn’t dispute that Li’s global mesh includes the claimed “ground wire” or that its first partial local mesh includes the “first local ground wire.” Pet.,

68-69; POR, 61-63. Realtek instead unsuccessfully argues they’re not coupled based on its theory that Li’s global mesh directly connects to the power domain. *Supra* §IV.B.2; EX2007, 147-48 (ALJ finding Li meets limitation). Li’s teaching of “power supplies that all share *the same chip ground reference*” shows all grounds are connected. EX1005, 495; *id.*, 493; EX1038 ¶¶17-18.

Realtek misrepresents Dr. Subramanian, pointing to Li’s Figure 4 and asserting that Li’s “global grid at the core actually connects to the switch in the power domain.” POR, 61. But he explained the “ground in the global mesh” connects to a “sleep transistor” connected to the ground “in the relevant local mesh for the particular core.” EX2005, 175:3-12; *id.*, 175:19-22. Realtek’s argument that Li discloses “ground wiring at the core” but no “local power grid,” POR, 62, is immaterial because the core ground wiring is part of the “local grid.” EX2005, 173:23-174:15, 175:3-12, 175:19-22.

The Petition also explained this limitation was at least obvious. Pet., 69. Realtek illogically argues that Li’s “switch” teaches away from connecting global ground to a local mesh, but the “switch” shows this very connection. POR, 63; *supra* §IV.B.2.

D. Claim 18

Realtek never contests Li teaches a “common” ground reference (GND). EX1005, 495; EX1037, 144:8-12 (Dr. Souri agreeing). Because every ground in Li’s

global mesh is shared by the local meshes, this limitation is plainly met. Pet., 70; EX1003 ¶181.

Realtek instead argues that Li’s local ground wires don’t “share the same ground wire of the global power mesh,” because Li’s local ground is not connected to global ground and there are no connections “below metal-6.” POR, 63-66. But Li taught “connecting local logic to the top-level power grid, to implement a complete full-chip power distribution network.” EX1005, 493. The ALJ already unsurprisingly rejected Realtek’s argument. EX2007, 149.

E. Claims 1-11 And 19-20

Realtek’s rerun of its Jiang arguments remains incorrect. *See* POR, 67, 70-72; *supra* §III.G. Its effort disputing motivation ignores the Petition’s detailed explanations and evidence. Pet., 70-72; EX1003 ¶¶182-87.

Realtek argues that Li’s mention of design reuse discourages deployment of APR tools. POR, 68. But Li never taught “design reuse” for the combination in this ground, Pet., 70-77, and Li expressly disclosed using “an in-house automated procedure” to layout “a complete full-chip power distribution network,” EX1005, 493.

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Advanced Micro Devices v. Realtek Semiconductor
Patent No. 8,006,218 – IPR2023-00920

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CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that foregoing **PETITIONER’S REPLY TO PATENT OWNER’S RESPONSE** exclusive of the parts exempted as provided in 37 C.F.R. § 42.24, contains 5,596 words and therefore complies with the type-volume limitations of 37 C.F.R. § 42.24.

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CERTIFICATE OF SERVICE

The undersigned certifies that pursuant to 37 C.F.R. § 42.6(e), a true copy of the foregoing **PETITIONER’S REPLY TO PATENT OWNER’S RESPONSE** and **EXHIBITS 1035-1038, 1040** are being served electronically on May 24, 2024 to the following lead and backup counsel for Petitioner to the following email addresses:

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