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UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

	)	
LG ELECTRONICS, INC.,	)	Case IPR2015-00325
	)	Patent 7,742,053 B2
Petitioner,	)	
	)	Case IPR2015-00326
v.	)	Patent 6,897,871
	)	
ATI TECHNOLOGIES ULC,	)	Case IPR2015-00330
	)	Patent 7,327,369 B2
Patent Owner.	)	

CONFIDENTIAL PURSUANT TO PROTECTIVE ORDER

VIDEOTAPED DEPOSITION OF ANDREW WOLFE, PH.D.

VOLUME II

November 10, 2015

Palo Alto, California

Reported by Michelle D. Knowles, CSR, RPR, CRR, CCRR

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1 VIDEOTAPED DEPOSITION OF ANDREW WOLFE,
2 PH.D., called on behalf of the petitioner as a
3 witness in the above-entitled matter, held at Mayer
4 Brown LLP, Two Palo Alto Square, Suite 300,
5 3000 El Camino Real, Palo Alto, California,
6 commencing at 8:56 a.m. on Tuesday, November 10,
7 2015, before Michelle D. Knowles, CSR No. 8979.

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1 I N D E X

2

3 WITNESS: PAGE

4 ANDREW WOLFE, PH.D.

5 Examination by Mr. Maier (Resumed) 286

6

7 E X H I B I T S

8

9 DEPOSITION EXHIBITS: PAGE

10 Wolfe Exhibit 12, United States Patent 287

11 5,500,939

12

13 Wolfe Exhibit 13, Declaration of Andrew Wolfe 299

14 Regarding U.S. Patent No. 7,327,369

15

16 Wolfe Exhibit 14, Declaration of Andrew Wolfe 301

17 Regarding Actual Reduction to Practice of

18 U.S. Patent No. 7,742,053

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1 PALO ALTO, CALIFORNIA;

2 TUESDAY, NOVEMBER 10, 2015, 8:56 A.M.

3 ---oOo---

4 THE VIDEOGRAPHER: Good morning. We are
5 now on the record.

6 This is Video No. 1 in the video
7 deposition of Andrew Wolfe, Ph.D., Volume No. II,
8 taken by the petitioner in the matter of LG
9 Electronics, Inc. versus ATI Technologies ULC, in
10 the United States Patent and Trademark Office,
11 Patent Trial and Appeal Board, No. IPR2015-00325,
12 326, and 330.

13 Today's date is Tuesday, November 10th,
14 2015. The time on the video screen is 8:56 a.m.

15 The location, court reporter, and
16 videographer are the same as Volume No. I.

17 Will all counsel now please state your
18 appearance for the record.

19 MR. MAIER: Cliff Maier of the firm Mayer
20 Brown on behalf of LG.

21 MR. NESE: Bryan Nese with Mayer Brown for
22 petitioner, LG Electronics, Inc.

1 MR. TUMINARO: Jonathan Tuminaro from
2 Sterne, Kessler, Goldstein & Fox on behalf of the
3 patent owner, ATI Technologies ULC, and the witness.

4 MR. BIRD: Jay Bird from Sterne, Kessler,
5 Goldstein & Fox, also on behalf of the patent owner,
6 ATI ULC Technologies, and the witness.

7 THE VIDEOGRAPHER: Okay. Did you want to
8 re-administer the oath or...

9 MR. MAIER: Sure.

10 ANDREW WOLFE, PH.D.,
11 having been first duly affirmed, was examined and
12 testified as follows:

13 EXAMINATION BY MR. MAIER (RESUMED)

14 MR. MAIER: Q. Well, welcome back,
15 Dr. Wolfe.

16 A. Hello.

17 Q. We'll try not to take up your entire day,
18 if we can. We did a good job yesterday of getting
19 through a lot of stuff, and so I won't remind you of
20 all of the introductory, how-to- --
21 how-to-be-deposed stuff that I went through
22 yesterday. But if, at any point, you want a break,

1 just let me know.

2 Let's start out back in Exhibit 2, which
3 is your declaration in the 326 IPR, and let's talk a
4 little bit about the Kurihara reference.

5 MR. MAIER: And did we distribute Kurihara
6 yesterday? I guess not.

7 MR. NESE: We did not.

8 MR. MAIER: Let's get that in evidence.

9 (Wolfe Exhibit 12 marked for
10 identification.)

11 MR. MAIER: And what's the number?

12 MR. NESE: 12.

13 MR. TUMINARO: Thanks, Bryan.

14 MR. NESE: You're welcome.

15 MR. MAIER: Q. So just some bookkeeping:
16 In front of you should now be Exhibit 12, which is
17 United States Patent No. 5,500,939 to Kurihawa --
18 -hara.

19 Do you recognize that?

20 A. I do.

21 Q. And that's one of the references that you
22 analyzed and opined on in Exhibit 2, which is your

1 declaration in the 326 proceeding; is that correct?

2 A. As part of a combination that was proposed
3 by LG, yes.

4 Q. Okay. I'd like to direct your attention
5 to page 259, paragraph 319 of the Exhibit 2.

6 MR. MAIER: I saw the look.

7 Q. And in this paragraph, you're discussing
8 that it's your opinion that Kurihara does not teach
9 or suggest the processor unit of claim 20; is that
10 correct?

11 A. It does say that, yes.

12 Q. And am I correct in understanding that one
13 of your arguments is that -- well, let me strike
14 that.

15 Does Kurihara suggest that vertex data can
16 be processed?

17 A. It does.

18 Q. And does Kurihara suggest that pixel data
19 can be processed?

20 A. It does but at a different time, in a
21 different phase.

22 Q. So it's your understanding that Kurihara

1 suggests that vertex and pixel data cannot be
2 processed at the same time?

3 MR. TUMINARO: Objection. Form.

4 THE WITNESS: Not without adding something
5 to Kurihara that's not there. The -- the -- all
6 Kurihara really teaches is that there are FIFOs that
7 can either be holding pixel data or can be holding
8 vertex data, and it only describes the situations
9 where it holds one or the other.

10 And the real teaching of Kurihara is that
11 you would set the FIFO or refill threshold
12 differently when processing vertex data than when
13 processing pixel data. And it doesn't even seem to
14 contemplate and certainly doesn't teach how to deal
15 with the situation where you could have both vertex
16 and pixel data in the same FIFO or where different
17 FIFOs could have different types of data.

18 And in claim 20 requires a -- a processor
19 unit that executes vertex calculations while pixel
20 calculations are still in progress, and that's
21 what's not disclosed in Kurihara.

22 MR. MAIER: Q. So I just want to make

1 sure I understand you.

2 So you agree that in Kurihara, there are
3 multiple graphics processors; correct?

4 A. There are.

5 Q. And you agree that those graphics
6 processors can operate simultaneously; correct?

7 A. Yes. Let me take a quick look and see
8 what the limitations are on that.

9 They can -- they can operate
10 simultaneously.

11 Q. And you agree that the graphics data in
12 the FIFO memories can be either vertex data or pixel
13 data; correct?

14 MR. TUMINARO: Objection. Form.

15 THE WITNESS: Yes. As is disclosed in
16 Kurihara, the FIFOs can either hold -- all the FIFOs
17 can hold pixel data, or all the FIFOs can hold
18 vertex data.

19 MR. MAIER: Q. Is it your understanding
20 that claim 20 requires that a single processor unit
21 stalls one type of graphics processing operation
22 while that operation is in progress in order to

1 perform another type of graphics processing
2 operation?

3 MR. TUMINARO: Objection. Form.

4 THE WITNESS: I think that's right.
5 There's only a single processor unit that's recited
6 in claim 20, and the vertex calculations and the
7 pixel calculations both have to operate on the
8 processor unit. So I think that's -- that's
9 correct.

10 MR. MAIER: Q. And it's your
11 understanding that if one operation is stalled and
12 then another operation is performed, that those two
13 operations are performed simultaneously?

14 A. Not simultaneously but while still in
15 progress. And actually, it wouldn't have to be
16 stalled. They -- they could both be executing
17 concurrently in a single processor unit if some- --
18 somehow -- or they could be -- they could be both in
19 the pipeline of a single processor unit.

20 It's -- it's a little bit broader than
21 that, but -- but if the processor units are simple,
22 then -- then one would have to stall.

1 Q. What does it mean when you say
2 that -- strike that.

3 What does it mean when you refer to
4 "interleaving calculations of different types" in
5 paragraph 320?

6 A. There's no disclosure in Kurihara that --
7 that while -- that -- that -- that vertex and pixel
8 operations, for example, can occur in close
9 proximity to each other in time or in space. All
10 that's described is that the FIFOs fill up with one
11 type of data, and then that whole phase is
12 completed.

13 And there's no description of placing data
14 of a different type into any one of the FIFOs while
15 any operation of a different type or from a previous
16 phase is still in progress.

17 Q. Is it your understanding that claim 20 of
18 the '871 patent requires interleaving calculations
19 of different types?

20 A. It doesn't require it, but that would be
21 one way -- that -- that was essentially what was
22 implied in the invalidity allegations, is that they

1 would be interleaved, and -- and it was just a
2 misreading of the reference.

3 Q. So claim 20 would permit a situation in
4 which the processor unit is capable of
5 simultaneously performing two operations?

6 MR. TUMINARO: Objection. Form.

7 THE WITNESS: It could.

8 MR. MAIER: Q. Let's turn to page 261 of
9 Exhibit 2.

10 Earlier, with respect to the 325 IPR, we
11 talked about objective indicia of nonobviousness.
12 Here in Exhibit 2, you also have some discussion of
13 objective indicia of nonobviousness.

14 One of the things that you talk about is
15 ATI's Xenos chip; is that correct?

16 A. Correct.

17 Q. And that chip was used in the Xbox 360; is
18 that correct?

19 A. Yes.

20 Q. And the Xbox 360 was generally directed
21 toward gaming; is that correct?

22 A. I guess that's correct; although, I think

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1 Microsoft marketing might not agree. They -- they
2 saw it as a -- as a multidimensional platform for
3 gaming and video and a number of other applications.

4 Q. Is it your understanding that the Xbox 360
5 was directed to engineering applications like
6 SOLIDWORKS?

7 A. No.

8 Q. Is it your understanding that ATI's Xenos
9 chip practiced any claim of the '871 patent?

10 A. Yes, it is.

11 Q. And on what do you base that
12 understanding?

13 MR. TUMINARO: I'll caution the witness
14 not to disclose the substance of any attorney
15 communication you may have had or work that you did
16 at the direction of counsel that's not in your
17 report.

18 THE WITNESS: It's my understanding that
19 the key functionality in the R400 source code that I
20 analyzed for this case is still present in the Xenos
21 chip.

22 MR. MAIER: Q. And what's the basis of

1 that understanding?

2 A. That's been represented to me by ATI.

3 Q. So there's no -- there's no evidence that
4 you can give me today that that's the case; is that
5 correct?

6 A. I think that's right.

7 Q. Have you prepared a claim chart that
8 compares the functionality of the Xenos chip to any
9 claim of the '871 patent?

10 MR. TUMINARO: Objection. Form.

11 THE WITNESS: Only to the extent that it's
12 consistent with the earlier development versions
13 that I analyzed.

14 MR. MAIER: Q. And how do you know that
15 it's consistent with those earlier development
16 versions?

17 A. That's what the developers have
18 represented to me.

19 Q. You mention an article in Computer
20 authored by Greg Humphreys in paragraph 324; is that
21 correct?

22 A. Yes.

1 Q. Is there information in that article
2 sufficient to allow you to determine that the Xenos
3 chip practiced any claim of the '871 patent?

4 A. No, not in the article alone.

5 Q. Does Microsoft operate chip fabs?

6 A. I'm not aware of them operating any chip
7 fabs, but I -- I wouldn't necessarily know.

8 Q. You say in paragraph 325 that the Xenos
9 chip was based on ATI's design; is that correct?

10 A. Yes.

11 Q. Did -- are you aware of whether or not
12 Microsoft modified that design in any way?

13 A. It's my understanding they did not.

14 Q. What is your understanding of what it
15 meant that -- when you say that Microsoft had the
16 Xenos chip fabricated?

17 A. It's my understanding that the tapeout
18 files were provided from ATI to Microsoft, and then
19 Microsoft entered a contract with the fabrication
20 facility to have the chips built.

21 Q. Are you aware of whether or not the
22 Xbox 360 was marked with the '871 patent number?

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1 A. I am not aware one way or the other.

2 Q. Are you -- are you aware of whether or not
3 ATI marks any of its products with the '871 patent
4 number?

5 A. I don't know one way or the other.

6 Q. You mention in paragraph 325
7 Dean Takahashi; is that correct?

8 A. Yes.

9 Q. What books has Dean Takahashi written?

10 A. Oh, I don't know if I know all of his
11 books, but he wrote a book on the Xbox and he wrote
12 a book on the Xbox 360. Primarily, he's been a
13 daily journalist through most of his career. He was
14 the Silicon Valley editor for the Wall Street
15 Journal, and he worked at -- at Red Herring and --
16 and now at GameBeat.

17 Q. In paragraph 325, you say you -- he -- you
18 know "he interviewed Microsoft staff extensively to
19 develop the facts reported in his book."

20 A. Uh-huh.

21 Q. What's the basis for that knowledge?

22 A. I was in regular communication with him

1 when he was making the trips and scheduling the
2 interviews, and he was telling me about them at the
3 time.

4 Q. So you know Dean Takahashi personally?

5 A. I do.

6 Q. Is there anything in any of the claims of
7 the '871 patent that re- -- strike that.

8 Does the -- does the term "unified shader"
9 appear anywhere in the claims of the '871 patent?

10 A. Yes.

11 Q. Where is that?

12 A. Preamble of claim 15, for example.

13 Q. Anywhere else?

14 A. It's referred back to as "the shader" in
15 the depending claims. A person of ordinary skill
16 would understand that to be referring to a unified
17 shader.

18 Q. And claim 15 doesn't just claim a unified
19 shader. It claims a specific unified shader;
20 correct?

21 A. It does.

22 Q. Is it possible to design a graphics chip

1 with a unified shader that doesn't infringe
2 claim 15?

3 MR. TUMINARO: Objection to form.

4 THE WITNESS: Depends how you define
5 "unified shader." I mean, certainly not -- it
6 depends how you define "unified shader."

7 Certainly, you could de- -- have a
8 structure that doesn't practice claim 15. I'd have
9 to look at it to see whether or not anybody would
10 call it a unified shader or not.

11 MR. MAIER: Let's jump to the third IPR.

12 (Wolfe Exhibit 13 marked for
13 identification.)

14 MR. MAIER: This is 13?

15 MR. NESE: Yes.

16 MR. TUMINARO: Thank you.

17 MR. MAIER: Q. So in front of you now
18 should be a document marked as Exhibit 13 entitled
19 "DECLARATION OF ANDREW WOLFE REGARDING U.S. PATENT
20 NO. 7,327,369."

21 This appears to be a declaration submitted
22 by you in IPR2015-00330; is that correct?

1 A. Correct.

2 MR. TUMINARO: I'll just note for the
3 record that this is black and white, and it was
4 produced in color.

5 MR. MAIER: Fair enough.

6 Q. In this declaration, do you offer any
7 opinions as to any of the prior art alleged to
8 invalidate the patent?

9 A. I offer the opinion that it's not, in
10 fact, prior art, that it postdates conception and
11 reduction to practice.

12 Q. Do you offer any opinions as to whether or
13 not any of that alleged prior art is missing any of
14 the limitations of any of the claims?

15 A. I don't.

16 Q. And so your argument is that it's not
17 prior art because of prior conception and reduction
18 to practice; is that correct?

19 A. That's my opinion.

20 MR. MAIER: And then we're done with that
21 one, so that was pretty easy.

22 Let's do the final, the -- that one.

1 (Wolfe Exhibit 14 marked for
2 identification.)

3 MR. MAIER: Q. In front of you now should
4 be Exhibit 14, which is entitled "DECLARATION OF
5 ANDREW WOLFE REGARDING ACTUAL REDUCTION TO PRACTICE
6 OF U.S. PATENT NO. 7,742,053." And this appears to
7 be a -- I believe it's a supplementary or a second
8 declaration for Case IPR2015-00325.

9 Is this a declaration that you offered in
10 that matter?

11 A. It is.

12 MR. TUMINARO: I'm just going to object to
13 form, but...

14 MR. MAIER: Okay.

15 Q. The -- earlier you were -- just a minute
16 ago, you were talking about, with respect to the
17 330, some -- that -- that one of your opinions was
18 that there was conception and reduction to practice
19 that predated some of the alleged prior art, and
20 that was based on the R400 chip; is that correct?

21 A. The R400 design, yes.

22 Q. And this declaration addresses similar

1 arguments but with respect to the '053 patent; is
2 that correct?

3 A. Yes, an actual reduction to practice and a
4 constructive reduction to practice.

5 Q. And maybe we can save a little bit of
6 time.

7 The evidence and the details regarding the
8 actual re- -- reduction to practice and conception,
9 do they differ between the three IPRs?

10 A. Yes.

11 Q. Other than comparing to the patent claims
12 and comparing to the dates or the actual --
13 they're -- they're not all based on the R400?

14 A. Oh, they are all based on the R400 but
15 different pieces of R400 code, and different pages
16 in the document correspond to different claim
17 elements.

18 Q. Okay. I understand that.

19 We would be looking at different
20 structures in the R400, different Verilog, but it's
21 the same R400 that we're talking about in all of
22 these cases; correct?

1 A. It is. Although, for the conception
2 documents, for one of the patents, at least, maybe
3 for -- I'm trying to remember which. I think for
4 the '871 and '369 patents, I look at two different
5 versions of the conception documents at two
6 different dates.

7 Q. Okay.

8 A. Actually, let me just check and make sure
9 I have that.

10 No. That's actually for the '053. I look
11 at the conception documents as of two different
12 dates, two different versions.

13 Q. Is it your understanding that actual
14 reduction to practice requires proof of either an
15 embodiment of a claimed invention or performance of
16 a process that includes all limitations of the
17 claimed invention?

18 A. That's what counsel has asked me to apply
19 as a legal principle for purposes of this
20 proceeding.

21 Q. And that's the legal principle you applied
22 in performing your analysis?

1 A. Yes.

2 Q. On paragraph -- in paragraph 23 on page 9,
3 you describe that you examined two types of source
4 code.

5 You talk about RTL code and Verilog and
6 emulator code in C++; is that correct?

7 A. Correct.

8 Q. And you examined those types of source
9 code as part of your analysis of actual reduction to
10 practice?

11 A. Yes. The RTL code is the evidence of
12 actual reduction to practice. The C++ code is --
13 basically corroborates it.

14 MR. TUMINARO: Just -- I'm going to
15 designate the transcript as confidential under the
16 protective order as we're getting into source code.

17 MR. NESE: Both days or just today?

18 MR. TUMINARO: Well, I think I'll
19 designate the whole thing, and then we'll -- we can
20 figure it out afterwards.

21 MR. NESE: Okay.

22 MR. MAIER: Q. When you say that you

1 examined the source code, what do you mean?

2 A. I read it, I reviewed it, I studied it to
3 the point that I could understand how it operated,
4 and then I documented relevant portions of it for
5 the purpose of preparing this report.

6 Q. The -- let's talk first about the emulator
7 code.

8 A. Okay.

9 Q. That was written in C++; is that correct?

10 A. Yes.

11 Q. Did you attempt to compile the emulator
12 code?

13 A. No.

14 Q. Did you attempt to execute the emulator
15 code?

16 A. Well, without compiling it, it wasn't
17 executable.

18 Q. Did you attempt to apply any inputs to the
19 emulator code to see what the outputs would be?

20 A. No. It's my understanding that ATI did
21 and that they have and will testify about that
22 experience, but I didn't do it.

1 Q. Have you seen any results of executing the
2 emulator code?

3 A. I don't think directly. I think that the
4 results I've seen are the results of executing the
5 RTL. And I think that I've heard witnesses say that
6 the results of the emulator code were identical, but
7 I don't think I've seen them separately.

8 Q. Have you -- well, let's -- let's talk
9 about that a little bit.

10 Is it your understanding that one of the
11 purposes of the emulator code is that you would
12 apply the same inputs to the RTL and the emulator
13 code and determine whether or not you get the same
14 outputs?

15 A. That's my understanding of one of its
16 purposes, yes.

17 Q. And is that called logic verification?

18 A. I don't know that I've heard the term
19 "logic verification" used. I -- I -- it -- I've
20 heard it referred to as "verification."

21 Q. Are there other types of verification that
22 need to be performed when one is designing a chip?

1 A. Yeah. There's timing verification.
2 Sometimes there's functional verification. Depends
3 on what the process is at an individual company.

4 Q. Do you know what the process was at A- --
5 at ATI when they were designing the R400?

6 MR. TUMINARO: Objection to form.

7 THE WITNESS: In general, I do.

8 MR. MAIER: Q. You state in paragraph 23
9 that RTL is used to instantiate a hardware design.
10 What did you mean by the term
11 "instantiate"?

12 A. To create an embodiment, to create a --
13 what we sometimes call a realization. So once you
14 think of a hardware design, you have to actually
15 create a version of it. And RTL is a specification
16 language, so it creates a version of a hardware
17 design in which the specific design decisions and
18 specific structure and function decisions have to be
19 made.

20 Q. It's your understanding that RTL creates
21 hardware?

22 A. In a sense. In the same sense that --

1 that source code creates software, that once you
2 create -- once you write the RTL, you can then use
3 an automated process to get a chip -- or to get the
4 manufacturing tooling for a chip.

5 Q. Is it your understanding that ATI used an
6 automated process to convert the RTL into a chip?

7 A. Which RTL?

8 Q. For the R400.

9 A. I don't know. I know that's their normal
10 process when they finish a design, but...

11 Q. Does -- strike that.

12 At the time that the R400 was being
13 designed, were physical designers employed to
14 place -- well, strike that.

15 Do you know if standard cells were used in
16 the R400?

17 A. It's my understanding they were.

18 Q. Do you know if custom macros were used in
19 the R400?

20 A. I don't know.

21 Q. Were there memory structures on the R400?

22 A. Yes.

1 Q. Were they created from standard cells?

2 A. Some of them may have been. There --
3 there is detailed RTL that -- you know, basically,
4 for -- for some of the memories, at least, that kind
5 of shows them to be a regi- --

6 (Interruption in the proceedings.)

7 MR. NESE: Let's go off the record.

8 THE VIDEOGRAPHER: We are now off the
9 record at 9:29.

10 (Recess taken.)

11 THE VIDEOGRAPHER: We are now on the
12 record at 9:42.

13 MR. MAIER: Well, I apologize for that
14 strange interruption, and let's keep our fingers
15 crossed that the TVs don't turn on again.

16 Q. We were talking about the R400.

17 Was the R400 ever taped out?

18 A. I don't know. There -- there are two
19 questions. One is that when they tape it out,
20 sometimes they change the name a little bit. They
21 call it the R400, but sometimes when they tape it
22 out, I think it might have -- supposed to be called

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1 the R420 as a product. But I don't know whether or
2 not it ever happened for certain. You'd have --
3 have to ask ATI.

4 Q. So just to be clear, because you raise a
5 good point, what I meant to ask is, did a chip ever
6 tape out based on the Verilog that you had examined?

7 MR. TUMINARO: Objection. Outside the
8 scope.

9 THE WITNESS: Well, as I said, it's my
10 understanding that same Verilog was still present in
11 a later version that became the Xenos, but -- but
12 that's -- again, that's just based on my discussions
13 with the developers.

14 MR. MAIER: Q. And you've never seen
15 Verilog for the Xenos; is that correct?

16 A. I think that's right.

17 Q. Let's talk a little bit about the process
18 of going from Verilog to a chip. So we were
19 discussing tapeout.

20 A. Uh-huh.

21 Q. What's tapeout?

22 A. Usually, tapeout is when you tell the

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1 computer-aided design tools to create a final
2 netlist and then use that final netlist to create
3 a -- a final maskset specification or -- I'm trying
4 to think what the best word for those files are
5 other than "tapeout" -- physical design files.

6 So you would run the netlist through a
7 placement and routing tool that gives you the
8 physical specifications for the final chip. It
9 creates a set of files that are usually called GDSII
10 files, and you send those to a -- a mask-making
11 house to make the physical manufacturing tooling for
12 the chip.

13 Q. So the Verilog doesn't get sent to the
14 fab; is that correct?

15 A. That's generally true. You place the
16 Verilog through a toolchain, and you send the output
17 of that toolchain to the fab.

18 Q. Why don't you send the Verilog to the fab
19 if all they have to do is run the software to
20 automatically convert it into a mask?

21 A. There are some business models where --
22 where that's done. But typically, in the case of a

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1 company like ATI, there are two issues: One is it's
2 source code, and it's considered proprietary and you
3 wouldn't want to share it even with a manufacturing
4 partner; and second, there would be a number of
5 verification steps in the toolchain where you would
6 check to make sure that the tools did things
7 correctly and to your specifications.

8 Q. How -- what's a floor plan for a chip?

9 A. A floor plan is a descr- -- high-level
10 description of where the logic blocks should be
11 placed on the die.

12 Q. With respect to the R400, how was the
13 floor plan created?

14 MR. TUMINARO: Objection. Outside the
15 scope.

16 THE WITNESS: I don't know.

17 MR. MAIER: Q. Was it -- strike that.

18 Are floor plans generally created by
19 someone by hand, or are they created by a tool that
20 automatically figures out where things should go?

21 A. It varies.

22 Q. How was the power grid designed in the

1 R400?

2 MR. TUMINARO: Objection. Outside the
3 scope.

4 THE WITNESS: I don't know.

5 MR. MAIER: Q. What are the issues that
6 come into play when somebody is designing a power
7 grid for a graphics processor?

8 A. Static and -- and dynamic voltage drops is
9 generally the issue. Sometimes, depending on what
10 the product is, block-level power management.
11 Sometimes on the ground plane, the things that I
12 call voltage drops, they'll call ground bounce.

13 Q. How was the clock grid design in the R400?

14 A. I don't know.

15 Q. Do you know if it was automatically
16 created?

17 A. I don't. I know there were automatic
18 tools at that time, but I don't know whether or not
19 ATI used them.

20 Q. What were the automatic tools at that
21 time?

22 A. I don't know their names, but major

1 vendors would sell you a clock grid -- generation
2 tool or a clock grid timing tool.

3 Q. Are you familiar with the term, in
4 physical design of chips, called "prerouting"?

5 A. Maybe. I'm not sure we're talking about
6 the same thing. Sometimes you do channel assignment
7 in an early stage in some layout techniques to be
8 able to do -- sometimes people call it a high-level
9 routing as opposed to a detailed routing.

10 Is that -- is that what we're talking
11 about?

12 Q. No.

13 A. Okay.

14 Q. Do you know what automatic -- automated
15 tools were used to convert the RTL that you looked
16 at into a chip?

17 MR. TUMINARO: Objection. Form.

18 THE WITNESS: I seem to recall someone
19 telling me that they used Design Compiler, but I'm
20 not sure whether or not that was the only tool.

21 MR. MAIER: Q. And do you know what time
22 period they used that tool?

1 A. No.

2 Q. Isn't it true that what Design Compiler
3 does is produce a netlist from the RTL?

4 A. Generally.

5 Q. It doesn't produce placement and routing
6 information, does it?

7 A. That was my understanding at the time.

8 Q. It's your understanding that Design
9 Compiler performs place and route?

10 A. No. My understanding was that as of this
11 time period that we're talking about, 2000 to 2004,
12 the Design Compiler produced a netlist, and one
13 would use a different tool to do place and route.

14 Q. Do you know what tool was used to do place
15 and route?

16 A. No.

17 Q. What are the inputs to Design Compiler?

18 A. It can vary, but typically, it's RTL code
19 and then some -- some scripts.

20 Q. What do those scripts do?

21 A. They set modes and parameters. They can
22 set options or specify criteria to prioritize.

1 Q. What sorts of criteria?

2 A. Speed, power, particular paths having to
3 meet certain timing criteria.

4 Q. You mentioned that it was your
5 understanding that the R400 was a standard cell base
6 design; is that correct?

7 A. Yes.

8 Q. Who designed the standard cells?

9 A. I don't know.

10 Q. Are standard cells designed in an
11 automated manner?

12 A. They can be. There are people who do
13 that, but I don't know whether or not that was the
14 case here. I think it's most likely they were
15 simply licensed from a vendor.

16 Q. Are you familiar with the term "formal
17 verification"?

18 A. Yes.

19 Q. Was for- -- formal verification used to
20 verify the design of the R400?

21 A. I don't know.

22 Q. You haven't seen any reports from a formal

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1 verification tool regarding the R400, have you?

2 A. I haven't seen any evidence of formal
3 verification, but I haven't asked for it.

4 Q. Verilog can also be simulated; is that
5 correct?

6 A. It can.

7 Q. Did you simulate the Verilog that you
8 looked at in preparing this report?

9 A. No.

10 Q. Do you know if the Verilog that you looked
11 at is capable of being simulated?

12 A. There's evidence that ATI simulated it at
13 the time or ran it on a hardware emulator -- I'm not
14 sure which -- but they executed it at the time, so I
15 assume it is.

16 Q. And is there any other basis for your
17 assumption other than what you just said?

18 MR. TUMINARO: Objection. Form.

19 THE WITNESS: Mr. Lefebvre's testimony
20 that -- that it was simulated or that it was
21 executed.

22 MR. MAIER: Q. Does Verilog describe the

1 transistors that would be present in the final chip
2 design?

3 A. Not precisely. It describes their overall
4 structure and function but not the individual
5 transistors. It describes them in -- in groups.

6 Q. So I could -- strike that.

7 What do you mean by "it describes them in
8 groups"?

9 A. It describes logic functions and
10 registers, each of which would be made up of
11 multiple transistors.

12 Q. Does the Verilog tell you what those
13 transistors are and how they're connected?

14 A. Not as written here. Not -- it doesn't
15 tell you the individual transistors.

16 Q. It tells you logic functions; is that
17 correct?

18 A. Logic functions and, in many cases,
19 structure: where buses exist, where registers
20 exist, what kind of timing exists between those
21 particular structures.

22 Q. What do you mean when you say that Verilog

1 describes timing?

2 A. It can tell you that -- that things happen
3 on clock edges.

4 Q. Verilog doesn't tell you how long it will
5 take to perform a particular function, does it?

6 A. It can, but this Verilog did not.

7 Q. Does Verilog -- does the Verilog that you
8 look at -- strike that.

9 Does the Verilog that you looked at tell
10 you where any particular structures would be located
11 on the chip?

12 A. Physically?

13 Q. Yes.

14 A. No. That gets determined at the
15 place-and-route stage.

16 Q. Is it your understanding that all of the
17 logic that's found in the RTL that you looked at was
18 converted to logic gates by CAD tools?

19 MR. TUMINARO: Objection. Form.

20 THE WITNESS: I think in some very -- I
21 think there were a few situations where there were
22 references to libraries that had already been

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1 created by a CAD tool. So it was created from
2 something other than what I looked at and then
3 reused.

4 MR. MAIER: Q. Have you seen a netlist
5 corresponding to the Verilog that you looked at?

6 A. I have not.

7 Q. If you haven't seen a netlist
8 corresponding to the Verilog you looked at, how can
9 you tell that it was created by tools and not by
10 somebody looking at the RTL and converting it into a
11 gate-level netlist by hand?

12 A. Because I'm aware of the process that ATI
13 uses from talking to their engineering team.

14 Q. And who did you talk to on their
15 engineering team?

16 MR. TUMINARO: You can -- I'll caution the
17 witness not to disclose the substance of any
18 communication, but you can say who you talked to.

19 THE WITNESS: I've talked to a number of
20 people over the years with respect to the R400
21 design, including Mr. Lefebvre, Eric Demers,
22 Bob Drebin, and Raja Koduri.

1 MR. MAIER: Q. And you're relying on
2 those conversations for your opinion that CAD tools
3 were used to convert the RTL into gates; is that
4 correct?

5 A. Yes. That would also be, by far, the
6 dominant process for a graphics chip design at the
7 time. I'm not aware of anyone having done it any
8 other way.

9 Q. Okay. So what specifically did those
10 engineers tell you?

11 A. That they compiled the RTL using a
12 standard cell library and that that's how they
13 created the netlist.

14 Q. And they were referring to this particular
15 RTL that you looked at?

16 A. They were referring to the R- -- R400
17 program, in general. And they told me that
18 sometimes memories came from libraries that had been
19 created by other memory generator tools and that
20 sometimes adders and multipliers came from libraries
21 that had been created by -- by generator tools.

22 Q. When you refer to -- when you refer to

1 "generator tools," you're referring to software that
2 is designed to create specific parameterized
3 structures?

4 A. Right. So, for example, you say, "I want
5 a 32-bit adder," and it generates one.

6 Q. In paragraph 44 of Exhibit 14, you talk
7 about -- or strike that -- you state that, for
8 example, "sqv" -- "sq.v instantiates a texture
9 thread arbiter"; is that correct?

10 A. Yes.

11 Q. And when you say "instantiates," you mean
12 what exactly?

13 A. When you're designing in Verilog, you
14 create modules. Those modules are essentially
15 templates for a particular piece of logic. And then
16 to actually put a copy of that logic into your
17 design, you reference the module by name and create
18 an instance, and that instance then gets a name.
19 And that way you can replicate the same logic more
20 than one time.

21 And I refer to that and I think many
22 people refer to that as instantiating the module.

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1 Q. So in the context of using the Verilog in
2 a simula- -- as a simulator, it's essentially
3 creating a routine that can be called with
4 particular inputs and produce particular outputs; is
5 that correct?

6 A. I don't know if I'd call it a routine.
7 It's a -- it's an embodiment of the logic for a
8 particular logic block that can then be simulated or
9 emulated.

10 Q. How is it an embodiment?

11 A. It includes an embodiment of the design.
12 It includes the -- the logical functions of the
13 design, and it includes much of the connectivity
14 structure of the design.

15 Q. It's software -- correct? -- in the
16 context of run- -- using the Verilog as a
17 simulation?

18 A. Well, it's -- it's a hardware
19 specification that you can then simulate. In other
20 words, you don't run it one line at a time like
21 other forms of software.

22 Q. "You don't run it one line at a time."

1 Can you explain what you mean by that?

2 A. The simulation can -- can have many parts
3 of the specification running concurrently.

4 Q. Well, software can run multiple things
5 concurrently, can't it?

6 A. It can, in some forms, yes.

7 Q. Well, it's -- when you -- when
8 you -- well, strike that.

9 So you have Verilog. Physically, what do
10 I do? When I'm sitting at a computer and I want to
11 simulate the Verilog, what do I do?

12 A. I'm sure there's multiple ways to do it,
13 but the way I would normally do it is I would load
14 the design into a simulator or an emulator.
15 Generally, I would also connect it to a test bench
16 of some type that will create some stimulus signals.

17 And then I would describe what out- --
18 what signals or what outputs I would want to view.
19 And -- and then I would begin the simulation for
20 some length -- some number of simulated milliseconds
21 or some number of clock cycles.

22 Q. What do you mean by you'd connect to a

1 test bench?

2 A. Generally, you would want to simulate the
3 inputs of a system but not always. Sometimes a
4 system can be self-contained. But, for example, if
5 I were -- if I had a complete graphics chip that I
6 wanted to simulate, I might create a test bench that
7 generated the commands from the host computer to
8 make it draw a triangle.

9 Q. Is the test bench software?

10 A. It can be software, but more commonly,
11 it's also hardware description language. It's a
12 emulation of another piece of hardware.

13 Q. So it's source code, the test bench?

14 A. Usually. Although, sometimes it's just a
15 list of -- of -- of vectors. Sometimes it's just a
16 list of -- of values to be placed onto a signal,
17 depending on what the simulation environment is.

18 Q. And so when you refer to connecting the
19 test bench to the simulation, what you're talking
20 about is providing inputs from the test bench to the
21 simulator; is that correct?

22 A. Right, and since they're both essentially

1 pieces of hardware being described in a hardware
2 description language, in many cases. The reason I
3 use the word "connecting" is the way that you
4 provide them is you draw wires between the two.

5 Q. When you draw wires between the test bench
6 and the simulated hardware, you're not physically
7 creating real wires, are you?

8 A. No. You're specifying wires.

9 Q. And when you're running the simulation and
10 sq.v instantiates a texture thread arbiter, is it
11 physically creating a texture thread arbiter?

12 MR. TUMINARO: Objection to form.

13 THE WITNESS: No. It's logically creating
14 it.

15 MR. MAIER: Q. Other than the Verilog
16 source code that you have reviewed in each of the
17 declarations in which you've discussed R400 source
18 code, have you looked at any other versions of R400
19 Verilog?

20 A. Ever?

21 Q. Yes.

22 A. Yes.

1 Q. And what were the circumstances?

2 MR. TUMINARO: I'll caution the witness
3 not to disclose the substance of any attorney-client
4 communication; or if you did something at the
5 direction of counsel, I'll object on privilege to
6 the extent that it calls for that type of
7 information.

8 THE WITNESS: I didn't understand the
9 instructions.

10 MR. TUMINARO: So the question is, what
11 were the circumstances?

12 You can't -- you could talk generally
13 about circumstances, but I don't want you to
14 disclose anything that you may have done at the
15 direction of counsel or any communication you may
16 have had with counsel.

17 THE WITNESS: I reviewed them with respect
18 to another matter at the direction of counsel.

19 MR. MAIER: Q. Was that a earlier or a
20 later version of the R400 Verilog?

21 A. Both.

22 Q. Were there any differences in the

1 structures that you analyzed in this matter as
2 compared to the source code that you looked at in
3 this other matter?

4 MR. TUMINARO: I'm going to object and
5 instruct the witness not to answer on work product.

6 THE WITNESS: I've been told not to
7 answer, and I'm going to follow that direction.

8 MR. MAIER: Q. Are you familiar with --
9 I'll strike that. Paragraph 137.

10 If we turn to page 68 of Exhibit 14, and
11 I'm looking at paragraph 137. And the last sentence
12 of that states, "The R400 RTL code that performs the
13 vector and scalar operations is included in sp.v,
14 vector.v, and scalar_lut.mc (and their reference
15 modules)"; is that correct?

16 A. Yes.

17 Q. Did you review sp.v?

18 A. Yes.

19 Q. Did you review vector.v?

20 A. Yes.

21 Q. Did you pro- -- did you review
22 scalar_lut.mc?

1 A. Yes.

2 Q. And did you rely on your review of those
3 files in forming the opinion that you express here?

4 A. Yes.

5 Q. Are you aware of whether or not each of
6 these files has been produced to LG in this
7 litigation?

8 A. I don't know one way or the other.

9 Q. Did you review any files that -- any other
10 files that are not listed somewhere in your
11 declaration?

12 A. Yes. I had the complete directory for SQ,
13 SP, and TP, and I re- -- I looked at other files in
14 those directories, and if I didn't find anything
15 relevant in them, I didn't cite to them.

16 Q. And do you know if all of those files were
17 produced --

18 A. I don't know --

19 Q. -- to LG?

20 A. I don't know what was produced.

21 Q. In paragraph 34 of Exhibit 14, you state,
22 "the '053 patent pertains to the chip-circuit

1 design"; is that correct?

2 A. Yes.

3 Q. What do you mean by that?

4 A. It -- the '053 is relevant to the
5 structures and functions that would physically be on
6 a chip.

7 Q. Yesterday you mentioned a situation when
8 you were employed at S3 where you taped out a chip,
9 it came back, didn't work.

10 Do you remember that?

11 A. Yes.

12 Q. Is that uncommon in the industry for chips
13 to come back from -- after being taped out and
14 sometimes they don't work?

15 A. It's not uncommon for them to have bugs
16 where specific features of them don't work. It's
17 much more uncommon to have them be completely broken
18 like that particular chip was, that they had
19 actually just skipped a manufacturing step.

20 Q. So sometimes even though a chip design has
21 passed all the verification steps, all the automated
22 types of testing that we talked about, all of the

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1 checking against constraints and the like, you tape
2 it out, it comes back, and there are bugs; is that
3 correct?

4 A. Yeah. There are two different
5 possibilities. One is it could have been
6 manufactured wrong, in which case you just do it
7 again, or there could be things that were untested
8 or improperly tested.

9 Q. And when that happens, the -- the latter
10 case, something wasn't accounted for, something
11 wasn't properly modeled, something wasn't properly
12 tested, what happens?

13 A. Engineers figure out what the error was,
14 and they either physically modify the chip, or they
15 go back and change the design and remanufacture it.
16 Or sometimes they ship it as is with -- with bugs
17 and use software to get around it or don't use a
18 particular feature.

19 Q. And all of that can happen even though
20 initially the -- the RTL verified as working; is
21 that correct?

22 A. Well, that's the point, is it doesn't

1 verify as working. It's -- it's pretty much
2 provably impossible to fully test the functionality
3 of a chip. So specific functionality gets tested;
4 and usually, that specific functionality will work
5 in the manufactured chip, but there's usually
6 something else that nobody thought to test, because
7 it was less important, that doesn't work.

8 Q. Is it possible that a chip which has had a
9 particular function logically tested -- so, in other
10 words, the RTL is tested to make sure that logically
11 it performs properly -- and yet due to physical
12 effects that weren't properly modeled, were other
13 manufacturing tolerances that were unexpected, that
14 the chip comes back and that logic function doesn't
15 work?

16 MR. TUMINARO: Objection to form.

17 THE WITNESS: It's possible. ATI uses a
18 design style called fully synchronous design that is
19 intended to make that kind of a situation extremely
20 unlikely. But -- but it's possible that somebody
21 could have made a mistake along the line.

22 MR. MAIER: Q. So even in fully

1 synchronous designs, for example, if someone fails
2 to -- if someone -- yesterday you talked about a
3 capacitance extraction or parasitics extraction.

4 If someone fails to account for, for
5 example, crosstalk, which my understanding is, at
6 the time, was not something that was commonly
7 referred -- commonly tested for or modeled, the chip
8 might not work even though logically it verifies;
9 isn't that correct?

10 MR. TUMINARO: Objection to form.

11 THE WITNESS: It's possible.

12 MR. MAIER: Q. In fact, that happened to
13 some manufacturers in that time period; isn't that
14 true?

15 A. Not that I'm aware of, but it could have.

16 Q. Yesterday we talked about Exponential
17 Technology.

18 Are you aware of their X704 chip?

19 A. That was much earlier. Exponential folded
20 before, I think, in early '99.

21 Q. Sure.

22 I'm just asking, are you aware of that

1 chip?

2 A. I'm aware of its existence.

3 Q. When is -- what is your understanding of
4 when crosstalk started to be modeled by commercial
5 static timing analysis tools?

6 A. I don't know. I think it was in the early
7 2000s.

8 MR. MAIER: I think this would be a good
9 time for a break. I think I'm probably done, but
10 I'd like to chat with my colleague and make sure.
11 And then we'll reconvene, if that's okay with you
12 guys.

13 MR. TUMINARO: Sure.

14 THE VIDEOGRAPHER: Okay. We are off the
15 record at 10:17.

16 (Recess taken.)

17 THE VIDEOGRAPHER: We are now on the
18 record at 10:24.

19 MR. MAIER: Well, welcome back.

20 At this time, I don't have any more
21 questions; however, I'm going to hold the deposition
22 open because it appears there's some documents that

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1 might -- that were relied on that have not been
2 produced, some Verilog files. And pending a
3 resolution of that, we're going to hold the
4 deposition open.

5 But for now, it's your turn.

6 MR. TUMINARO: Well, I have no questions.

7 MR. MAIER: Well, in that case, we're
8 done.

9 THE WITNESS: Thank you.

10 THE VIDEOGRAPHER: Okay. This is the end
11 of Video 1 of 1 in Volume II and concludes
12 Volume II. The master videos of Volume I and II
13 will be retained by Digital Evidence Group.

14 We are now off the record. The time is
15 10:25.

16 (Deposition adjourned at 10:25 a.m.)

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2
3 I, MICHELLE D. KNOWLES, a Certified
4 Shorthand Reporter, hereby certify that the witness
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Dated: November 16, 2015



MICHELLE D. KNOWLES, CSR No. 8979

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1 Andrew Wolfe c/o
2 STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
3 1100 New York Avenue, NW
4 Washington, DC 20005
5

6 Case: LG Electronics, Inc. v. ATI Technologies ULC
7 Date of deposition: November 10, 2015
8 Deponent: Andrew Wolfe
9

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