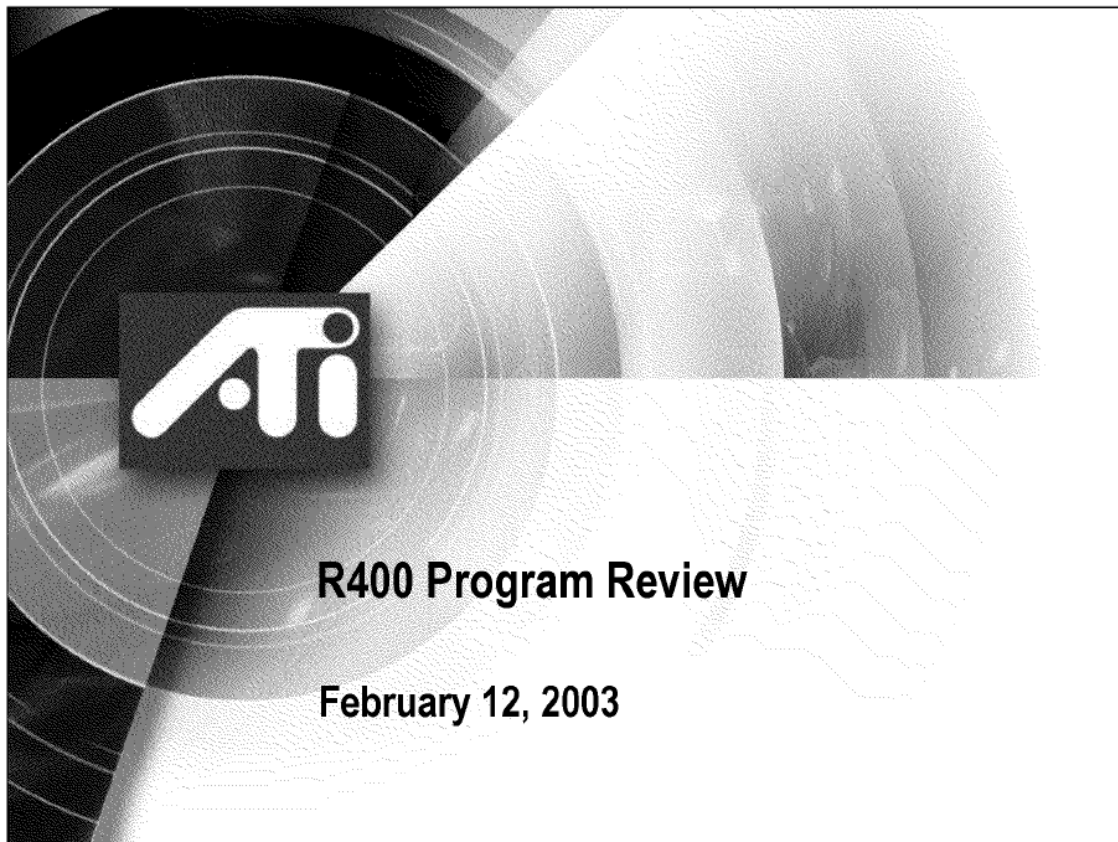




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R400 Review Action Summary

- Program – Next tentative review date is on March 12th

- Last Month

- R400 Software

- Plan support for packet dump capture – Complete
 - Quality goal needed for conformance of compression/coherency code - Open
 - IKOS Meeting with Ron White for SW – Complete

- R400 Hardware

- SDR 3.3V support on DVO port (requirements) – Closing, finalizing
 - RB break-up for Netlist delivery (NL4.0 vs NL5.0) – Planned for NL5
 - Code coverage analysis on all blocks – In process
 - DC dependency on MH bugs - Ken Correll focused on support
 - DC instance count – Instance count reduced, discussing with Mark Lee
 - SQ test coverage review – Complete

- Performance

- PA performance registers – Complete
 - GC testbench for better performance data – Not working yet, still debugging
 - Contractors to run/analyze tests – Ko Yu, Allen G. will pursue as necessary

- Chip Integration

- Power – Greg S. analyzing power
 - Operations – Update meeting held with Anita Siu, working fuse process
 - Pad – Review scheduled for end of February

- Physical Design

- Feedback from Netlist 3 needed – Mark Lee began, PD/LD meetings in process

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R400 Review Action Summary

- **This review**

- **R400 Software**

- Quality goal needed for conformance of compression/coherency code - **Open**
 - Is HW testing using Set_state or Type0 packets in tests – Mark Fowler
 - SW ran into problem recently

- **R400 Hardware**

- RB split for netlist 5 – Frank Hering
 - AB file dumps – Mike Mantor / Larry Seiler
 - Remove degamma from DXTC as a feature ?
 - Code coverage analysis on blocks – Mark Fowler
 - TC performance path – Steve Morein / Clay Taylor / Andy Gruber
 - DC instance count high – Lili S./Frank H. to close with Mark Lee
 - Assist with debug of 2D tests – Mark Earl / John Carey / Harry Wise
 - SQ/SX has risk, continue to monitor – Peter Pellerite
 - Review CP code
 - Rewrite of 2D Drivers for derivative area savings – Joe Cox
 - CP code removed, need to review – Andy Gruber / John Carey

- **Performance**

- Orlando to work more with playback – Chris Gray / Allen G.
 - GC testbench for better performance data – **Open**

- **Chip Integration**

- Thermal solution need overall owner
 - Boards group involvement priority (or window is lost)
 - Operations – give memory/fuse package to Anita for ASE
 - Pad – clock distribution in pads needs to be finalized with SiV

- **Physical Design**

- BIF description for R400 PD – Lili Sinclair
 - PD to LD communication mostly working (may need to expand/change list)
 - Clock insertion methodology – meeting 2/14

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High Level Schedule

Task	Original	Last FC	Current FC
Emulator Test template Complete	01-18-02	01-18-02	Complete
GC Emulator integration – 1 triangle	02-22-02	02-21-02	Complete
Core Emulator pixel / shader tests run	03-15-02	03-19-02	Complete
Block Testing Begins	04-16-02	05-01-02	Complete
GC/Chip Integration Start	05-17-02	05-15-02	Complete
Simulate 1 Triangle / Emulator ready for SW	06-15-02	07-01-02	Complete
First Syntheses (n-1)	07-12-02	08-03-02	Complete
Verilog Feature Complete	09-16-02	10-31-02	Complete
Second Synthesis (n)	09-23-02	10-04-02	Complete
IKOS Emulation start	10-11-02	01-13-03	Complete
Third Synthesis	11-01-02	01-02-03	Complete
Early block delivery starts	11-08-02	12-16-02	Complete
Netlist 4.0	02-14-03	02-07-03	02-12-03
Netlist 5.0	03-03-03	03-03-03	03-03-03
IKOS Emulation (w/ Software) begins	11-11-02	01-16-02	03-16-03
RTL Freeze / Final Netlist (Gate level ECO only)	11-15-02	01-31-03	05-01-03
A11 Base Layers Tapeout	01-10-03	03-28-03	06-26-03
A11 Metal Layers Tapeout	01-24-03	04-11-03	07-10-03
First Samples for Engineering		06-25-03	09-12-03
R400 First Customer Samples		07-16-03	10-03-03
A12 Tapeout		07-31-03	10-17-03
A12 Samples for Engineering		09-04-03	11-28-03
R400 Customer Samples		09-11-03	12-05-03
Product Delivery		10-04-03	12-29-03

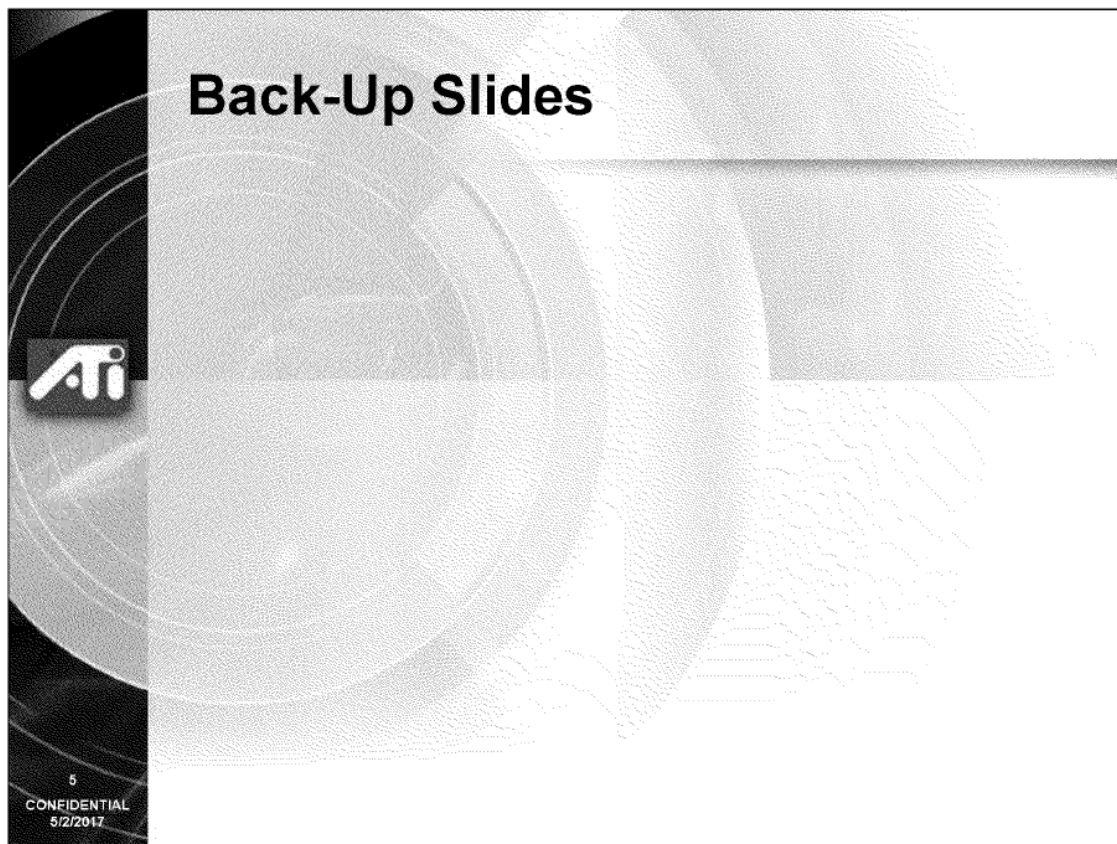
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R400 Area Summary (2/09/03)

R400 Area Estimate (0.13)

Block	Pre Route Logic Area	Utilization	Post Route Logic Unit Area	Macro Area	Total Unit Area	R400 Qty	R400 Total	RV400 Qty	RV400 Total	Synthesis Date
BIF (Bus Interface)	1,319,516	0.70	1,885,023	0	1,885,023	1	1,885,023	1.00	1,885,023	1/29/2003 1%
DC (Display Controller)	6,330,003	0.70	9,042,862	2,155,268	11,198,128	1	11,198,128	1.00	11,198,128	2/1/2003 5%
VIP (Video In Port)		0.70				1	0	1.00	0	2/1/2003 0%
SI (Clock Gen, TST, DBG, ROM)	222,069	0.70	317,242	0	317,242	1	317,242	1.00	317,242	2/4/2003 0%
CP (Control Processor)	2,433,753	0.70	3,478,790	1,586,958	5,065,748	1	5,065,748	1.00	5,065,748	2/7/2003 2%
RBMM (Register Backbone Manager)	146,901	0.70	209,988	162,392	372,379	1	372,379	1.00	372,379	1/29/2003 0%
MM (Memory Hub)	5,393,979	0.70	7,705,541	1,270,941	8,976,482	1	8,976,482	0.75	6,732,362	2/8/2003 4%
IDCT	1,228,255	0.70	1,756,079	0	1,756,079	1	1,756,079	1.00	1,756,079	1/30/2003 1%
VGT (Vertex Group and Tessellate)	753,077	0.70	1,075,824	463,907	1,539,731	1	1,539,731	1.00	1,539,731	1/28/2003 1%
PA (Viewport Xform, Clip and Setup)	3,155,429	0.70	4,507,756	1,349,122	5,856,878	1	5,856,878	1.00	5,856,878	1/28/2003 3%
SC (Scan Converter)	3,281,784	0.70	4,688,263	1,088,714	5,786,977	1	5,786,977	1.00	5,786,977	1/28/2003 3%
SC_B (Scan Converter)	3,483,305	0.70	4,976,150	0	4,976,150	1	4,976,150	1.00	4,976,150	1/28/2003 2%
SP (Shader Pipe)	7,143,861	0.70	10,205,236	2,724,847	12,929,877	4	51,719,508	2.00	25,659,754	2/5/2003 24%
SQ (Sequencer)	1,851,753	0.70	2,616,790	3,686,854	6,293,645	1	6,293,645	1.00	6,293,645	2/7/2003 3%
TP (Texture Pipe)	2,977,446	0.70	4,110,637	889,007	4,779,644	4	19,118,577	2.00	9,559,289	2/5/2003 9%
TC - TCF (Texture Fetch)	2,067,420	0.70	2,853,457	552,886	3,606,343	1	3,606,343	0.60	2,103,686	2/7/2003 2%
TC - TCM (Texture Memory)	3,358,348	0.70	4,799,069	2,496,368	7,295,437	1	7,295,437	0.60	4,377,262	2/5/2003 3%
TC - TCR (Texture Return)	3,488,817	0.70	4,685,453	1,043,284	6,028,737	1	6,028,737	0.60	3,617,242	2/8/2003 3%
RB (Render Backend)	7,086,140	0.70	10,123,058	1,583,484	11,706,542	4	46,826,167	2.00	23,413,084	2/8/2003 21%
AB (Alpha Blend)	1,780,887	0.70	2,558,124	0	2,558,124	4	10,232,497	2.00	5,116,249	2/7/2003 5%
RC (Render Central)	165,001	0.70	264,287	0	264,287	1	264,287	1.00	264,287	1/27/2003 0%
SX (Shader Export)	1,258,829	0.70	1,798,042	2,307,229	4,105,271	2	8,210,541	1.00	4,105,271	2/8/2003 4%
MC (Memory Controller)	412,438	0.70	589,197	538,583	1,127,779	4	4,511,117	2.00	2,255,559	1/28/2003 2%
Analog + DFT							8,534,500		7,932,191	12/31/2002 3%
Total Core (um²)							218,259,974		140,372,214	100%

Current Pad separation (um)	60		
Current Pad height (um)	350		
Scribe	0.18		
Core mm ² /side		14.77	11.85
Total mm ² /side		15.65	12.73

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