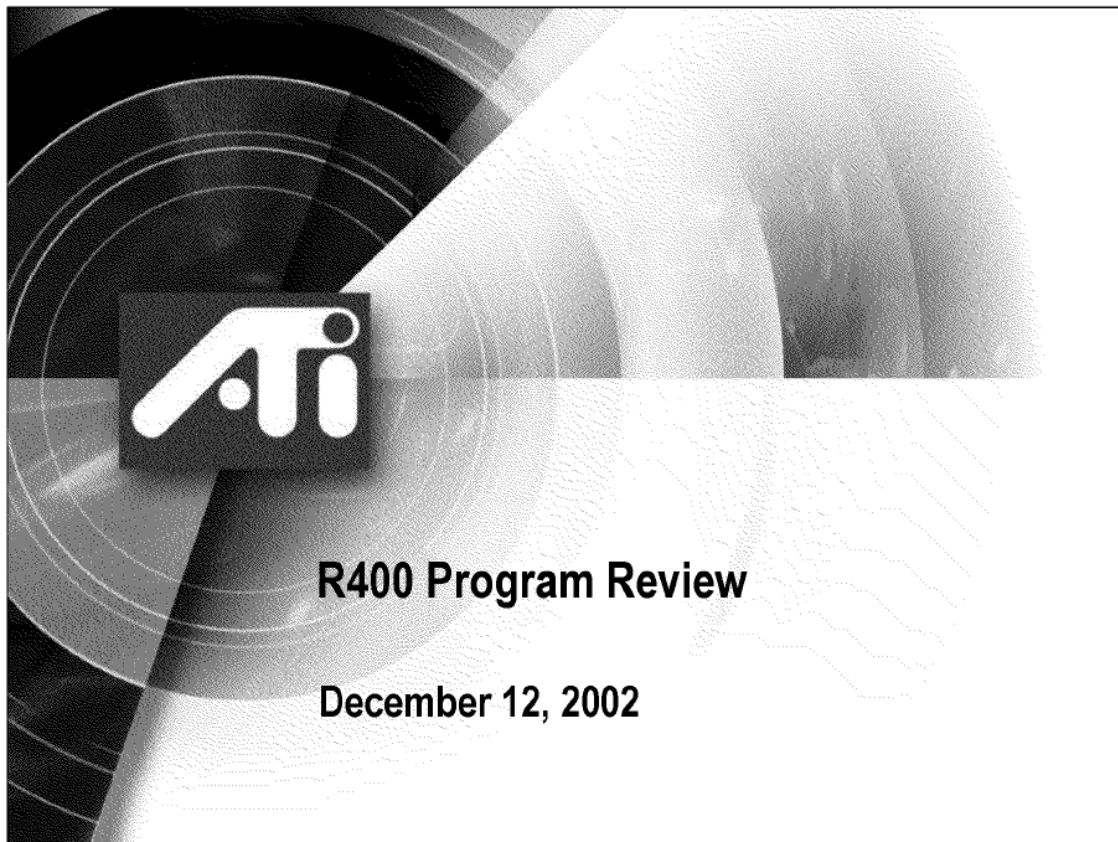




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R400 Review Action Summary

- Program – Next review on January 15th
- R400 Software
 - Emulator release tied to software tests; Peter Pellerite will set up meeting to discuss
 - AIW schedule for 1 month after graphics will not work – 3 months – Ray T. to work
 - Board VIVO closure for debug
- R400 Hardware
 - DDR DVO at 480MHz needs to drop 3.3V Support, 2.5V maximum, 1.8V standard; Ray T. to call meeting
 - SP will need to add larger buffer – Add now ? Need to discuss asap and decide. Peter Pellerite to call meeting.
 - Need generic fix to scripts for timing fix ? Mark Sprague
- Chip Integration
 - Power issues with latest memories (4x higher) - need to figure out issue
 - Need operations involved on Virage fuses, harvesting fuse
 - Pad ring coordination meeting with Sam, Lili, Frank
- Physical Design
 - Feedback from Netlist 3 – Mark Lee
- Performance
 - RTL to IKOS ? Frank Hering

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High Level Schedule

Task	Original	Last FC	Current FC
Emulator Test template Complete	01-18-02	01-18-02	Complete
GC Emulator integration – 1 triangle	02-22-02	02-21-02	Complete
Core Emulator pixel / shader tests run	03-15-02	03-19-02	Complete
Block Testing Begins	04-16-02	05-01-02	Complete
GC/Chip Integration Start	05-17-02	05-15-02	Complete
Simulate 1 Triangle / Emulator ready for SW	06-15-02	07-01-02	Complete
First Syntheses (n-1)	07-12-02	08-03-03	Complete
Verilog Feature Complete	09-16-02	10-31-02	Complete
Second Synthesis (n)	09-23-02	10-04-02	Complete
IKOS Emulation start	10-11-02	11-15-02	01-04-02
Third Synthesis	11-01-02	11-15-02	12-18-02
Early block delivery begins	11-08-02	11-18-02	12-16-02
IKOS Emulation (w/ Software) begins	11-11-02	12-16-02	01-16-02
RTL Freeze / Final Netlist (Gate level ECO only)	11-15-02	01-31-03	01-31-03
A11 Base Layers Tapeout	01-10-03	03-28-03	03-28-03
A11 Metal Layers Tapeout	01-24-03	04-11-03	04-11-03
First Samples for Engineering		06-25-03	06-25-03
A12 Tapeout		07-31-03	07-31-03
A12 Samples for Engineering		09-04-03	09-04-03
R400 Customer Samples		09-11-03	09-11-03
Product Delivery		10-04-03	10-04-03

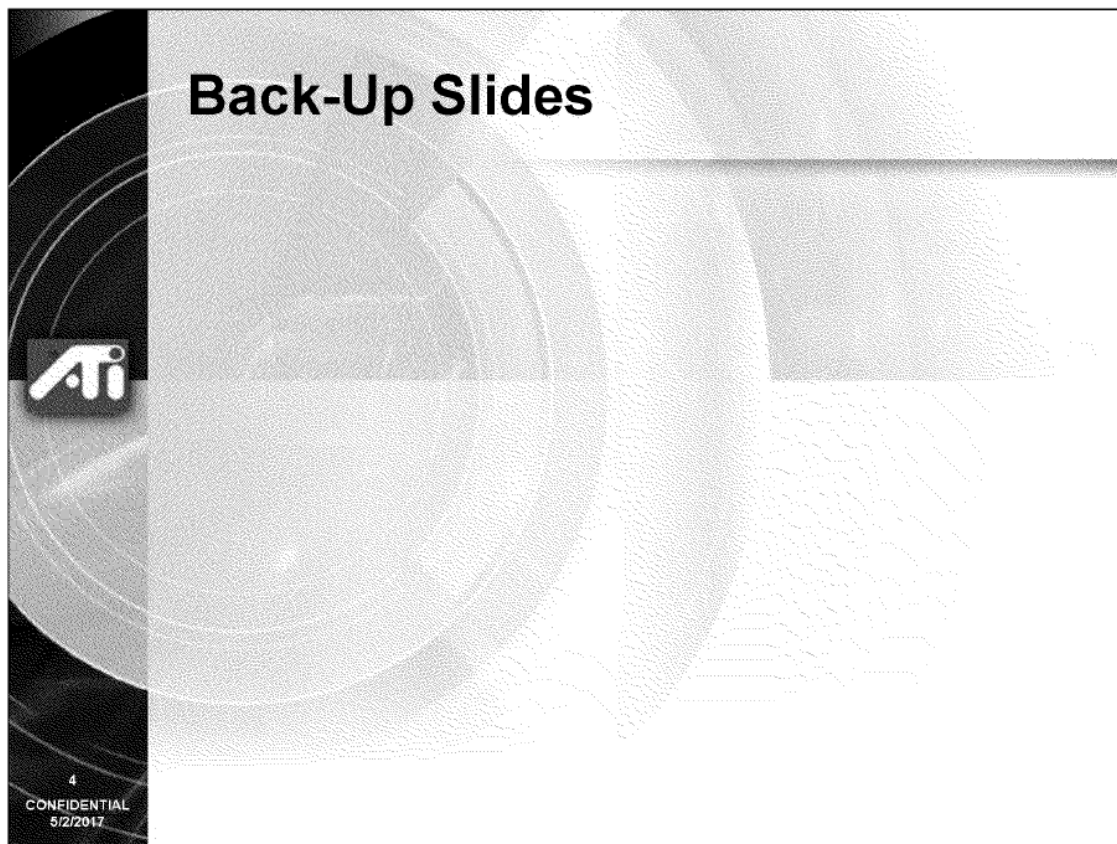
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R400 Area Summary (Previous)

R400 Area Estimate (0.13)

Block	Pre Route Logic Area	Utilization	Post Route Logic Unit Area	Micro Area	Total Unit Area	R400 Qty	R400 Total	RV400 Qty	RV400 Total
BIF (Bus Interface)	148,037	0.70	2,116,009	0	2,116,009	1	2,116,009	0.00	2,116,009
DC (Display Controller)	5,348,478	0.70	7,642,111	1,754,490	9,396,601	1	9,396,601	1.00	9,396,601
VIP (Video In Port)	0	0.70	0	0	0	1	0	1.00	0
CG (Clock Gen)	123,883	0.70	176,976	0	176,976	1	176,976	1.00	176,976
ROM (ROM and debug controller)	73,107	0.70	104,439	0	104,439	1	104,439	1.00	104,439
TSTC (Test Controller)	9,600	0.70	13,714	0	13,714	1	13,714	1.00	13,714
CP (Control Processor)	2,795,951	0.70	3,994,216	1,563,982	5,547,297	1	5,547,297	1.00	5,547,297
RBBM (Register Backdoor Manager)	103,059	0.70	147,228	91,462	238,690	1	238,690	1.00	238,690
MH (Memory Hub)	3,934,344	0.70	5,620,482	908,915	6,529,407	1	6,529,407	0.75	4,897,055
IDCT	1,200,396	0.70	1,714,852	0	1,714,852	1	1,714,852	1.00	1,714,852
VGT (Vertex Group and Tessellate)	756,947	0.70	1,061,210	340,919	1,402,128	1	1,402,128	1.00	1,402,128
PA (Viewport Xform, Clip and Setup)	2,783,577	0.70	3,976,538	755,252	4,731,790	1	4,731,790	1.00	4,731,790
SC (Scan Converter)	7,203,312	0.70	10,290,446	634,893	10,925,339	1	10,925,339	0.60	6,555,083
SP (Shader Pipe)	6,054,940	0.70	8,649,915	2,413,711	11,063,625	4	44,254,501	2.00	22,127,251
SG (Sequences)	1,648,958	0.70	2,355,654	2,333,798	4,689,452	1	4,689,452	1.00	4,689,452
TP (Texture Pipe)	2,305,274	0.70	3,293,249	596,969	3,890,218	4	15,560,950	2.00	7,780,475
TC (Texture Cache)	11,342,989	0.70	16,261,286	3,755,397	20,016,682	1	20,016,682	0.60	12,010,009
RB (Render Backend)	6,971,479	0.70	9,950,250	1,167,919	11,118,275	4	44,505,101	2.00	22,252,551
RC (Render Central)	151,388	0.70	216,268	0	216,268	1	216,268	1.00	216,268
SX (Shader Export)	702,959	0.70	1,004,228	2,048,405	3,052,633	2	6,105,266	1.00	3,052,633
MC (Memory Controller)	351,689	0.70	502,413	445,311	947,725	4	3,790,908	2.00	1,895,449
Analogy							5,456,740		7,518,980
Total Core (um2)							187,521,491		118,465,893

Current Pad separation (um)	50	17,087,057	
Current Pad height (um)	350		
Scribe	0.18		
Core minxside		13.69	10.88
Total minxside		14.57	11.76

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