



ATI Corporate Presentation

AMD1044_0170987

ATI Ex. 2033
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Target Milestones in Last Month

- **R400 Program Milestones**

- Whole chip code freeze by 11/23

- **Toronto R400 revised milestones**

- Achieve 100% passing in block regression by 12/13 with tvout being 1/6.
- Start IKOS debug 12/20.
- Achieve revised timing goals by 12/30.
- Achieve 50% regression passing in chip by 12/30, 100% by 1/30.
- Start Gate level simulation in Jan.
- Complete system tests & debugged by 1/30
- Deliver final netlist 1/30.



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What Have We Achieved

• Status Summary

- ✓ Achieved 100% passing on block level regression on Dec 30 with the exception of tvout and bif
- ✓ Achieved over 50% passing on chip level regression on Dec 30
- ✓ PCI configuration cycles passed on IKOS validation on netlist 2.0
- ✓ System tests are on track to be delivered & debugged
- ✓ Emulation work in bif & tvout are on track. The completion dates are Jan 24 for tvout and Feb 7 for bif
- ✓ Synthesis timing/area closure is in progress
- ✓ Deliver IDCT final netlist on Jan 24

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What Have We Achieved (specs, coding, emulation, tests)

- Coding is 100% complete with 2% outstanding in BIF (agg 64byte write & perf counter).
- Emulation is 100% completed with vga (tilde mem dump) and bif.
- Tests are 100% released with lb, tvout, bif & system outstanding, covering RT, hdtv, bif changes.

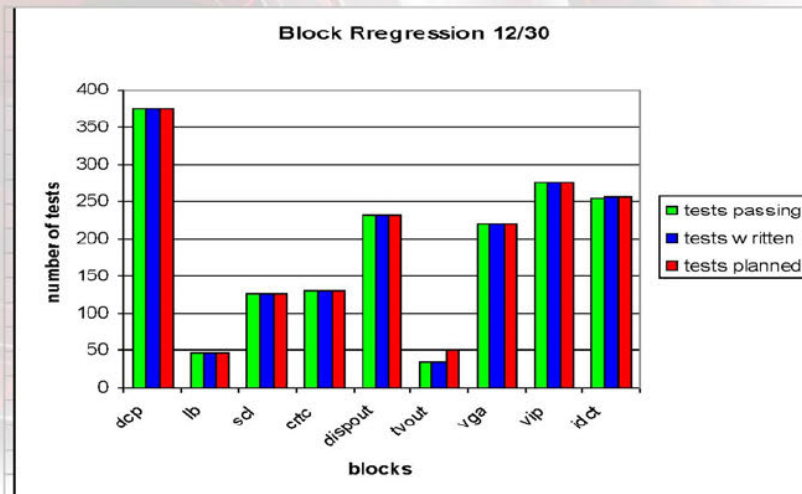
Design		RTL specs	RTL coding	Emulation	Tests Written
display	dcp	100%	100%	100%	100%
	lb	100%	100%	100%	98%
	scl	100%	100%	100%	100%
	crtc	100%	100%	100%	100%
	dispout	100%	100%	100%	100%
	tvout	100%	100%	100%	80%
vga		100%	100%	99%	100%
vip		100%	100%	100%	100%
BIF		96%	98%	90%	50%
IDCT		100%	100%	100%	100%
system					35%

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What Have We Achieved (block RTL regression)

- All blocks are 100% passing
- Tcout reached 80% passing and plan to complete by Jan24

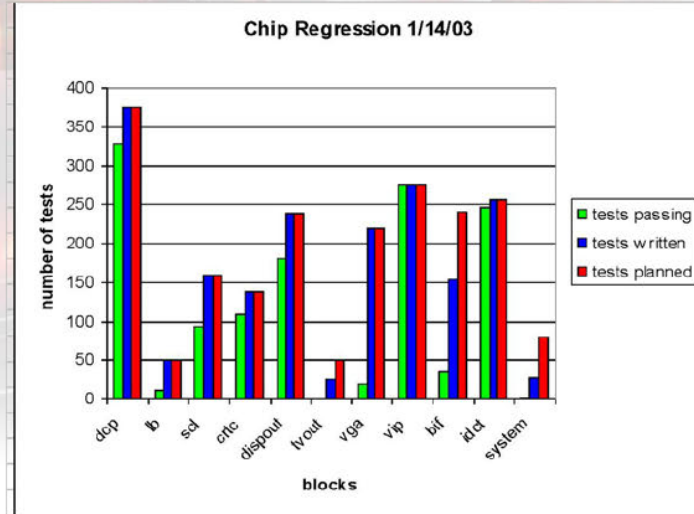


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What Have We Achieved (Chip regression)

- Overall 68% passed on chip level with VIP 100% & IDCT 96%
- Dcp, scl, crtc, dispout all have above 60% passing. The failing 40% was due to DC-MH interface bugs.
- Vga is gated by tiled memory dump while bif is catching up.



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What Have We Achieved (Chip regression emulation)

- Most blocks are 100% passing
- Tvout & vga plan to complete by Jan 24
- Bif plan to complete by Feb 15

Design	Chip emu regress	Tests passing	Tests Released	Tests Planned
dcp	100%	375	375	375
lb	100%	47	47	47
scl	85%	135	159	159
crtc	100%	131	131	131
dispout	100%	232	232	232
tvout	0%	0	0	50
vga	59%	130	171	220
vip	100%	275	275	275
DC		1325	1390	1489
BIF	83%	200	153	240
IDCT	96%	246	256	256
System	0%	0	0	80
Total	86%	1771	1799	2065

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What Have We Achieved (Area & Timing)

- More efforts are in place to close timing and area issues.
- IDCT to close by Jan 24
- Most violations in DC should be fixed through a number of iterations of synthesis. DC still have some violations caused by improper constraints. The area goal is 7mm2.
- BIF's timing issue are due to design changes and they are in review to be updated.

DC			BIF		
Area (mm2)	8.4		Area (mm2)	1.63	
Cell Count	392K		Cell Count	163K	
Timing			Timing		
Path Groups	Speed (ns)	Violation (ns)	Path Groups	Speed (ns)	Violation (ns)
PCLK_CRTC1	2.5	-0.05	SCLK_G_BIF	2.25	-0.58
PCLK_CRTC2	2.5	-0.10	AGPCLK	3.5	0
SCLK_G_DCP	2.25	-0.35	BCLK	14	0
SCLK_G_SCL1	2.25	-0.27			
SCLK_G_SCL2	2.25	-0.27	IDCT		
SCLK_G_VGA	2.25	-1.34	Area (mm2)	1.23	
SCLK_G_VIP	2.25	-0.01	Cell Count	72K	
SCLK_M	2.25	-0.11	Timing		
SCLK_P_DC	2.25	-1.33	Path Groups	Speed (ns)	Violation (ns)
SCLK_R_DISP	2.25	-1.61	SCLK_G_DCT	2.25	-0.16
SCLK_R_TVOUT	2.25	-0.04			
SCLK_R_VIP	2.25	-0.67			

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What's ahead?

Next Set of Goals:

- Deliver IDCT final netlist by Jan 24
- Achieve DC 100% passing in chip level regression by Jan 30
- IKOS validation on netlist 3.0.
- Achieve DC timing goals by Jan 30.
- Deliver DC final netlist by Feb 15.
- Start Gate level simulation in Jan.
- Close bif timing & existing tests issues by 1/30.
- Deliver BIF final netlists by Feb 28

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Issues

Chip level regression:

- 7 MH related bugs reported for last 2 weeks
 - 5 hardware issues to be fixed & released
 - 2 emulation issues(vga rotation) to be fixed
- 4 BIF related emulator bugs reported
 - 1 due to dma hang resolved
 - 3 others related to FB_START, HDP_FB_START, APÉR_CNTL to be resolved
- DVO pad
 - Recommended mem pad doesn't support SDR mode
 - Can we drop 3.3V support?

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Risks

- MH bug fixes has been the bottleneck for chip regression.
 - Need Marlboro MH team to increase their priority in resolving these issues
- Marlboro's RTL code releasing process has been ranging from 2 to 5 days before it get released.
 - This is critical in resolving chip issues quickly.
 - Currently, DC progress is being slow down on chip regression.
- The next step is to get IKOS running with display
 - This again require MH/MC issues and bugs to be resolved
- Area reduction plan may have schedule impact

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