



ATI TECHNOLOGIES INC.

**R400 PD**

**August 29, 2002**



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# R400 PD Team

## Goals

- Schedule, schedule, schedule, schedule, ...
- Reuse Flow: better floorplan, reduce # of tiles, put tiles on the shelf earlier...

## Staffing

- Ed C (owns PD schedule)
- Joe G (owns front-end Marlboro `Link')
- Dedicated PD team (separate teams for RV350 & R350 Re-spin's & SB300)
  - Experienced R400 PD team (15 total)
    - 2 ATI on R400 now
    - 8 ATI roll over from RV350 (9) PD team
    - 5 Contractors (Nova & Spike) & ATI



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# Flow/Tools

- Leverage RV350 flow/tools
  - PhysOpt for Placement Engine
  - Clockwise for Clock Tree Generation
  - Celtic for Signal Integrity analysis
  - Voltage Storm for IR analysis



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# Netlist Handoff's

## 1<sup>st</sup> Netlist

- Netlist quality good enough so initial floorplan work not wasted
- Rough pad ring and analog macro placement in place.
- Clock structure in place, with some documentation
- Reasonable top level constraints
- Need libraries in-place (e.g., preliminary lef's of all netlist components)

## Deliverable from Marlboro

- 1<sup>st</sup> SPC pass floor-plan (Marlboro lead, SVC CAD support)



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# Netlist Cont'd

N+1 to 95% Netlist

## Deliverable from Marlboro

- \* 95% netlist, meeting pre-layout timing w/ slack
- \* Powercompiler, pipeline flops, and any special netlist all in place.
- \* Fullchip constraints (SDC) w/ false/multi-cycle paths
- \* Synthesis frozen for new features. Bug fixes only.
- \* DFT near final, with final documentation.
- \* Clock structure near final, with final documentation, including fullchip clock diagram.
- \* SPC floorplan with valid superblocks identified (good pin count, < 300K instances, 70% initial utilization)
- \* Replicable blocks identified.
- \* PAD ring in place, with replication in mind.



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# Netlist Cont'd

N+1 to 95% Netlist

## SVC Responsibility

- \* Execute and create real floor-plan, with superblocks, and toplevel.

- \* Create constraints for the superblocks

- \* Implement real powergrid, including SRAM power strategy

- \* Iterate to find best SRAM placements.

- \* Iterate to find best analog macro placements

- \* Execute PD flow for all unique superblocks, provide feedback on routability and timing

- \* Execute PD flow for toplevel, provide feedback for timing



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# Netlist Cont'd

## Final Netlist

### Deliverable from Marlboro

- \* Final netlist
- \* All bug fixes by ECO only or as requested by SVC
- \* Final padding



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# Netlist Cont'd

## Final Netlist

### SVC Responsibility

- \* Iterate to get routability/good timing on all superblocks
- \* Execute and create real floor-plan, with superblocks, and toplevel.
- \* Create constraints for the superblocks.
- \* Implement real powergrid, including SRAM power strategy.
- \* Finalize SRAM placements.
- \* Finalize analog macro placements.
- \* Execute PD flow for all unique superblocks, provide feedback on routability and timing.
- \* Execute PD flow for toplevel, provide feedback for timing.



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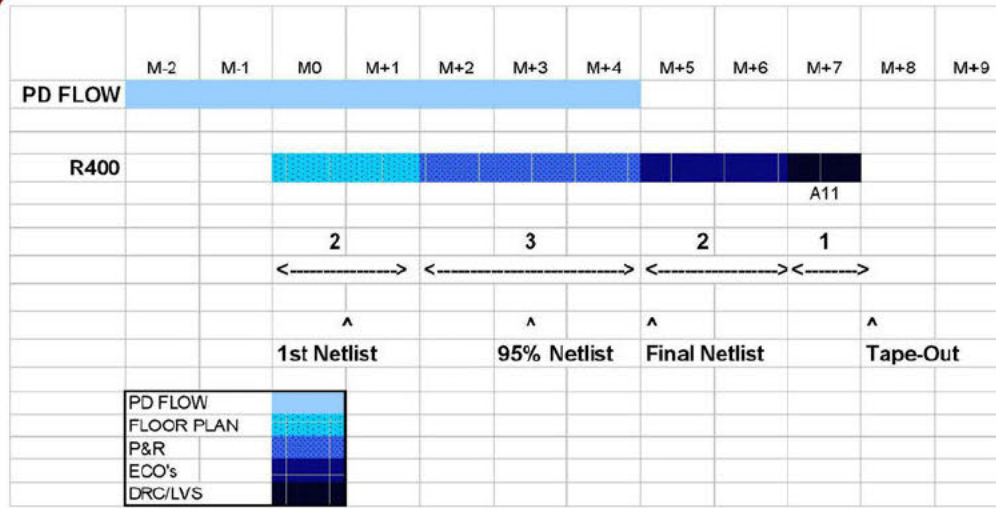
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# R400 PD Schedule



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