

I/O Pads

- Silicon Valley has committed to creating the pads and the pad ring for R400
 - Pads will be based off of RV350 pads
 - Memory pads will have to be modified to support DDR3
 - R400 has 664 signals and using the $80\mu \times 350\mu$ pad pitch yields a pad limited die of 13.98 mm
 - This does not include any power, ground, transition, or bonding pads that are needed

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I/O Pad Schedule

- Initial verilog delivery for pads and near pad logic - Rv350 based model 8/16
- Initial LEF, TLF, Synopsys models - Rv350 based model 8/16
- Initial IKOS and Sunrise models 9/1
- Final verilog delivery for pads and near pad logic - 11/1 R400 specific
- Final LEF, TLF, Synopsys models - 12/1
- Final IKOS and Sunrise models - 12/1
- Clean GDS of individual cells - 12/21
- Clean GDS of entire ring - 1/1
- Integrate ring into full chip and start full chip DRC/LVS -1/15

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Chip Integration

- Rom Controller/CG/CGM/Debug Bus:
 - Block Testing Completed
 - Regression Test Plan Created
 - 33% of regression test completed
 - Eric is in process of bringing up full chip simulation environment to start running regressions on these items
- Pad Out
 - Initial Ball Out has been created based off of the R300 package
 - 39 X 39 will still be used, but needed to move some inner ball rings to outside for signal integrity grounds
 - Ball out is being reviewed by various groups including the board group
 - Pad out is underway

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Chip Integration

- **Modified the clock gater modules to have programmable windows**
- **Chip ID's, personality bits, harvesting bits will be defined and implemented in the next two weeks**

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Chip Level Netlist

- A full chip initial netlist was delivered 8/3
- Toronto physical design group place and routed all block based on bound boxes and delivered wireloads models.
- This uncovered a number of process issues and a design compiler issues that are being addressed
- Next major release will be at the end of September, however incremental release will take place as a result of the physical design process

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DFT – Memory and Repair

- Virage has continually slipping their deliverables and it appears what they delivered on 8/14 is not all together.
- Basically we have an assortment of pieces from various process types
- They are introducing new pieces of the memory test system.
- The Register File Compiler appear to be okay
- The High Density memory is not okay
- The Star Processor and it associated pieces only work LV
- Need to push on masking configurations
- Virage is proposing a 9/23 date to get this sorted out.

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Design for Test

- Finally starting to move resources to R400
- TetraMax versus FastScan has been completed and currently analyzing the data
- Initial Specification for test controller is complete
- Eric is going to work on the RTL for it
- Near Near Pad test logic need to specified next month
- Experiment with ILM scan insertion will take place next month.

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Concerns

- **Virage**
 - Pulling together Star System
 - Test Chip problems
 - Memory repair process
- **Many issues are not being address or only being giving lip service due to the lack of people to work them**
 - Memory Controller to Pad interface
 - Analog IP and other issues
 - DFT scan process development
 - Getting ready for physical design
 - Clocking system

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