

Design	RTL Coding	RTL regress	Gate regress	Area	Synthesis timing	Internal Worst timing	External Worst timing	Target timing	Violation
BIF	100%				SCLK				
					BCLK				
					AGPCLK				
					MCLK				
MC	95%				SCLK				
					MCLK				
HDP	100%				SCLK				
					BCLK				
VIP/ROM/I2C	100%				SCLK				
					FCP				
Display	100%				SCLK				
					PIXCLK				
					P2GCLK				
					OV0CLK				
					TMDS				
					TVOUT				
					DVOCLK				
DFT/IO	100%				NA				
System	NA				NA	NA	NA	NA	NA

Design		RTL specs	RTL coding	Emulation	Tests Written
display	dcp	100%	100%	100%	100%
	lb	100%	100%	98%	98%
	scl	100%	100%	98%	91%
	crtc	100%	100%	100%	100%
	dispout	100%	100%	100%	100%
	tvout	100%	100%	80%	50%
-----	-----	-----	-----	-----	-----
dccg		100%	100%	no emu	no tests
-----	-----	-----	-----	-----	-----
dccif		100%	100%	no emu	no tests
rbbmif		100%	100%	no emu	no tests
dmif		100%	100%	no emu	no tests
vga		100%	100%	99%	100%
vip		100%	100%	100%	100%
VideoIP(DC)					
BIF		90%	90%	90%	30%
IDCT		100%	100%	100%	100%
Total					

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Design		Clock	Area (mm2)	Area accuracy	Timing
display	dcp	2.25	2.41	100%	3.72
	lb	2.25	1.42	100%	3.25
	scl	2.25	1.39	100%	3.23
	crtc	2.25	0.25	100%	2.25
	dispout	2.25	0.67	100%	3.13
	tvout	10.00	0.93	100%	10.76
vga		2.25	0.39	100%	4.43
vip		2.25	0.49	100%	2.38
VideoIP(DC)			8.27	97%	
BIF		14.00	1.63	99%	12.39
		3.50			3.50
		2.25			2.78
IDCT		2.25	1.22	99%	2.90
Total					

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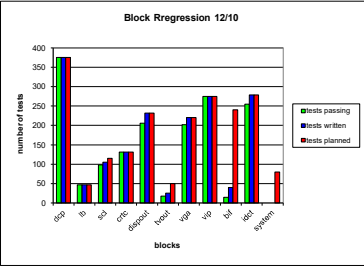
Design	features		EMU	Completed	Planned	Added
VideolP(DC)	display		100%	143	143	0
		dcp	#DIV/0!			
		lb	100%	89	89	
		scl	#DIV/0!			
		crtc				
		dispout	100%	54	54	
		tvout	#DIV/0!			
	vga					
		vip	100%	100	100	
			100%	72	72	
Subtotal			100%	458	458	0
IDCT			100%	396	396	
Total			100%	854	854	0

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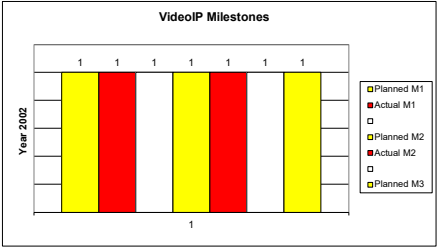
Design	features	RTL regress	Tests passing	Tests Written	Tests Planned	Tests written
VideoIP(DC)	DC					
	dcp	100%	375	375	375	100%
	ib	100%	47	47	47	100%
	scl	85%	98	105	115	91%
	crtc	100%	131	131	131	100%
	disput	89%	206	232	232	100%
	tvout	36%	18	25	50	50%
	vga	92%	202	220	220	100%
	vip	100%	275	275	275	100%
	bif	6%	15	40	240	17%
BIF	bif					
IDCT	idct	91%	255	279	279	100%
	system	0%	0	0	80	0%
Total		93%	1607	1689	1724	98%

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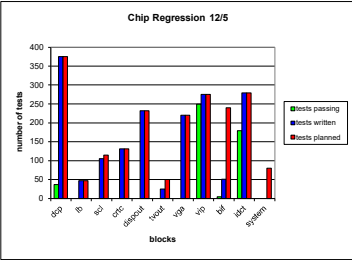
Design	features	RTL regress	Tests passing	Tests Written	Tests Planned
VideoIP(DC)	dcp	#REF!	#REF!	#REF!	#REF!
	ib	32%	57	180	202
	scl	21%	3	14	18
	crtc	38%	3	8	78
	disput	44%	15	34	50
	disput	54%	29	54	79
	disput	54%	29	54	79
	vga	65%	22	34	154
	vip	100%	270	270	275
	bif	7%	15	225	240
BIF	bif				
IDCT	idct	86%	240	279	279
IDCT	idct				
Total		63%	495	783	798

Design	features	Planned M1	Achieved M1	Planned M2	Achieved M2	Planned M2	Achieved M2	feature completion	code freeze
VideoIP(DC)	dcp	30-Apr	31-May						
	ib	30-Apr	31-May						
	scl	30-Apr	31-May						
	crtc	30-Apr	31-May						
	disput	30-Apr	31-May						
	disput	30-Apr	31-May						
	disput	30-Apr	31-May						
	vga	30-Apr	31-May						
	vip	30-Apr	31-May						
	bif	30-May							
BIF	bif								
IDCT	idct	30-May	30-Jun						
IDCT	idct	30-May	30-Jun						
Total								783	798



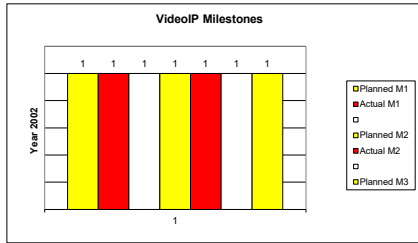
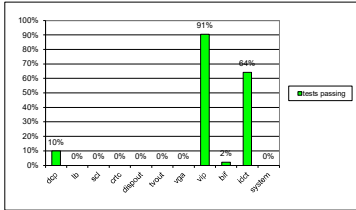
Design	features	RTL regress	Tests passing	Tests Released	Tests Planned	
VideoIP(DC)	DC					
	dcp	10%	37	375	375	100%
	lb	0%		47	47	100%
	scl	0%		105	115	91%
	crtc	0%		131	131	100%
	dispout	0%		232	232	100%
	trout	0%		25	50	50%
	vga	0%	0	220	220	100%
	vip	91%	249	275	275	100%
	bif	2%	5	51	240	21%
IDCT	idct	64%	179	279	279	100%
	system	0%	0	0	80	0%
Total		11%	184	1740	2044	

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Design	features	RTL regress	Tests passing	Tests Written	Tests Planned
VideoIP(DC)		#REF!	#REF!	#REF!	#REF!
	dcp	32%	57	180	202
	lb	21%	3	14	18
	scl	38%	3	8	78
	crtc	44%	15	34	50
	dispout	54%	29	54	79
	dispout	54%	29	54	79
	vga	65%	22	34	154
	vip	100%	270	270	275
	bif	7%	15	225	240
IDCT		86%	240	279	279
		86%	240	279	279
Total		63%	495	783	798

Design	features	Planned M1	Achieved M1	Planned M2	Achieved M2	Planned M2	Achieved M2	feature completion	code freeze
VideoIP(DC)	VideoIP(D	30-Apr	31-May	31-Jul	31-Aug	31-Oct		#REF!	#REF!
	dcp	30-Apr	31-May	31-Jul	31-Aug	31-Oct		180	202
	lb	30-Apr	31-May	31-Jul	31-Aug	31-Oct		14	18
	scl	30-Apr	31-May	31-Jul	31-Aug	31-Oct		8	78
	crtc	30-Apr	31-May	31-Jul	31-Aug	31-Oct		34	50
	dispout	30-Apr	31-May	31-Jul	31-Aug	31-Oct		54	79
	dispout	30-Apr	31-May	31-Jul	31-Aug	31-Oct		54	79
	vga	30-Apr	31-May	31-Jul	31-Aug	31-Oct		34	154
	vip	30-Apr	31-May	31-Jul	31-Aug	31-Oct		270	275
	bif	30-May						225	240
IDCT	idct	30-May	30-Jun					279	279
	idct	30-May	30-Jun					279	279
Total								783	798



			RTL	Tests	No. of	No. of
Design	features		regress	passing	tests	new tests
VideoIP(DC)	display	dcp lb scl crtc dispout	100%	143	143	0
			#DIV/0!			
			100%	89	89	
			#DIV/0!			
			100%	54	54	
	#DIV/0!					
	vga vip		100%	100	100	
			100%	72	72	
Subtotal			100%	458	458	0
BIF			100%	120	120	5
IDCT			100%	396	396	
Total			100%	974	974	5

Display/VIP/HDP/I2C/ROM	8	
Wayne Wu	100%	Team Lead
Eric Shen	100%	Display syn; syncgen, macrovision, vip
Jonathan Wang	90%	ov0scale, vcp
Nat Barbarieo	100%	subpic, i2c, rom
Merat Khabbari	100%	tvout, dvo, panel, panel2
Stephen Bagshaw	60%	hdcp, rmx
Gabriel Abarca	100%	display1, display2, hdp, cgms
Slaven	100%	vip syn; syncgen, macrovision,
CG/CGM/dispclkblk	1	
		clock generation, power management, dynamic
Nader Tavasoli	100%	clocking

MC		
Carl Mizuyabu	70%	Team Lead, architect
Desmond Wong	100%	mc syn, performance improvements
William Hui	100%	mc client interfaces
Boris Boskovic	100%	QDR IO changes
Mark Dell'Agnese	100%	MC verification
BIF		
Danny Cheung	90%	Team Lead
Gord Caruk	90%	agp fast write
Anthony Tam		bif syn & verification
DFT		
Rob Treuer	50%	Team lead
Ed Morson	50%	JTAG; scan chain
Name	100%	scan insertion(sblk1, sblk2)

IKOS functions			
	Plan	Completion	Diag plan(status) Software plan(status)
IKOS PC#1-boot up	15-Sep		
Reg r/w	22-Sep		
mem r/w	29-Sep		
bios,Display/2D	30-Oct		
IKOS PC#2-boot up,			
sdr bring up	15-Nov		
3D/AGP	30-Nov		
DDR, SDR	30-Dec		