



ATI Corporate Presentation

AMD1044_0188919

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Orlando Hardware Status

- ◆ CP / RBBM / VGT / PA / SC / SC_B 100% coded
- ◆ Gate Level simulations of all blocks started
- ◆ Synthesis / Timing improvements in process
- ◆ Real Time Streams implemented
 - Status: Passed first RTS and mixed NRTS/RTS test
- ◆ Code Coverage results being reviewed for feedback to Validation team

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Synthesis Results

BLOCK	PA	VGT	SC	SC_B	CP	RBBM
Synth Date	Dec 11, 2002	Dec 9, 2002	Dec 10, 2002	Dec 4, 2002	Dec 10, 2002	Dec 3, 2002
Code Version	N/A	N/A	N/A	N/A	N/A	N/A
Worst Timing	-0.33	-0.17	-0.14	-0.01	-0.09	-0.15
# > 1.00 nS	0**	0**	0**	0	0**	0
# > 0.50 nS	0**	0**	0**	0	0**	0
# > 0.20 nS	62**	0**	0**	0	0**	0
# > 0.00 nS	827**	440**	709**	135	160**	185
Total Neg Slack	81.1	25.7	41.0	1.3	9.2	9.1
Wireload	N/A	N/A	N/A	N/A	N/A	N/A
Cell Area (sqmm)	3.207	0.850	3.377	3.600	2.725	0.146
Macro Area (sqmm)	1.006	0.385	0.899	0.000	1.855	0.124
Total Area (sqmm)	4.213	1.235	4.276	3.600	4.580	0.271
Timing Summary link (.tsumm)	pa_tsumm	vgt_tsumm	sc_tsumm	sc_b_tsumm	cp_tsumm	rbbm_tsumm
Area Summary link (.reflog)	pa_reflog	vgt_reflog	sc_reflog	sc_b_reflog	cp_reflog	rbbm_reflog

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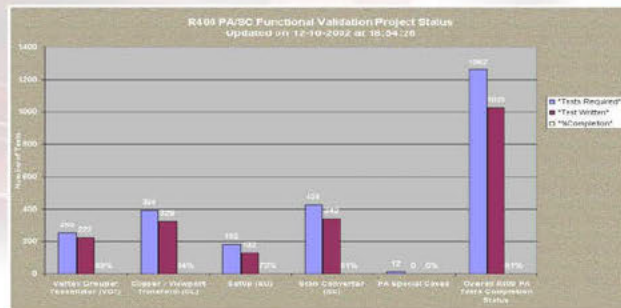
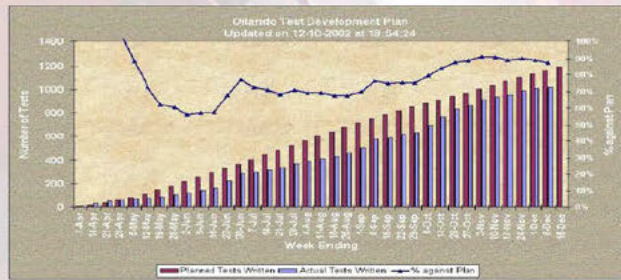
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Test Suite Development (PA, VGT, SC)



- 80% of the planned tests written
- Current suite covers 100% of planned features (awaiting cover results)
- Remaining tests are largely stress test ... expect to complete by 12/20

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Block Validation

◆ Block Level Test Regressions

Test Bench	Tests Run	Tests Pass	% Pass	Report Date
VGT	2308	2308	100%	12/09/02
CP/RBBM	902	890	98%	12/10/02
SC	2308	2198	95%	12/10/02
PA	2309	2201	95%	12/10/02

◆ Block Level Random Testing

- VGT / PA / SC Block Randoms coded & passing 100%
- PA / SC Chip Randoms passing
- VGT / CP Chip Randoms started

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Issues / Risks

- ◆ Synthesis Timing Closure (CP/RBBM/PA/VGT/SC/SC_B)
- ◆ Real-time stream validation: Checkers at GC/Full Chip level
- ◆ Block level Performance
- ◆ Integrated Performance
 - SC -> SQ/SP/SX (SP Buffer Size increase potential)
- ◆ PM4 Packet dumps needed for performance testing / and feature validation
 - 3dMark03, UT03, Doom3
- ◆ Full chip / GC validation ramping now
- ◆ Pipe Disable Validation for Quickturn
- ◆ Configuration Testing (ie ... pipe disable, one Quad/clk, walking order within tile, packer optimized, # clip controllers, fifo size, linear/tiled, clock gating)

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Chip Validation Status

- ◆ GFX (fullchip) and System (chip_vidfull) Simulations are now parts of parts_lib release mechanism ... stabilizes nightly builds
- ◆ Top level clean up activity underway
 - Force all interconnecting nets to be driven or removed
 - Connect all scan, debug, memory test signals
 - Clean up warnings on size mismatches of connecting signals
- ◆ Nightly regressions running for chip testing for GFX (Orlando) and System (Toronto) blocks
- ◆ System Test Plan drafted ... describes:
 - **BASIC SYSTEM TESTS** – these are simple initialization tests, register read/write tests, testing functionality that must be tested at the chip level (such as power, reset, clocks, scan tests, chip id test, etc ...)
 - **CONCURRENCY-STRESS TESTS** – these tests are enabling multiple engines, testing synchronization mechanisms (rts/nrts), stressing arbiters in the design.
 - **PERFORMANCE TESTS** – These tests are measure and predict performance for all areas identified in the MRD, and any performance measurements relative to me current industry standard performance applications. (see [doc_lib/verification/PV.doc](#))

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Chip Validation Status (cont'd)

- ◆ Shifting emphasis from block level validation to GC/Chip level testing
 - Orlando now has 4 engineers running / debugging chip level tests
 - Toronto increased number of chip tests being run
- ◆ Environment enhancements still in works
 - Makefile enhancements to support parameterized tests
 - Continue to add monitors / checkers at hardware interfaces to support faster chip level debugging / performance verification
- ◆ Progress is slow but steady

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Chip Validation Status (cont'd)

Orlando Full Chip Validation:

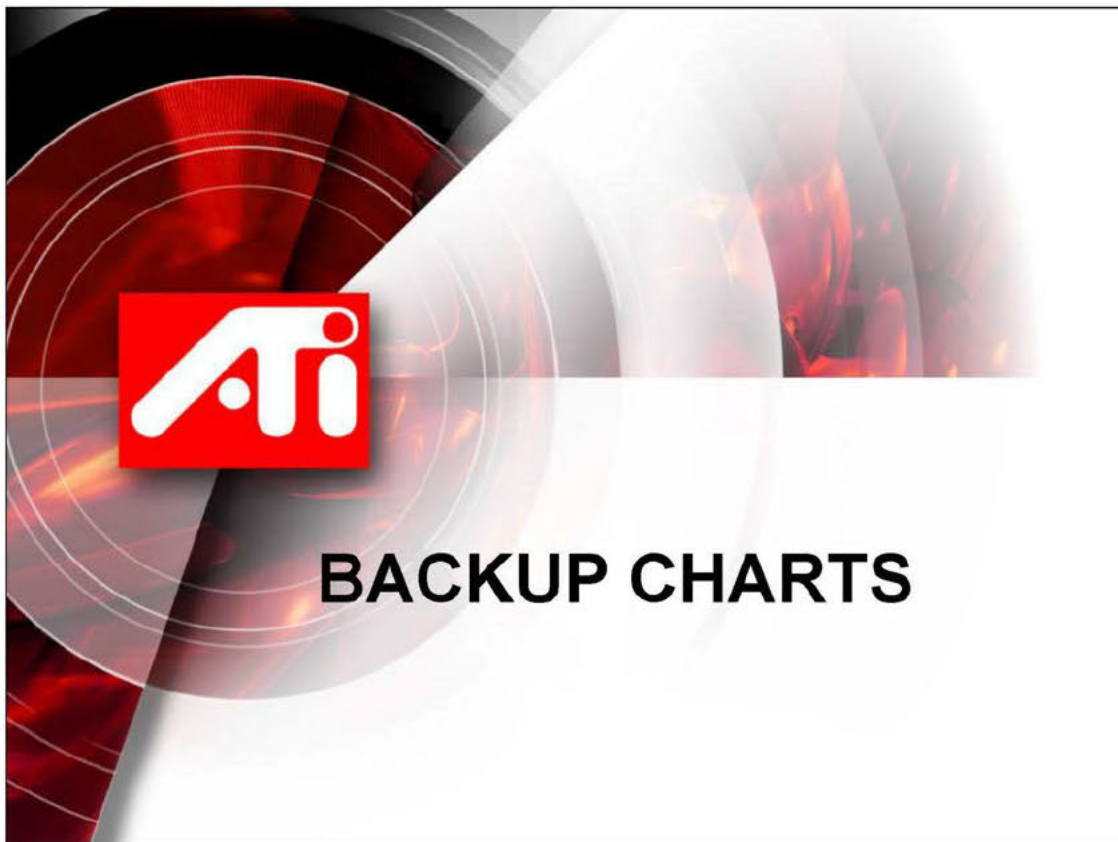
	Total Tests	Tests Written	Tests Passing	% Complete
CP	1182	785	215	28%
RBBM	100	1	1	1.00%
GFX	500	>500	2*	0.4*%

*focus on environment enhancements / build stability / clean up

Toronto Full Chip Validation

Overall Block Statistics					
TestBlock	Type	#Planned	#ExpectedRun	#Passing	(%Passing)
dcp_engine	SIM	32	32	1	(3)
dcp_graphics	SIM	50	50	36	(72)
dcp_overlay	SIM	44	44	0	(0)

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