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Emulator

- ◆ Emulator mostly feature complete and focus is on debug/test
- ◆ SQ/SP/SX
 - ◆ Closing out last few mismatches between HW/EMU in MACC and interpolator
 - ◆ SQRT tables being added in conjunction w/ HW
 - ◆ Fixing alpha test in SX
- ◆ TP/TC
 - ◆ Behind in validation of features due to transfer of resource to HW RTL debug (sw team hitting bugs before hw team)
 - ◆ Debugging DXT4/5 hang, cubic mapping, LOD correction, misc. formats
 - ◆ Updated to new LOD bias scheme (change in texture constant)
 - ◆ TC needs new degamma DXT and DXN
- ◆ RB/RC
 - ◆ Debugging depth export
 - ◆ Debugging ZPASS counter (proposed addition of event for writing counter)
 - ◆ Fixing degamma and misc. precision issues
- ◆ MC/MH
 - ◆ Debugging HDP aperture mapping

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HW Verification (directed tests)				
Block	Planned	%Written	%Running	%Passing
MC/MH	2433	98%	100%	99%
RB/RC	4000	78%	78%	97%
SP	1505	100%	100%	95%
SQ	150	97%	97%	24%
SX	45	95%	95%	71%
TP/TC	5500	85%	14%	36%

Random Validation		
Block	Running	%Passing
MC/MH	1694	32%
RB/RC (AB)	404	75%
SP (interp/MACC)	1250	73%



June 14, 2017

R400 I/O Staff

- 1 Manager (SamH)
- 3 ATI Engineers (LinC, JennH, JohnL)
- 1 Contractor Engineer (JoeN)
- 2 ATI layout designers (KarenW, KathieC)
- 2 Contractor layout designers (ChrisV, JerryB)



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[Date Time]

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R400 I/O Activities

- Memory I/O and clock design (LinC and JoeN)
- Memory near pad logic (JennH)
- Pad ring ordering/planning
 - Spreadsheet – GregS of Marlborough
 - Ring issues – SamH
- Library generation (JohnL)
- Top Level ring issues (SamH)



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Memory I/O & Clock

- LinC – memory I/O cell; JoeN – memory clock
- The idea is share over 90% of the sub circuits in both cells.
- Scheduled for first pass design complete – 1/9 most likely to be first pass design complete on 1/17 for memory I/O.
- Memory clock a week later – 1/24
- Layout for the output driver section has started and scheduled for completion on 2/15
- Initial library files (LEF, TLF, LIB, DB, and verilog) will be delivered by 1/17.



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Memory Near Pad Logic

- RTL-to-schematic implementation (JennH)
 - ADDR, DATA, and DQSM are done first pass
 - DQSS and HCLK are currently in progress
 - Schedule for completion on 2/1
- Initial library files (LEF, TLF, LIB, and DB) will be deliver on 1/17.
- Layout to start on 2/1 and complete on 3/1
- On going memory system timing – complete on 3/15



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Delay Line and misc layout

- First pass design is done (JoeN)
- ChrisV started on layout – complete on 2/1
- Miscellaneous layout
 - JerryB started on 1/14
 - PVREF
 - Corners
 - Spacers
 - Breaks
 - Complete on 3/1



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Deliverables

- 1/17
 - LEF, TLF, LIB, DB and verilog for the NPLs and memory I/O and clock
- Final LEF, TLF, LIB, DB and verilog on 3/1
- Ring DRC/LVS clean and gds delivery on 4/15



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Pull in possibilities

- Current schedule allows for a month of DRC/LVS
- We learned a lot from RV350 and since we are utilizing a lot of its cells, LVS may take less time.
- Optimistic – final clean DRC/LVS ring by 4/1.



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Marlboro Hardware Design Block Status

- SQ
 - Closure rate of SQ debug was not matching planned schedule
 - Orlando has resources available
 - Orlando ramp-up started, division of labor identified
 - Regular meetings started 1/06/03 w/ Orlando to coordinate responsibilities
- SP
 - Last few bugs are being worked
 - Ironing precision out
 - Updated SQRT in emulator Monday, in HW Tuesday
 - TP formatter verification within SP (Vishal)
 - Plan is to freeze SP with Netlist 4.0 release (2/14/03)
- SX
 - Moving export allocate counter to SQ to solve performance issue
 - Debug remainder of export features (dependent on SQ debug)
 - FOG, multi-pass, pixel kill, alpha test, cylindrical wrap, etc.
 - Add resource to speed debug of SX (TBD)

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Marlboro Hardware Design Block Status

- TP / TC
 - TP verification debug is currently a bottleneck
 - Moving resource (Suba D.) from TC to TP for debug
 - Moving verification resource (Kevin Olson.) to TC design
 - Using synthesis contractor (Steve Mburu) for TC block split
 - Mark Fowler has been added to drive TP/TC debug
- TP
 - Working LOD logic, expect wrap-up this week
 - Belief is LOD is a major blockage to tests passing
 - Many changes made Monday – large jump in tests passing
- TC
 - Performance improvements designed and released
 - Break-up of the TC in progress, expected done for Netlist 4.0
 - Study and identify AGP vertex performance issue
 - Repair not yet fully understood
 - Expect some area/schedule impact for TC
 - Architectural deadlock issue
 - Identified and fix being implemented (expected complete in one week)

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Marlboro Hardware Design Block Status

- RB
 - Random testing continues with a high failure rate
 - Fixes being implemented 1/14/03
 - Identified RB needs division to fit in physical design tools
 - Will not gate Netlist 4.0 (plan for Netlist 5.0)
 - Timing has improved from 5ns to 1.7ns violation over the Holidays
 - Mark Sprague is fixing timing issues
 - Adding Dan Clifton for stencil decompression/compression
- AB
 - Validation (complete? – ask Jay in the morning)
 - Performance analysis is complete and satisfactory
 - Block awaiting PD feedback
- MC/MH
 - MC Pad interface logic design in progress, complete by 1/31/03.
 - Completion is gating Netlist 4.0
 - Electrical interface for pads requires SiV input (most issues closed)
 - Plan for calibration unit in place requires SiV agreement
 - Issues raised on Clock signal pad and strobe pads requires SiV resolution
 - MC/MH Block level test complete, identified verification coverage holes that are being addressed
 - Moving Bei Wang to test writing
 - Adding Brian Favela to implement MC/MH testbench enhancements
 - Starting significant stress and random verification

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Marlboro Hardware Design Block Status

BLOCK	SQ	SP	SX	RB	AB	RC	TP	TC
Synth Date	Jan 11, 2003	Dec 26, 2002	Dec 16, 2002	Jan 14, 2003	Jan 8, 2003	Dec 18, 2002	Jan 14, 2003	Jan 2, 2003
Worst Timing	-0.84	-0.45	-1.17	-2.50	-0.21	0.0	-0.93	-0.96
Previous Worst Timing	-0.25	-0.25	-0.25	-3.95	-0.44		-0.25	-5.25
Total Neg Slack	135.9	1580.4	1954.2	14503.8	0.3	0.0	499.0	16109.9
Total Area (sqmm)	5.359	9.243	2.772	9.045	1.772	0.187	3.643	N/A
Previous Area (sqmm)	4.69	11.06	3.05	11.13	1.66	0.22	3.89	20.02



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Marlboro Hardware Design Block Status

BLOCK	MH	MC	SI	IO	CHIP
Synth Date	Jan 14, 2003	Dec 16, 2002	Dec 20, 2002	N/A	Dec 31, 2002
Worst Timing	-0.32	-0.61	0.0	N/A	0.0
Previous Worst Timing	-0.53	-0.25			
Total Neg Slack	1922.2	36.3		N/A	
Total Area (sqmm)	6.965	0.847	0.206	N/A	6.569
Previous Area (sqmm)	5.71	0.95			

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Marlboro Hardware Design Block Status

Major Block	Plan	Last FC	Current FC
RB Blend (AB Block)	11/18/2002	12/18/2002	1/2/2003
SP	11/18/2002	1/9/2003	2/14/2003
SX	12/2/2002	1/11/2003	2/28/2003
MC	12/16/2002	1/20/2003	3/15/2003
MH	1/2/2003	1/2/2003	3/15/2003
SQ	1/15/2003	1/15/2003	5/1/2003
RB (Remaining)	1/15/2003	1/15/2003	4/10/2003
TP	1/31/2003	1/31/2003	4/30/2003
TC	1/31/2003	1/31/2003	4/30/2003



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Target Milestones in Last Month

- **R400 Program Milestones**

- Whole chip code freeze by 11/23

- **Toronto R400 revised milestones**

- Achieve 100% passing in block regression by 12/13 with tvout being 1/6.
- Start IKOS debug 12/20.
- Achieve revised timing goals by 12/30.
- Achieve 50% regression passing in chip by 12/30, 100% by 1/30.
- Start Gate level simulation in Jan.
- Complete system tests & debugged by 1/30
- Deliver final netlist 1/30.



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What Have We Achieved

• Status Summary

- ✓ Achieved 100% passing on block level regression on Dec 30 with the exception of tvout and bif
- ✓ Achieved over 50% passing on chip level regression on Dec 30
- ✓ PCI configuration cycles passed on IKOS validation on netlist 2.0
- ✓ System tests are on track to be delivered & debugged
- ✓ Emulation work in bif & tvout are on track. The completion dates are Jan 24 for tvout and Feb 7 for bif
- ✓ Synthesis timing/area closure is in progress
- ✓ Deliver IDCT final netlist on Jan 24



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What Have We Achieved (specs, coding, emulation, tests)

- Coding is 100% complete with 2% outstanding in BIF(agg 64byte write & perf counter).
- Emulation is 100% completed with vga(tiled mem dump) and bif.
- Tests are 100% released with lb, tvout, bif & system outstanding, covering RT, hdtv, bif changes.

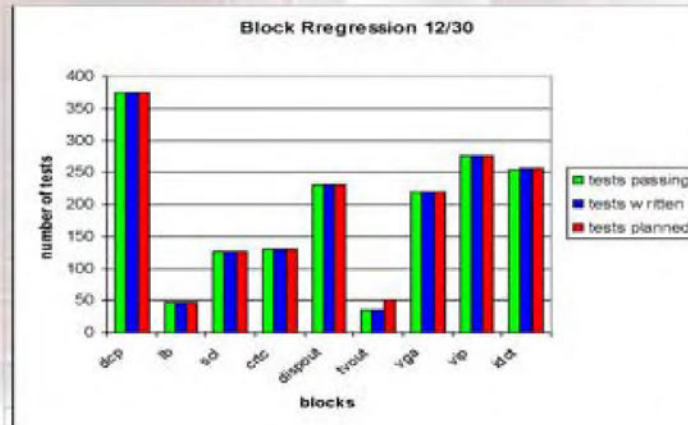
Design		RTL specs	RTL coding	Emulation	Tests Written
display	dcp	100%	100%	100%	100%
	lb	100%	100%	100%	98%
	scl	100%	100%	100%	100%
	crtc	100%	100%	100%	100%
	dispout	100%	100%	100%	100%
	tvout	100%	100%	100%	80%
vga		100%	100%	99%	100%
vip		100%	100%	100%	100%
BIF		96%	98%	90%	50%
IDCT		100%	100%	100%	100%
system					35%

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What Have We Achieved (block RTL regression)

- All blocks are 100% passing
- Tvout reached 80% passing and plan to complete by Jan24



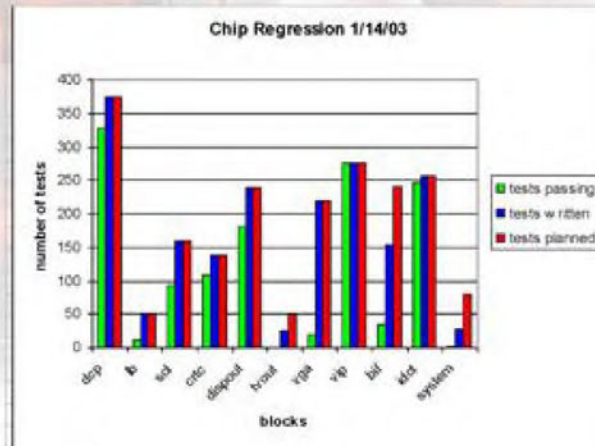
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What Have We Achieved (Chip regression)

- Overall 68% passed on chip level with VIP 100% & 1DCT 96%
- Dcp, scl, crtc, dispout all have above 60% passing. The failing 40% was due to DC-MH interface bugs.
- Vga is gated by tiled memory dump while bif is catching up.



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What Have We Achieved (Chip regression emulation)

- Most blocks are 100% passing
- Tvout & vga plan to complete by Jan 24
- Bif plan to complete by Feb 15

Design	Chip emu regress	Tests passing	Tests Released	Tests Planned
dcp	100%	375	375	375
lb	100%	47	47	47
scl	85%	135	159	159
crtc	100%	131	131	131
dispout	100%	232	232	232
tvout	0%	0	0	50
vga	59%	130	171	220
vip	100%	275	275	275
DC		1325	1390	1489
BIF	83%	200	153	240
IDCT	96%	246	256	256
System	0%	0	0	80
Total	86%	1771	1799	2065

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What Have We Achieved (Area & Timing)

- More efforts are in place to close timing and area issues.
- IDCT to close by Jan 24
- Most violations in DC should be fixed through a number of iterations of synthesis. DC still have some violations caused by improper constraints. The area goal is 7mm2.
- BIF's timing issue are due to design changes and they are in review to be updated.

DC			BIF		
Area (mm2)	8.4		Area (mm2)	1.63	
Cell Count	392K		Cell Count	163K	
Timing			Timing		
Path Groups	Speed (ns)	Violation (ns)	Path Groups	Speed (ns)	Violation (ns)
PCLK_CRTC1	2.5	-0.06	SCLK_G_BIF	2.25	-0.58
PCLK_CRTC2	2.5	-0.10	AGPCLK	3.5	0
SCLK_G_DCP	2.25	-0.35	BCLK	14	0
SCLK_G_SCL1	2.25	-0.27			
SCLK_G_SCL2	2.25	-0.27	IDCT		
SCLK_G_VGA	2.25	-1.34	Area (mm2)	1.23	
SCLK_G_VIP	2.25	-0.01	Cell Count	72K	
SCLK_M	2.25	-0.11	Timing		
SCLK_P_DC	2.25	-1.33	Path Groups	Speed (ns)	Violation (ns)
SCLK_R_DISP	2.25	-1.61	SCLK_G_DCT	2.25	-0.16
SCLK_R_TVOUT	2.25	-0.04			
SCLK_R_VIP	2.25	-0.67			

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What's ahead?

Next Set of Goals:

- Deliver IDCT final netlist by Jan 24
- Achieve DC 100% passing in chip level regression by Jan 30
- IKOS validation on netlist 3.0.
- Achieve DC timing goals by Jan 30.
- Deliver DC final netlist by Feb 15.
- Start Gate level simulation in Jan.
- Close bif timing & existing tests issues by 1/30.
- Deliver BIF final netlists by Feb 28



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Issues

Chip level regression:

- 7 MH related bugs reported for last 2 weeks
 - 5 hardware issues to be fixed & released
 - 2 emulation issues(vga rotation) to be fixed
- 4 BIF related emulator bugs reported
 - 1 due to dma hang resolved
 - 3 others related to FB_START, HDP_FB_START, APER_CNTL to be resolved
- DVO pad
 - Recommended mem pad doesn't support SDR mode
 - Can we drop 3.3V support?



10
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Risks

- MH bug fixes has been the bottleneck for chip regression.
 - Need Marlboro MH team to increase their priority in resolving these issues
- Marlboro's RTL code releasing process has been ranging from 2 to 5 days before it get released.
 - This is critical in resolving chip issues quickly.
 - Currently, DC progress is being slow down on chip regression.
- The next step is to get IKOS running with display
 - This again require MH/MC issues and bugs to be resolved
- Area reduction plan may have schedule impact



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Orlando Hardware Status

- CP / RBBM / VGT / PA / SC / SC_B 100% coded (Netlist 3)
- Gate Level simulations of all blocks in progress
 - PA identified problem with Virage memory models
 - Several issues identified in Hardware and fixed
- Code coverage results used to improve random and stress test coverage
- Continued synthesis realizing timing improvements and area reduction
 - 0.445 mm² reduction => 2.5% improvement over netlist 3
- Real Time Streams, Pipe Disable, 2D Validation in progress ... moving to GC/Full chip testing

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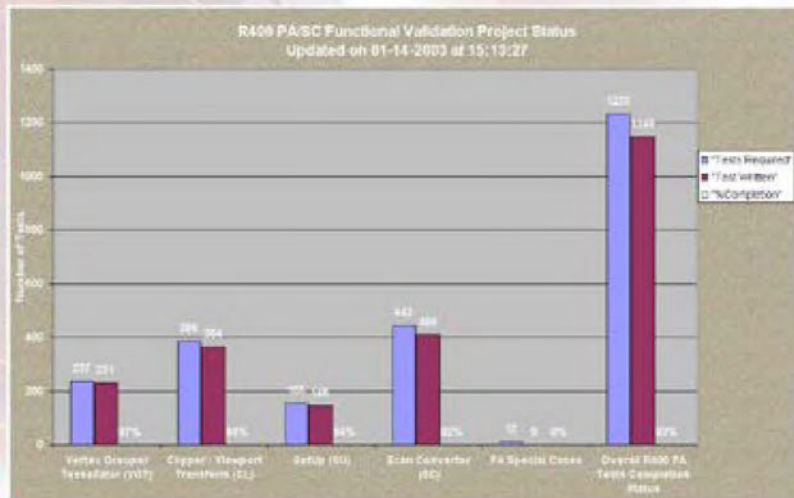
Orlando Synthesis Summary

BLOCK	PA	VGT	SC	SC_B	CP	RBBM
Synth Date	Jan 10, 2003	Jan 13, 2003	Jan 12, 2003	Jan 10, 2003	Jan 13, 2003	Jan 2, 2003
Code Version	N/A	N/A	N/A	N/A	N/A	N/A
Worst Timing	-0.84	-0.86	-0.17	-0.81	0	-0.03
# > 1.00 nS	0	0	0	0	0	0
# > 0.50 nS	0	0	0	0	0	0
# > 0.20 nS	0	0	0	0	0	0
# > 0.05 nS	311	165	539	2	0	22
Total Neg Slack	5.7	4.3	27.5	0.1	0.0	0.4
Wireload	N/A	N/A	N/A	N/A	N/A	N/A
Cell Area (sqmm)	3.134	0.752	3.271	3.481	2.449	0.143
Macro Area (sqmm)	1.006	0.401	0.903	0.000	1.797	0.125
Total Area (sqmm)	4.140	1.152	4.174	3.481	4.245	0.268
Number of Cells	185910	53735	187484	169572	152683	8877
Number of nets	200899	57814	200427	183741	162532	9986
Timing Summary link (.tsumm)	pa.tsumm	vgt.tsumm	sc.tsumm	sc_b.tsumm	cp.tsumm	rbbm.tsumm
Area Summary link (.reflog)	pa.reflog	vgt.reflog	sc.reflog	sc_b.reflog	cp.reflog	rbbm.reflog
Netlist 3 Results						
Worst Timing	-0.33	-0.17	-0.14	-0.81	-0.89	-0.15
Total Area (sqmm)	4.213	1.235	4.278	3.608	4.580	0.271

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Orlando Function Test Status



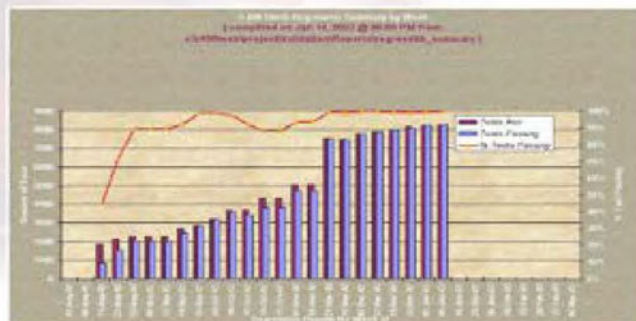
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Block Validation

Orlando Block Regression Status Summary

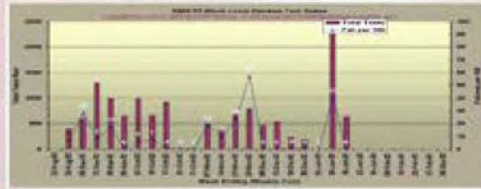
Test Bench	Tests Run	Tests Pass	% Pass	Report Date
VGT	2484	2479	99%	01-14-03
CP_RBBM	907	819	90%	01-14-03
SC	2486	2460	98%	01-14-03
PA	2485	2478	99%	01-14-03



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Block Random Results

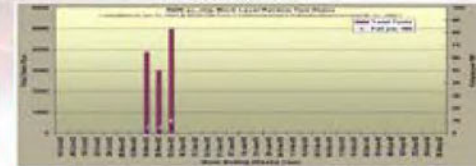
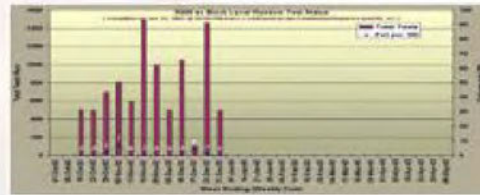


PA

- 13298 tests run
- 0 failures per 100

SC

- 8231 tests run
- 0 failures per 100



SC_CHIP

- 11892 tests run
- 5 failures per 100

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Orlando Resource Reallocation

- ◆ Designers shifting to other R400 blocks
 - SQ: 6 engineers assisting with RTL validation, test bench generation, test suite review and performance analysis / validation
 - Laurent Lefebvre – Emulator updates, debugging, help everyone up to speed.
 - Vic Romaker – Key debugger, Waterfalling, Kill Mask, Export and Multi-Pass, Control Flow etc.
 - Doug Duncan – Debug, Clock gating, Performance Counters, Instr & Const Store issues, GPR alloc
 - George Valaitas – Test Suites
 - Yung Giang – Add performance counter test etc
 - Scott Hartog – Stand alone SQ test bench
 - Mike Mantor – Debug, focus Performance and SC/SQ/SP interface functionality
 - Mike Mang – Architecture and performance analysis, Predication debug
 - Donald Lee – RTL focus on predication and export buffer counter change
 - Clay Taylor – Performance analysis and general debug
 - Randy Ramsey – Debug focus on Control Flow
 - Stevie Camlin – SQ synthesis / error clean-up



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Orlando Resource Reallocation

- TP: 1 engineer added for TP stand-alone test bench creation
- RB: 1 engineer added for RTL coding / validation
- SX: Possibly 1 engineer added for stand-alone test bench creation



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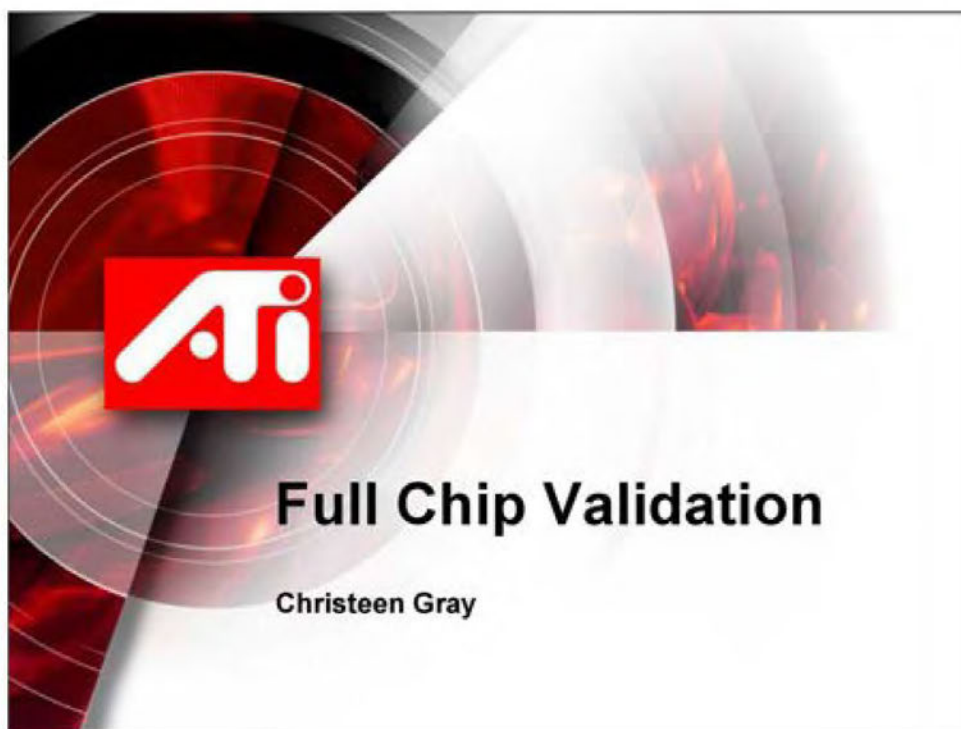


Issues / Risks

- ♦ PM4 Packet dumps needed for performance testing / and feature validation
 - 3dMark03, UT03, Doom3
- ♦ Full chip / GC validation
- ♦ Pipe Disable Validation for IKOS
- ♦ Real-time stream and 2D validation (require integrated testing)
- ♦ Reallocation of Orlando resources
 - Spin up time on new areas
 - Shifting focus from existing blocks

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Chip Validation Status

- Most chip environment updates (for graphics testing) are in place. Remaining are:



- Makefile updates to handle sim target for new parameterized tests
- Continue to clean up warnings from chip compile/simulation
 - Runtime memory model warnings
 - Connectivity warnings from compile
- Automate method of tracking system test progress (requires multi-sited data collection)

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Chip Validation Status (cont'd)

◆ Orlando Full Chip Validation:

	Total Tests	Tests Written	Tests Passing	% Complete
CP	1182	785	246	28%
RBBM	100	10	10	10%
GFX	500	>500	44	9%

◆ Toronto Full Chip Validation

#Planned	#ExpectedRun	#Passing (%Passing)
1684	1684	1305 (77 %)

12
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Chip Validation Tasks

- Continue to add trackers, monitors, debugging aids to Chip / GC testbench

The diagram illustrates the R600 Graphics Pipeline. It shows a sequence of processing stages: a vertex shader, a geometry shader, a tessellation shader, a primitive assembly, a rasterizer, and a fragment shader. Each stage is represented by a block with internal components and data flow arrows. The pipeline is connected to a memory block and a display output. The diagram is labeled 'R600 Graphics Pipeline' at the top.

- Review test suites for coverage
- Plan and continue to write chip level functional and stress tests

13
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ATI Ex. 2063
IPR2023-00922
Page 46 of 150

Issues / Risks

- ◆ Compute Resources
 - With increased users on the GC / Chip environment, Orlando linux farm / disk space was inadequate
 - Ordered 10 additional linux machines
- ◆ Maturity / functionality of blocks at a point to start validation of functions requiring integrated testing:
 - 2D Validation
 - Performance
 - Bad Pipe
 - Real Time Streams
- ◆ Improvements to block level test benches will improve progress at integrated GC and Chip level testing
 - Adding randomization at interfaces
 - Lower-level Test Benches are being built

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BLOCK	PA	VGT	SC	SC_B	CP	RBBM
Synth Date	Jan 10, 2003	Jan 13, 2003	Jan 12, 2003	Jan 10, 2003	Jan 13, 2003	Jan 2, 2003
Code Version	N/A	N/A	N/A	N/A	N/A	N/A
Worst Timing	-0.04	-0.06	-0.17	-0.01	0	-0.03
# > 1.00 nS	0	0	0	0	0	0
# > 0.50 nS	0	0	0	0	0	0
# > 0.20 nS	0	0	0	0	0	0
# > 0.00 nS	311	165	539	2	0	22
Total Neg Slack	5.7	4.3	27.5	0.1	0.0	0.4
Wireload	N/A	N/A	N/A	N/A	N/A	N/A
Cell Area (sqmm)	3.134	0.752	3.271	3.481	2.449	0.143
Macro Area (sqmm)	1.006	0.401	0.903	0.000	1.797	0.125
Total Area (sqmm)	4.140	1.152	4.174	3.481	4.245	0.268
Number of Cells	185919	53735	187484	169572	152883	8877
Number of nets	200899	57814	200427	183741	162532	9986
Timing Summary link (.tsumm)	pa.tsumm	vgt.tsumm	sc.tsumm	sc_b.tsumm	cp.tsumm	rbbm.tsumm
Area Summary link (.reflog)	pa.reflog	vgt.reflog	sc.reflog	sc_b.reflog	cp.reflog	rbbm.reflog
Netlist 3 Results						
Worst Timing	-0.33	-0.17	-0.14	-0.01	-0.00	-0.15
Total Area (sqmm)	4.313	1.235	4.275	3.600	4.580	0.271

Orlando Block Regression Status Summary

Test Bench	Tests Run	Tests Pass	% Pass	Report Date
VGT	2484	2479	99%	01-14-03
CP-RBBM	907	819	90%	01-14-03
SC	2486	2460	98%	01-14-03
PA	2485	2478	99%	01-14-03

```
=====
Type  #Planned  #ExpectedRun #Passing(%Passing)
-----
SIM   1684      1684      1305    (77      )
```



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Orlando Hardware Status

- CP / RBBM / VGT / PA / SC / SC_B 100% coded (Netlist 3)
- Gate Level simulations of all blocks in progress
 - PA identified problem with Virage memory models
 - Several issues identified in Hardware and fixed
- Code coverage results used to improve random and stress test coverage
- Continued synthesis realizing timing improvements and area reduction
 - 0.445 mm² reduction => 2.5% improvement over netlist 3
- Real Time Streams, Pipe Disable, 2D Validation in progress ... moving to GC/Full chip testing

2
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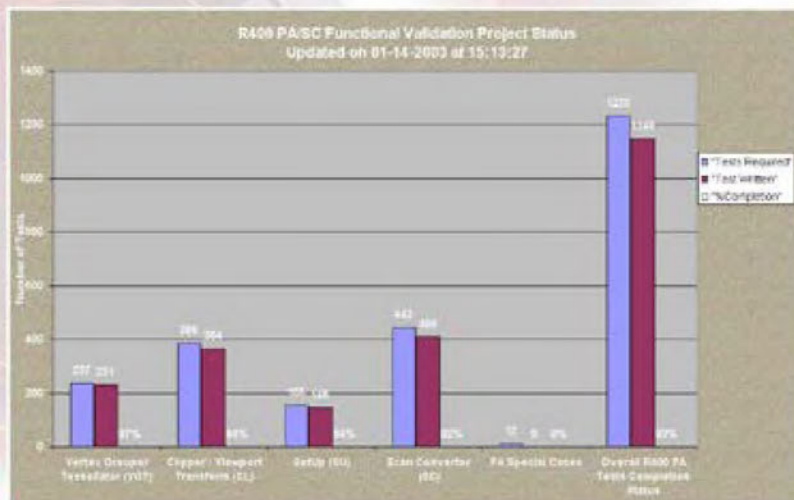
Orlando Synthesis Summary

BLOCK	PA	VGT	SC	SC_B	CP	RBBM
Synth Date	Jan 10, 2003	Jan 13, 2003	Jan 12, 2003	Jan 10, 2003	Jan 13, 2003	Jan 2, 2003
Code Version	N/A	N/A	N/A	N/A	N/A	N/A
Worst Timing	-0.84	-0.86	-0.17	-0.81	0	-0.03
# > 1.00 nS	0	0	0	0	0	0
# > 0.50 nS	0	0	0	0	0	0
# > 0.20 nS	0	0	0	0	0	0
# > 0.05 nS	311	165	539	2	0	22
Total Neg Slack	5.7	4.3	27.5	0.1	0.0	0.4
Wireload	N/A	N/A	N/A	N/A	N/A	N/A
Cell Area (sqmm)	3.134	0.752	3.271	3.481	2.449	0.143
Macro Area (sqmm)	1.006	0.401	0.903	0.000	1.797	0.125
Total Area (sqmm)	4.140	1.152	4.174	3.481	4.245	0.268
Number of Cells	185910	53735	187484	169572	152683	8877
Number of nets	200899	57814	200427	183741	162532	9986
Timing Summary link (.tsumm)	pa.tsumm	vgt.tsumm	sc.tsumm	sc_b.tsumm	cp.tsumm	rbbm.tsumm
Area Summary link (.reflog)	pa.reflog	vgt.reflog	sc.reflog	sc_b.reflog	cp.reflog	rbbm.reflog
Netlist 3 Results						
Worst Timing	-0.33	-0.17	-0.14	-0.81	-0.89	-0.15
Total Area (sqmm)	4.213	1.235	4.276	3.609	4.580	0.271

5
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Orlando Function Test Status



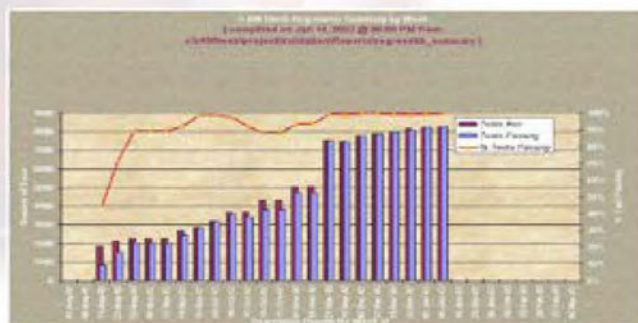
4
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Block Validation

Orlando Block Regression Status Summary

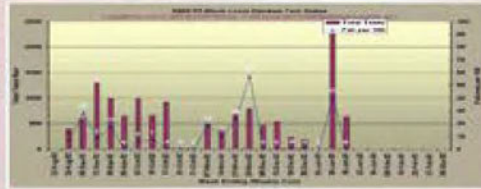
Test Bench	Tests Run	Tests Pass	% Pass	Report Date
VGT	2484	2479	99%	01-14-03
CP_RBBM	907	819	90%	01-14-03
SC	2486	2460	98%	01-14-03
PA	2485	2478	99%	01-14-03



5
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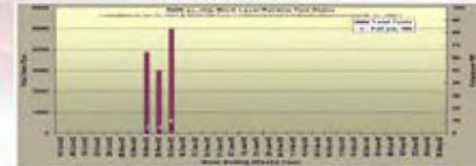
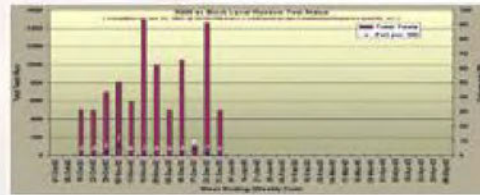
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Block Random Results



- PA
 - 13298 tests run
 - 0 failures per 100

- SC
 - 8231 tests run
 - 0 failures per 100



- SC_CHIP
 - 11892 tests run
 - 5 failures per 100

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Orlando Resource Reallocation

◆ Designers shifting to other R400 blocks

- SQ: 6 engineers assisting with RTL validation, test bench generation, test suite review and performance analysis / validation
- Laurent Lefebvre – Emulator updates, debugging, help everyone up to speed.
- Vic Romaker – Key debugger, Waterfalling, Kill Mask, Export and Multi-Pass, Control Flow etc.
- Doug Duncan – Debug, Clock gating, Performance Counters, Instr & Const Store issues, GPR alloc
- George Valaitas – Test Suites
- Yung Giang – Add performance counter test etc
- Scott Hartog – Stand alone SQ test bench
- Mike Mantor – Debug, focus Performance and SC/SQ/SP interface functionality
- Mike Mang – Architecture and performance analysis, Predication debug
- Donald Lee – RTL focus on predication and export buffer counter change
- Clay Taylor – Performance analysis and general debug
- Randy Ramsey – Debug focus on Control Flow
- Stevie Camlin – SQ synthesis / error clean-up



7
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Orlando Resource Reallocation

- TP: 1 engineer added for TP stand-alone test bench creation
- RB: 1 engineer added for RTL coding / validation
- SX: Possibly 1 engineer added for stand-alone test bench creation



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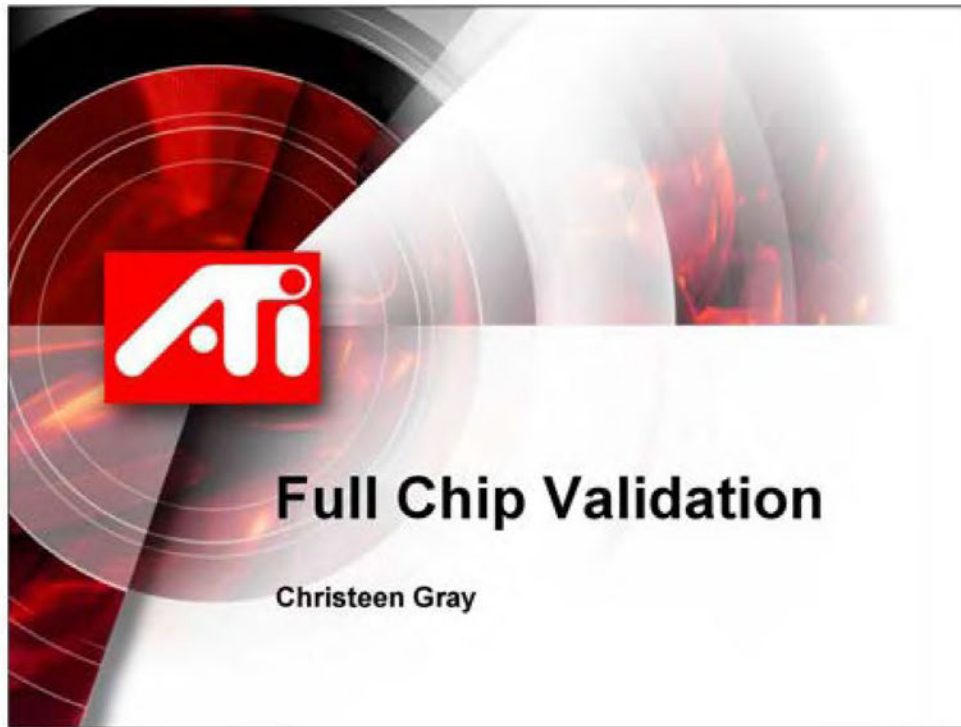


Issues / Risks

- ♦ PM4 Packet dumps needed for performance testing / and feature validation
 - 3dMark03, UT03, Doom3
- ♦ Full chip / GC validation
- ♦ Pipe Disable Validation for IKOS
- ♦ Real-time stream and 2D validation (require integrated testing)
- ♦ Reallocation of Orlando resources
 - Spin up time on new areas
 - Shifting focus from existing blocks

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Chip Validation Status

- Most chip environment updates (for graphics testing) are in place. Remaining are:
 - Makefile updates to handle sim target for new parameterized tests
 - Handle/Fix 1 LSB precision difference between emulator and hardware
 - Continue to clean up warnings from chip compile/simulation
 - Runtime memory model warnings
 - Connectivity warnings from compile
 - Automate method of tracking system test progress (requires multi-sited data collection)



11
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Chip Validation Status (cont'd)

◆ Orlando Full Chip Validation:

	Total Tests	Tests Written	Tests Passing	% Complete
CP	1182	785	246	28%
RBBM	100	10	10	10%
GFX	500	>500	44	9%

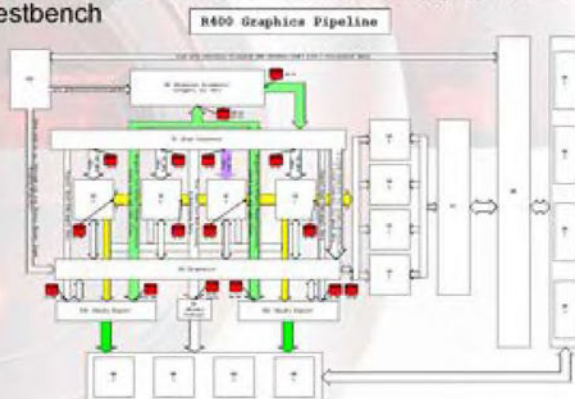
◆ Toronto Full Chip Validation

#Planned	#ExpectedRun	#Passing (%Passing)
1684	1684	1305 (77)

12
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Chip Validation Tasks

- Continue to add trackers, monitors, debugging aids to Chip / GC testbench



- Review test suites for coverage
- Plan and continue to write chip level functional and stress tests

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Issues / Risks

- ◆ Compute Resources
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```
=====
Type  #Planned  #ExpectedRun #Passing(%Passing)
-----
SIM   1684      1684        1305    (77      )
```



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Performance Counters

• Current Status

- Several blocks have implemented performance counters
- MH, SC, RB (partial), SX are complete
- Expecting MC, SQ, TP/TC to be implemented soon
- This includes "phantom" counters; not synthesized but allow dumping of all information after simulation

• Analysis

- Able to dump all performance counters to file after a simulation
- Have some tools to post-process dumps (clean-up, sort, add to spreadsheet, etc)
- Plan to add support for analysis...



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Performance Counter Output

◆ Sample SC and RB Counts

```
----- start of module sc count -----
testbench.top.go.gc.sc.uvc_perfmon_gp_num_quads_low,      4096
testbench.top.go.gc.sc.uvc_perfmon_gp_covered_h16_low,    256
testbench.top.go.gc.sc.uvc_perfmon_hior_num_quads_low,    4096
testbench.top.go.gc.sc.uvc_perfmon_det_num_quads_low,     4096
testbench.top.go.gc.sc.uvc_perfmon_det_mask_h16_low,      0
testbench.top.go.gc.sc.uvc_perfmon_det_mask_h1_low,       0
-
----- end of module sc count -----
----- start of module rb count -----
testbench.top.go.gc.rb_3.uvc_perfmon_wrapper.uvc_perfmon_rb_ctrlt_busy_low,      4527
testbench.top.go.gc.rb_3.uvc_perfmon_wrapper.uvc_perfmon_num_quads_passed_s_low,  1024
testbench.top.go.gc.rb_3.uvc_perfmon_wrapper.uvc_perfmon_num_quads_failed_s_low,  1
testbench.top.go.gc.rb_3.uvc_perfmon_wrapper.uvc_perfmon_num_8x256_depth_cache_fills_sep_low, 0
testbench.top.go.gc.rb_3.uvc_perfmon_wrapper.uvc_perfmon_num_8x256_depth_cache_fills_sep_low, 0
testbench.top.go.gc.rb_3.uvc_perfmon_wrapper.uvc_perfmon_num_8x256_depth_cache_flushes_low, 0
testbench.top.go.gc.rb_3.uvc_perfmon_wrapper.uvc_perfmon_num_8x256_depth_cache_flushes_sep, 0
-
----- end of module rb count -----
```

5

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Directed Tests

◆ Gathering Data

- Running lots of parameterized directed tests to gather data for various fill rates on the simulator
- Focusing on simple fill rate tests such as color fills, blending, depth tests, and basic texturing
- Processing and analyzing data with architects and leads to understand and interpret the numbers

◆ Analysis

- Color fills appear to be achieving peak goal of 8 pix/clk
- Blends are currently not hitting the peak numbers (~6 pix/clk); this is under investigation at the moment
- The numbers are adjusted to not include flush time (up to 1K 32-bit pixels to memory or approx 256 cycles)
- Numbers still include setup time (30-50 cycles) which is most likely why they are slightly below 8

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Directed Tests

• Sample Data (RBRC color fills)

R400 Fill Rate Tests
Updated 1/15/2003

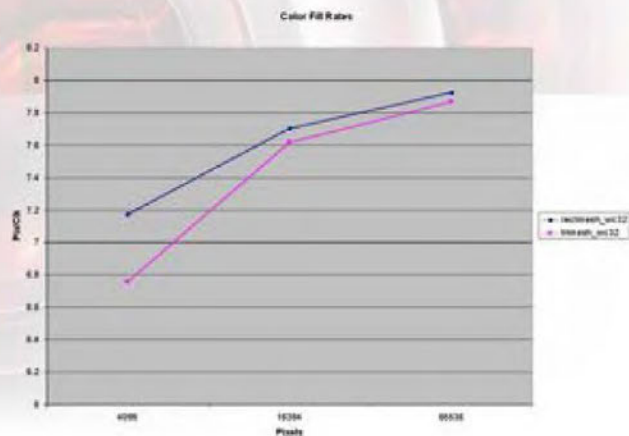
RBRC									
Test	Grid Size (nxn)	Pixels	Cliks	Pix/Cik	Pix/Cik (noflush)	R400 (Exp)	% R400 Expected	R300 (Sim)	% R300 Simulated
rectmesh_wc32	64 1	4096	827	4.952842	7.17338	8	89.67%		
rectmesh_wc32	64 4	65536	8543	7.67131	7.90829	8	98.85%		
rectmesh_wc32	128 1	16384	2383	6.875367	7.702868	8	96.25%		
rectmesh_wc32	128 2	65536	8527	7.685704	7.923588	8	99.04%		
rectmesh_wc32	256 1	65536	8527	7.685704	7.923588	8	99.04%	7.871	100.66%
trimesh_wc32	64 1	4096	862	4.75174	6.759076	8	84.49%		
trimesh_wc32	64 4	65536	8795	7.451507	7.674903	8	95.94%		
trimesh_wc32	128 1	16384	2407	6.806813	7.616922	8	95.21%		
trimesh_wc32	128 2	65536	8526	7.686606	7.924547	8	99.06%		
trimesh_wc32	256 1	65536	8585	7.63378	7.868412	8	98.36%		

5
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Directed Tests

- RBRC color fill (increasing pixels)

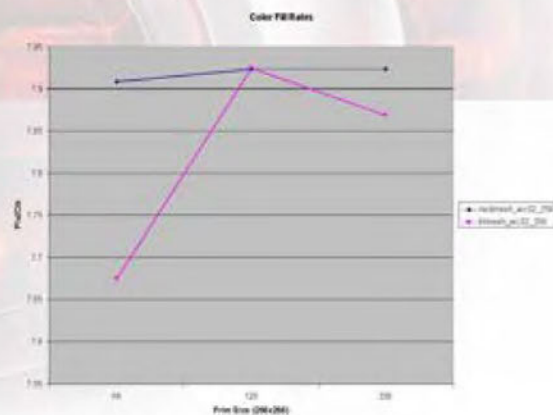


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Directed Tests

- RBRC color fill (constant pixels)



7
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Directed Tests

• Sample Data (RBRC blends)

R400 Fill Rate Tests										
Updated 1/15/2003										
RBRC										
Test	Size	Grid (nxn)	Pixels	Ckts	Pix/Cik	Pix/Cik (noflush)	R400 (Exp)	% R400 (Exp)	R300 (Sim)	% R300 (Sim)
rectmesh_nwc32	128	1	16384	2704	6.0691716	6.68281	8	75.74%		
rectmesh_nwc32	128	2	65536	11656	5.622512	5.748772	8	70.28%		
rectmesh_nwc32	256	1	65536	11272	5.8140625	5.949165	8	72.68%	7.0981	81.91%
trimesh_nwc32	128	1	16384	3095	5.2936955	5.771046	8	66.17%		
trimesh_nwc32	128	2	65536	11909	5.5030649	5.623959	8	68.79%		
trimesh_nwc32	256	1	65536	11571	5.6838147	5.791958	8	70.80%		

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Directed Tests

◆ Issues

- Want to use GC for all performance measurements; however, GC is not fully optimal yet preventing peak measurements for many directed tests (eg textures)
- Depth unit is currently not optimized so no useful data yet
- Texturing is not optimal yet; however, performance has improved 4X in a very short time
- Need more time spent on back end processing of data; currently the process is too manual

◆ What's next

- Texturing tests, depth tests, stencil tests, etc
- Small batch tests, scissoring tests, shadows?, shaders?

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R400 Capture & Playback Tools

• QS Capture Functionality

- Capture tool functionality is currently broken; series of unconnected and unfortunate events preventing this from working (spec changes, booting issues, blue screens, etc)
- Toronto is providing support on the boot and crash issues; we believe the boot problem is fixed and crash is understood and fix is imminent (just provided a new driver w/ fixes – testing...)
- Because of this, not a lot of capturing has been going on lately...

• Parser Tools

- Corinna's HWPG have been continuing to support the R400 in the parser tools; adding support for PM4Cut, formatting changes, etc
- Looking into support of R400 shader disassembly from existing tools

10
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R400 Capture & Playback (con't)

◆ Emu/Sim Playback

- ◆ R400 playback tool checked in and building;
- ◆ New support for multiple header formats implemented
- ◆ The FB_START issue has been resolved in primlib
- ◆ Nothing else new here w/o new up to date dump files to debug...

◆ Misc

- ◆ All participating groups are continuing weekly meetings to discuss schedules, implementation details, etc
- ◆ Corinna is working on support for capture and playback of 2D packets...

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R400 Tools

◆ Optimizer Tool (PM4Opt)

- Will parse dump files from D3D and OpenGL drivers, analyze the render states, shader programs, etc, and update new dump file for playback
- Allows performance verification work to proceed without creating a dependency on the driver folks; information gleaned can be fed back to the R400 driver and compiler groups
- Based on R400 parser library tools; modeled against the R300 program
- Progress is slow w/o dump files...

◆ Frame/Scissor Tools (DX8Logger, GLWrapper)

- Allow the capture of individual frames as well as selected regions (high res) of the screen
- Implemented, initial tests appear to work

12
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Application Tests

• Tgl to primlib port

- Allows R300 synthetic and high level (complex) tests to be run on R400 (SiV); will complement the directed tests
- Scripting language (dv) allows for large numbers of test variations
- These tests are now running on both the emulator and the simulator here in Marlboro; all previous setup and build issues have apparently been resolved ☺

• Pseudo-benchmark apps

- Simpler apps that are designed to emulate known algorithms used in benchmarks
- Have Doom3 final shader pass and stencil shadow algorithms; R300 perf suite complex tests will complement these tests

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Benchmark Tests

◆ 3DMark 2003

- ◆ Has DX7, DX8, and DX9 tests with most emphasis on the DX9 test; also has some fill rate and geometry tests;
- ◆ Benchmark, tools, etc in place to begin debug of this DirectX benchmark; however, unclear if the driver is ready to support the execution of this test as of yet
- ◆ Plenty of information can be gathered if the dump files are incomplete; the PM4Opt tool can be used to work through problem areas, analyze shaders, etc...

◆ Doom3

- ◆ Do not have the 'latest' version of this OpenGL game/benchmark (due to recent snafu)
- ◆ As with above benchmark, ready to debug as far as the driver will allow us

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Current PV Issues

- ◆ Need capture and playback issues solved
- ◆ Need GC performance improvement
- ◆ Driver support with benchmark and other applications

15
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Next Month...

- ◆ Get capture and playback working
- ◆ Begin debug and analysis of benchmark (et al) applications
- ◆ Successful implementation of R400 optimizer tool
- ◆ Complete implementation of performance counters in all the blocks
- ◆ Continue and expand directed test coverage and analysis, provide more extensive data to wider audience
- ◆ Run more of the perfsuite tests
- ◆ Provide hardware and software folks with useful performance information!!!
- ◆ Include set of performance regression tests as part of nightly build

18
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Directed Tests

Test	Planned	Written	% Written	Analyzed	% Analyzed
pv_triangle	28	21	75%	.5	0%
pv_texture	27	27	100%	0	0%
pv_texture_multi	12	4	33%	0	0%
pv_scissor	3	3	100%	0	0%
pv_fog	8	4	50%	0	0%
pv_line	8	4	50%	0	0%
pv_point	8	1	12%	0	0%
pv_rb	19	19	100%	0	0%
pv_tcache	12?	0	0%	0	0%
pv_hiz_sten	10?	0	0%	0	0%
pv_shader	12?	0	0%	0	0%
miscellaneous	20?	0	0%	0	0%
Total	167	83	50%	.5	0%

18
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```

----- start of module sc count -----
testbench.top.gc.gc.sc.usc_perfmon_qm_num_quads_low,      4096
testbench.top.gc.gc.sc.usc_perfmon_qm_covered_hl6_low,    256
testbench.top.gc.gc.sc.usc_perfmon_hier_num_quads_low,    4096
testbench.top.gc.gc.sc.usc_perfmon_det_num_quads_low,     4096
testbench.top.gc.gc.sc.usc_perfmon_det_mask_h0_low,       0
testbench.top.gc.gc.sc.usc_perfmon_det_mask_hl_low,       0
.
.
----- end of module sc count -----
----- start of module rb count -----
testbench.top.gc.gc.rb_3.urb_perfmon_wrapper.urb_perfmon_rb_cntxl7_busy_low,      4527
testbench.top.gc.gc.rb_3.urb_perfmon_wrapper.urb_perfmon_num_quads_passed_z_low,    1024
testbench.top.gc.gc.rb_3.urb_perfmon_wrapper.urb_perfmon_num_quads_failed_z_low,     1
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testbench.top.gc.gc.rb_3.urb_perfmon_wrapper.urb_perfmon_num_8x256_depth_cache_fills_sep_low, 0
testbench.top.gc.gc.rb_3.urb_perfmon_wrapper.urb_perfmon_num_8x256_depth_cache_flushes_low, 0
testbench.top.gc.gc.rb_3.urb_perfmon_wrapper.urb_perfmon_num_8x256_depth_cache_flushes_sep, 0
.
.
----- end of module rb count -----

```



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Agenda		
• 10:00am	Gathering and Introduction	Peter Pellerite
• 10:15am	Logic Design & Verification	
	– MC / MH / RB / Shader / Texture	Ken Correll
	– Display / VIP / BIF	Mark Fowler
	– PA/SC/VGT/CP/RBBM	Lili Sinclair
• 11:15am	Full Chip Validation	Mike Mantor
• 11:35am	Performance Validation Plan	Christeen Gray
• 12:00	Lunch Break	Allen Gallotta
• 1:00pm	Software Update	
	– BIOS / 2D	Liang Shen
	– Multimedia	
	– DirectX / OpenGL	Peter Pownall
	– Compiler	
• 2:00pm	IP Update	Raj Verma
• 2:15pm	Chip Integration / Pads	Frank Hering / Sam Huynh
• 2:45pm	Physical Design Update	Joe Grass
• 3:15pm	Break	
• 3:30pm	Program Overview (Summary)	Peter Pellerite

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[Date Time]

R400 Multimedia

- Overview
- TV Out
- Video Capture
- Overlay
- Video Acceleration
- MM Shader
- Risks

June 14, 2017

Overview

- At this time there are 8 full time engineers (4 of them are seniors) working on R400 in MM.
- All design documents and bringup plans are now complete.
- Capture team begins coding this week as per schedule.
- Shader schedule has moved out about 4 weeks, Overlay schedule has moved in about 4 weeks.
- Verification - Verification has been done on IDCT, FDCT, MC frame picture forward prediction, all texture formats needed by MM, with linear interpolation, and 20 new MC modes for WMV9. Also 2 tests have been written for real time queue support but not yet verified.



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TV Out

- One full time developer started coding in mid december.
- Software documentation completed 11/29/02
- Coding complete 01/31//03
- Risks – Relatively low risk. Not much work. Support new BIOS structure, support new DAL interface, R400 class object implementation, add SECAM support.



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Video capture

- Video capture development begins this week, as per schedule. Only design and documentation work has been done to date.
- Coding complete 03/21/03
- Risks –
 - Relatively low risk. Not a lot of work. Most of it is for AIW only, so not needed for first graphics only boards. RTS video port flipping, Update MMLIB and VPLIB with R400 register definitions, Update de-noise algorithm and port to R400 shader.
 - Strong dependency on the availability of good boards with video input.
 - This team has a lot of involvement with new AIW product introductions. Lots of maintenance work and resource conflicts.



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Overlay

- One full time developer since late September.
- Design doc complete 12/06/02
- Basic graphics features coding complete 03/17/03
- All features (including AIW live TV) coding complete 04/24/03
- SW testing complete 05/06/03
- Comments –
 - Good news. The overlay schedule has moved in by about 4 weeks. The milestones have been coming in ahead of schedule. The original schedule was just overly conservative.



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Video Acceleration

- One full time developer started in late September.
- Design doc complete 12/06/02.
- Some significant structural changes are being made to the driver at this time. MVALIB/VHDLIB. A re-architecture to isolate the ASIC dependent code and shader code. The intent is to release this new architecture on R300 cores in 7.84. This will remove it as a risk item for R400. This work is now checked in. MM QA has done a test pass and all but 2 issues have been fixed, so this work is basically done.
- Basic features (MPEG decode/encode) coding and testing complete 04/21/03
- WMV 8/9 coding and testing of DXVA interface complete 03/28/03
- MPEG4 coding and testing of DXVA interface complete 05/22/03



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MM Shader

- Design work completed. Bringup plan completed.
- Decode – testing complete: 03/31/03 (was 03/03/03)
- Encode – testing complete: 05/13/03 (was 04/08/03)
- Overlay – testing complete: 04/18/03 (no change)
- WMV – testing complete: 06/30/03 (was 06/04/03)
- Comments – 4 week slippage. Attributed to delays in integration with new MVALIB architecture and adapting to SSM interface changes. This is pretty severe and we are looking for ways to recover some of this time.



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Risks

- It has been realized that upsampling 420 to 444 for the overlay will cause artifacts. A new gradient filter is being added to the shader to compensate. Likely performance and visual impact. Work is ongoing on this issue.
- No design yet for bandwidth sharing.
- We don't yet have a synchronized schedule with the Cobra team.
- We still need to produce an IKOS plan.



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Contents

- R400 BIOS Development
 - BIOS Progress
 - BIOS Verification Status
 - BIOS Risks and Plan
- R400 2D Display Driver Development
 - 2D Driver Progress
 - 2D Driver Verification Status
 - 2D Driver Risks and Plan
- R400 3D Graphics Driver Development
 - 3D Driver Progress
 - 3D Driver Verification Status
 - 3D Driver Risks and Plan
- Some Snapshots

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R400 BIOS Progress

- New BIOS Architecture = Command Decoder + BIOS Tables
- Command Decoder
 - Macros: 20 macros implemented and tested; 4 more macros identified, but currently do not think they are required (set as low priority tasks)
 - Commands: 34 commands implemented and tested; 10 more commands identified, but currently do not think they are required (set as low priority tasks)
 - Mechanisms: 4 required mechanisms implemented and tested
- BIOS Tables
 - 76 BIOS tables are spec'ed out and need to be implemented and tested on IKOS before A11 back
 - VGA BIOS for IKOS bringup is ready
- BIOS Engineering build process is implemented
- BIOS utility is under development

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R400 BIOS Verification

- Command Decoder Coverage Test

Test Category	Test Result (01/14/03)		
	PASS	FAIL	%PASS
Move/Alignment Tests	20	4	83%
ALU Tests	20	8	71%
Control Command Tests	19	8	70%
Total	59	20	75%

- Detailed IKOS BIOS Test Checklist is created

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R400 BIOS Risks and Plan

- Risks
 - Amount of testing on IKOS is huge due to new BIOS architecture
 - Timing critical implementations can not be verified until ASIC back
- Plan
 - Categorize R400 BIOS tasks with proper priority and verify them on IKOS in a proper order
 - Using existing ASIC (R300) to verify timing critical implementation

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R400 2D Display Driver Progress

Component	Review	Critical			High			Medium			Low			Total
		Q	A	FA+	Q	A	FA+	Q	A	FA+	Q	A	FA+	
CMMQS	Last Review	0	0	8	1	4	3	7	1	2	2	1	0	29
	This Review	0	0	8	0	2	6	7	1	2	2	0	1	29
CAE	Last Review	0	2	2	0	1	3	2	0	1	1	0	0	12
	This Review	0	0	4	0	2	3	2	0	1	1	0	0	13
DALGXO	Last Review	0	3	10	7	7	19	21	3	3	7	1	1	82
	This Review	0	0	13	1	5	25	24	3	5	8	0	2	86
2DNTx	Last Review	0	1	17	2	5	8	4	0	4	5	0	0	46
	This Review	0	0	18	0	4	13	5	0	4	5	0	0	49
2D% ₂	Last Review	0	0	0	3	1	4	10	0	5	3	0	2	28
	This Review	0	0	0	0	0	6	13	1	5	3	0	2	30
Subtotal	Last Review	0	6	37	13	18	37	44	4	15	18	2	3	197
	This Review	0	0	43	1	13	53	51	5	17	19	0	5	207
Summary	Last Review	0%	14%	86%	19%	26%	54%	78%	6%	24%	78%	9%	13%	
	This Review	0%	0%	100%	1%	19%	79%	78%	7%	23%	79%	0%	21%	
	Progress	0%	-14%	14%	-18%	-7%	23%	0%	1%	-1%	1%	-9%	8%	

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R400 2D Driver Verification

- DDT has been revived and enhanced to run with QS-EMU
(Note: "Unknown" are still under run and will affect overall PASS percentage)

M	Test Group	# Cases	Test Result (01/10/03)	
			PASS	FAIL
640x480x32	BitBlt	242	Unknown	
	DrawIcon	1	1	0
	SetDIBits	1	1	0
	StretchBlt	13	Unknown	
	Text	23	14	9
	Drawing	10	9	1
	Poly	6	6	0
	Region	6	6	0
	Shape	7	7	0
	Summary	309	81.48%	18.52%

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R400 2D Driver Risks and Plan

- Risks
 - R400 DAL/GXO implementation can only be verified on IKOS
 - Bandwidth sensitive tasks can not be verified until ASIC back
- Plan
 - Using the small (5M) IKOS box to start DAL/GXO testing ASAP (only MC/BIF/DC/MH/SI blocks are required)
 - Dump more 2D packets for h/w teams testing
 - Profiling of 2D driver with various benchmarks is under way; results will be used for performance tuning
- Open Issues
 - Two new PM4 packets: ALPHABLEND and AAFONT were implemented by h/w; but testing was failed

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R400 3D Graphics Driver Progress

- Compiler
 - Major critical functionalities are implemented, except for wildcarding, OGL2 IL instructions, and more renderstates support
 - Bug fixing has been one of the major activities: # of open bugs has been kept small
 - Optimization is started and is the new focus recently
- SSM
 - Added support for Flat Shading, Cylindrical Wrapping, and Cubemap
 - Implemented vidmem alloc/free tracking and eviction mechanism
 - Added AbstractState for Two Sided Lighting, Pixel Fog, and Denormalized Texture Coordinates
 - More texture formats and texture filtering support
 - High order surface support design has started

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R400 3D Graphics Driver Progress (cont.)

- D3D
 - Completed Cubemap and Pixel Fog
 - Vertex Shader 2.0 implemented, with bugs filed to compiler
 - Debugging various test failures; progressing on DXn SDK Apps
- OGL
 - Cubemap and 3D Textures are working properly
 - Testing of Point AA and Line AA is complete
 - Debugging various test failures; progressing on OGL Conformance Tests

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R400 3D Driver Verification

- SSM/Compiler
 - Preliminary result with SSMClient2_33323 (11/26/2002) and emulator 12/20/2002 release (note: this is an early, incomplete run with emulator hangs and some improper golden images; re-run is under way)

Test Name	#Cases	Test Results				
		PASS	FAIL	ERR/HANG	UNKNOWN	%PASS
SSMClient	6734	722	221	5791	0	10.72%

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R400 3D Driver Verification (cont.)

- D3D Driver
 - Verification Tests

Test Name	#Cases	Test Results with Emulator CL#75526 (01/10/2003)					Note
		PASS	FAIL	ERR/HANG	UNKNOWN	%PASS	
SimpleD3D	535	448	81	6	0	83.74%	4 errors are false
DX8 Shader	936	936	0	0	0	100.00%	~20 texture instructions not included
DX9 Shader	1665	1539	83	43	0	92.43%	not all included, esp. 3.0 shader inst
FuncTest	1818	389	799	628	0	21.42%	preliminary results; under review

- DXn SDK Apps

DXn	PASS		FAIL		ERROR/HANG		UNKNOWN		Total
	#	%	#	%	#	%	#	%	
7	14	51.85%	4	14.81%	9	33.33%	0	0.00%	27
8.1	7	28.00%	9	36.00%	6	24.00%	3	12.00%	25
9	6	22.22%	8	29.63%	13	48.15%	0	0.00%	27

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R400 3D Driver Verification (cont.)

- OGL Driver

- OpenGL Conformance Tests

Passed		Not Run		Failed		Crashed		Hung		Total
#	%	#	%	#	%	#	%	#	%	
56	70.89%	0	0.00%	18	22.78%	1	1.27%	4	5.06%	79

- OpenGL Red Book Apps

- Smooth - PASS
 - Alpha - PASS
 - Checker - PASS
 - Light - PASS
 - Scene - PASS
 - Texgen - FAIL
 - Teapots - PASS

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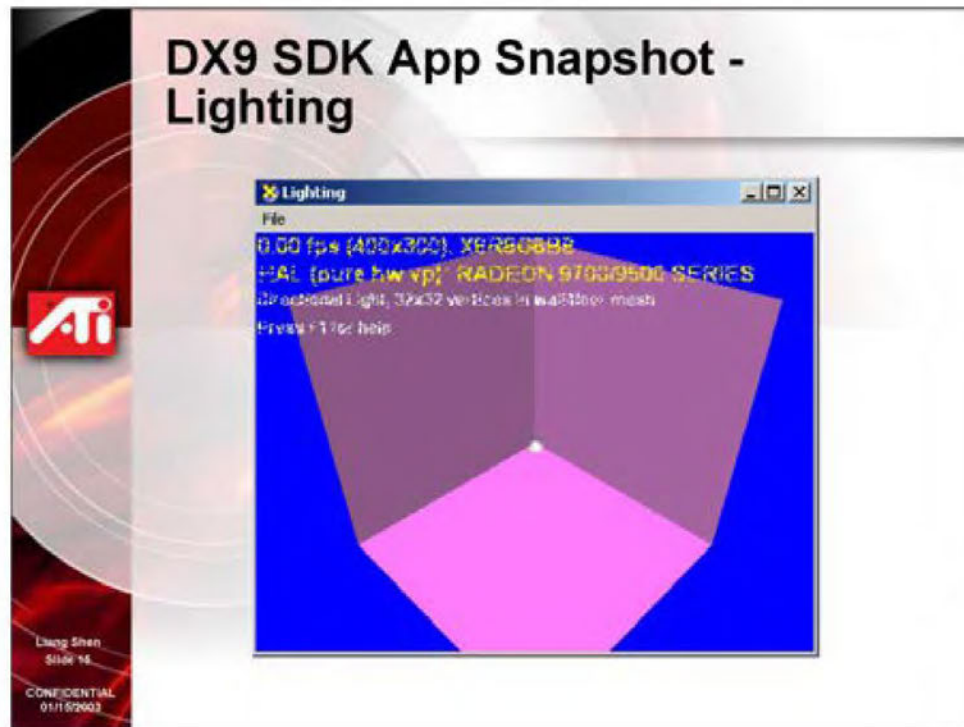


R400 3D Driver Risks and Plan

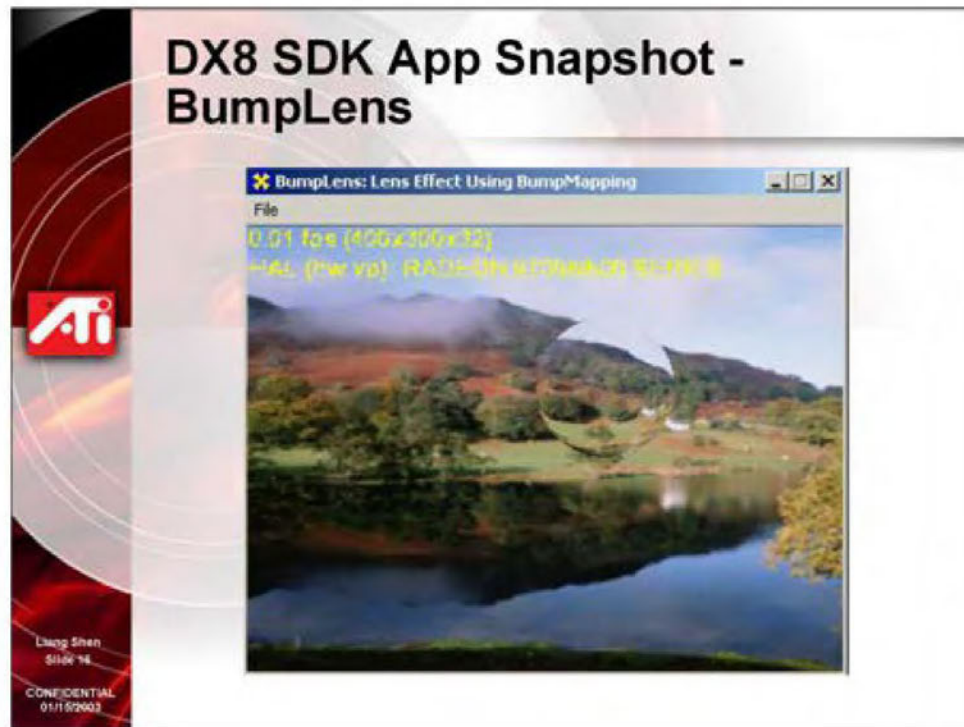
- Risks
 - Test Coverage of 3D Component Test Suites
 - Compiler and StateCache performance is not yet known
 - Emulator issues and feature completeness are critical for s/w development
- Plan
 - Completing development of the following planned test suites for IKOS by 2/28
 - Emphasizing more on s/w testing and complete the following s/w verification milestone before s/w IKOS starts (3/16)
 - SSM/Compiler: pass all SSMClient test suite except for branching
 - D3D: 100% pass of DX7 and DX8 shader test suites and func tests; 90% pass of DX9 shader test suites and func tests
 - OpenGL: pass all red book apps and OGL applets; at least 80% pass of WHQL Test Set, Conformance Test Suite, and ATI's Quickcheck Test Suite
 - Developing driver optimization and performance tuning plan for delivery at end of February.

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The slide features a vertical red bar on the left side. Within this bar, the ATI logo is positioned in the middle, and at the bottom, there is a small text block containing the name 'Liang Shen', the date '5/16/04', and the word 'CONFIDENTIAL' followed by the number '01/15/2003'. The background of the slide is white with a large, faint, circular graphic element in the center.

R400 Snapshots Web Page

Other snapshots are available at
<http://cvfsvr02/tcswfsr01/R400/snapshots.html>
and new ones will be added when available

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IP – Virage

- As of last evening we received the final Compilers from Virage
 - These also include the customization of power rings
 - IKOS models and Bit Masking fixes need to confirmed
 - Expect an array reduction from netlist 3.0
- Virage has been contracted to produce the JPC
 - This provides the connections tile's Star Processor to the test controller.
 - Delivery is expect January 17, 2003
- Validation of Star is in progress on the tile level
- Still need to move the Fuse to one area, but need a floorplan (this will happen in next netlist)



Front Imaging

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Virage - Backend and test issues

◆ Operation and Test Flow

- Operation, Test, and Engineering met with Virage and Virage went through the production flow
- Virage also pointed up problem area were other customers have gotten themselves in trouble
- ASE has been selected to take on the repair
 - The are suggested vendor of Virage and one of ATI's primary vendors
- Operations will be providing a plan and schedule 1st week of February

◆ Virage Star Test Chip Shuttles

- FSG – Wafer out January 24
- LowK – Tape out First part of February



Front loading

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IP – Analog

- ◆ R400 is going to use the A5 DAC with the internal output muxing for TV signals
 - ◆ Now have the pad space due to core size
 - ◆ Saves components and electrical issues on board
- ◆ Temperature Sensor has been deferred to a later chip
 - ◆ Risk of not getting it done in time
 - ◆ Question remain to what is needed
 - ◆ Size concerns for R400
- ◆ Analog group is committed to looking at MPLL to provide a glitches power up and transition at 1.2Ghz speeds.
- ◆ Need to explore if a 5X1 or 3X2 aspect block of PLL is better for layout.



Front Covering

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Pads and Pad ring

- ◆ Final Pad Ring is being created by Greg
 - ◆ All major issue have been resolved
 - ◆ Pad interface to update Memory Controller will be completed by the end of January
- ◆ DVO pads
 - ◆ A derivative of the new memory pad will create for this interface
 - ◆ This will only support a <1.8 Volt interfaces
 - ◆ Board level translators would have to be used if the parallel Rom is every used. (This is a backup to Serial Roms anyways)
 - ◆ An RV part would have an issue with zoom video, but the same issue would on the memory



Front loading

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Packaging and Boards

- ◆ R400 will use the same 40X40 ball package as R300
 - ◆ Stiffener will not be part of the package because corner ball will be removed. This solves the planarity issue
 - ◆ Laser fuses will allow ID'ing of parts
 - ◆ This allows final test to determine speed, workstation and so on.
- ◆ 2 other packages will be created to allow for ½ harvested parts.
- ◆ Package Routing experiment to begin once final pad out is completed.
- ◆ Board Team is looking at ball out and beginning board memory routing studies.



Front View

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System Integration

- ◆ Validation continues on the clock blocks
- ◆ Board and Board marketing groups committed to reviewing strapping and chip id's for all variations.
- ◆ All smaller blocks have been merged into the SI block for layout
- ◆ Debugging various chip level issues rising out of Toronto validation
- ◆ Need final floorplan to hook up some top level signals



FROM: [illegible]

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Netlist Generation

• Netlist 3

- Release on January 2, to Physical Design and Hardware emulation
- Some minor issues have been found and for the most part they have been address for the next time
 - Assign statement
 - Constant assignment
 - Virage compiler revisions



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Netlist Generation

• Netlist 4

- Ground Hog Day! (Feb 2)
- Final AB, SP, VGT, PA, SC, SB_B Blocks
- Split TC
- Final Memory Controller Pad interface for DDR3
- Fuses migrate to SI block
- First pass look at DFT coverage over whole chip
- Various other Details such as FF interfaces, CRC, and so on



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Netlist Generation

• Netlist 5

- 1st week of March
- Final Top Level interconnect, including test
- Split of RB block due to instance count
- Final Tile configurations
- Feedback from netlist 3.0 used in synthesis
- Next wave of final blocks



Final Netlist

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DFT

- ◆ Continue development of Test controller
 - Needs SOCBIST Operation Control
 - Needs Interface to RBBM
 - When Virage deliver JPC, this needs to be incorporated
 - Validation of Controller is beginning, but a formal plan needs to be finalized
- ◆ SOCBist
 - Project is committing to this new technology
 - MH test case has provided 99.46% coverage with impressive short amount of patterns
 - Netlist 3 frozen blocks will run through this week.
- ◆ Virage
 - Tile validation has begun and some typos have been discovered
 - Full validation will begin with the delivery of JPC

Diagnostics

- ◆ Since the return of RV280 and RV250 issues work on R400 has grinded to a halt
- ◆ There are basic tests ready for all 3D function
- ◆ Complicated and stress tests area the next thing on plate and on hold.
- ◆ Waiting for IKOS to start debugging
- ◆ Toronto diagnostics have only 1 junior person working on them.
- ◆ The Toronto diags will be the critical path since they are required first in IKOS



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Hardware Emulation

- ◆ Netlist 3.0 has made rapid progress in IKOS
- ◆ The graphic-less chip is now running on the IKOS box
 - ◆ We have preformed configuration cycles
 - ◆ There were some issues with clocks that have resolved
 - ◆ We are now working on register reads
- ◆ Full chip is 25.7 million IKOS gates!
- ◆ In order to proceed to get memory working, netlist 4 is need. We may try using RTL compile to speed this along.



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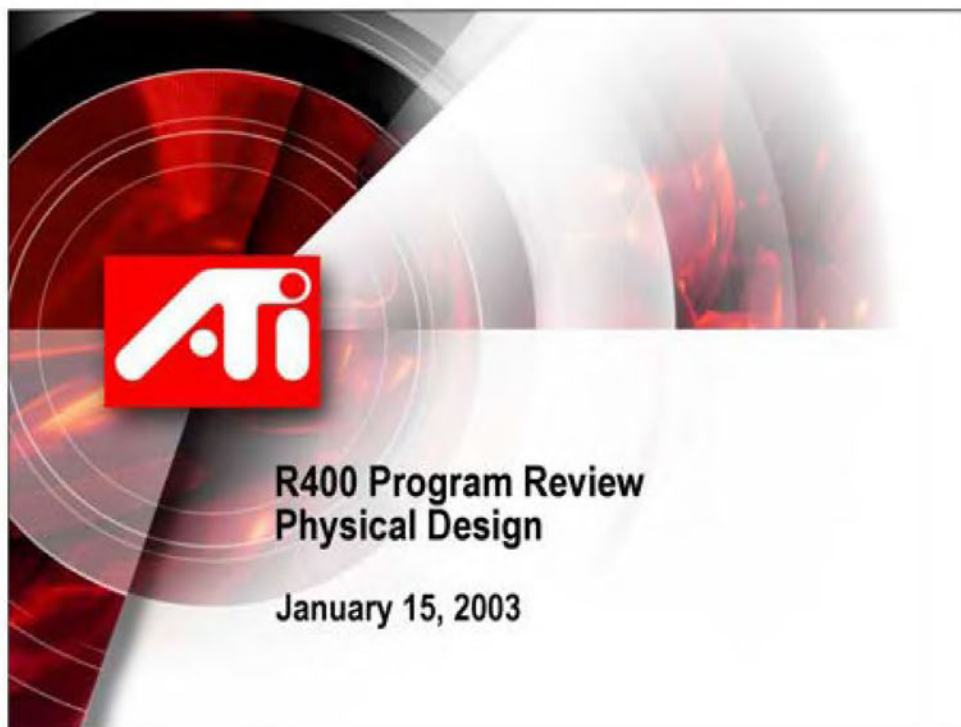


Issues

- ◆ Need to deal with packaging and memory interface modeling issues to get 600Mhz
- ◆ Need to come up with a limited harvesting plan
 - ◆ The full blown solution hurts my brain
- ◆ Timely Feedback from Physical Design is now becoming very important.
- ◆ Resolving final issues with Pad and I/O cells will allow a number of items to proceed
- ◆ A significant number of netlist 3 issues are in the DC block and need to resolved.

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Previous Physical Design Activities

- Tool Evaluations
- R400 Block Testcases for Netlist 2.0
- Tile Netlist Generation Flow
- Initial Floorplan Effort
- Netlist 3.0 Related Work



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Tool Evaluations

- PC replacement – FE and PKS
- Pbopt replacement – PKS
- Wroute replacement – nanoroute
- Motivations:
 - Decrease iteration times
 - Move away from gcf - removes the need to run both pearl and PT
 - Automatic SI fixing – decrease manual SI fixing iterations



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Resulting Tile P&R Flow

- Setup
- FE (placement)
- scanStitch.SEonly (for high fanout nets)
- Clockwise (cts)
- scanStitch.noSE (for SI)
- PKS (logic restructuring and initial IPO, ipo0)
- Nanoroute
- PKS (ipo1)
- Nanoroute1
- QX (extract)
- PT (timing)
- Calibre (LVS/DRC)
- Celtic (SI)

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Tile Flow Risks and Issues

- Tentatively confident on the flow, but identifying fall backs to minimize schedule risks.
- If FE doesn't do a good enough job on some R400 tiles → fall back is to use PC
- If nanoroute causes too many DRC violations → fall back is to use wroute. Currently identifying DRC issues and finding fixes
- PKS – don't have a fall back for this unless willing to deal with the pain of gcfs
- Need to rework timing targets and support scripts to work with Primetime instead of Pearl.
- Currently have a pipecleaner tile to flush out flow issues

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R400 block testcases for netlist 2.0

- Three tiles should have netlist + dspf by the end of the week (mh, sc, dc) for wireload generation. Delay due to Simplex library issues for virage memories.
- sp has a timing/constraint issue and didn't make it through the flow
- Testcases are not realistic compared to final tiles (1:1 aspect ratios, clock period relaxed, no toplevel influence, etc), so will affect wireload quality.



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Tile Netlist Generation Flow

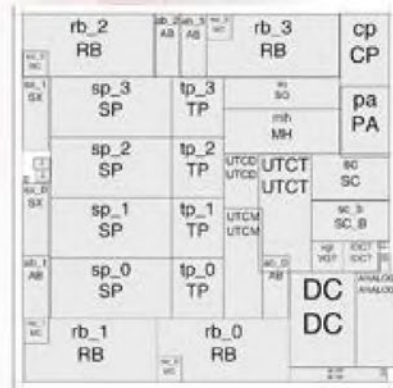
- Use netlist 2.0 to debug the tile netlist generation flow
- FE hang during placement stage → workaround after netlist hacking (1'b0, assigns, etc)
- FE hang during commitPartition stage → worked with Cadence and found a fix, finished validation this morning
- commitPartition problem affected netlist 3.0 tile netlist generation



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Initial Floorplan Effort

- Worked with Front End to iterate on netlist 2.0
- Based on netlist 2.0 Front End provided a netlist 3.0 starting point.

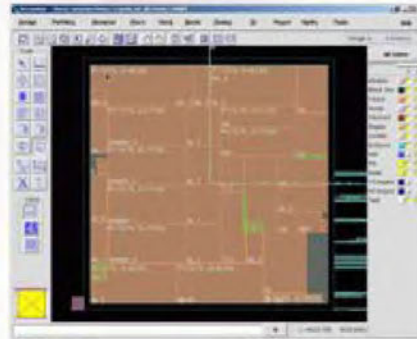


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Netlist 3.0 Work

- Took Front End guides through tile generation flow
- By-passed commitPartition problem in order get first cut at tiles
- Generated initial tiles with proper aspect ratios and areas
- Split TC into 3 blocks for floorplanning purposes
- Bloated pad ring due to chip area increase.
- Netlist 3.0 core size: 14.8mmx14.8mm
- Netlist 3.0 die size: 15.6mmx15.6mm



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Current Physical Design Activities and Short Term Goals

- Wrap up tool evaluations and netlist 2.0 testcases – will have most if not all issues wrapped up this week.
- Debug new tile flow – current estimate is 2 weeks
- Netlist 3.0 tile P&R – 2 – 3 weeks depending on tile
 - Push tiles through the flow, goal is to get as many tiles routed, extracted, and timed as possible.
 - Provide FE team with feedback (local congestion problems, timing, routability, etc)
- Debug top level flow, improve tile deliverables (incremental tile releases), many things currently missing due to commitPartition problem – first incremental release this week (rel_3.0B)
 - Sram/pin placements
 - Repeater allocation
 - Metal6 obstructions
- Start toplevel P&R activities – dependent on getting top level flow clean – rel_3.0B is a starting candidate
- Initial floorplan efforts for netlist 3.0

10
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Netlist 3.0 tile info

tile name	instance count	blocks	reuse?	FE owner	email	show	FE owner	email	show
AS	115,005	as	yes	4	George Marks	geormar@ati.com	8044	Paul Vella	pvella@ati.com
BF	132,884	bf_top	?	?	?	?	8046	Thamiruthu	thamiruthu@ati.com
CP	173,323	cp	?	?	Kaunurti R	kaunurti@ati.com	8027	Frank Lipton	flipton@ati.com
DC	369,608	dc	?	?	Joe Grass	jgrass@ati.com	8004	Li Sinclair	lsin@ati.com
MC	24,820	mc	yes	4	?	?	?	Bob Bloomer	bbloomer@ati.com
MR	288,465	mr	?	?	Theresa Bai	tbai@ati.com	8069	Peter Runstadler	prunstad@ati.com
PA	180,041	pa	?	?	Shagufa Siddique	shagufa@ati.com	8443	Bob Harrison	bharrison@ati.com
RB	492,570	rb	yes	4	Lari Vello	lari@ati.com	8034	Jay Wilkerson	jaye@ati.com
SC	181,550	sc	?	?	Shankar Nagarajan	snagar@ati.com	8045	Donald Lee	donald@ati.com
SC_6	172,307	sc	?	?	Orshan Radu	oradu@ati.com	8372	Randy Ramsie	ramsey@ati.com
SP	408,333	spader	yes	4	Gary Kuo	gkuo@ati.com	8021	Andi Skende	skende@ati.com
SQ	119,436	sq	?	?	Shankar Nagarajan	snagar@ati.com	8390	Steve Carsten	scarsten@ati.com
SX	47,581	sx	yes	2	Sharanthi Ramdass	sharanthi@ati.com	?	Doug Duncan	daug@ati.com
TC0	345,209	tc0	?	?	Maneesh Bhote	mhbote@ati.com	8382	Steven Mitsu	smitsu@ati.com
TC1	245,905	tc1	?	?	?	?	?	Nick Kocuk	nkocuk@ati.com
TC2	369,434	tc2	?	?	Darryl Greco	dgreco@ati.com	8076	Ray Manapat	manapat@ati.com
TP	194,868	tp	yes	4	Anil Tappag	atappag@ati.com	8443	Suba Duranjan	subad@ati.com
TBN	138,043	tbln, rbln, vgl	?	?	?	?	?	Tusha Shah	tusha@ati.com
top level	54,495	ic, cgm, rc, si, analog	no	?	Mitsuhisa Matsuo	m-matsuo@ati.com	8003	Eric Newman	enewman@ati.com

- Have one new hire starting Thursday
- Some people might free up from the respin effort – will know in a few weeks
- Will probably assign some people to work on multiple tiles

11
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Risks

- Top level flow and issues – runtime and reuse
- Tile flow – have fall backs for most issues
- Tile size – impact on top level floorplan. Would prefer to get TC breakup and pad ring change earlier to get P&R started on MC and TC blocks.
- Tile timing closure
- Top level P&R and timing closure



12

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R400 Review Action Summary

- Program – Next tentative review date is on February 12th
- Last Month
 - R400 Software
 - Emulator release tied to software tests: Mark Fowler attending SW meetings
 - AJW schedule: Target still 1 month after graphics product
 - Board VIVO closure for debug: Planning with Board Management
 - R400 Hardware
 - DDR DVO at 480MHz needs to drop 3.3V Support: Yes, drop but still need to discuss requirements more thoroughly (see this month's review actions)
 - SP will need to add larger buffer: Buffer size not upsizing
 - Need generic fix to scripts for timing fix ? Ongoing fixes being made
 - Chip Integration
 - Power issues with latest memories (4x higher) – Virage was broken
 - Operations involvement on Virage fuses, harvesting fuse: Kick-off meeting has occurred (1/09/03)
 - Pad ring coordination meeting: Done
 - Physical Design
 - Feedback from Netlist 3: Netlist 3.0 delivered 1/02/03 – Mark Lee working
 - Performance
 - RTL to IKOS ? Frank Hering is continuing to work this with Ron White

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R400 Review Action Summary

- **This review:**
 - **R400 Software**
 - Plan support for packet dump capture – Liang S / Phil R.
 - Quality goal needed for conformance of compression/coherency code - ?
 - IKOS Meeting with Ron White and software team – Frank Hering
 - **R400 Hardware**
 - SDR 3.3V support on DVO port (requirements) – Frank H. to call meeting
 - RB break-up for Netlist delivery (NL4.0 vs NL5.0) – Peter P. to call meeting
 - Code coverage analysis on all blocks – Mark F., Lili S., Mike M.
 - DC dependency on MH bug closure (Ken Correll to drive MH closure, added resource)
 - DC instance count high – Lili S./Frank H. to work with Mark Lee
 - SQ test coverage review – George V. calling review meeting
 - **Performance**
 - PA performance registers – Dan Clifton to contact Allen G. for use of them
 - GC testbench for better performance data -
 - Contractors to run/analyze tests – Allen G. to speak with Bob Drebin
 - **Chip Integration**
 - Build test package (w/o corner balls) to test theory on shear problems on R300
 - Plan to over-ride laser fuse for chip personality – Frank H. / Peter P.
 - Diagnostics for Toronto usage – Liang S. / Peter P. to follow up.
 - **Physical Design**
 - Feedback from Netlist 3 needed
 - Tile size issues

3
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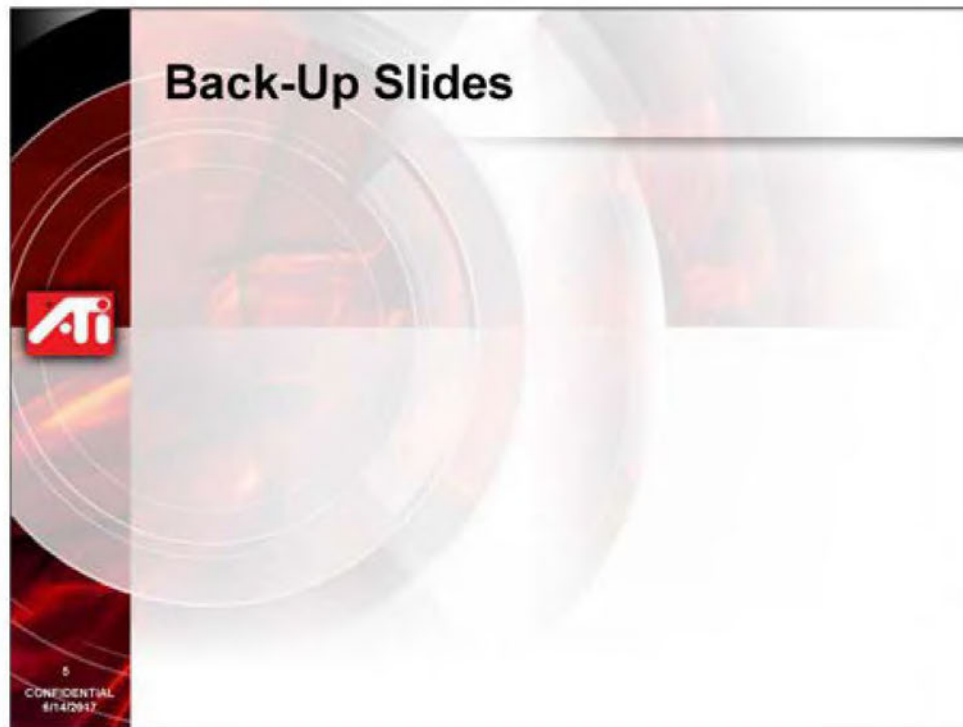
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High Level Schedule

Task	Original	Last FC	Current FC
Emulator Test template Complete	01-18-02	01-18-02	Complete
GC Emulator integration - 1 triangle	02-22-02	02-21-02	Complete
Core Emulator pixel / shader tests run	03-15-02	03-19-02	Complete
Block Testing Begins	04-16-02	05-01-02	Complete
GC/Chip integration Start	05-17-02	05-15-02	Complete
Simulate 1 Triangle / Emulator ready for SW	06-15-02	07-01-02	Complete
First Syntheses (n-1)	07-12-02	08-03-02	Complete
Verilog Feature Complete	09-16-02	10-31-02	Complete
Second Synthesis (n)	09-23-02	10-04-02	Complete
IKOS Emulation start	10-11-02	01-13-03	Complete
Third Synthesis	11-01-02	01-02-03	Complete
Early block delivery starts	11-08-02	12-16-02	Complete
IKOS Emulation (w/ Software) begins	11-11-02	01-16-02	03-16-03
RTL Freeze / Final Netlist (Gate level ECO only)	11-15-02	01-31-03	05-01-03
A11 Base Layers Tapeout	01-10-03	03-28-03	06-26-03
A11 Metal Layers Tapeout	01-24-03	04-11-03	07-10-03
First Samples for Engineering		06-25-03	09-12-03
A12 Tapeout		07-31-03	10-17-03
A12 Samples for Engineering		09-04-03	11-28-03
R400 Customer Samples		09-11-03	12-05-03
Product Delivery		10-04-03	12-29-03

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R400 Area Estimate (Q.13)

Current Pad separation (um)	50		
Current Pad height (um)	350		
Scribe	0.18		
Core inside		14.90	11.77
Total inside		15.78	12.65

ATI Ex. 2063
IPR2023-00922
Page 150 of 150